

TPS53015 4.5V~28V 入力、D-CAP2™、同期整流降圧型コンバータ、PGOOD 付き

1 特長

- D-CAP2™モード制御
 - 高速過渡応答
 - ループ補償に外付け部品が不要
 - セラミック出力コンデンサに対応
- 初期精度が高い基準電圧 (±1%)
- 広い入力電圧範囲: 4.5V~28V
- 出力電圧: 0.77V~7V
- ローサイド $R_{DS(ON)}$ の無損失電流センシング
- 固定ソフトスタート時間: 1.4ms
- シンクなしのプリバイアス付きソフト・スタート
- スイッチング周波数: 500kHz
- サイクル単位の過電流制限制御
- 自動スキップ Eco-Mode™により軽負荷時に高効率を実現
- パワー・グッド出力
- OCL、OVP、UVP、UVLO、TSD 保護
- 昇圧 PMOS スイッチ内蔵の適応型ゲート・ドライバ
- 温度補償された OCP、4000ppm/°C
- 10 ピン VSSOP

2 アプリケーション

- 広範なアプリケーション向けの低消費電力システムのポイント・オブ・ロード (POL) レギュレーション
 - デジタル・テレビ用電源
 - ネットワーク・ホーム・ターミナル
 - デジタル・セットトップ・ボックス (STB)
 - DVD プレーヤー / レコーダー
 - ゲーム機など

3 概要

TPS53015 デバイスは、シングル、適応型オン時間の D-CAP2™モード、同期整流降圧コントローラです。このデバイスを採用することで、各種機器の電源バス・レギュレータに対して、コスト効果が高く、外部部品数の少ない、低スタンバイ電流のソリューションを実現できます。TPS53015 の主制御ループは、外部補償部品なしで非常に高速な過渡応答が得られる D-CAP2 モード制御を使用しています。適応型オン時間制御により、高負荷時の PWM モードと、軽負荷時の Eco-mode™動作との間をシームレスに移行できます。Eco-mode 動作により、このデバイスは軽負荷条件時に高い効率を維持できます。また、POSCAP や SP-CAP などの低 ESR (等価直列抵抗) 出力コンデンサと超低 ESR セラミック・コンデンサの両方に対応できます。このデバイスは 4.5V~28V の入力電圧、0.77V~7V の出力電圧に対応しており、使いやすく高効率で動作します。

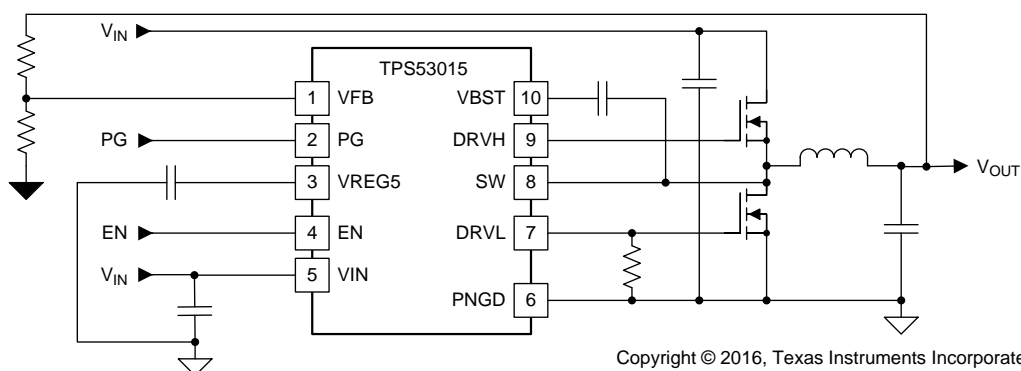
TPS53015 は、3mm x 3mm の 10 ピン VSSOP (DGS) パッケージで供給され、-40°C~85°C の周囲温度範囲で動作が規定されています。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
TPS53015	DGS (10)	3.00mmx3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

アプリケーション概略図



Copyright © 2016, Texas Instruments Incorporated



目次

1	特長	1	7.3	Feature Description.....	13
2	アプリケーション	1	7.4	Device Functional Modes.....	15
3	概要	1	8	Application and Implementation	16
4	改訂履歴	2	8.1	Application Information.....	16
5	Pin Configuration and Functions	3	8.2	Typical Application.....	17
6	Specifications	4	9	Power Supply Recommendations	20
6.1	Absolute Maximum Ratings.....	4	10	Layout	20
6.2	ESD Ratings.....	4	10.1	Layout Guidelines.....	20
6.3	Recommended Operating Conditions.....	4	10.2	Layout Example.....	21
6.4	Thermal Information.....	4	11	デバイスおよびドキュメントのサポート	22
6.5	Electrical Characteristics.....	6	11.1	商標.....	22
6.6	Typical Characteristics.....	8	11.2	静電気放電に関する注意事項.....	22
7	Detailed Description	13	11.3	Glossary.....	22
7.1	Overview.....	13	12	メカニカル、パッケージ、および注文情報	22
7.2	Functional Block Diagram.....	13			

4 改訂履歴

Revision B (August 2012) から Revision C に変更 Page

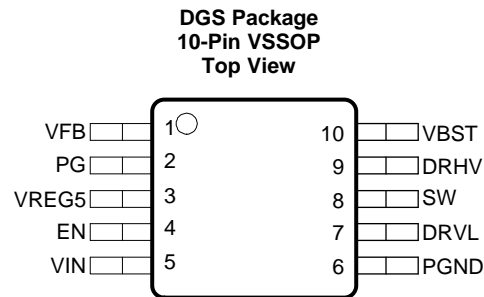
•	最新の TI ドキュメント標準に更新.....	1
---	-------------------------	----------

Revision A (July 2012) から Revision B に変更 Page

•	「特長」一覧で「可変ソフトスタート」を「1.4ms 固定ソフトスタート」に変更.....	1
•	「特長」一覧に「パワー・グッド出力」を追加.....	1
•	文書番号をリビジョン A からリビジョン B に変更.....	1
•	Changed from "SS" to "PG" in the Absolute Maximum Ratings table.....	4
•	Changed from "SS" to "PG" in the Recommended Operating Conditions table.....	4
•	Changed T _{SS} spec from "1.0 ms" to "1.4 ms" Typical.....	6
•	Changed T _{PGDLY} spec from "1.5 ms" to "1.2 ms".....	6
•	Changed T _{PGCOMPSS} spec from "2.2 ms" to "2.3 ms".....	6
•	Changed MIN t _{UVPEN} specification from "1.4 ms" to "1.7 ms".....	7
•	Changed TYP t _{UVPEN} specification from "1.7 ms" to "2.2 ms".....	7
•	Changed MAX t _{UVPEN} specification from "2.0 ms" to "2.7 ms".....	7
•	Changed soft-start time from "1.0 ms" to "1.4 ms" in.....	14
•	Changed adjusted reference to UVP delay timing from "1.7 ms" to "2.2 ms" in the section.....	14
•	Added section describing POWER GOOD operation.....	15

2012年7月発行のものから更新 Page

5 Pin Configuration and Functions



Pin Functions

PIN		I/O ⁽¹⁾	DESCRIPTION
NAME	NO.		
DRVH	9	O	High-side N-channel MOSFET gate driver output. SW referenced driver switches between SW(OFF) and VBST(ON).
DRVL	7	O	Low-side N-Channel MOSFET gate driver output. PGND referenced driver switches between PGND(OFF) and VREG5(ON).
EN	4	I	Enable. Pull high to enable converter.
PG	2	O	Open drain power good output.
PGND	6	I	System ground.
SW	8	I/O	Switch node connections for both the high-side driver and overcurrent comparator.
VBST	10	I	High-side MOSFET gate driver bootstrap voltage input. Connect a capacitor from VBST to SW. An internal diode is connected between VREG5 and VBST
VFB	1	I	D-CAP2 feedback input. Connect to output voltage with resistor divider.
VIN	5	I	Supply Input for 5-V linear regulator. Bypass to GND with a minimum 0.1- μ F high quality ceramic capacitor.
VREG5	3	O	Output of 5-V linear regulator and supply for MOSFET driver. Bypass to GND with a minimum 4.7- μ F high-quality ceramic capacitor. VREG5 is active when EN is asserted high.

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

		MIN	MAX	UNIT
Input voltage range	VIN, EN, SW	-0.3	30	V
	VBST	-0.3	36	
	(VBST - SW), VFB	-0.3	6	
	SW (10 ns transient)	-3.0	30	
Output voltage range	DRVH	-2	36	V
	DRVH - SW	-0.3	6	
	DRVL, VREG5, PG	-0.3	6	
	PGND	-0.3	0.3	
Junction temperature range, T _J		-40	150	°C
Storage temperature, T _{stg}		-55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to device GND terminal.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply input voltage range	VIN	4.5	28	V
Input voltage range	VBST	-0.1	33.5	V
	VBST - SW	-0.1	5.5	
	VFB	-0.1	5.5	
	EN	-0.1	28	
	SW	-1.0	28	
Output Voltage range	DRVH	-1.0	33.5	V
	DRVH - SW	-0.1	5.5	
	DRVL, VREG5, PG	-0.1	5.5	
	PGND	-0.1	0.1	
Operating free-air temperature, T _A		-40	85	°C
Operating junction temperature, T _J		-40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS53015	UNIT
		DGS (VSSOP)	
		10 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	109.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	31.2	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

Thermal Information (continued)

THERMAL METRIC ⁽¹⁾		TPS53015	UNIT
		DGS (VSSOP)	
		10 PINS	
$R_{\theta JB}$	Junction-to-board thermal resistance	54.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54.1	°C/W

6.5 Electrical Characteristics

 over operating free-air temperature range, $V_{IN} = 12$ V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{IN}	Supply current	V_{IN} current, $EN = 5$ V, $V_{VFB} = 0.8$ V, $V_{SW} = 0$ V, $T_A = 25^\circ\text{C}$		660		μA
I_{VINSDN}	Shutdown current	V_{IN} current, $T_A = 25^\circ\text{C}$, No Load, $V_{EN} = 0$ V, $V_{REG5} = \text{OFF}$		6.0		μA
VFB VOLTAGE and DISCHARGE RESISTANCE						
V_{VFBTHL}	Threshold voltage	$V_{OUT} = 1.05$ V, $T_A = 25^\circ\text{C}$	765.3	773.0	780.7	mV
TC_{VFB}	Temperature coefficient ⁽¹⁾	$T_A = 25^\circ\text{C}$	-140		140	ppm/ $^\circ\text{C}$
I_{VFB}	Input current	$V_{FB} = 0.8$ V, $T_A = 25^\circ\text{C}$	-150	-10	100	nA
VREG5 OUTPUT						
V_{VREG5}	Output voltage	$T_A = 25^\circ\text{C}$, 6 V < V_{IN} < 28 V, $I_{VREG5} = 5$ mA		5.1		V
I_{VREG5}	Output current	$V_{VIN} = 5.5$ V, $V_{VREG5} = 4.0$ V, $T_A = 25^\circ\text{C}$		120		mA
OUTPUT: N-CHANNEL MOSFET GATE DRIVERS						
R_{DRVH}	Resistance	Source, $I_{DRVH} = -50$ mA, $T_A = 25^\circ\text{C}$		3.2	4.7	Ω
		Sink, $I_{DRVH} = 50$ mA, $T_A = 25^\circ\text{C}$		1.4	2.4	
R_{DRVL}	Resistance	Source, $I_{DRVL} = -50$ mA, $T_A = 25^\circ\text{C}$		6.9	8.2	Ω
		Sink, $I_{DRVL} = 50$ mA, $T_A = 25^\circ\text{C}$		0.8	1.7	
t_D	Dead-time ⁽¹⁾	DRVH-low to DRVL-on		15		ns
		DRVL-low to DRVH-on		20		
INTERNAL BOOST DIODE						
V_{FBST}	Forward voltage	$V_{VREG5-VBST}$, $I_F = 10$ mA, $T_A = 25^\circ\text{C}$		0.1	0.2	V
SOFT-START TIME						
t_{ss}	Internal soft-start time			1.4		ms
POWER GOOD						
V_{PGTH}	PGOOD threshold	PGOOD LOW		84		%
		PGOOD HIGH		116		%
I_{PG}	PGOOD sink current	$V_{PG} = 0.5$ V		5		mA
t_{PGDLY}	PGOOD delay time	Delay for PGOOD in		1.2		ms
		Delay for PGOOD out		2		μs
$t_{PGCOMPSS}$	PGOOD comparator start-up delay	PGOOD comparator wake up delay		2.3		ms
UVLO						
$V_{UVVREG5}$	VREG5 UVLO threshold	VREG5 Rising		4.0		V
		Hysteresis		0.3		
LOGIC THRESHOLD						
V_{ENH}	High-level threshold voltage		1.6			V
V_{ENL}	Low-level threshold voltage				0.5	V
R_{EN}	EN pin resistance to GND	$V_{EN} = 12$ V	225	450	900	k Ω
CURRENT SENSE						
I_{TRIP}	Source current	$V_{DRVL} = 0.1$ V, $T_A = 25^\circ\text{C}$	14.3	15	15.8	μA
TC_{VTRIP}	V_{TRIP} Temperature coefficient	Relative to $T_A = 25^\circ\text{C}$		4000		ppm/ $^\circ\text{C}$
V_{OCL}	Current limit threshold	$R_{TRIP} = 75$ k Ω , $T_A = 25^\circ\text{C}$	234	336	424	mV
		$R_{TRIP} = 27$ k Ω , $T_A = 25^\circ\text{C}$	121	174	220	
		$R_{TRIP} = 6.8$ k Ω , $T_A = 25^\circ\text{C}$	35	50	63	

(1) Ensured by design. Not production tested.

Electrical Characteristics (continued)

over operating free-air temperature range, $V_{IN} = 12\text{ V}$ (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
ON-TIME TIMER CONTROL						
t_{ON}	On-time ⁽¹⁾	$V_{OUT} = 1.05\text{ V}$		250		ns
$t_{OFF(min)}$	Minimum off-time	$V_{IN} = 4.5\text{ V}$, $V_{VFB} = 0.7\text{ V}$, $T_A = 25^\circ\text{C}$		230		ns
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP trip threshold	OVP detect voltage	115%	120%	125%	
t_{OVPDEL}	Output OVP propagation delay				10	μs
V_{UVP}	Output UVP trip threshold	UVP detect voltage	63%	68%	73%	
t_{UVPDEL}	Output UVP delay			1		ms
t_{UVPEN}	Output UVP enable delay		1.7	2.2	2.7	ms
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature ⁽¹⁾		150		$^\circ\text{C}$
		Hysteresis ⁽¹⁾		25		

6.6 Typical Characteristics

$V_{IN} = 12\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

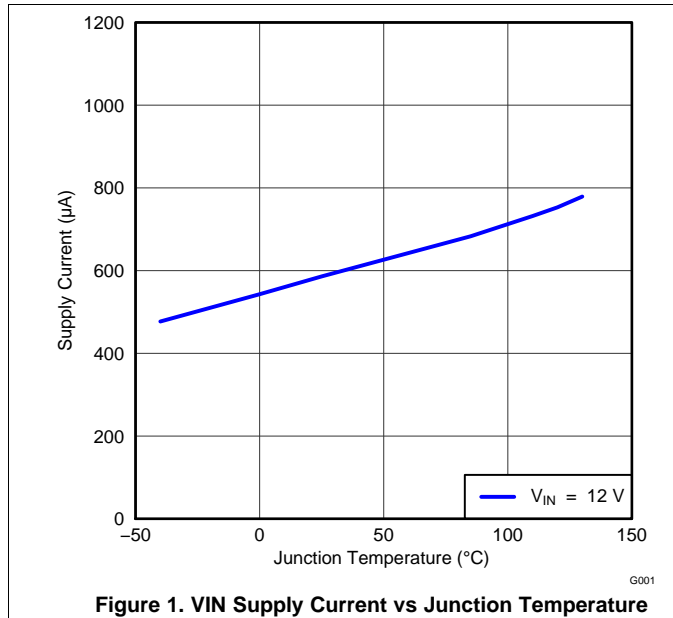


Figure 1. VIN Supply Current vs Junction Temperature

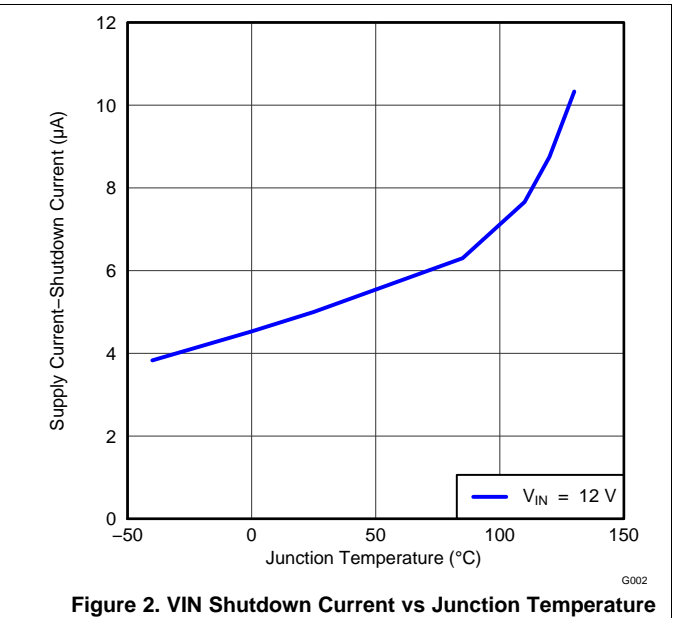


Figure 2. VIN Shutdown Current vs Junction Temperature

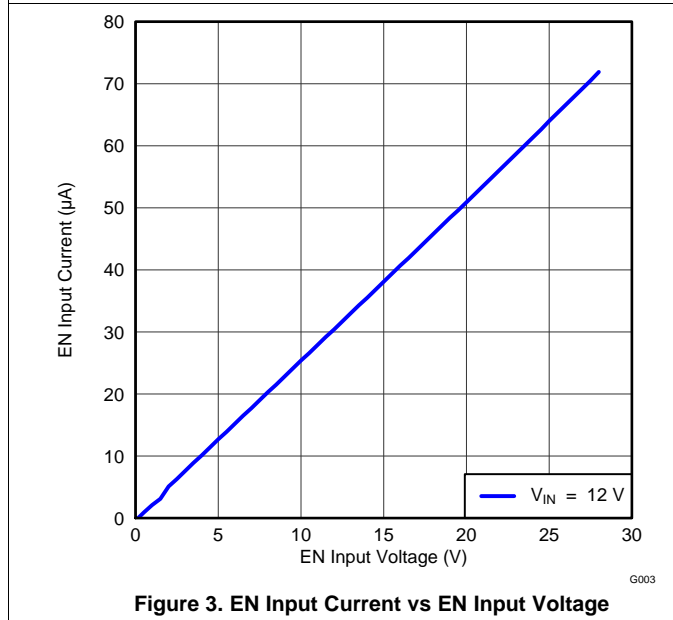


Figure 3. EN Input Current vs EN Input Voltage

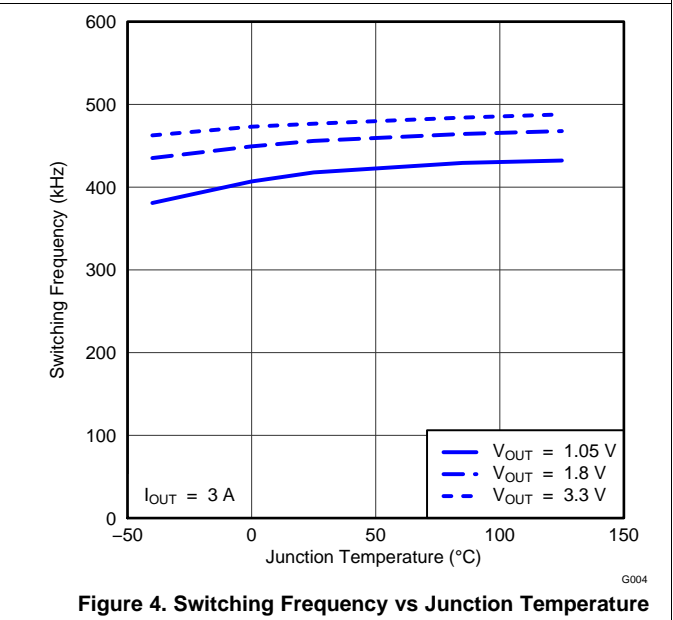
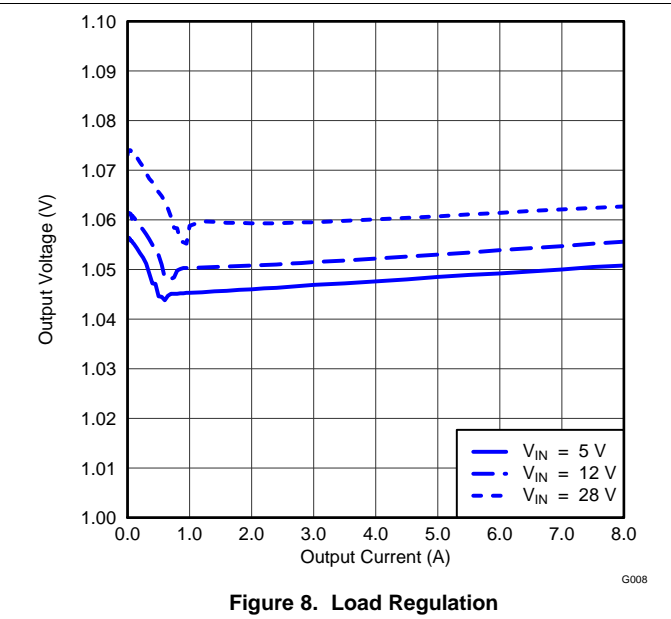
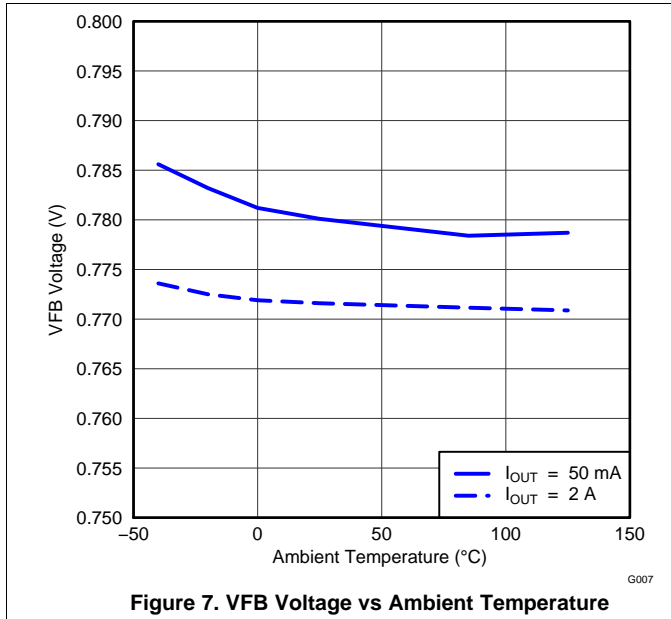
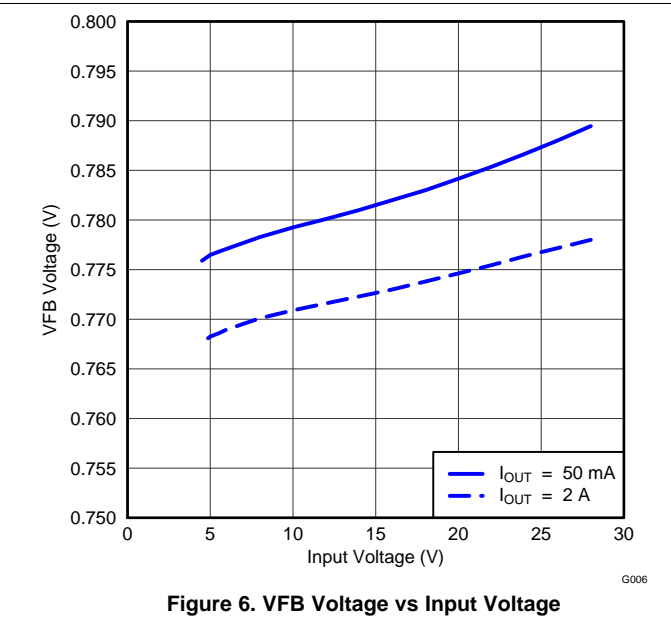
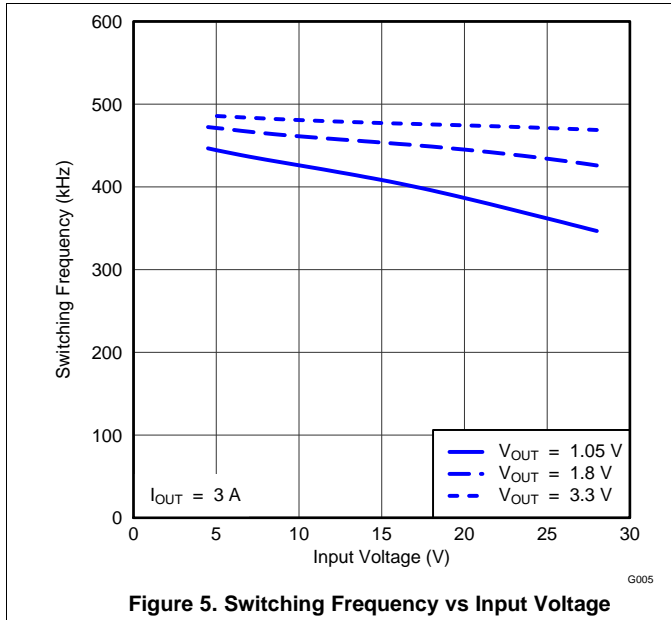


Figure 4. Switching Frequency vs Junction Temperature

Typical Characteristics (continued)

$V_{IN} = 12\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)



Typical Characteristics (continued)

$V_{IN} = 12\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

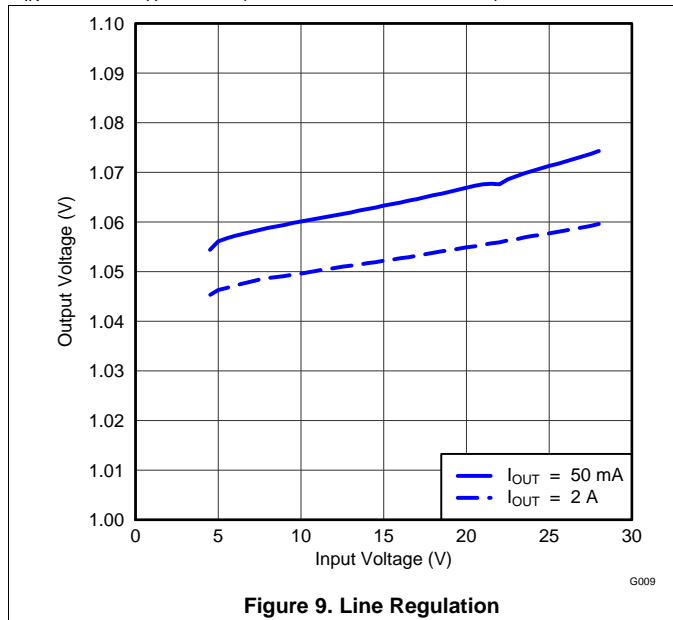


Figure 9. Line Regulation

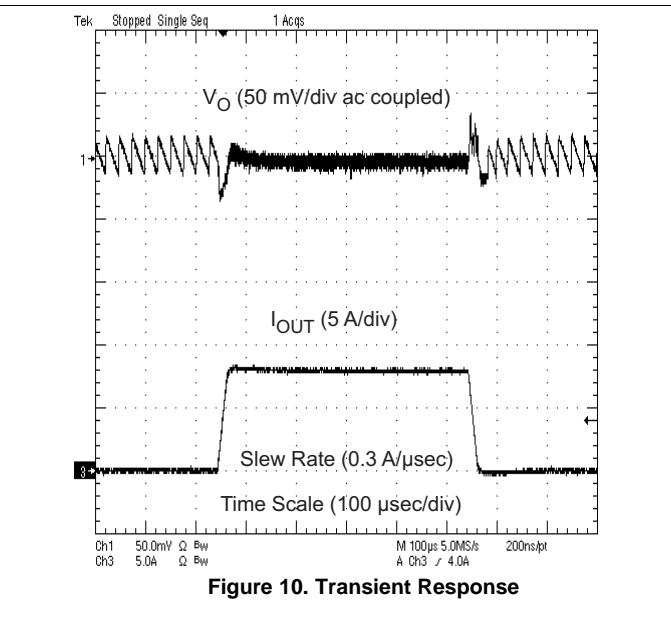


Figure 10. Transient Response

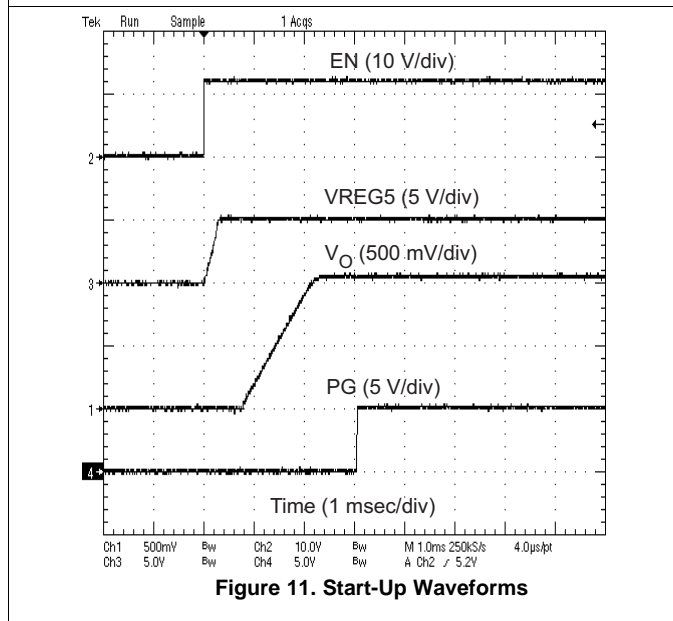


Figure 11. Start-Up Waveforms

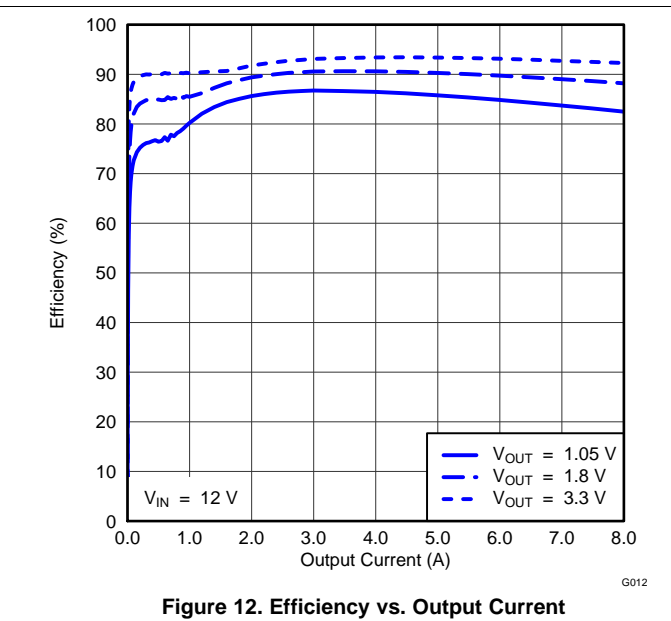


Figure 12. Efficiency vs. Output Current

Typical Characteristics (continued)

$V_{IN} = 12\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

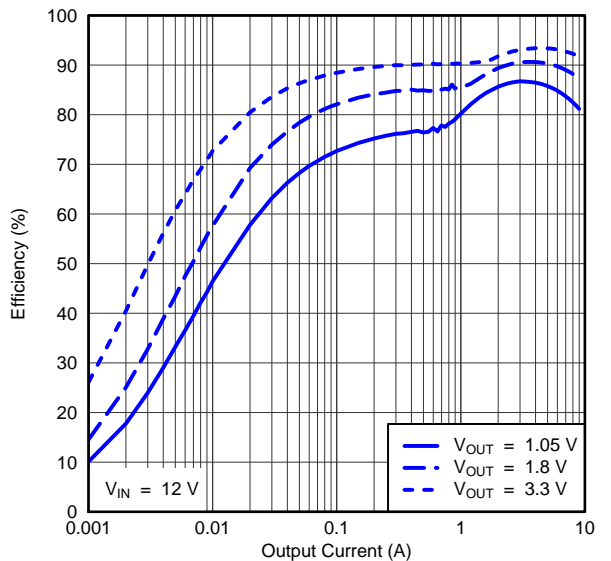


Figure 13. Light Load Efficiency vs. Output Current

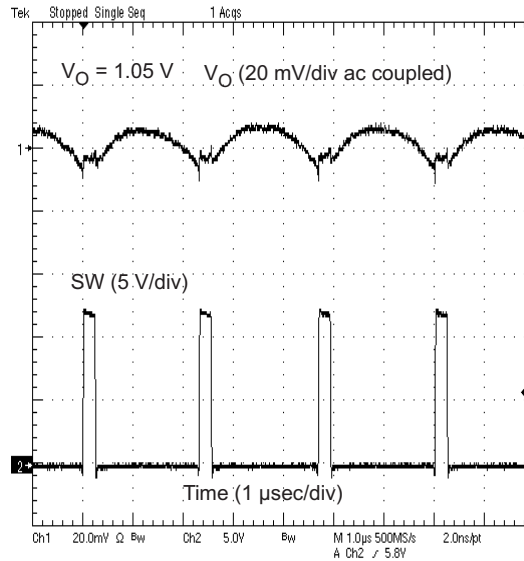


Figure 14. Output Voltage Ripple

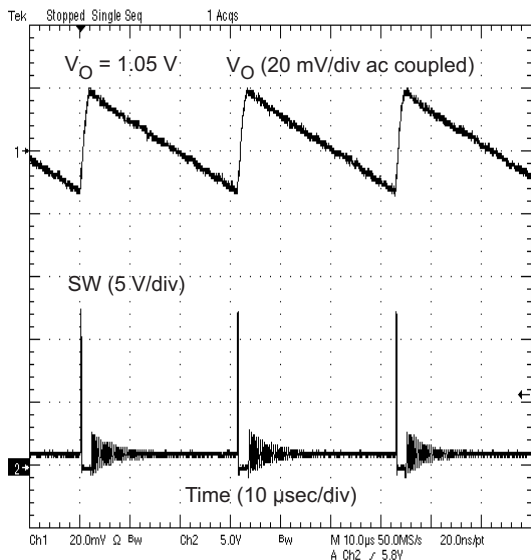


Figure 15. Output Voltage Ripple

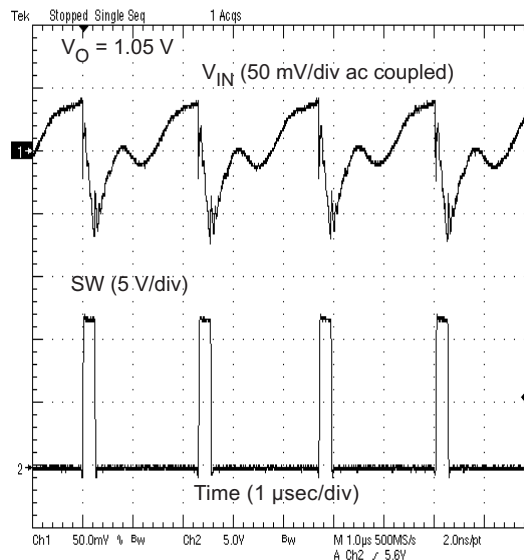
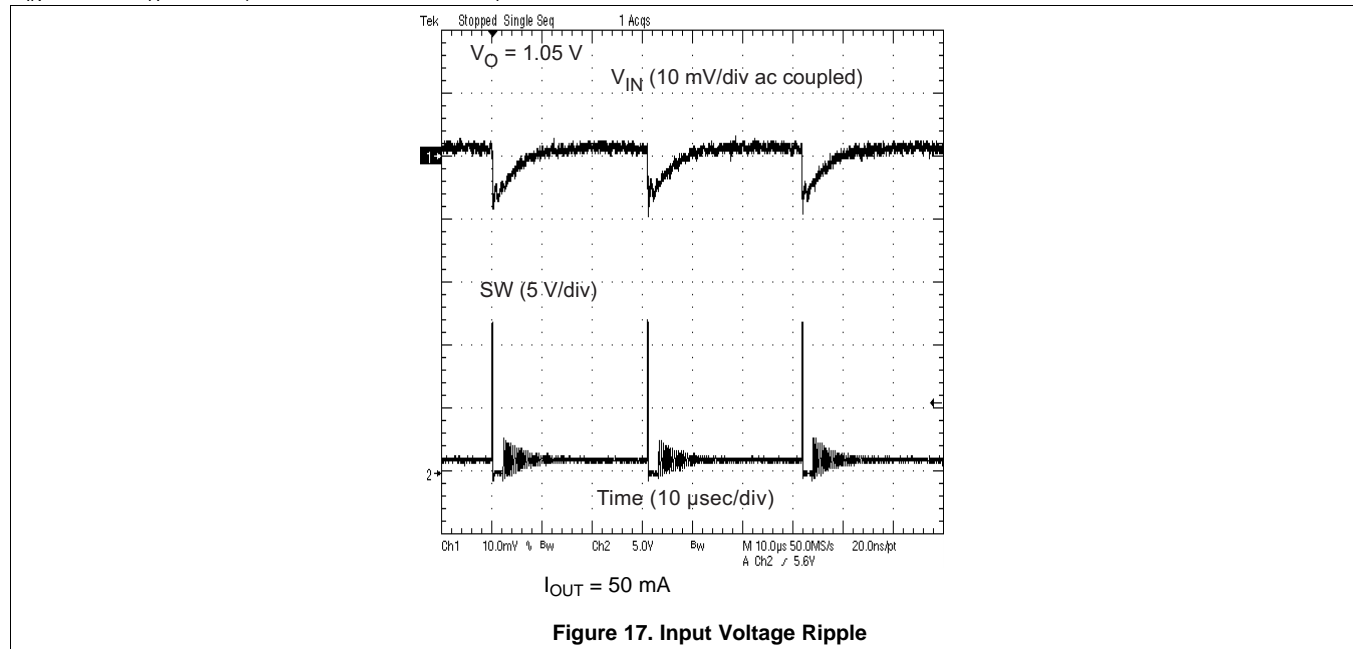


Figure 16. Input Voltage Ripple

Typical Characteristics (continued)

$V_{IN} = 12\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

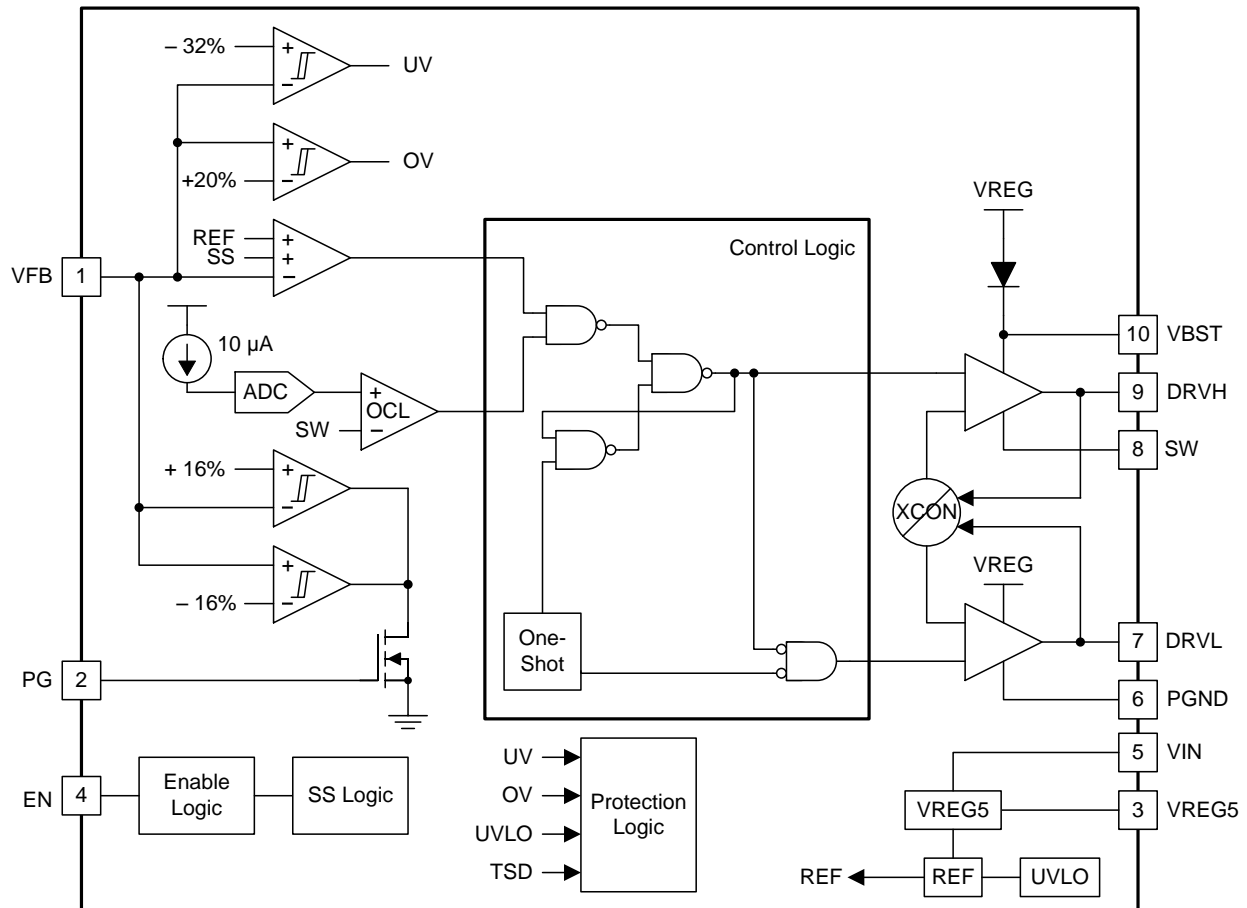


7 Detailed Description

7.1 Overview

The TPS53015 is single synchronous step-down buck controller. It operates using D-CAP2 mode control. The fast transient response of D-CAP2 control reduces the required amount of output capacitance to meet a specific level of performance. Proprietary internal circuitry allows the use of low-ESR output capacitors including ceramic and special polymer types.

7.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

7.3 Feature Description

7.3.1 Drivers

The TPS53015 device contains two high-current resistive MOSFET gate drivers. The low-side driver is a PGND referenced, VREG5 powered driver designed to drive the gate of a high-current, low $R_{DS(on)}$ N-channel MOSFET whose source is connected to PGND. The high-side driver is a floating SW referenced, VBST powered driver designed to drive the gate of a high-current, low $R_{DS(on)}$ N-channel MOSFET. To maintain the VBST voltage during the high-side driver ON-time, a capacitor is placed from SW to VBST. Each driver draws average current equal to gate charge (Q_g and $V_{gs} = 5\text{ V}$) times switching frequency (f_{SW}). To prevent cross-conduction, there is a narrow dead-time when both high-side and low-side drivers are OFF between each driver transition. During this time the inductor current is carried by one of the MOSFETs body diodes.

Feature Description (continued)

7.3.2 5-Volt Regulator

The TPS53015 has an internal 5-V low-dropout (LDO) regulator to provide a regulated voltage for all both drivers and the device internal logic. A high-quality 4.7- μ F or greater ceramic capacitor from VREG5 to GND is required to stabilize the internal regulator.

7.3.3 Soft-Start and Pre-biased Soft-Start Time

The TPS53015 operates with an internally set, 1.4-ms soft-start time. When the EN pin becomes high and the VREG5 voltage is above the UVLO threshold, an internal DAC ramps up the reference voltage to the PWM comparator. Smooth control of the output voltage is maintained during start up.

The device contains a unique circuit to prevent current from being pulled from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft-start time becomes greater than internal feedback voltage VFB), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-biased output, and ensures that the output voltage (V_{OUT}) starts and ramps up smoothly into regulation from pre-biased startup to normal mode operation.

7.3.4 Overcurrent Protection

The TPS53015 device has a cycle-by-cycle over current limit feature. The over current limits the inductor valley current by monitoring the voltage drop across the low-side MOSFET $R_{DS(on)}$ during the low-side driver on-time. If the inductor current is larger than the overcurrent limit (OCL), the device delays the start of the next switching cycle until the sensed inductor current falls below the OCL current. MOSFET $R_{DS(on)}$ current sensing is used to provide an accuracy and cost effective solution without external devices. To program the OCL, a resistor should be connected between DRVL and PGND. The recommended values are given in [Table 1](#).

Table 1. OCL Resistor Values

Resistor Value ($k\Omega$)	V_{TRIP} (V)
6.8	0.050
11	0.087
18	0.125
27	0.174
39	0.224
56	0.274
75	0.336

Use [Equation 1](#) to calculate I_{OCL} .

$$I_{OCL} = \left(\frac{(V_{IN} - V_{OUT})}{2 \times L \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \right) + \frac{V_{TRIP}}{R_{DS(ON)}} \quad (1)$$

The trip voltage is set between 0.05 V to 0.336 V over all operational temperature, including the 4000ppm/ $^{\circ}$ C temperature slope compensation for the temperature dependency of the $R_{DS(on)}$. If the load current exceeds the overcurrent limit, the voltage begins to drop. If the overcurrent conditions continues the output voltage falls below the undervoltage protection threshold and the device shuts down.

7.3.5 Overvoltage and Undervoltage Protection

The TPS53015 device monitors a resistor divided feedback voltage to detect an overvoltage or undervoltage condition. If the feedback voltage is higher than 120% of the reference voltage, the OVP comparator output goes high and the circuit latches the high-side MOSFET driver OFF and the low-side MOSFET driver ON.

When the feedback voltage is lower than 68% of the reference voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1 ms, the device latches OFF both top and bottom MOSFET drivers. This function is enabled approximately 2.2 ms after power-on. The OVP and UVP latch off is reset when EN goes low.

7.3.6 UVLO Protection

The TPS53015 offers undervoltage lockout protection (UVLO) by monitoring the voltage of VREG5 pin. When the VREG5 pin voltage is lower than UVLO threshold voltage, the device shuts off. All output drivers are OFF. The UVLO is non-latch protection.

7.3.7 Thermal Shutdown

During normal operation, when the temperature of the TPS53015 device exceeds the threshold value (typically 150°C), the device shuts off. When the temperature falls below the threshold, the device starts again. During VIN start-up when the VREG5 output voltage is below its nominal value, the device maintains the thermal shutdown threshold lower than 150°C. During the period where VIN rises, the junction temperature (T_J) must be maintained at lower than 110°C.

7.3.8 Power Good

The VFB pin measures the power-good output and the function activates after the soft-start period has completed. If the output voltage is within ±16% of the target voltage, the internal comparator detects the power-good state and the power-good signal becomes high after 1.2-ms delay. During start-up, this internal delay starts after 2.2 times the soft-start time to avoid a glitch of power-good signal. If the feedback voltage goes outside ±16% of target value, the power-good signal becomes low after 2-μs delay.

7.4 Device Functional Modes

7.4.1 PWM Operation

The main control loop of the TPS53015 device is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2 control mode. D-CAP2 control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output. At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off when the internal timer expires. This timer is set by the converter input voltage VIN, and the output voltage (V_{OUT}) to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the nominal output voltage. An internal ramp is added to the reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2 mode control.

7.4.2 Auto-skip Eco-Mode Control

The TPS53015 operates in Auto-Skip Eco-mode to increase light-load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point where its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET turns off when the device detects a zero inductor current. As the load current further decreases, the converter transitions into discontinuous conduction mode. The on-time is maintained to almost half of what it was during continuous conduction mode operation because it takes longer to discharge the output capacitor with a smaller load current to the level of the reference voltage. Use [Equation 2](#) to calculate the transition point to the light-load operation current (I_{OX(LL)}) using a 500-kHz switching frequency.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (2)$$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

This design example describes a D-CAP2 mode control in a cost sensitive application. Providing a 1.05-V output at up to 8 A from a loosely regulated 12 V (8 V – 22 V) source, this design demonstrates the TPS53015 in a typical point-of-load application.

8.2 Typical Application

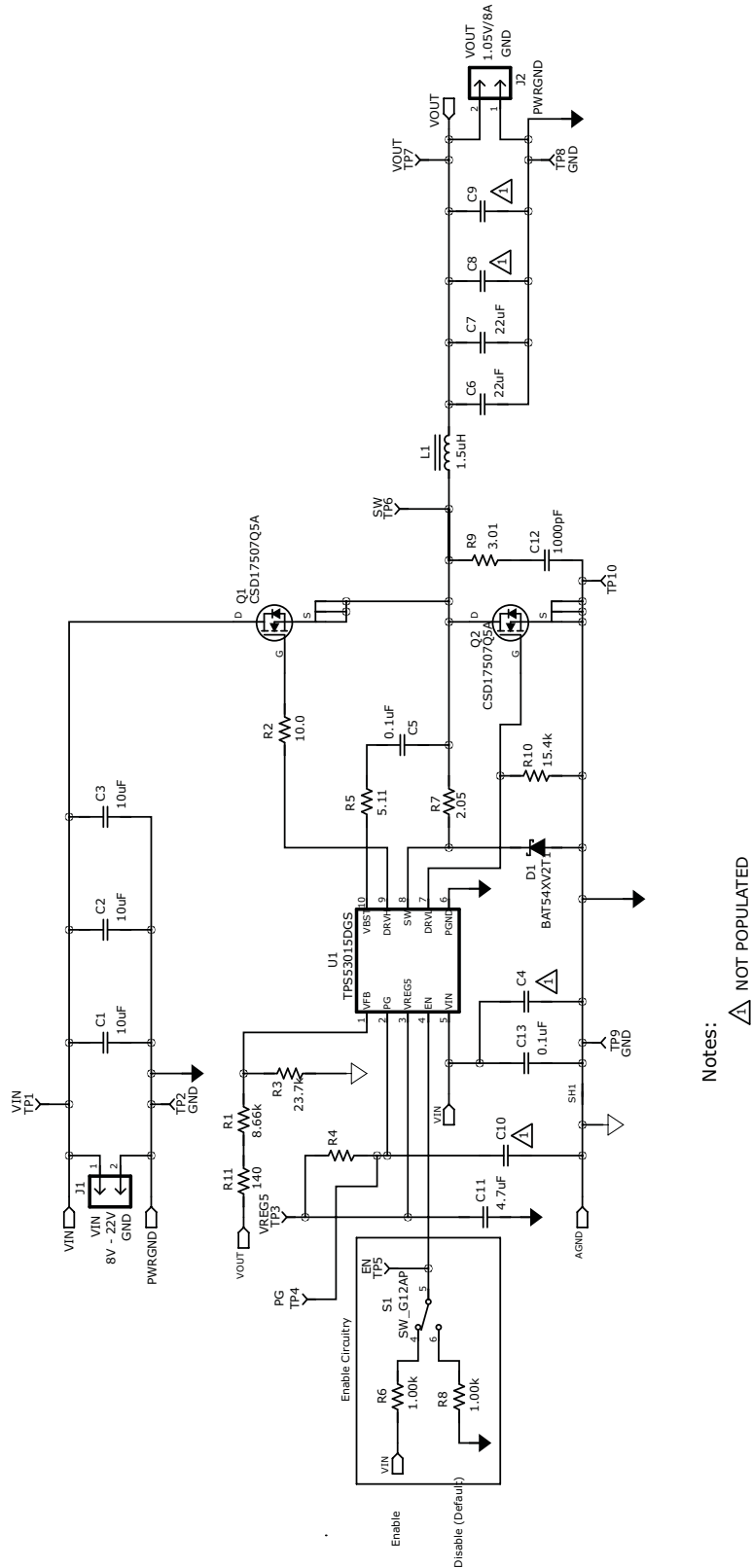


Figure 18. POL Application Using TPS53015

Typical Application (continued)

8.2.1 Design Requirements

Table 2. TPS53015 Design Requirements

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
Voltage range		8.0	12	22	V
Maximum input current	$V_{IN} = 12\text{ V}, I_{OUT} = 8\text{ A}$		0.9		A
No load input current	$V_{IN} = 12\text{ V}, I_{OUT} = 0\text{ A}$		0.6		mA
OUTPUT CHARACTERISTICS					
Output voltage			1.05		V
Output voltage regulation	Setpoint accuracy ($V_{IN} = 12\text{ V}, I_{OUT} = 8\text{ A}$)	-2%		2%	
	Line regulation ($V_{IN} = 8.0\text{ V} - 22\text{ V}, I_{OUT} = 8\text{ A}$)		1%		
	Load regulation ($V_{IN} = 12\text{ V}, I_{OUT} = 0\text{ A} - 8\text{ A}$)		1.5%		
Output voltage ripple	$V_{IN} = 12\text{ V}, I_{OUT} = 8\text{ A}$		20		mVpp
Output load current		0		8.0	A
Overcurrent limit	$V_{IN} = 12\text{ V}$		11		
SYSTEMS CHARACTERISTICS					
Switching frequency			500		kHz
Peak efficiency	$V_{IN} = 12\text{ V}, I_{OUT} = 3.2\text{ A}$		86.5%		
Full load efficiency	$V_{IN} = 12\text{ V}, I_{OUT} = 8.0\text{ A}$		81.4%		
Operating temperature			25		°C

8.2.2 Detailed Design Procedure

8.2.2.1 Determine the Inductance Value

The inductance value is selected to provide approximately 30% peak to peak ripple current at maximum load. Larger ripple current increases output ripple voltage, improve signal-to-noise ratio and contribute to stable operation. Use Equation 3 to calculate the value for L_{OUT} .

$$L_{OUT} = \frac{V_{IN(MAX)} - V_{OUT}}{I_{L(RIPPLE)} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN(MAX)}} \quad (3)$$

The inductor current ratings must support both the RMS (thermal) current and the peak (saturation) current. The RMS and peak inductor current can be estimated as shown in Equation 4.

$$I_{L(RIPPLE)} = \frac{V_{IN(MAX)} - V_{OUT}}{L_{OUT} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN(MAX)}} \quad (4)$$

$$I_{L(PEAK)} = \frac{V_{TRIP}}{R_{DS(ON)}} + I_{L(RIPPLE)} \quad (5)$$

$$I_{L(RMS)} = \sqrt{I_{OUT}^2 + \frac{1}{12} \times I_{L(RIPPLE)}^2} \quad (6)$$

注

式 6 serves as a general reference. To further improve transient response, the output inductance could be reduced further but must be considered along with the selection of the output capacitor.

8.2.2.2 Output Capacitor

The capacitor value and ESR determines the amount of output voltage ripple and load transient response. Ceramic output capacitors with X5R dielectric or better are recommended.

$$C_{OUT} = \frac{I_{L(RIPPLE)}}{8 \times V_{OUT(RIPPLE)}} \times \frac{1}{f_{SW}} \quad (7)$$

$$C_{OUT} = \frac{\Delta I_{LOAD}^2}{2 \times V_{OUT} \times \Delta V_{OS}} \times L_{OUT}$$

where

- ΔV_{OS} is the allowable amount of overshoot voltage in load transition (8)

$$C_{OUT} = \frac{\Delta I_{LOAD}^2}{2 \times K \times \Delta V_{US}} \times L_{OUT}$$

where

- ΔV_{US} is the allowable amount of undershoot voltage in load transition (9)

$$K = (V_{IN} - V_{OUT}) \times \left(\frac{t_{ON}}{t_{ON} - t_{OFF(min)}} \right)$$

where

- $t_{OFF(min)}$ is the minimum off time (10)

Select the capacitance value greater than the largest value calculated from 式 7, 式 8 and 式 9. The minimum recommended output capacitance is 44 μ F.

8.2.2.3 Input Capacitor

The TPS53015 device requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A minimum 10- μ F high-quality ceramic capacitor is recommended for the input capacitor. The capacitor voltage rating must be greater than the maximum input voltage.

8.2.2.4 Bootstrap Capacitor

The TPS53015 device requires a bootstrap capacitor from SW to VBST to provide the floating supply for the high-side drivers. A minimum 0.1- μ F high-quality ceramic capacitor is recommended. The capacitor voltage rating must be greater than 10 V.

8.2.2.5 VREG5 Capacitor

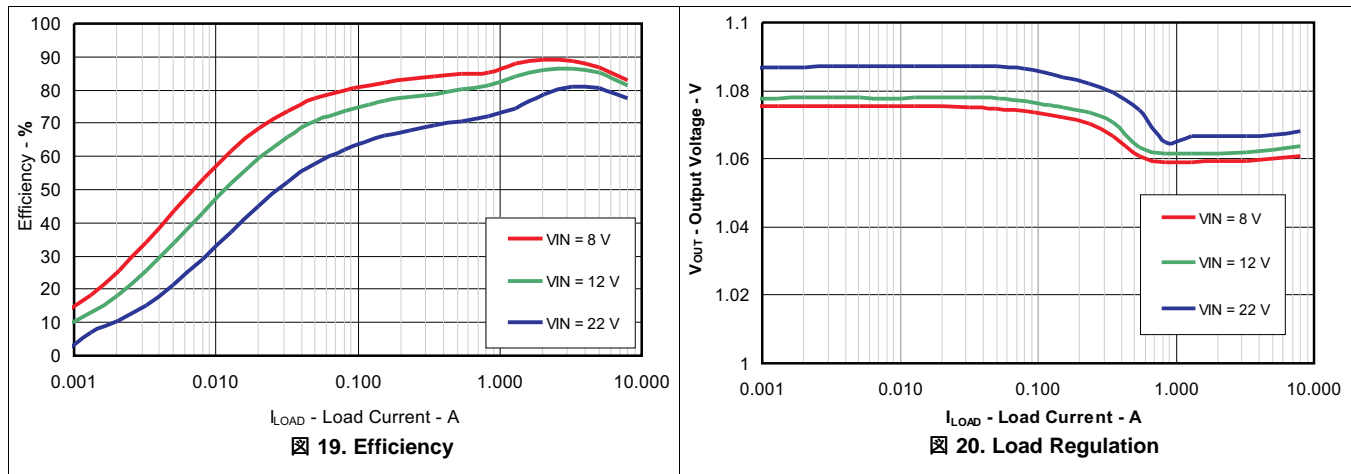
The TPS53015 device requires that the VREG5 regulator is bypassed. A minimum 4.7- μ F high-quality ceramic capacitor must be connected between the VREG5 and PGND for proper operation. The capacitor voltage rating should be greater than 10 V.

8.2.2.6 Choose Output Voltage Resistors

The output voltage is set with a resistor divider from output voltage node to the VFB pin. It is recommended to use 1% tolerance or better resistors. Select an R2 value between 10 k Ω and 100 k Ω and use 式 11 to calculate R1.

$$R1 = \left(\frac{V_{OUT}}{V_{VFB}} - 1 \right) \times R2 \quad (11)$$

8.2.3 Application Curves



注

For more performance curves, see the PWR126 EVM user guide. (SLUU944)

9 Power Supply Recommendations

The TPS53015 device operates using an input voltage supply range from 4.5 V to 28 V. This input supply must be well regulated. Proper bypassing of input supplies and internal regulators is also critical for noise performance, as is PCB layout and grounding scheme

10 Layout

10.1 Layout Guidelines

Considerations these design guidelines before beginning the application layout process.

- Design an input switching current loop as small as possible.
- Place the input capacitor close to the top switching FET.
- Design the output switching current loop as small as possible.
- The SW node must be physically small and as short as possible as to minimize parasitic capacitance and inductance and to minimize radiated emissions.
- Bring Kelvin connections from the output to the feedback pin (VFB) of the device.
- Place analog and non-switching components far away from switching components.
- Make a single point connection from the signal ground to power ground.
- Do not allow switching current to flow under the device.

10.2 Layout Example

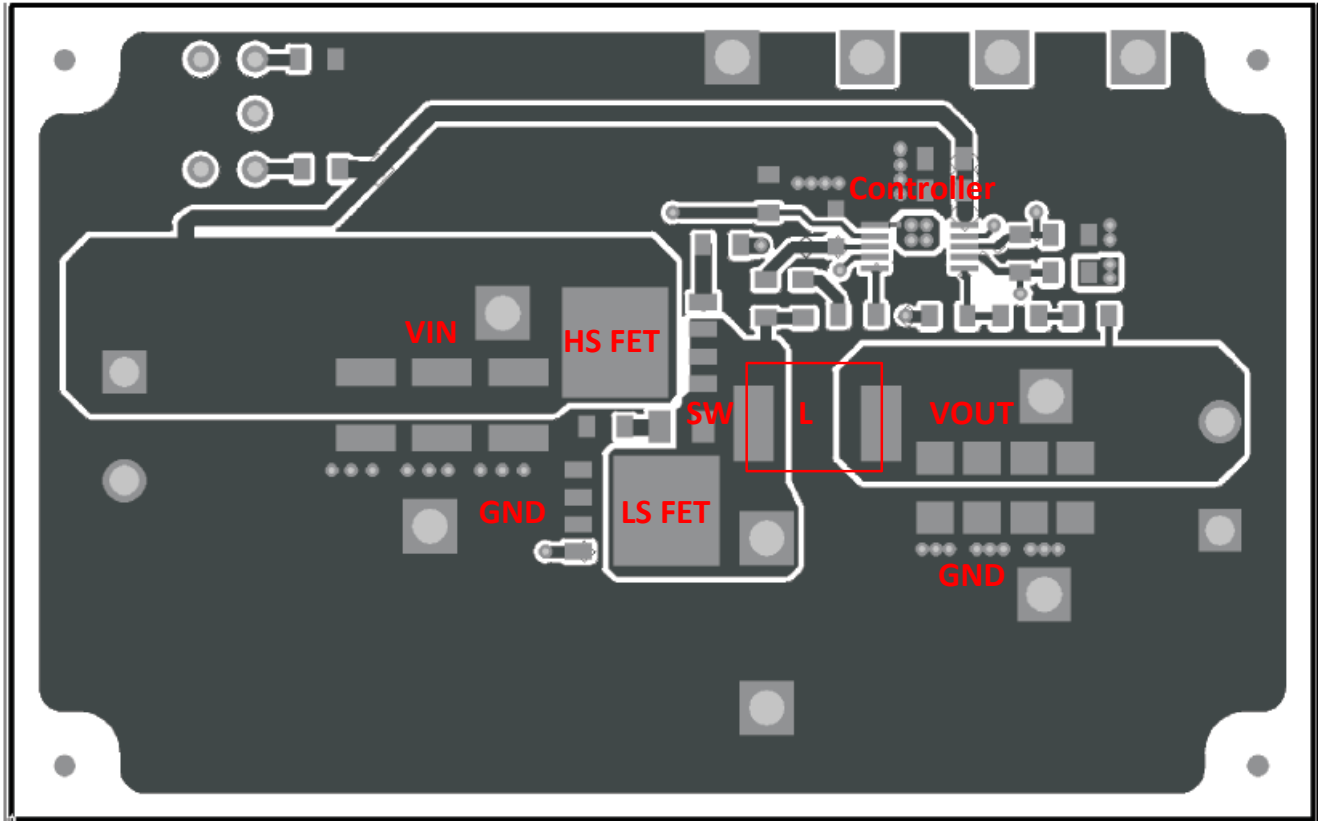


图 21. TPS53015 Layout

11 デバイスおよびドキュメントのサポート

11.1 商標

D-CAP2, Eco-Mode, Eco-mode are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.2 静電気放電に関する注意事項



これらのデバイスは、限定的なESD(静電破壊)保護機能を内蔵しています。保存時または取り扱い時は、MOSゲートに対する静電破壊を防止するために、リード線同士をショートさせておくか、デバイスを導電フォームに入れる必要があります。

11.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS53015DGS	LIFEBUY	VSSOP	DGS	10	80	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	53015	
TPS53015DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG SN	Level-2-260C-1 YEAR	-40 to 85	53015	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53015DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53015DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPS53015DGS	DGS	VSSOP	10	80	330	6.55	500	2.88

DGS0010A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4221984/A 05/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated