

This device is designed specifically to power Intel processors under a strict disclosure agreement with Intel Corporation. The end user must have a current CNDA in place with Intel Corporation to access this information.

For a detailed datasheet and other design support tools, please contact <u>VR@list.ti.com</u>.



# **PACKAGE OPTION ADDENDUM**

10-Dec-2020

### PACKAGING INFORMATION

www.ti.com

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
TPS53661RSBR	ACTIVE	WQFN	RSB	40	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-10 to 105	TPS 53661	Samples
TPS53661RSBT	ACTIVE	WQFN	RSB	40	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-10 to 105	TPS 53661	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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10-Dec-2020



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# TAPE AND REEL INFORMATION



# TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

# QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53661RSBR	WQFN	RSB	40	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS53661RSBR	WQFN	RSB	40	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS53661RSBT	WQFN	RSB	40	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS53661RSBT	WQFN	RSB	40	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2



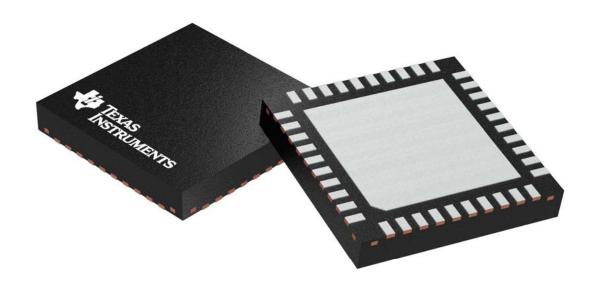
www.ti.com 11-May-2024



## \*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53661RSBR	WQFN	RSB	40	3000	346.0	346.0	33.0
TPS53661RSBR	WQFN	RSB	40	3000	367.0	367.0	35.0
TPS53661RSBT	WQFN	RSB	40	250	210.0	185.0	35.0
TPS53661RSBT	WQFN	RSB	40	250	210.0	185.0	35.0

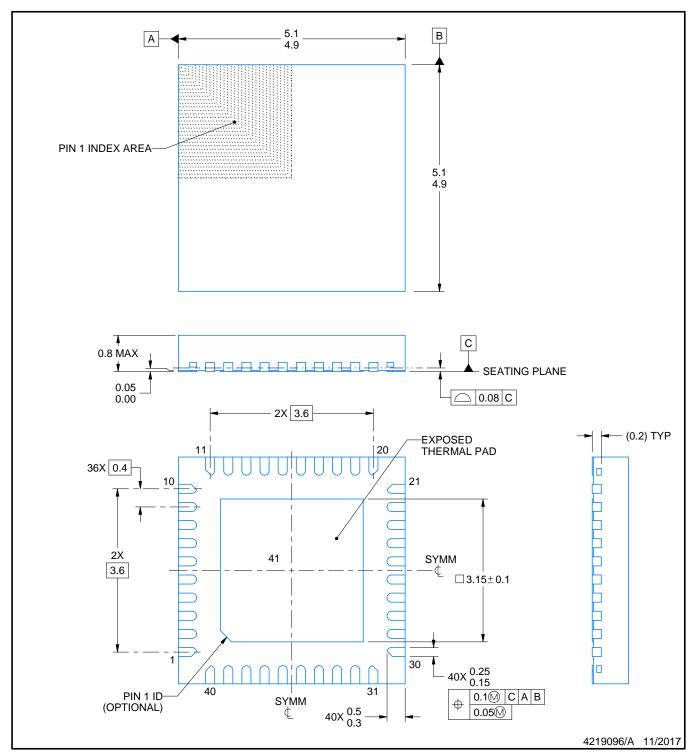
5 x 5 mm, 0.4 mm pitch



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



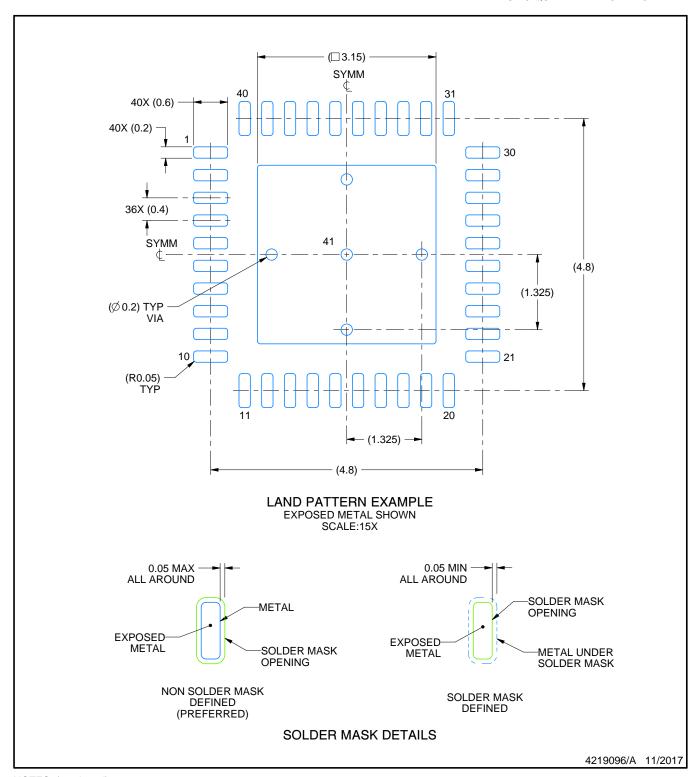




# NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

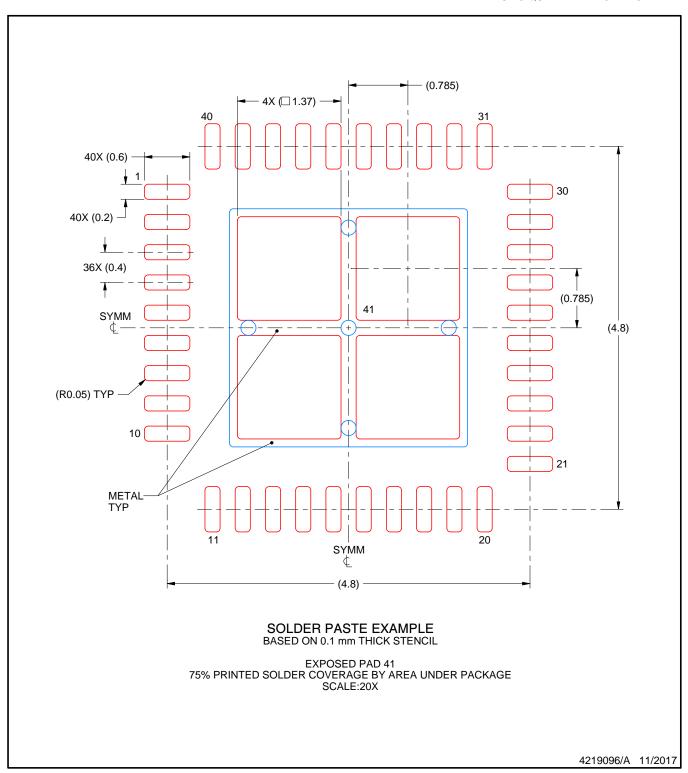




NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



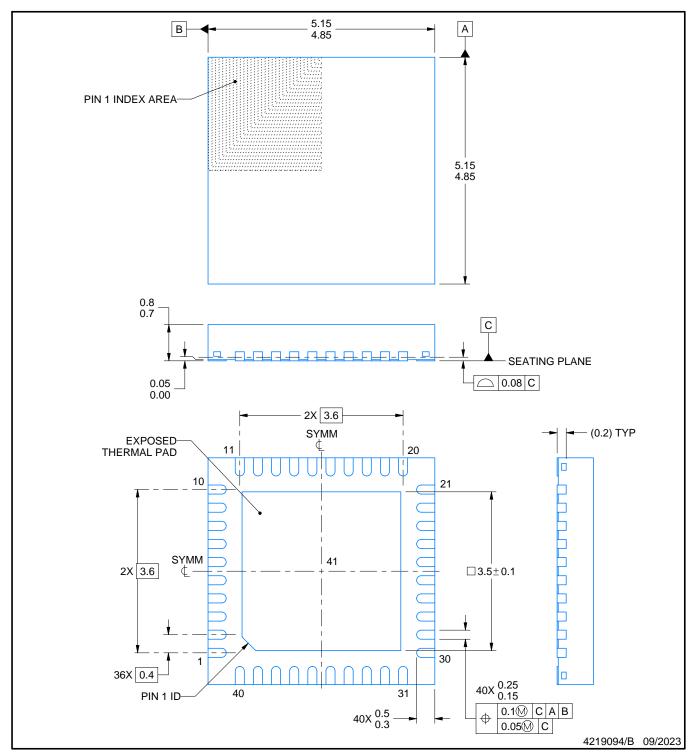


NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



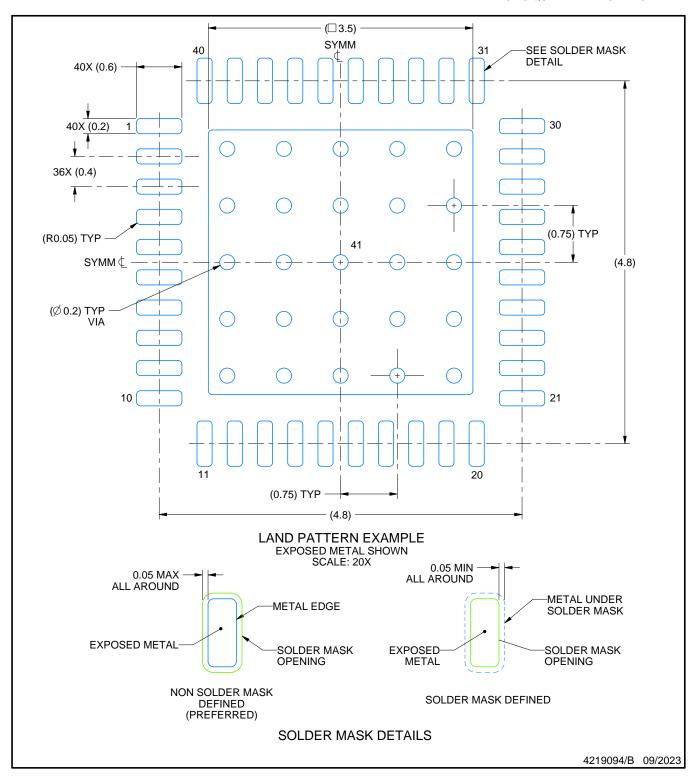




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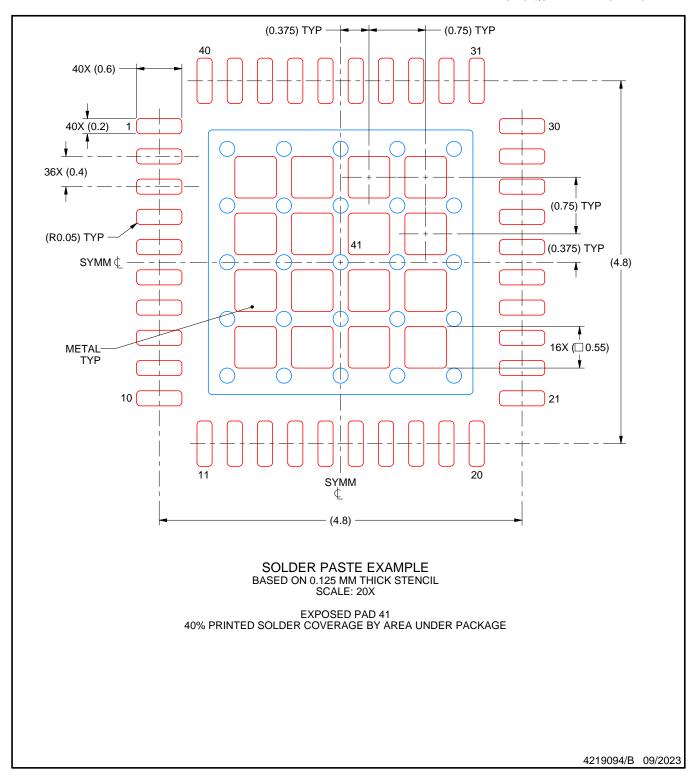




NOTES: (continued)

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NOTES: (continued)

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