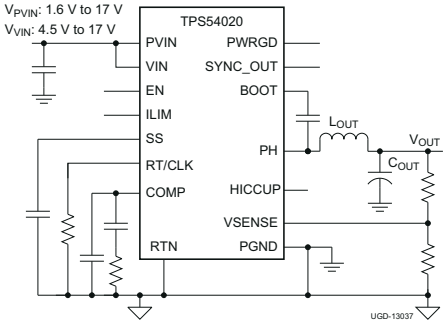
TPS54020 軽負荷効率向上、小型、10A、4.5V～17V 入力、SWIFT™ 同期整流降圧型コンバータ

1 特長

- 動作時の接合部温度範囲：–40℃～+150℃
- 8mΩ/6mΩ の MOSFET を内蔵
- 放熱特性の優れた 3.5mm × 3.5mm HotRod™ パッケージ
- ピーク電流モード制御
- Eco-mode™ パルス・スキップによる効率の向上
- 両方の MOSFET に対する過電流保護
- 選択可能な過電流保護方式
- 選択可能な過電流保護レベル
- 分割電源レール：1.6V～17V (PVIN)
- 電圧リファレンス：0.6V、精度 ±1%
- 200kHz～1.2MHz のスイッチング周波数
- 外部クロックに同期
- 出力をプリバイアスした状態で起動
- 過熱保護および過電圧保護
- 調整可能なソフト・スタートおよび電源シーケンス
- 低電圧および過電圧用パワー・グッド出力モニタ
- SYNC_OUT 機能により位相差 180° の出力クロック信号を提供
- SWIFT™ ドキュメントと WEBENCH については Web ページを参照
- WEBENCH® Power Designer により、TPS54020 を使用するカスタム設計を作成

2 アプリケーション

- 無線インフラストラクチャおよび有線通信機器
- 試験 / 測定機器
- 航空宇宙 / 防衛
- 産業用アプリケーションの DSP と FPGA のポイント・オブ・ロード (POL)



アプリケーション概略回路図

3 概要

TPS54020 は 10A、4.5V～17V 入力の SWIFT コンバータです。画期的な 3.5mm × 3.5mm の HotRod パッケージにより、高密度の降圧設計を最適化できます。TPS54020 は必要な機能をすべて搭載したコンバータです。

ハイサイドおよびローサイド MOSFET の画期的な統合とパッケージングによって高効率を実現しており、高負荷条件では連続電流モード (CCM) で動作し、軽負荷時にはパルスをスキップしながら Eco-mode に遷移して効率を高めます。

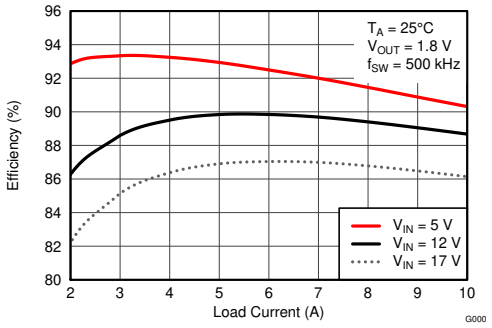
両方の MOSFET に対する電流制限により、デバイスおよびシステムを保護できます。ハイサイド MOSFET ではサイクルごとの電流制限によって過負荷状況に対する保護を提供し、ローサイド MOSFET ではゼロ電流検出機能により、軽負荷動作時にローサイド MOSFET がオフになります。3 つの電流制限スレッショルドから選択可能なため、さまざまな用途に対応します。ヒカップまたはサイクルごとの過電流保護方式も選択できます。

サーマル・シャットダウン保護機能により、ダイ温度がサーマル・シャットダウン・トリップ・ポイントを超えるとスイッチングはディセーブルになり、設定された温度ヒステリシスの分だけ温度が低下し、シャットダウン・ヒカップ時間が経過するとスイッチングはイネーブルになります。

製品情報

部品番号	パッケージ(1) (1 ページ)	本体サイズ (公称)
TPS54020	VQFN (15)	3.50mm × 3.50mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



効率と負荷電流との関係

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (March 2019) to Revision F (November 2020)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• 「アプリケーション」を更新	1
• Removed 1000 V/V MIN specification for error amplified dc gain	6
• Changed low-side switch sinking current limit units from "mA" to "A"	6
• Increased MAX specification for low-side switch sinking current limit from -0.8 A to -1.15 A	6

Changes from Revision D (December 2014) to Revision E (March 2019)	Page
• WEBENCH のリンクを追加	1
• Changed symbols in *セクション 7.4*; changed $R_{\theta JA}$ from 16.6°C/W to 25°C/W	6
• Changed "$I_{IN(EN)}$" to "I_P" and added "V_{EN} below threshold"; added "I_H" and "V_{EN} above threshold"	6
• Added 2 sentences to end of *セクション 8.3.12*	17
• Changed "proper operation of the device" to "startup of V_{OUT2} after a fault"	17
• Changed 式 5 and 式 8	17
• Added paragraph to end of *セクション 8.3.13*	17
• Deleted "and the low-side MOSFET is turned ON..."	19
• Changed last sentence of first paragraph in *セクション 8.3.14*	19

Changes from Revision C (March 2013) to Revision D (November 2014)	Page
• 「ピン構成および機能」セクション、「取り扱いに関する定格」の表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1

Changes from Revision B (February 2013) to Revision C (March 2013)	Page
• Deleted Note 2 from the Thermal Information table	5
• Added VIN internal UVLO threshold and VIN internal UVLO hysteresis rows	6
• Changed OVERVIEW paragraph "The TPS54020 starts up..."	12

Changes from Revision A (September 2012) to Revision B (February 2013)	Page
• Changed the Input Voltage and Power Input Voltage Pins (VIN and PVIN) section	14
• Changed the DETAILED DESCRIPTION section	20
• Changed the DESIGN EXAMPLE section	26

Changes from Revision * (July 2011) to Revision A (September 2012)	Page
• デバイスを「製品プレビュー」から「量産」に変更	1

5 Description (Continued)

The SS pin controls the output voltage start-up ramp and allows for selectable soft-start times. Power supply sequencing is also available by configuring the enable (EN) and the open-drain power-good (PWRGD) pins.

Two TPS54020 devices may be synchronized 180° out-of-phase by using the SYNC_OUT and CLK pins.

6 Pin Configuration and Functions

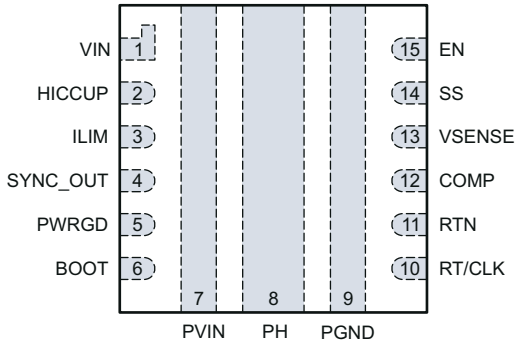


図 6-1. 15-Pin VQFN RUW Package (Top View)

表 6-1. Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
BOOT	6	S	A bootstrap capacitor is required between BOOT and PH. If the voltage on this capacitor is below the minimum required by the high-side MOSFET (BOOT UVLO), the PH node is forced low so that the capacitor is refreshed.
COMP	12	O	Error amplifier current output, and input to the output switch current comparator. Connect frequency compensation to this pin.
EN	15	I	A divider network must be used to implement an undervoltage lockout function. To disable switching and reduce quiescent current, this pin must be pulled to ground.
HICCUP	2	O	Overcurrent protection scheme select pin
ILIM	3	O	Current limit threshold select pin
PGND	9	G	Power Ground. Return for the low-side MOSFET
PH	8	O	Switch node
PVIN	7	I	Power input. Supplies the power switches of the power converter
PWRGD	5	O	Power-good fault pin. Asserts low if output voltage is out of regulation due to thermal shutdown, dropout, overvoltage, EN shutdown, or during soft start.
RT/CLK	10	I/O	Automatically selects between RT mode and CLK mode. An external timing resistor adjusts the switching frequency of the device. In CLK mode, the device synchronizes to an external clock.
RTN	11	G	Return for control circuitry
SS	14	I/O	Soft-start pin. An external capacitor connected to this pin sets the internal voltage reference rise time. The voltage on this pin overrides the internal reference. It can be used for sequencing.
SYNC_OUT	4	O	Synchronization output provides a clock signal 180° out-of-phase with the power switch.
VIN	1	I	Supplies the control circuitry of the power converter
VSENSE	13	I	Inverting node of the transconductance (gm) error amplifier

(1) I = Input, O = Output, S = Supply, G = Ground Return

7 Specifications

7.1 Absolute Maximum Ratings (1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VIN, PVIN	–0.3	20	V
	EN	–0.3	6	
	BOOT	–0.3	27	
	COMP, HICCUP, ILIM, SS/TR, SYNC_OUT, VSENSE	–0.3	3	
	PWRGD, RT/CLK	–0.3	6	
Output voltage	BOOT-PH	0	7.5	V
	PH	–1	20	
	PH (10-ns transient)	–3	20	
Source current	RT/CLK	–100	100	µA
	PH		Current Limit	A
Sink current	PH		Current Limit	A
	PVIN		Current Limit	
	COMP	–200	200	µA
	PWRGD	–0.1	5	mA
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *セクション 7.3* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Operating junction temperature – T_J		–40	150	°C
Control input voltage	VIN	4.5	17	V
Power stage input voltage	PVIN	1.6	17	V

7.4 Thermal Information

THERMAL METRIC[2]		TPS54020 RUW (VQFN) 15 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25[1]	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.3	°C/W

(1) Applicable only to the EVM in free space with no airflow.
(2) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

T_J = –40°C to +150°C, V_{IN} = 4.5 V to 17 V, P_{VIN} = 4.5 V to 17 V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN AND PVIN PINS)						
	PVIN operating input voltage		1.6		17	V
	VIN operating input voltage		4.5		17	V
	VIN internal UVLO threshold	VIN Rising		4	4.5	V
	VIN internal UVLO hysteresis			150		mV
	VIN shutdown supply current	V_{EN} = 0 V		2	10	µA
	VIN operating – nonswitching supply current	V_{VSENSE} = 610 mV		600	1000	µA
ENABLE AND UVLO (EN PIN)						
V_{EN}	Enable threshold	Rising		1.22	1.26	V
		Falling	1.10	1.17		V
I_P	Input current V_{EN} below threshold	V_{EN} = 1.1 V		–1.15		µA
I_H	Added hysteresis current V_{EN} above threshold	V_{EN} = 1.3 V		–3.3		µA
VOLTAGE REFERENCE						
V_{REF}	Voltage reference	0 A ≤ I_{OUT} ≤ 10 A, –40°C ≤ T_A ≤ 150°C	0.594	0.6	0.606	V
MOSFET						
DRVH	High-side switch resistance	BOOT-PH = 3 V		9.5	18	mΩ
		BOOT-PH = 6 V[1]		8	14	mΩ
DRVL	Low-side switch resistance[1]	V_{VIN} = 12 V		6	11	mΩ
ERROR AMPLIFIER						
	Error amplifier input bias current	V_{VIN} = 12 V		50		nA
g_M	Error amplifier transconductance	–2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V		1300		µS
	Error amplifier dc gain	V_{VSENSE} = 0.6 V		3000		V/V
	Error amplifier source/sink	V_{COMP} = 1 V, 100 mV Overdrive		±100		µA
	Start switching threshold	V_{COMP}		0.27		V
g_M	COMP to I_{SWITCH} transconductance	I_{ILIM} = NC		20		A/V
		I_{ILIM} = RTN		17		
		499 kΩ (1%) between ILIM and RTN		13		

T_J = –40°C to +150°C, V_{IN} = 4.5 V to 17 V, P_{VIN} = 4.5 V to 17 V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT						
	High-side switch current limit threshold	I_{ILIM} = NC	13.4	15.1	16.5	A
		I_{ILIM} = RTN	11.2	12.75	14	
	High-side switch current limit threshold	499 kΩ (1%) between ILIM and RTN	8.3	9.4	10.2	A
	Low-side switch sourcing current limit	I_{ILIM} = NC	11	13	15	A
		I_{ILIM} = RTN	9	10.5	12	
	Low-side switch sourcing current limit	499 kΩ (1%) between ILIM and RTN	6.5	8	9.5	A
	Low-side switch sinking current limit	–ve current denotes current sourced from PH pin		–0.2	–1.15	A
	Overcurrent protection scheme	(HICCUP = RTN)		Cycle-by-cycle		
	Hiccup delay before re-start	HICCUP OPEN		16384		Cycles
	Hiccup wait time	HICCUP OPEN		128		Cycles
THERMAL SHUTDOWN						
	Thermal shutdown			175		°C
	Thermal shutdown hysteresis			10		°C
	Thermal shutdown hiccup time			16384		Cycles
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)						
	Switching frequency	$R_{RT/CLK}$ = 250 kΩ (1%)	185	205	230	kHz
		$R_{RT/CLK}$ = 100 kΩ (1%)	475	500	525	
		$R_{RT/CLK}$ = 50 kΩ (1%)	890	990	1090	
	Minimum CLK pulse width			20		ns
	RT/CLK high threshold				2	V
	RT/CLK low threshold		0.8			V
	RT/CLK falling edge to PH rising edge delay	Measure at 500 kHz with RT resistor in series		66		ns
	PLL frequency range		200		1200	kHz
SYNC_OUT (SYNC_OUT PIN)						
	Phase with RT/CLK			180		Degree
	SYNC_OUT low threshold				0.8	V
	SYNC_OUT high threshold		2			V
PH (PH PIN)						
$t_{ON(min)}$	Minimum on-time	Measured at 90% to 90% of VIN, I_{PH} = 2 A		112	165	ns
$I_{PH(LK)}$	PH leakage current	V_{VIN} = 17 V, V_{OUT} = 0.6 V, T_A = 150°C		300		µA
BOOT (BOOT PIN)						
	BOOT-PH UVLO			2.1	3	V
SOFT START AND TRACKING (SS/TR PIN)						
I_{SS}	Soft-start charge current		2.1	2.3	2.5	µA
	SS/TR to VSENSE matching	$V_{SS/TR}$ = 0.4 V		22	45	mV

T_J = –40°C to +150°C, V_{IN} = 4.5 V to 17 V, P_{VIN} = 4.5 V to 17 V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD (PWRGD PIN)						
	VSENSE threshold	V_{VSENSE} falling (Fault)		91		%V_{REF}
		V_{VSENSE} rising (Good)		95		
		V_{VSENSE} rising (Fault)		108		
		V_{VSENSE} falling (Good)		104		
	Output high leakage	V_{VSENSE} = VREF, V_{PWRGD} = 5.5 V		3	100	nA
	Output low	I_{PWRGD} = 2 mA			0.3	V
	Minimum input voltage for valid output	V_{PWRGD} < 0.5 V at 100 µA		0.6	1	V
	Minimum soft-start voltage for valid PWRGD				1.4	V

(1) Measured at pins.

7.6 Typical Characteristics

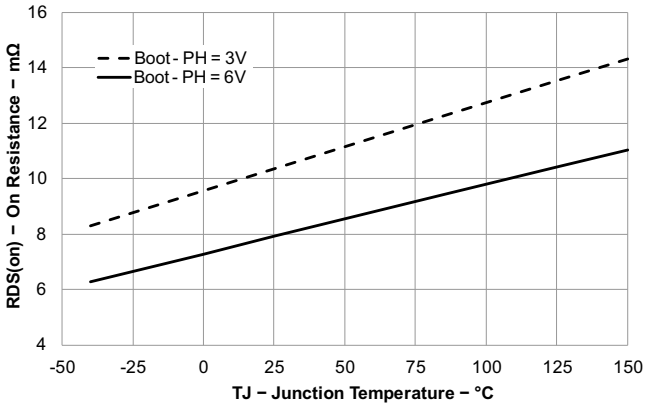


図 7-1. High-Side MOSFET On-Resistance vs Junction Temperature

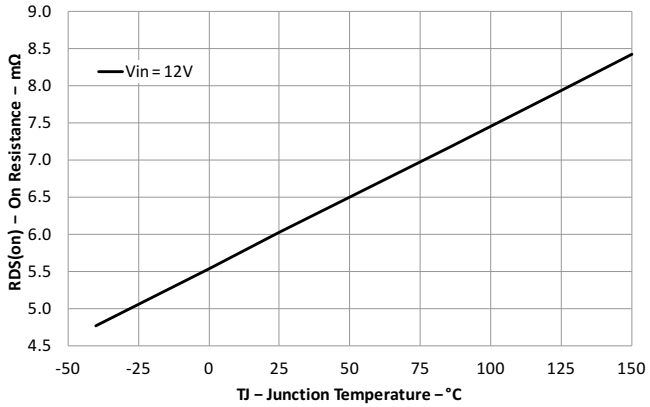


図 7-2. Low-Side MOSFET On-Resistance vs Junction Temperature

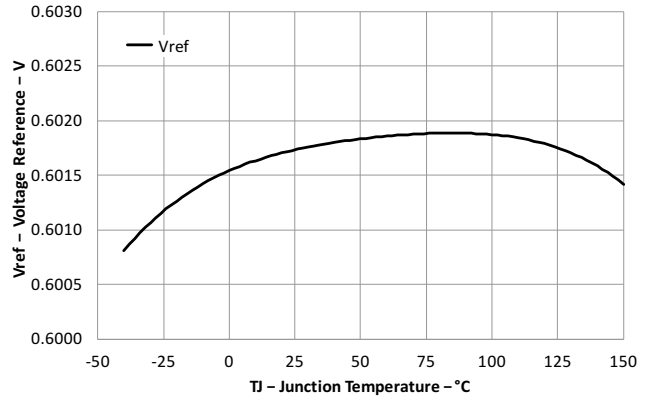


図 7-3. Voltage Reference vs Junction Temperature

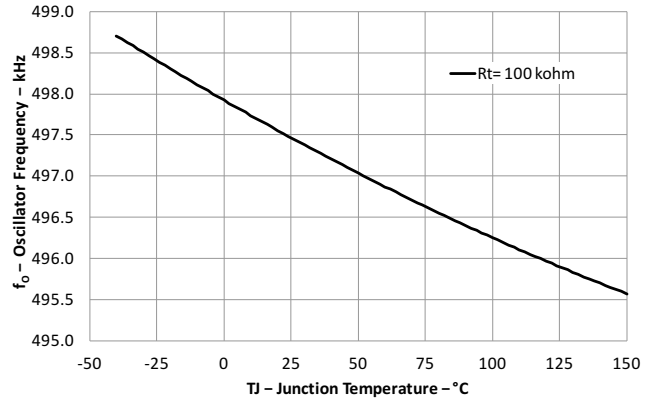


図 7-4. Oscillator Frequency vs Junction Temperature

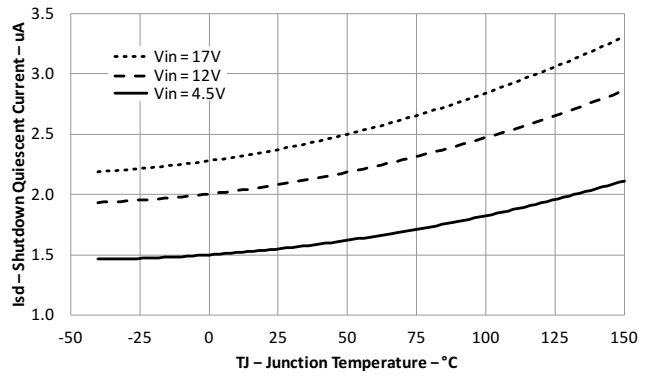


図 7-5. Shutdown Quiescent Current vs Junction Temperature

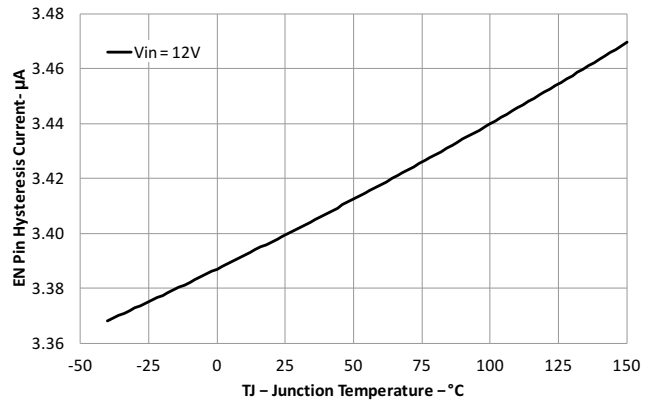


図 7-6. EN Pin Hysteresis Current vs Junction Temperature, V_{EN} = 1.3 V

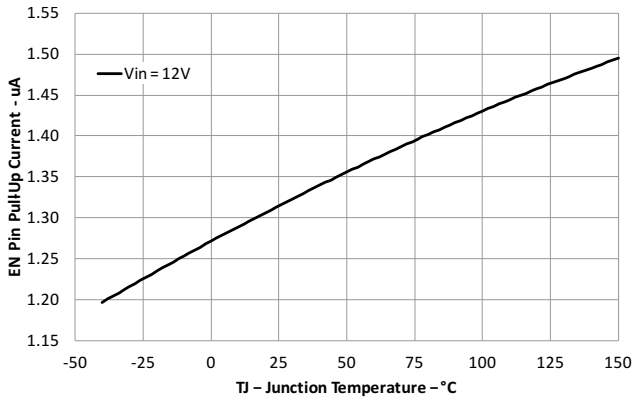


図 7-7. EN Pin Pullup Current vs Junction Temperature, V_{EN} = 1.1 V

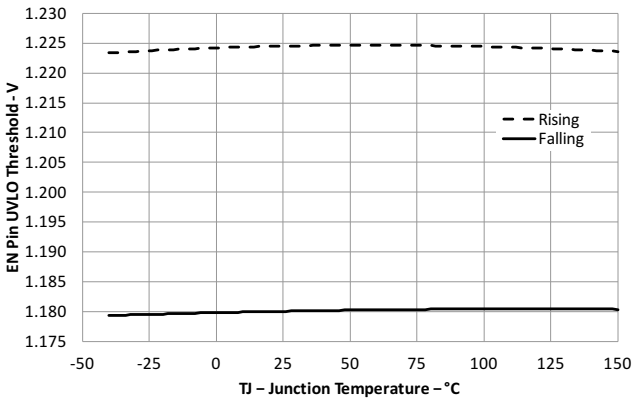


図 7-8. EN Pin UVLO Threshold vs Junction Temperature, V_{VIN} = 12 V

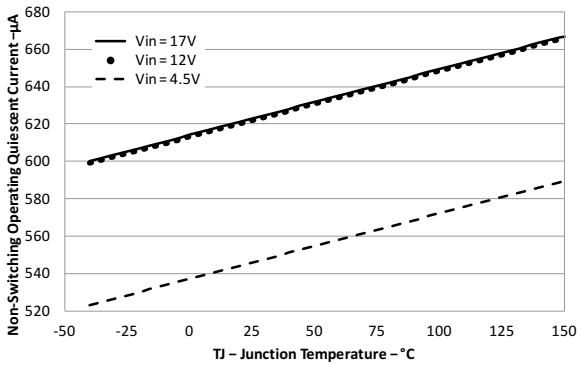


図 7-9. Nonswitching Operating Current vs vs Junction Temperature

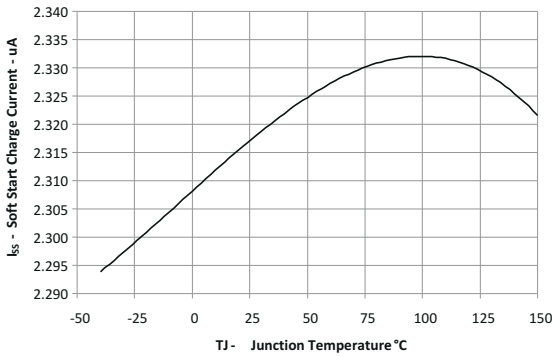


図 7-10. Soft-Start Charge Current vs Junction Temperature

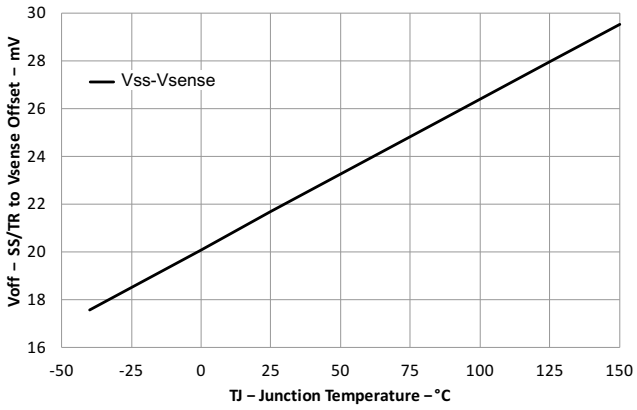


図 7-11. (V_{SS}-V_{VSENSE}) Offset vs Junction Temperature

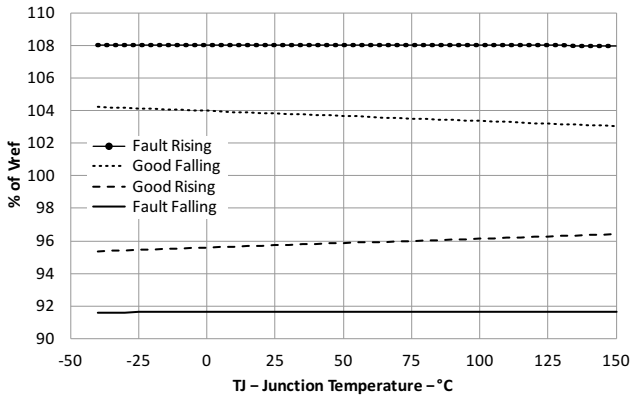


図 7-12. Power-Good Threshold vs Junction Temperature

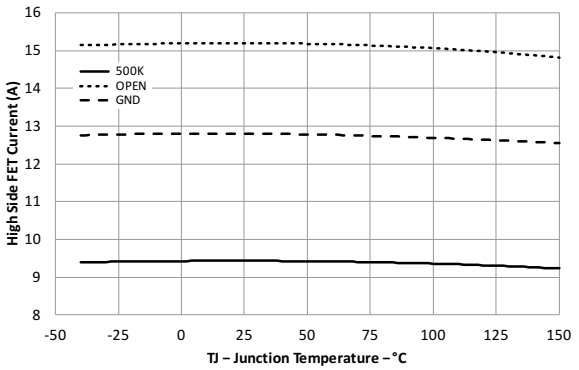


図 7-13. High-Side MOSFET Current Limit vs Junction Temperature, V_{IN} = 12 V

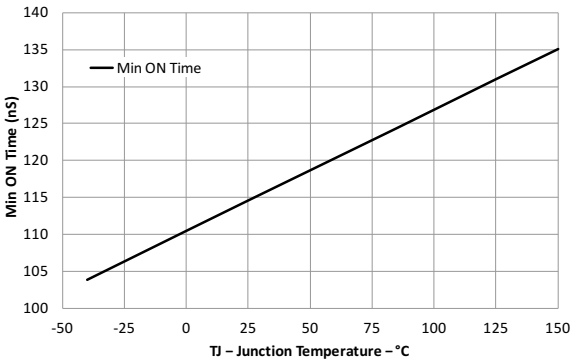


図 7-14. Minimum On-Time vs Temperature

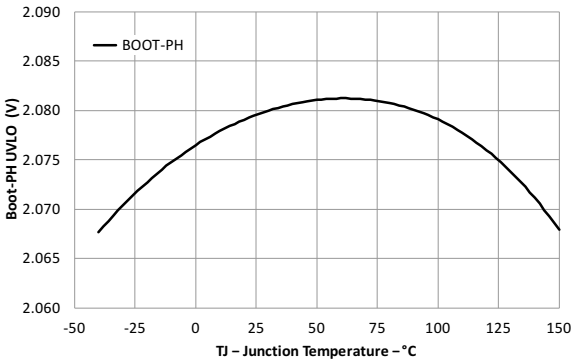


図 7-15. BOOT-PH UVLO vs Junction Temperature

8 Detailed Description

8.1 Overview

The TPS54020 is a 17-V, 10-A, synchronous step-down (buck) converter with two integrated N-channel MOSFETs. To improve performance during line and load transients, the TPS54020 implements a constant frequency, peak current mode control which also simplifies external frequency compensation. The wide switching frequency range between 200 kHz and 1200 kHz allows for efficiency and size optimization when selecting the output filter components. A resistor to ground on the RT/CLK pin adjusts the switching frequency. The TPS54020 also has an internal phase lock loop (PLL) controlled by the RT/CLK pin that can be used to synchronize the switching cycle to the falling edge of an external system clock.

The TPS54020 starts up safely into pre-biased loads. The device implements an internal undervoltage lockout (UVLO) feature on the VIN pin with a nominal START voltage of 4 V and a nominal hysteresis of 150 mV. If the design requires more hysteresis due to an input source that droops with load or if different START and STOP thresholds are required, this functionality can be achieved by using the EN pin. The EN pin has a hysteretic internal pullup current source that can be used to adjust the input voltage UVLO with two external resistors. The total operating current for the TPS54020 is approximately 600 µA when not switching and under no load. When the TPS54020 is disabled, the supply current is typically less than 2 µA.

The integrated MOSFETs allow for high-efficiency power supply designs with continuous output currents up to 10 A. The MOSFETs are sized to optimize efficiency for low to medium duty cycle applications

The TPS54020 reduces the external component count by integrating the boot recharge circuit. A capacitor connected between the BOOT and PH pins supplies the bias voltage for the integrated high-side MOSFET. A UVLO circuit from BOOT to PH monitors the boot capacitor voltage. This monitoring ensures that the BOOT voltage is sufficient for proper high-side MOSFET gate drive current by allowing the device to pull the PH pin low to recharge the boot capacitor. The TPS54020 can operate at 100% duty cycle during transient conditions while the boot capacitor voltage is higher than the preset BOOT-PH UVLO threshold which is typically 2.1 V. The output voltage can be stepped down to as low as the 0.6-V voltage reference (V_{REF}).

The TPS54020 has a power good comparator (PWRGD) with hysteresis which monitors the output voltage through the VSENSE pin. The PWRGD pin is an open-drain MOSFET which is pulled low when the VSENSE pin voltage is less than 91% or greater than 108% of the reference voltage (V_{REF}) and asserts high when the VSENSE pin voltage is 95% to 104% of V_{REF}.

The SS (soft start) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor or resistor divider should be coupled to the pin for soft start or critical power supply sequencing requirements.

The device has three preset current limit thresholds to fit 10-A, 8-A, and 6-A applications. 表 8-1 shows ILIM pin setting selections.

表 8-1. Current Limit Thresholds

ILIM to RTN IMPEDANCE (kΩ)	CURRENT LIMIT OPTION (A)
NC	10
SHORT	8
499	6

The TPS54020 protects from output overvoltage, overload, and thermal fault conditions. The TPS54020 minimizes excessive output overvoltage transients by taking advantage of the overvoltage circuit power good comparator. When the overvoltage comparator activates, the high-side MOSFET turns off and the device prevents it from turning on until the VSENSE pin voltage is lower than 104% of V_{REF}. The TPS54020 implements both high-side MOSFET overload protection and bi-directional, low-side MOSFET overload protection which helps control the inductor current and avoid current runaway.

The device uses hiccup or cycle-by-cycle overcurrent protection features as listed in 表 8-2.

表 8-2. Overcurrent Protection

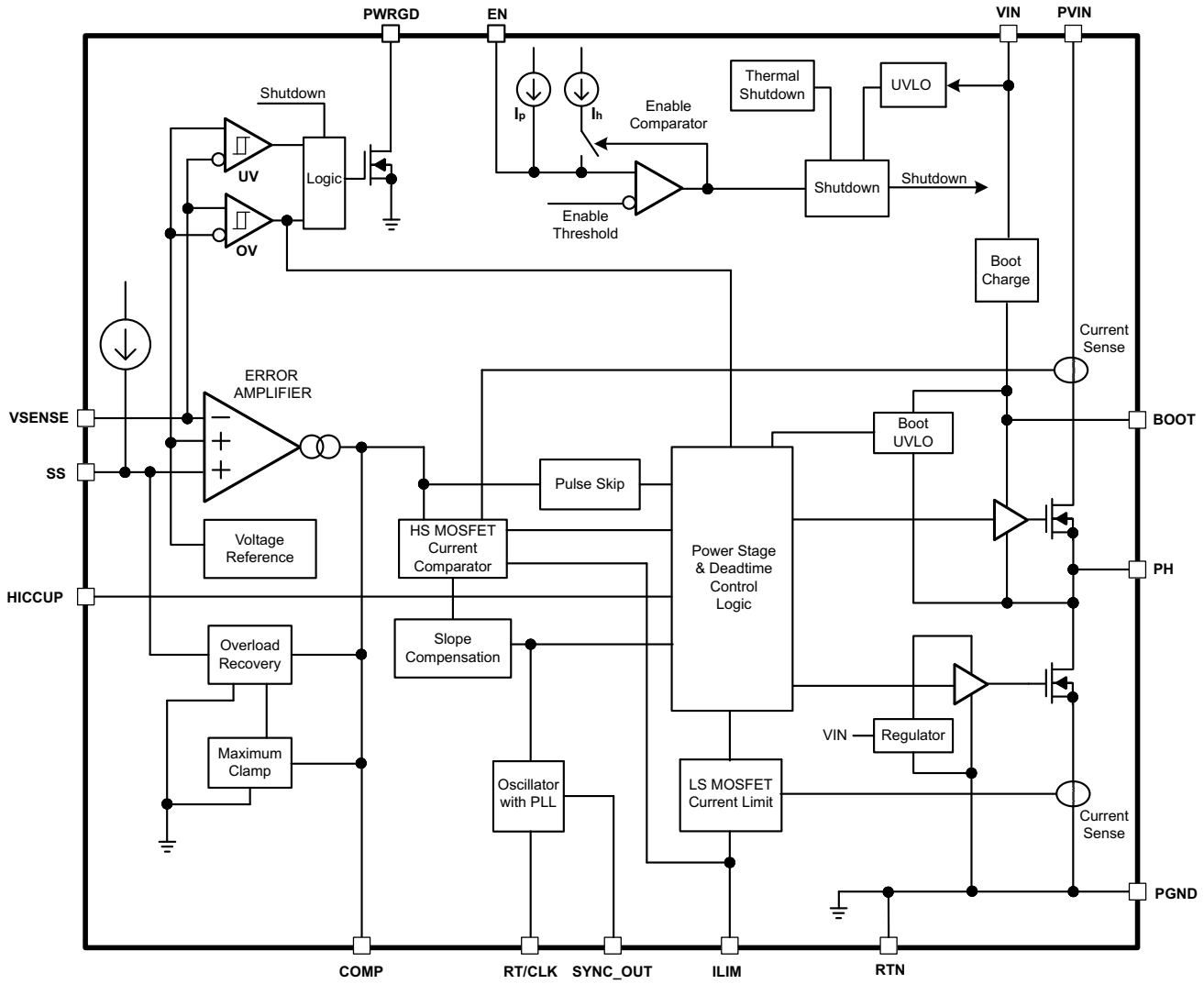
HICCUP TO RTN IMPEDANCE	CURRENT LIMIT OPTION
OPEN	16384 Cycle Hiccup
SHORT	Cycle-Cycle

The TPS54020 shuts down if the junction temperature is higher than the thermal shutdown trip point of 175°C. Once the junction temperature drops to 10°C (typical) below the thermal shutdown trip point, the internal thermal shutdown hiccup timer begins to count. The TPS54020 restarts under the control of the soft-start circuit automatically after the thermal shutdown hiccup time reaches (16384 cycles).

The TPS54020 operates in CCM (continuous conduction mode) at load conditions where the inductor current is always positive (towards the load). To boost efficiency at lighter load conditions, the device enters pulse skipping mode and turns OFF the low-side MOSFET when inductor current tries to reverse.

For applications that require two converters to be synchronized together, the SYNC_OUT and RT/CLK pins can be used. The two converters can be configured to operate 180° out-of-phase by using the SYNC_OUT signal from one of the devices and applying it to the RT/CLK pin of the other device.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fixed Frequency PWM Control

The device uses adjustable fixed-frequency, peak current mode control. External resistors on the VSENSE pin sense the output voltage. The device compares this sensed voltage to an internal 0.6-V voltage reference by a transconductance error amplifier. The resulting error signal is a current, and this current drives the COMP pin.

An internal oscillator initiates the turn ON of the high-side power switch. The device converts the COMP pin voltage into a current reference which is compared to the high-side power switch current. When the power switch current reaches current reference generated by the COMP voltage level, the high-side power switch is turned OFF and the low-side power switch is turned ON until the next clock cycle. At lighter load conditions, the low-side MOSFET turns OFF when the inductor approaches zero, which results in pulse skipping mode.

8.3.2 Input Voltage and Power Input Voltage Pins (VIN and PVIN)

The device allows for a variety of applications by using the VIN and PVIN pins together or separately. The VIN pin voltage supplies the internal control circuits of the device. The PVIN pin voltage provides the input voltage to the power stage of the device. If tied together, the input voltage for VIN and PVIN can range from 4.5 V to 17 V. If using the VIN separately from PVIN, the VIN pin must be between 4.5 V and 17 V, and the PVIN pin can range from as low as 1.6 V to 17 V. The device provides an internal UVLO function on the VIN pin, but in cases where more hysteresis or different thresholds are required, a voltage divider connected to the EN pin can be used. When using an external divider, it is recommended to design the minimum turn OFF threshold at 4.2 V or greater, and the minimum turn ON threshold at 4.4 V or greater. These minimum thresholds are required to avoid interference between the user-defined UVLO threshold levels and the device internal UVLO.

8.3.3 Voltage Reference (V_{REF})

The voltage reference system produces a precise ±1% voltage reference over temperature by scaling the output of a temperature stable bandgap circuit.

8.3.4 Adjusting the Output Voltage

The output voltage is set by the resistor divider network of R_{UPPER} and R_{LOWER}. It is recommended that the lower divider resistor, R_{LOWER}, maintain a range between 1 kΩ and 3 kΩ. During light-load conditions, this resistor range provides enough load current to exceed the bias leakage current that can be sourced by the PH pin. To change the output voltage of a design, it is necessary to change the value of the resistor R_{UPPER}. Changing the value of R_{UPPER} can change the output voltage between 0.6 V and 5 V. The value of R_{UPPER} for a specific output voltage can be calculated using 式 1.

$$R_{UPPER} = \frac{(V_{OUT} - V_{REF}) \times R_{LOWER}}{V_{REF}} \quad (1)$$

The minimum output setpoint voltage cannot be less than the reference voltage of 0.6 V, but it can also be limited by the minimum ON time of the high-side MOSFET. The maximum output voltage can be limited by bootstrap voltage (BOOT-PH voltage). See more details located in *セクション 9.2.2.9.1* and *セクション 8.3.12*.

8.3.5 Safe Start-up into Prebiased Outputs

The device prevents the low-side MOSFET from discharging a pre-biased output. During pre-biased start-up, the low-side MOSFET does not turn on until the high-side MOSFET has started switching. The high-side MOSFET does not start switching until the soft-start voltage exceeds the voltage at the VSENSE pin.

8.3.6 Error Amplifier

The transconductance error amplifier compares the VSENSE pin voltage to either the SS pin voltage or the internal 0.6-V voltage reference, whichever is lower. The transconductance of the error amplifier is 1300 µA/V during normal operation. The frequency compensation network is connected between the COMP pin and ground.

8.3.7 Slope Compensation

The device adds a compensating ramp to the switch current signal. This slope compensation prevents subharmonic oscillations when operating conditions demand greater than 50% duty cycle. The available peak inductor current remains constant over the full duty cycle range.

8.3.8 Enable and Adjusting Undervoltage Lockout

The EN pin provides electrical on and off control of the device. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low quiescent state. The EN pin has an internal hysteretic current source, allowing the user to design the ON and OFF threshold voltages with a resistor divider at the EN pin. If an application requires controlling the EN pin, use open drain or open collector output logic to interface with the pin.

The EN pin can be configured as shown in 図 8-1, 図 8-2, and 図 8-3. It is recommended to set the UVLO hysteresis to be greater than 500 mV to avoid repeated chatter during start-up or shutdown. The EN pin has a small fixed pullup current i_P which sets the current source value before the start-up sequence. The device includes the second current source i_H when the threshold voltage has been exceeded. To achieve clean transitions between the OFF and ON states, TI recommendeds that the turn OFF threshold is no less than 4.2 V, and the turn ON threshold is no less than 4.4 V on the VIN pin.

The UVLO thresholds can be calculated using 式 2 and 式 3.

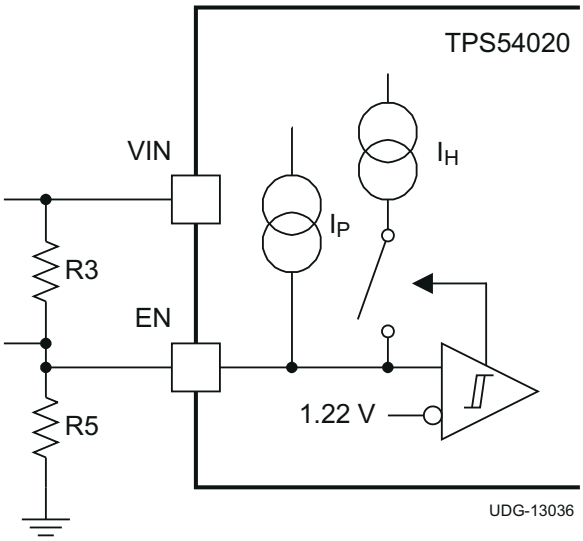


図 8-1. Adjustable VIN Undervoltage Lockout

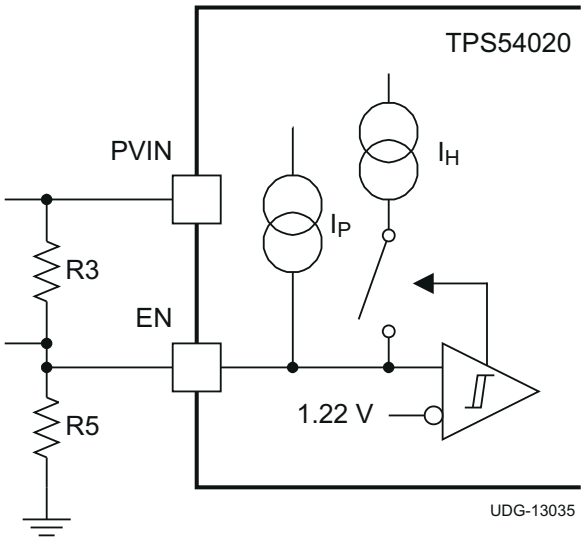


図 8-2. Adjustable PVIN Undervoltage Lockout, PVIN ≥ 4.5 V

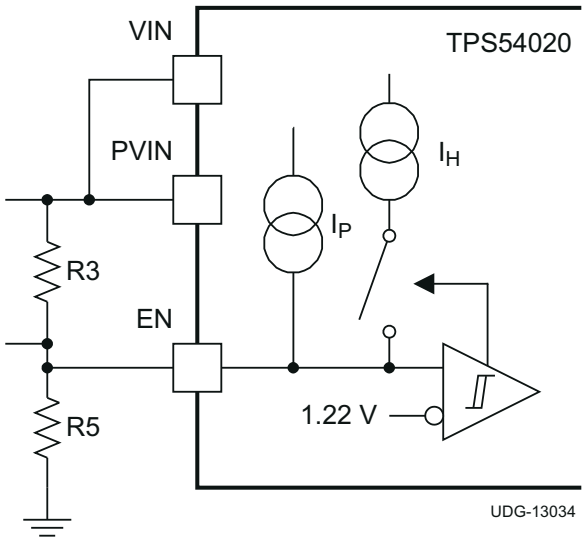


図 8-3. Adjustable VIN and PVIN Undervoltage Lockout

R3, the top UVLO divider resistor, is calculated using 式 2.

$$R3 = \frac{V_{START} \times \left(\frac{V_{EN(falling)}}{V_{EN(rising)}} \right) - V_{STOP}}{I_P \times \left(1 - \frac{V_{EN(falling)}}{V_{EN(rising)}} \right) + I_H} \quad (2)$$

R5, the bottom UVLO divider resistor, is calculated in 式 3.

$$R5 = \frac{R3 \times V_{EN(falling)}}{V_{STOP} - V_{EN(falling)} + R3 \times (I_P + I_H)} \quad (3)$$

In this example:

- I_H = 3.3 µA
- I_P = 1.15 µA
- $V_{ENRISING}$ = 1.22 V
- $V_{ENFALLING}$ = 1.17 V

8.3.9 Adjustable Switching Frequency and Synchronization (RT/CLK)

The RT/CLK pin can be used to set the switching frequency of the device in two modes. In RT mode, a resistor (RT resistor) is connected between the RT/CLK pin and GND. The switching frequency of the device is adjustable from 200 kHz to 1200 kHz. In CLK mode, an external clock is connected directly to the RT/CLK pin. The device is synchronized to the external clock frequency with an internal PLL. The CLK mode overrides the RT mode. The device detects the proper mode automatically and switches from RT mode to CLK mode. See *セクション 8.4* for more information.

8.3.10 Soft-Start (SS) Sequence

The device has two non-inverting inputs to the error amplifier. One input is the 0.6-V reference (V_{REF}) , and the other is the SS pin voltage. The device regulates to the lower of these two voltages. A capacitor on the SS pin to ground implements a soft-start time. The internal pullup current source of 2.3 µA charges the external soft-start

capacitor. The calculations for the soft-start time (t_{SS}, 10% to 90%) and soft-start capacitor (C_{SS}) are shown in 式 4. The voltage reference (V_{REF}) is 0.6 V and the soft-start charge current (I_{SS}) is 2.3 µA.

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{REF}} \quad (4)$$

where

- C_{SS} is the soft-start capacitance in nF
- I_{SS} is the soft-start current in µA
- t_{SS} is the soft-start time in ms
- V_{REF} of the voltage reference in V

The device stops switching and enters low-current operation when either the input voltage UVLO is triggered, the EN pin is pulled below 1.2 V, or if a thermal shutdown event occurs. During the subsequent power up sequence, when the shutdown condition is removed, the device does not start switching until it has discharged the SS pin to ground ensuring proper soft-start behavior.

8.3.11 Power Good (PWRGD)

The PWRGD pin is an open drain output. Once the VSENSE pin is between 95% and 104% of the internal voltage reference the PWRGD pin pull-down is deasserted and the pin floats. It is recommended to use a pullup resistor between the values of 10kΩ and 100kΩ to a voltage source that is 5.5V or less. The PWRGD is in a defined state once the VIN input voltage is greater than 1V but with reduced current sinking capability. The PWRGD achieves full current sinking capability once the VIN input voltage is above 4.5V. The PWRGD pin is pulled low when the VSENSE pin voltage is lower than 91% or greater than 108% of the nominal internal reference voltage. Also, the PWRGD is pulled low if the input UVLO or thermal shutdowns are asserted, or the EN pin is pulled low, or the SS pin voltage is below 1.4 V.

8.3.12 Bootstrap Voltage (BOOT) and Low Dropout Operation

The device has an integrated bootstrap voltage regulator and requires a small ceramic capacitor between the BOOT and PH pins to provide the gate drive voltage for the high-side MOSFET. The boot capacitor is charged when the BOOT pin voltage is less than VIN and BOOT-PH voltage is below regulation. The value of this ceramic capacitor should be 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics over temperature and voltage. To improve dropout, the device is designed to operate at 100% duty cycle as long as the BOOT-to-PH pin voltage is greater than the BOOT-PH UVLO threshold, which is typically 2.1 V. When the voltage between BOOT and PH drops below the BOOT-PH UVLO threshold, the high-side MOSFET is turned off and the low-side MOSFET is turned on, allowing the boot capacitor to be recharged. In applications with split input voltage rails, 100% duty cycle operation can be achieved as long as (VIN – PVIN) > 4 V. However, if the TPS54020 is configured for hiccup overcurrent protection, hiccup also occurs if the input voltage is insufficient to regulate the output voltage for longer than the hiccup wait time. If continuous operation at 100% duty cycle is needed, configure the TPS54020 for cycle-by-cycle current limit.

8.3.13 Sequencing (SS)

Many of the common power supply sequencing methods can be implemented using the SS, EN, and PWRGD pins. The sequential method is illustrated in 図 8-4 using two TPS54020 devices. The power good of the first device is coupled to the EN pin of the second device which enables the second power supply once the primary supply reaches regulation.

図 8-5 shows the method of implementing ratio-metric sequencing by connecting the SS pins of the two devices together. The regulator outputs ramp up and reach regulation at the same time. When calculating the soft-start time, the pullup current source must be doubled in 式 4.

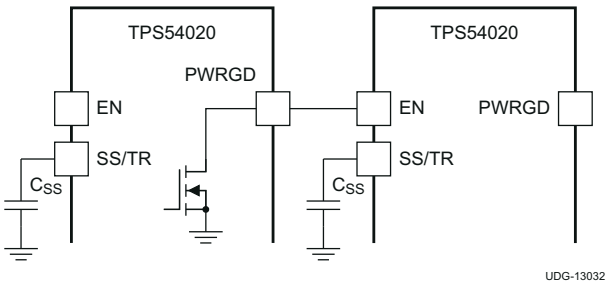


図 8-4. Sequential Start-up Sequence

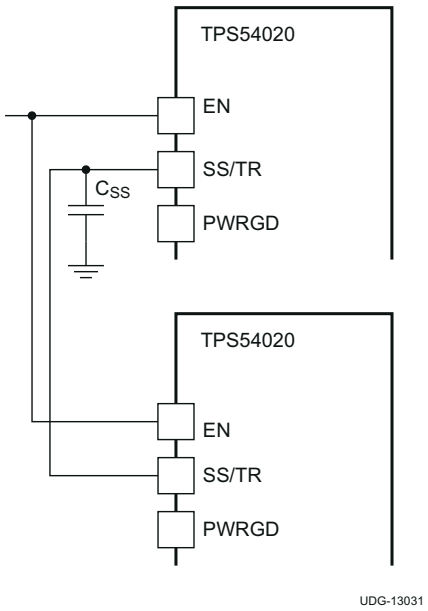


図 8-5. Ratiometric Start-up Sequence

Ratio-metric and simultaneous power supply sequencing can be implemented by connecting the resistor network of RS1 and RS2 shown in 図 8-6 to the output of the power supply to which to be tracked, or alternately another voltage reference source. Using 式 5 and 式 6, the tracking resistors can be calculated to initiate the V_{OUT2} slightly before, after, or at the same time as V_{OUT1}. 式 7 is the voltage difference between V_{OUT1} and V_{OUT2}. To design a ratio-metric start-up where the V_{OUT2} voltage is slightly greater than the V_{OUT1} voltage when V_{OUT2} reaches regulation, use a negative number in 式 5 and 式 6 for ΔV. 式 7 results in a positive number for applications where V_{OUT2} is slightly lower than V_{OUT1} when V_{OUT2} regulation is achieved. The ΔV variable is zero volts for simultaneous sequencing. To minimize the effect of the inherent SS to VSENSE offset ($V_{SS(offset)}$, 29 mV) in the soft-start circuit and the offset created by the pullup current source (I_{SS}, 2.3 µA) and tracking resistors, $V_{SS(offset)}$ and I_{SS} are included as variables in the equations. To ensure start-up of V_{OUT2} after a fault, the calculated RS1 value from 式 5 must be greater than the value calculated in 式 8.

$$RS1 = \frac{V_{OUT2} + \Delta V}{V_{REF}} \times \frac{V_{SS(offset)}}{I_{SS}} \tag{5}$$

$$RS2 = \frac{V_{REF} \times RS1}{V_{OUT2} + \Delta V - V_{REF}} \tag{6}$$

$$\Delta V = V_{OUT1} - V_{OUT2} \tag{7}$$

$$RS1 = 19000 \times V_{OUT1} \tag{8}$$

There are two important considerations when using a resistor divider to the SS/TR pin for simultaneous start-up. First, as described in セクション 8.3.11, for the PWRGD output to be active, the SS/TR voltage must be above 1.4 V max. The external divider can prevent the SS/TR voltage from charging above the threshold. For the SS/TR pin to charge above the threshold, a switch can be needed to disconnect the resistor divider or modify the resistor divider ratio of the V_{OUT2} converter after start-up is complete. The PWRGD pin of the V_{OUT1} converter can be used for this. One solution is to add a resistor from SS/TR of the V_{OUT2} converter to the PWRGD of the V_{OUT1} converter. While the PWRGD of V_{OUT1} pulls low, this resistor will be in parallel with RS2. When V_{OUT1} is in regulation its PWRGD pin will float. If the PWRGD pin of V_{OUT1} is connected to a pullup voltage, make sure to include this in calculations. A second option is to use the PWRGD pin to turn on or turn off the external switch to change the divide ratio. The second consideration is that a pre-bias on V_{OUT1} can prevent V_{OUT2} from turning on.

When the TPS54020 is enabled, an internal 500-Ω switch at the SS/TR pin turns on to discharge the SS/TR voltage as described in セクション 8.3.10. The SS/TR pin voltage must discharge below 26 mV before the TPS54020 starts up. If the upper resistor at the SS/TR pin is too small, the SS/TR pin does not discharge below the threshold, and V_{OUT2} does not ramp up. The upper resistor in the SS/TR divider may need to be increased to allow the SS/TR pin to discharge below the threshold.

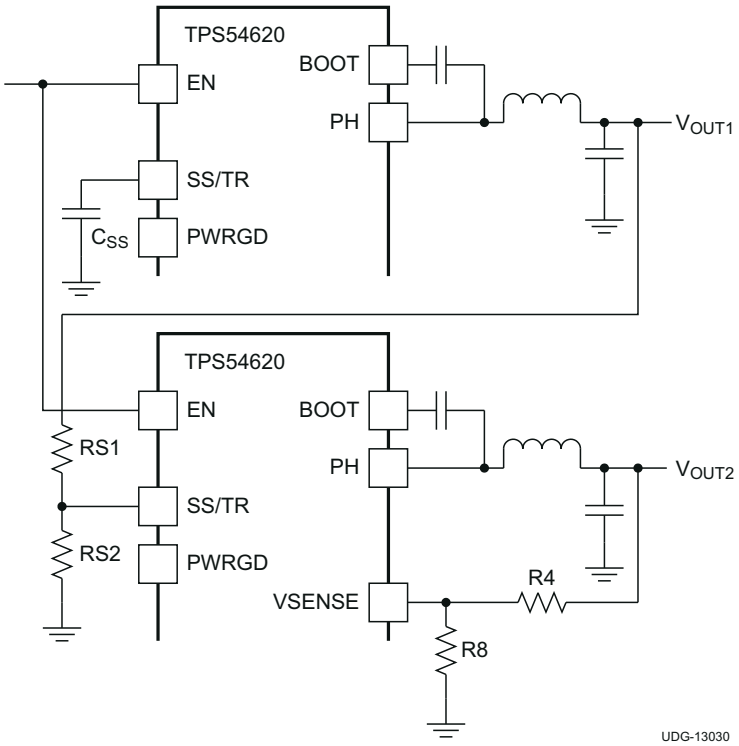


図 8-6. Ratiometric and Simultaneous Start-up Sequence

8.3.14 Output Overvoltage Protection (OVP)

The device incorporates an output overvoltage protection (OVP) circuit to minimize output voltage overshoot. For example, when the load current is abruptly reduced from a high value to a low value, the output voltage response can exceed the OVP trip threshold, especially if the capacitance on the output voltage bus is relatively low value. The OVP feature minimizes the overshoot by comparing the VSENSE pin voltage to the OVP threshold. If the VSENSE pin voltage is greater than the OVP threshold the high-side MOSFET is turned OFF. The OVP threshold is the same as the VSENSE rising (fault) threshold of 108%. When the VSENSE voltage drops lower than the VSENSE falling (good) threshold of 104%, the high-side MOSFET is allowed to turn on at the next clock cycle.

During an OVP event, the low-side reverse current limit still applies, and the device does not allow current flow into the PH pin.

8.3.15 Overcurrent Protection

The device is protected from overcurrent conditions with cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET.

8.3.15.1 High-side MOSFET Overcurrent Protection

The device implements current mode control which uses the COMP pin voltage to control the turnoff of the high-side MOSFET and the turnon of the low-side MOSFET on a cycle-by-cycle basis. Each cycle, the switch current and the current reference generated by the COMP pin voltage are compared. The high-side switch is turned off when the peak switch current intersects the current reference. High-side overcurrent protection is achieved by clamping the current reference.

8.3.15.2 Low-side MOSFET Overcurrent Protection

While the low-side MOSFET is turned on, its conduction current is monitored by the internal circuitry. During normal operation, the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally-set low-side sourcing current limit. If the low-side sourcing current is exceeded, the high-side MOSFET is not turned on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET is turned on again when the low-side MOSFET current is less than the low-side MOSFET sourcing current limit at the start of a cycle.

To boost efficiency in light load conditions, the control circuitry does not allow the low-side MOSFET to sink current from the load. When negative low-side MOSFET current is detected, the low-side MOSFET is turned OFF immediately for the rest of that clock cycle. In this scenario, both MOSFETs are off until the start of the next cycle.

Additionally, if an output overload condition (as measured by the COMP pin voltage) has lasted for more than the hiccup wait time which is programmed for 128 switching cycles, the device shuts down and restarts only after the hiccup time of 16384 cycles has elapsed. The hiccup mode helps to reduce the device power dissipation under severe overcurrent conditions.

8.3.16 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds a nominal value of 175°C. Once the junction temperature drops below 165°C typically, the internal thermal hiccup timer begins to count. The device reinitiates the power up sequence after the built-in thermal shutdown hiccup time of 16384 cycles has elapsed.

8.4 Device Functional Modes

8.4.1 Single-Supply Operation

The TPS54020 is designed to operate from either a single input voltage, or split control logic and power stage supplies. To operate the TPS54020 from a single supply voltage, connect the VIN pin to the power stage PVIN strip.

8.4.2 Split Rail Operation

The TPS54020 is designed to be able to operate from separate VIN and PVIN voltages. Bias for the control logic is provided by VIN. Power conversion input is provided by PVIN. Note that the minimum recommended VIN voltage is 4.5 V, while the minimum PVIN voltage can be as low as 1.6 V, both have a maximum recommended operating voltage of 17 V.

8.4.3 Continuous Current Mode Operation (CCM)

As a synchronous buck converter, the device normally works in CCM (continuous conduction mode) under load conditions where the inductor current is always positive. It is possible for the device to exhibit extended ON or OFF times (longer than 1 clock cycle) during large signal conditions such as a severe load up-transient (extended ON time) or current limit or OV (extended OFF time).

8.4.4 Eco-mode Light-Load Efficiency Operation

The TPS54020 operates in pulse skip mode (see 図 8-9) at light-load currents to improve efficiency by reducing switching, gate drive, and circulating current losses. When the output voltage is in regulation and the peak switch current at the end of any switching cycle remains below the pulse skipping current threshold, the device enters pulse skip mode. This current threshold is the current level corresponding to a nominal COMP voltage of 270 mV.

When in pulse skip mode, the device clamps the COMP pin voltage to 270 mV and inhibits the high-side MOSFET. Further decreases in load current cannot drive the COMP pin below this clamp voltage level.

When the device is not switching while in pulse skip mode, the output voltage tends to decay. As the voltage control loop compensates for the falling output voltage, the COMP pin voltage begins to rise. At this time, the device enables the high-side MOSFET, and a switching pulse initiates on the next clock cycle. The COMP pin voltage sets the peak switch current. The output voltage re-charges to the regulation set point value, and then

the demand for peak switch current will decrease. Eventually, the COMP pin voltage once again falls below the pulse skip mode threshold, at which time the device again enters pulse skip mode.

Bias circuits in the BOOT regulator and high-side MOSFET gate drive both return bias current out from the PH pin. While this current is small and in the range of 150 µA (nominal), during very light load conditions, it is possible that the output voltage rises above the desired output voltage setpoint due to this current. If the application design anticipates that system loads can fall below this current level, it is recommended to add a fixed resistor load to the design that dissipates this current. An easy implementation of this fixed load can be achieved with the feedback voltage divider resistors. The recommendation is to use a lower divider resistor value of 2.5 kΩ or lower in this case, and this lower divider resistor should be installed even when the output voltage setpoint is 0.6 V.

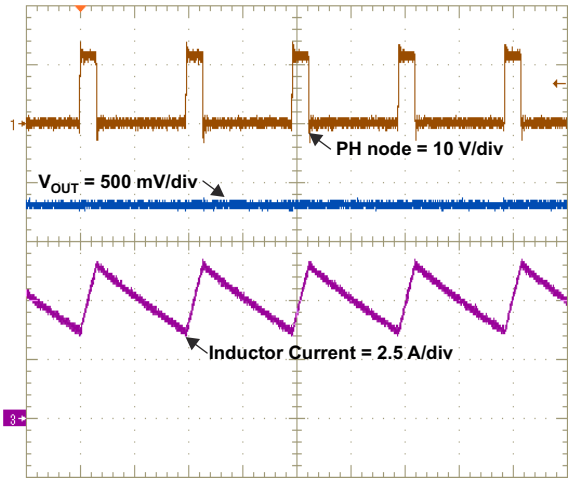


図 8-7. TPS54020 in Continuous Conduction Mode

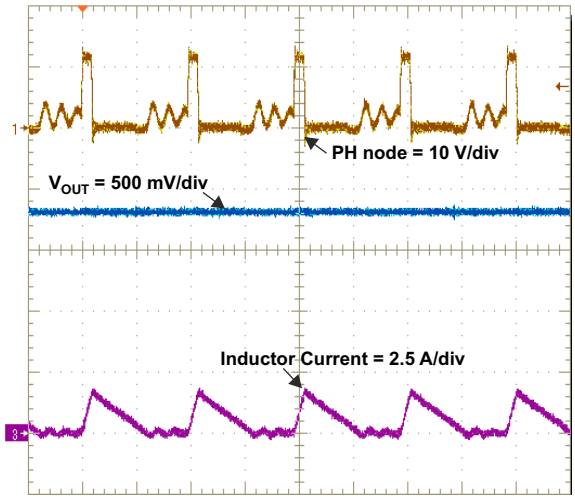


図 8-8. TPS54020 in Discontinuous Conduction Mode

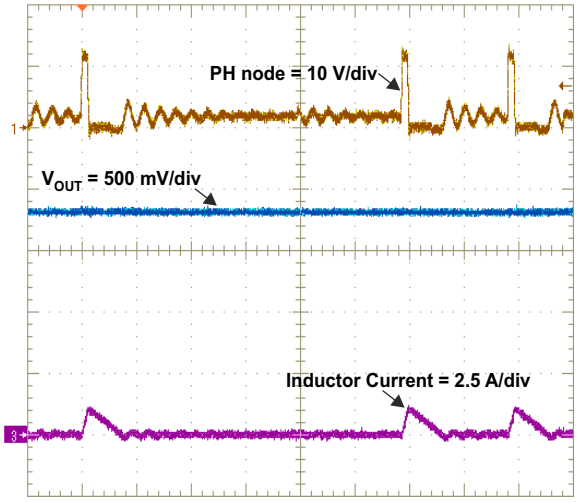


図 8-9. TPS54020 in Pulse Skipping Mode

8.4.5 Adjustable Switching Frequency (RT Mode)

To determine the R_{RT} resistance for a given switching frequency, use 式 9, or the curve in 図 8-10. In an attempt to reduce the overall solution size, the temptation is to set the switching frequency as high as possible, but the designer should consider the minimum controllable on-time and the tradeoff between f_{SW} and supply efficiency.

$$f_{SW} = 42533.5 \times (R_{RT})^{-0.964356} \quad (9)$$

where

- R_{RT} is in kΩ
- f_{SW} is in kHz

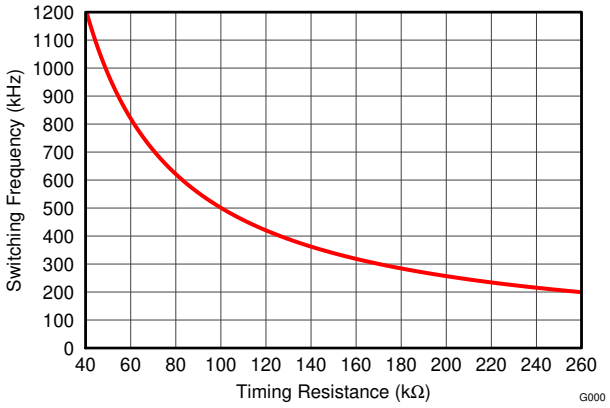


図 8-10. Timing Resistance vs Switching Frequency

8.4.6 Synchronization (CLK Mode)

An internal phase locked loop (PLL) has been implemented to allow synchronization at frequencies between 200 kHz and 1200 kHz, and to easily switch from RT mode to CLK mode. To implement the synchronization feature, connect a square wave clock signal to the RT/CLK pin with a duty cycle between 20% and 80%. The clock signal amplitude must transition lower than 0.8 V and higher than 2.0 V. The start of the switching cycle is synchronized to the falling edge of RT/CLK pin. In applications where both RT mode and CLK mode are needed, the device can be configured as shown in 図 8-11. Before the external clock is present, the device functions in RT mode and the switching frequency is set by the R_{RT} resistor. When the external clock is present, the CLK mode overrides the RT mode. The first time the SYNC pin is pulled above the RT/CLK high threshold (2.0 V), the device switches from RT mode to CLK mode and the RT/CLK pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock. It is not recommended to switch from CLK mode to RT mode because the internal switching frequency decreases to 100 kHz first before returning to the switching frequency set by the R_{RT} resistor.

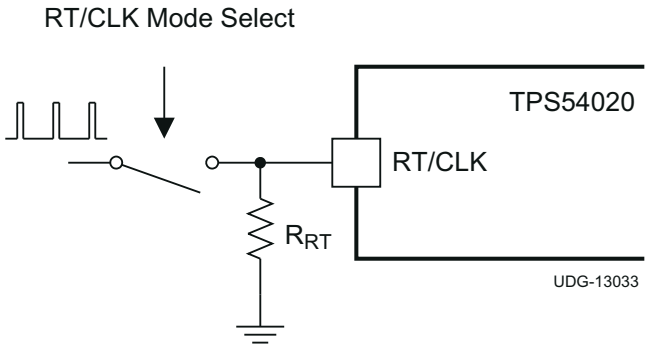


図 8-11. Synchronization to External CLK and Rt Mode Interface

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Small Signal Model for Loop Response

図 9-1 shows an equivalent model for the device control loop which can be modeled in a circuit simulation program to check frequency response and transient responses. The error amplifier is a transconductance amplifier with a gm of 1300 µA/V. The error amplifier can be modeled using an ideal voltage controlled current source. The resistor R_{OEA} (2.38 MΩ) and capacitor $C_{OUT(ea)}$ (20.7 pF) model the open loop gain and frequency response of the error amplifier. A low amplitude (between 10 mV and 100 mV AC) voltage source between node **a** and node **b** effectively breaks the control loop for the frequency response measurements. Plotting the designators **a-c** yields the small signal response of the plant, and plotting designators **c-b** yields the small signal response of the frequency compensation. Plotting designators **a-b** yields the small signal response of the overall loop. The dynamic loop response can be simulated by replacing the R_{LOAD} with a current source with the appropriate load step amplitude and step rate in a time domain analysis.

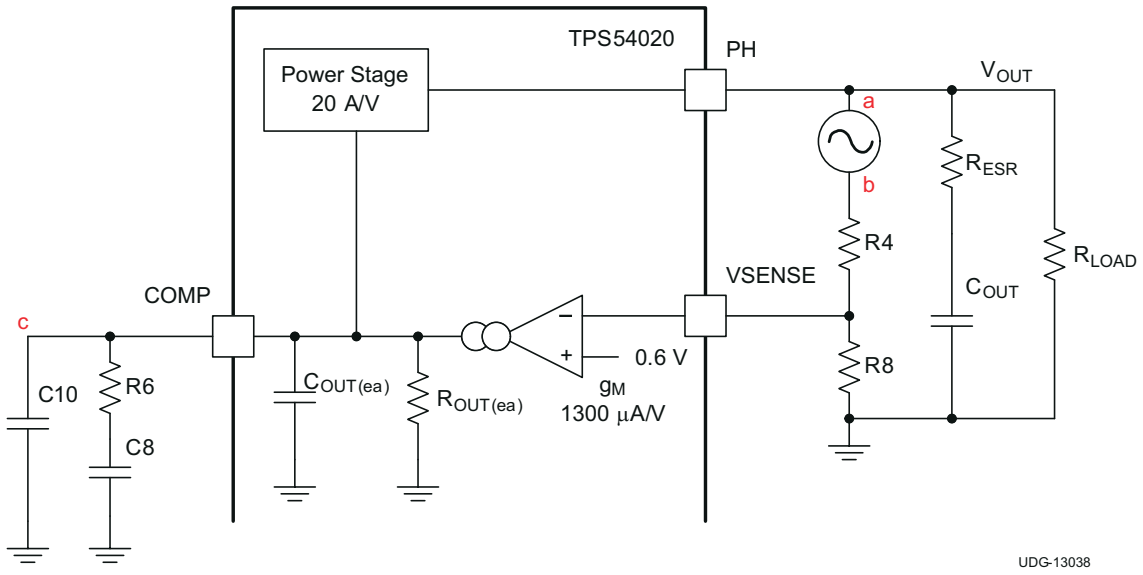


図 9-1. Small Signal Model for Loop Response

9.1.2 Simple Small Signal Model for Peak Current Mode Control

図 9-2 is a small signal model that can be used to understand how to design the frequency compensation network. This is a simplified model that does not include the effects of slope compensation. The device power stage, or Plant, can be approximated by a voltage controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor. The control to output transfer function is shown in 式 10 and consists of a dc gain, one dominant pole and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in 図 9-1) is the power stage transconductance (gm_{ps}) which is 20 A/V for the TPS54020 (when ILIM is open). The DC gain or amplification of the power stage, A_{DC}, is the product of gm_{ps} and the load resistance RL as shown in 式 11 with resistive loads. As the load current increases, the DC gain decreases. This variation with load may seem problematic at first glance, but fortunately the dominant pole moves with load current (see 式 12). The combined effect is highlighted by the dashed line in 図 9-3. As the load

current decreases, the gain increases and the pole frequency reduces, keeping the 0-dB crossover frequency the same for the varying load conditions which makes it easier to design the frequency compensation.

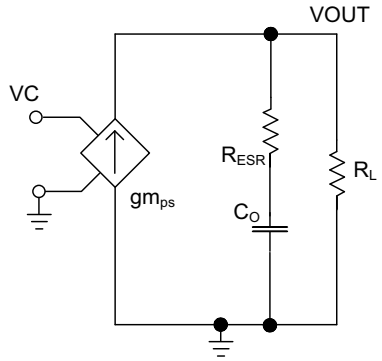


図 9-2. Simplified Small Signal Model for Peak Current Mode Control

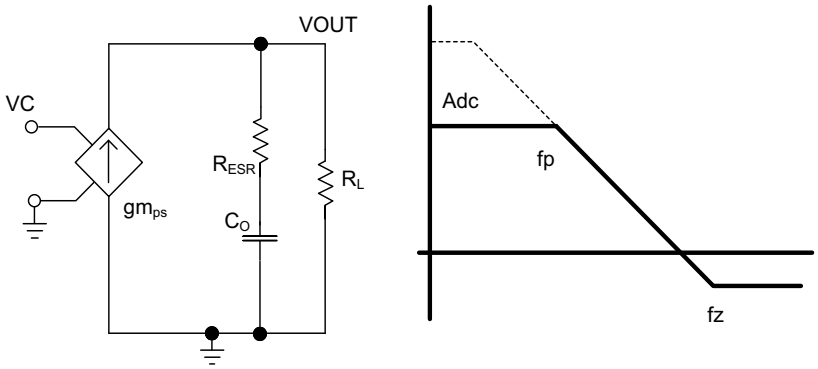


図 9-3. Simplified Frequency Response for Peak Current Mode Control

The simplified control-to-output transfer function is shown in 式 10.

$$\frac{V_{OUT}}{V_C} = Adc \times \frac{1+\left(\frac{s}{2\pi \times f_Z}\right)}{1+\left(\frac{s}{2\pi \times f_P}\right)} \tag{10}$$

The power stage DC gain is shown in 式 11.

$$Adc = g_{M(PS)} \times R_{LOAD} \tag{11}$$

The pole from load is show in 式 12.

$$f_P = \frac{1}{C_{OUT} \times R_{LOAD} \times 2\pi} \tag{12}$$

To calculate the zero from the capacitor ESR use 式 13.

$$f_Z = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi} \quad (13)$$

where

- $g_{M(ea)}$ is the transconductance amplifier gain (1300 µA/V)
- $g_{M(ps)}$ is the power stage gain (20 A/V)
- R_{LOAD} is the load resistance
- C_{OUT} is the output capacitance
- R_{ESR} is the equivalent series resistance of the output capacitor

9.1.3 Small Signal Model for Frequency Compensation

The device uses a transconductance amplifier for the error amplifier and readily supports two of the commonly used Type II compensation circuits and a Type III frequency compensation circuit, as shown in 図 9-4. In Type IIA, one additional high frequency pole, C10, is added to attenuate high frequency noise. In Type III, one additional capacitor, C7, is added to provide a phase boost at the crossover frequency. See *Designing Type III Compensation for Current Mode Step-Down Converters* (SLVA352) for a complete explanation of Type III compensation.

The design guidelines described in *セクション 9.1.4* are provided for advanced designers who prefer to compensate using the general method. The following equations apply only to designs in which ESR zero is above the bandwidth of the control loop. This is usually true with ceramic output capacitors.

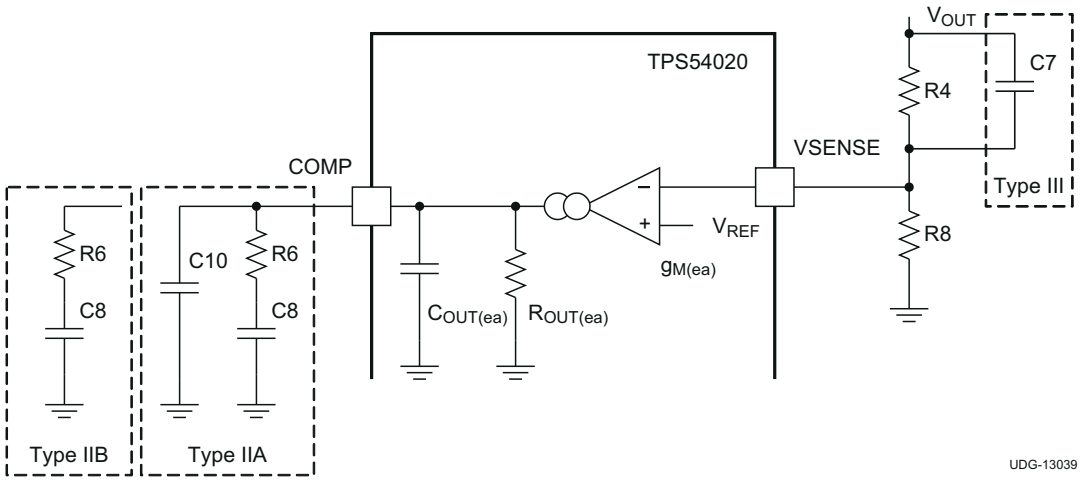


図 9-4. Types of Frequency Compensation

Note

The comp-to-switch transconductance $g_{M(ps)}$ is dependent on the current limit level that is selected. If a different current limit option is selected, the compensation needs to be redesigned with the new $g_{M(ps)}$.

9.1.4 Designing the Device Loop Compensation

The general design guidelines for device loop compensation are shown in this section.

9.1.4.1 Step One: Determine the Crossover Frequency (f_C)

To begin, choose 1/10th of the switching frequency, f_{SW}

9.1.4.2 Step Two: Determine a Value for R6

Resistor R6 is calculated in 式 14.

$$R6 = \frac{2\pi \times C_{OUT} \times f_C \times V_{OUT}}{g_{M(ea)} \times V_{REF} \times g_{M(ps)}} \quad (14)$$

where

- $g_{M(ea)}$ is the transconductance amplifier gain (1300 µA/V)
- $g_{M(ps)}$ is the power stage gain (20 A/V)
- V_{REF} is the reference voltage (0.6 V)

9.1.4.3 Step Three: Calculate the Compensation Zero.

Place a compensation zero at the dominant pole found in 式 12. The zero is achieved by the combination of R6 and C8, which is calculated in 式 15.

$$C8 = \frac{C_{OUT} \times R_{LOAD}}{R6} \quad (15)$$

9.1.4.4 Step Four: Calculate the Compensation Noise Pole.

C10 is optional. It can be used to cancel the zero from the ESR (equivalent series resistance) of the output capacitor (C_{OUT}).

$$C10 = \frac{R_{ESR} \times C_{OUT}}{R6} \quad (16)$$

9.1.4.5 Step Five: Calculate the Compensation Phase Boost Zero.

Type III compensation can be implemented with the addition of one capacitor, C7. This addition allows for slightly higher loop bandwidths and higher phase margins. If used, C7 is calculated from 式 17

$$C7 = \frac{1}{2\pi \times R4 \times f_C} \quad (17)$$

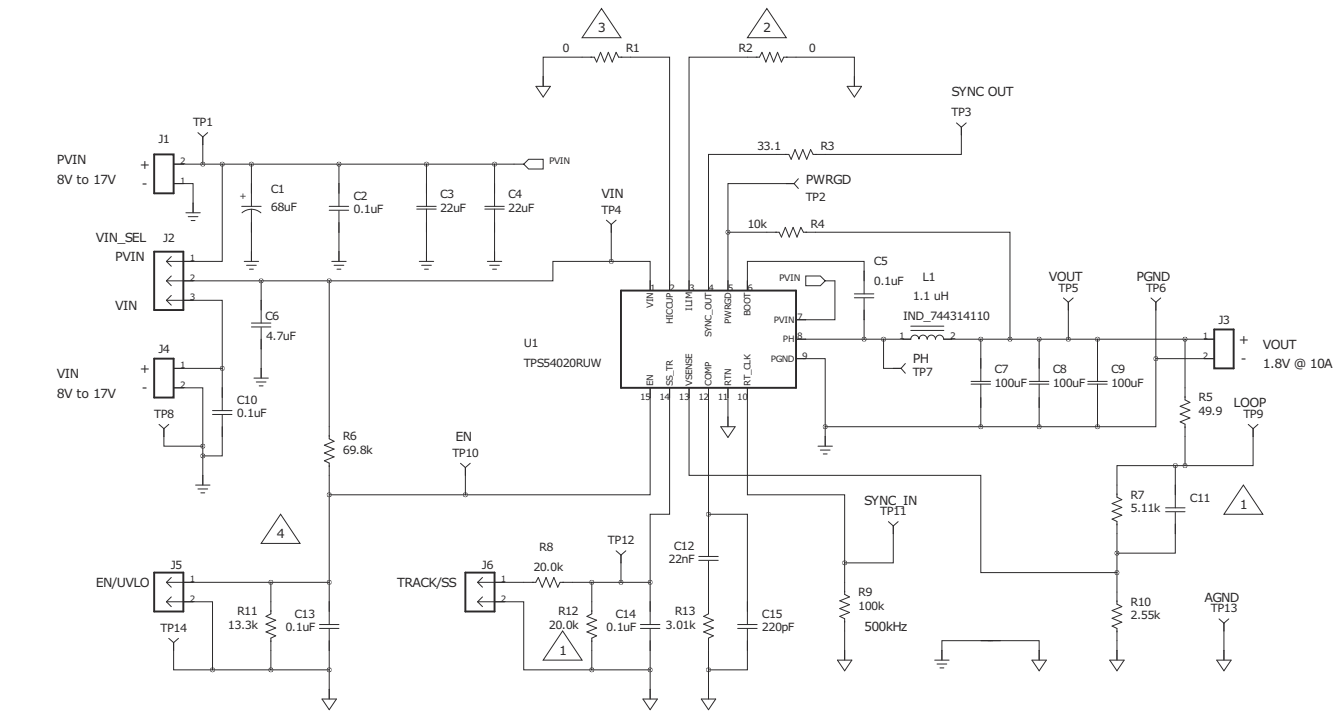
9.1.5 Fast Transient Considerations

In applications where fast transient responses are very important, Type III frequency compensation can be used instead of the traditional Type II frequency compensation.

For more information about Type II and Type III frequency compensation circuits, see *Designing Type III Compensation for Current Mode Step-Down Converters* (SLVA352).

9.2 Typical Application

The application schematic shown in 図 9-5 meets the requirements shown in 表 9-1. This circuit is available as the TPS54020EVM-082 evaluation module. The design procedure is given in this section. For more information about Type II and Type III frequency compensation circuits, see *Designing Type III Compensation for Current Mode Step-Down Converters* (SLVA352).



NOTES:

1. DO NOT INSTALL
2. ILIM_SEL
   9.4A: INSTALL R2 = 500k ohms
   12.75A: INSTALL R2 = short
   15A: REMOVE R2
3. HICCUP_SEL
   CYCLE-CYCLE: INSTALL R1
   16384 CYCLES: REMOVE R1
4. R6 and R11 yield Von = 7.5V, Voff = 7.1V

図 9-5. Typical Application Circuit

9.2.1 Design Requirements

A few parameters must be known in order to start the design process. These parameters are typically determined at the system level. For this example, we start with the known parameters shown in 表 9-1.

表 9-1. Design Example Characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage			1.8		V
I_{OUT}	Output current			10		A
	Transient response	5-A load step		ΔV_{OUT} ≤ 5 %		A
V_{IN}	Input voltage		8	12	17	V
$V_{OUT(ripple)}$	Output voltage ripple			10		$mV_{(P-P)}$
	Start input voltage	Rising input voltage		7.5		V
	Stop Input Voltage	Falling input voltage		7.1		V
f_{SW}	Switching Frequency			500		kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS54020 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.

3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

This example details the design of a high frequency switching regulator design using ceramic output capacitors.

9.2.2.2 Operating Frequency

The first step is to decide on a switching frequency for the regulator. There is a tradeoff between higher and lower switching frequencies. Higher switching frequencies can produce smaller a solution size using lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the higher switching frequency causes extra switching losses, which reduce the efficiency of the converter and thermal performance. In this design, a moderate switching frequency of 500 kHz is selected to achieve both a small solution size and a high efficiency operation.

9.2.2.3 Output Inductor Selection

To calculate the value of the output inductor, use 式 18. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impact the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, K_{IND} is normally from 0.1 to 0.3 for the majority of applications.

$$L_{OUT} = \frac{V_{IN(max)} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN(max)} \times f_{SW}} \tag{18}$$

For this design example, use K_{IND} = 0.3 and the inductor value is calculated to be 1.07 µH. For this design, a nearest standard value was chosen at 1 µH. For the output filter inductor, it is important that the rms current and saturation current ratings not be exceeded. The rms and peak inductor current are calculated in 式 19 and 式 20.

$$I_{RIPPLE} = \frac{\left(V_{IN(max)} - V_{OUT}\right)}{L1} \times \frac{V_{OUT}}{V_{IN(max)} \times f_{SW}} \tag{19}$$

$$I_{L(rms)} = \sqrt{\left(I_{OUT}\right)^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{V_{IN(max)} \times L1 \times f_{SW}} \right)^2} \tag{20}$$

$$I_{L(peak)} = I_{OUT} + \left(\frac{I_{RIPPLE}}{2} \right) \tag{21}$$

For this design, the rms inductor current is calculated to be 10.04 A and the peak inductor current is 11.6 A.

The chosen inductor is 1.0 µH, with a saturation current rating of 13 A. The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults, or transient load conditions, the inductor current can increase above the peak inductor current level calculated above. In transient conditions, the

inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

9.2.2.4 Output Capacitor Selection

There are three primary considerations for selecting the value of the output capacitor. The output capacitor affects three criteria:

- how the regulator responds to a change in load current or load transient
- the output voltage ripple
- the amount of capacitance on the output voltage bus

The last of these three considerations is important when designing regulators that must operate where the electrical conditions are unpredictable. The output capacitance needs to be selected based on the most stringent of these three criteria.

9.2.2.4.1 Response to a Load Transient

The desired response to a load transient is the first criteria. The output capacitor needs to supply the load with the required current when not immediately provided by the regulator. When the output capacitor supplies load current, the impedance of the capacitor greatly affects the magnitude of voltage deviation during the transient.

In order to meet the requirements for control loop stability, this peak current mode regulator requires the addition of compensation components in the design of the error amplifier. While these compensation components provide for a stable control loop, they often also reduce the speed with which the regulator can respond to load transients. The delay in the regulator response to load changes can be two or more clock cycles before the control loop reacts to the change. During that time, the difference between the old and the new load current must be supplied (or absorbed) by the output capacitance. The output capacitor impedance must be designed to be able to supply or absorb the delta current while maintaining the output voltage within acceptable limits. 式 22 calculates the minimum capacitance necessary to limit the voltage deviation based on a delay of two switching cycles.

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} \tag{22}$$

where

- ΔI_{OUT} is the change in output current
- f_{SW} is the switching frequency
- ΔV_{OUT} is the allowable change in the output voltage

For this example, the transient load response is specified as a 5% change in V_{OUT} for a load step of 5 A. For this example, ΔI_{OUT} = 5 A and ΔV_{OUT} = 0.05 × 1.8 = 0.09 V. Using these numbers gives a minimum capacitance of 222 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

9.2.2.4.2 Output Voltage Ripple

The output voltage ripple is the second criteria. 式 23 calculates the minimum output capacitance required to meet the output voltage ripple specification.

$$C_{OUT} > \frac{1}{8 \times f_{SW}} \times \frac{I_{RIPPLE}}{V_{OUT(ripple)}} \tag{23}$$

where

- f_{SW} is the switching frequency
- V_{RIPPLE} is the maximum allowable output voltage ripple

- I_{RIPPLE} is the inductor ripple current.

In this case, the maximum output voltage ripple is 10 mV. Under this requirement, the minimum output capacitance for ripple (as calculated in 式 24) yields 80.5 µF. 式 24 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. 式 24 indicates the ESR should be less than 3 mΩ, and this is the requirement when the impedance of the output capacitance is dominated by ESR, such as with an electrolytic capacitor. However, because the output voltage ripple is a combination of capacitive ripple and resistive ripple, the ESR must be much lower than this result when the capacitance is purely ceramic. This is because the lower capacitance values obtained with ceramic capacitors will result in a larger capacitive ripple component of the total ripple.

$$R_{ESR} = \frac{V_{OUT(ripple)}}{I_{RIPPLE}} \tag{24}$$

Additional capacitance de-ratings for aging, temperature, and DC bias should be factored in, which increases the minimum required capacitance value. For this design example, three 100-µF, 6.3-V, X5R, ceramic capacitors with 2 mΩ each of ESR were selected. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the RMS (root mean square) value of the maximum ripple current. 式 25 can be used to calculate the RMS ripple current the output capacitor needs to support. For this application, 式 25 yields 929 mA.

$$I_{C(rms)} = \frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{\sqrt{12} \times V_{IN(max)} \times L1 \times f_{SW}} \tag{25}$$

9.2.2.4.3 Bus Capacitance

The amount of bus capacitance is the third criteria. This requirement is optional. However, extra output bus capacitance should be considered in systems where the electrical environment is unpredictable, or not fully defined, or can be subject to severe events such as hot plug events or even electrostatic discharge (ESD) events.

During a hot plug event, when a discharged load capacitor is plugged into the output of the regulator, the instantaneous current demand required to charge this load capacitance will be far too rapid to be supplied by the control loop. Often the peak charging current can be multiple times higher than the current limit of the regulator. Additional output capacitance will help maintain the bus voltage within acceptable limits. For hot plug events, the amount of required bus capacitance can be calculated if the load capacitance is known, based on the concept of conservation of charge.

An ESD event, or even non-direct lightning surges at the primary circuit level can cause glitches at this converter system level. A glitch of sufficient amplitude to falsely trip OVP or UVLO can cause several clock cycles of disturbance. In such cases, it is beneficial to design in more bus capacitance than is required by the simpler load transient and ripple requirements. The amount of extra bus capacitance can be calculated based on maintaining the output voltage within acceptable limits during the disturbance. This capacitance can be as much as required to fully support the load for the duration of the interrupted converter operation.

9.2.2.5 Input Capacitor Selection

The TPS54020 requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 4.7 µF of effective capacitance on the PVIN input voltage pins and another 4.7 µF on the VIN input voltage pin. In some applications, additional bulk capacitance can also be required for the PV_{IN} input. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple to the device during full load. The input ripple current can be calculated using 式 26.

$$I_{CIN(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{\left(V_{IN(min)} - V_{OUT}\right)}{V_{IN(min)}}} \quad (26)$$

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance-to-volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases. For this example design, a ceramic capacitor with at least a 25-V voltage rating is required to support the maximum input voltage. For this example, two 22-µF, 25-V ceramic capacitors and one 68-µF, 25-V electrolytic capacitor in parallel have been selected for the PV_{IN} voltage rail. For the V_{IN} voltage rail, one 4.7-µF, 25-V ceramic capacitor was selected. The V_{IN} and PV_{IN} inputs are normally tied together so the TPS54020 can operate from a single supply. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using 式 27. Using the design example values, $I_{OUT(max)}$ = 10 A, C_{IN} = 48.7 µF, f_{SW} = 500 kHz, yields an input voltage ripple of 103 mV and a RMS input ripple current of 4.18 Arms. Because an electrolytic capacitor typically features a much higher ESR, it was not included in this calculation. The input capacitor ripple voltage is calculated in 式 27.

$$\Delta V_{IN} = \frac{I_{OUT(max)} \times 0.25}{C_{IN} \times f_{SW}} \quad (27)$$

9.2.2.6 Soft-Start Capacitor Selection

The soft-start capacitor determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is very large and would require large amounts of current to quickly charge the capacitor to the output voltage level. The extra current required to charge the output capacitors can cause the TPS54020 to reach the current limit. The soft-start current surge from the input can cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems. The soft-start capacitor value can be calculated using 式 28. For the example circuit, the soft-start time is not critical because the output capacitor value is only 300 µF which does not require much current to charge to 1.8 V. The example circuit has the soft-start time set to an arbitrary value of 30 ms, which requires a 100-nF capacitor. In this case, I_{SS} is 2.3 µA and V_{REF} is 0.6 V.

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{REF}} \quad (28)$$

where

- C_{SS} is the soft-start capacitance in nF
- I_{SS} is the soft-start current in µA
- t_{SS} is the soft-start time in ms
- V_{REF} of the voltage reference in V

9.2.2.7 Bootstrap Capacitor Selection

A ceramic capacitor with a value of 0.1 µF must be connected between the BOOT and PH pins for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have voltage rating of 10 V or higher.

9.2.2.8 Undervoltage Lockout Set Point

It is recommended that an external divider be connected to the EN pin for clean transitions from OFF to ON and ON to OFF. The undervoltage lockout (UVLO) can be designed using the external voltage divider network of R6 and R11. R6 is connected between the VIN and EN pin of the TPS54020 and R11 is connected between EN and

GND. The UVLO has two thresholds: one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 7.5 V (UVLO start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below 7.1 V (UVLO stop or disable). 式 2 and 式 3 can be used to calculate the values for the upper and lower resistor values. For the UVLO voltages specified, the nearest standard resistor value for R6 is 69.8 kΩ and for R11 is 13.3 kΩ.

9.2.2.9 Output Voltage Feedback Resistor Selection

The resistor divider network R7 and R10 is used to set the output voltage. For the example design, R10 was set to 2.55 kΩ. This yields a value of 5.11 kΩ for R7. These relatively low values are used so as to provide some minimum DC load current that is higher than the PH pin bias leakage current.

9.2.2.9.1 Minimum Output Voltage

Due to internal design limitations of the TPS54020, there is a minimum output voltage limit for any given input voltage. The output voltage can never be lower than the internal voltage reference of 0.6 V. However, the output voltage can also be limited to values greater than 0.6 V by the minimum controllable on time. The minimum output voltage in this case is given by 式 29

$$V_{OUT(min)} = t_{ON(min)} \times f_{SW(max)} \times \left(V_{IN(max)} + I_{OUT(min)} \times \left(R_{DS2(min)} - R_{DS1(min)}\right)\right) - I_{OUT(min)} \left(R_{LOAD} - R_{DS2(min)}\right) \quad (29)$$

where

- $V_{OUT(min)}$ is the minimum achievable output voltage
- $t_{ON(min)}$ is the minimum controllable on-time (135 nsec max)
- $f_{SW(max)}$ is the maximum switching frequency including tolerance
- $V_{IN(max)}$ is the maximum input voltage
- $I_{OUT(min)}$ is the minimum load current
- $R_{DS1(min)}$ is the minimum high-side MOSFET on resistance (36 mΩ to 32 mΩ typical)
- $R_{DS2(min)}$ is the minimum low-side MOSFET on resistance (19 mΩ typical)
- R_{LOAD} is the series resistance of output inductor

9.2.2.10 Compensation Component Selection

There are several industry techniques used to compensate DC/DC regulators. The method presented here is easy to calculate and yields high phase margins. For most conditions, the regulator has a phase margin between 60 and 90 degrees. The method presented here ignores the effects of the slope compensation that is internal to the TPS54020. Because the slope compensation is ignored, the actual cross over frequency is usually lower than the cross over frequency used in the calculations. Use the PSPICE model for a more accurate design.

First, the modulator pole, $f_{P(mod)}$, and the esr zero, $f_{Z(mod)}$, must be calculated using 式 30 and 式 31.

For the output capacitance, use a derated value of 225 µF. As a quick estimate, an f_C value between three and five times the double pole frequency of the output filter is chosen. In this case, an f_C of 35 kHz was selected. $f_{P(mod)}$ is 3.93 kHz and $f_{Z(mod)}$ is 10.6 MHz.

$$f_{P(mod)} = \frac{I_{OUT}}{2 \times \pi \times V_{OUT} \times C_{OUT}} \quad (30)$$

$$f_{Z(mod)} = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}} \quad (31)$$

Now the compensation components can be calculated. First, calculate the value for C12 which sets the gain of the compensated network at low frequencies far below f_C. Because the desired f_C is 35 kHz, and the expected gain curve is a single pole roll off, two decades below f_C (which is 350 Hz), the gain should be +40 dB. Following this logic, the plant gain at DC is calculated in 式 32.

$$A_{Vdc} = 20 \times \log\left(g_{M(ea)} \times 2.38\,M \times g_{M(ps)} \times \left(\frac{V_{OUT}}{I_{OUT}} \right) \right) = 80.94\,dB \tag{32}$$

This implies that at 350 Hz, the compensation pole capacitor C12 should reduce the gain by (80.94-40) = 40.94 dB, or result in a gain of -40.94 dB. (See 式 33)

$$20 \times \log\left(\frac{Z_C}{2.38\,M} \right) = -40.94\,dB \tag{33}$$

$$Z_C = 2.38Meg \times 10^{\left(\frac{-40.94}{20} \right)} = 21.367k\Omega(at\,350Hz) \tag{34}$$

$$C = \frac{1}{2\pi \times f_{SW} \times Z_C} = \frac{1}{2\pi \times 350 \times 21.367} = 21.28\,nF \tag{35}$$

where

- f_{SW} is in kHz

The closest standard value is 22 nF.

From 式 30, the required compensation zero resulting from R13 should be placed at $f_{P(mod)}$ of 3.93 kHz.

$$f_{Z(comp)} = \frac{1}{2\pi \times R13 \times C12} \tag{36}$$

$$R13 = \frac{1}{2\pi \times f_{Z(comp)} \times C12} = \frac{1}{2\pi \times 3.93 \times 22} = 1.84 \tag{37}$$

where

- $f_{Z(comp)}$ is in kHz
- C12 is in nF
- R13 is in kΩ

This value was adjusted after actual Bode measurements to 3.01 kΩ.

An additional high frequency pole can be used if necessary by adding a capacitor in parallel with the series combination of R13 and C12. The pole frequency can be placed at the ESR zero frequency of the output capacitor as given by 式 13. Use 式 38 to calculate the required capacitor value for C10.

$$C10 = \frac{R_{ESR} \times C_{OUT}}{R13} = \frac{666\ \mu\Omega \times 225\ \mu F}{3.01\,k\Omega} = 49\ pF \tag{38}$$

This value was adjusted upwards to 22 0pF to reduce jitter.

9.2.3 Application Curves

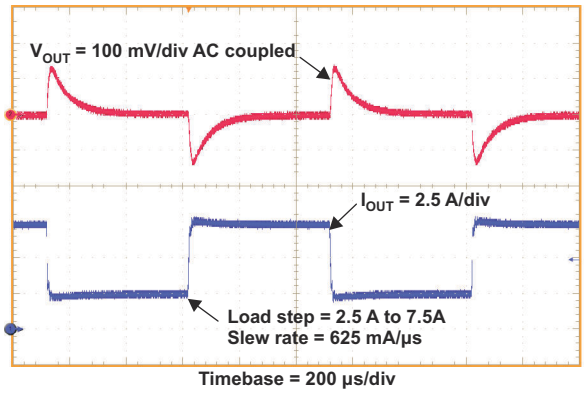


図 9-6. Load Transient

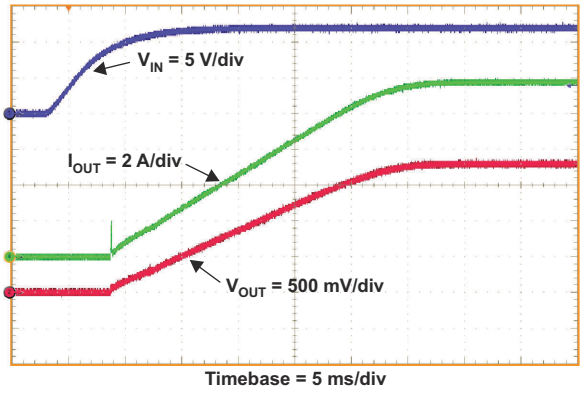


図 9-7. Start-Up With VIN

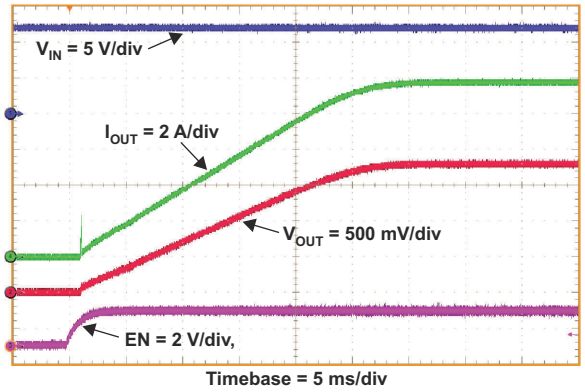


図 9-8. Start-Up With EN

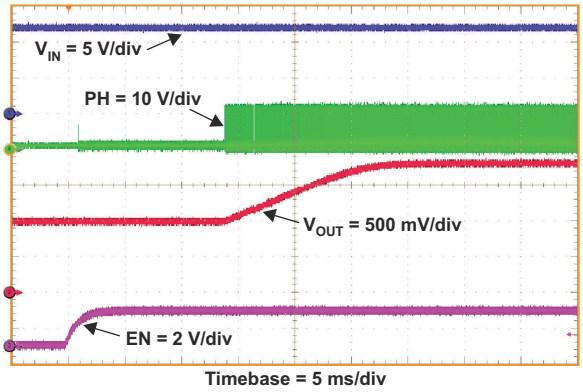


図 9-9. Start-Up With Prebias

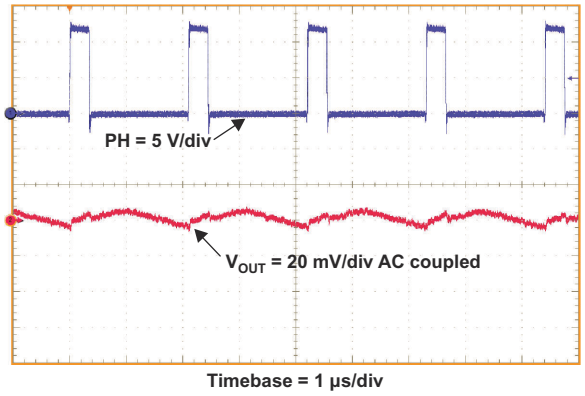


図 9-10. Output Voltage Ripple With Full Load

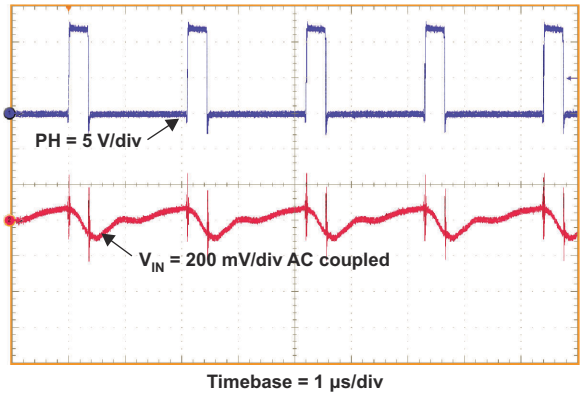


図 9-11. Input Voltage Ripple With Full Load

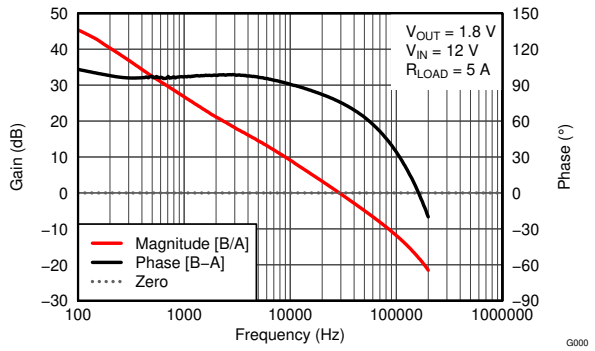


図 9-12. Closed-Loop Bode Response

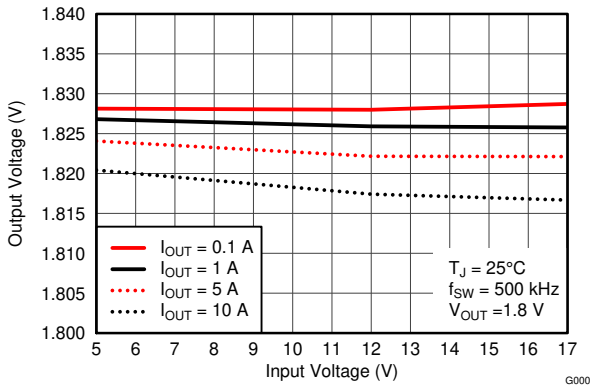


図 9-13. Line Regulation

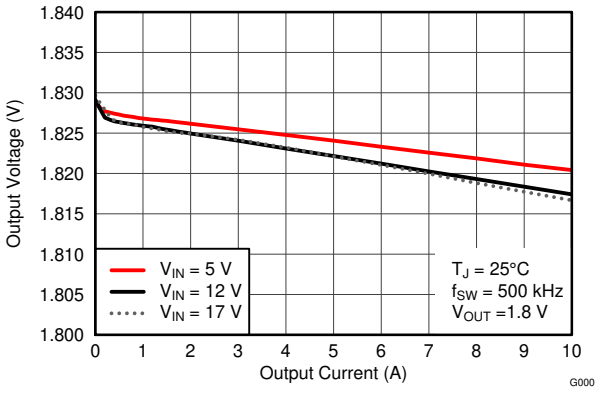


図 9-14. Load Regulation

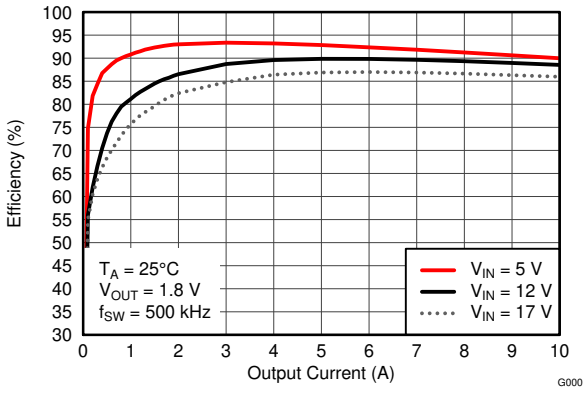


図 9-15. Efficiency

10 Power Supply Recommendations

The TPS54020 operates from a controller bias voltage supply between 4.5 V and 17 V, and a power stage input voltage between 1.6 V and 17 V. The TPS54020 is designed to support either split-rail or single-supply operation, and may be operated from separate PVIN and VIN voltages. Proper bypassing of input supplies and internal regulators is also critical for noise performance, as is PCB layout and grounding scheme. See the recommendations in *セクション 11* and *セクション 6*.

11 Layout

11.1 Layout Guidelines

Layout is a critical portion of good power supply design. See 図 11-1 for a PCB layout example. The top layer contains the main power traces for PVIN, VIN, VOUT, and VPHASE. Also on the top layer are connections for several analog pins of the TPS54020 and a large area filled with PGND. The two internal layers are the same and contain mostly power planes, including PGND, VOUT, PVIN, and VPHASE. The bottom layer contains the remainder of the analog circuit connections, plus power planes similar to the internal layers. The top-side power and ground planes are connected to the bottom and internal power and ground planes with multiple vias placed around the board including several vias directly under the TPS54020 device to provide a thermal path from the top-side power planes to the other layer power planes. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supply performance.

To help eliminate these noise problems, the PVIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the PVIN pins, and the ground connections. The VIN pin must also be bypassed to ground using a low ESR ceramic capacitor with X5R or X7R dielectric. Make sure to connect this capacitor to the quiet analog ground trace rather than the power ground trace of the PVIn bypass capacitor. Because the PH connection is the switching node, the output inductor should be located close to the PH pin, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The output filter capacitor ground should use the same power ground trace as the PVIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width. The small signal components should be grounded to the analog ground path as shown. The RT/CLK pin is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal trace lengths. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layouts, however this layout has been shown to produce good results and is meant as a guideline.

Land pattern and stencil information is provided in the data sheet addendum. The dimension and outline information is for the standard RUW package.

11.2 Layout Examples

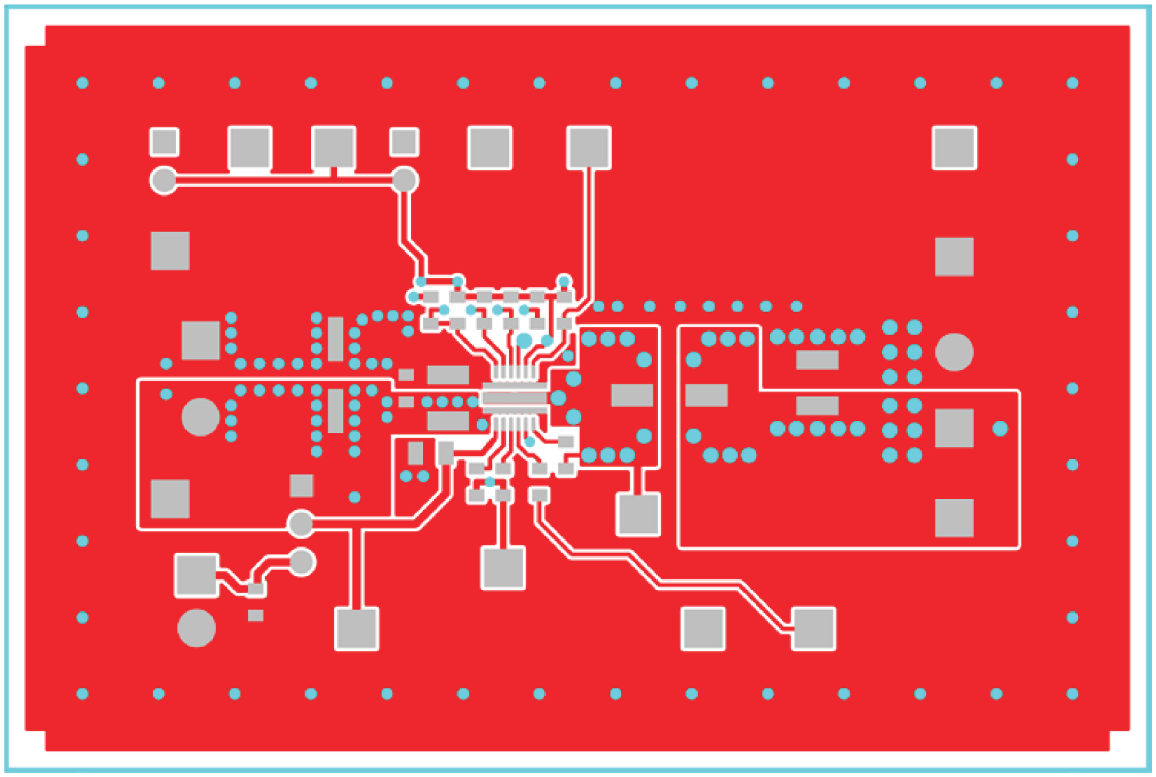


図 11-1. TPS54020EVM-082 Top Side Copper

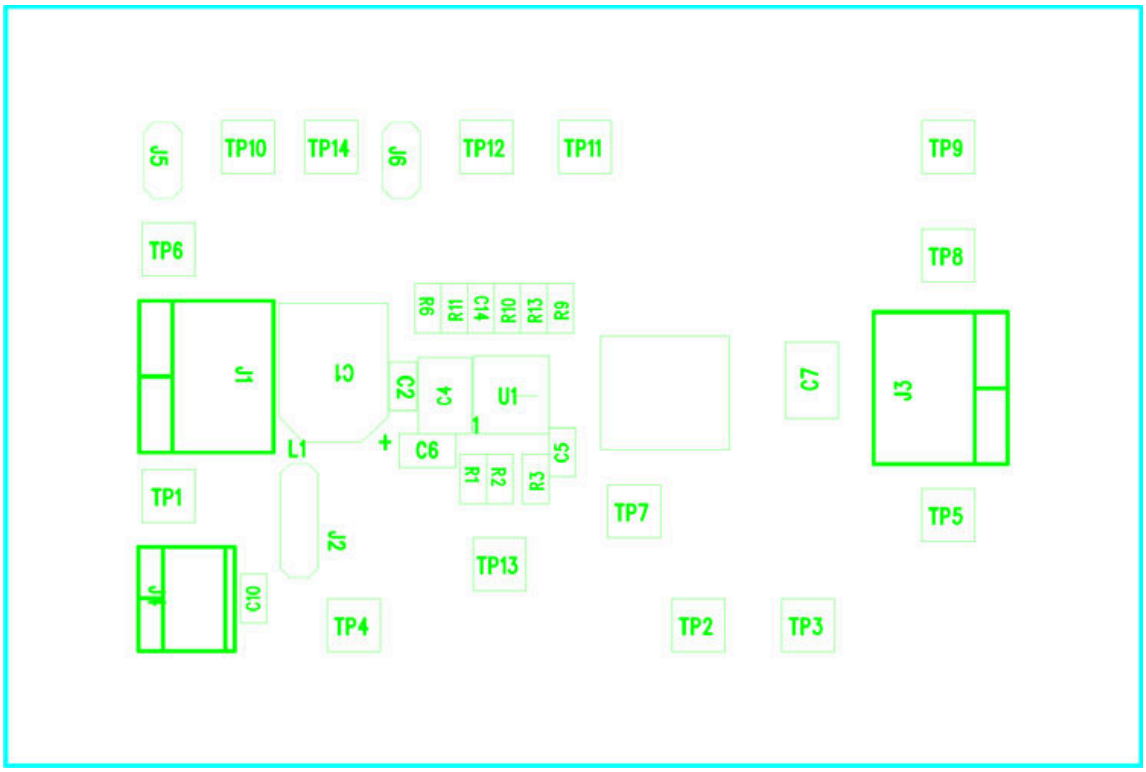


図 11-2. TPS54020EVM-082 Top Side Component Placement

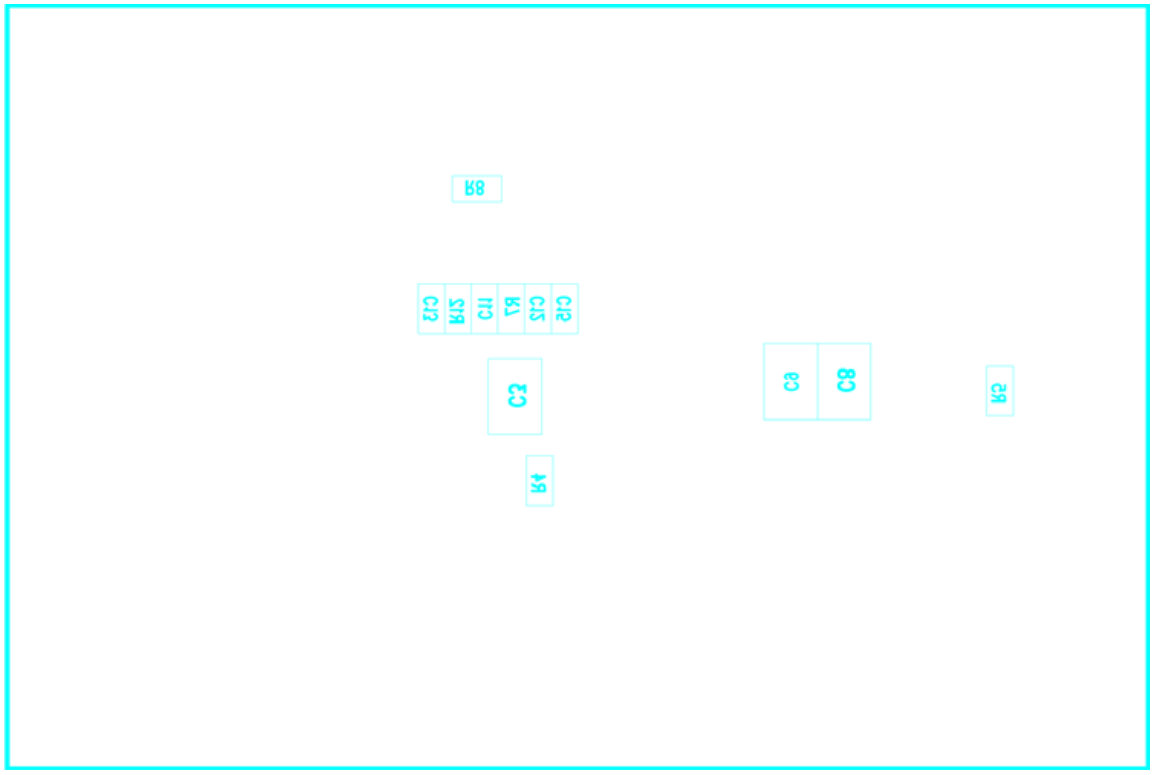


図 11-3. TPS54020EVM-082 Bottom Side Component Placement

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS54020 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

12.2 Documentation Support

12.2.1 Related Documentation

Designing Type III Compensation for Current Mode Step-Down Converters (SLVA352)

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54020RUWR	ACTIVE	VQFN-HR	RUW	15	3000	RoHS-Exempt & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 150	54020	Samples
TPS54020RUWT	ACTIVE	VQFN-HR	RUW	15	250	RoHS-Exempt & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 150	54020	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

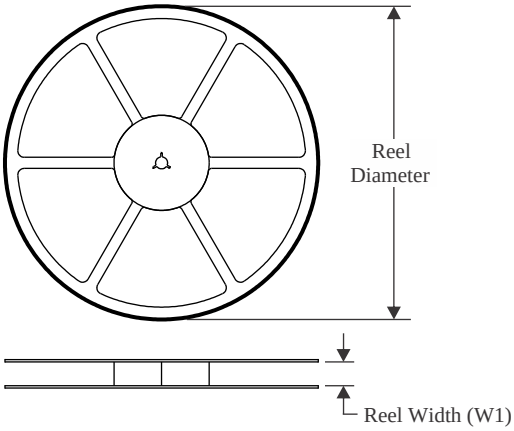
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

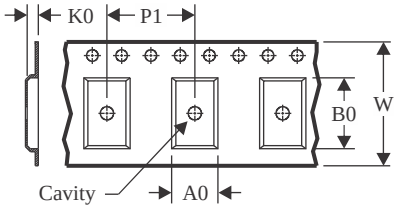
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

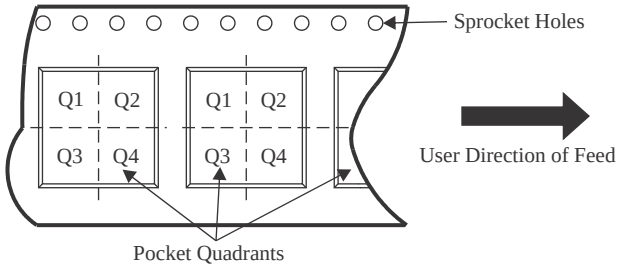


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

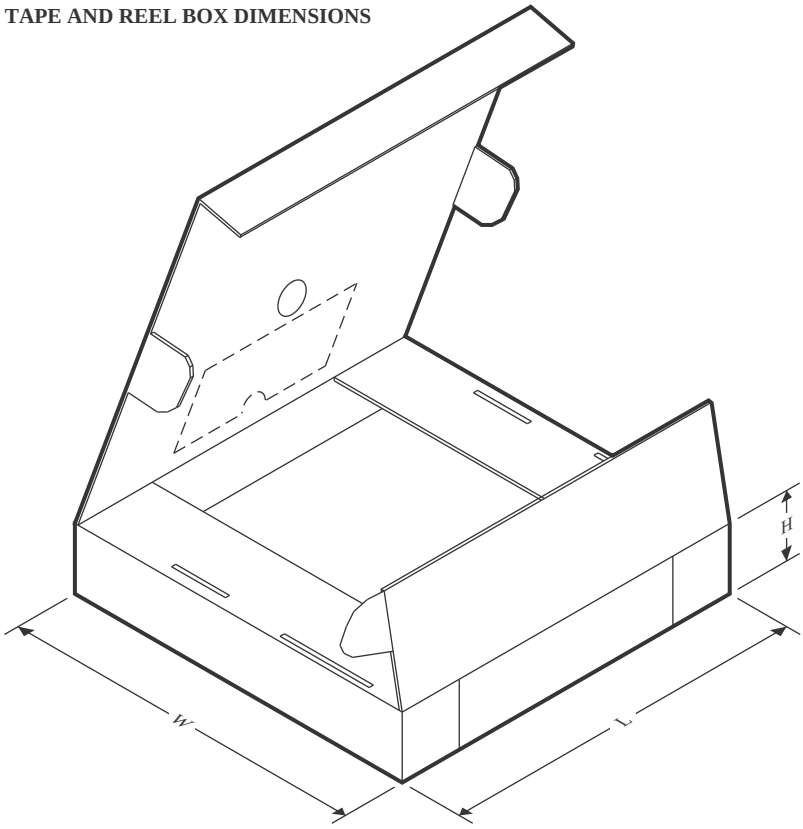
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54020RUWR	VQFN-HR	RUW	15	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TPS54020RUWT	VQFN-HR	RUW	15	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

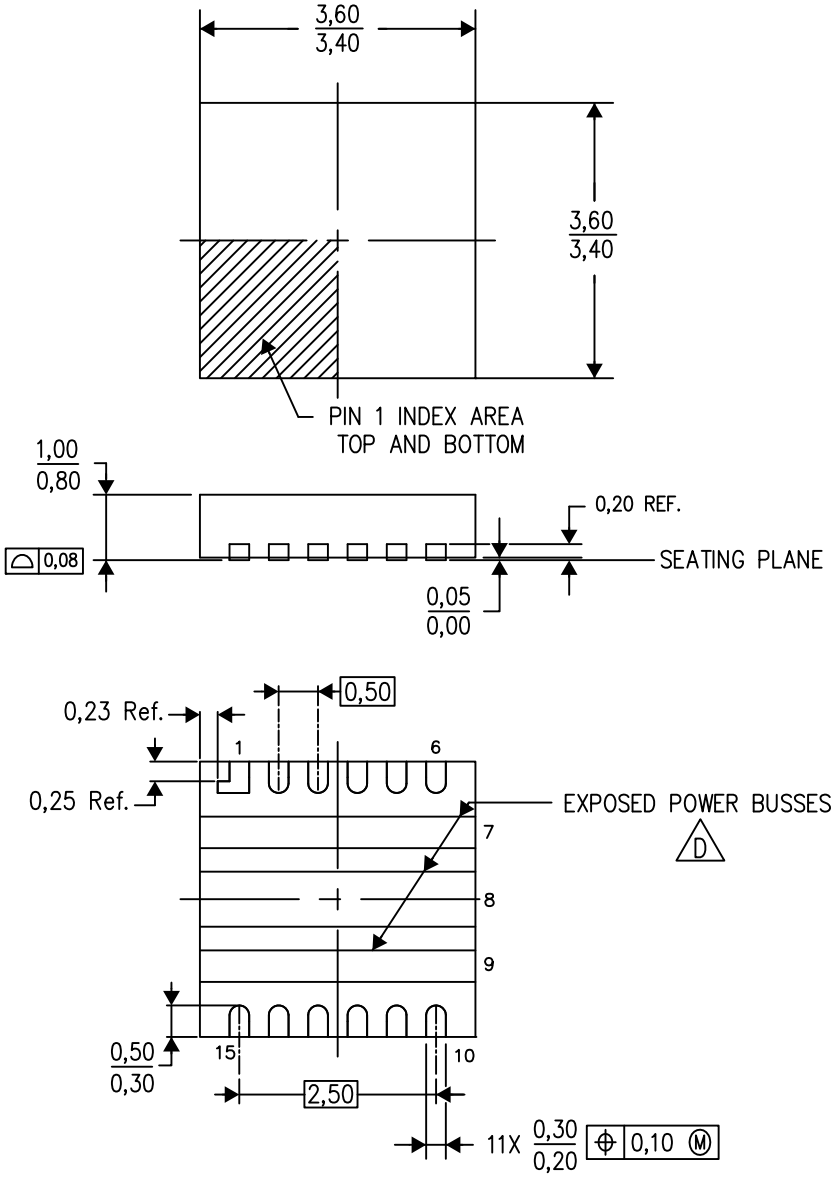
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54020RUWR	VQFN-HR	RUW	15	3000	356.0	356.0	35.0
TPS54020RUWT	VQFN-HR	RUW	15	250	210.0	185.0	35.0

RUW (S–PVQFN–N15) PLASTIC QUAD FLATPACK NO–LEAD



Bottom View

4209401–2/E 07/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. See the Product Data Sheet for details regarding the exposed power buss dimensions.
E. RoHS exempt flip chip application. Internal solder joints may contain Pb.
F. Exposed terminals are Pb–free

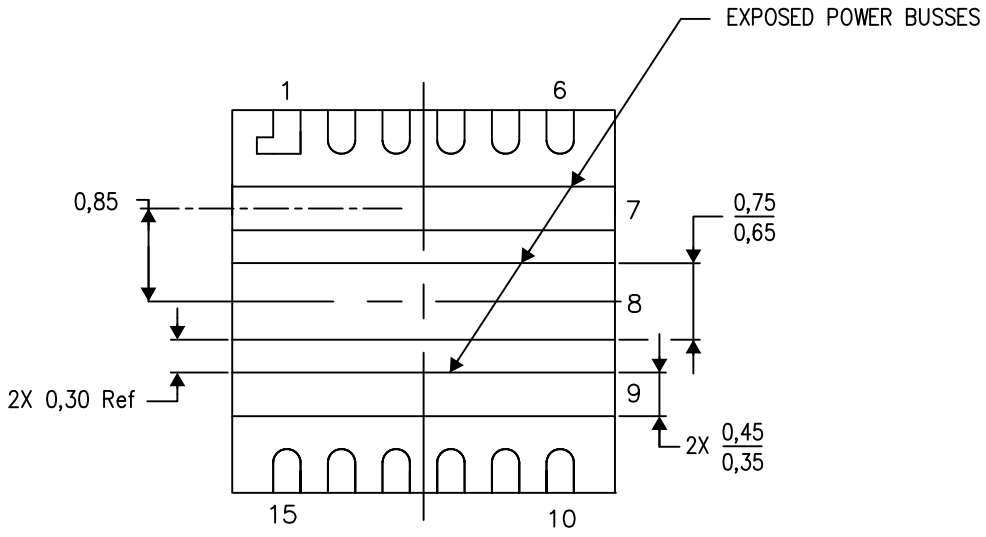
RUW (S–PVQFN–N15) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



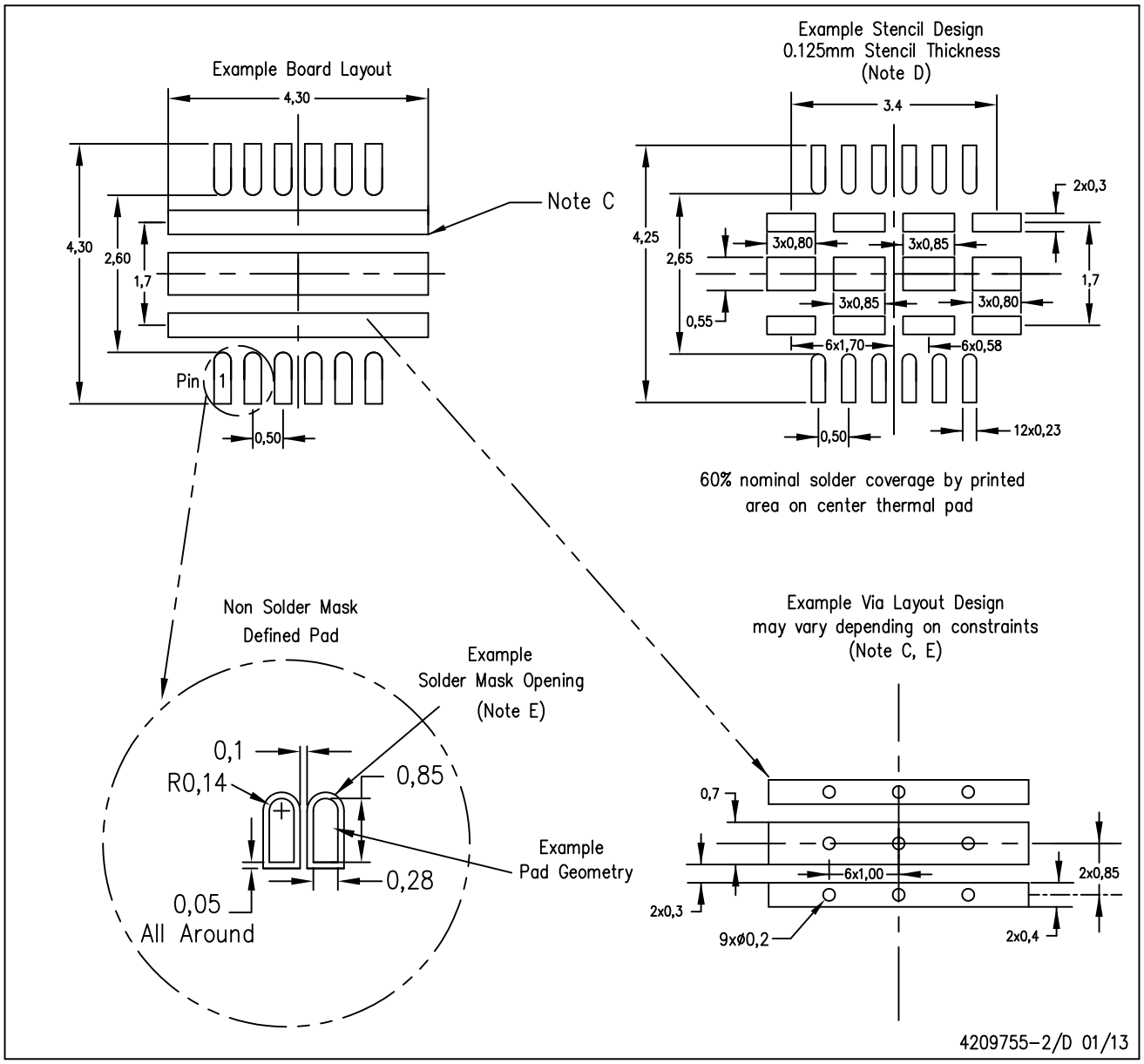
Bottom View

Exposed Thermal Pad Dimensions

4209411–2/E 09/12

NOTE: All linear dimensions are in millimeters

RUW (R–PVQFN–N15) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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