TEXAS INSTRUMENTS
TPS54308
JAJSD91A – JUNE 2017 – REVISED APRIL 2021

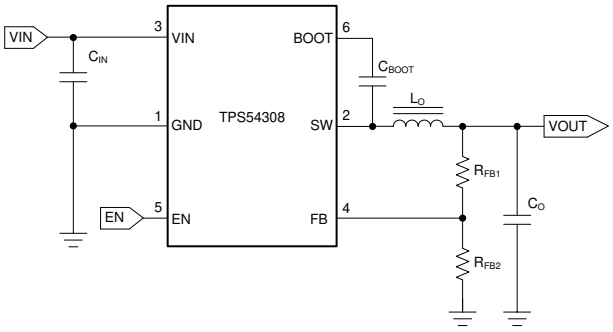
TPS54308 4.5V～28V 入力、3A 出力、同期整流 350kHz FCCM 降圧コンバータ、SOT23 パッケージ

1 特長

- 4.5V～28V の広い入力電圧範囲
- 85mΩ と 40mΩ の MOSFET を内蔵し、3A の連続出力電流に対応
- 低いシャットダウン時電流 (2μA) と静止電流 (300μA)
- 5ms のソフト・スタート内蔵
- 350kHz の固定スイッチング周波数
- ピーク電流モード制御
- ループ補償内蔵
- ヒカップ・モード保護機能付き、2 個の MOSFET の過電流保護
- 過電圧保護
- サーマル・シャットダウン
- SOT-23 (6) パッケージ
- WEBENCH® Power Designer により、TPS54308 を使用するカスタム設計を作成

2 アプリケーション

- 12V、24V の分散パワー・バス電源
- 産業用アプリケーション
  - 白物家電
- 消費者向けアプリケーション
  - オーディオ
  - STB、DTV
  - プリンタ



概略回路図

3 概要

TPS54308 は入力電圧範囲が 4.5V～28V で、3A の同期整流降圧コンバータです。このデバイスには 2 つの内蔵スイッチング FET、内部的なループ補償、および 5ms の内部ソフトスタートが搭載されているため、部品数を減らすことができます。

また MOSFET を内蔵し、SOT-23 パッケージを採用しているので、高い電力密度を実現し、PCB 上の占有面積を節減できます。

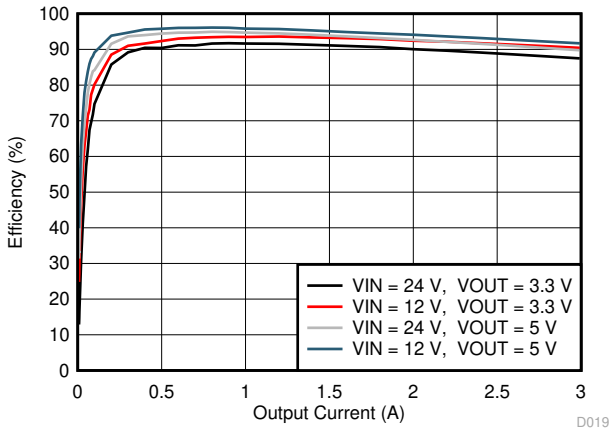
軽負荷状態では、TPS54308 は強制連続導通モード (FCCM) で動作します。スイッチング周波数は、負荷範囲全体にわたってほぼ一定のレベルに維持されます。

両方のハイサイド MOSFET でサイクル単位の電流制限を行い、過負荷の状況でコンバータを保護します。また、ローサイド MOSFET の電流制限を自由に設定でき、電流暴走を防止することで、さらに保護が強化されています。プリセット時間を上回る長さで過電流状態が続いた場合、ヒカップ・モード保護機能をトリガします。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TPS54308	SOT-23 (6)	1.60mm × 2.90mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



効率と出力電流との関係

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (June 2017) to Revision A (April 2021)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• 文書全体にわたって文法と採番を訂正	1

5 Pin Configuration and Functions

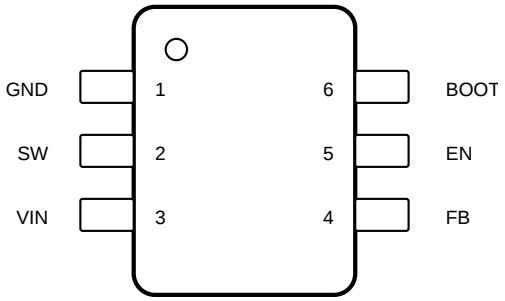


図 5-1. 6-Pin SOT-23 DDC Package (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
BOOT	6	O	Supply input for the high-side NFET gate drive circuit. Connect a 0.1-µF capacitor between BOOT and SW pins.
EN	5	I	This pin is the enable pin. Float the EN pin to enable.
FB	4	I	Converter feedback input. Connect to output voltage with feedback resistor divider.
GND	1	–	Ground pin source terminal of the low-side power NFET and the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	O	Switch node connection between high-side NFET and low-side NFET
VIN	3	–	Input voltage supply pin. The drain terminal of high-side power NFET

(1) O = Output; I = Input

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage range, V_I	VIN	–0.3	30	V
	EN	–0.3	7	V
	FB	–0.3	7	V
Output voltage range, V_O	BOOT-SW	–0.3	7	V
	SW	–0.3	30	V
	SW (20 ns transient)	–5	30	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_I	Input voltage range	VIN	4.5	28	V
		EN	–0.1	7	V
		FB	–0.1	7	V
V_O	Output voltage range	BOOT-SW	–0.1	7	V
		SW	–0.1	28	V
T_J	Operating junction temperature		–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS54308 DDC (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. T_J = –40°C to +125°C, V_{IN} = 4.5 V to 28 V, (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{IN}	Input voltage range		4.5		28	V
I_Q	Non switching quiescent current	EN =5 V, VFB = 1 V		300		µA
I_{OFF}	Shut down current	EN = GND		2		µA
$V_{IN(UVLO)}$	VIN under voltage lockout	Rising V_{IN}	3.8	4.1	4.45	V
		Falling V_{IN}	3.3	3.6	3.9	V
	Hysteresis		400	480	600	mV
ENABLE (EN PIN)						
$V_{(EN\_RISING)}$	Enable threshold	Rising		1.21	1.28	V
$V_{(EN\_FALLING)}$		Falling	1.1	1.19		V
$I_{(EN\_INPUT)}$	Input current	V_{EN} = 1 V		0.7		µA
$I_{(EN\_HYS)}$	Hysteresis current	V_{EN} = 1.5 V		1.55		µA
FEEDBACK AND ERROR AMPLIFIER						
V_{FB}	Feedback Voltage	V_{IN} = 12 V	0.581	0.596	0.611	V
POWER STAGE						
$R_{(HSD)}$	High-side FET on resistance	T_A = 25°C, V_{BST} – SW = 6 V		85		mΩ
$R_{(LSD)}$	Low-side FET on resistance	T_A = 25°C, V_{IN} = 12		40		mΩ
CURRENT LIMIT						
$I_{(LIM\_HS)}$	High side current limit	Maximum inductor peak current	4	5	5.9	A
$I_{(LIM\_LS)}$	Low side source current limit	Maximum inductor valley current	3.1	4	5.5	A
$I_{(LIM\_LSSOC)}$	Low side sink current limit		1.75	2.8	3.85	A
OSCILLATOR						
F_{sw}	Centre switching frequency		255	350	445	kHz
OVER TEMPERATURE PROTECTION						
Thermal Shutdown(1)	Rising temperature			165		°C
	Hysteresis			10		°C
	Hiccup time			32768		Cycles

(1) Not production tested

6.6 Timing Requirements

		MIN	TYP	MAX	UNIT
OVER CURRENT PROTECTION					
t_{HIC_WAIT}	Hiccup wait time		512		Cycles
$t_{HIC\_RESTART}$	Hiccup time before restart		16384		Cycles
t_{SS}	Soft-start time		5		ms
ON TIME CONTROL					
t_{MIN_ON} (1)	Minimum on time, measured at 90% to 90% and 1-A loading		110		ns

Typical Characteristics

V_{IN} = 12, unless otherwise specified

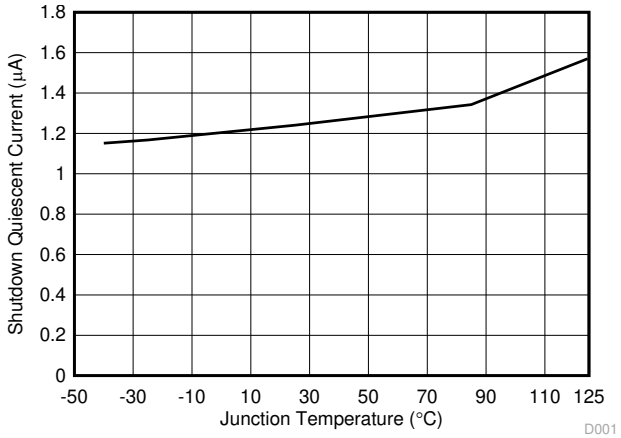


図 6-1. Shutdown Quiescent Current vs Junction Temperature

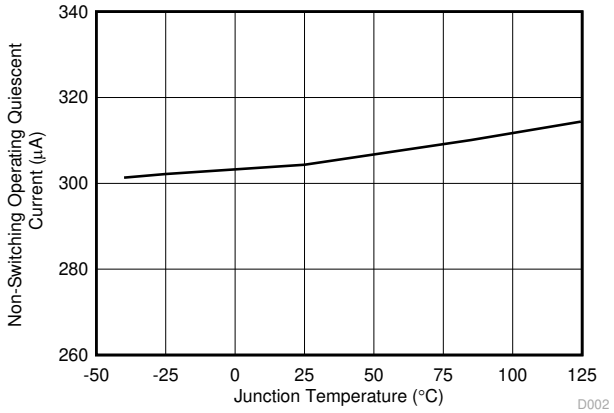


図 6-2. Non-Switching Operating Quiescent Current vs Junction Temperature

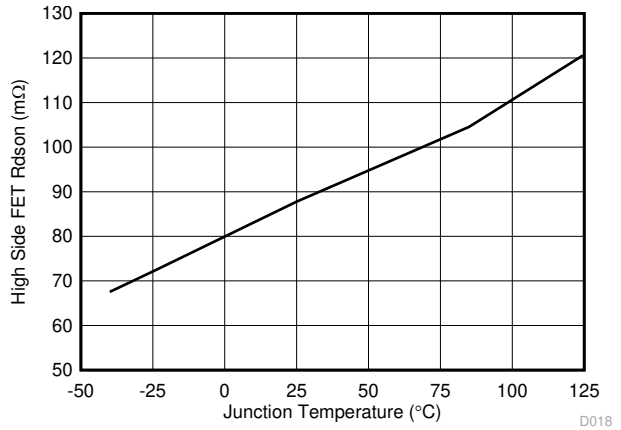


図 6-3. High-Side Resistance vs Junction Temperature

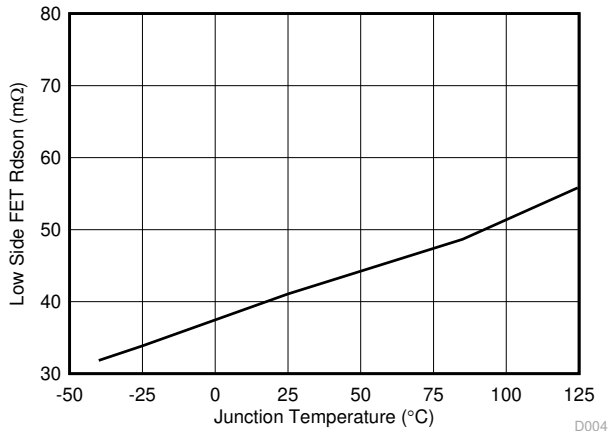


図 6-4. Low-Side FET On Resistance vs Junction Temperature

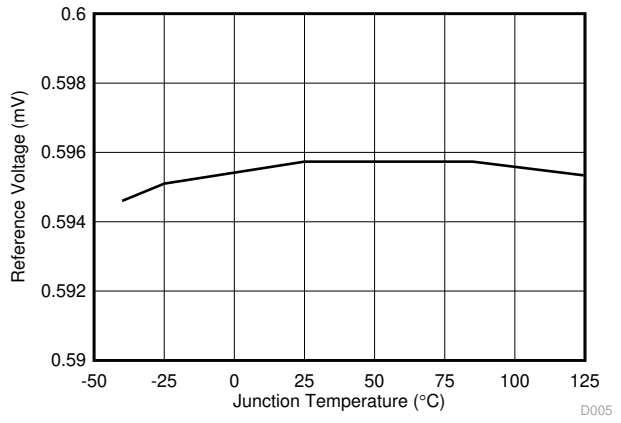


図 6-5. Reference Voltage vs Junction Temperature

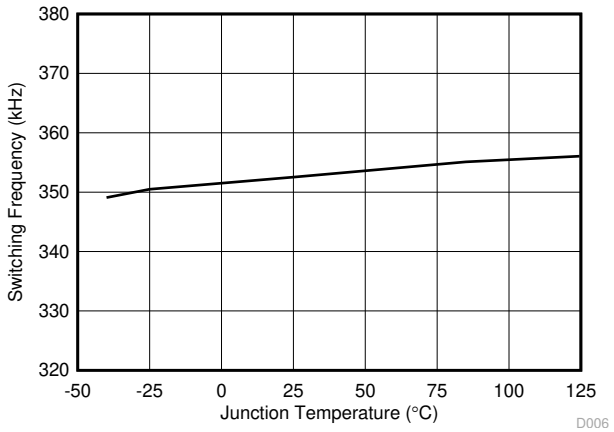


図 6-6. Centre Switching Frequency vs Junction Temperature

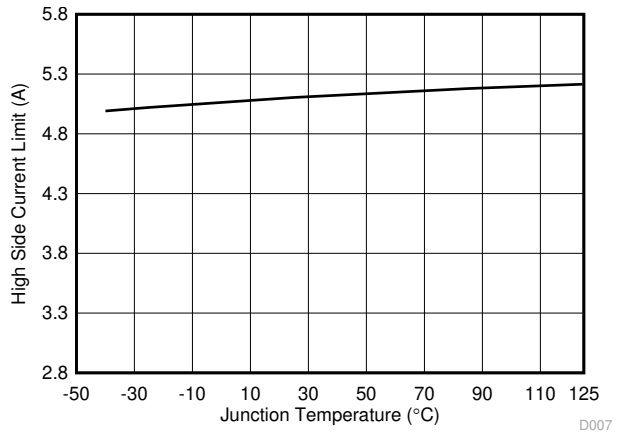


図 6-7. High-Side Current Limit Threshold vs Junction Temperature

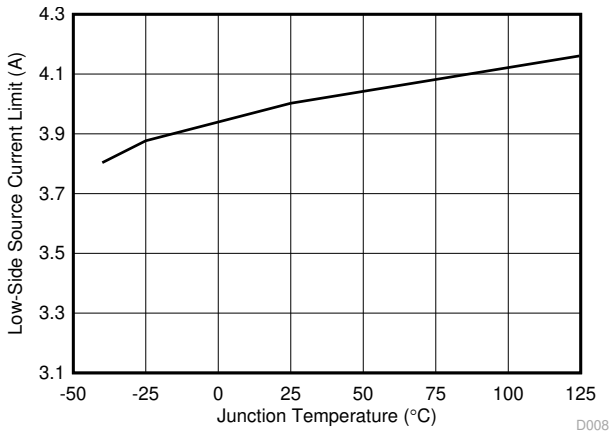


図 6-8. Low-Side Source Current Limit Threshold vs Junction Temperature

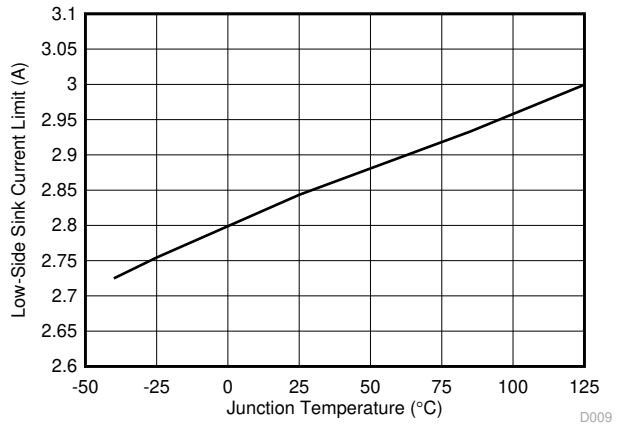


図 6-9. Low-Side Sink Current Limit Threshold vs Junction Temperature

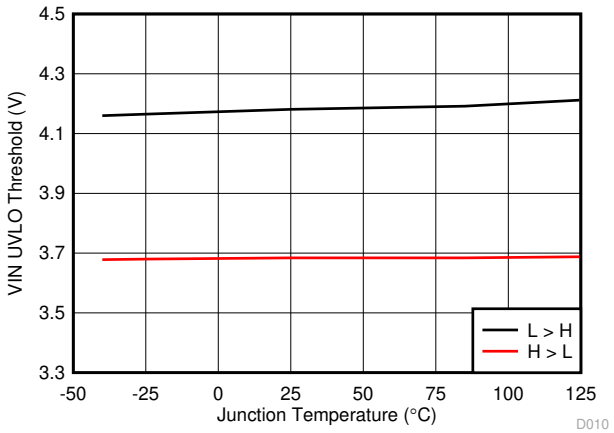


図 6-10. VIN UVLO Threshold vs Junction Temperature

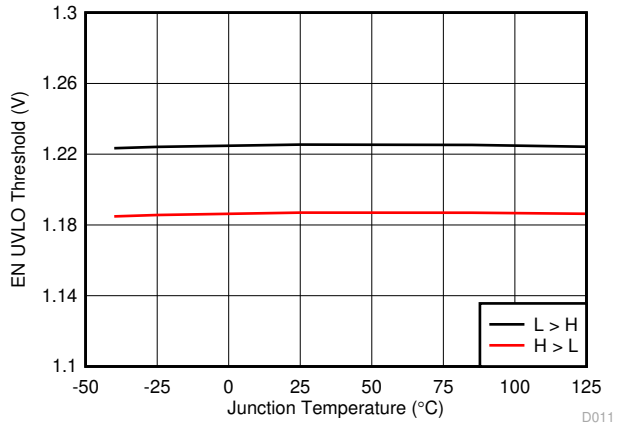


図 6-11. EN Threshold vs Junction Temperature

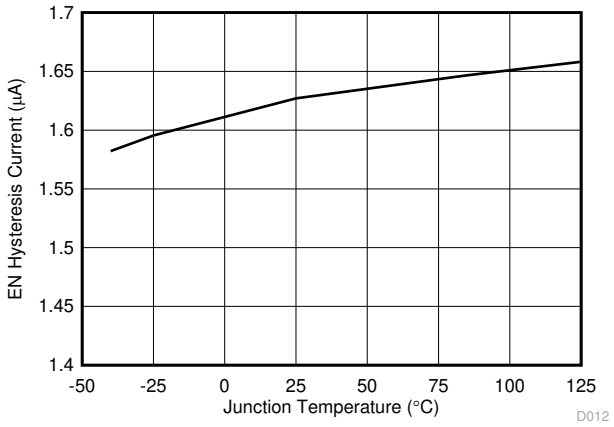


図 6-12. EN Hysteresis Current vs Junction Temperature

7 Detailed Description

7.1 Overview

The device is a 28-V, 3-A, synchronous step-down (buck) converter with two integrated n-channel MOSFETs. To improve performance during line and load transients, the device implements a constant-frequency, peak current mode control which reduces output capacitance. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

The switching frequency of the TPS54308 is fixed to 350 kHz. This device operates in continuous conduction mode (FCCM) during light load conditions. During FCCM, the switching frequency is maintained at an almost constant level over the entire load range, which is suitable for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load.

The TPS54308 starts switching when V_{IN} is equal to 4.5 V. The operating current is 300 µA (typical) when the device is not switching and under no load. When the device is disabled, the supply current is 2 µA (typical).

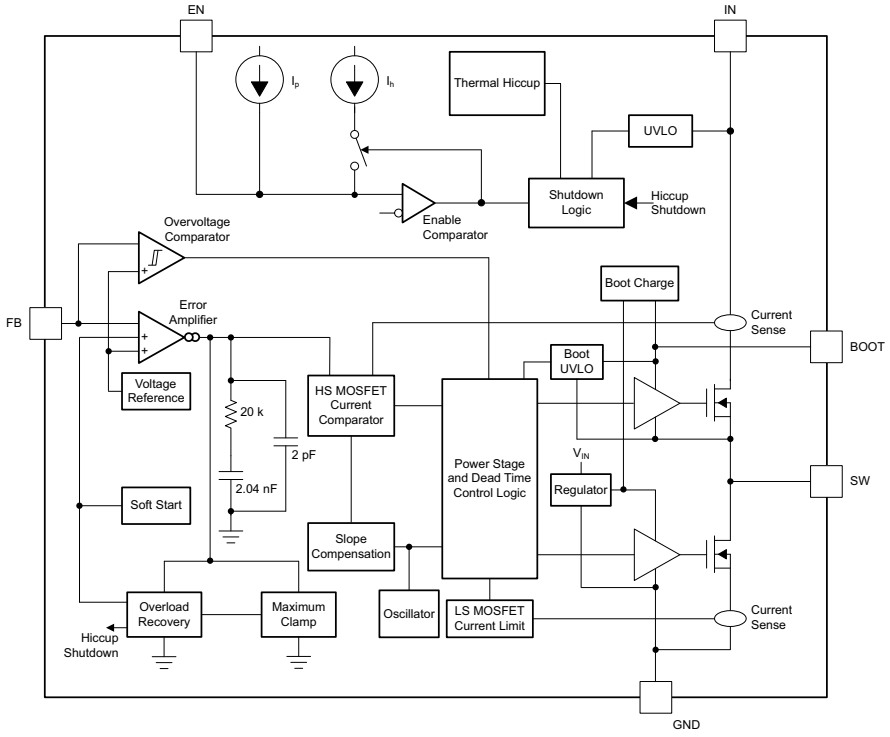
The integrated 85-mΩ high-side MOSFET and 40-mΩ low-side MOSFET allow for high-efficiency power supply designs with continuous output currents up to 3 A.

The TPS54308 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by an external capacitor on the BOOT to PH pins. The boot capacitor voltage is monitored by an UVLO circuit and turns the high-side MOSFET off when the voltage falls below a preset threshold of 2.1 V (typical).

The device minimizes excessive output overvoltage transients by taking advantage of the overvoltage comparator. When the regulated output voltage is greater than 118% of the nominal voltage, the overvoltage comparator is activated, and the high-side MOSFET is turned off and masked from turning on until the output voltage is lower than 104%.

The TPS54308 device has internal 5-ms soft-start time to minimize inrush currents.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fixed-Frequency PWM Control

The device uses a fixed-frequency, peak current-mode control. The output voltage is compared through external resistors on the FB pin to an internal voltage reference by an error amplifier. An internal oscillator initiates the turn-on of the high-side power switch. The error amplifier output is compared to the current of the high-side power switch. When the power-switch current reaches the error amplifier output voltage level, the high-side power switch is turned off and the low-side power switch is turned on. The error amplifier output voltage increases and decreases as the output current increases and decreases. The device implements a current limit by clamping the error amplifier voltage to a maximum level. The device also implements a minimum clamp for improved transient-response performance.

7.3.2 Force Continuous Conduction Mode (FCCM)

The TPS54308 is designed to operate in forced continuous conduction mode (FCCM) during light load conditions. During FCCM, the switching frequency is maintained at an almost constant level over the entire load range which is suitable for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load. For some audio applications, this mode can help avoid switching frequency drop into an audible range that can introduce some "noise".

7.3.3 Error Amplifier

The device has a transconductance amplifier as the error amplifier. The error amplifier compares the FB voltage to the lower of the internal soft-start voltage or the internal 0.596-V voltage reference. The transconductance of the error amplifier is 240 µA/V typically. The frequency compensation components are placed internally between the output of the error amplifier and ground.

7.3.4 Slope Compensation and Output Current

The device adds a compensating ramp to the signal of the switch current. This slope compensation prevents subharmonic oscillations as the duty cycle increases. The available peak inductor current remains constant over the full duty-cycle range.

7.3.5 Enable and Adjusting Undervoltage Lockout

The EN pin provides electrical on and off control of the device. When the EN pin voltage exceeds the threshold voltage, the device begins operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters the low-quiescent (IQ) state.

The EN pin has an internal pullup current source which allows the user to float the EN pin to enable the device. If an application requires control of the EN pin, use open-drain or open-collector output logic to interface with the pin.

The device implements internal undervoltage-lockout (UVLO) circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 480 mV.

If an application requires a higher UVLO threshold on the VIN pin, then the EN pin can be configured as shown in 図 7-1. When using the external UVLO function, setting the hysteresis at a value greater than 500 mV is recommended.

The EN pin has a small pullup current, Ip, which sets the default state of the pin to enable when no external components are connected. The pullup current is also used to control the voltage hysteresis for the UVLO function because it increases by Ih when the EN pin crosses the enable threshold. Use 式 1 and 式 2 to calculate the values of R4 and R5 for a specified UVLO threshold.

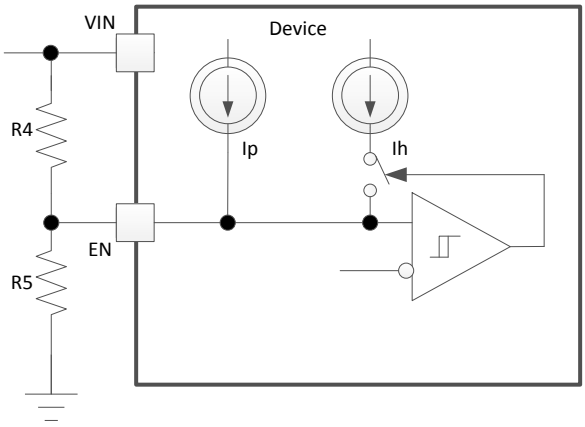


図 7-1. Adjustable VIN Undervoltage Lockout

$$R4 = \frac{V_{START}\left(\frac{V_{ENfalling}}{V_{ENrising}}\right) - V_{STOP}}{I_p\left(1 - \frac{V_{ENfalling}}{V_{ENrising}}\right) + I_h} \quad (1)$$

Where:

- I_p = 0.7 µA
- I_h = 1.55 µA
- $V_{ENfalling}$ = 1.19 V
- $V_{ENrising}$ = 1.22 V

$$R5 = \frac{R4 \times V_{ENfalling}}{V_{STOP} - V_{ENfalling} + R4\left(I_p + I_h\right)} \quad (2)$$

7.3.6 Safe Start-Up into Pre-Biased Outputs

The device has been designed to prevent the low-side MOSFET from discharging a pre-biased output. During monotonic pre-biased start-up, both high-side and low-side MOSFETs are not allowed to be turned on until the internal soft-start voltage is higher than FB pin voltage.

7.3.7 Voltage Reference

The voltage reference system produces a precise ±2.5% voltage-reference over temperature by scaling the output of a temperature stable bandgap circuit. The typical voltage reference is designed at 0.596 V.

7.3.8 Adjusting Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. It is recommended to use divider resistors with 1% tolerance or better. Start with 100 kΩ for the upper resistor divider. Use 式 3 to calculate the output voltage. To improve efficiency at ligh,t loads, consider using larger value resistors. If the values are too high the regulator is more susceptible to noise and voltage errors from the FB input current are noticeable.

$$V_{OUT} = V_{ref} \times \left[\frac{R2}{R3} + 1\right] \quad (3)$$

7.3.9 Internal Soft Start

The TPS54308 device uses the internal soft-start function. The internal soft start time is set to 5 ms (typical).

7.3.10 Bootstrap Voltage (BOOT)

The TPS54308 has an integrated boot regulator and requires a 0.1-µF ceramic capacitor between the BOOT and SW pins to provide the gate drive voltage for the high-side MOSFET. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage. To improve dropout, the TPS54308 is designed to operate at 100% duty cycle as long as the BOOT to SW pin voltage is greater than 2.1 V (typical).

7.3.11 Overcurrent Protection

The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET.

7.3.11.1 High-Side MOSFET Overcurrent Protection

The device implements current mode control, which uses the internal COMP voltage to control the turn-off of the high-side MOSFET and the turn-on of the low-side MOSFET on a cycle-by-cycle basis. During each cycle, the switch current and the current reference generated by the internal COMP voltage are compared. When the peak switch current intersects the current reference, the high-side switch turns off.

7.3.11.2 Low-Side MOSFET Overcurrent Protection

While the low-side MOSFET is turned on, the conduction current is monitored by the internal circuitry. During normal operation, the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current-limit. When the inductor valley current is exceeded by the low-side source current limit, the high-side MOSFET does not turn on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET turns on again when the inductor valley current is below the low-side sourcing current-limit at the start of a cycle as shown in 図 7-2.

Furthermore, if an output overload condition occurs for more than the hiccup wait time, which is programmed for 512 switching cycles, the device shuts down and restarts after the hiccup time of 16384 cycles. Hiccup mode helps reduce the device power dissipation under severe overcurrent conditions.

The low-side MOSFET can also sink current from load. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario, both MOSFETs are off until the start of the next cycle.

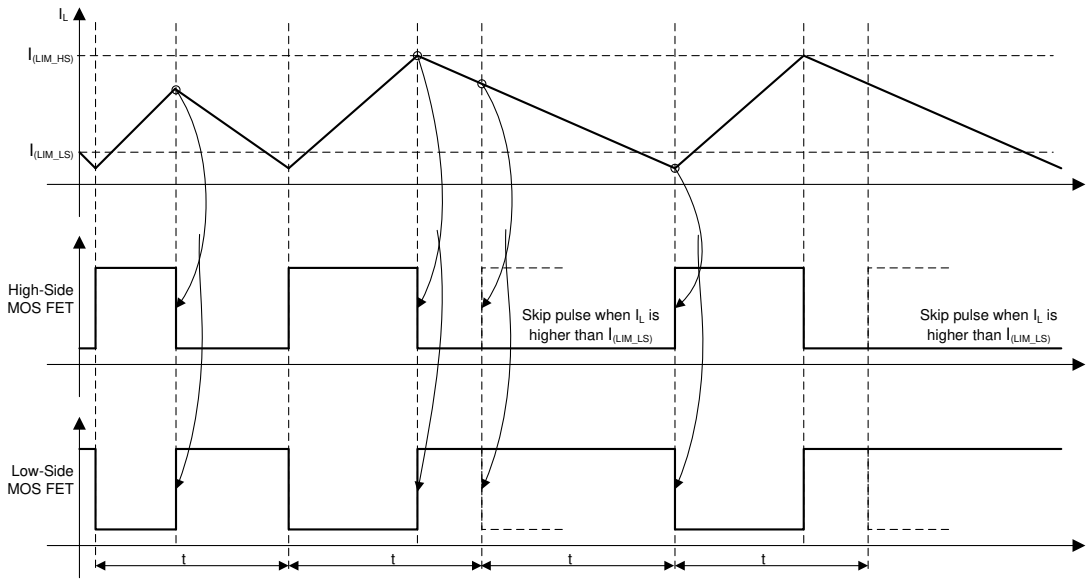


図 7-2. Overcurrent Protection for Both MOSFETs

7.3.12 Output Overvoltage Protection (OVP)

The TPS54308 incorporates an overvoltage transient protection (OVTP) circuit to minimize output voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP circuit includes an overvoltage comparator to compare the FB pin voltage and internal thresholds. When the FB pin voltage goes above 118% × Vref, the high-side MOSFET is forced off. When the FB pin voltage falls below 104% × Vref, the high-side MOSFET is enabled again.

7.3.13 Thermal Shutdown

The internal thermal-shutdown circuitry forces the device to stop switching if the junction temperature exceeds 165°C typically. When the junction temperature drops below 155°C typically, the internal thermal-hiccup timer begins to count. The device reinitiates the power-up sequence after the built-in thermal-shutdown hiccup time (32768 cycles) is over.

7.4 Device Functional Modes

When the input voltage is above the UVLO threshold, the TPS54308 operate in force continuous conduction mode (FCCM). During FCCM, the switching frequency is maintained at an almost constant level over the entire load range.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS54308 is typically used as a step-down converter, which converts an input voltage from 8 V – 28 V to a fixed output voltage of 3.3 V.

8.2 Typical Application

8.2.1 TPS54308 8-V to 28-V Input, 5-V Output Converter

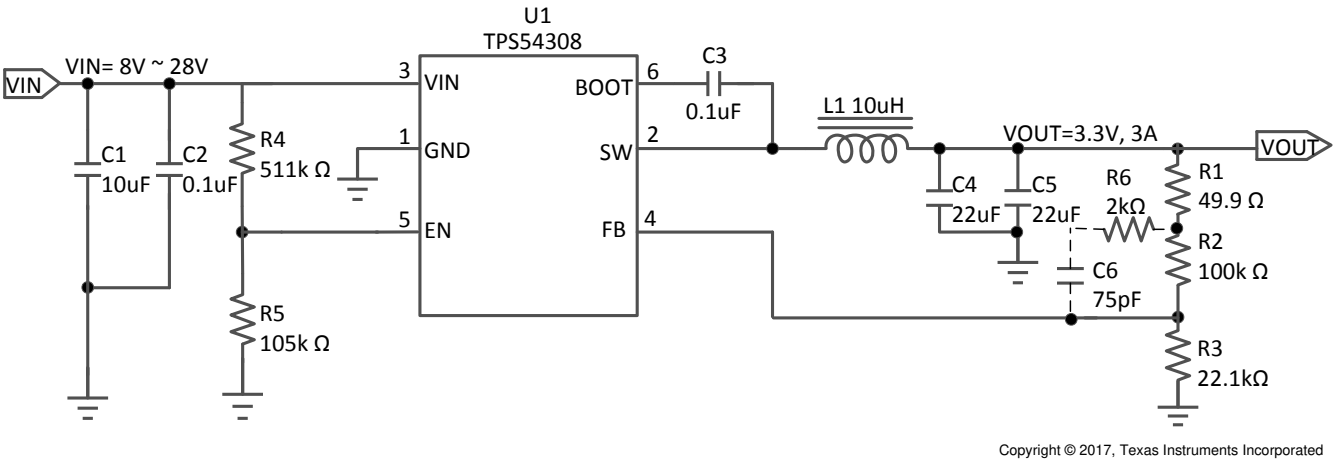


図 8-1. 5-V, 3-A Reference Design

8.2.2 Design Requirements

For this design example, use the parameters in 表 8-1.

表 8-1. Design Parameters

PARAMETER	VALUE
Input voltage range	8 V to 28 V
Output voltage	3.3 V
Output current	3 A
Transient response, 1.5-A load step	ΔV_{OUT} = ±5 %
Input ripple voltage	400 mV
Output voltage ripple	30 mVpp
Switching frequency	350 kHz

8.2.3 Detailed Design Procedure

8.2.3.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS54308 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.3.2 Input Capacitor Selection

The device requires an input decoupling capacitor. A bulk capacitor is also needed, depending on the application. A ceramic capacitor over 10 µF is recommended for the decoupling capacitor. An additional 0.1-µF capacitor (C2) from VIN to GND is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

Use 式 4 to calculate the input ripple voltage (ΔV_{IN}).

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{sw}} + \left(I_{OUT(MAX)} \times ESR_{MAX} \right) \tag{4}$$

where:

- C_{BULK} is the bulk capacitor value
- f_{SW} is the switching frequency
- $I_{OUT(MAX)}$ is the maximum loading current
- ESR_{MAX} is maximum series resistance of the bulk capacitor

The maximum RMS (root mean square) ripple current must also be checked. For worst case conditions, use 式 5 to calculate $I_{CIN(RMS)}$.

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{2} \tag{5}$$

The actual input-voltage ripple is greatly affected by parasitic associated with the layout and the output impedance of the voltage source. 表 8-1 show the actual input voltage ripple for this circuit, which is larger than the calculated value. This measured value is still below the specified input limit of 400 mV. The maximum voltage across the input capacitors is VIN (MAX) + ΔVIN / 2. The selected bypass capacitor is rated for 35 V and the ripple current capacity is greater than 2 A. Both values provide ample margin. The maximum ratings for voltage and current must not be exceeded under any circumstance.

8.2.3.3 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BOOT to SW pin for proper operation. It is recommended to use a ceramic capacitor.

8.2.3.4 Output Voltage Set Point

The output voltage of the TPS54308 device is externally adjustable using a resistor divider network. In the application circuit of 図 8-1, this divider network is comprised of R2 and R3. Use 式 6 and 式 7 to calculate the relationship of the output voltage to the resistor divider.

$$R3 = \frac{R2 \times V_{ref}}{V_{OUT} - V_{ref}} \tag{6}$$

$$V_{OUT} = V_{ref} \times \left[\frac{R2}{R3} + 1\right] \tag{7}$$

Select a value of R2 to be approximately 100 kΩ. Slightly increasing or decreasing R3 can result in closer output voltage matching when using standard value resistors. In this design, R2 = 100 kΩ and R3 = 22.1 kΩ which results in a 3.3-V output voltage. The 49.9-Ω resistor, R1, is provided as a convenient location to break the control loop for stability testing.

8.2.3.5 Undervoltage Lockout Set Point

The undervoltage lockout (UVLO) set point can be adjusted using the external-voltage divider network of R4 and R5. R4 is connected between the VIN and EN pins of the TPS54308 device. R5 is connected between the EN and GND pins. The UVLO has two thresholds: one for power up when the input voltage is rising and one for power down or brownouts when the input voltage is falling. For this example design, the minimum input voltage is 8 V, so the start voltage threshold is set to 6.74 V and the stop voltage threshold is set to 5.83 V. Use 式 1 and 式 2 to calculate the values for the upper and lower resistor values of R4 and R5.

8.2.3.6 Output Filter Components

Two components must be selected for the output filter: the output inductor (L_O) and C_O.

8.2.3.6.1 Inductor Selection

Use 式 8 to calculate the minimum value of the output inductor (L_{MIN}).

$$L_{MIN} = \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times K_{IND} \times I_{OUT} \times f_{sw}} \tag{8}$$

Where:

- K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current

In general, the value of K_{IND} is at the discretion of the designer, however, the following guidelines can be used. For designs using low-ESR output capacitors, such as ceramics, a higher K_{IND} can be used. When using higher-ESR output capacitors, K_{IND} = 0.2 yields better results.

For this design example, use K_{IND} = 0.3. The minimum inductor value is calculated as 9.24 µH. For this design, a close standard value of 10 µH was selected for L_{MIN}.

For the output filter inductor, the RMS current and saturation current ratings must not be exceeded. Use 式 9 to calculate the RMS inductor current ($I_{L(RMS)}$).

$$I_{L(MAX)} = \sqrt{I_{OUT(MAX)}^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT} \right)}{V_{IN(MAX)} \times L_O \times f_{SW} \times 0.8} \right)^2} \quad (9)$$

Use 式 10 to calculate the peak inductor current ($I_{L(PK)}$).

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT} \right)}{1.6 \times V_{IN(MAX)} \times L_O \times f_{SW}} \quad (10)$$

Smaller or larger inductor values can be used, depending on the amount of ripple current the designer wants to allow as long as the other design requirements are met. Larger value inductors have lower AC current and result in lower output voltage ripple. Smaller inductor values increase AC current and output voltage ripple.

8.2.3.6.2 Output Capacitor Selection

Consider three primary factors when selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance must be selected based on the more stringent of these three criteria.

The desired response to a large change in the load current is the first criterion. The output capacitor must supply the load with current when the regulator cannot. This situation occurs if the desired hold-up times are present for the regulator. In this case, the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily unable to supply sufficient output current if a large, fast increase occurs affecting the current requirements of the load, such as a transition from no load to full load. The regulator usually requires two or more clock cycles for the control loop to notice the change in load current and output voltage and to adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for two clock cycles while only allowing a tolerable amount of drop in the output voltage. Use 式 11 to calculate the minimum required output capacitance.

$$C_O > \frac{2 \times \Delta I_{OUT}}{f_{sw} \times \Delta V_{OUT}} \quad (11)$$

Where:

- ΔI_{OUT} is the change in output current
- f_{SW} is the switching frequency of the regulator
- $\Delta V_{(OUT)}$b is the allowable change in the output voltage

For this example, the transient load response is specified as a 5% change in the output voltage, V_{OUT}, for a load step of 1.5 A. For this example, ΔI_{OUT} = 1.5 A and ΔV_{OUT} = 0.05 × 3.3 = 0.165 V. Using these values results in a minimum capacitance of 52 µF. This value does not consider the ESR of the output capacitor in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

式 12 calculates the minimum output capacitance required to meet the output voltage ripple specification. In this case, the maximum output voltage ripple is 30 mV. Under this requirement, 式 12 yields 9.9 µF.

$$C_O > \frac{1}{8 \times f_{SW}} \times \frac{1}{\frac{V_{OUTripple}}{I_{ripple}}} \quad (12)$$

Where:

- f_{SW} is the switching frequency
- $V_{(OUTripple)}$ is the maximum allowable output voltage ripple
- $I_{(ripple)}$ is the inductor ripple current

Use 式 13 to calculate the maximum ESR an output capacitor can have to meet the output-voltage ripple specification. 式 13 indicates the ESR must be less than 36 mΩ. In this case, the ESR of the ceramic capacitor is much smaller than 36 mΩ.

$$R_{ESR} < \frac{V_{OUTripple}}{I_{ripple}} \quad (13)$$

The output capacitor can affect the crossover frequency f_o. Considering to the loop stability and effect of the internal parasitic parameters, choose the crossover frequency less than 40 kHz without considering the feedforward capacitor. A simple estimation for the crossover frequency without the feed forward capacitor C6 is shown in 式 14, assuming C_{OUT} has small ESR.

$$f_o = \frac{5.1}{V_{OUT} \times C_O} \quad (14)$$

Additional capacitance deratings for aging, temperature, and DC bias must be considered, which increases this minimum value. For this example, two 22-µF 25-V, X7R ceramic capacitors are used. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the RMS value of the maximum ripple current. Use 式 15 to calculate the RMS ripple current that the output capacitor must support. For this application, 式 15 yields 120 mA for each capacitor.

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT} \right)}{V_{IN(MAX)} \times L_O \times f_{SW} \times N_C} \right) \quad (15)$$

8.2.3.6.3 Feedforward Capacitor

The TPS54308 is internally compensated. The internal compensation network is composed of two capacitors and one resister shown on the block diagram. Depending on the V_{OUT}, if the output capacitor C_{OUT} is dominated by low ESR (ceramic types) capacitors, it can result in low phase margin. To improve the phase boost, an external feedforward capacitor C6 can be added in parallel with R2. C6 is chosen such that phase margin is boosted at the crossover frequency.

式 16 for C6 was tested:

$$C6 = \frac{1}{2\pi f_o} \times \frac{1}{R2} \tag{16}$$

For this design, feedforward capacitor C6 is not needed since load transient performance looks good and meets design requirement. If further boosting phase margin for low-ESR (ceramic types) capacitors is desired, use 表 8-2 as a starting point for the feedforward capacitor choosing. It also recommends in series with one 2-kΩ resistor (R6) with this feedforward capacitor to get better steady-state performance under high V_{IN} with a heavy load.

表 8-2. Recommended Component Values

V_{OUT} (V)	L (µH)	C_{OUT} (µF)	R2 (kΩ)	R3 (kΩ)	C6 (µF)	R6 (kΩ)
1.8	5.6	66	100	49.9	47	2
2.5	6.8	66	100	31.6	47	2
3.3	10	44	100	22.1	75	2
5	15	44	100	13.3	75	2
12	22	44	100	5.23	100	2

8.2.4 Application Curves

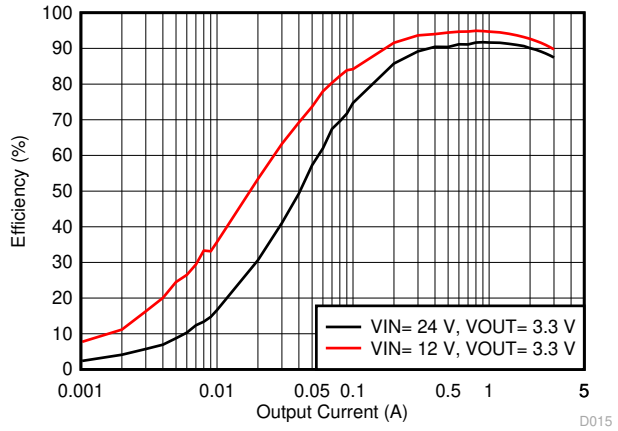


図 8-2. Efficiency

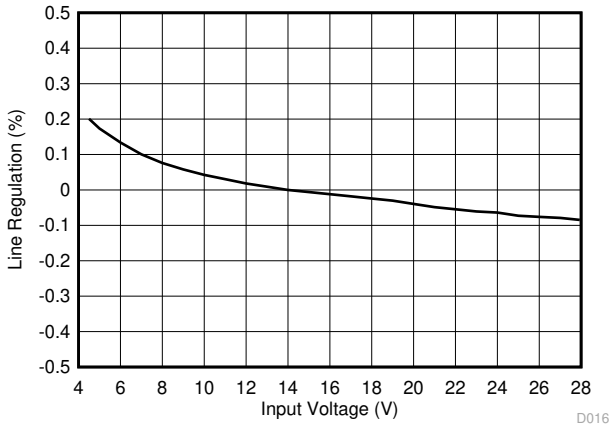


図 8-3. Line Regulation

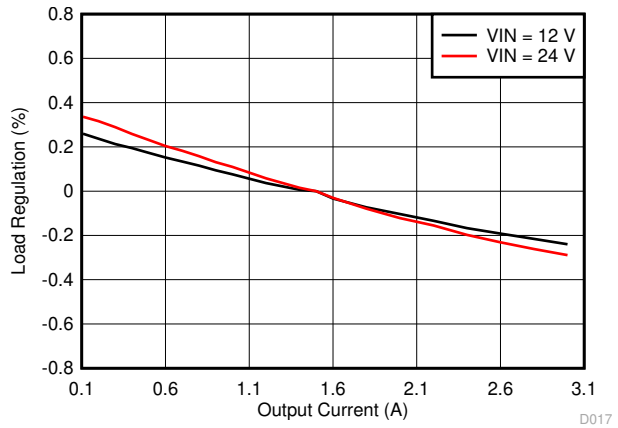


図 8-4. Load Regulation

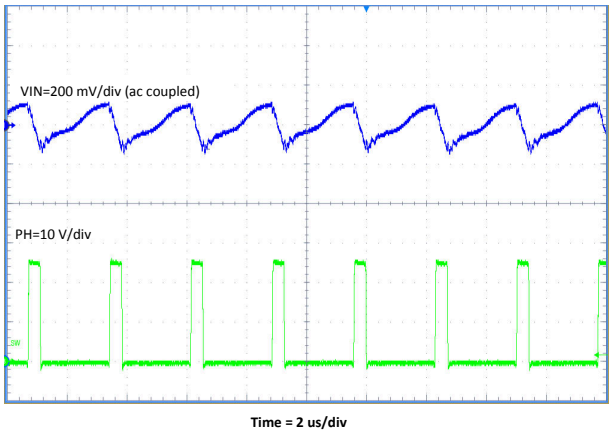
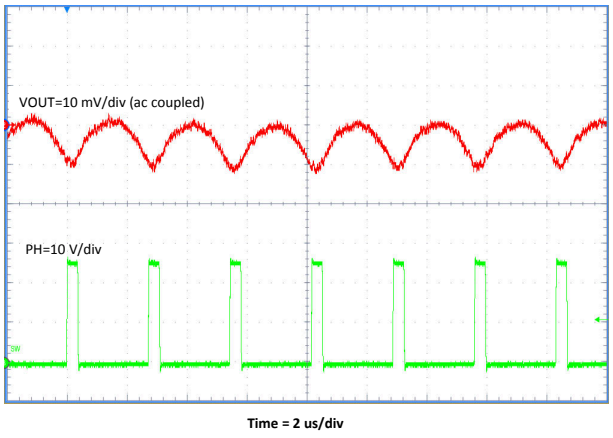
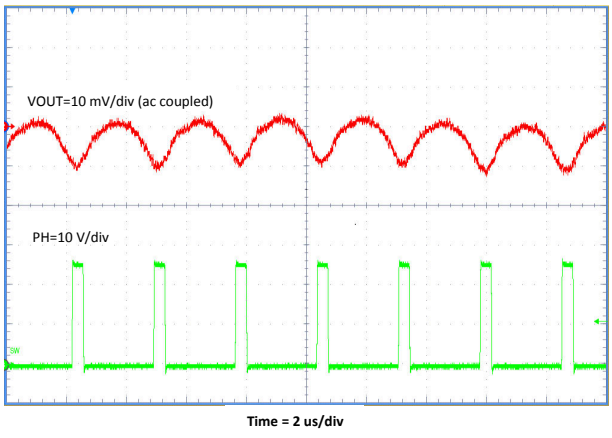


図 8-5. Input Voltage Ripple



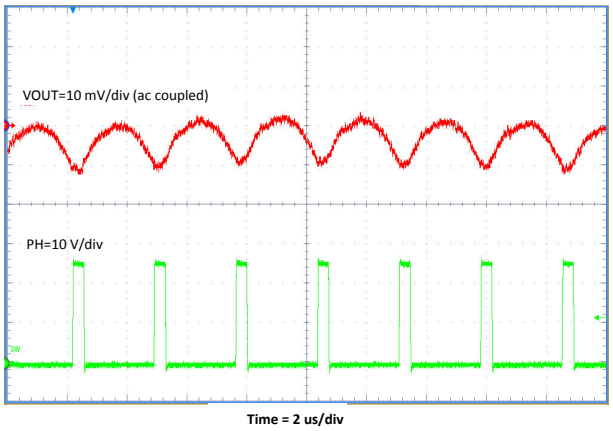
I_{OUT} = 0 A

図 8-6. Output Voltage Ripple



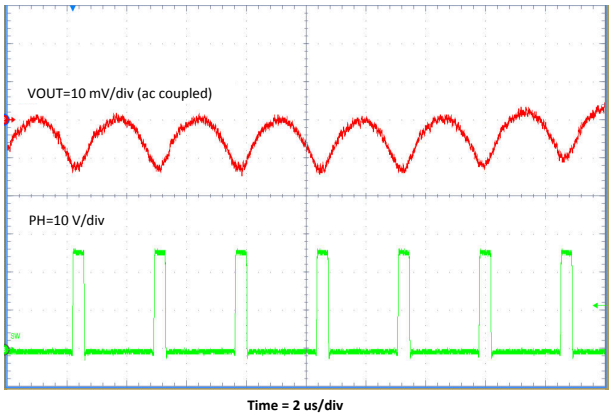
I_{OUT} = 10 mA

図 8-7. Output Voltage Ripple



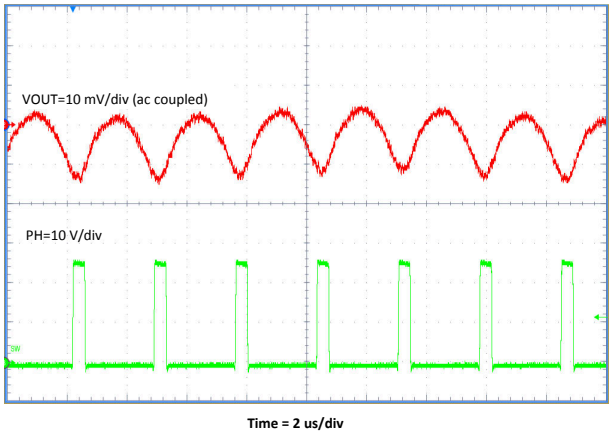
I_{OUT} = 100 mA

図 8-8. Output Voltage Ripple



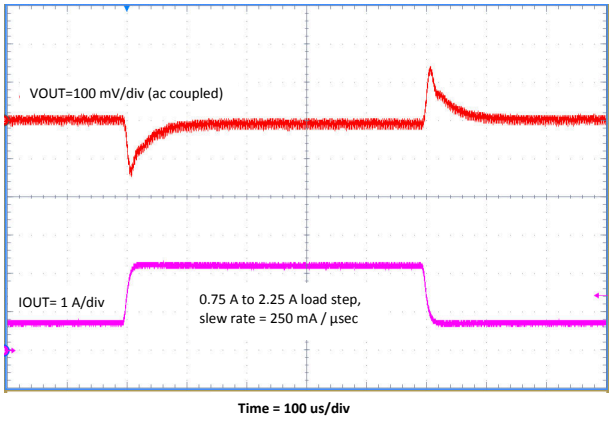
I_{OUT} = 1.5 A

図 8-9. Output Voltage Ripple



I_{OUT} = 3 A

図 8-10. Transient Response



0.75 to 2.25-A load step, slew rate = 250 mA/µsec

図 8-11. Transient Response

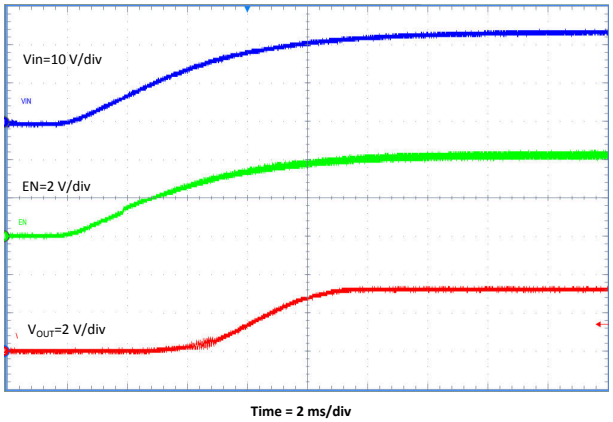


図 8-12. Start-Up Relative to VIN

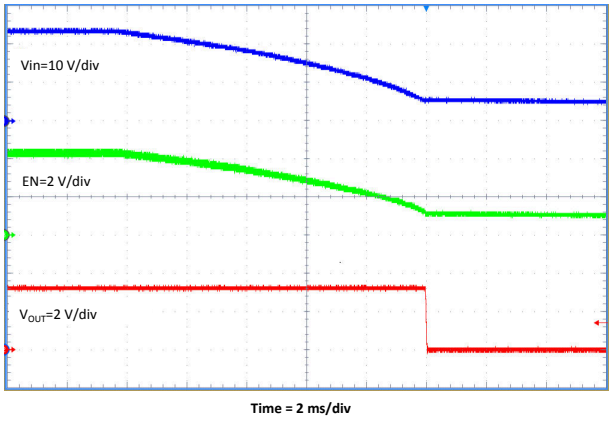


図 8-13. Shutdown Relative to VIN

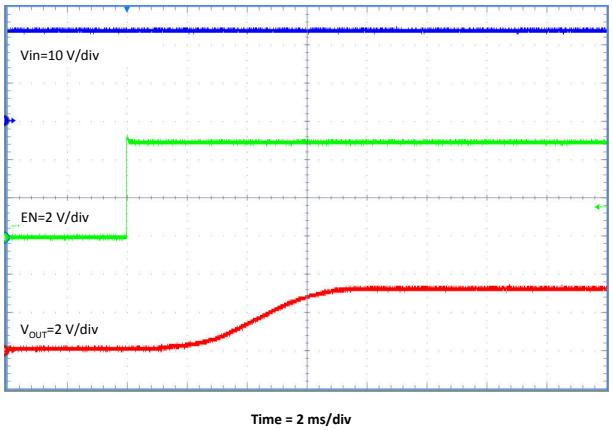


図 8-14. Start-Up Relative to EN

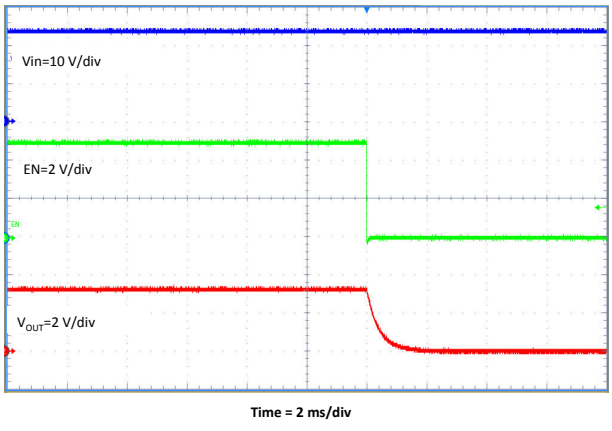


図 8-15. Shutdown Relative to EN

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 4.5 V and 28 V. This input supply must be well regulated. If the input supply is located more than a few inches from the device or converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

- VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
- The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
- Provide sufficient vias for the input capacitor and output capacitor.
- Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
- Do not allow switching current to flow under the device.
- A separate VOUT path should be connected to the upper feedback resistor.
- Make a Kelvin connection to the GND pin for the feedback path.
- Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
- The trace of the VFB node should be as small as possible to avoid noise coupling.
- The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

10.2 Layout Example

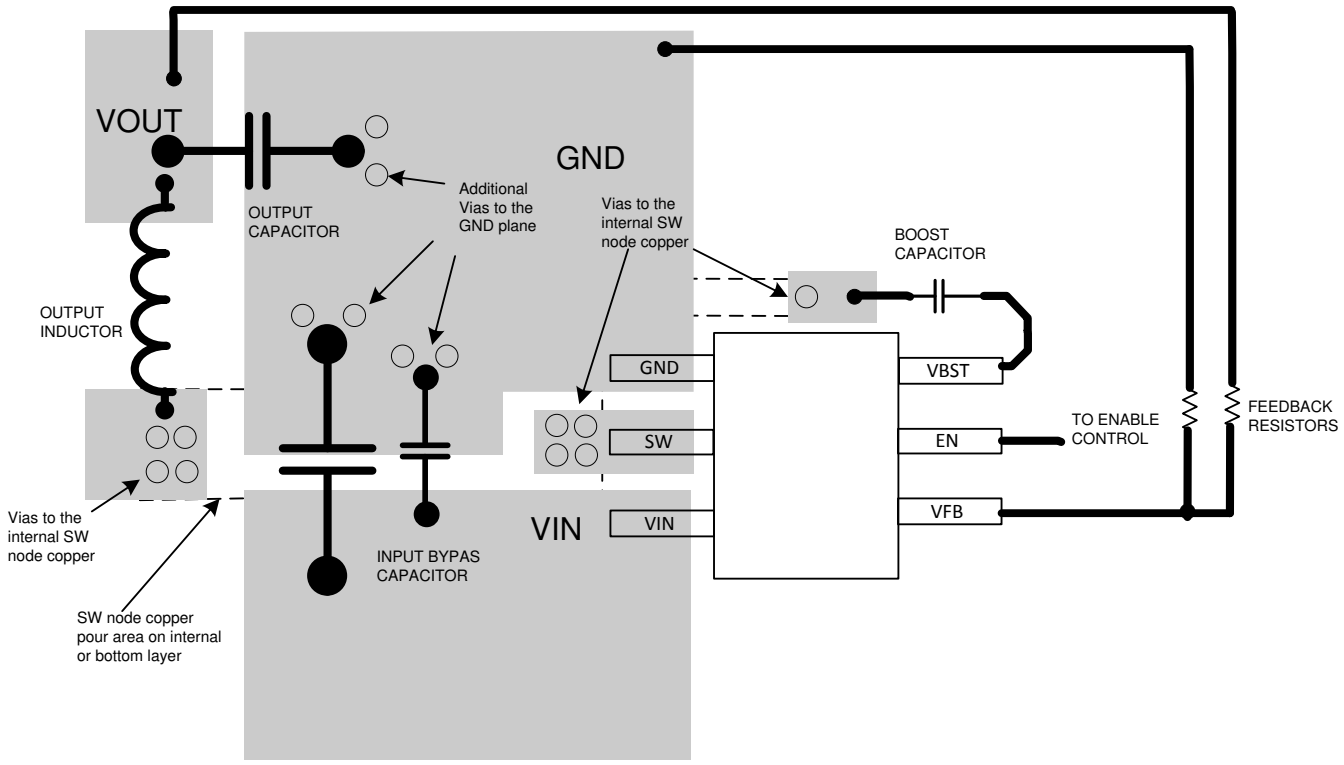


図 10-1. Board Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Development Support

11.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS54308 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
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- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54308DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	4308	Samples
TPS54308DDCT	ACTIVE	SOT-23-THIN	DDC	6	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	4308	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

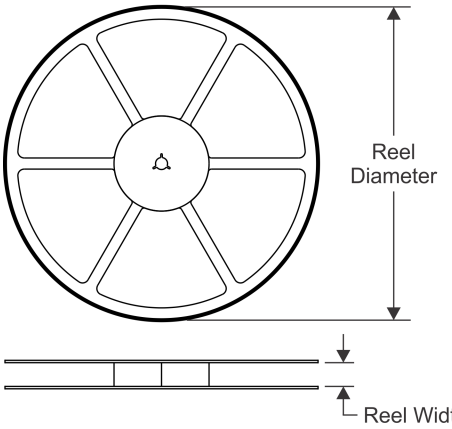
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

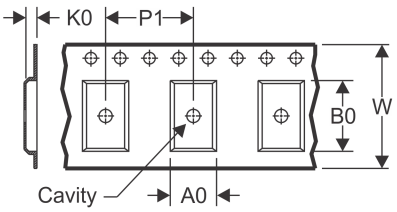
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

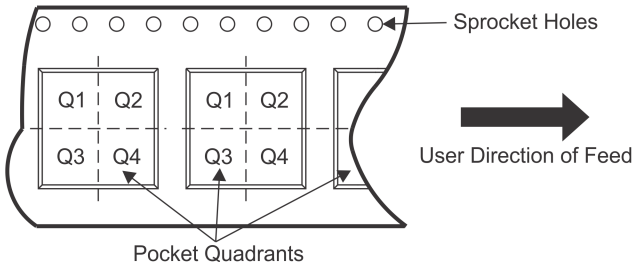


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

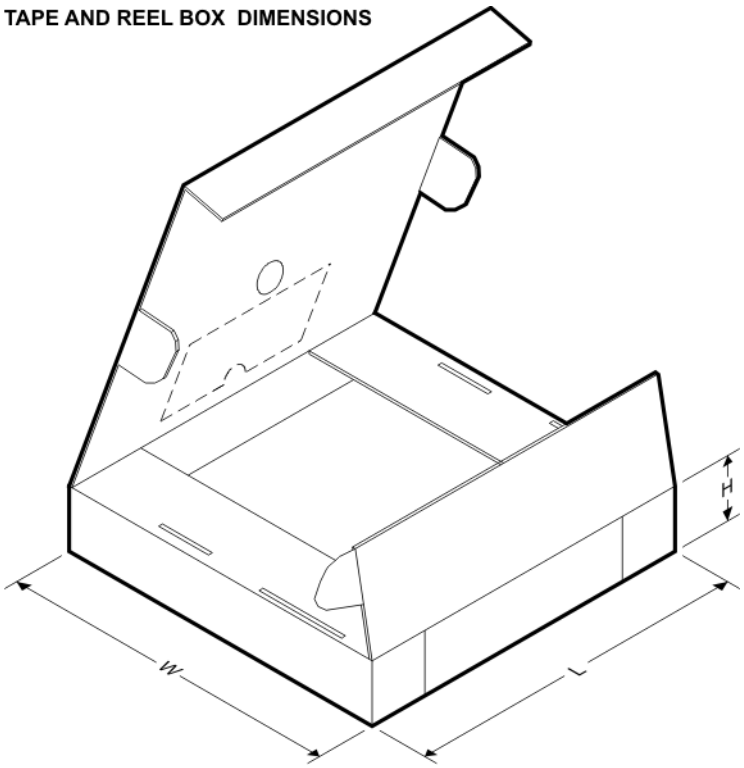
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54308DDCR	SOT-23-THIN	DDC	6	3000	180.0	9.5	3.17	3.1	1.1	4.0	8.0	Q3
TPS54308DDCT	SOT-23-THIN	DDC	6	250	180.0	9.5	3.17	3.1	1.1	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

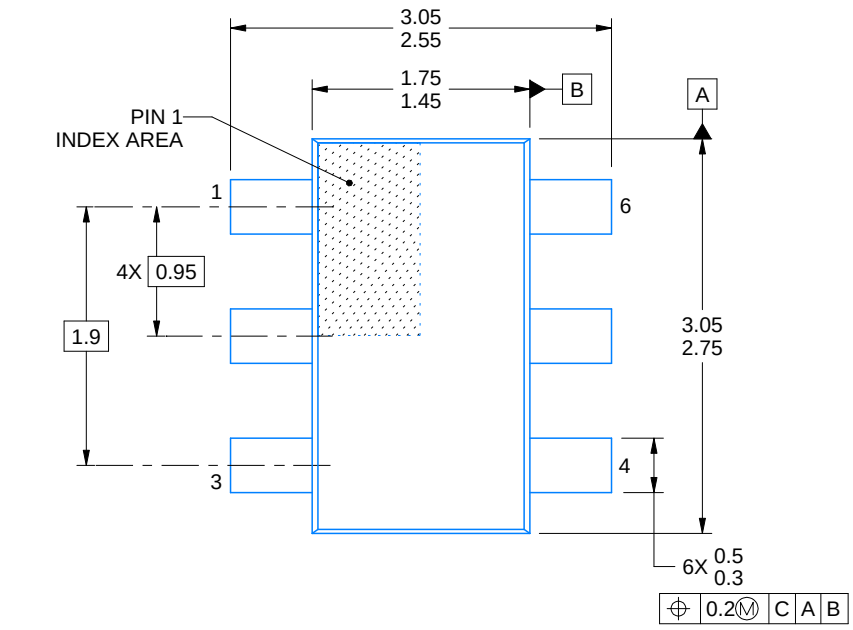
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54308DDCR	SOT-23-THIN	DDC	6	3000	184.0	184.0	19.0
TPS54308DDCT	SOT-23-THIN	DDC	6	250	184.0	184.0	19.0

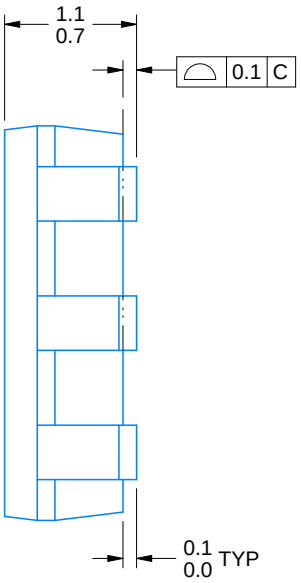
PACKAGE OUTLINE

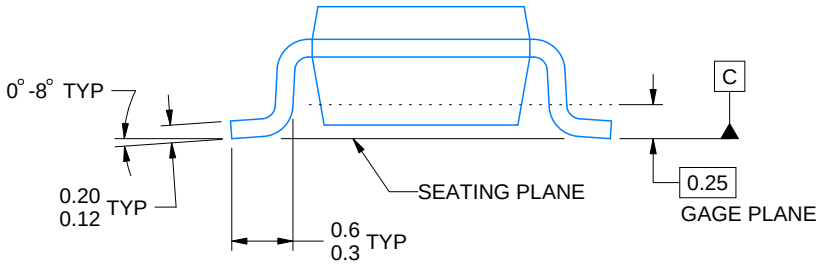
DDC0006A

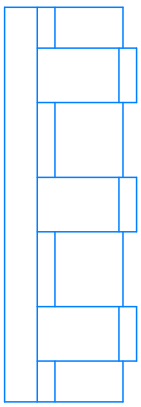
SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR









ALTERNATIVE PACKAGE
SINGULATION VIEW

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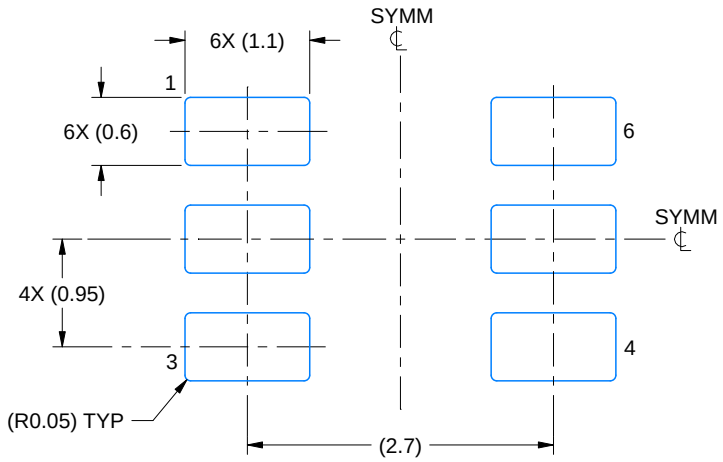
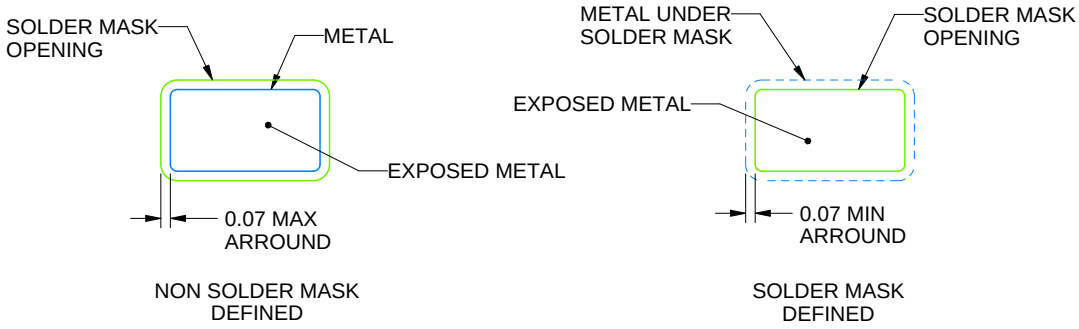
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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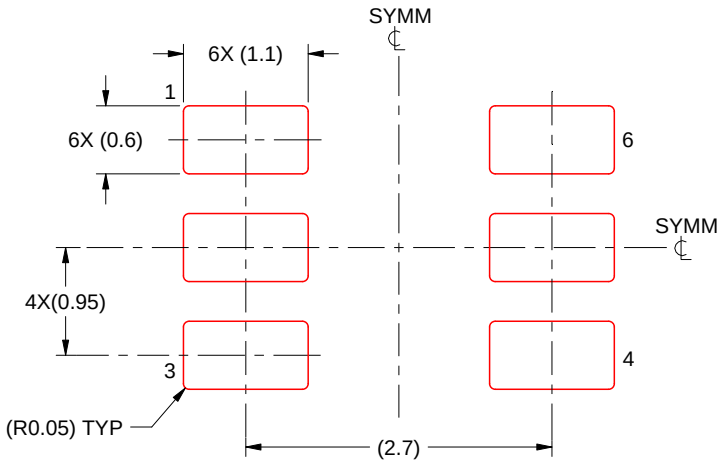
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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