

# TPS543B20 4V<sub>IN</sub>~19V<sub>IN</sub>、25A、スタック可能、適合型内部補償搭載の同期整流降圧型SWIFT™コンバータ

## 1 特長

- 内部で補償される高度な電流モード制御: 25A POL
- 入力電圧範囲: 4V~19V
- 出力電圧範囲: 0.6V~5.5V
- 内蔵の4.1/1.9mΩスタック式 NexFET™電源段と、無損失のローサイド電流センシング
- 固定周波数 - 外部クロックまたはSYNC出力に同期
- ピン・ストラッピングによりスイッチング周波数をプログラム可能
  - スタンドアロンで300kHz~2MHz
  - スタック可能で300kHz~1MHz
- 2xのスタックにより、電流共有、電圧共有、CLK同期で最大50Aが可能
- ピン・ストラッピングにより基準電圧を0.6V~1.1Vにプログラム可能、精度0.5%
- 差動リモート・センシング
- プリバイアス出力への安全なスタートアップ
- 高精度のヒカップ電流制限
- 非同期パルス注入(API)およびボディ・ブレーキング
- 40ピン、5mm×7mm、0.5mmピッチ、単一サーマル・パッドのLQFNパッケージ
- **WEBENCH® Power Designer**により、TPS543B20を使用するカスタム設計を作成

## 2 アプリケーション

- 無線および有線の通信インフラストラクチャ機器
- エンタープライズ・サーバー、スイッチ、ルーター
- エンタープライズ・ストレージ、SSD
- ASIC、SoC、FPGA、DSPコア、I/Oレール

## 3 概要

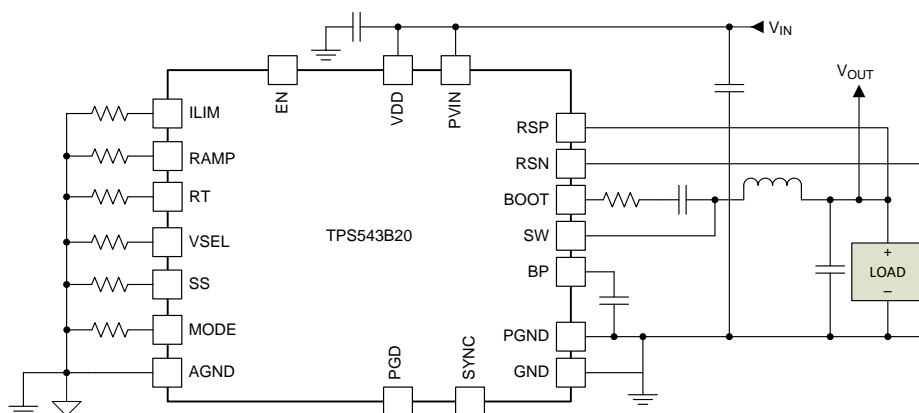
TPS543B20は、EMIに敏感なPOL用に、内部で補償され、エミュレートされるピーク電流モード制御と、クロック同期可能な固定周波数変調器を採用しています。内部積分器と、直接増幅を行うランプ・トラッキング・ループにより、広い範囲の周波数について外部的な補償が必要なくなり、システムの設計が柔軟、高密度、単純になります。オプションのAPIおよびボディ・ブレーキングは、それぞれアンダーシュートとオーバーシュートを大きく低減し、過渡特性の改善に役立ちます。内蔵の NexFET™ MOSFETと低損失のスイッチングにより、高い効率が得られ、最高25Aを供給できます。レイアウトしやすいサーマル・パッドを備えた5mm×7mmの PowerStack™ パッケージで供給されます。2つのTPS543B20デバイスをスタックすると、最高50Aのポイント・オブ・ロード(POL)電流を供給できます。

### 製品情報<sup>(1)</sup>

| 型番        | パッケージ          | 本体サイズ(公称)     |
|-----------|----------------|---------------|
| TPS543B20 | LQFN-CLIP (40) | 5.00mm×7.00mm |

1. 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

### 概略回路図



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## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

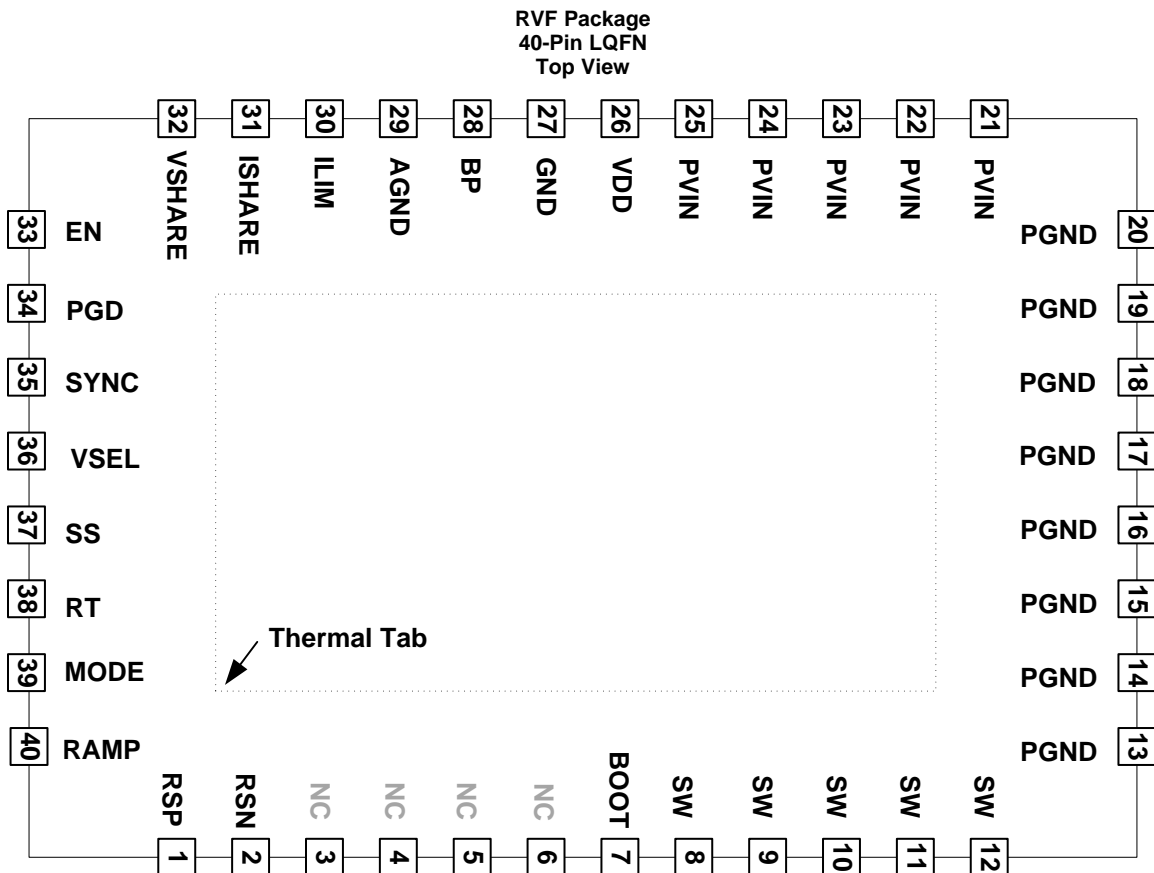
| Revision A (July 2017) から Revision B に変更                                                                                       | Page |
|--------------------------------------------------------------------------------------------------------------------------------|------|
| • データシートのタイトルに「スタック可能」を追加.....                                                                                                 | 1    |
| • スタック可能な周波数オプションを追加.....                                                                                                      | 1    |
| • Added Frequency range for stackable applications .....                                                                       | 10   |
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| • 追加 "Place a 10-nF to 100-nF capacitor close to IC from Pin 25 VIN to Pin 27 GND." to <a href="#">Layout Guidelines</a> ..... | 32   |

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| • 変更 "40-A" to "25-A" ..... | 14   |
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## 5 Device Comparison Table

| DEVICE    | OUTPUT CURRENT |
|-----------|----------------|
| TPS543B20 | 25 A           |
| TPS543C20 | 40 A           |

## 6 Pin Configuration and Functions



### Pin Functions

| PIN     |             | I/O/P <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                                                                                                                                 |
|---------|-------------|----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NO.     | NAME        |                      |                                                                                                                                                                                                                                                                                                             |
| 1       | RSP         | I                    | The positive input of the remote sense amplifier. Connect RSP pin to the output voltage at the load. For multi-phase configuration, the remote sense amplifier is not needed for slave devices.                                                                                                             |
| 2       | RSN         | I                    | The negative input of the remote sense amplifier. Connect RSN pin to the ground at load side. For multi-phase configuration, the remote sense amplifier is not needed for slave devices.                                                                                                                    |
| 3 – 6   | NC          |                      | Not connected                                                                                                                                                                                                                                                                                               |
| 7       | BOOT        | I                    | Bootstrap pin for the internal flying high-side driver. Connect a typical 100-nF capacitor from this pin to SW. To reduce the voltage spike at SW, a BOOT resistor with a value between 1 $\Omega$ to 10 $\Omega$ may be placed in series with the BOOT capacitor to slow down turnon of the high-side FET. |
| 8 – 12  | SW          | B                    | Output of converted power. Connect this pin to the output Inductor.                                                                                                                                                                                                                                         |
| 13 – 20 | PGND        | G                    | These ground pins are connected to the return of the internal low-side MOSFET                                                                                                                                                                                                                               |
| 21 – 25 | PVIN        | I                    | Input power to the power stage. Low impedance bypassing of these pins to PGND is critical. A 10-nF to 100-nF capacitor from PVIN to PGND close to IC is required.                                                                                                                                           |
| 26      | VDD         | I                    | Controller power supply input                                                                                                                                                                                                                                                                               |
| 27      | GND         | G                    | Ground return for the controller. This pin should be directly connected to the thermal pad on the PCB board. A 10-nF to 100-nF capacitor from PVIN to GND close to IC is required.                                                                                                                          |
| 28      | BP          | O                    | Output of the 5 V on board regulator. This regulator powers the driver stage of the controller and must be bypassed with a minimum of 2.2 $\mu$ F to the thermal pad (power stage ground, that is, GND). Low impedance bypassing of this pin to PGND is critical.                                           |
| 29      | AGND        | G                    | GND return for internal analog circuits.                                                                                                                                                                                                                                                                    |
| 30      | ILIM        | O                    | Current protection pin; connect a resistor from this pin to AGND sets current limit level.                                                                                                                                                                                                                  |
| 31      | ISHARE      | I                    | Current sharing signal for multi-phase operation. Float this pin for single phase.                                                                                                                                                                                                                          |
| 32      | VSHARE      | B                    | Voltage sharing signal for multi-phase operation. Float this pin for single phase.                                                                                                                                                                                                                          |
| 33      | EN          | I                    | The enable pin turns on the switcher.                                                                                                                                                                                                                                                                       |
| 34      | PGD         | O                    | Open-drain power-good status signal which provides start-up delay after the FB voltage falls within the specified limits. After the FB voltage moves outside the specified limits, PGOOD goes low.                                                                                                          |
| 35      | SYNC        | B                    | For frequency synchronization. This pin can be configured as sync in or sync out by MODE pin and RT pin for master and slave devices.                                                                                                                                                                       |
| 36      | VSEL        | I                    | Connect a resistor from this pin to AGND to select internal reference voltage.                                                                                                                                                                                                                              |
| 37      | SS          | O                    | Connect a resistor from this pin to AGND to select soft-start time.                                                                                                                                                                                                                                         |
| 38      | RT          | O                    | Frequency setting pin. Connect a resistor from this pin to AGND to program the switching frequency. This pin also selects sync point for devices in stackable applications                                                                                                                                  |
| 39      | MODE        | B                    | Enable or disable API or body brake function, choose API threshold, also selects the operation mode in stackable applications                                                                                                                                                                               |
| 40      | RAMP        | B                    | Ramp level selection, with a resistor to AGND to adjust internal loop.                                                                                                                                                                                                                                      |
| –       | Thermal Tab | –                    | Package thermal tab, internally connected to PGND. The thermal tab must have adequate solder coverage for proper operation.                                                                                                                                                                                 |

(1) I = Input, O = Output, B = Bidirectional, P = Supply, G = Ground

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

|                                       |                                    | MIN     | MAX  | UNIT |     |  |
|---------------------------------------|------------------------------------|---------|------|------|-----|--|
| Input voltage                         | VIN                                | -0.3    | 20   | V    |     |  |
|                                       | VIN to SW                          | DC      | -0.3 |      | 24  |  |
|                                       |                                    | < 10 ns | -5   |      | 24  |  |
|                                       | VDD                                | -0.3    | 22   |      |     |  |
|                                       | BOOT                               | -0.3    | 34.5 |      |     |  |
|                                       | BOOT to SW                         | DC      | -0.3 |      | 6.5 |  |
|                                       |                                    | < 10 ns | -0.3 |      | 7   |  |
|                                       | VSEL, SS, MODE, RT, SYNC, EN, ILIM |         | -0.3 |      | 7   |  |
|                                       | RSP                                |         | -0.3 |      | 3.6 |  |
|                                       | RSN                                |         | -0.3 |      | 0.3 |  |
| PGND, GND                             |                                    | -0.3    | 03   |      |     |  |
| SW                                    | DC                                 | -0.3    | 24   |      |     |  |
|                                       | < 10 ns                            | -5      | 24   |      |     |  |
| Output voltage                        | BP, RAMP                           | -0.3    | 7    | V    |     |  |
|                                       | PGD                                | -0.3    | 7    |      |     |  |
| Junction temperature, T <sub>J</sub>  |                                    | -55     | 150  | °C   |     |  |
| Storage temperature, T <sub>stg</sub> |                                    | -55     | 150  | °C   |     |  |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the network ground terminal unless otherwise noted.

### 7.2 ESD Ratings

|                                            |                                                                                | VALUE | UNIT |
|--------------------------------------------|--------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2500 | V    |
|                                            | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±1500 |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

### 7.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                       |                                    |         | MIN  | MAX  | UNIT |
|---------------------------------------|------------------------------------|---------|------|------|------|
| Input voltage <sup>(2)</sup>          | VIN                                |         | 4    | 19   | V    |
|                                       | VIN to SW                          | DC      | -0.1 | 24   |      |
|                                       |                                    | < 10 ns | -3   | 24   |      |
|                                       | VDD                                |         | 4    | 22   |      |
|                                       | BOOT                               |         | -0.1 | 23.5 |      |
|                                       | BOOT to SW                         | DC      | -0.1 | 5.5  |      |
|                                       |                                    | < 10 ns | -0.1 | 6    |      |
|                                       | VSEL, SS, MODE, RT, SYNC, EN, ILIM |         | -0.1 | 5.5  |      |
|                                       | RSP                                |         | -0.1 | 1.7  |      |
|                                       | RSN                                |         | -0.1 | 0.1  |      |
| PGND, GND                             |                                    | -0.1    | 0.1  |      |      |
| SW                                    | DC                                 | -0.1    | 24   |      |      |
|                                       | < 10 ns                            | -5      | 24   |      |      |
| Output voltage <sup>(2)</sup>         | BP, RAMP                           |         | -0.3 | 7    | V    |
|                                       | PGD                                |         | -0.3 | 7    |      |
| Junction temperature, T <sub>J</sub>  |                                    |         | -40  | 125  | °C   |
| Storage temperature, T <sub>stg</sub> |                                    |         | -55  | 125  | °C   |

(1) Stresses beyond those listed under may cause permanent damage to the device.

(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

### 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | TPS543B20  | UNIT |
|-------------------------------|----------------------------------------------|------------|------|
|                               |                                              | RVF (LQFN) |      |
|                               |                                              | 40 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 29.1       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 19.3       | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 4.2        | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 1.4        | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 4.2        | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 1.2        | °C/W |

 (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                  |                                                                               | TEST CONDITIONS                                                             | MIN   | TYP      | MAX   | UNIT             |
|--------------------------------------------|-------------------------------------------------------------------------------|-----------------------------------------------------------------------------|-------|----------|-------|------------------|
| <b>MOSFET <math>R_{DS(on)}</math></b>      |                                                                               |                                                                             |       |          |       |                  |
| $R_{DS(on)HS}$                             | HS FET                                                                        | VBST – VSW = 5 V, $I_D = 20$ A, $T_j = 25^\circ\text{C}$                    |       | 4.1      |       | m $\Omega$       |
| $R_{DS(on)LS}$                             | LS FET                                                                        | VDD = 5 V, $I_D = 20$ A, $T_j = 25^\circ\text{C}$                           |       | 1.9      |       | m $\Omega$       |
| $t_{DEAD(LtoH)}$                           | Power stage driver dead-time from Low-side off to High-side on <sup>(1)</sup> | VDD $\geq 12$ V, $T_j = 25^\circ\text{C}$                                   |       | 12       |       | ns               |
| $t_{DEAD(HtoL)}$                           | Power stage driver dead-time from High-side off to Low-side on <sup>(1)</sup> | VDDN $\geq 12$ V, $T_j = 25^\circ\text{C}$                                  |       | 15       |       | ns               |
| <b>INPUT SUPPLY and CURRENT</b>            |                                                                               |                                                                             |       |          |       |                  |
| $V_{VIN}$                                  | Power stage voltage                                                           |                                                                             | 4     |          | 19    |                  |
| $V_{VDD}$                                  | VDD supply voltage                                                            |                                                                             | 4     |          | 22    |                  |
| $I_{VDD}$                                  | VDD bias current                                                              | $T_A = 25^\circ\text{C}$ , no load, power conversion enabled (no switching) |       | 4.3      |       | mA               |
| $I_{VDDSTBY}$                              | VDD standby current                                                           | $T_A = 25^\circ\text{C}$ , no load, power conversion disabled               |       | 4.3      |       | mA               |
| <b>UNDERVOLTAGE LOCKOUT</b>                |                                                                               |                                                                             |       |          |       |                  |
| $V_{VDD\_UVLO}$                            | VDD UVLO rising threshold                                                     |                                                                             |       | 3.8      |       | V                |
| $V_{VDD\_UVLO\_HYS}$                       | VDD UVLO hysteresis                                                           |                                                                             |       | 0.2      |       | v                |
| $V_{VIN\_UVLO}$                            | VIN UVLO rising threshold                                                     |                                                                             |       | 3.2      |       | V                |
| $V_{VIN\_UVLO\_HYS}$                       | VIN UVLO hysteresis                                                           |                                                                             |       | 0.2      |       | v                |
| $V_{EN\_ON\_TH}$                           | EN on threshold                                                               |                                                                             | 1.45  | 1.6      | 1.75  | V                |
| $V_{HYS}$                                  | EN hysteresis                                                                 |                                                                             | 270   | 300      | 330   | mV               |
| $I_{EN\_LKG}$                              | EN input leakage current                                                      |                                                                             | -1    | 0        | 1     | $\mu\text{A}$    |
| <b>INTERNAL REFERENCE VOLTAGE</b>          |                                                                               |                                                                             |       |          |       |                  |
| $V_{INTREF}$                               | Internal REF voltage                                                          | $R_{VSEL} = \text{OPEN}$                                                    |       | 1000     |       | mV               |
| $V_{INTREFTOL}$                            | Internal REF voltage tolerance                                                | $T_j = -40^\circ\text{C}$ to $125^\circ\text{C}$                            | -0.5% |          | +0.5% |                  |
| $V_{INTREF\_VSEL}$                         | Internal REF voltage range                                                    | Programable by VSEL (pin 36)                                                | 0.6   |          | 1.1   | V                |
| <b>OUTPUT VOLTAGE</b>                      |                                                                               |                                                                             |       |          |       |                  |
| $I_{RSP}$                                  | RSP input current                                                             | $V_{RSP} = 600$ mV                                                          | -1    |          | 1     | $\mu\text{A}$    |
| <b>DIFFERENTIAL REMOTE SENSE AMPLIFIER</b> |                                                                               |                                                                             |       |          |       |                  |
| $f_{UGBW}$                                 | Unity gain bandwidth <sup>(1)</sup>                                           |                                                                             | 5     | 8.5      |       | MHz              |
| A0                                         | Open loop gain <sup>(1)</sup>                                                 |                                                                             | 75    |          |       | dB               |
| SR                                         | SLew rate <sup>(1)</sup>                                                      |                                                                             |       | $\pm 10$ |       | V/ $\mu\text{s}$ |
| $V_{ICM}$                                  | Input common mode range <sup>(1)</sup>                                        |                                                                             | -0.2  |          | 1.7   | V                |
| $V_{OFFSET}$                               | Input offset voltage <sup>(1)</sup>                                           | $V_{RSN-VGND} = 0$ mV                                                       | -1    |          | 1     | mV               |
|                                            |                                                                               | $V_{RSN-VGND} = \pm 100$ mV                                                 | -1.9  |          | 1.9   |                  |

(1) Specified by design. Not production tested.

**Electrical Characteristics (continued)**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                        |                                                                              | TEST CONDITIONS                                                     | MIN                       | TYP  | MAX | UNIT |
|----------------------------------|------------------------------------------------------------------------------|---------------------------------------------------------------------|---------------------------|------|-----|------|
| <b>SWITCHING FREQUENCY</b>       |                                                                              |                                                                     |                           |      |     |      |
| F <sub>SW</sub>                  | V <sub>O</sub> switching frequency maximum frequency for multi-phase is 1MHz | V <sub>IN</sub> = 12 V, V <sub>VO</sub> = 1 V, RT = 66.5 kΩ         |                           | 300  |     | kHz  |
|                                  |                                                                              | V <sub>IN</sub> = 12 V, V <sub>VO</sub> = 1 V, RT = 48.7 kΩ         |                           | 400  |     |      |
|                                  |                                                                              | V <sub>IN</sub> = 12 V, V <sub>VO</sub> = 1 V, RT = 39.2 kΩ         |                           | 500  |     |      |
|                                  |                                                                              | V <sub>IN</sub> = 12 V, V <sub>VO</sub> = 1 V, RT = 28.0 kΩ         |                           | 700  |     |      |
|                                  |                                                                              | V <sub>IN</sub> = 12 V, V <sub>VO</sub> = 1 V, RT = 22.6 kΩ         |                           | 850  |     |      |
|                                  |                                                                              | V <sub>IN</sub> = 12 V, V <sub>VO</sub> = 1 V, RT = 19.1 kΩ         |                           | 1000 |     |      |
|                                  |                                                                              | V <sub>IN</sub> = 12 V, V <sub>VO</sub> = 1 V, RT = 15.4 kΩ         |                           | 1200 |     |      |
|                                  |                                                                              | V <sub>IN</sub> = 12 V, V <sub>VO</sub> = 1 V, RT = 8.06 kΩ         |                           | 2000 |     |      |
| t <sub>ON(min)</sub>             | Minimum on-time <sup>(1)</sup>                                               | DRVH rising to falling                                              |                           | 30   |     | ns   |
| t <sub>OFF(min)</sub>            | Minimum off-time <sup>(1)</sup>                                              | DRVH falling to rising                                              |                           | 250  |     | ns   |
| <b>INTERNAL BOOTSTRAP SWITCH</b> |                                                                              |                                                                     |                           |      |     |      |
| V <sub>F</sub>                   | Forward voltage                                                              | V <sub>BP-VBST</sub> , T <sub>A</sub> = 25°C, I <sub>F</sub> = 5 mA |                           | 0.1  | 0.2 | V    |
| <b>VSEL</b>                      |                                                                              |                                                                     |                           |      |     |      |
| VSEL                             | Internal reference voltage                                                   | R <sub>VSEL</sub> = 0 kΩ                                            |                           | 0.6  |     | V    |
|                                  |                                                                              | R <sub>VSEL</sub> = 8.66 kΩ                                         |                           | 0.7  |     |      |
|                                  |                                                                              | R <sub>VSEL</sub> = 15.4 kΩ                                         |                           | 0.75 |     |      |
|                                  |                                                                              | R <sub>VSEL</sub> = 23.7 kΩ                                         |                           | 0.8  |     |      |
|                                  |                                                                              | R <sub>VSEL</sub> = 34.8 kΩ                                         |                           | 0.85 |     |      |
|                                  |                                                                              | R <sub>VSEL</sub> = 51.1 kΩ                                         |                           | 0.9  |     |      |
|                                  |                                                                              | R <sub>VSEL</sub> = 78.7 kΩ                                         |                           | 0.95 |     |      |
|                                  |                                                                              | R <sub>VSEL</sub> = OPEN                                            |                           | 1    |     |      |
|                                  |                                                                              | R <sub>VSEL</sub> = 121 kΩ                                          |                           | 1.05 |     |      |
|                                  |                                                                              | R <sub>VSEL</sub> = 187 kΩ                                          |                           | 1.1  |     |      |
| <b>SOFT START</b>                |                                                                              |                                                                     |                           |      |     |      |
| t <sub>SS</sub>                  | Soft-start time                                                              | V <sub>O</sub> rising from 0 V to 95% of final set point            | R <sub>SS</sub> = 0 kΩ    |      | 0.5 | ms   |
|                                  |                                                                              |                                                                     | R <sub>SS</sub> = 8.66 kΩ |      | 1   |      |
|                                  |                                                                              |                                                                     | R <sub>SS</sub> = 15.4 kΩ |      | 2   |      |
|                                  |                                                                              |                                                                     | R <sub>SS</sub> = Open    |      | 4   |      |
|                                  |                                                                              |                                                                     | R <sub>SS</sub> = 23.7 kΩ |      | 5   |      |
|                                  |                                                                              |                                                                     | R <sub>SS</sub> = 34.8 kΩ |      | 8   |      |
|                                  |                                                                              |                                                                     | R <sub>SS</sub> = 51.1 kΩ |      | 12  |      |
|                                  |                                                                              |                                                                     | R <sub>SS</sub> = 78.7 kΩ |      | 16  |      |
|                                  |                                                                              |                                                                     | R <sub>SS</sub> = 121 kΩ  |      | 24  |      |
|                                  |                                                                              |                                                                     | R <sub>SS</sub> = 187 kΩ  |      | 32  |      |
| <b>POWER ON DELAY</b>            |                                                                              |                                                                     |                           |      |     |      |
| t <sub>PODLY</sub>               | Power-on delay time                                                          | Delay from enable to switching                                      |                           | 512  |     | μs   |



## Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

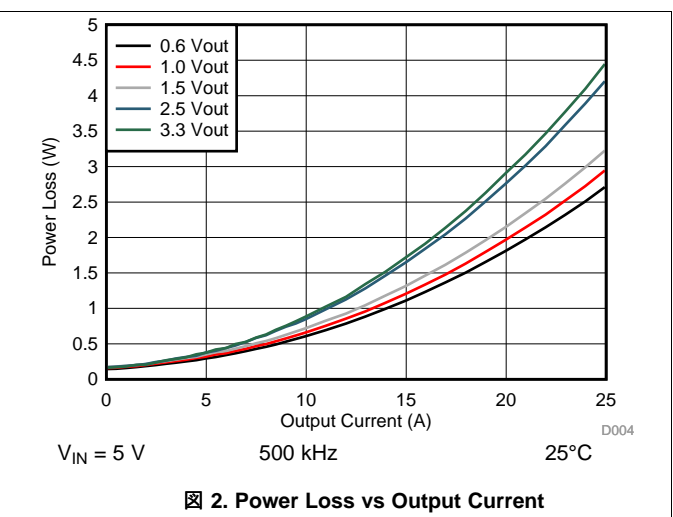
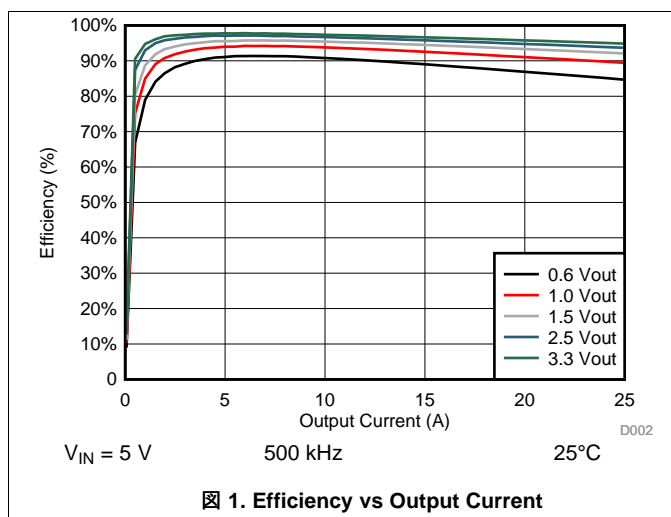
| PARAMETER                     |                                                                                                                                                                             | TEST CONDITIONS                                    | MIN  | TYP        | MAX | UNIT          |
|-------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------|------|------------|-----|---------------|
| <b>PGOOD COMPARATOR</b>       |                                                                                                                                                                             |                                                    |      |            |     |               |
| $V_{PG(thresh)}$              | OV warning threshold on RSP pin, PGOOD fault threshold on rising                                                                                                            | $V_{REF} = 600\text{ mV}$                          | 108  | 112        | 116 | % $V_{REF}$   |
|                               | UV warning threshold on RSP pin, PGOOD fault threshold on falling                                                                                                           | $V_{REF} = 600\text{ mV}$                          | 84   | 88         | 92  |               |
| $V_{PGD(rise)}$               | PGOOD threshold on rising and UV warning threshold de-assertion threshold at RSP pin                                                                                        | $V_{REF} = 600\text{ mV}$                          |      | 95         |     | % $V_{REF}$   |
| $V_{PGD(fall)}$               | PGOOD threshold on falling and OV warning threshold de-assertion threshold at RSP pin                                                                                       | $V_{REF} = 600\text{ mV}$                          |      | 105        |     | % $V_{REF}$   |
| $R_{PGD}$                     | PGOOD pulldown resistance                                                                                                                                                   | $I_{PGOOD} = 5\text{ mA}$ , $V_{RSP} = 0\text{ V}$ | 30   | 45         | 60  | $\Omega$      |
| $t_{PGDLY}$                   | PGOOD delay time                                                                                                                                                            | Delay for PGOOD going in                           |      | 1.024      |     | ms            |
|                               |                                                                                                                                                                             | Delay for PGOOD coming out                         |      |            | 2   | $\mu\text{s}$ |
| $V_{PGD(OL)}$                 | PGOOD output low level voltage at no supply voltage                                                                                                                         | $V_{DD}=0$ , $I_{PGOOD} = 80\text{ }\mu\text{A}$   |      |            | 0.8 | V             |
| $I_{PGLK}$                    | PGOOD leakage current                                                                                                                                                       | $V_{PGOOD} = 5\text{ V}$                           |      |            | 15  | $\mu\text{A}$ |
| <b>CURRENT SHARE ACCURACY</b> |                                                                                                                                                                             |                                                    |      |            |     |               |
| $I_{SHARE(acc)}$              | Output current sharing accuracy among stackable devices, defined as the ratio of the current difference between devices to total current(sensing error only) <sup>(1)</sup> | $I_{OUT} \geq 20\text{ A/phase}$                   | -15% |            | 15% |               |
|                               |                                                                                                                                                                             | $I_{OUT} \leq 20\text{ A/phase}$                   |      | $\pm 3$    |     | A             |
| <b>CURRENT DETECTION</b>      |                                                                                                                                                                             |                                                    |      |            |     |               |
| $V_{ILIM}$                    | $V_{TRIP}$ voltage range                                                                                                                                                    | $R_{dson}$ sensing                                 | 0.1  |            | 1.2 | V             |
| $I_{OCP}$                     | Low-side FET current protection threshold and tolerance                                                                                                                     | $R_{ILIM} = 48.7\text{ k}\Omega$                   |      | 20         |     | A             |
|                               |                                                                                                                                                                             | OC tolerance                                       |      | $\pm 15\%$ |     |               |
| $I_{OCP\_N}$                  | Negative current limit threshold                                                                                                                                            | Valley-point current sense                         |      | -23        |     | A             |
| $I_{CLMP\_LO}$                | Clamp current at $V_{TRIP}$ clamp at lowest                                                                                                                                 | $25^\circ\text{C}$ , $V_{TRIP} = 0.1\text{ V}$     | 5.5  | 6.5        | 7.5 | A             |

### Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                 |                                                                           | TEST CONDITIONS                                                                | MIN | TYP               | MAX  | UNIT  |
|-------------------------------------------|---------------------------------------------------------------------------|--------------------------------------------------------------------------------|-----|-------------------|------|-------|
| <b>HIGH-SIDE SHORT-CIRCUIT PROTECTION</b> |                                                                           |                                                                                |     |                   |      |       |
| $I_{HSOC}$                                | High-side short circuit protection fault threshold <sup>(1)</sup>         |                                                                                |     | 45                |      | A     |
| <b>OV / UV PROTECTION</b>                 |                                                                           |                                                                                |     |                   |      |       |
| $V_{OVP}$                                 | OVP threshold voltage                                                     | OVP detect voltage                                                             | 113 | 117               | 121  | %VREF |
| $t_{OVPDLY}$                              | OVP response time <sup>(1)</sup>                                          | OVP response time with 100-mV overdrive                                        |     |                   | 1    | μs    |
| $V_{UVP}$                                 | UVP threshold voltage                                                     | UVP detect voltage                                                             | 79  | 83                | 87   | %VREF |
| $t_{UVPDLY}$                              | UVP delay <sup>(1)</sup>                                                  | UVP delay                                                                      |     |                   | 1.5  | μs    |
| $t_{HICDLY}$                              | Hiccup delay time                                                         | Regular $t_{SS}$ setting                                                       |     | $7 \times t_{SS}$ |      | ms    |
| <b>BP LDO REGULATOR</b>                   |                                                                           |                                                                                |     |                   |      |       |
| BP                                        | LDO output voltage                                                        | $V_{IN} = 12\text{ V}$ , $I_{LOAD} = 0\text{ to }10\text{ mA}$                 | 4.5 | 5                 | 5.5  | V     |
| $V_{BPUVLO}$                              | BP UVLO threshold voltage                                                 | Wakeup                                                                         |     | 3.32              |      | V     |
|                                           |                                                                           | Shutdown                                                                       |     | 3.11              |      |       |
| $V_{LDOBP}$                               | LDO low dropout voltage                                                   | $V_{IN} = 4.5\text{ V}$ , $I_{LOAD} = 30\text{ mA}$ , $T_A = 25^\circ\text{C}$ |     |                   | 365  | mV    |
| $I_{LDOMAX}$                              | LDO overcurrent limit                                                     | $V_{IN} = 12\text{ V}$ , $T_A = 25^\circ\text{C}$                              |     | 100               |      | mA    |
| <b>SYNCHRONIZATION</b>                    |                                                                           |                                                                                |     |                   |      |       |
| $V_{IH(SYNC)}$                            | High-level input voltage                                                  |                                                                                | 2   |                   |      | V     |
| $V_{IL(SYNC)}$                            | Low-level input voltage                                                   |                                                                                |     |                   | 0.8  |       |
| $t_{PSW(SYNC)}$                           | Sync input minimum pulse width                                            |                                                                                |     |                   | 100  | ns    |
| $F_{SYNC}$                                | Synchronization frequency                                                 |                                                                                | 300 |                   | 2000 | kHz   |
|                                           | Dual-phase                                                                |                                                                                | 300 |                   | 1000 |       |
| $t_{SYNC\text{ to SW}}$                   | Sync to SW delay tolerance, percentage from phase-to-phase <sup>(1)</sup> | $F_{SYNC} = 300\text{ kHz to }1\text{ MHz}$ ,                                  |     | 10%               |      |       |
| $t_{Lose\_SYNC\_delay}$                   | Delay when lose sync clock <sup>(1)</sup>                                 | $F_{SYNC} = 300\text{ kHz}$                                                    |     | 5                 |      | μs    |
| <b>THERMAL SHUTDOWN</b>                   |                                                                           |                                                                                |     |                   |      |       |
| $T_{SDN}$                                 | Built-in thermal shutdown threshold <sup>(1)</sup>                        | Shutdown temperature                                                           | 155 | 165               |      | °C    |
|                                           |                                                                           | Hysteresis                                                                     |     | 30                |      |       |

### 7.6 Typical Characteristics



Typical Characteristics (continued)

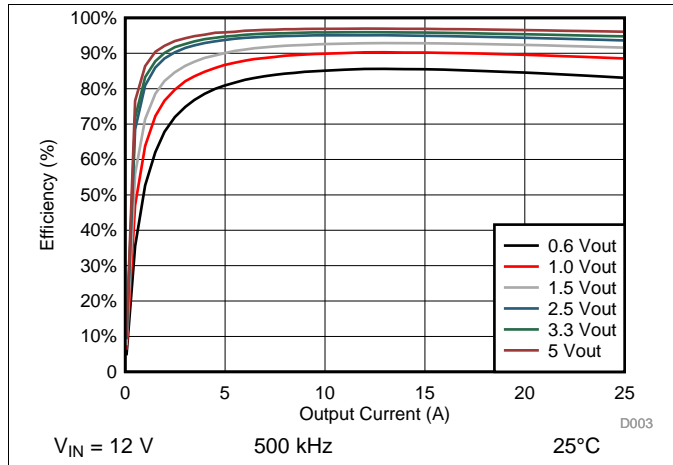


Fig 3. Efficiency vs Output Current

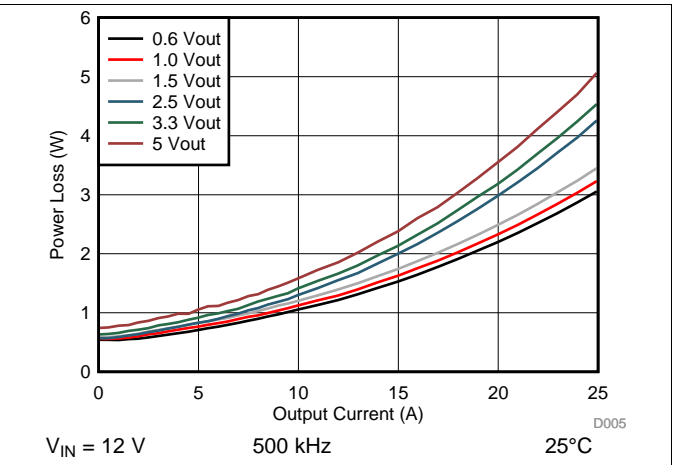


Fig 4. Power Loss vs Output Current

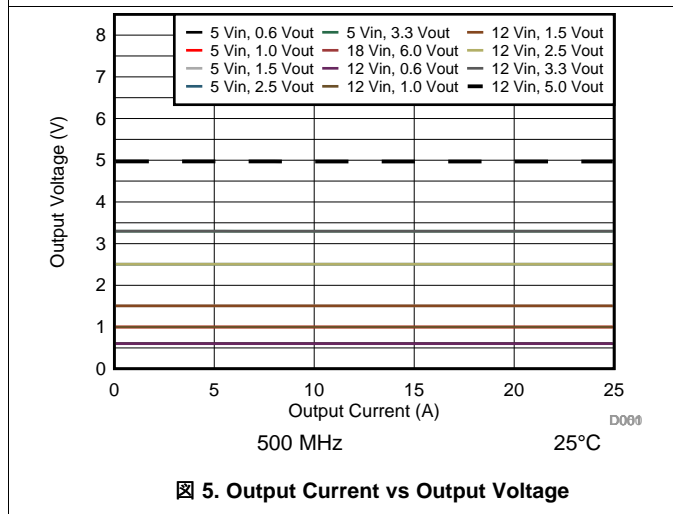


Fig 5. Output Current vs Output Voltage

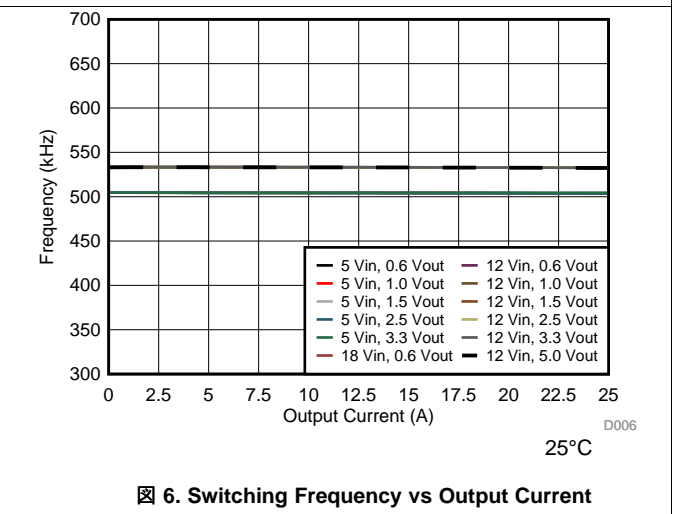


Fig 6. Switching Frequency vs Output Current

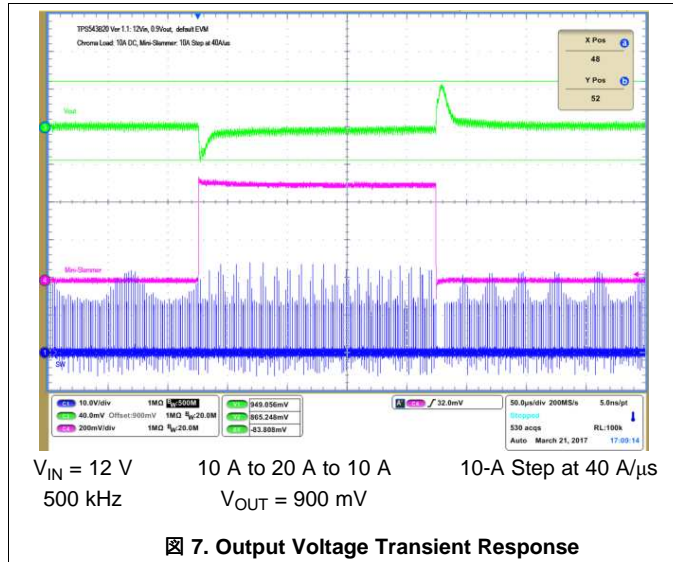


Fig 7. Output Voltage Transient Response

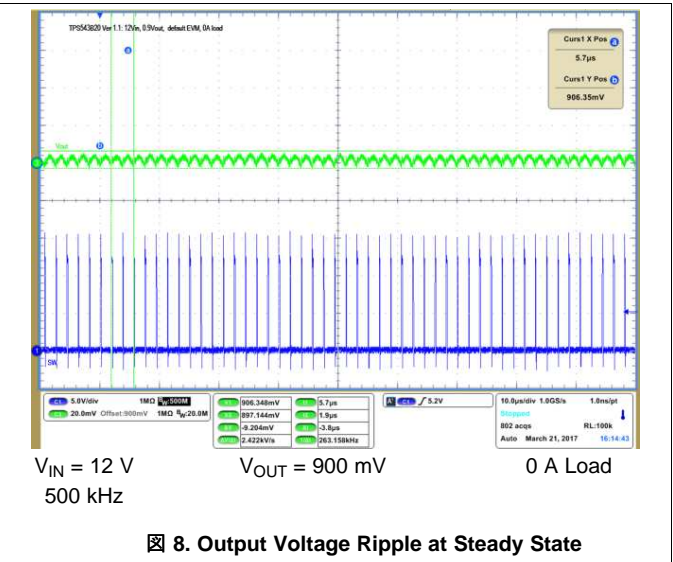
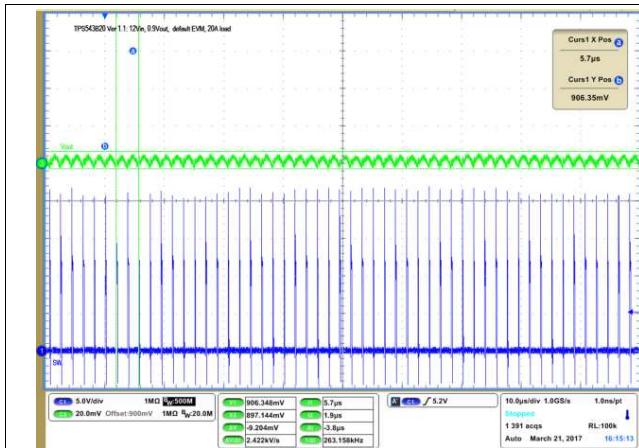


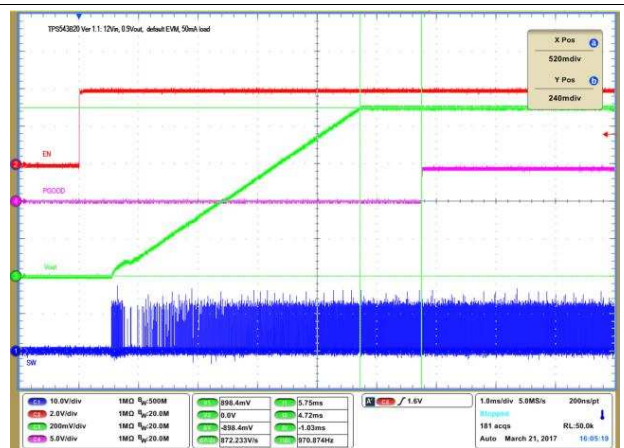
Fig 8. Output Voltage Ripple at Steady State

Typical Characteristics (continued)



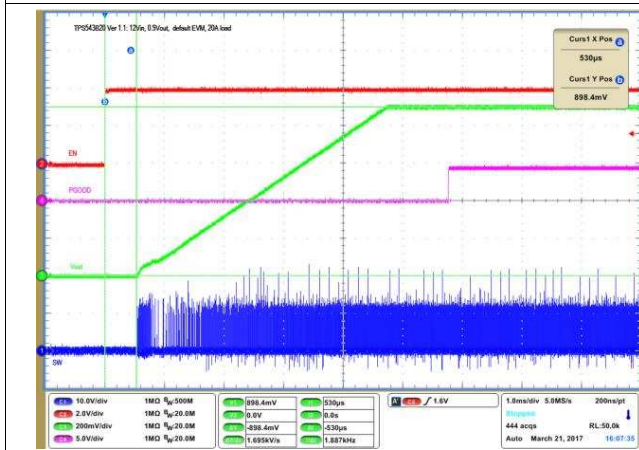
$V_{IN} = 12\text{ V}$   
 $V_{OUT} = 900\text{ mV}$   
20 A Load  
500 kHz

9. Output Voltage Ripple at Steady State



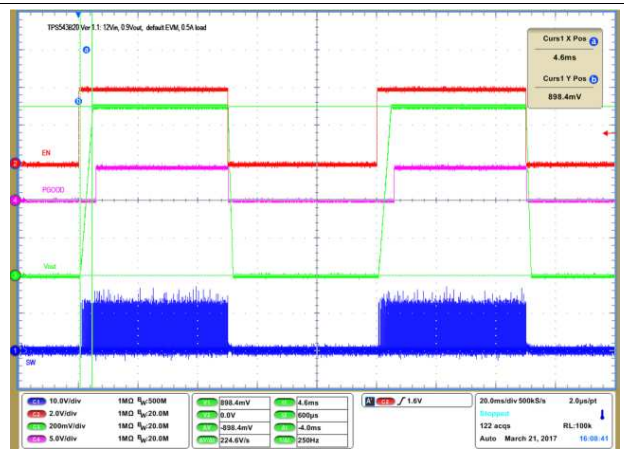
$V_{IN} = 12\text{ V}$   
 $V_{OUT} = 900\text{ mV}$   
50 mA Load  
500 kHz

10. Startup From EN



$V_{IN} = 12\text{ V}$   
 $V_{OUT} = 900\text{ mV}$   
20 A Load  
500 kHz

11. Start-Up From EN



12. Output Voltage Start-Up and Shutdown

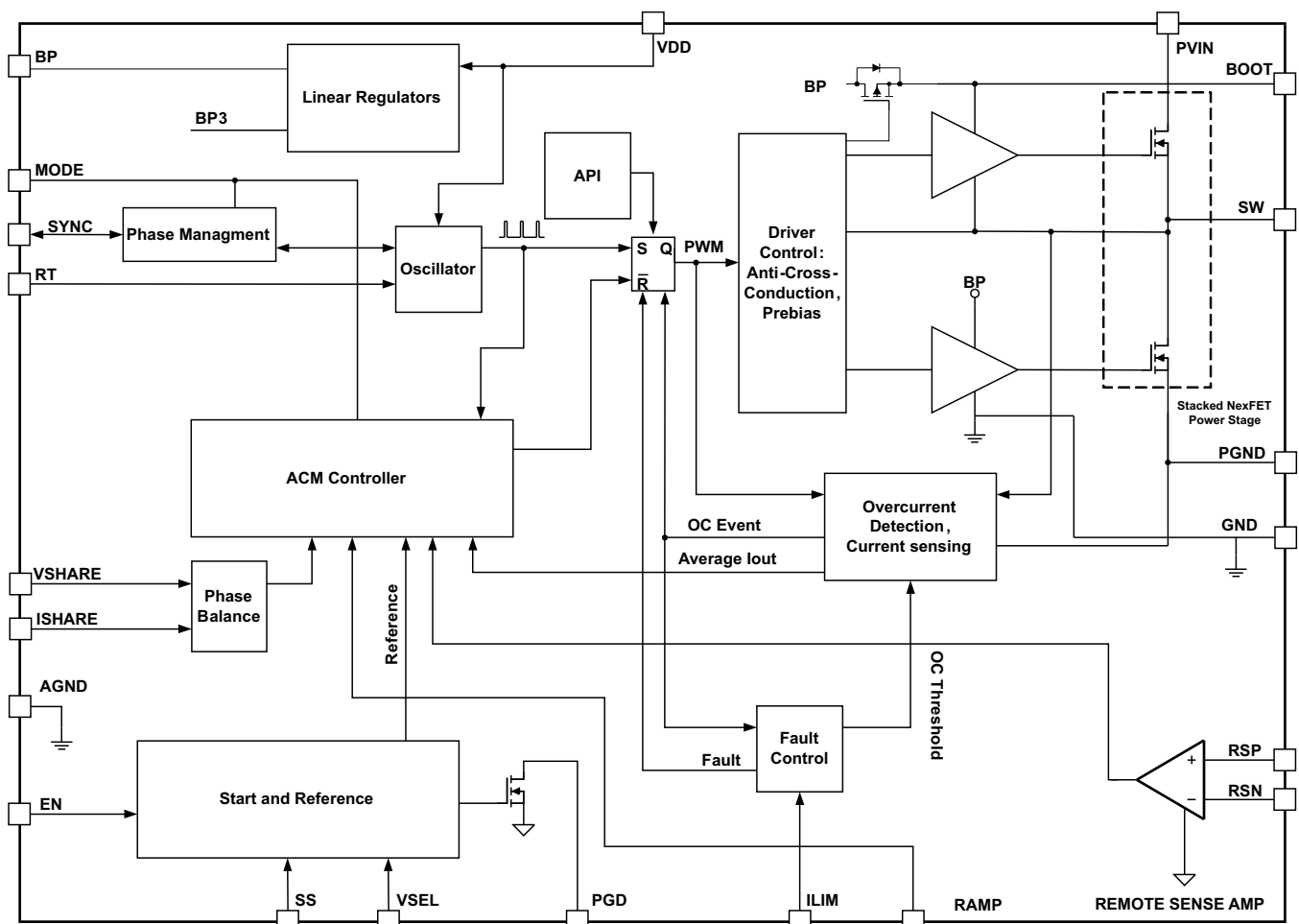
## 8 Detailed Description

### 8.1 Overview

The TPS543B20 device is 25-A, high-performance, synchronous buck converter with two integrated N-channel NexFET™ power MOSFETs. These devices implement the fixed frequency non-compensation mode control. Safe pre-bias capability eliminates concerns about damaging sensitive loads. Two TPS543B20 devices can be paralleled together to provide up to 50-A load. Current sensing for over-current protection and current sharing between devices is done by sampling a small portion of the power stage current providing accurate information independent on the device temperature.

**Advanced Current Mode (ACM)** is an emulated peak current control topology. It supports stable static and transient operation without complex external compensation design. This control architecture includes an internal ramp generation network that emulates inductor current information, enabling the use of low ESR output capacitors such as multi-layered ceramic capacitors (MLCC). The internal ramp also creates a high signal to noise ratio for good noise immunity. The TPS543B20 has 10 ramp options (see [Ramp Selections](#) for detail) to optimize internal loop for various inductor and output capacitor combinations with only a simple resistor to GND. The TPS543B20 is easy to use and allows low external component count with fast load transient response. Fixed-frequency modulation also provides ease-of-filter design to overcome EMI noise.

### 8.2 Functional Block Diagram



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### 8.3 Feature Description

The TPS543B20 device is a high-performance, integrated FET converter supporting current rating up to 25-A thermally. It integrates two N-channel NexFET™ power MOSFETs, enabling high power density and small PCB layout area. In order to limit the switch node ringing of the device, TI recommends adding a R-C snubber from the SW node to the PGND pins. *Also a 10~100nF capacitor from VIN (Pin 25) to GND (Pin 2 7) is mandatory to reduce high side FET stress.* Refer to [Layout Guidelines](#) for the detailed recommendations.

The typical on-resistance (RDS(on)) for the high-side MOSFET is 4.1 mΩ and typical on-resistance for the low-side MOSFET is 1.9 mΩ with a nominal gate voltage (VGS) of 5 V.

### 8.4 Device Functional Modes

#### 8.4.1 Soft-Start Operation

In the TPS543B20 device, the soft-start time controls the inrush current required to charge the output capacitor bank during start-up. The device offers 10 selectable soft-start options ranging from 0.5 ms to 32 ms. When the device is enabled the reference voltage ramps from 0 V to the final level defined by VSEL pin strap configuration, in a given soft-start time, which can be selected by SS pin. See [表 1](#) for details.

**表 1. SS Pin Configuration**

| SS TIME (ms) | RESISTOR VALUE (kΩ) <sup>(1)</sup> |
|--------------|------------------------------------|
| 0.5          | 0                                  |
| 1            | 8.66                               |
| 2            | 15.4                               |
| 5            | 23.7                               |
| 4            | OPEN                               |
| 8            | 34.8                               |
| 12           | 51.1                               |
| 16           | 78.7                               |
| 24           | 121                                |
| 32           | 187                                |

(1) The E48 series resistors with no more than 1% tolerance are recommended.

#### 8.4.2 Input and VDD Undervoltage Lockout (UVLO) Protection

The TPS543B20 provides fixed VIN and VDD undervoltage lockout threshold and hysteresis. The typical VIN turnon threshold is 3.2 V and hysteresis is 0.2 V. The typical VDD turnon threshold is 3.8 V and hysteresis is 0.2 V. No specific power-up sequence is required.

#### 8.4.3 Power Good and Enable

The TPS543B20 has power-good output that indicates logic high when output voltage is within the target. The power-good function is activated after soft-start has finished. When the soft-start ramp reaches 90% of setpoint, PGOOD detection function will be enabled. If the output voltage becomes within ±8% of the target value, internal comparators detect power-good state and the power good signal becomes high after a delay. If the output voltage goes outside of ±12% of the target value, the power good signal becomes low after an internal delay. The power-good output is an open-drain output and must be pulled up externally.

This part has internal pull up for EN. EN is internally pulled up to BP when EN pin is floating. EN can be pulled low through external grounding. When EN pin voltage is below its threshold, TPS543B20 enters into shutdown operation, and the minimum time for toggle EN to reset is 5 μs.

#### 8.4.4 Voltage Reference

VSEL pin strap is used to program initial boot voltage value from 0.6 V to 1.1 V by the resistor connected from VSEL to AGND. The initial boot voltage is used to program the main loop voltage reference point. VSEL voltage settings provide TI designated discrete internal reference voltages. [表 2](#) lists internal reference voltage selections.

表 2. VSEL Pin Configuration

| DEFAULT Vref (V) | RESISTOR VALUE (kΩ) <sup>(1)</sup> |
|------------------|------------------------------------|
| 0.6              | 0                                  |
| 0.7              | 8.66                               |
| 0.75             | 15.4                               |
| 0.8              | 23.7                               |
| 0.85             | 34.8                               |
| 0.9              | 51.1                               |
| 0.95             | 78.7                               |
| 1.0              | OPEN                               |
| 1.05             | 121                                |
| 1.1              | 187                                |

(1) The E48 series resistors with no worse than 1% tolerance are recommended

### 8.4.5 Prebiased Output Start-up

The TPS543B20 device prevent current from being discharged from the output during start-up, when a pre-biased output condition exists. No SW pulses occur until the internal soft-start voltage rises above the error amplifier input voltage, if the output is pre-biased. As soon as the soft-start voltage exceeds the error amplifier input, and SW pulses start, the device limits synchronous rectification after each SW pulse with a narrow on-time. The low-side MOSFET on-time slowly increases on a cycle-by-cycle basis until 128 pulses have been generated and the synchronous rectifier runs fully complementary to the high-side MOSFET. This approach prevents the sinking of current from a pre-biased output, and ensures the output voltage start-up and ramp-to regulation sequences are smooth and monotonic.

### 8.4.6 Internal Ramp Generator

Internal ramp voltage is generated from duty cycle that contains emulated inductor ripple current information and then feed it back for control loop regulation and optimization according to required output power stage, duty ratio and switching frequency. Internal ramp amplitude is set by RAMP pin by adjusting an internal ramp generation capacitor  $C_{RAMP}$ , selected by the resistor connected from MODE pin to GND. For best performance, we recommend ramp signal to be no more than 4 times of output ripple signal for all Low ESR output capacitor (MLCC) applications, or no more than 2 times larger than output ripple signal for regular ESR output capacitor (Pos-cap) applications. For design recommendation, please find the design tool at [www.ti.com/WEBENCH](http://www.ti.com/WEBENCH).

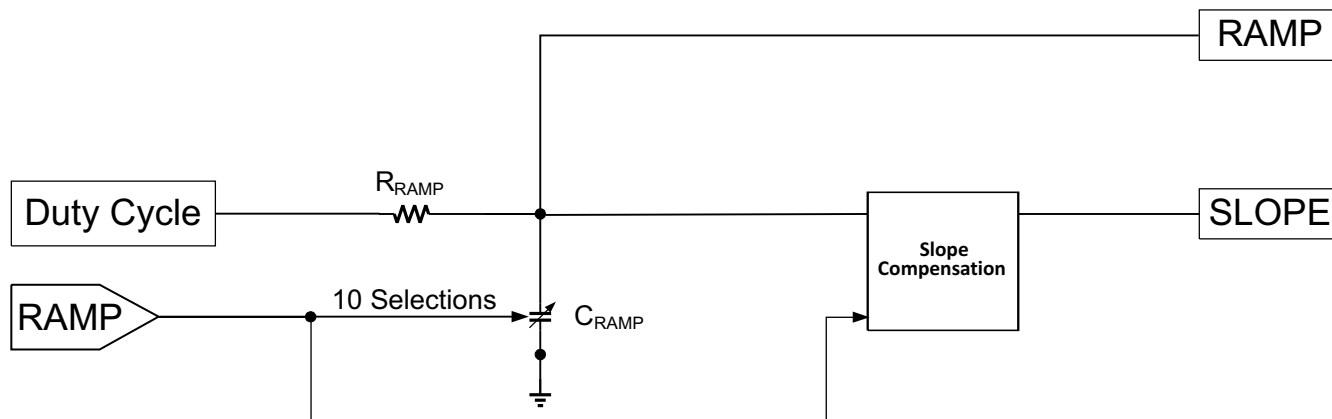


图 13. Internal Ramp Generator

### 8.4.6.1 Ramp Selections

RAMP pin sets internal ramp amplitude for the control loop. RAMP amplitude is determined by internal RC, selected by the resistor connected from MODE pin to GND, to optimize the control loop. See 表 3.

**表 3. RAMP Pin-strapping Selection**

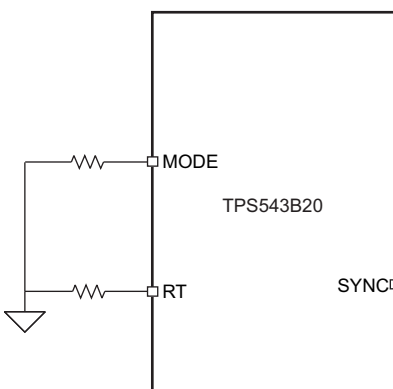
| $C_{RAMP}$ (pF) | RESISTOR VALUE (k $\Omega$ ) <sup>(1)</sup> |
|-----------------|---------------------------------------------|
| 1               | 0                                           |
| 1.42            | 8.66                                        |
| 1.94            | 15.4                                        |
| 2.58            | 23.7                                        |
| 3.43            | 34.8                                        |
| 4.57            | 51.1                                        |
| 6.23            | 78.7                                        |
| 8.91            | 121                                         |
| 14.1            | 187                                         |
| 29.1            | Open                                        |

(1) The E48 series resistors with tolerance of 1% or less are recommended.

### 8.4.7 Switching Frequency

The converter supports analog frequency selections from 300 kHz to 2 MHz, for stand alone device and sync frequency from 300 kHz to 1 MHz for stackable configuration. The RT pin also sets clock sync point (SP) for the slave device.

#### Switching Frequency Configuration for Stand-alone and Master Device in Stackable Configuration



**图 14. Stand-alone: RT Pin Sets the Switching Frequency**



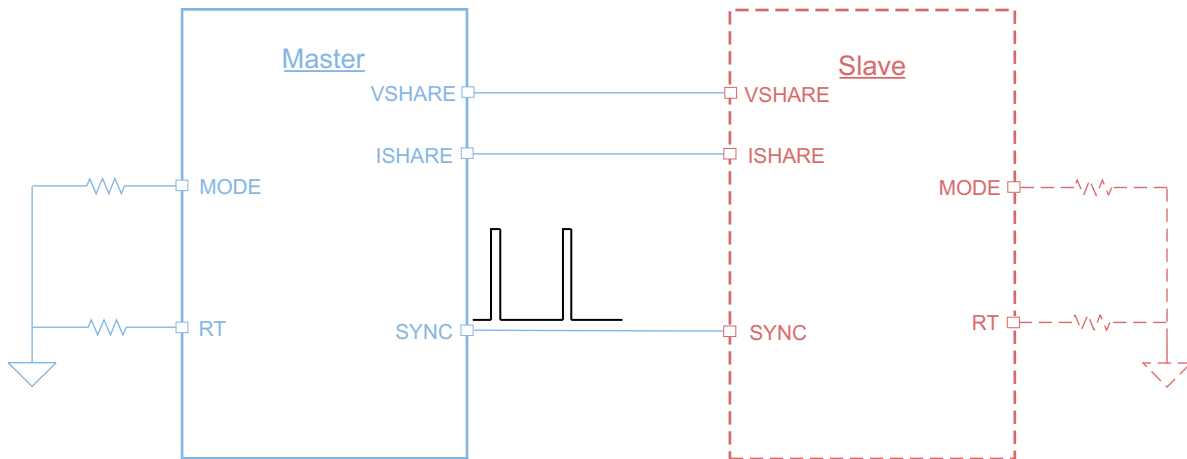


图 15. Stackable: Master (as Clock Master) RT Pin Sets Switching Frequency, and passes it to Slave

Resistor  $R_{RT}$  sets the continuous switching frequency selection by

$$R_{RT} = \frac{20 \times 10^9}{f_{SW}} - \frac{f_{SW} \times 2}{2000}$$

where

- R is the resistor from RT pin to GND, in  $\Omega$
- $f_{SW}$  is the desired switching frequency, in Hz

(1)

#### 8.4.8 Clock Sync Point Selection

The TPS543B20 device implements an unique clock sync scheme for phase interleaving during stackable configuration. The device will receive the clock through sync pin and generate sync points for another TPS543B20 device to sync to one of them to achieve phase interleaving. Sync point options can be selected through RT pin when 1) device is configured as master sync in, 2) device is configured as slave. See 表 5 for Control Mode Selection.

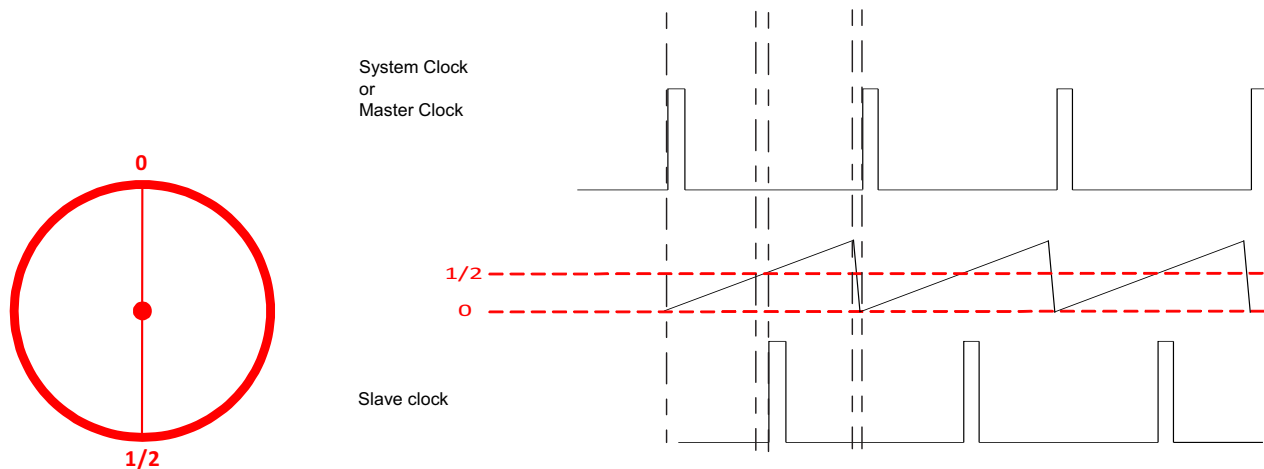


图 16. 2-Phase Stackable with 180° Clock Phase Shift

**表 4. RT Pin Sync Point Selection**

| CLOCK SYNC OPTIONS             | RESISTOR VALUE (kΩ) |
|--------------------------------|---------------------|
| <b>0 (0° Interleaving)</b>     | <b>0</b>            |
| 1/4 (90° Interleaving)         | 8.66                |
| 1/3 (120° Interleaving)        | 15.4                |
| 2/3 (240° Interleaving)        | 23.7                |
| 3/4 (270° Interleaving)        | 34.8                |
| <b>1/2 (180° Interleaving)</b> | <b>OPEN</b>         |

### 8.4.9 Synchronization and Stackable Configuration

The TPS543B20 device can synchronize to an external clock which must be equal to or higher than internal frequency setting. For stand alone device, the external clock should be applied to the SYNC pin. A sudden change in synchronization clock frequency causes an associated control loop response, resulting in an overshoot or undershoot on the output voltage.

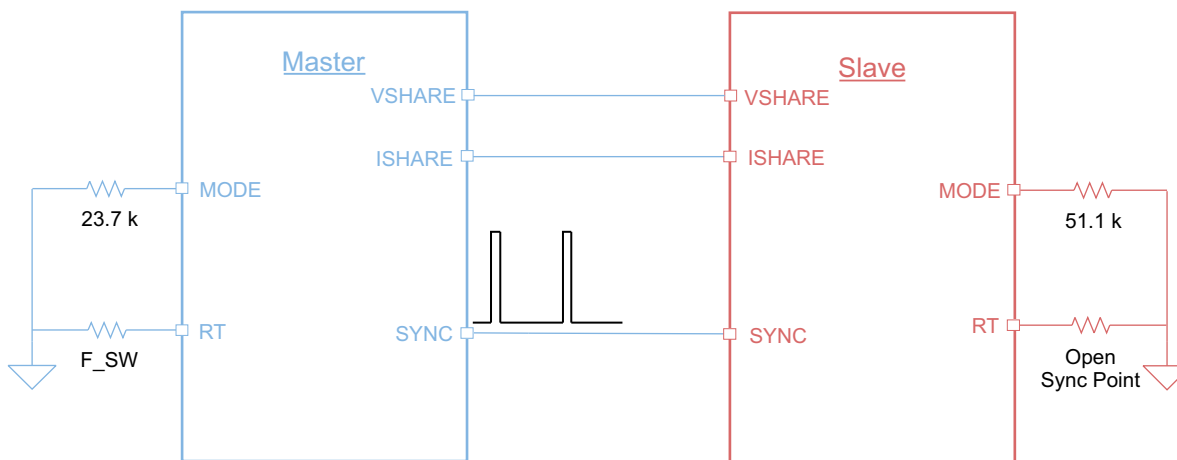
In dual phase stackable configuration:

- when there is no external system clock applied, the master device will be configured as clock master, sending out pre-set switching frequency clock to slave device through SYNC pin. Slave will receive this clock as switching clock with phase interleaving.
- when a system clock is applied, both master and slave devices will be configured as clock slave, they will sync to the external system clock as switching frequency with proper phase shift

### 8.4.10 Dual-Phase Stackable Configurations

#### 8.4.10.1 Configuration 1: Master Sync Out Clock-to-Slave

- Direct SYNC, VSHARE and ISHARE connections between Master and Slave.
- Switching frequency is set by RT pin of Master, and pass to slave through SYNC pin. SYNC pin of master will be configured as sync out by it's MODE pin.
- Slave receives clock from SYNC pin. It's RT pin determines the sync point for clock phase shift.


**图 17. 2-Phase Stackable with 180° Phase Shift: Master Sync Out Clock-to-Slave**

#### 8.4.10.2 Configuration 2: Master and Slave Sync to External System Clock

- Direct connection between external clock and SYNC pin of Master and Slave.
- Direct VSHARE and ISHARE connections between Master and Slave.
- SYNC pin of master will be configured as sync in by it's MODE pin.
- Master and Slave receive external system clock from SYNC pin. Their RT pin determine the sync point for clock phase shift.

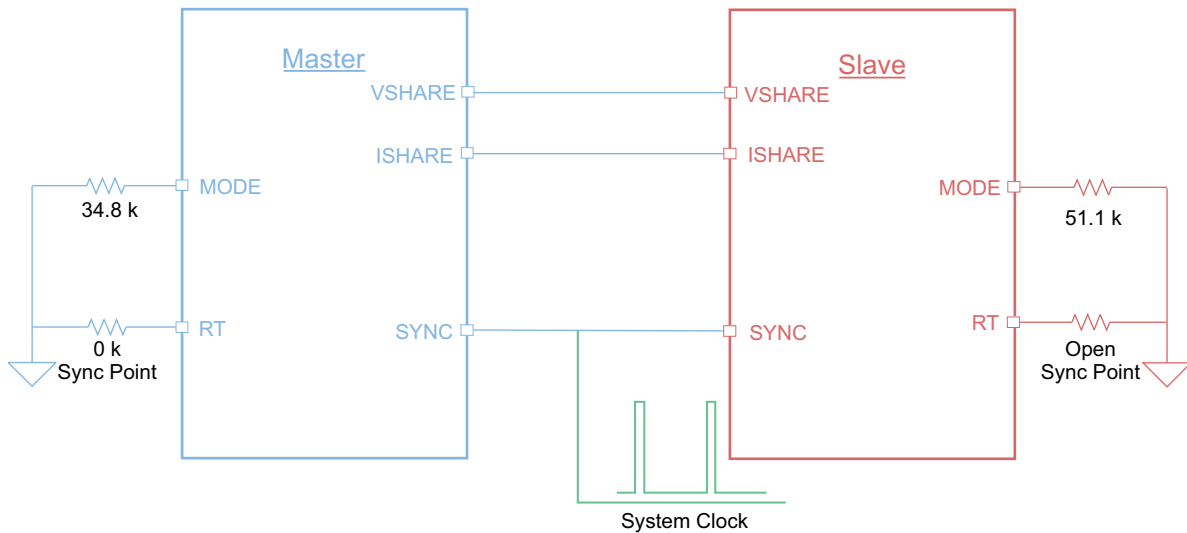


图 18. 2-Phase Stackable with 180° Phase Shift: Master and Slave Sync to External System Clock

### 8.4.11 Operation Mode

The operation mode and API/Body Brake feature is set by the MODE pin. They are selected by the resistor connected from MODE pin to GND. Mode pin sets the device to be stand-alone mode or stackable mode. In stand-alone mode, MODE pin sets the API on/off or trigger point sensitivity of API (1x stands for most sensitive and 4x stands for least sensitive). In stackable mode, the MODE pin sets the device as master or slave, as well as SYNC pin function (sync in or sync out) of the master device.

表 5. MODE Pin-Strapping Selection

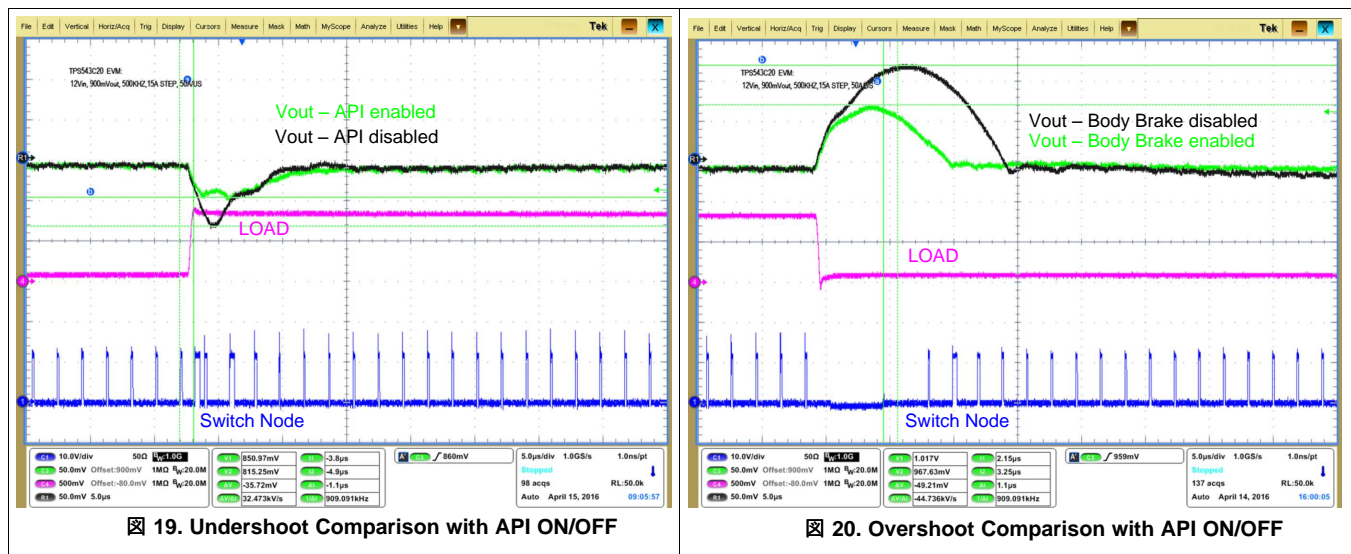
| CONTROL MODE SELECTION        | API/BODY BRAKE                             | RESISTOR VALUE (kΩ) and API/BB Threshold <sup>(1)</sup> | NOTE                                                                                                              |
|-------------------------------|--------------------------------------------|---------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------|
| Standalone API/body brake     | API OFF<br>BB OFF                          | Open                                                    | <ul style="list-style-type: none"> <li>• Sync pin to receive clock</li> <li>• RT pin to set frequency</li> </ul>  |
|                               | API ON<br>BB OFF                           | 15.4, API = 35 mV                                       |                                                                                                                   |
|                               | API ON<br>BB ON<br>(API Threshold Setting) | 121, API = 15 mV, BB = 30 mV                            |                                                                                                                   |
|                               |                                            | 187, API = 25 mV, BB = 30 mV                            |                                                                                                                   |
|                               |                                            | 8.66, API = 35 mV, BB = 30 mV                           |                                                                                                                   |
| 78.7, API = 45 mV, BB = 30 mV |                                            |                                                         |                                                                                                                   |
| (Master sync out)             | API OFF<br>BB OFF                          | 23.7                                                    | <ul style="list-style-type: none"> <li>• Sync pin to send out clock</li> <li>• RT pin to set frequency</li> </ul> |
| (Master sync in)              |                                            | 34.8                                                    | <ul style="list-style-type: none"> <li>• Sync pin to receive clock</li> <li>• RT pin to set sync point</li> </ul> |
| (Slave Sync In)               |                                            | 51.1                                                    | <ul style="list-style-type: none"> <li>• Sync pin to receive clock</li> <li>• RT pin to set sync point</li> </ul> |

(1) The E48 series resistors with tolerance of 1% or less are recommended.

### 8.4.12 API/BODY Brake

TPS543B20 is a true fixed frequency converter. The major limitation for any fixed frequency converter is that during transient load step up, the converter needs to wait for the next clock cycle to response to the load change, depending on loop bandwidth design and the timing of load transient, this delay time could cause additional output voltage drop. TPS543B20 implements a special circuitry to improve transient performance. During load step up, the converter senses both the speed and the amplitude of the output voltage change, if the output voltage change is fast and big enough, the converter will issue an additional PWM pulse before the next available clock cycle to stop output voltage from further dropping, thus reducing the undershoot voltage.

During load step down, TPS543B20 implements a body brake function, that turns off both high-side and lowside FET, and allows power to dissipate through the low-side body diode, reducing overshoot. This approach is very effective while having some impact on efficiency during transient. See [Figure 19](#) and [Figure 20](#).



### 8.4.13 Sense and Overcurrent Protection

#### 8.4.13.1 Low-Side MOSFET Overcurrent Protection

The TPS543B20 utilizes ILIM pin to set the OCP level. The ILIM pin should be connected to AGND through the ILIM voltage setting resistor, RILIM. The ILIM terminal sources IILIM current, which is around 11.2  $\mu\text{A}$  typically at room temperature, and the ILIM level is set to the OCP ILIM voltage VILIM as shown in [Equation 2](#). In order to provide both good accuracy and cost effective solution, TPS543B20 supports temperature compensated MOSFET  $R_{DS(on)}$  sensing.

$$V_{ILIM} (\text{mV}) = R_{ILIM} (\text{k}\Omega) \times I_{ILIM} (\mu\text{A})$$

Consider  $R_{DS(on)}$  variation vs VDD in calculation (2)

Also, TPS543B20 performs both positive and fixed negative inductor current limiting.

The inductor current is monitored by the voltage between GND pin and SW pin during the OFF time. ILIM has 1200 ppm/ $^{\circ}\text{C}$  temperature slope to compensate the temperature dependency of the  $R_{DS(on)}$ . The GND pin is used as the positive current sensing node.

The device has cycle-by-cycle over-current limiting control. The inductor current is monitored during the OFF state and the controller maintains the OFF state during the period that the inductor current is larger than the overcurrent ILIM level.  $V_{ILIM}$  sets the Peak level of the inductor current. Thus, the load current at the overcurrent threshold,  $I_{OCP}$ , can be calculated as shown in [Equation 3](#).

$$I_{OCP} = V_{ILIM} / (14 \times R_{DS(on)}) - I_{IND(ripple)} / 2$$

$$= \frac{V_{ILIM}}{14 \times R_{DS(on)}} - \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

where

- $R_{DS(on)}$  is the on-resistance of the low-side MOSFET. (3)

[Equation 3](#) is valid for  $V_{DD} \geq 5 \text{ V}$ . Use 1.58 m $\Omega$  for  $R_{DS(on)}$  in calculation, which is the pure on-resistance for current sense.

If an overcurrent event is detected in a given switching cycle, the device increments an overcurrent counter. When the device detects three consecutive overcurrent (either high-side or low-side) events, the converter responds, entering continuous restart hiccup. In continuous hiccup mode, the device implements a 7 soft-start cycle timeout, followed by a normal soft-start attempt. When the overcurrent fault clears, normal operation resumes; otherwise, the device detects overcurrent and the process repeats.

#### **8.4.13.2 High-Side MOSFET Overcurrent Protection**

The device also implements a fixed high-side MOSFET overcurrent protection to limit peak current, and prevent inductor saturation in the event of a short circuit. The device detects an overcurrent event by sensing the voltage drop across the high-side MOSFET during ON state. If the peak current reaches the IHOSC level on any given cycle, the cycle terminates to prevent the current from increasing any further. High-side MOSFET overcurrent events are counted. If the devices detect three consecutive overcurrent events (high-side or low-side), the converter responds by entering continuous restart hiccup.

#### **8.4.14 Output Overvoltage and Undervoltage Protection**

The device includes both output overvoltage protection and output undervoltage protection capability. The devices compare the RSP pin voltage to internal selectable pre-set voltages. If the RSP voltage with respect to RSN voltage rises above the output overvoltage protection threshold, the device terminates normal switching and turns on the low-side MOSFET to discharge the output capacitor and prevent further increases in the output voltage. Then the device enters continuous restart hiccup.

If the RSP pin voltage falls below the undervoltage protection level, after soft-start has completed, the device terminates normal switching and forces both the high-side and low-side MOSFETs off, then enters hiccup time-out delay prior to restart.

#### **8.4.15 Overtemperature Protection**

An internal temperature sensor protects the devices from thermal runaway. The internal thermal shutdown threshold,  $T_{SD}$ , is fixed at 165°C typical. When the devices sense a temperature above  $T_{SD}$ , power conversion stops until the sensed junction temperature falls by the thermal shutdown hysteresis amount; then, the device starts up again.

#### **8.4.16 RSP/RSN Remote Sense Function**

RSP and RSN pins are used for remote sensing purpose. In the case where feedback resistors are required for output voltage programming, the RSP pin should be connected to the mid-point of the resistor divider and the RSN pin should always be connected to the load return.

In the case where feedback resistors are not required as when the VSEL programs the output voltage set point, the RSP pin should be connected to the positive sensing point of the load and the RSN pin should always be connected to the load return. RSP and RSN pins are extremely high-impedance input terminals of the true differential remote sense amplifier. The feedback resistor divider should use resistor values much less than 100 k $\Omega$ . A simple rule of thumb is to use a 10-k $\Omega$  lower divider resistor and then size the upper resistor to achieve the desired ratio.

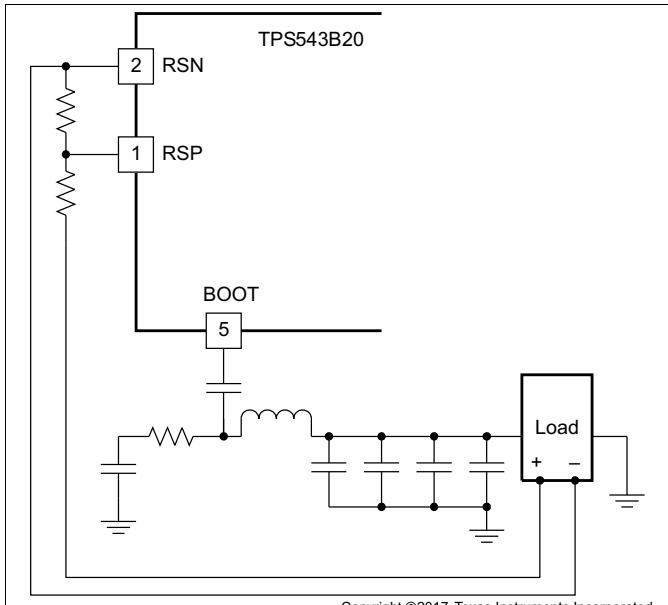


Figure 21. Remote Sensing With Feedback Resistors

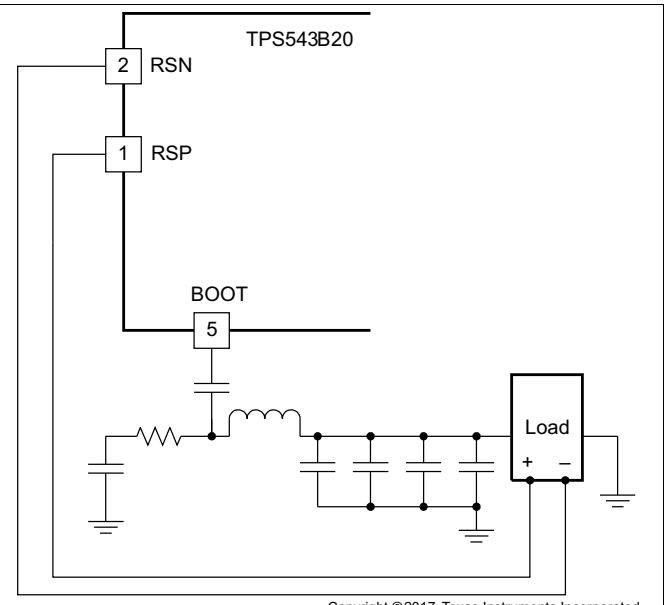


Figure 22. Remote Sensing Without Feedback Resistors

### 8.4.17 Current Sharing

When devices operate in dual-phase stackable application, a current sharing loop maintains the current balance between devices. Both devices share the same internal control voltage through VSHARE pin. The sensed current in each phase is compared first in a current share block by connecting ISHARE pin of each device, then the error current is added into the internal loop. The resulting voltage is compared with the PWM ramp to generate the PWM pulse.

### 8.4.18 Loss of Synchronization

During sync clock condition, each individual converter will continuously compare current falling edge and previous falling edge, if current falling edge exceeded a 1us delay versus previous pulse, converter will declare a lost sync fault, and response by pulling down ISHARE to shut down all phases.

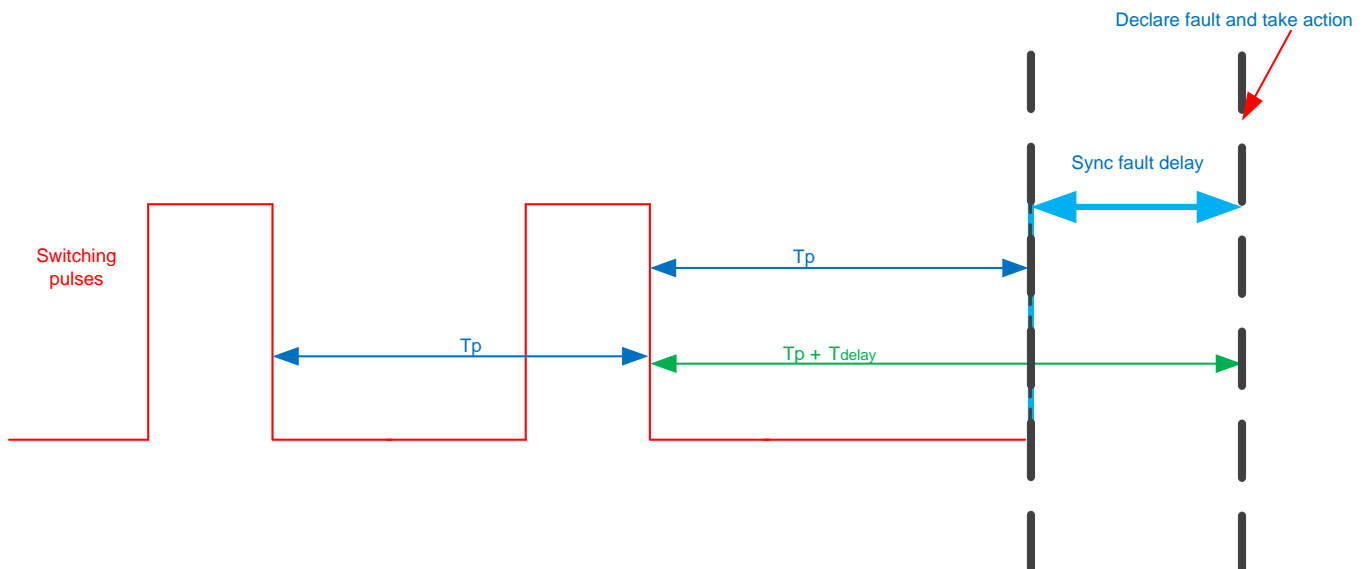


Figure 23. Switching Response When Sync Clock Lost

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TPS543B20 device is a highly-integrated synchronous step-down DC/DC converter. The device is used to convert a higher DC input voltage to a lower DC output voltage, with a maximum output current of 25 A. Use the following design procedure to select key component values for this device.

### 9.2 Typical Application: TPS543B20 Stand-alone Device

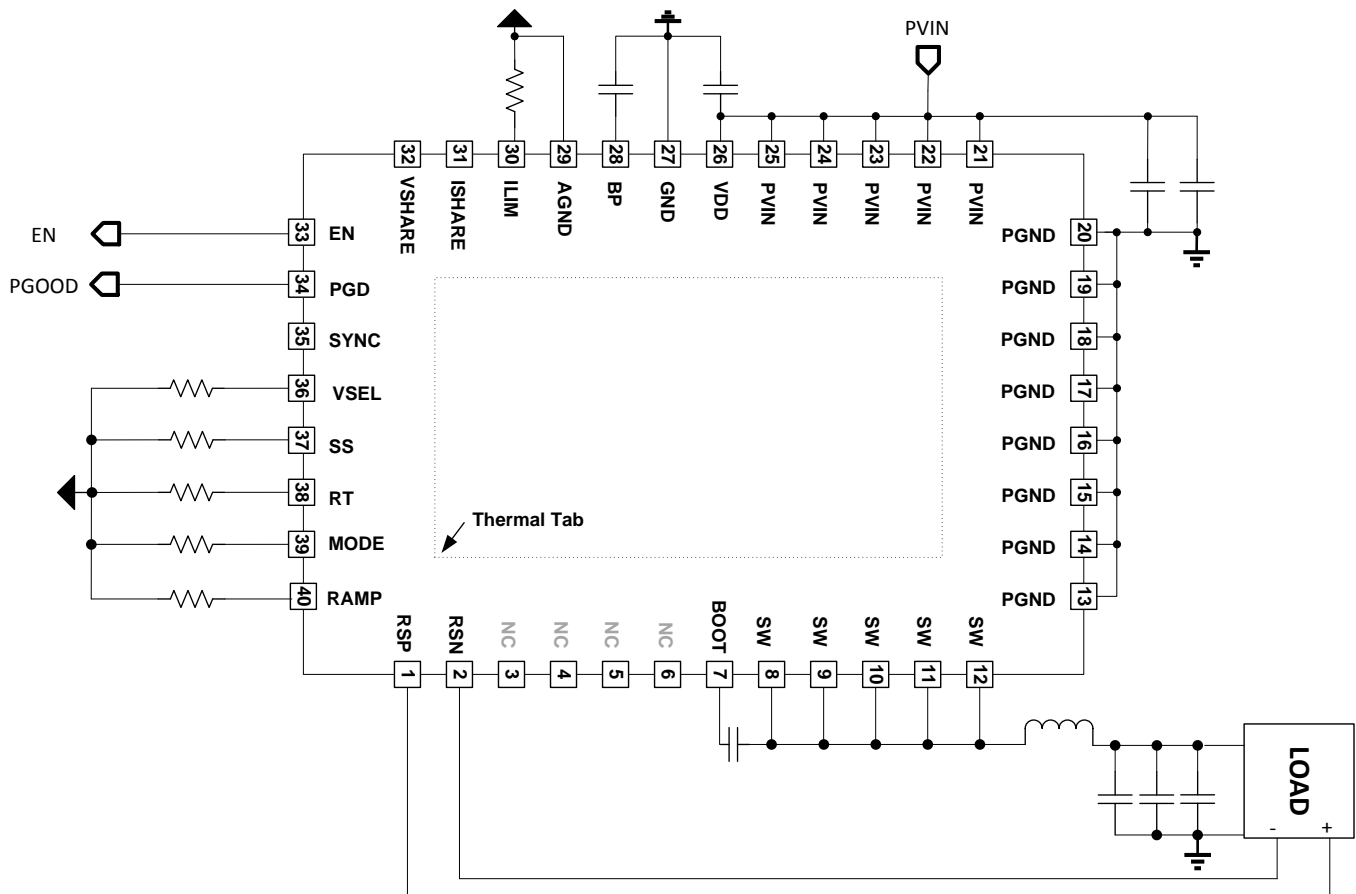


Figure 24. 4.5-V to 19-V Input, 1-V Output, 25-A Converter

## 9.2.1 Design Requirements

For this design example, use the input parameters shown in [Table 6](#).

**Table 6. Design Example Specifications**

| PARAMETER        |                                       | TEST CONDITION                                                     | MIN | TYP | MAX  | UNIT |
|------------------|---------------------------------------|--------------------------------------------------------------------|-----|-----|------|------|
| $V_{IN}$         | Input voltage                         |                                                                    | 4   | 12  | 19   | V    |
| $V_{IN(ripple)}$ | Input ripple voltage                  | $I_{OUT} = 25\text{ A}$                                            |     |     | 0.4  | V    |
| $V_{OUT}$        | Output voltage                        |                                                                    |     | 0.9 |      | V    |
|                  | Line regulation                       | $5\text{ V} \leq V_{IN} \leq 19\text{ V}$                          |     |     | 0.5% |      |
|                  | Load regulation                       | $0\text{ V} \leq I_{OUT} \leq 25\text{ A}$                         |     |     | 0.5% |      |
| $V_{PP}$         | Output ripple voltage                 | $I_{OUT} = 25\text{ A}$                                            |     | 20  |      | mV   |
| $V_{OVER}$       | Transient response overshoot          | $I_{STEP} = 10\text{ A}$                                           |     | 50  |      | mV   |
| $V_{UNDER}$      | Transient response undershoot         | $I_{STEP} = 10\text{ A}$                                           |     | 50  |      | mV   |
| $I_{OUT}$        | Output current                        | $5\text{ V} \leq V_{IN} \leq 19\text{ V}$                          |     | 20  | 25   | A    |
| $t_{SS}$         | Soft-start time                       | $V_{IN} = 12\text{ V}$                                             |     | 4   |      | ms   |
| $I_{OC}$         | Overcurrent trip point <sup>(1)</sup> |                                                                    |     | 30  |      | A    |
| $\eta$           | Peak efficiency                       | $I_{OUT} = 10\text{ A}, V_{IN} = 12\text{ V}, V_{DD} = 5\text{ V}$ |     | 90% |      |      |
| $f_{SW}$         | Switching frequency                   |                                                                    | 300 | 500 | 700  | kHz  |

(1) DC overcurrent level

## 9.2.2 Detailed Design Procedure

### 9.2.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the TPS543B20 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ( $V_{IN}$ ), output voltage ( $V_{OUT}$ ), and output current ( $I_{OUT}$ ) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at [www.ti.com/WEBENCH](http://www.ti.com/WEBENCH).

### 9.2.2.2 Switching Frequency Selection

Select a switching frequency for the TPS543B20. There is a trade off between higher and lower switching frequencies. Higher switching frequencies may produce smaller solution size using lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the higher switching frequency causes extra switching losses, which decrease efficiency and impact thermal performance. In this design, a moderate switching frequency of 500 kHz achieves both a small solution size and a high efficiency operation is selected. The device supports continuous switching frequency programming; see [Equation 4](#). additional considerations (internal ramp compensation) other than switching frequency need to be included.



$$R_{RT} = \frac{20 \times 10^9}{500 \times 10^3} - 2 \times \frac{500 \times 10^3}{2000} = 39.5 \text{ k}\Omega \quad (4)$$

In this case, a standard resistor value of 40.2 kΩ is selected.

### 9.2.2.3 Inductor Selection

To calculate the value of the output inductor (L), use . The coefficient  $K_{IND}$  represents the amount of inductor-ripple current relative to the maximum output current. The output capacitor filters the inductor-ripple current. Therefore, selecting a high inductor-ripple current impacts the selection of the output capacitor because the output capacitor must have a ripple-current rating equal to or greater than the inductor-ripple current. Generally, the  $K_{IND}$  should be kept between 0.1 and 0.3 for balanced performance. Using this target ripple current, the required inductor size can be calculated as shown in [Equation 5](#).

$$L = \frac{V_{OUT}}{V_{IN} \times f_{SW}} - \frac{V_{IN} - V_{OUT}}{I_{OUT} \times K_{IND}} = \frac{0.9 \text{ V} \times (12 \text{ V} - 0.9 \text{ V})}{12 \text{ V} \times 500 \text{ kHz} \times 25 \text{ A} \times 0.15} = 444 \text{ nH} \quad (5)$$

A standard inductor value of 470 nH is selected. For this application, Würth 744309047 was used from the web-orderable EVM.

### 9.2.2.4 Input Capacitor Selection

The TPS543B20 devices require a high-quality, ceramic, type X5R or X7R, input decoupling capacitor with a value of at least 1 μF of effective capacitance on the VDD pin, relative to AGND. The power stage input decoupling capacitance (effective capacitance at the PVIN and PGND pins) must be sufficient to supply the high switching currents demanded when the high-side MOSFET switches on, while providing minimal input voltage ripple as a result. This effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple to the device during full load. The input ripple current can be calculated using [Equation 6](#).

$$I_{CIN(rms)} = I_{OUT(max)} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \frac{(V_{IN} - V_{OUT})}{V_{IN}}} = 6.6 \text{ Arms} \quad (6)$$

The minimum input capacitance and ESR values for a given input voltage ripple specification,  $V_{IN(ripple)}$ , are shown in [Equation 7](#) and [Equation 8](#). The input ripple is composed of a capacitive portion,  $V_{RIPPLE(cap)}$ , and a resistive portion,  $V_{RIPPLE(esr)}$ .

$$C_{IN(min)} = \frac{I_{OUT(max)} \times V_{OUT}}{V_{RIPPLE(cap)} \times V_{IN(max)} \times f_{SW}} = 38.5 \text{ }\mu\text{F} \quad (7)$$

$$ESR_{CIN(max)} = \frac{V_{RIPPLE(ESR)}}{I_{OUT(max)} + \left(\frac{I_{RIPPLE}}{2}\right)} = 7 \text{ m}\Omega \quad (8)$$

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The input capacitor must also be selected with the DC bias taken into account. For this example design, a ceramic capacitor with at least a 25-V voltage rating is required to support the maximum input voltage. For this design, allow 0.1-V input ripple for  $V_{RIPPLE(cap)}$ , and 0.3-V input ripple for  $V_{RIPPLE(esr)}$ . Using [Equation 7](#) and [Equation 8](#), the minimum input capacitance for this design is 38.5 μF, and the maximum ESR is 9.4 mΩ. For this example, four 22-μF, 25-V ceramic capacitors and one additional 100-μF, 25-V low-ESR polymer capacitors in parallel were selected for the power stage.

### 9.2.2.5 Bootstrap Capacitor Selection

A ceramic capacitor with a value of 0.1 μF must be connected between the BOOT and SW pins for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. Use a capacitor with a voltage rating of 25 V or higher.

### 9.2.2.6 BP Pin

Bypass the BP pin to GND with 4.7- $\mu$ F of capacitance. In order for the regulator to function properly, it is important that these capacitors be localized to the TPS543B20, with low-impedance return paths. See [Power Good and Enable](#) section for more information.

### 9.2.2.7 R-C Snubber and VIN Pin High-Frequency Bypass

Though it is possible to operate the TPS543B20 within absolute maximum ratings without ringing reduction techniques, some designs may require external components to further reduce ringing levels. This example uses two approaches: a high frequency power stage bypass capacitor on the VIN pins, and an R-C snubber between the SW area and GND.

The high-frequency VIN bypass capacitor is a lossless ringing reduction technique which helps minimize the outboard parasitic inductances in the power stage, which store energy during the low-side MOSFET on-time, and discharge once the high-side MOSFET is turned on. For this example twin 2.2-nF, 25-V, 0603-sized high-frequency capacitors are used. The placement of these capacitors is critical to its effectiveness.

Additionally, an R-C snubber circuit is added to this example. To balance efficiency and spike levels, a 1-nF capacitor and a 1- $\Omega$  resistor are chosen. In this example a 0805-sized resistor is chosen, which is rated for 0.125 W, nearly twice the estimated power dissipation. See [SLUP100](#) for more information about snubber circuits.

### 9.2.2.8 Output Capacitor Selection

There are three primary considerations for selecting the value of the output capacitor. The output capacitor affects three criteria:

- Stability
- Regulator response to a change in load current or load transient
- Output voltage ripple

These three considerations are important when designing regulators that must operate where the electrical conditions are unpredictable. The output capacitance needs to be selected based on the most stringent of these three criteria.

#### 9.2.2.8.1 Response to a Load Transient

The output capacitance must supply the load with the required current when current is not immediately provided by the regulator. When the output capacitor supplies load current, the impedance of the capacitor greatly affects the magnitude of voltage deviation (such as undershoot and overshoot) during the transient.

Use [Equation 9](#) and [Equation 10](#) to estimate the amount of capacitance needed for a given dynamic load step and release.

---

#### NOTE

There are other factors that can impact the amount of output capacitance for a specific design, such as ripple and stability.

---

$$C_{OUT(min\_under)} = \frac{L \times \Delta I_{LOAD(max)}^2}{2 \times \Delta V_{LOAD(INSERT)} \times (V_{IN} - V_{VOUT})} + \frac{\Delta I_{LOAD(max)} \times (1-D) \times t_{SW}}{\Delta V_{LOAD(INSERT)}} \quad (9)$$

$$C_{OUT(min\_over)} = \frac{L_{OUT} \times (\Delta I_{LOAD(max)})^2}{2 \times \Delta V_{LOAD(release)} \times V_{OUT}}$$

where

- $C_{OUT(min\_under)}$  is the minimum output capacitance to meet the undershoot requirement
  - $C_{OUT(min\_over)}$  is the minimum output capacitance to meet the overshoot requirement
  - D is the duty cycle
  - L is the output inductance value (0.47  $\mu$ H)
  - $\Delta I_{LOAD(max)}$  is the maximum transient step (10 A)
  - $V_{OUT}$  is the output voltage value (900 mV)
  - $t_{SW}$  is the switching period (2.0  $\mu$ s)
  - $V_{IN}$  is the minimum input voltage for the design (12 V)
  - $\Delta V_{LOAD(insert)}$  is the undershoot requirement (50 mV)
  - $\Delta V_{LOAD(release)}$  is the overshoot requirement (50 mV) (10)
- This example uses a combination of POSCAP and MLCC capacitors to meet the overshoot requirement.
    - POSCAP bank #1: 2 x 330  $\mu$ F, 2.5 V, 3 m $\Omega$  per capacitor
    - MLCC bank #2: 3 x 100  $\mu$ F, 6.3 V, 1 m $\Omega$  per capacitor

#### 9.2.2.8.2 Ramp Selection Design to Ensure Stability

Certain criteria is recommended for TPS543B20 to achieve optimized loop stability, bandwidth and switching jitter performance. As a rule of thumb, the internal ramp voltage should be 2~4 times bigger than the output capacitor ripple (capacitive ripple only). TPS543B20 is defined to be ease-of-use, for most applications, TI recommends ramp resistor to be 187 k $\Omega$  to achieve the optimized jitter and loop response. For detailed design procedure, see the WEBENCH® Power Designer.

9.2.3 Application Curves

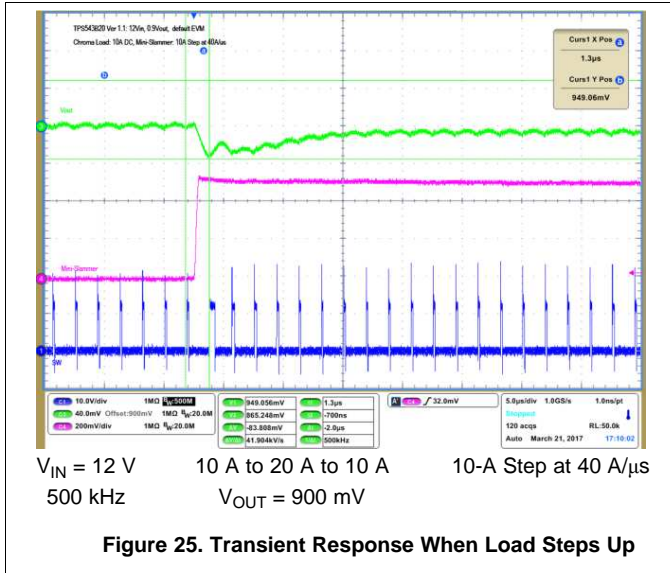


Figure 25. Transient Response When Load Steps Up

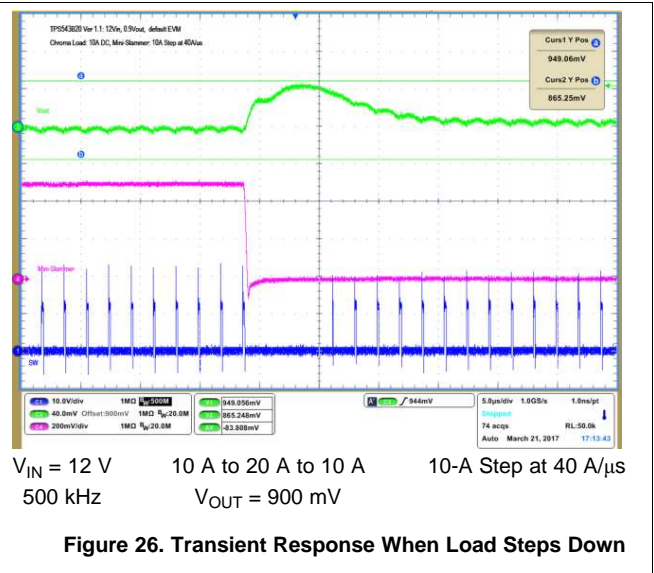


Figure 26. Transient Response When Load Steps Down

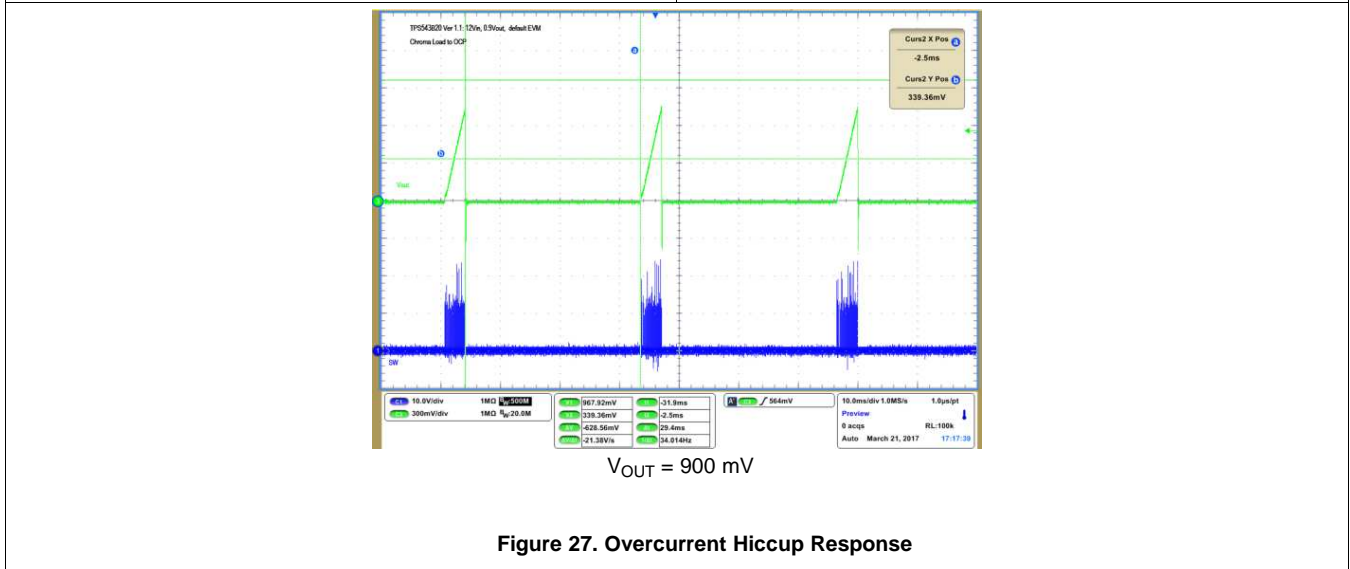


Figure 27. Overcurrent Hiccup Response

### 9.3 System Example

#### 9.3.1 Two-Phase Stackable

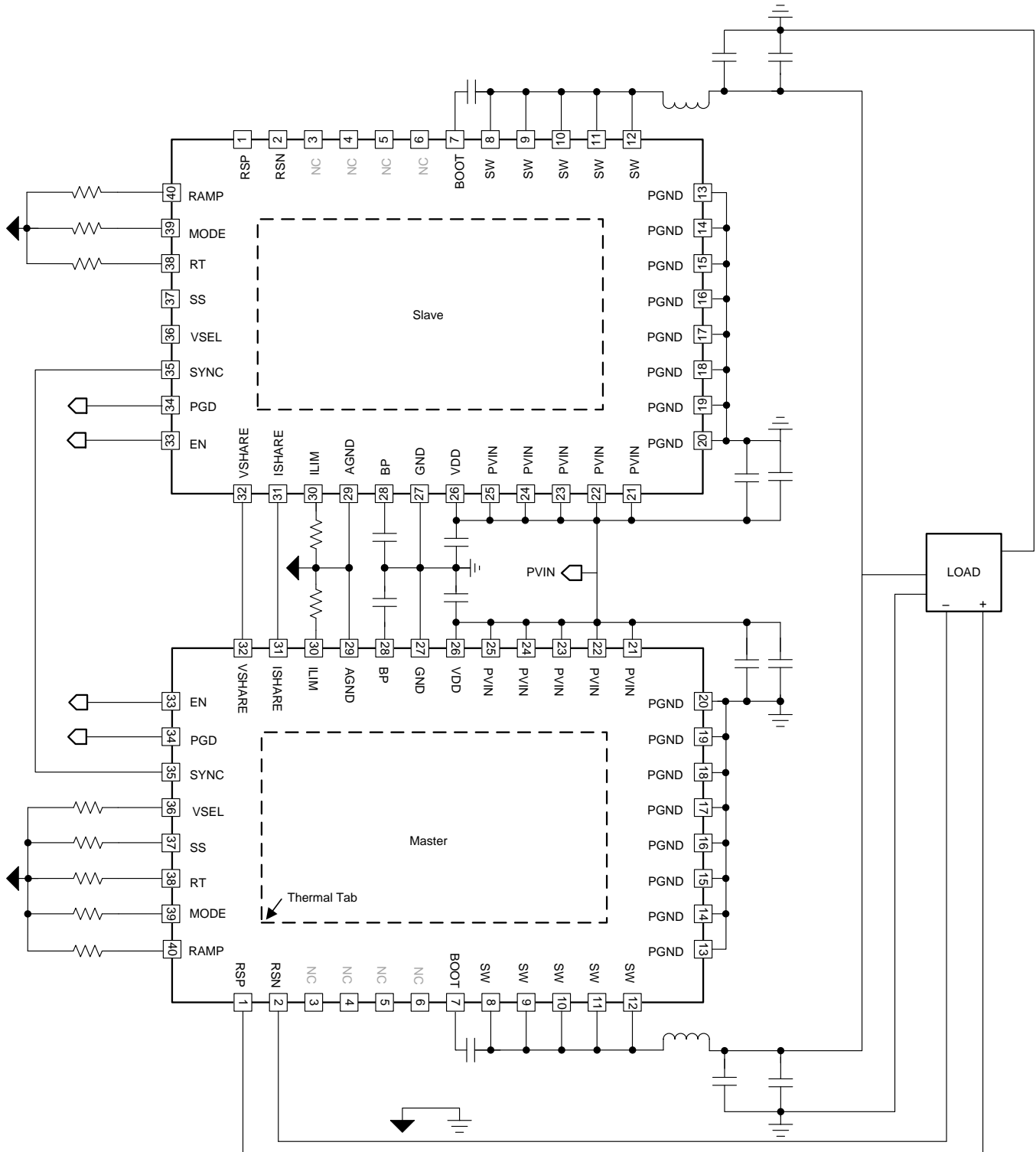


Figure 28. 2-Phase Stackable

See [Synchronization and Stackable Configuration](#) section.

System Example (continued)

9.3.1.1 Application Curves

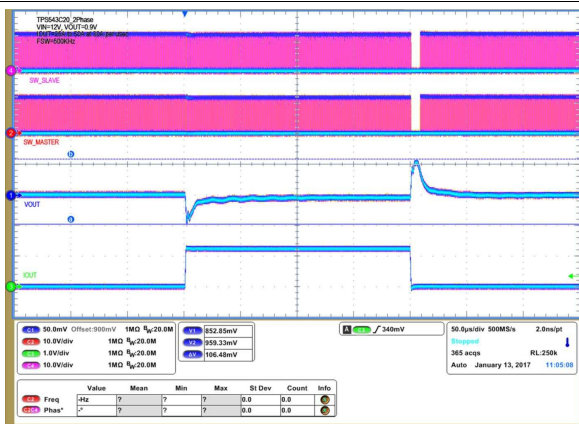


Figure 29. Transient Response of 0.9-V Output at 12 VIN, Transient is 25 A to 50 A, Step is 25 A at 30 A/μs

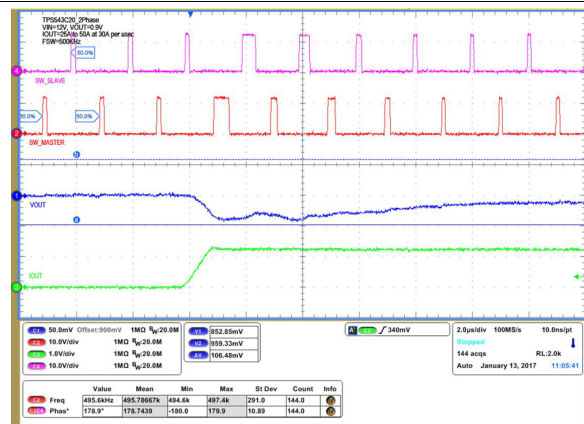


Figure 30. Transient Response of 25-A to 50-A Load at 30 A/μs Rise

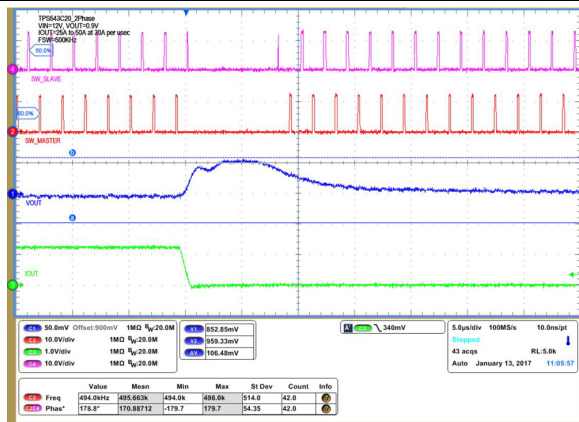


Figure 31. Transient Response of 50-A to 25-A Load at 30 A/μs Fall

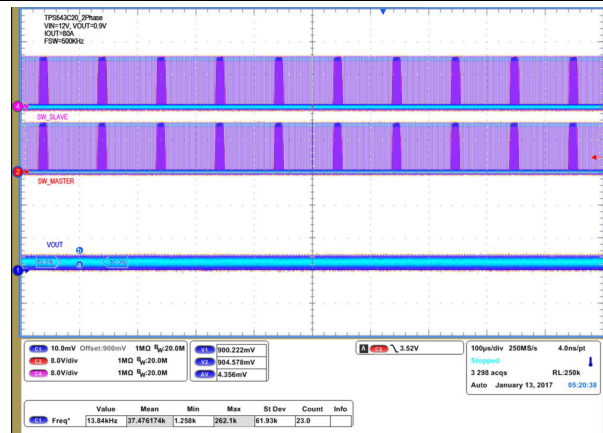


Figure 32. Output Ripple and SW Node of 0.9-V Output at 12 VIN, 50-A Output

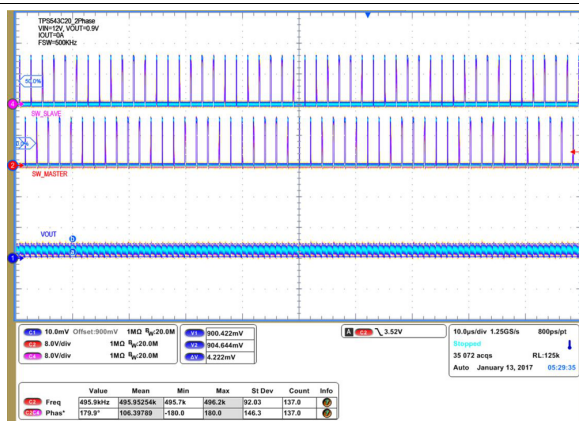


Figure 33. Output Ripple and SW Node of 0.9-V Output at 12 VIN, 0-A Output

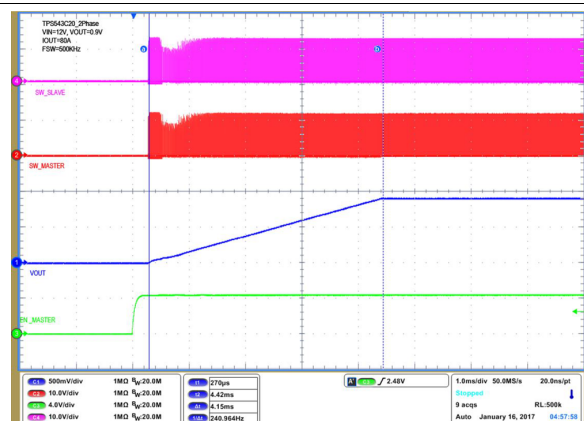


Figure 34. Start up from Enable, 0.9-V Output at 12 VIN, 50-A Output

System Example (continued)

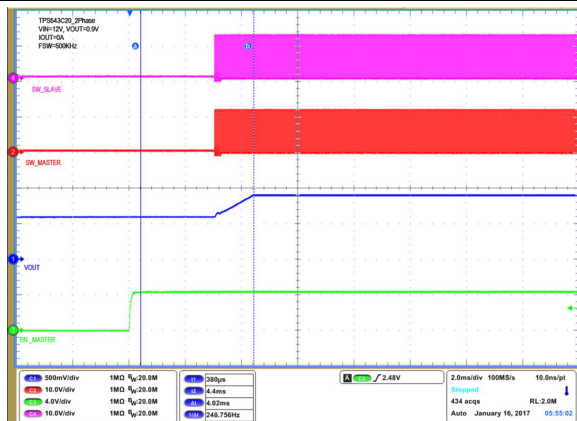


Figure 35. 0.6-V Pre-Bias Start Up From Enable, 0.9-V Output at 12 VIN, 0-A Output

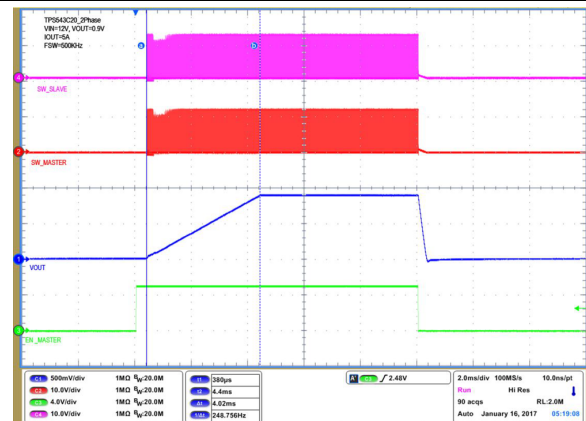


Figure 36. Output Voltage Start-up and Shutdown, 0.9-V Output at 12 VIN, 5-A Output

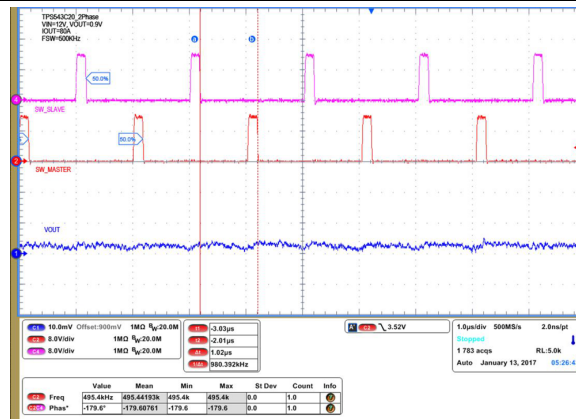


Figure 37. Master-Slave 180° Synchronization

10 Power Supply Recommendations

This device is designed to operate from an input voltage supply between 4 V and 19 V. Ensure the supply is well regulated. Proper bypassing of input supplies and internal regulators is also critical for noise performance, as is the quality of the PCB layout and grounding scheme. See the recommendations in [Layout](#).

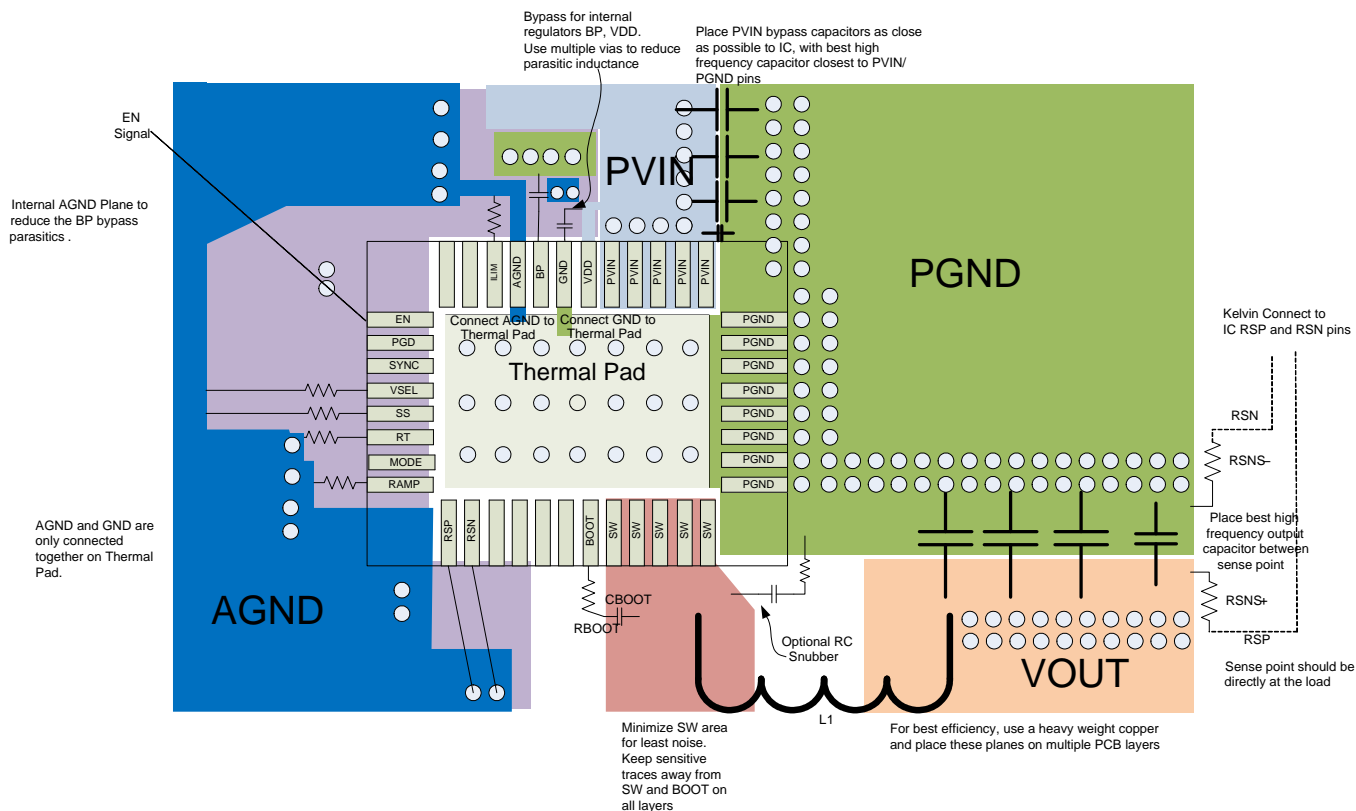
## 11 Layout

### 11.1 Layout Guidelines

- It is absolutely critical that all GND pins, including AGND (pin 29), GND (pin 27), and PGND (pins 13, 14, 15, 16, 17, 18, 19, and 20) are connected directly to the thermal pad underneath the device via traces or plane. The number of thermal vias needed to support 25-A thermal operation should be as many as possible; in the EVM design orderable on the Web, a total of 23 thermal vias are used. The TPS543B20EVM-799 is available for purchase at ti.com.
- Place the power components (including input/output capacitors, output inductor, and TPS543B20 device) on one side of the PCB (solder side). At least one or two inner layers/planes should be inserted, connecting to power ground, in order to shield and isolate the small signal traces from noisy power lines.
- Place the VIN decoupling capacitors as close to the PVIN and PGND as possible to minimize the input AC current loop. The high frequency decoupling capacitor (1 nF to 0.1  $\mu$ F) should be placed next to the PVIN pin and PGND pin as close as the spacing rule allows. This helps suppressing the switch node ringing.
- Place a 10-nF to 100-nF capacitor close to IC from Pin 25 VIN to Pin 27 GND.
- Place VDD and BP decoupling capacitors as close to the device pins as possible. Do not use PVIN plane connection for VDD. VDD needs to be tapped off from PVIN with separate trace connection. Ensure to provide GND vias for each decoupling capacitor and make the loop as small as possible.
- The PCB trace defined as switch node, which connects the SW pins and up-stream of the output inductor should be as short and wide as possible. In web orderable EVM design, the SW trace width is 400mil. Use separate via or trace to connect SW node to snubber and bootstrap capacitor. Do not combine these connections.
- All sensitive analog traces and components such as RAMP, RSP, RSN, ILIM, MODE, VSEL and RT should be placed away from any high voltage switch node (itself and others), such as SW and BOOT to avoid noise coupling. In addition, MODE, VSEL, ILIM, RAMP and RT programming resistors should be placed near the device/pins.
- The RSP and RSN pins operate as inputs to a differential remote sense amplifier that operates with very high impedance. It is essential to route the RSP and RSN pins as a pair of diff-traces in Kelvin-sense fashion. Route them directly to either the load sense points (+ and –) or the output bulk capacitors. The internal circuit uses the VOSNS pin for on-time adjustment. It is critical to tie the VOSNS pin directly tied to VOUT (load sense point) for accurate output voltage result.
- Use caution when routing of the SYNC, VSHARE and ISHARE traces for 2-phase configurations. The SYNC trace carries a rail-to-rail signal and should be routed away from sensitive analog signals, including the VSHARE, ISHARE, RT, and FB signals. The VSHARE and ISHARE traces should also be kept away from fast switching voltages or currents formed by the PVIN, AVIN, SW, BOOT, and BP pins.



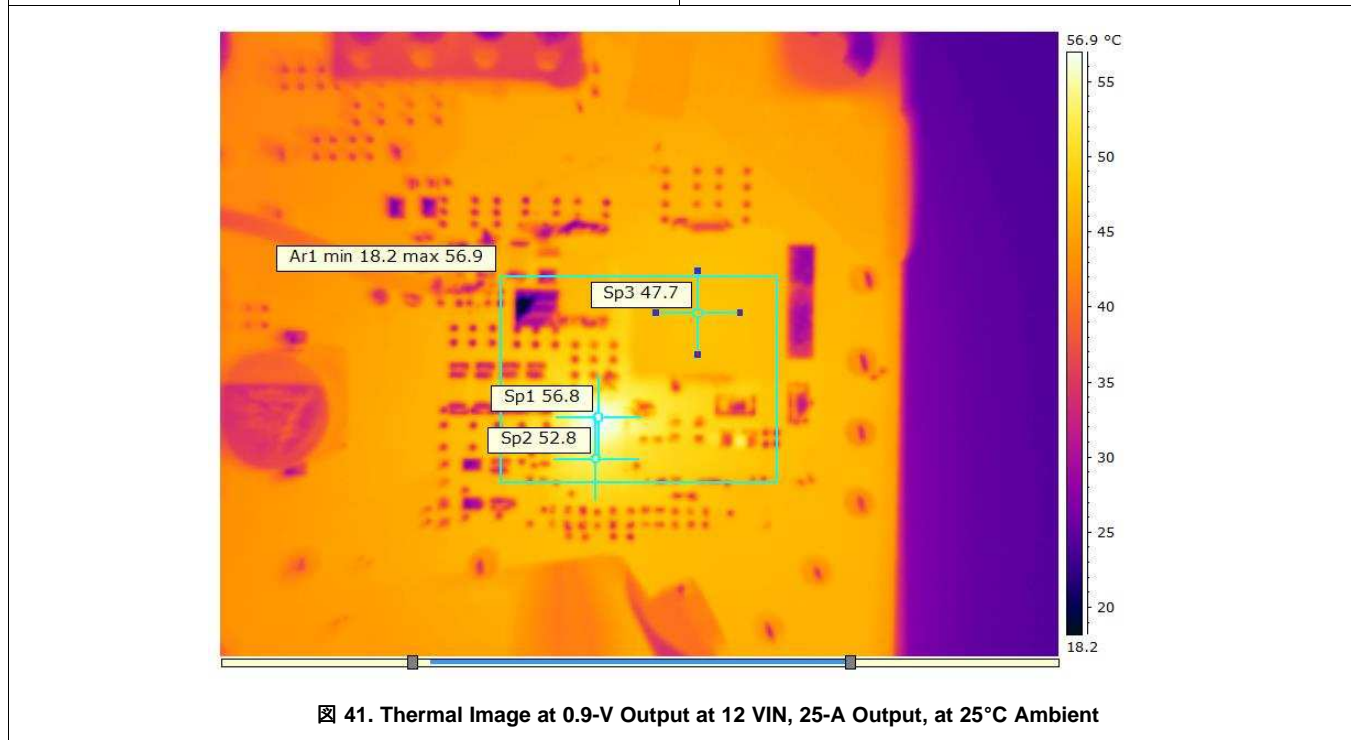
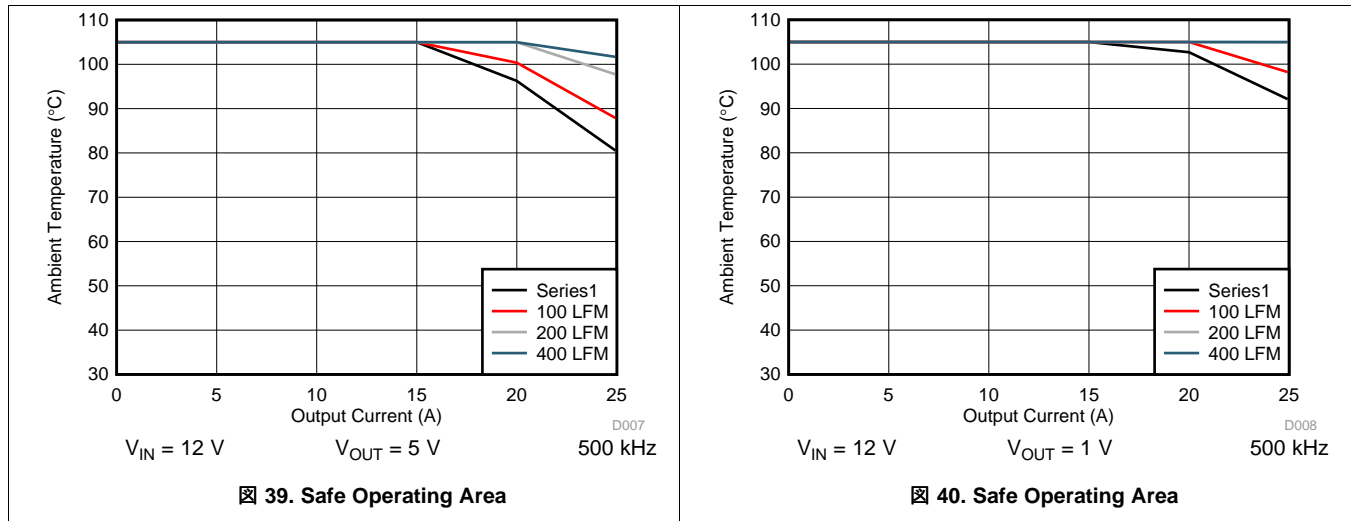
## 11.2 Layout Example



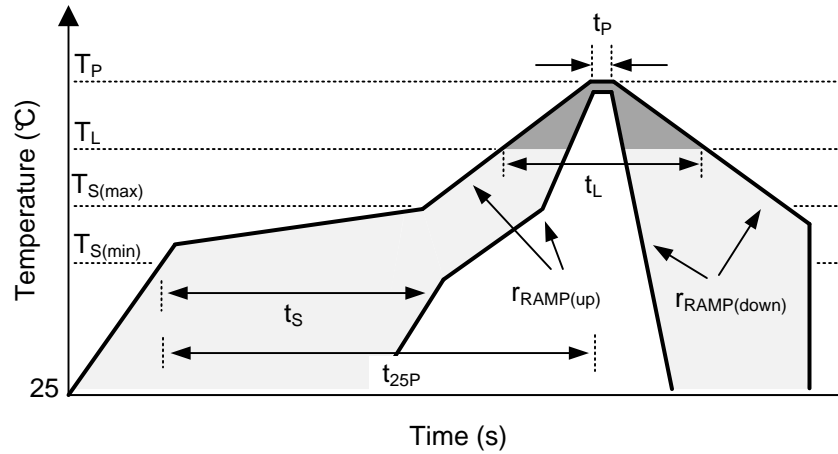
38. Example Layout

### 11.3 Package Size, Efficiency and Thermal Performance

The TPS543B20 device is available in a 5 mm x 7 mm, QFN package with 40 power and I/O pins. It employs TI proprietary MCM packaging technology with thermal pad. With a properly designed system layout, applications achieve optimized safe operating area (SOA) performance. The curves shown in [Fig 39](#) and [Fig 40](#) are based on the orderable evaluation module design.



**Package Size, Efficiency and Thermal Performance (continued)**



**图 42. Recommended Reflow Oven Thermal Profile**

**表 7. Recommended Thermal Profile Parameters**

| PARAMETER                    |                                                                | MIN | TYP | MAX | UNIT |
|------------------------------|----------------------------------------------------------------|-----|-----|-----|------|
| <b>RAMP UP AND RAMP DOWN</b> |                                                                |     |     |     |      |
| r <sub>RAMP(up)</sub>        | Average ramp-up rate, T <sub>S(MAX)</sub> to T <sub>P</sub>    |     |     | 3   | °C/s |
| r <sub>RAMP(down)</sub>      | Average ramp-down rate, T <sub>P</sub> to T <sub>S(MAX)</sub>  |     |     | 6   | °C/s |
| <b>PRE-HEAT</b>              |                                                                |     |     |     |      |
| T <sub>S</sub>               | Pre-heat temperature                                           | 150 |     | 200 | °C   |
| t <sub>S</sub>               | Pre-heat time, T <sub>S(min)</sub> to T <sub>S(max)</sub>      | 60  |     | 180 | s    |
| <b>REFLOW</b>                |                                                                |     |     |     |      |
| T <sub>L</sub>               | Liquidus temperature                                           |     | 217 |     | °C   |
| T <sub>P</sub>               | Peak temperature                                               |     |     | 260 | °C   |
| t <sub>L</sub>               | Time maintained above liquidus temperature, T <sub>L</sub>     | 60  |     | 150 | s    |
| t <sub>P</sub>               | Time maintained within 5°C of peak temperature, T <sub>P</sub> | 20  |     | 40  | s    |
| t <sub>25P</sub>             | Total time from 25°C of peak temperature, T <sub>P</sub>       |     |     | 480 | s    |

## 12 デバイスおよびドキュメントのサポート

### 12.1 デバイス・サポート

#### 12.1.1 開発サポート

##### 12.1.1.1 WEBENCH®ツールによるカスタム設計

[ここをクリック](#)すると、WEBENCH® Power Designerにより、TPS543B20デバイスを使用するカスタム設計を作成できます。

- 最初に、入力電圧( $V_{IN}$ )、出力電圧( $V_{OUT}$ )、出力電流( $I_{OUT}$ )の要件を入力します。
- 最適化ダイアログを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
- 生成された設計を、テキサス・インスツルメンツが提供する他のソリューションと比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

ほとんどの場合、次の操作を実行可能です。

- 電氣的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットでエクスポートする。
- 設計のレポートをPDFで印刷し、同僚と設計を共有する。

WEBENCHツールの詳細は、[www.ti.com/WEBENCH](http://www.ti.com/WEBENCH)でご覧になれます。

#### 12.1.2 ドキュメントのサポート

##### 12.1.2.1 関連資料

関連資料については、以下を参照してください。

[『TPS543B20 25A、シングル・フェーズ同期整流降圧型コンバータ』](#)

### 12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com)のデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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**設計サポート** TIの設計サポート役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

### 12.4 商標

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### 12.5 静電気放電に関する注意事項



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## 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)     | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|---------------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS543B20RVFR    | ACTIVE        | LQFN-CLIP    | RVF             | 40   | 2500        | RoHS-Exempt & Green | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | TPS543B20               | <a href="#">Samples</a> |
| TPS543B20RVFT    | ACTIVE        | LQFN-CLIP    | RVF             | 40   | 250         | RoHS-Exempt & Green | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | TPS543B20               | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS543B20RVFR | LQFN-CLIP    | RVF             | 40   | 2500 | 330.0              | 16.4               | 5.35    | 7.35    | 1.7     | 8.0     | 16.0   | Q1            |
| TPS543B20RVFT | LQFN-CLIP    | RVF             | 40   | 250  | 180.0              | 16.4               | 5.35    | 7.35    | 1.7     | 8.0     | 16.0   | Q1            |



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

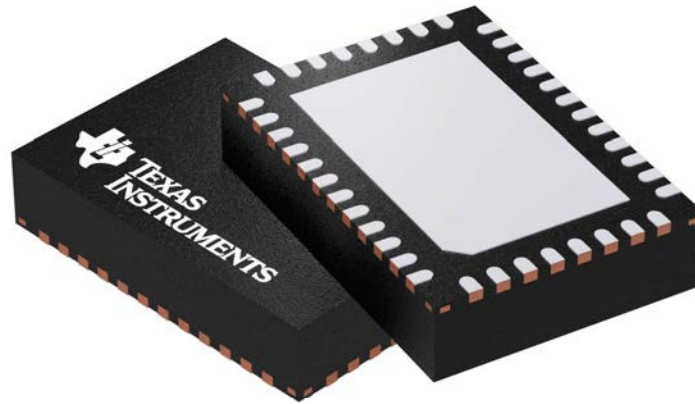
| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS543B20RVFR | LQFN-CLIP    | RVF             | 40   | 2500 | 367.0       | 367.0      | 38.0        |
| TPS543B20RVFT | LQFN-CLIP    | RVF             | 40   | 250  | 210.0       | 185.0      | 35.0        |

## GENERIC PACKAGE VIEW

**RVF 40**

**LQFN-CLIP - 1.52 mm max height**

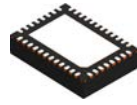
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4211383/D

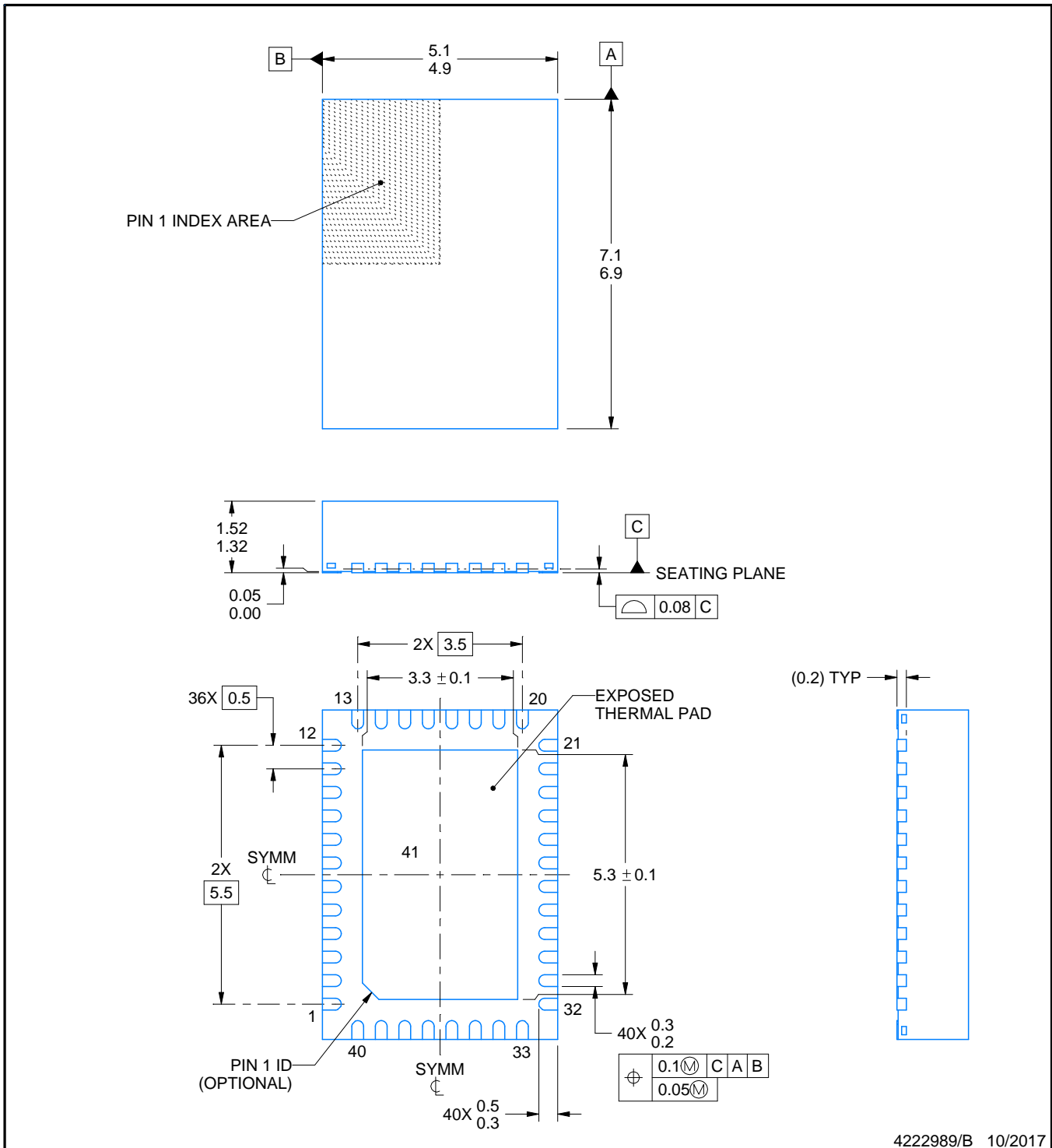
**RVF0040A**



**PACKAGE OUTLINE**

**LQFN-CLIP - 1.52 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



**NOTES:**

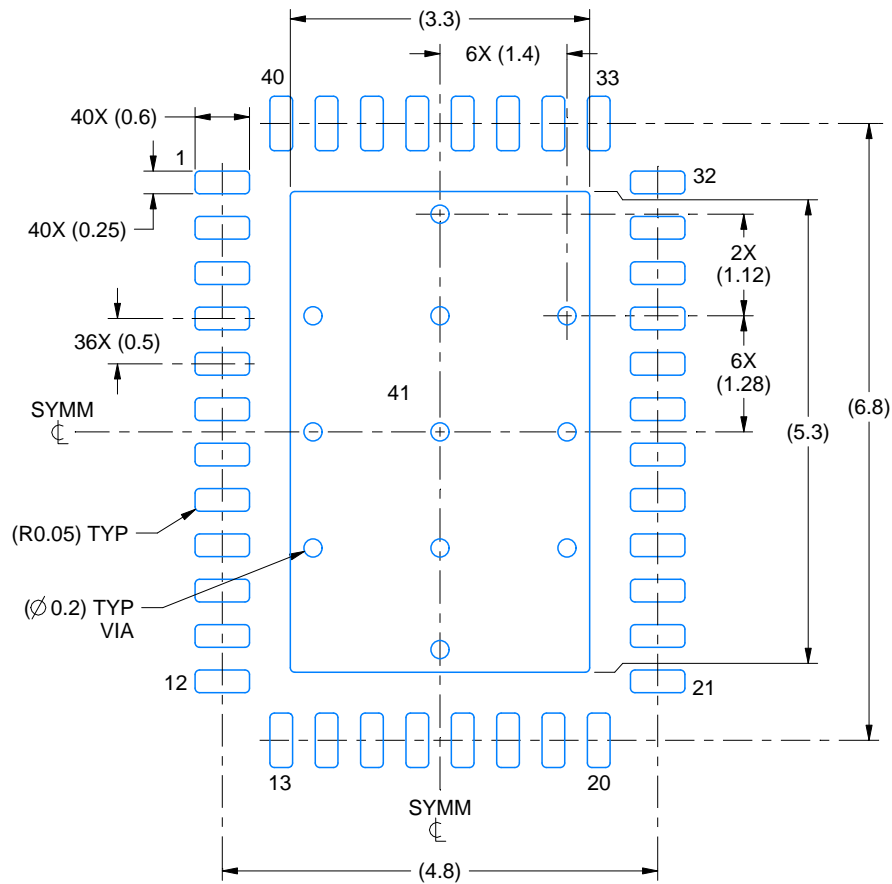
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220.

# EXAMPLE BOARD LAYOUT

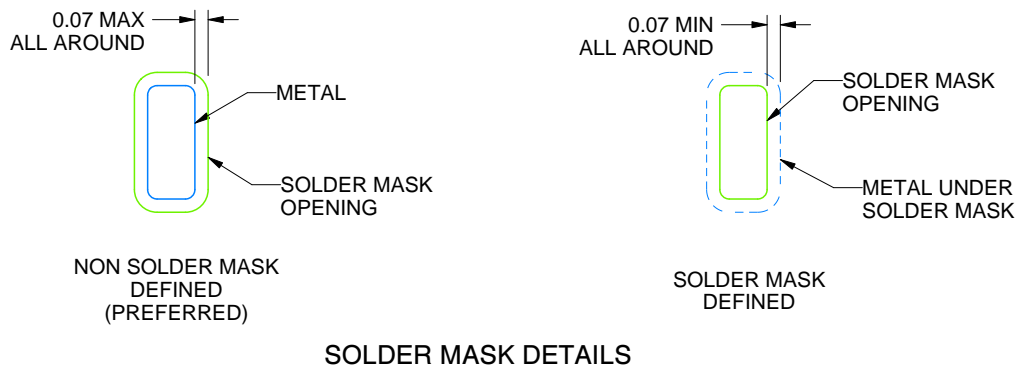
**RVF0040A**

**LQFN-CLIP - 1.52 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



**LAND PATTERN EXAMPLE**  
SCALE:12X



**SOLDER MASK DETAILS**

4222989/B 10/2017

NOTES: (continued)

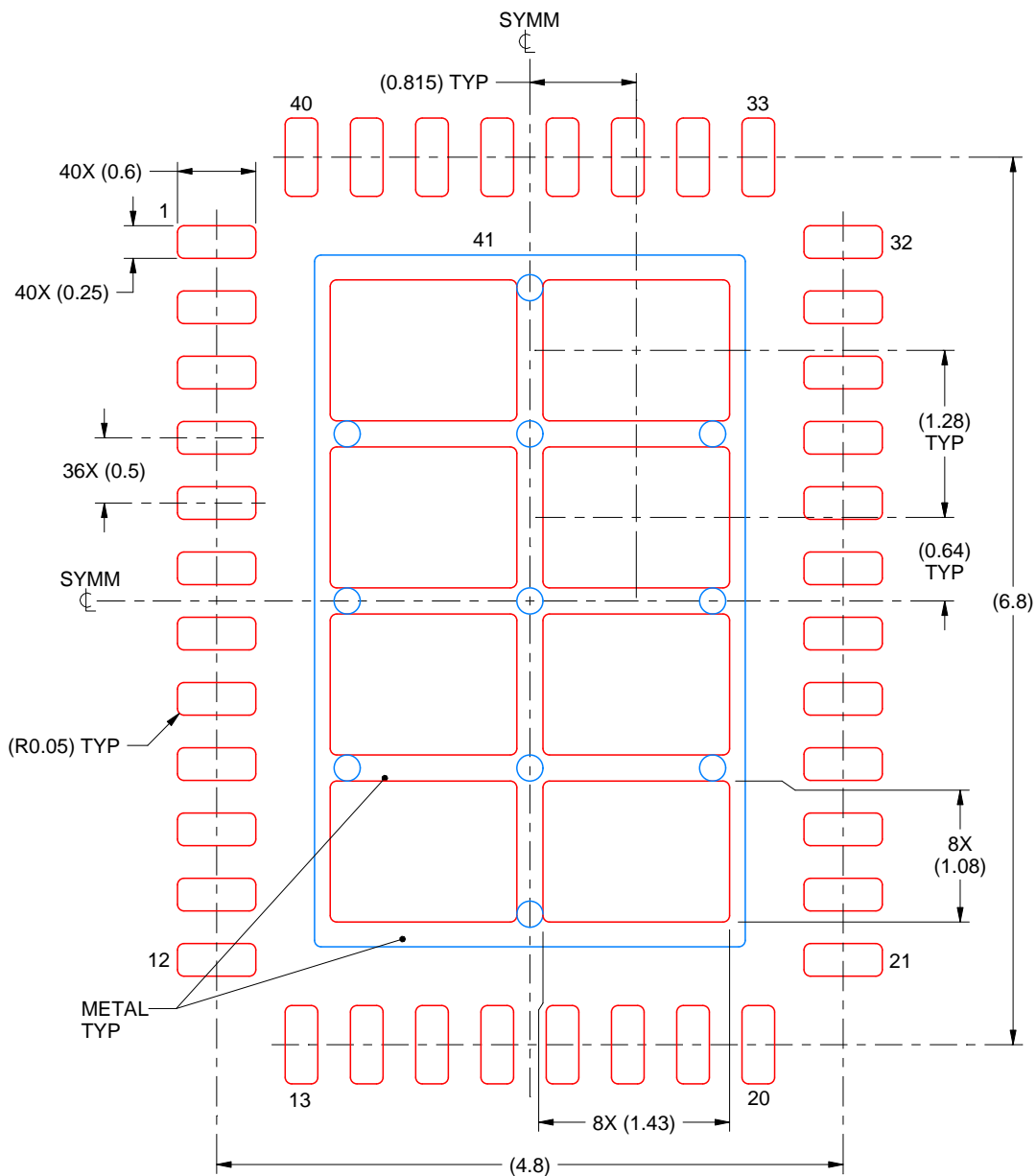
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

**RVF0040A**

**LQFN-CLIP - 1.52 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
71% PRINTED SOLDER COVERAGE BY AREA  
SCALE:18X

4222989/B 10/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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