JAJSHM1B – JULY 2008 – REVISED JUNE 2019

TPS5450-Q1 車載用、5.5V～36V、5A 降圧型コンバータ

1 特長

- 車載アプリケーションに対応
- 広い入力電圧範囲：5.5V～36V
- 最大 5A の連続出力電流 (ピーク 6A)
- 110mΩ の内蔵 MOSFET スイッチで 90% を超える高効率を実現
- 広い出力電圧範囲: 1.5%の初期精度で最低1.22Vまで設定可能
- 内部補償により外付け部品の数を最小化
- 500kHz の固定スイッチング周波数によりフィルタを小型化
- シャットダウン時の消費電流：18µA
- 入力電圧フィード･フォワードにより、ライン･レギュレーションと過渡応答が向上
- 過電流制限、過電圧保護、サーマル・シャットダウンによりシステムを保護
- 動作時の接合部温度範囲：-40℃～125℃
- 熱特性が強化された小型の 8 ピン SOIC PowerPAD™パッケージで供給
- WEBENCH® Power Designer により、TPS5450-Q1 を使用するカスタム設計を作成

2 アプリケーション

- 高密度のポイント・オブ・ロード・レギュレータ
- LCD ディスプレイ、プラズマ・ディスプレイ
- バッテリ充電器
- 12V/24Vの分散型電源システム

3 概要

TPS5450-Q1 は、低抵抗のハイサイド N チャネル MOSFET を内蔵した大出力電流の PWM コンバータです。一覧の特長とともに、過渡条件で高い電圧レギュレーション精度を維持できる高性能電圧エラー･アンプ、入力電圧が 5.5V に達するまでスタートアップを抑止する低電圧誤動作防止回路、突入電流を制限するように内部的に設定されるスロースタート回路、過渡応答を改善するための電圧フィードフォワード回路が基板に搭載されています。ENA ピンを使用すると、シャットダウン時の消費電流を 18µA (標準値) に低減できます。また、アクティブ HIGH イネーブル、過電流制限、過電圧保護、サーマル･シャットダウンの機能も備えています。設計の複雑性を低減し、外付け部品数を減らすため、TPS5450-Q1 の帰還ループは内部的に補償されています。

TPS5450-Q1 デバイスは、熱特性が強化された 8 ピン SOIC PowerPAD™ パッケージで供給されます。TI は、お客様が短期間の開発サイクルに対応して高性能電源を設計できるように、評価モジュールとソフトウェア･ツールを提供しています。

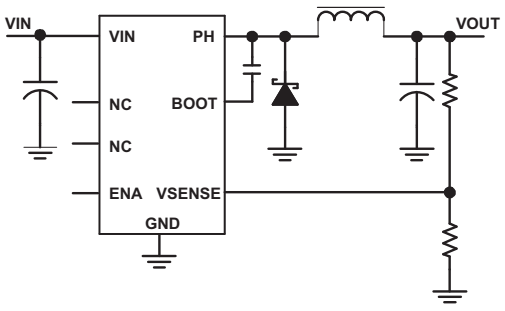
製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS5450-Q1	HSOIC (8)	4.89mm×3.90mm

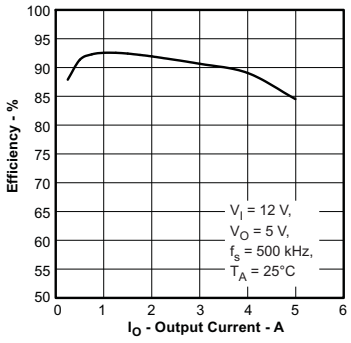
(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図と効率曲線

Simplified Schematic



Efficiency vs Output Current



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (October 2011) から Revision B に変更 **Page**

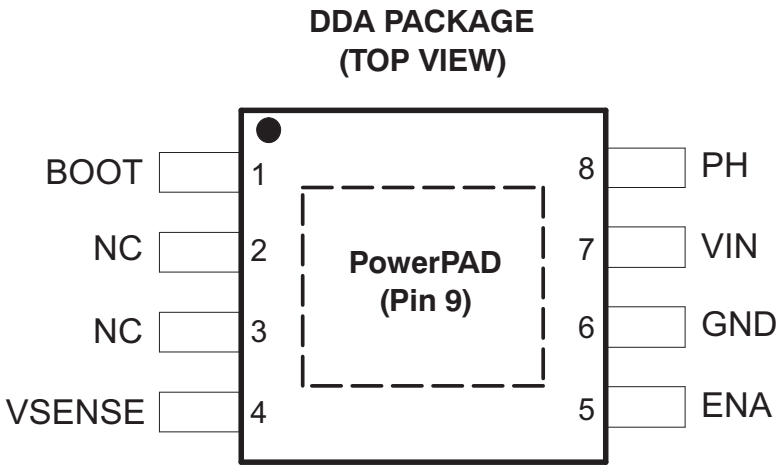
- 編集上の変更のみ、WEBENCH へのリンクを追加 ... 1

2008年7月発行のものから更新 **Page**

- Added *Thermal Table* ... 4

5 Pin Configuration and Functions

DDA Package
8-Pin SO PowerPAD
Top View



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
BOOT	1	Boost capacitor for the high-side FET gate driver. Connect 0.01-µF low-ESR capacitor from BOOT pin to PH pin.
NC	2, 3	No internal connection
VSENSE	4	Feedback voltage for the regulator. Connect to output voltage divider.
ENA	5	On/off control. Below 0.5 V, the device stops switching. Float the pin to enable.
GND	6	Ground. Connect to thermal pad.
VIN	7	Input supply voltage. Bypass VIN pin to GND pin close to device package with a high-quality low-ESR ceramic capacitor.
PH	8	Source of the high side power MOSFET. Connected to external inductor and diode.
PowerPAD	9	GND pin must be connected to the exposed pad for proper operation.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

V_I	Input voltage range	VIN	–0.3 V to 40 V(3)
		BOOT	–0.3 V to 50 V
		PH (steady-state)	–0.6 V to 40 V(3)
		ENA	–0.3 V to 7 V
		BOOT-PH	10 V
		VSENSE	–0.3 V to 3 V
		PH (transient < 10 ns)	–1.2 V
I_O	Source current	PH	Internally Limited
I_{lkg}	Leakage current	PH	10 μA
T_J	Operating virtual-junction temperature range		–40°C to 150°C
T_{stg}	Storage temperature		–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Approaching the absolute maximum rating for the VIN pin may cause the voltage on the PH pin to exceed the absolute maximum rating.

6.2 Recommended Operating Conditions

		MIN	MAX	UNIT
V_I	Input voltage range	5.5	36	V
T_J	Operating virtual-junction temperature	–40	125	°C

6.3 Thermal Information

THERMAL METRIC(1)		TPS5450-Q1 DDA 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	48.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	47.1	°C/W
θ_{JB}	Junction-to-board thermal resistance(4)	22.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)	5.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter(6)	22.4	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	2.9	°C/W

(1) 従来および新しい熱測定値の詳細については、『*Semiconductor and IC Package Thermal Metrics*』アプリケーション・レポート (SPRA953)を参照してください。
(2) 自然対流における、接合部と周囲の空気との間の熱抵抗は、JESD51-2aに記述されている環境において、JESD51-7で規定されているJEDEC標準のHigh-Kボード上でのシミュレーションによって求められます。
(3) 接合部とケース(上面)との間の熱抵抗は、パッケージ上面での冷却板試験のシミュレーションによって求められます。JEDEC規格試験では規定されていませんが、ANSIが策定したSEMI規格のG30-88に類似した記述があります。
(4) 接合部と基板との間の熱抵抗は JESD51-8で説明されているように、PCB温度を制御するリング型冷却板治具で環境をシミュレーションすることにより求められます。
(5) 接合部とケース上部との間の特性パラメータψ_{JT}は、実際のシステムにおけるデバイスの接合部温度を推定するもので、JESD51-2a (セクション6および7)に記述されている手順を用いて、$R_{\theta JA}$を求めるためのシミュレーションデータから抽出されます。
(6) 接合部と基板との間の特性パラメータψ_{JB}は、実際のシステムにおけるデバイスの接合部温度を推定するもので、JESD51-2a (セクション6および7)に記述されている手順を用いて、$R_{\theta JA}$を求めるためのシミュレーションデータから抽出されます。
(7) 接合部とケース(底面)との間の熱抵抗は、露出したパッド(Power PAD)上での冷却板試験のシミュレーションによって求められます。JEDEC規格試験では規定されていませんが、ANSIが策定したSEMI規格のG30-88に類似した内容があります。

6.4 Dissipation Ratings(1)(2)

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT
8-Pin DDA (4-layer board with solder)(3)	30°C/W

(1) Maximum power dissipation may be limited by overcurrent protection.
(2) Power rating at a specific ambient temperature T_A should be determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long-term reliability. See *Thermal Calculations* in applications section of this data sheet for more information.
(3) Test board conditions:
  (a) 2 in x 1.85 in, 4 layers, 0.062-in (1,57-mm) thickness
  (b) 2-oz copper traces located on the top and bottom of the PCB
  (c) 2-oz copper ground planes on the two internal layers
  (d) Four thermal vias in the PowerPAD area under the device package

6.5 Electrical Characteristics

T_J = –40°C to +125°C, V_{IN} = 5.5 V to 36 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
I_Q	Quiescent current	VSENSE = 2 V, Not switching, PH pin open		3	4.4	mA
		Shutdown, ENA = 0 V		18	50	μA
UNDERVOLTAGE LOCKOUT (UVLO)						
	Start threshold voltage, UVLO			5.3	5.5	V
	Hysteresis voltage, UVLO			330		mV
VOLTAGE REFERENCE						
	Voltage reference accuracy	T_J = 25°C	1.202	1.221	1.239	V
		I_O = 0 A – 5 A	1.196	1.221	1.245	
OSCILLATOR						
	Internally set free-running frequency		400	500	600	kHz
	Minimum controllable on time			150	200	ns
	Maximum duty cycle		87	89		%
ENABLE (ENA PIN)						
	Start threshold voltage, ENA				1.3	V
	Stop threshold voltage, ENA		0.5			V
	Hysteresis voltage, ENA			450		mV
	Internal slow-start time (0~100%)		5.4	8	10	ms
CURRENT LIMIT						
	Current limit		5.7	7.5	9.0	A
	Current limit hiccup time		13	16	21	ms
THERMAL SHUTDOWN						
	Thermal shutdown trip point		135	162		°C
	Thermal shutdown hysteresis			14		°C
OUTPUT MOSFET						
$r_{DS(on)}$	High-side power MOSFET switch	VIN = 5.5 V		150		mΩ
				110	230	

6.6 Typical Characteristics

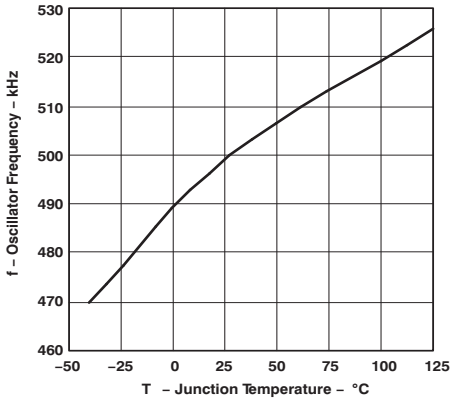


図 1. Oscillator Frequency vs Junction Temperature

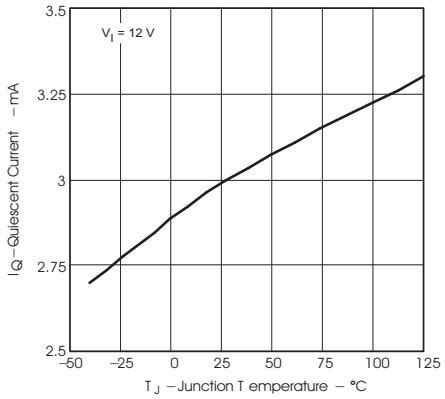


図 2. Non-Switching Quiescent Current vs Junction Temperature

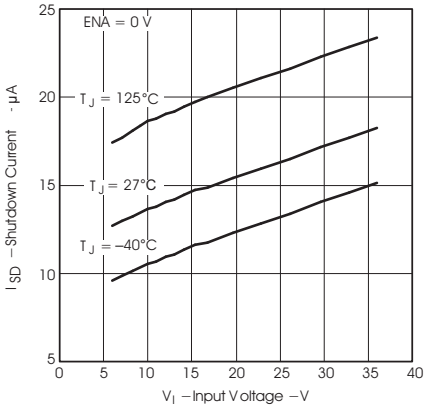


図 3. Shutdown Quiescent Currentvsinput Voltage

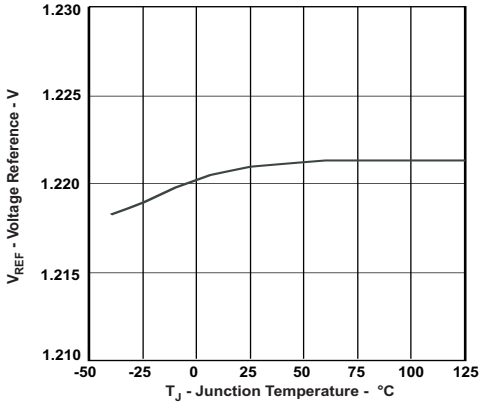


図 4. Voltage Reference vs Junction Temperature

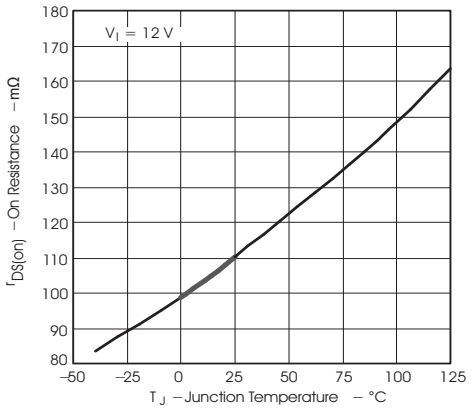


図 5. On-Resistance vs Junction Temperature

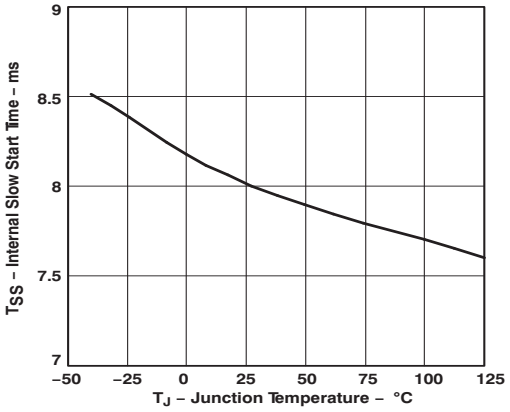


図 6. Internal Slow Start Time vs Junction Temperature

Typical Characteristics (continued)

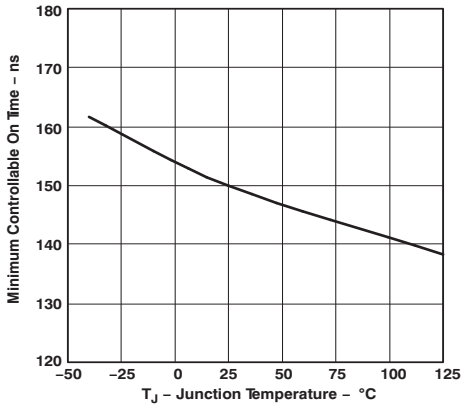


図 7. Minimum Controllable On-Time vs Junction Temperature

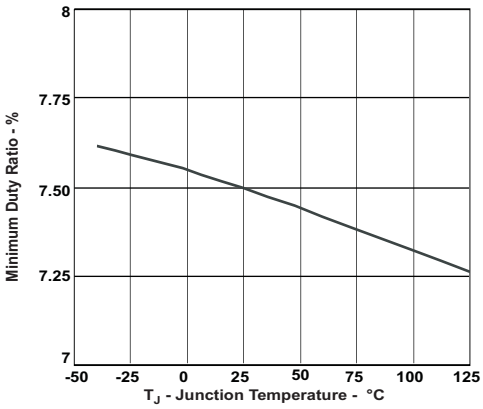


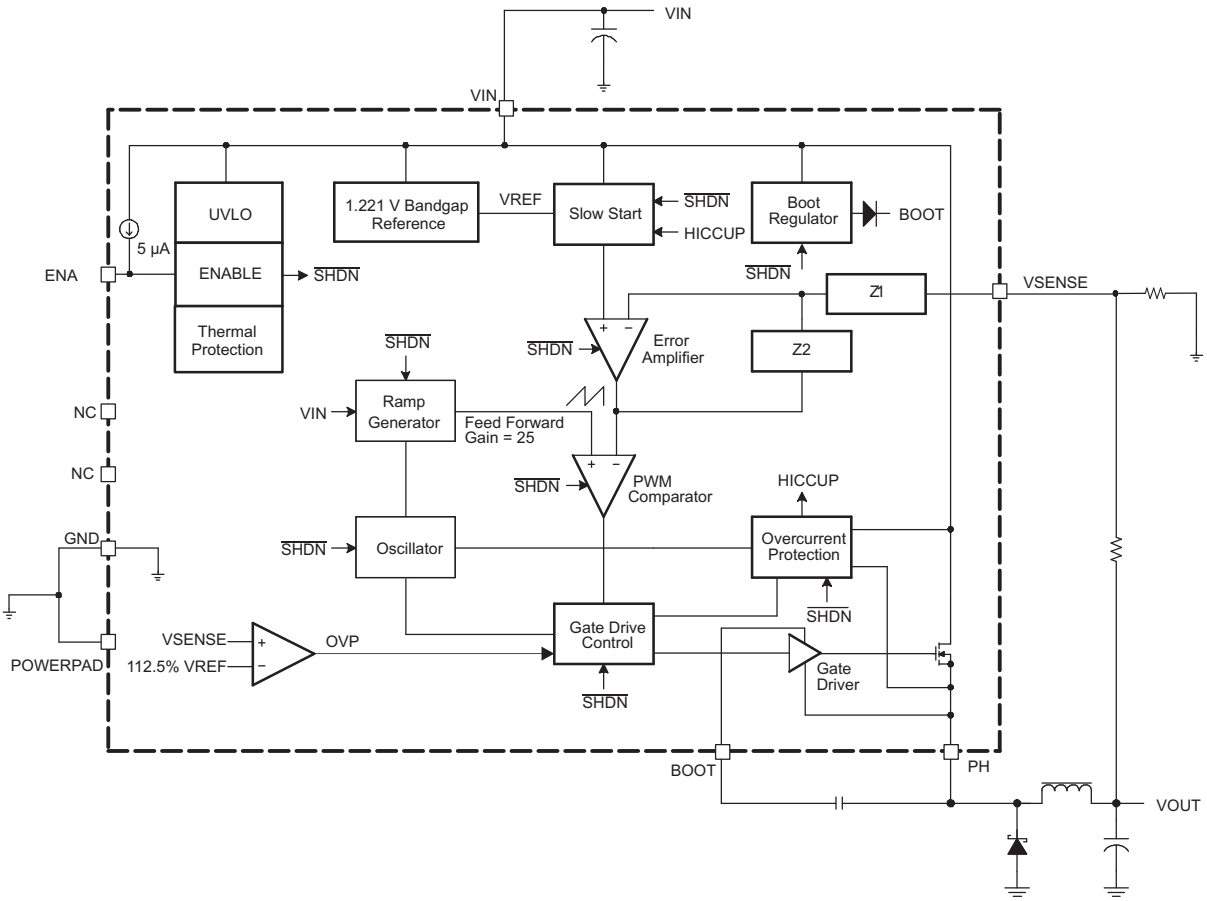
図 8. Minimum Controllable Duty Ratio vs Junction Temperature

7 Detailed Description

7.1 Overview

The TPS5450-Q1 is a high-output-current PWM converter that integrates a low-resistance high-side N-channel MOSFET. Included on the substrate with the listed features are a high-performance voltage error amplifier that provides tight voltage regulation accuracy under transient conditions, an undervoltage-lockout circuit to prevent start-up until the input voltage reaches 5.5 V, an internally set slow-start circuit to limit inrush currents, and a voltage feedforward circuit to improve the transient response. Using the ENA pin, shutdown supply current is reduced to 18 μA typically. Other features include an active-high enable, overcurrent limiting, overvoltage protection, and thermal shutdown. To reduce design complexity and external component count, the TPS5450-Q1 feedback loop is internally compensated.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Oscillator Frequency

The internal free-running oscillator sets the PWM switching frequency at 500 kHz. The 500-kHz switching frequency allows less output inductance for the same output ripple requirement resulting in a smaller output inductor.

7.3.2 Voltage Reference

The voltage reference system produces a precision reference signal by scaling the output of a temperature stable bandgap circuit. The bandgap and scaling circuits are trimmed during production testing to an output of 1.221 V at room temperature.

7.3.3 Enable (ENA) and Internal Slow Start

The ENA pin provides electrical on/off control of the regulator. Once the ENA pin voltage exceeds the threshold voltage, the regulator starts operation and the internal slow start begins to ramp. If the ENA pin voltage is pulled below the threshold voltage, the regulator stops switching and the internal slow start resets. Connecting the pin to ground or to any voltage less than 0.5 V disables the regulator and activates the shutdown mode. The quiescent current of the TPS5450-Q1 in shutdown mode is 18 μA (typical).

The ENA pin has an internal pullup current source, allowing the user to float the ENA pin. If an application requires controlling the ENA pin, use open drain or open collector output logic to interface with the pin. To limit the start-up inrush current, an internal slow-start circuit is used to ramp up the reference voltage from 0 V to its final value, linearly. The internal slow start time is 8 ms (typical).

7.3.4 Undervoltage Lockout (UVLO)

The TPS5450-Q1 incorporates an undervoltage lockout circuit to keep the device disabled when VIN (the input voltage) is below the UVLO start voltage threshold. During power up, internal circuits are held inactive and the internal slow start is grounded until VIN exceeds the UVLO start threshold voltage. Once the UVLO start threshold voltage is reached, the internal slow start is released and device start-up begins. The device operates until VIN falls below the UVLO stop threshold voltage. The typical hysteresis in the UVLO comparator is 330 mV.

7.3.5 Output Feedback (VSENSE) and Internal Compensation

The output voltage of the regulator is set by feeding back the center point voltage of an external resistor divider network to the VSENSE pin. In steady-state operation, the VSENSE pin voltage must be equal to the voltage reference 1.221 V.

The TPS5450-Q1 implements internal compensation to simplify the regulator design. Because the TPS5450-Q1 uses voltage-mode control, a type 3 compensation network has been designed on chip to provide a high crossover frequency and a high phase margin for good stability. See the *Internal Compensation Network* section for more details.

7.3.6 Voltage Feedforward

The internal voltage feedforward provides a constant dc power stage gain despite any variations with the input voltage. This greatly simplifies the stability analysis and improves the transient response. Voltage feedforward varies the peak ramp voltage inversely with the input voltage so that the modulator and power stage gain are constant at the feed forward gain:

$$\text{Feed Forward Gain} = \frac{\text{VIN}}{\text{Ramp}_{\text{pk}-\text{pk}}} \tag{1}$$

The typical feed forward gain of TPS5450-Q1 is 25.

Feature Description (continued)

7.3.7 Pulse-Width-Modulation (PWM) Control

The regulator employs a fixed-frequency pulse-width-modulator (PWM) control method. First, the feedback voltage (VSENSE pin voltage) is compared to the constant voltage reference by the high-gain error amplifier and compensation network to produce a error voltage. Then, the error voltage is compared to the ramp voltage by the PWM comparator. In this way, the error-voltage magnitude is converted to a pulse width, which is the duty cycle. Finally, the PWM output is fed into the gate drive circuit to control the on-time of the high-side MOSFET.

7.3.8 Overcurrent Limiting

Overcurrent limiting is implemented by sensing the drain-to-source voltage across the high-side MOSFET. The drain to source voltage is then compared to a voltage level representing the overcurrent threshold limit. If the drain-to-source voltage exceeds the overcurrent threshold limit, the overcurrent indicator is set true. The system ignores the overcurrent indicator for the leading edge blanking time at the beginning of each cycle to avoid any turnon noise glitches.

Once overcurrent indicator is set true, overcurrent limiting is triggered. The high-side MOSFET is turned off for the rest of the cycle after a propagation delay. The overcurrent limiting mode is called cycle-by-cycle current limiting.

Sometimes under serious overload conditions such as short-circuit, the overcurrent runaway may still happen when using cycle-by-cycle current limiting. A second mode of current limiting is used; in other words, hiccup mode overcurrent limiting. During hiccup mode overcurrent limiting, the voltage reference is grounded and the high-side MOSFET is turned off for the hiccup time. Once the hiccup time duration is complete, the regulator restarts under control of the slow start circuit.

7.3.9 Overvoltage Protection

The TPS5450-Q1 has an overvoltage protection (OVP) circuit to minimize voltage overshoot when recovering from output fault conditions. The OVP circuit includes an overvoltage comparator to compare the VSENSE pin voltage and a threshold of 112.5% × VREF. Once the VSENSE pin voltage is higher than the threshold, the high-side MOSFET is forced off. When the VSENSE pin voltage drops lower than the threshold, the high-side MOSFET is enabled again.

7.3.10 Thermal Shutdown

The TPS5450-Q1 protects itself from overheating with an internal thermal shutdown circuit. If the junction temperature exceeds the thermal shutdown trip point, the voltage reference is grounded and the high-side MOSFET is turned off. The part is restarted under control of the slow start circuit automatically when the junction temperature drops 14°C below the thermal shutdown trip point.

8 Application Information

8.1 Application Information

The TPS5450-Q1 can provide up to 5-A output current at a nominal output voltage of 5 V. For proper thermal performance, the exposed PowerPAD™ underneath the device must be soldered down to the printed-circuit board. The following design procedure can be used to select component values for the TPS5450-Q1.

8.2 Typical Application

図 9 shows the schematic for a typical TPS5450-Q1 application.

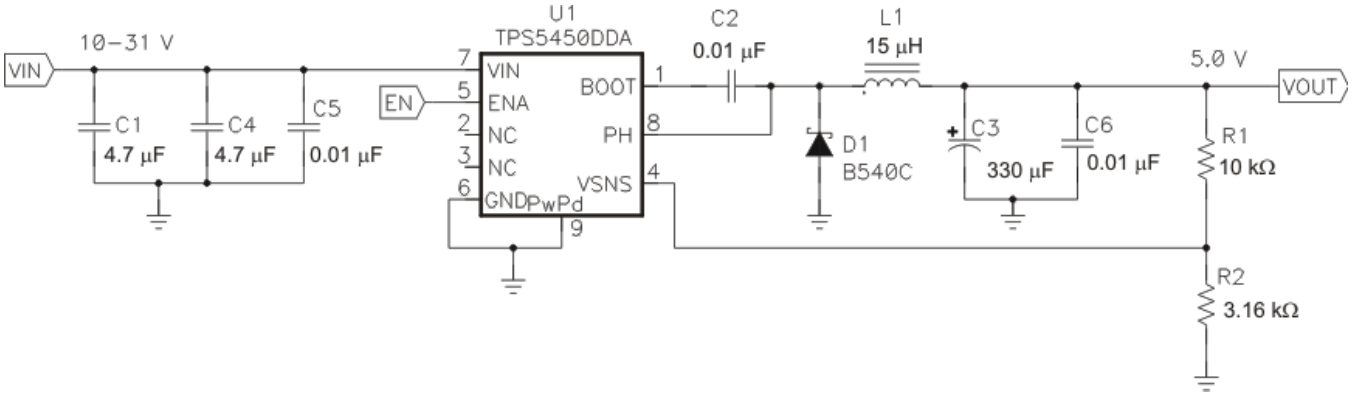


図 9. Application Circuit, 12-V to 5-V

8.2.1 Design Requirements

To begin the design process a few parameters must be decided upon. The designer needs to know the following:

- Input voltage range
- Output voltage
- Input ripple voltage
- Output ripple voltage
- Output current rating
- Operating frequency

表 1. Design Parameters

DESIGN PARAMETER(1)	EXAMPLE VALUE
Input voltage range	10 V to 31 V
Output voltage	5 V
Input ripple voltage	400 mV
Output ripple voltage	30 mV
Output current rating	5 A
Operating frequency	500 kHz

(1) As an additional constraint, the design is set up to be small size and low component height.

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS5450-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Boost Capacitor (BOOT)

Connect a 0.01-μF low-ESR ceramic capacitor between the BOOT pin and PH pin. This capacitor provides the gate drive voltage for the high-side MOSFET. X7R or X5R grade dielectrics are recommended due to their stable values over temperature.

8.2.2.3 Switching Frequency

The switching frequency for the TPS5450-Q1 is internally set to 500 kHz. It is not possible to adjust the switching frequency.

8.2.2.4 Input Capacitors

The TPS5450-Q1 requires an input decoupling capacitor and, depending on the application, a bulk input capacitor. The minimum recommended decoupling capacitance is 4.7 μF. A high-quality ceramic type X5R or X7R is required. For some applications, a smaller value decoupling capacitor may be used, so long as the input voltage and current ripple ratings are not exceeded. The voltage rating must be greater than the maximum input voltage, including ripple.

This input ripple voltage can be approximated by 式 2 :

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{sw}} + \left(I_{OUT(MAX)} \times ESR_{MAX}\right) \quad (2)$$

where

- $I_{OUT(MAX)}$ is the maximum load current
- f_{SW} is the switching frequency
- C_{IN} is the input capacitor value
- ESR_{MAX} is the maximum series resistance of the input capacitor

For this design, the input capacitance consists of two 4.7 μF capacitors, C1 and C4, in parallel. An additional high-frequency bypass capacitor, C5 is also used.

The maximum RMS ripple current also needs to be checked. For worst case conditions, this can be approximated by 式 3 :

$$I_{CIN} = \frac{I_{OUT(MAX)}}{2} \quad (3)$$

In this case the input ripple voltage would be 281 mV and the RMS ripple current would be 2.5 A. The maximum voltage across the input capacitors would be VIN max plus delta VIN/2. The chosen input decoupling capacitor is rated for 50 V, and the ripple current capacity is greater than 2.5 A each, providing ample margin. It is very important that the maximum ratings for voltage and current are not exceeded under any circumstance.

Additionally some bulk capacitance may be needed, especially if the TPS5450-Q1 circuit is not located within about 2 inches from the input voltage source. The value for this capacitor is not critical but it also should be rated to handle the maximum input voltage including ripple voltage and should filter the output so that input ripple voltage is acceptable.

8.2.2.5 Output Filter Components

Two components need to be selected for the output filter, L1 and C2. Because the TPS5450-Q1 is an internally compensated device, a limited range of filter component types and values can be supported.

8.2.2.5.1 Inductor Selection

To calculate the minimum value of the output inductor, use 式 4:

$$L_{MIN} = \frac{V_{OUT(MAX)} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times K_{IND} \times I_{OUT} \times F_{SW(MIN)}} \quad (4)$$

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. Three things need to be considered when determining the amount of ripple current in the inductor: the peak-to-peak ripple current affects the output ripple voltage amplitude, the ripple current affects the peak switch current, and the amount of ripple current determines at what point the circuit becomes discontinuous. For designs using the TPS5450-Q1, K_{IND} of 0.2 to 0.3 yields good results. Low output ripple voltages can be obtained when paired with the proper output capacitor, the peak switch current will be well below the current limit set point, and relatively low load currents can be sourced before discontinuous operation.

For this design example use K_{IND} = 0.2 and the minimum inductor value is calculated to be 10.4 μH. A higher standard value is 15 μH, which is used in this design.

For the output filter inductor it is important that the RMS current and saturation current ratings not be exceeded. The RMS inductor current can be found from 式 5:

$$I_{L(RMS)} = \sqrt{I^2_{OUT(MAX)} + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW(MIN)}}\right)^2} \quad (5)$$

and the peak inductor current can be determined with 式 6:

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{1.6 \times V_{IN(MAX)} \times L_{OUT} \times F_{SW(MIN)}} \quad (6)$$

For this design, the RMS inductor current is 5.004 A, and the peak inductor current is 5.34 A. The chosen inductor is a Sumida CDRH1127/LD-150 15 μH. It has a minimum rated current of 5.65 A for both saturation and RMS current. In general, inductor values for use with the TPS5450-Q1 are in the range of 10 μH to 100 μH.

8.2.2.5.2 Capacitor Selection

The important design factors for the output capacitor are dc voltage rating, ripple current rating, and equivalent series resistance (ESR). The dc voltage and ripple current ratings cannot be exceeded. The ESR is important because, along with the inductor ripple current, it determines the amount of output ripple voltage. The actual value of the output capacitor is not critical, but some practical limits do exist. Consider the relationship between the desired closed loop crossover frequency of the design and LC corner frequency of the output filter. Due to the design of the internal compensation, it is desirable to keep the closed loop crossover frequency in the range 3 kHz to 30 kHz, as this frequency range has adequate phase boost to allow for stable operation. For this design example, it is assumed that the intended closed loop crossover frequency is between 2590 Hz and 24 kHz and also below the ESR zero of the output capacitor. Under these conditions the closed loop crossover frequency is related to the LC corner frequency by:

$$f_{CO} = \frac{f_{LC}^2}{85\ V_{OUT}} \quad (7)$$

And the desired output capacitor value for the output filter to:

$$C_{OUT} = \frac{1}{3357 \times L_{OUT} \times f_{CO} \times V_{OUT}} \quad (8)$$

For a desired crossover of 12 kHz and a 15-μH inductor, the calculated value for the output capacitor is 330 μF. The capacitor type should be chosen so that the ESR zero is above the loop crossover. The maximum ESR should be:

$$ESR_{MAX} = \frac{1}{2\pi \times C_{OUT} \times f_{CO}} \quad (9)$$

The maximum ESR of the output capacitor also determines the amount of output ripple as specified in the initial design parameters. The output ripple voltage is the inductor ripple current times the ESR of the output filter. Check that the maximum specified ESR as listed in the capacitor data sheet results in an acceptable output ripple voltage:

$$V_{PP}\,(MAX) = \frac{ESR_{MAX} \times V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{N_C \times V_{IN(MAX)} \times L_{OUT} \times F_{SW}} \quad (10)$$

where

- ΔV_{PP} is the desired peak-to-peak output ripple
- N_C is the number of parallel output capacitors
- F_{SW} is the switching frequency

For this design example, a single 330-μF output capacitor is chosen for C3. The calculated RMS ripple current is 143 mA and the maximum ESR required is 40 mΩ. A capacitor that meets these requirements is a Sanyo Poscap 10TPB330M, rated at 10 V with a maximum ESR of 35 mΩ and a ripple current rating of 3 A. An additional small 0.1-μF ceramic bypass capacitor, C6 is also used in this design.

The minimum ESR of the output capacitor should also be considered. For good phase margin, the ESR zero when the ESR is at a minimum should not be too far above the internal compensation poles at 24 kHz and 54 kHz.

The selected output capacitor must also be rated for a voltage greater than the desired output voltage plus one half the ripple voltage. Any derating amount must also be included. The maximum RMS ripple current in the output capacitor is given by 式 11:

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times N_C} \right) \quad (11)$$

where

- N_C is the number of output capacitors in parallel
- F_{SW} is the switching frequency

Other capacitor types can be used with the TPS5450-Q1, depending on the needs of the application.

8.2.2.6 Output Voltage Setpoint

The output voltage of the TPS5450-Q1 is set by a resistor divider (R1 and R2) from the output to the VSENSE pin. Calculate the R2 resistor value for the output voltage of 5 V using 式 12:

$$R2 = \frac{R1 \times 1.221}{V_{OUT} - 1.221} \quad (12)$$

For any TPS5450-Q1 design, start with an R1 value of 10 kΩ. For an output voltage closest to but at least 5 V, R2 is 3.16 kΩ.

8.2.2.7 Boot Capacitor

The boot capacitor must be 0.01 μF.

8.2.2.8 Catch Diode

The TPS5450-Q1 is designed to operate using an external catch diode between PH and GND. The selected diode must meet the absolute maximum ratings for the application: Reverse voltage must be higher than the maximum voltage at the PH pin, which is V_{INMAX} + 0.5 V. Peak current must be greater than I_{OUTMAX} plus on half the peak to peak inductor current. Forward voltage drop should be small for higher efficiencies. It is important to note that the catch diode conduction time is typically longer than the high-side FET on time, so attention paid to diode parameters can make a marked improvement in overall efficiency. Additionally, check that the device chosen is capable of dissipating the power losses. For this design, a Diodes, Inc. B540A is chosen, with a reverse voltage of 40 V, forward current of 5 A, and a forward voltage drop of 0.5 V.

8.2.2.9 Output Voltage Limitations

Due to the internal design of the TPS5450-Q1, there are both upper and lower output voltage limits for any given input voltage. The upper limit of the output voltage set point is constrained by the maximum duty cycle of 87% and is given by:

$$V_{OUTMAX} = 0.87 \times \left(\left(V_{INMIN} - I_{OMAX} \times 0.230\right) + V_D\right) - \left(I_{OMAX} \times R_L\right) - V_D$$

where

- V_{INMIN} = minimum input voltage
- I_{OMAX} = maximum load current
- V_D = catch diode forward voltage
- R_L= output inductor series resistance (13)

This equation assumes maximum on resistance for the internal high side FET.

The lower limit is constrained by the minimum controllable on time, which may be as high as 200 ns. The approximate minimum output voltage for a given input voltage and minimum load current is given by:

$$V_{OUTMIN} = 0.12 \times \left(\left(V_{INMAX} - I_{OMIN} \times 0.110\right) + V_D\right) - \left(I_{OMIN} \times R_L\right) - V_D$$

where

- V_{INMAX} = maximum input voltage
- I_{OMIN} = minimum load current
- V_D = catch diode forward voltage
- R_L= output inductor series resistance (14)

This equation assumes nominal on resistance for the high-side FET and accounts for worst case variation of operating frequency set point. Any design operating near the operational limits of the device should be carefully checked to ensure proper functionality.

8.2.2.10 Internal Compensation Network

The design equations given in the example circuit can be used to generate circuits using the TPS5450-Q1. These designs are based on certain assumptions and will tend to always select output capacitors within a limited range of ESR values. If a different capacitor type is desired, it may be possible to fit one to the internal compensation of the TPS5450-Q1. 式 15 gives the nominal frequency response of the internal voltage-mode type III compensation network:

$$H(s) = \frac{\left(1 + \frac{s}{2\pi \times Fz1}\right) \times \left(1 + \frac{s}{2\pi \times Fz2}\right)}{\left(\frac{s}{2\pi \times Fp0}\right) \times \left(1 + \frac{s}{2\pi \times Fp1}\right) \times \left(1 + \frac{s}{2\pi \times Fp2}\right) \times \left(1 + \frac{s}{2\pi \times Fp3}\right)} \quad (15)$$

where

- Fp0 = 2165 Hz, Fz1 = 2170 Hz, Fz2 = 2590 Hz
- Fp1 = 24 kHz, Fp2 = 54 kHz, Fp3 = 440 kHz
- Fp3 represents the non-ideal parasitics effect

Using this information along with the desired output voltage, feed forward gain and output filter characteristics, the closed loop transfer function can be derived.

8.2.3 Application Curves

The performance graphs (図 10 through 図 16) are applicable to the circuit in 図 9. T_A = 25 °C. unless otherwise specified.

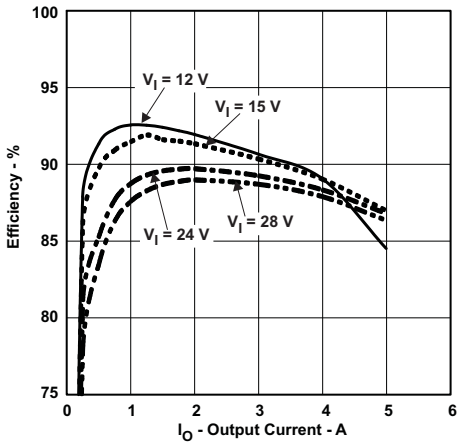


図 10. Efficiency vs Output Current

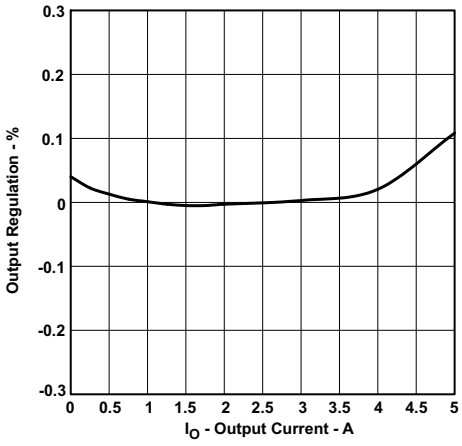


図 11. Output Regulation % vs Output Current

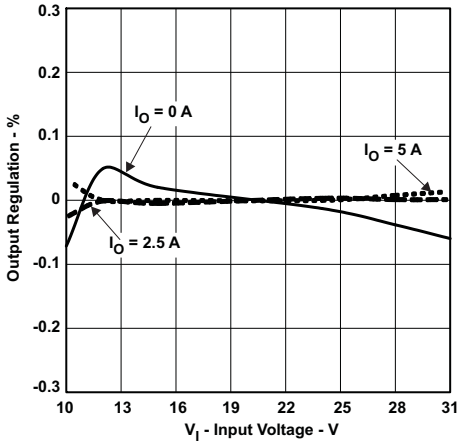
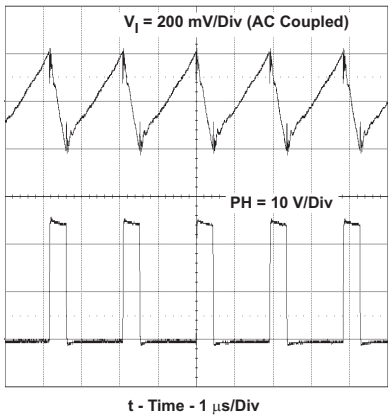
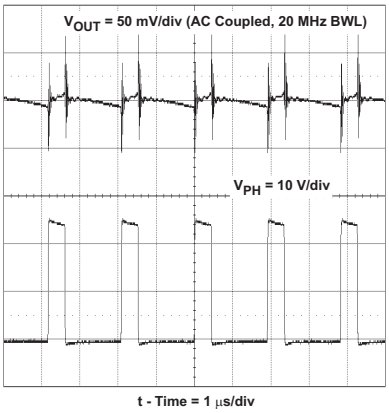


図 12. Output Regulation % vs Input Voltage



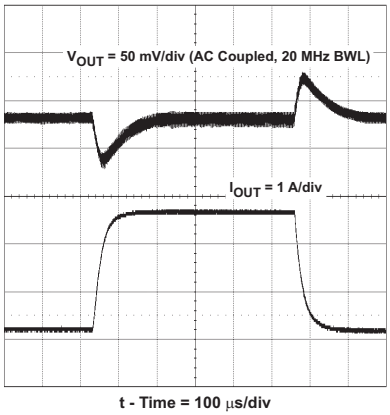
I_{OUT} = 5 A

図 13. Input Voltage Ripple and PH Node



I_{OUT} = 5 A

図 14. Output Voltage Ripple and PH Node



I_{OUT} Step 1.25 To 3.75 A

図 15. Transient Response

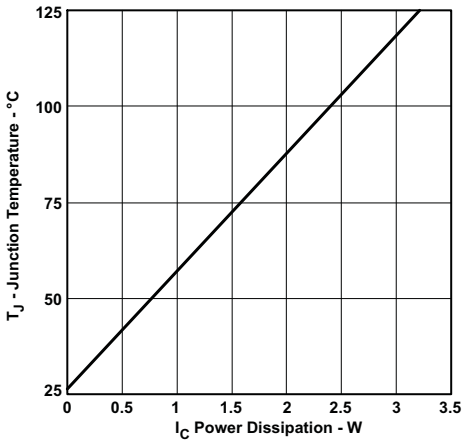


図 16. TPS5450-Q1 Power Dissipation vs Junction Temperature.

9 Layout

9.1 Layout Guidelines

Connect a low ESR ceramic bypass capacitor to the VIN pin. Take care to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the TPS5450-Q1 ground pin. The best way to do this is to extend the top-side ground area from under the device adjacent to the VIN trace, and place the bypass capacitor as close as possible to the VIN pin. The minimum recommended bypass capacitance is 4.7-µF ceramic with a X5R or X7R dielectric.

There must be a ground area on the top layer directly underneath the IC, with an exposed area for connection to the PowerPAD. Use vias to connect this ground area to any internal ground planes. Use additional vias at the ground side of the input and output filter capacitors as well. Tie the GND pin to the PCB ground by connecting it to the ground area under the device as shown below.

Route the PH pin to the output inductor, catch diode, and boot capacitor. Because the PH connection is the switching node, locate the inductor very close to the PH pin and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The catch diode should also be placed close to the device to minimize the output current loop area. Connect the boot capacitor between the phase node and the BOOT pin as shown. Keep the boot capacitor close to the IC and minimize the conductor trace lengths. The component placements and connections shown work well, but other connection routings also may be effective.

Connect the output filter capacitor(s) as shown between the VOUT trace and GND. It is important to keep the loop formed by the PH pin, L_{OUT}, C_{OUT}, and GND as small as is practical.

Connect the VOUT trace to the VSENSE pin using the resistor divider network to set the output voltage. Do not route this trace too close to the PH trace. Due to the size of the IC package and the device pinout, the trace may need to be routed under the output capacitor. Alternately, the routing may be done on an alternate layer if a trace under the output capacitor is not desired.

If using the grounding scheme shown in 図 17, use a via connection to a different layer to route to the ENA pin.

9.2 Layout Examples

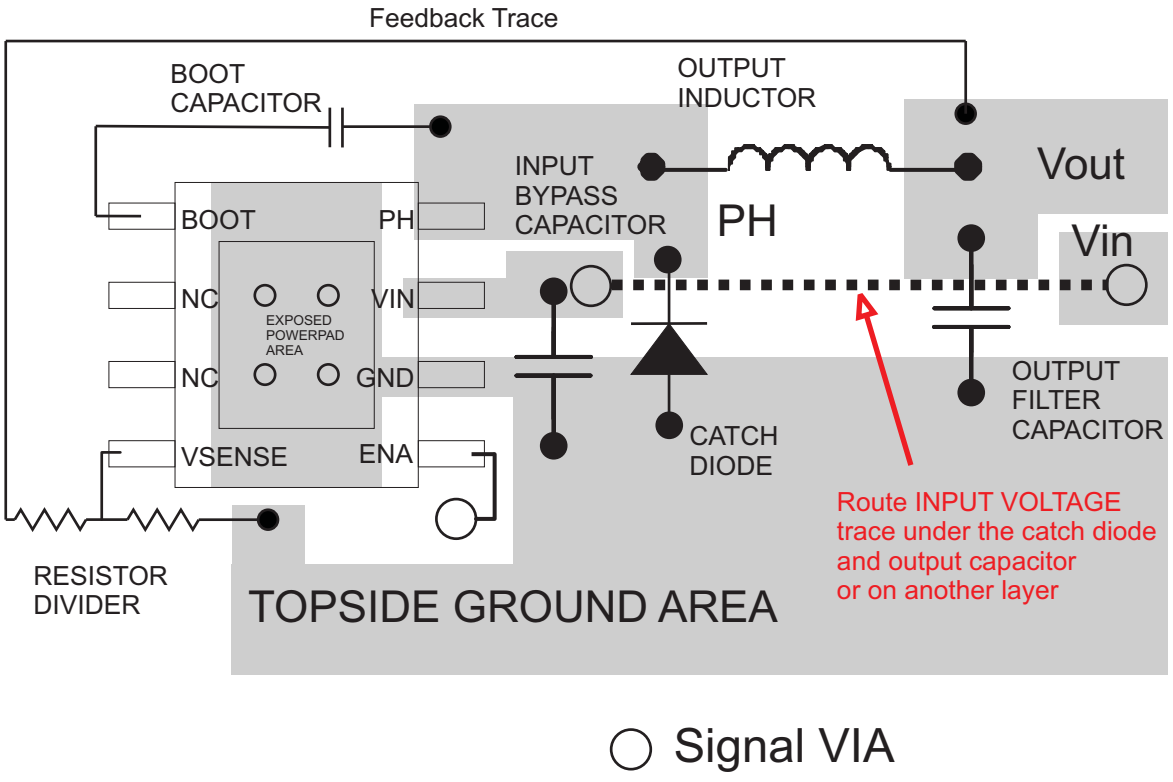


図 17. Design Layout

Layout Examples (continued)

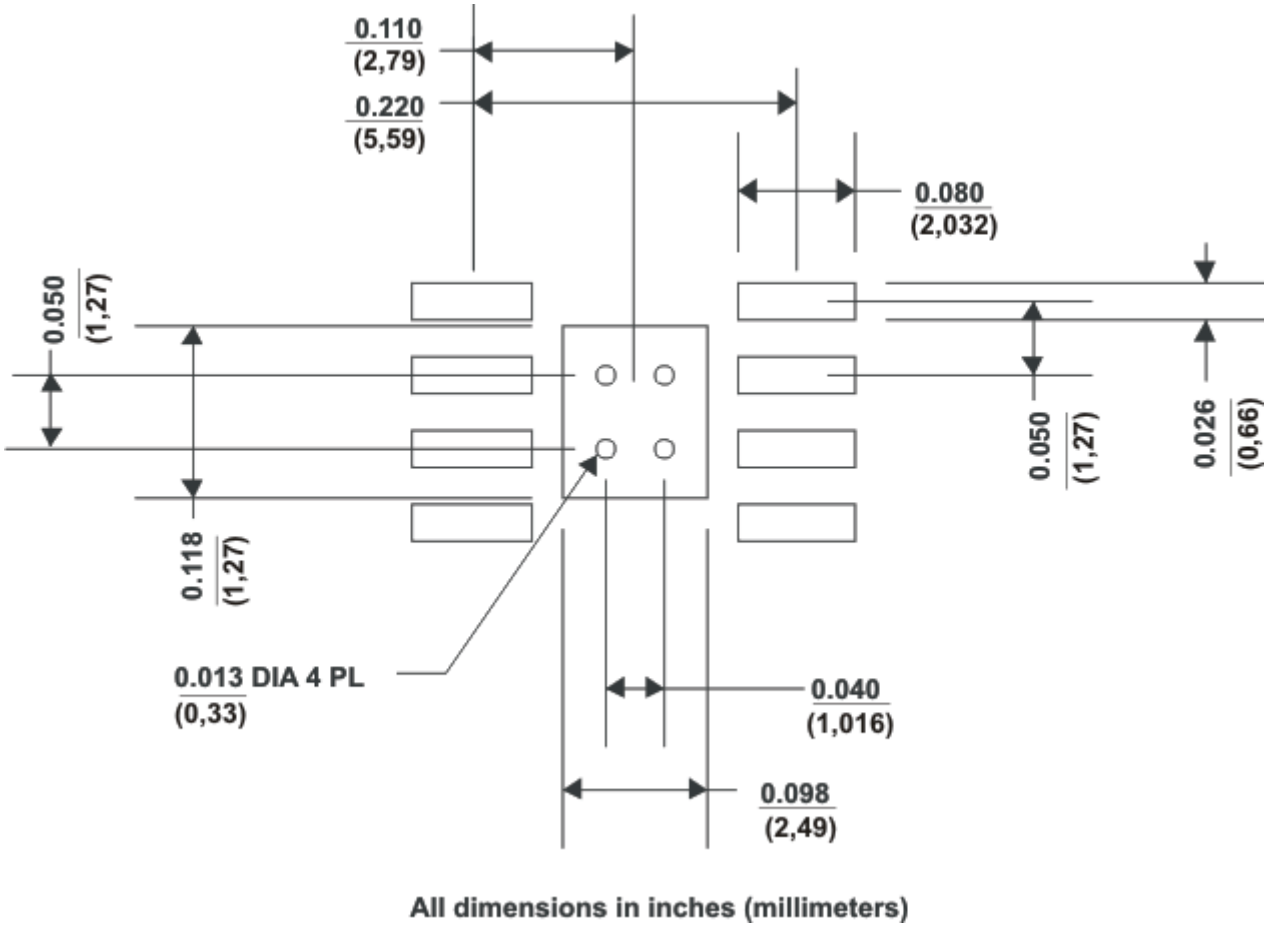


図 18. TPS5450-Q1 Land Pattern

9.3 Thermal Calculations

The following formulas show how to estimate the device power dissipation under continuous conduction mode operations. They should not be used if the device is working at light loads in the discontinuous conduction mode.

Conduction Loss: $Pcon = I_{OUT}^2 \times R_{DS(on)} \times V_{OUT}/V_{IN}$

Switching Loss: $Psw = V_{IN} \times I_{OUT} \times 0.01$

Quiescent Current Loss: $Pq = V_{IN} \times 0.01$

Total Loss: $Ptot = Pcon + Psw + Pq$

Given T_A => Estimated Junction Temperature: $T_J = T_A + Rth \times Ptot$

Given T_{JMAX} = 125°C => Estimated Maximum Ambient Temperature: $T_{AMAX} = T_{JMAX} – Rth \times Ptot$

10 デバイスおよびドキュメントのサポート

10.1 デバイス・サポート

10.1.1 デベロッパー・ネットワークの製品に関する免責事項

デベロッパー・ネットワークの製品またはサービスに関するTIの出版物は、単独またはTIの製品、サービスと一緒に提供される場合に関係なく、デベロッパー・ネットワークの製品またはサービスの適合性に関する是認、デベロッパー・ネットワークの製品またはサービスの是認の表明を意味するものではありません。

10.2 開発サポート

10.2.1 WEBENCH®ツールによるカスタム設計

ここをクリックすると、WEBENCH® Power Designer により、TPS5450-Q1 デバイスを使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他の方式と比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

通常、次の操作を実行可能です。

- 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットで出力する。
- 設計のレポートをPDFで印刷し、設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

10.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

10.5 商標

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WEBENCH is a registered trademark of Texas Instruments.
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10.6 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

10.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS5450QDDARQ1	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	5450Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS5450-Q1 :

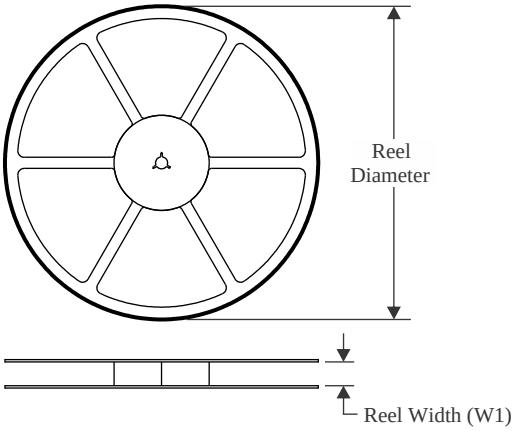
- Catalog : TPS5450
- Enhanced Product : TPS5450-EP

NOTE: Qualified Version Definitions:

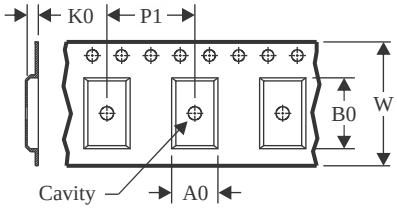
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

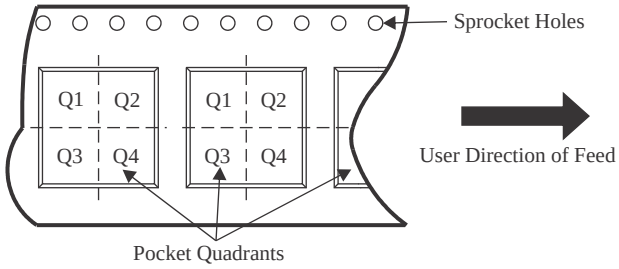


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

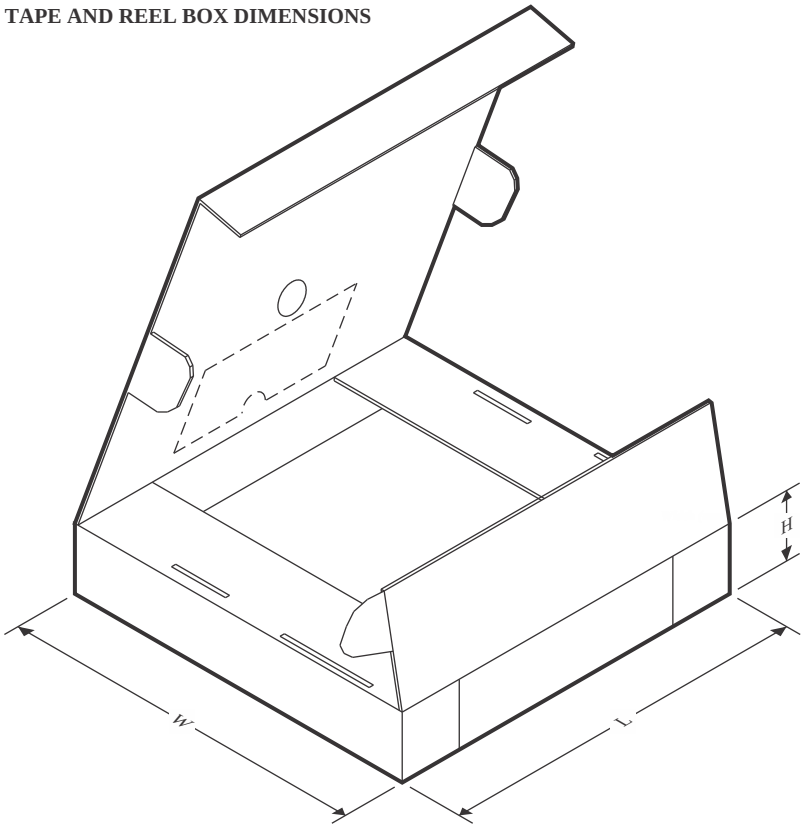
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS5450QDDARQ1	SO PowerPAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

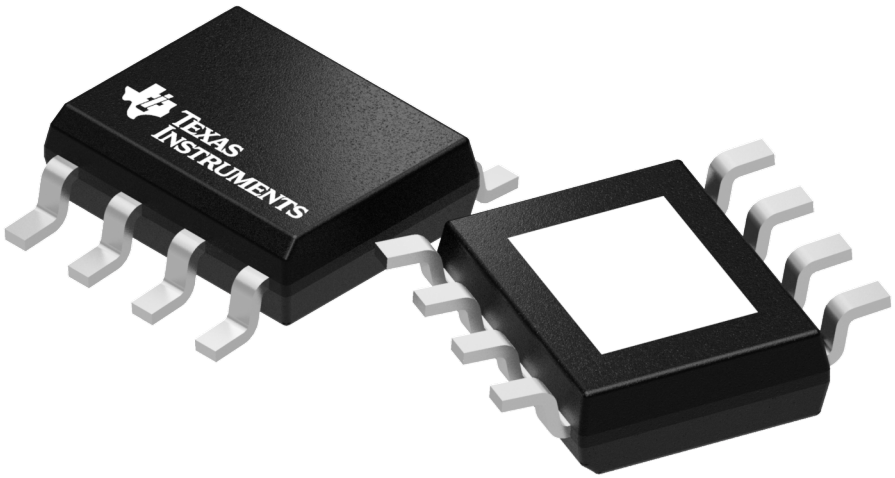


*All dimensions are nominal

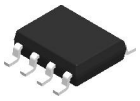
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS5450QDDARQ1	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

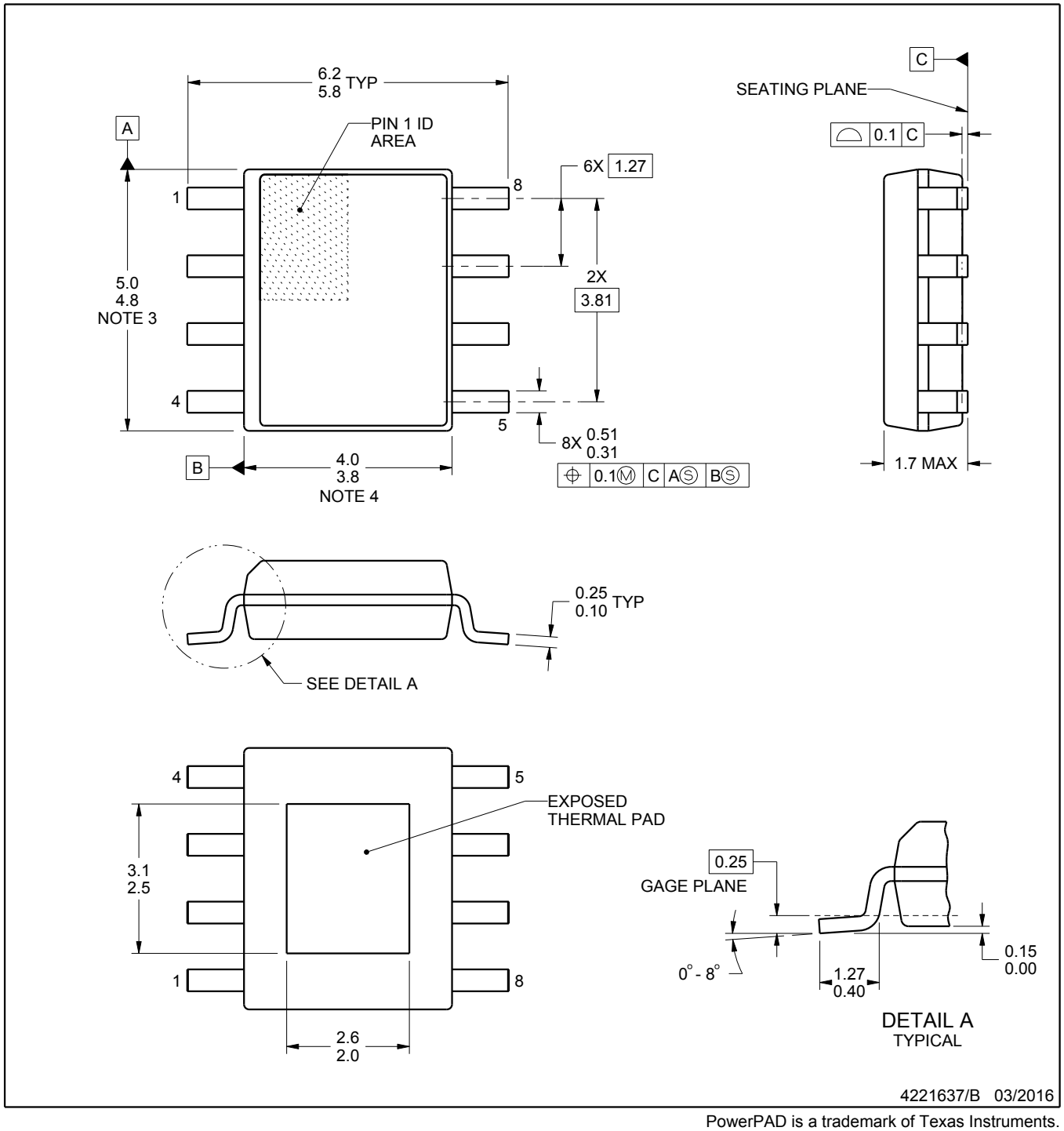


PACKAGE OUTLINE

DDA0008J

PowerPAD™ SOIC - 1.7 mm max height

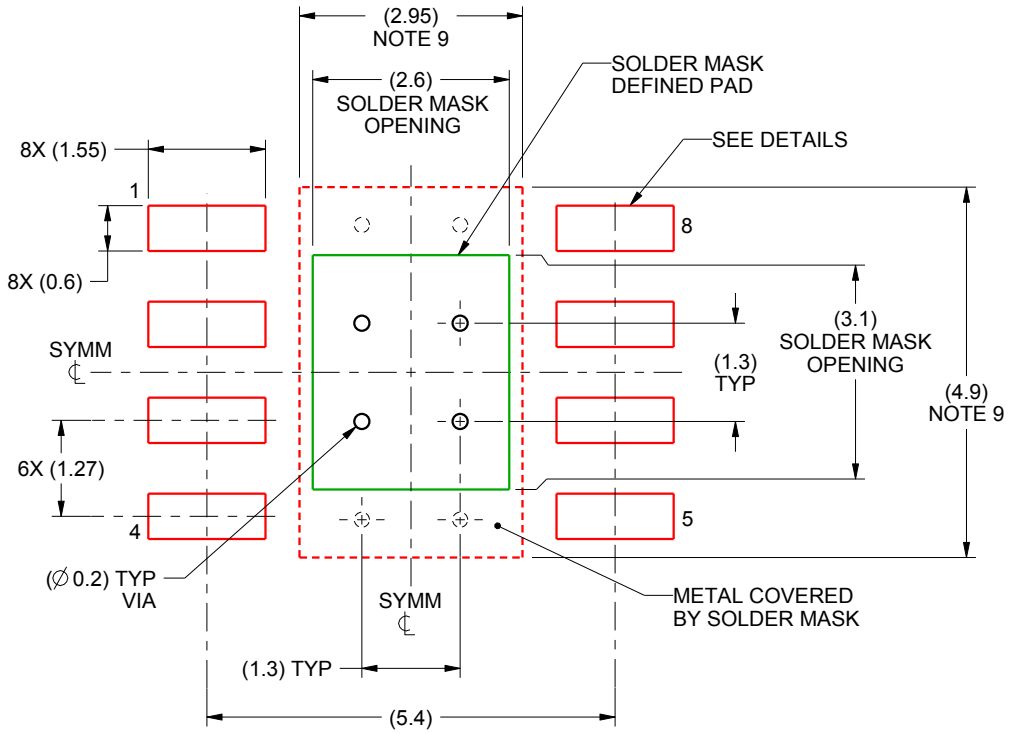
PLASTIC SMALL OUTLINE



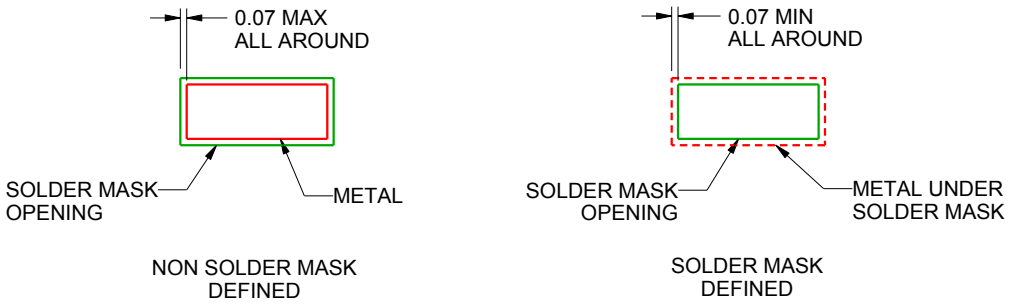
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS

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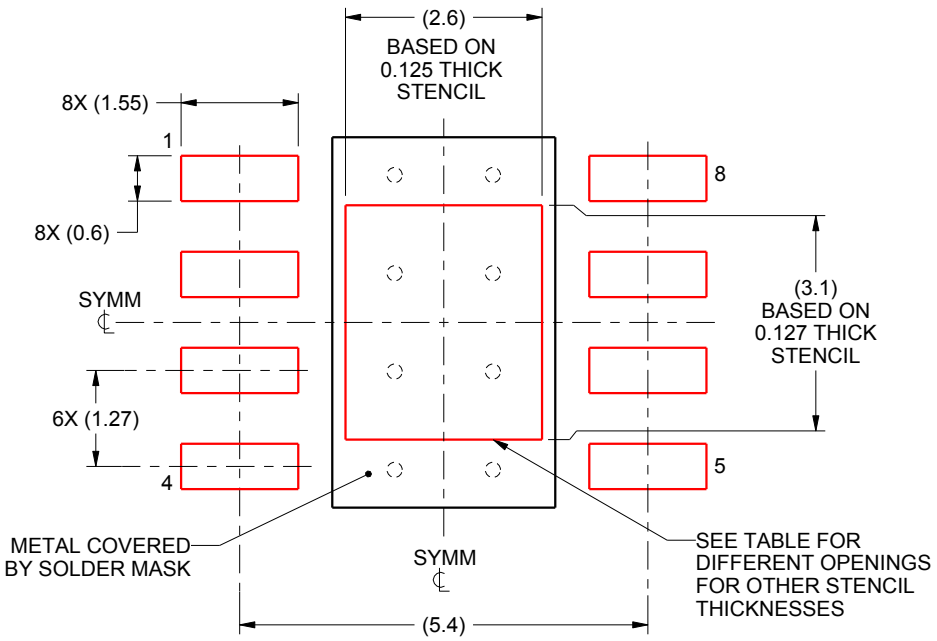
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 3.47
0.125	2.6 X 3.1 (SHOWN)
0.150	2.37 X 2.83
0.175	2.20 X 2.62

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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