参考資料

TEXAS INSTRUMENTS

TPS54525
JAJSLN5B – MAY 2012 – REVISED APRIL 2021

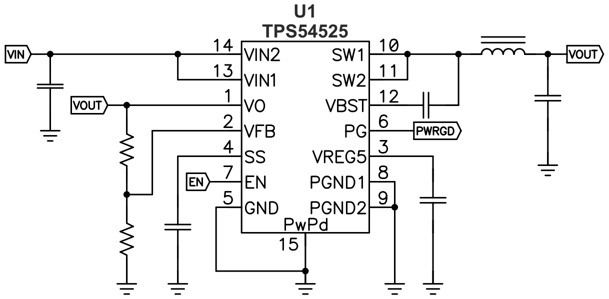
4.5V～18V 入力、5.5A、同期整流式降圧コンバータ

1 特長

- 高速過渡応答を可能にする D-CAP2™ モード
- 低出力リップルで、出力セラミック・コンデンサが使用可能
- 広い V_{IN} 入力電圧範囲：4.5V～18V
- 出力電圧範囲：0.76V～5.5V
- 低デューティ・サイクルのアプリケーションに対して最適化された高効率の内蔵 FET
  – 63mΩ (ハイサイド) および 33mΩ (ローサイド)
- 高効率、シャットダウン時 10μA 未満
- 高い初期バンドギャップ・リファレンス精度
- 調整可能なソフト・スタート
- プリバイアス印加のソフト・スタート
- スイッチング周波数 (f_{SW})：650kHz
- サイクル単位の過電流制限
- パワー・グッド出力

2 アプリケーション

- 幅広い範囲の低電圧システム用アプリケーション
  - デジタル・テレビ用電源
  - 高精細 Blu-ray Disc™ プレーヤ
  - ネットワーク・ホーム・ターミナル
  - デジタル・セットトップ・ボックス (STB)

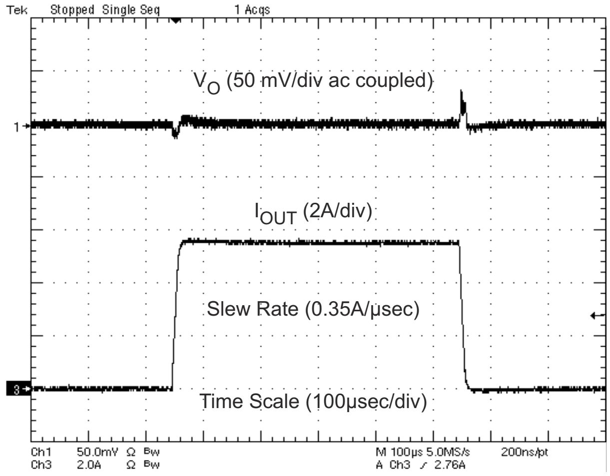


3 概要

TPS54525 は、適応型オン時間、D-CAP2™ モードの同期整流式降圧コンバータです。このデバイスを採用することで、各種機器の電源バス・レギュレータに対して、コスト効果が高く、部品数の少ない、低スタンバイ電流のソリューションを実現できます。本デバイスの主制御ループは、外部補償部品なしで非常に高速な過渡応答が得られる D-CAP2™ モード制御を使用しています。また、低 ESR (等価直列抵抗) の出力コンデンサ (例：POSCAP、SP-CAP) と超低 ESR セラミック・コンデンサの両方をサポートできる独自の回路も備えています。このデバイスは、4.5V ～18V の VIN 入力で動作します。出力電圧は、0.76V～5.5V の範囲でプログラミングできます。また、調整可能なソフト・スタート時間とパワー・グッド機能も備えています。TPS54525 は 14 ピンの HTSSOP パッケージで供給され、–40℃～85℃の温度範囲で動作するよう設計されています。

製品情報

部品番号	パッケージ	本体サイズ
TPS54525	HTSSOP	5.00mm × 6.40mm



English Data Sheet: SLVSB82

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (July 2013) to Revision B (April 2021)	Page
• 以下のセクションを追加。*「ESD 定格」、「機能説明」、「デバイスの機能モード」、「強制連続導通モード」、「アプリケーションと実装」、「アプリケーション情報」、「設計要件」、「詳細な設計手順」、「アプリケーション曲線」、「電源に関する推奨事項」、「レイアウト」、「レイアウト例」、「デバイスおよびドキュメントのサポート」、「メカニカル、パッケージ、および注文情報」*	1
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• Updated 式 2	14

Changes from Revision May 2012 * () to Revision A (July 2013)	Page
• Deleted V_{FBTH} - T_A = 0°C to 85°C, V_O = 1.05 V, continuous mode from the Electrical Characteristics.	5
• Changed V_{FBTH} - T_A = –40°C to 85°C, V_O = 1.05 V, continuous mode From: MIN = 751 MAX = 779 mV To: MIN = 754 MAX = 776 mV in the Electrical Characteristics.	5
• Changed the Over/Under Voltage Protection section. From: "as the high-side MOSFET driver turns off and the low-side MOSFET turns on" To: "as both the high-side and low-side MOSFET drivers turn off"	12

5 Pin Configuration and Functions

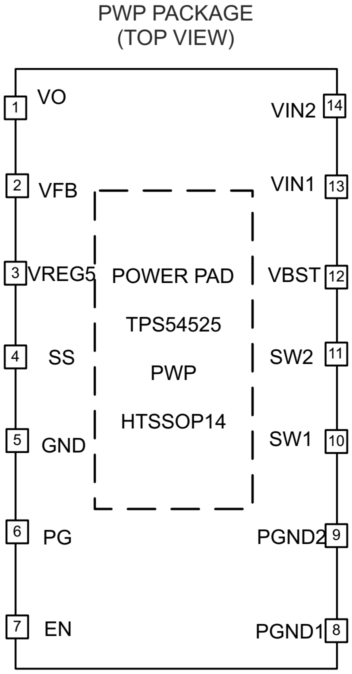


表 5-1. Pin Functions

PIN		DESCRIPTION
NAME	**NO.**	
VO	1	Connect to output of converter. This pin is used for output discharge function.
VFB	2	Converter feedback input. Connect to output voltage with feedback resistor divider.
VREG5	3	5.5 V power supply output. A capacitor (typical 1 µF) should be connected to GND. VREG5 is not active when EN is low.
SS	4	Soft-start control. An external capacitor should be connected to GND.
GND	5	Signal ground pin
PG	6	Open drain power good output
EN	7	Enable control input. EN is active high and must be pulled up to enable the device.
PGND1, PGND2	8, 9	Ground returns for low-side MOSFET. Also serve as inputs of current comparators. Connect PGND and GND strongly together near the IC.
SW1, SW2	10, 11	Switch node connection between high-side NFET and low-side NFET. Also serve as inputs to current comparators.
VBST	12	Supply input for high-side NFET gate driver (boost terminal). Connect capacitor from this pin to respective SW1, SW2 terminals. An internal PN diode is connected between VREG5 to VBST pin.
VIN1, VIN2	13, 14	Power input and connected to high side NFET drain. Supply input for 5-V internal linear regulator for the control circuitry.
PowerPAD™	Back side	Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Should be connected to PGND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage range	VIN1, VIN2 EN	–0.3	20	V
	VBST	–0.3	26	V
	VBST (10 ns transient)	–0.3	28	V
	VBST (vs SW1, SW2)	–0.3	6.5	V
	VFB, VO, SS, PG	–0.3	6.5	V
	SW1, SW2	–2	20	V
	SW1, SW2 (10 ns transient)	–3	22	V
Output voltage range	VREG5	–0.3	6.5	V
	PGND1, PGND2	–0.3	0.3	V
Voltage from GND to PowerPAD™, V_{diff}		–0.2	0.2	V
Operating junction temperature, T_J		–40	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE		UNIT
			MIN	MAX	
Storage temperature, T_{stg}			-55	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	-2000	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	-500	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Supply input voltage range		4.5	18	V
V_I	Input voltage range	VBST	–0.3	24	V
		VBST(10 ns transient)	–0.3	27	
		VBST (vs SW1, SW2)	-0.3	5.7	
		SS, PG	–0.3	5.7	
		EN	–0.3	18	
		VO, VFB	–0.3	5.5	
		SW1, SW2	–1.8	18	
		SW1, SW2 (10 ns transient)	–3	21	
		PGND1, PGND2	–0.3	0.1	
V_O	Output voltage range	VREG5	–0.3	5.7	V
I_O	Output Current range	I_{VREG5}	0	5	mA
T_A	Operating free-air temperature		–40	85	°C
T_J	Operating junction temperature		–40	150	°C

6.4 Thermal Information

THERMAL METRIC		TPS54525	UNITS
		PWP	
		14 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	43.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	33.1	
θ_{JB}	Junction-to-board thermal resistance	28.4	
ψ_{JT}	Junction-to-top characterization parameter	1.3	
ψ_{JB}	Junction-to-board characterization parameter	28.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	4.7	

6.5 Electrical Characteristics

over operating free-air temperature range, V_{IN} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VIN}	Operating - non-switching supply current	V_{IN} current, T_A = 25°C, EN = 5 V, V_{VFB} = 0.8 V		900	1400	µA
I_{VINSDN}	Shutdown supply current	V_{IN} current, T_A = 25°C, EN = 0 V		3.6	10	µA
LOGIC THRESHOLD						
V_{ENH}	EN high-level input voltage		1.6			V
V_{ENL}	EN low-level input voltage				0.6	V
R_{EN}	EN pin resistance to GND	V_{EN} = 12 V	220	440	880	kΩ
VFB VOLTAGE AND DISCHARGE RESISTANCE						
V_{FBTH}	VFB threshold voltage	T_A = 25°C, V_O = 1.05 V, continuous mode	757	765	773	mV
		T_A = –40°C to 85°C, V_O = 1.05 V, continuous mode(1)	754		776	
I_{VFB}	VFB input current	V_{VFB} = 0.8 V, T_A = 25°C		0	±0.15	µA
R_{Dischg}	V_O discharge resistance	V_{EN} = 0 V, V_O = 0.5 V, T_A = 25°C		50	100	Ω
VREG5 OUTPUT						

over operating free-air temperature range, V_{IN} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VREG5}	VREG5 output voltage	T_A = 25°C, 6.0 V < V_{IN} < 18 V, 0 < I_{VREG5} < 5 mA	5.2	5.5	5.7	V
V_{VREG5}	VREG5 Line regulation	6.0 V < V_{IN} < 18 V, I_{VREG5} = 5 mA			20	mV
V_{VREG5}	VREG5 Load regulation	0 mA < I_{VREG5} < 5 mA			100	mV
I_{VREG5}	VREG5 Output current	V_{IN} = 6 V, V_{VREG5} = 4 V, T_A = 25°C		60		mA
MOSFET						
R_{dsonh}	High side switch resistance	T_A = 25°C, V_{BST} - $V_{SW1,2}$ = 5.5 V		63		mΩ
R_{dsonl}	Low side switch resistance	T_A = 25°C		33		mΩ
CURRENT LIMIT						
I_{ocl}	Current limit	L_{OUT} = 1.5 µH(1)	6.1	6.9	8.4	A
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature (1)		165		°C
		Hysteresis (1)		35		
ON-TIME TIMER CONTROL						
T_{ON}	On time	V_{IN} = 12 V, V_O = 1.05 V		155		ns
$T_{OFF(MIN)}$	Minimum off time	T_A = 25°C, V_{VFB} = 0.7 V		260	330	ns
SOFT START						
I_{SSC}	SS charge current	V_{SS} = 1 V	4.2	6.0	7.8	µA
I_{SSD}	SS discharge current	V_{SS} = 0.5 V	0.1	0.2		mA
POWER GOOD						
V_{THPG}	PG threshold	V_{VFB} rising (good)	85	90	95	%
		V_{VFB} falling (fault)		85		%
I_{PG}	PG sink current	V_{PG} = 0.5 V	2.5	5		mA
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP trip threshold	OVP detect	120	125	130	%
T_{OVPDEL}	Output OVP prop delay			10		µs
V_{UVP}	Output UVP trip threshold	UVP detect	60	65	70	%
		Hysteresis		10		%
T_{UVPDEL}	Output UVP delay			0.25		ms
T_{UVPEN}	Output UVP enable delay	Relative to soft-start time		x 1.7		
UVLO						
V_{UVLO}	UVLO threshold	Wake up VREG5 voltage	3.31	3.61	3.91	V
		Fall VREG5 voltage	2.82	3.12	3.42	
		Hysteresis VREG5 voltage	0.37	0.49	0.61	

(1) Not production tested.

6.6 Typical Characteristics

V_{IN} = 12 V, T_A = 25 °C (unless otherwise noted)

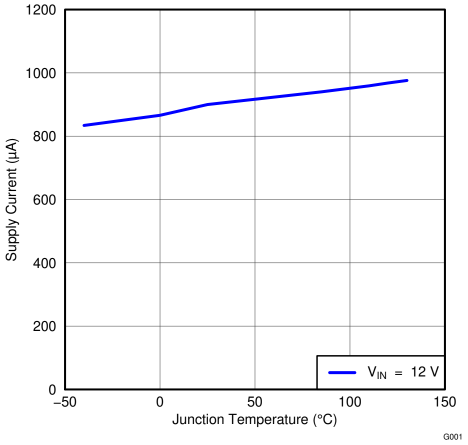


図 6-1. V_{IN} Current vs Junction Temperature

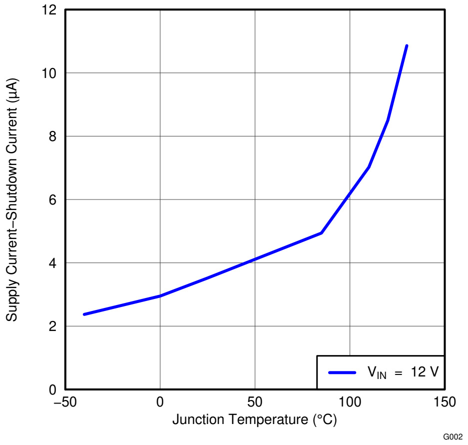


図 6-2. V_{IN} Shutdown Current vs Junction Temperature

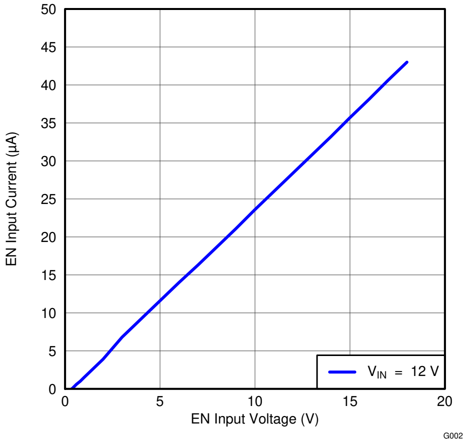


図 6-3. EN Current vs EN Voltage

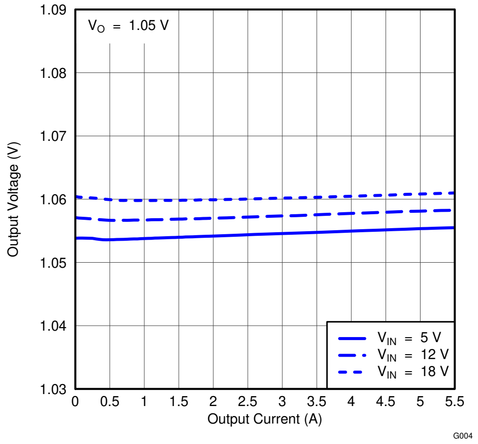


図 6-4. 1.05-V Output Voltage vs Output Current

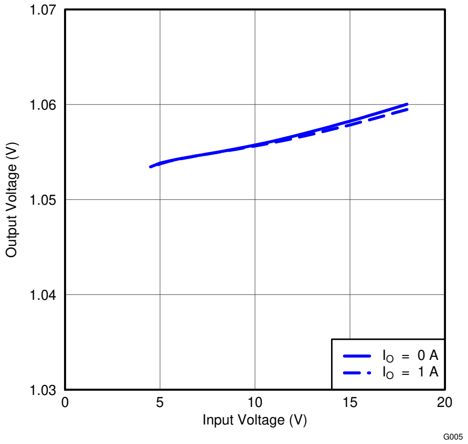


図 6-5. 1.05-V Output Voltage vs Input Voltage

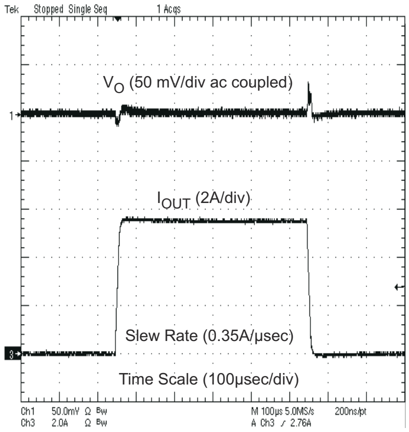


図 6-6. 1.05-V, 50-mA to 5.5-A Load Transient Response

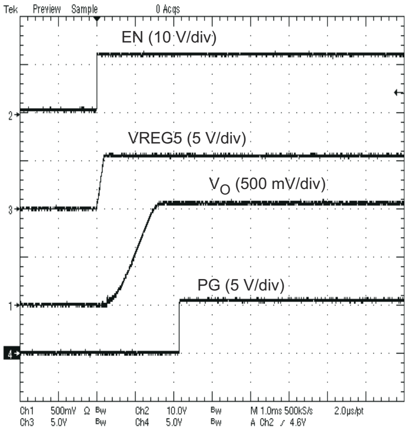


図 6-7. Start-Up Waveform

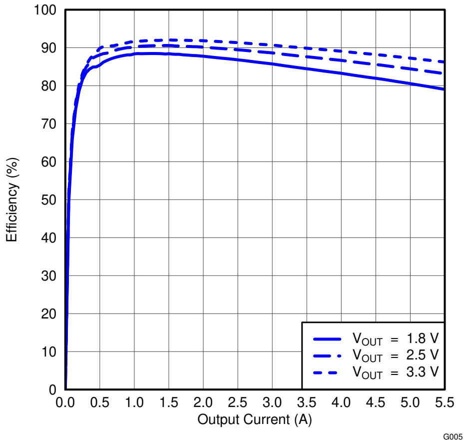


図 6-8. Efficiency vs Output Current

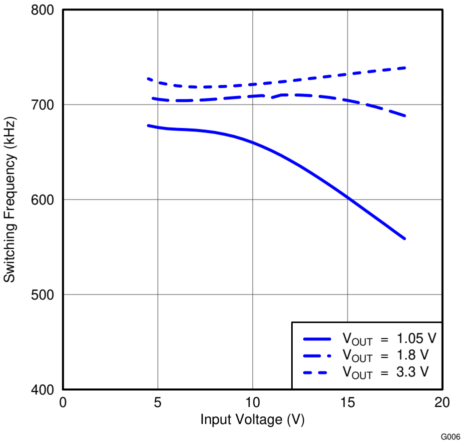


図 6-9. Switching Frequency vs Input Voltage (I_O = 1 A)

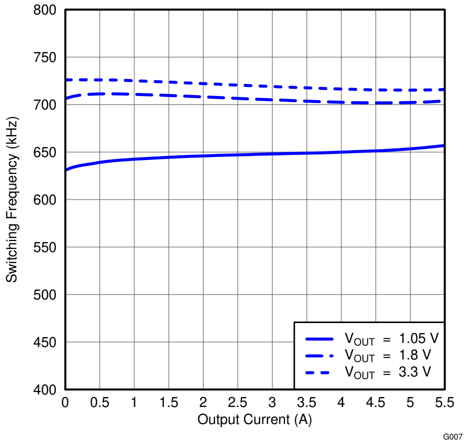


図 6-10. Switching Frequency vs Output Current

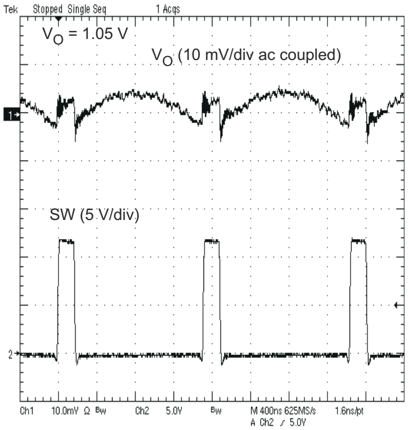


図 6-11. Voltage Ripple at Outptut (I_O = 5.5 A)

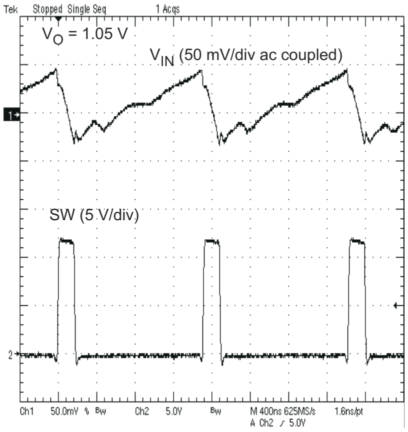


図 6-12. Voltage Ripple at Input (I_O = 5.5 A)

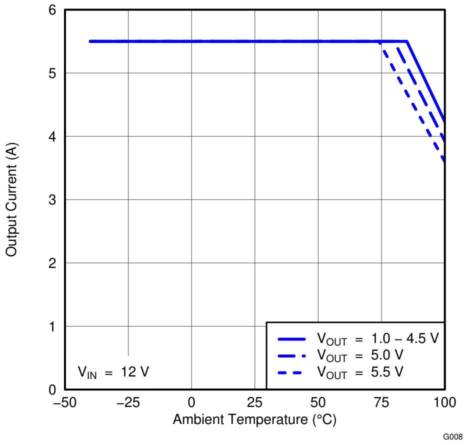


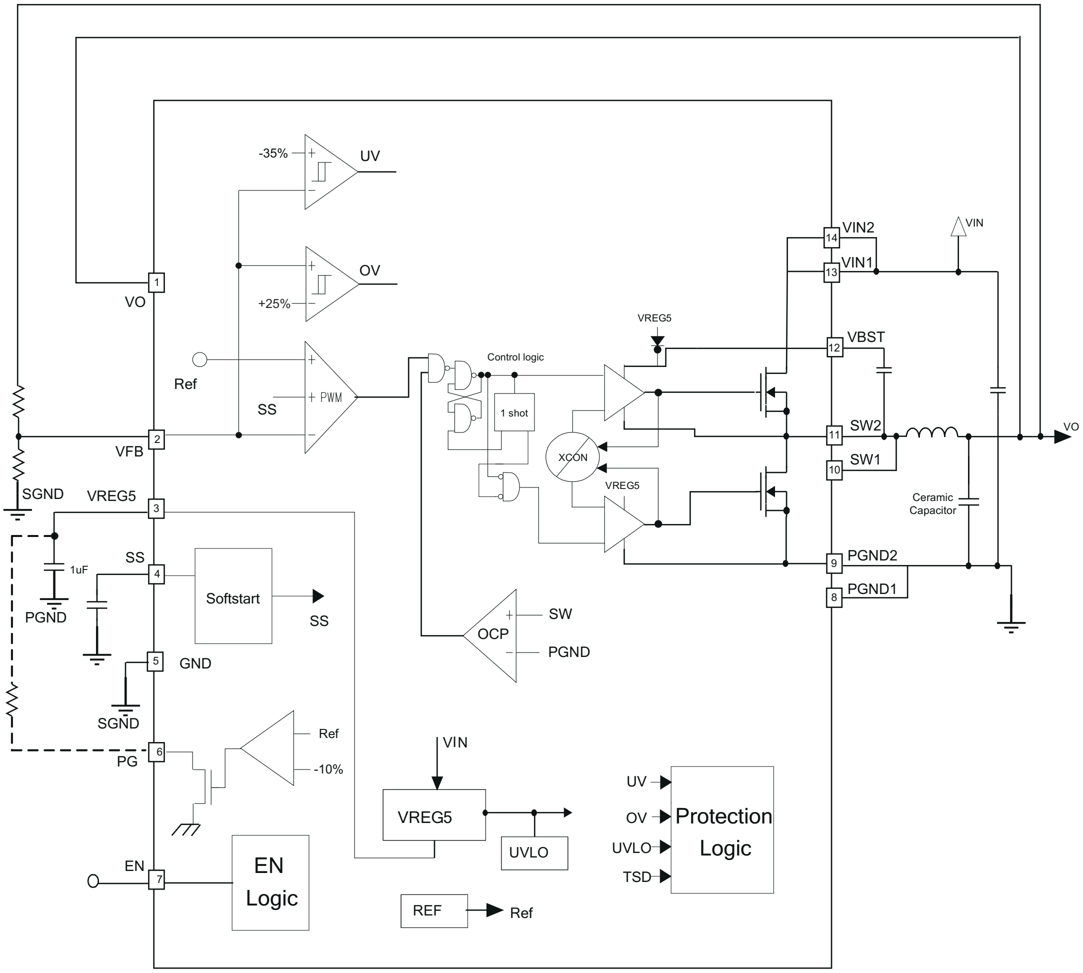
図 6-13. Output Current vs Ambient Temperature

7 Detailed Description

7.1 Overview

The TPS54525 is a 5.5-A synchronous step-down (buck) converter with two integrated N-channel MOSFETs. It operates using D-CAP2™ mode control. The fast transient response of D-CAP2™ control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Operation

The main control loop of the TPS54525 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. D-CAP2™ mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot is set by the converter input voltage, VIN, and the output voltage, VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

7.3.2 PWM Frequency and Adaptive On-Time Control

TPS54525 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS54525 runs with a pseudo-constant frequency of 650 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage, therefore, when the duty ratio is VOUT/VIN, the frequency is constant.

7.3.3 Soft Start and Pre-Biased Soft Start

The soft start function is adjustable. When the EN pin becomes high, 6-µA current begins charging the capacitor which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start up. The equation for the slow start time is shown in 式 1. VFB voltage is 0.765 V and SS pin source current is 6 µA.

$$t_{SS}(ms) = \frac{C_{SS}(nF) \text{ x } V_{REF} \times 1.1}{I_{SS}(\mu A)} = \frac{C_{SS}(nF) \text{ x } 0.765 \times 1.1}{6} \quad (1)$$

The TPS54525 contains a unique circuit to prevent current from being pulled from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft start becomes greater than feedback voltage V_{FB}), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensure that the out voltage (VO) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

7.3.4 Power Good

The TPS54525 has power-good open drain output. The power good function is activated after soft start has finished. The power good function becomes active after 1.7 times soft-start time. When the output voltage is within -10% of the target value, internal comparators detect power good state and the power good signal becomes high. Rpg resister value ,which is connected between PG and VREG5, is required from 25kΩ to 150kΩ. If the feedback voltage goes under 15% of the target value, the power good signal becomes low.

7.3.5 VREG5

VREG5 is an internally generated voltage source used by the TPS54525. It is derived directly from the input voltage and is nominally regulated to 5.5 V when the input voltage is above 5.6 V. The output of the VREG5 regulator is the input to the internal UVLO function. VREG5 must be above the UVLO wake up threshold voltage (3.6 V typical) for the TPS54525 to function. Connect a 1 µF capacitor between pin 3 of the TPS54525 and power ground for proper regulation of the VREG5 output. The VREG5 output voltage is available for external use. It is recommended to use no more than 5 mA for external loads. The VREG5 output is disabled when the TPS54525 EN pin is open or pulled low.

7.3.6 Output Discharge Control

TPS54525 discharges the output when EN is low, or the controller is turned off by the protection functions (OVP, UVP, UVLO and thermal shutdown). The output is discharged by an internal 50-Ω MOSFET which is connected from VO to PGND. The internal low-side MOSFET is not turned on during the output discharge operation to avoid the possibility of causing negative voltage at the output.

7.3.7 Current Protection

The output overcurrent protection (OCP) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the SW pin and GND. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by V_{IN}, V_{OUT}, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT}. If the measured voltage is above the voltage proportional to the current limit, Then , the device constantly monitors the low-side FET switch voltage, which is proportional to the switch current, during the low-side on-time.

The converter maintains the low-side switch on until the measured voltage is below the voltage corresponding to the current limit at which time the switching cycle is terminated and a new switching cycle begins. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of overcurrent protection. The load current one half of the peak-to-peak inductor current higher than the overcurrent threshold. Also when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output undervoltage protection circuit to be activated. When the over current condition is removed, the output voltage returns to the regulated value. This protection is non-latching.

7.3.8 Over/Under Voltage Protection

TPS54525 monitors a resistor divided feedback voltage to detect over and under voltage. When the feedback voltage becomes higher than 125% of the target voltage, the OVP comparator output goes high and the circuit latches as both the high-side and low-side MOSFET drivers turn off. When the feedback voltage becomes lower than 65% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins. After 250 μs, the device latches off both internal top and bottom MOSFET. This function is enabled approximately 1.7 x softstart time.

7.3.9 UVLO Protection

Undervoltage lock out protection (UVLO) monitors the voltage of the V_{REG5} pin. When the V_{REG5} voltage is lower than UVLO threshold voltage, the TPS54525 is shut off. This is protection is non-latching.

7.3.10 Thermal Shutdown

TPS54525 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 165°C), the device is shut off. This is non-latch protection.

7.4 Device Functional Modes

7.4.1 Forced CCM Mode

The TPS54525 operates in Forced CCM (FCCM) mode, which keeps the converter operating in continuous current mode during light-load conditions and allows the inductor current to become negative. During FCCM mode, the switching frequency (FSW) is maintained at an almost constant level over the entire load range, which is suitable for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load.”

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

図 8-1 shows a typical application for TPS54525 with 1.05-V output. This design converts an input voltage range of 4.5 V to 18 V down to 1.05 V with a maximum output current of 5.5 A.

8.2 Typical Application

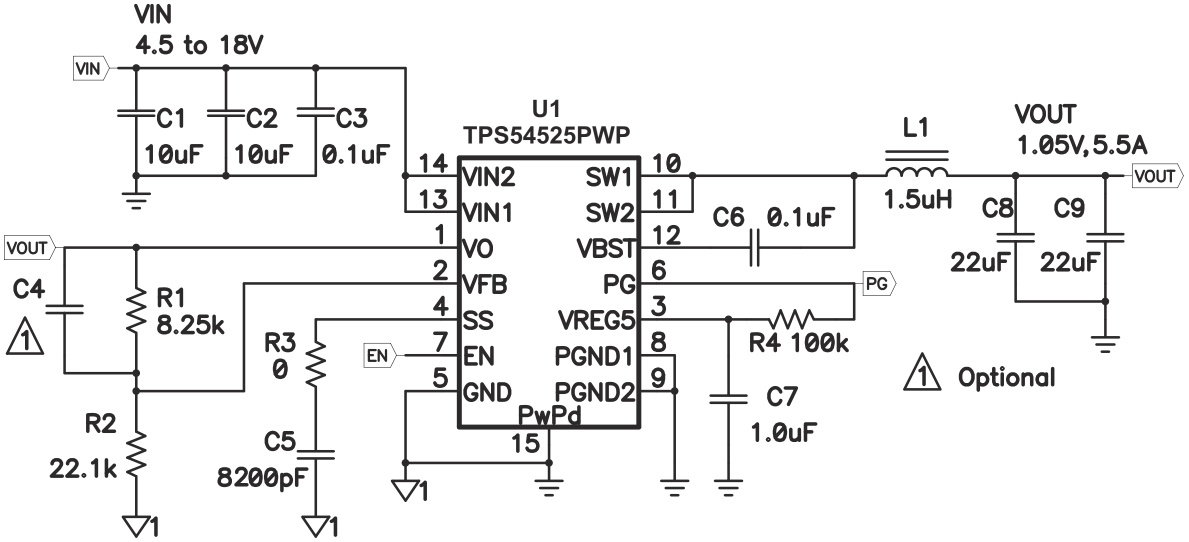


図 8-1. Schematic Diagram

8.2.1 Design Requirements

For this design example, use the following input parameters:

表 8-1. Design Parameters

PARAMETER	VALUE
Input voltage range	4.5 V – 18 V
Output voltage	1.05 V
Output current rating	0 A – 5.5 A
Output voltage ripple	7 mV_{PP} (12 V_{IN} / 5.5 A)

8.2.2 Detailed Design Procedure

8.2.2.1 Step By Step Design Procedure

To begin the design process, you must know a few application parameters:

- Input voltage range
- Output voltage
- Output current
- Output voltage ripple
- Input voltage ripple

8.2.2.2 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using 式 2 to calculate V_{OUT}.

To improve efficiency at very light loads consider using larger value resistors, too high of resistance will be more susceptible to noise and voltage errors from the VFB input current will be more noticeable.

$$V_{OUT} = (0.7651 - 0.0011 \times VOUT\_SET) \times \left(1 + \frac{R1}{R2}\right)$$

$$\text{where } VOUT\_SET \text{ is target VOUT voltage} \tag{2}$$

8.2.2.3 Output Filter Selection

The output filter used with the TPS54525 is an LC circuit. This LC filter has double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \tag{3}$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS54525. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a -40 dB per decade rate and the phase drops rapidly. D-CAP2™ introduces a high frequency zero that reduces the gain roll off to -20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of 式 3 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in 表 8-2

表 8-2. Recommended Component Values

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	C4 (pF)(1)	L1 (µH)	C8 + C9 (µF)
1	6.81	22.1		1.0 - 1.5	22 - 68
1.05	8.25	22.1		1.0 - 1.5	22 - 68
1.2	12.7	22.1		1.0 - 1.5	22 - 68
1.5	21.5	22.1		1.5	22 - 68
1.8	30.1	22.1	5 - 22	1.5	22 - 68
2.5	49.9	22.1	5 - 22	2.2	22 - 68
3.3	73.2	22.1	5 - 22	2.2	22 - 68
5	124	22.1	5 - 22	3.3	22 - 68

(1) Optional

For higher output voltages at or above 1.8 V, additional phase boost can be achieved by adding a feed forward capacitor (C4) in parallel with R1.

Since the DC gain is dependent on the output voltage, the required inductor value will increase as the output voltage increases. For higher output voltages at or above 1.8 V, additional phase boost can be achieved by adding a feed forward capacitor (C4) in parallel with R1

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using 式 4, 式 5 and 式 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 650 kHz for f_{SW}.

Use 650 kHz for f_{SW}. Make sure the chosen inductor is rated for the peak current of 式 5 and the RMS current of 式 6.

$$Ilp - p = \frac{V_{OUT}}{V_{IN\,(max)}} \bullet \frac{V_{IN\,(max)} - V_{OUT}}{L_O \bullet f_{SW}} \tag{4}$$

$$I_{lpeak} = I_O + \frac{Ilp - p}{2} \tag{5}$$

$$I_{Lo(RMS)} = \sqrt{I_O^{\,2} + \frac{1}{12} Ilp - p^2} \tag{6}$$

For this design example, the calculated peak current is 6.01 A and the calculated RMS current is 5.5 A. The inductor used is a TDK SPM6530-1R5M100 with a peak current rating of 11.5 A and an RMS current rating of 11 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS54525 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 22uF to 68uF. Use 式 7 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \bullet (V_{IN} - V_{OUT})}{\sqrt{12} \bullet V_{IN} \bullet L_O \bullet f_{SW}} \tag{7}$$

For this design two TDK C3216X5R0J226M 22uF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.284 A and each output capacitor is rated for 4A.

8.2.2.4 Input Capacitor Selection

The TPS54525 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 μF is recommended for the decoupling capacitor. An additional 0.1 μF capacitor from pin 14 to ground is recommended to improve the EMI performance. The capacitor voltage rating needs to be greater than the maximum input voltage.

8.2.2.5 Bootstrap Capacitor Selection

A 0.1 μF ceramic capacitor must be connected between the VBST to SW pin for proper operation. It is recommended to use a ceramic capacitor.

8.2.2.6 VREG5 Capacitor Selection

A 1.0 μF ceramic capacitor must be connected between the VREG5 to GND pin for proper operation. It is recommended to use a ceramic capacitor.

8.2.3 Application Curves

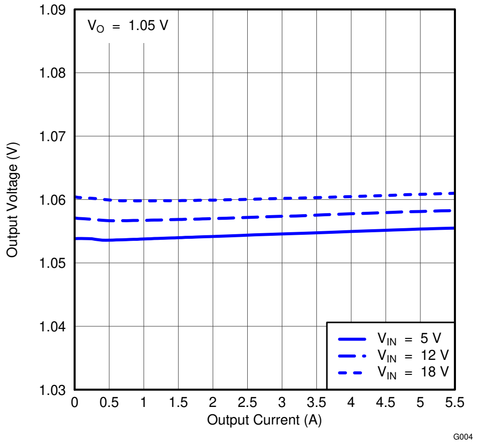


図 8-2. 1.05-V Output Voltage vs Output Current

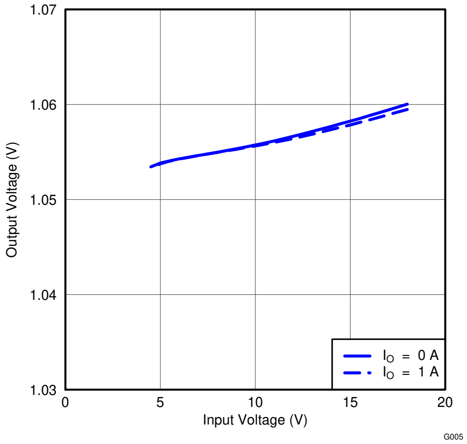


図 8-3. 1.05-V Output Voltage vs Input Voltage

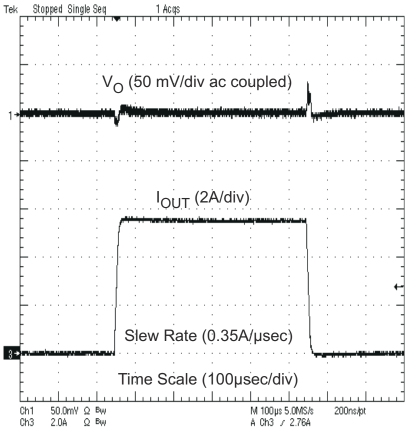


図 8-4. 1.05-V, 50-mA to 5.5-A Load Transient Response

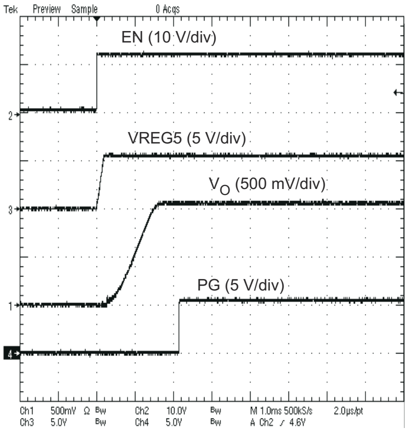


図 8-5. Start-Up Waveform

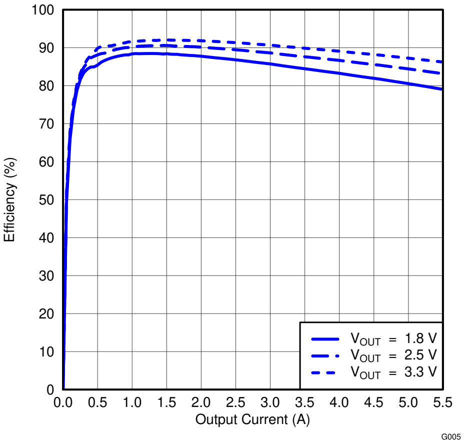


図 8-6. Efficiency vs Output Current

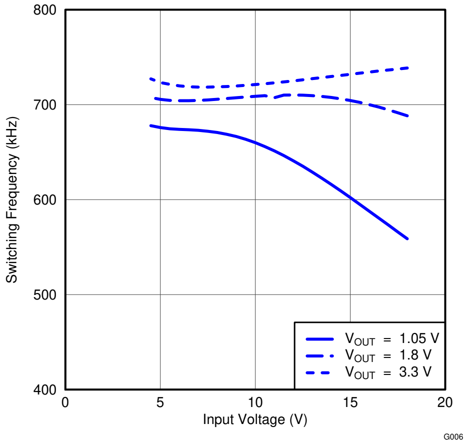


図 8-7. Switching Frequency vs Input Voltage (I_O = 1 A)

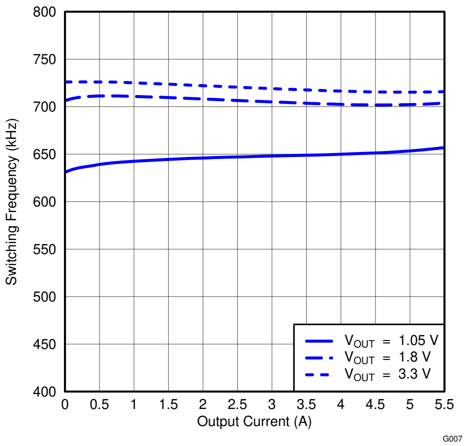


図 8-8. Switching Frequency vs Output Current

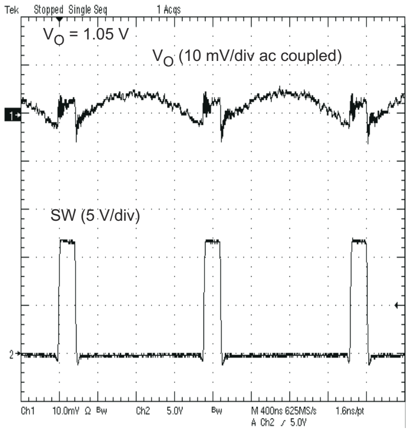


図 8-9. Voltage Ripple at Outptut (I_O = 5.5 A)

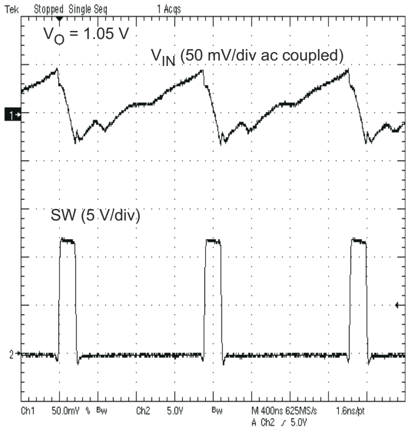


図 8-10. Voltage Ripple at Input (I_O = 5.5 A)

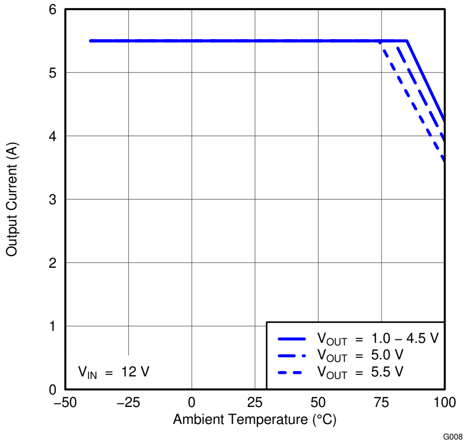


図 8-11. Output Current vs Ambient Temperature

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 4.5 V and 18 V. This input supply should be well regulated. If the input supply is located more than a few inches from the TPS54525 converter additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

- Keep the input switching current loop as small as possible.
- Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin of the device.
- Keep analog and non-switching components away from switching components.
- Make a single point connection from the signal ground to power ground.
- Do not allow switching current to flow under the device.
- VREG5 capacitor should be placed near the device, and connected PGND.
- Output capacitor should be connected to a broad pattern of the PGND.
- Voltage feedback loop should be as short as possible, and preferably with ground shield.
- Lower resistor of the voltage divider which is connected to the VFB pin should be tied to SGND.
- Providing sufficient via is preferable for VIN, SW and PGND connection.
- PCB pattern for VIN and SW should be as broad as possible.
- VIN Capacitor should be placed as near as possible to the device.
- The top side power ground (PGND) copper fill area near the IC should be as large as possible. This will aid in thermal dissipation as well lower conduction losses in the ground return
- Exposed pad of device must be connected to PGND with solder. The PGND area under the IC should be as large as possible and completely cover the exposed thermal pad. The bottom side of the board should contain a large copper area under the device that is directly connected to the exposed area with small diameter vias. Small diameter vias will prevent solder from being drawn away from the exposed thermal pad. Any additional internal layers should also contain copper ground areas under the device and be connected to the thermal vias.

10.2 Layout Guidelines

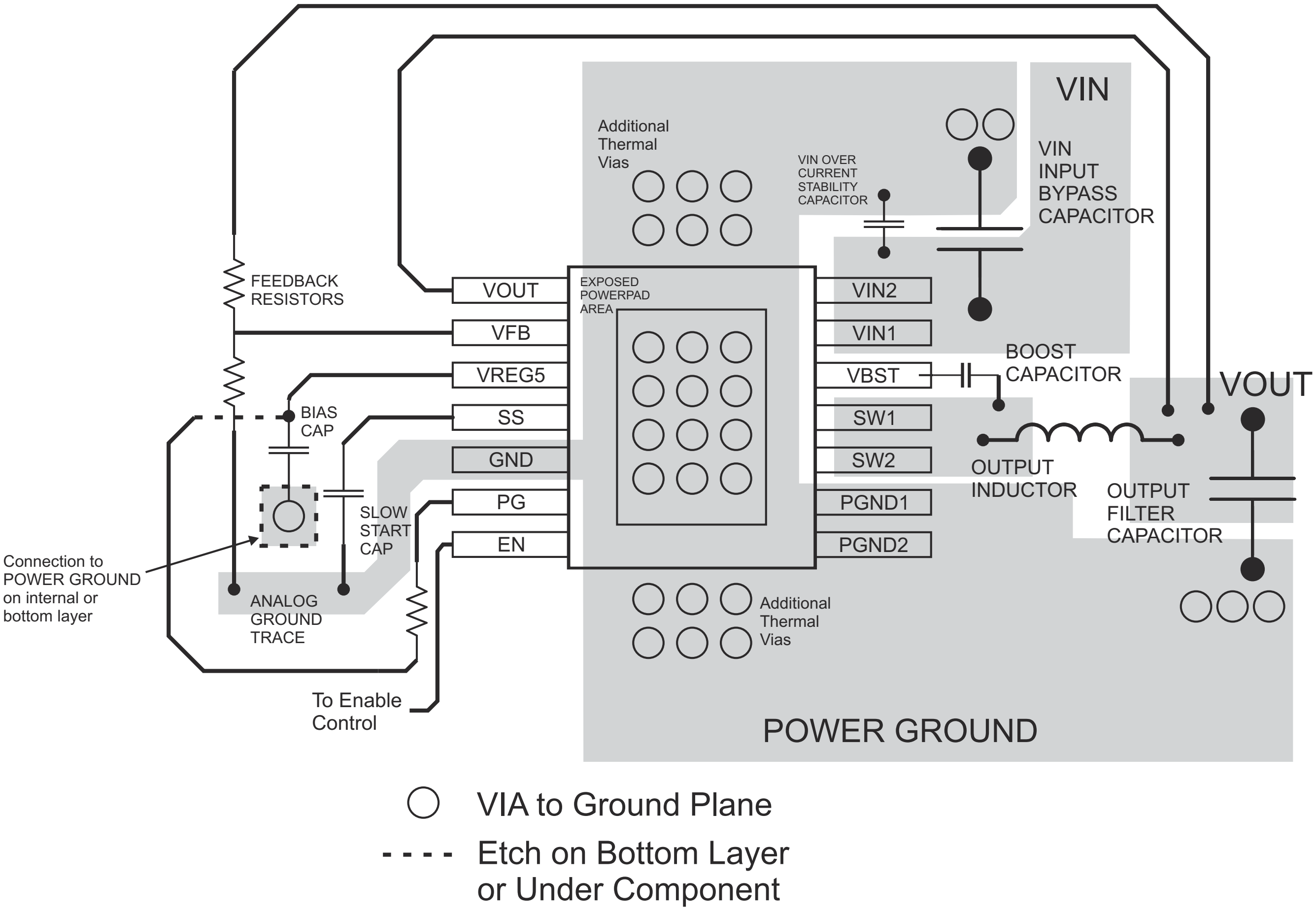


図 10-1. PCB Layout

10.2.1 Thermal Considerations

This PowerPad™ package incorporates an exposed thermal pad that is designed to be directly to an external heartsick. The thermal pad must be soldered directly to the printed board (PCB). After soldering, the PCB can be used as a heartsick. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heartsick structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD™ package and how to use the advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD™ Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD™ Made Easy, Texas Instruments Literature No. SLMA004.

The exposed thermal pad dimensions for this package are shown in the following illustration.

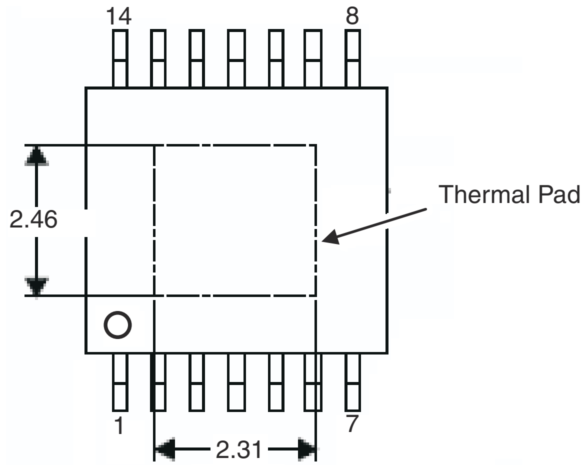


図 10-2. Thermal Pad Dimensions

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 用語集

TI 用語集	この用語集には、用語や略語の一覧および定義が記載されています。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54525PWP	ACTIVE	HTSSOP	PWP	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS54525	Samples
TPS54525PWPR	ACTIVE	HTSSOP	PWP	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS54525	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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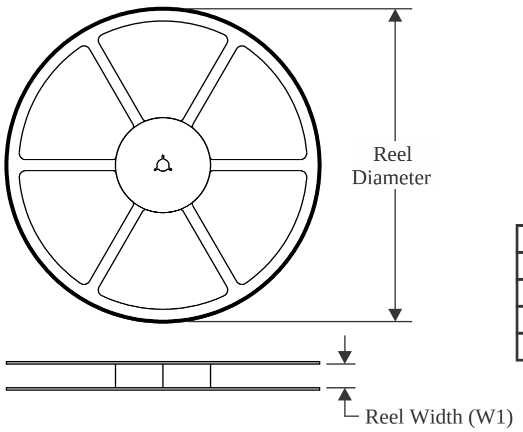
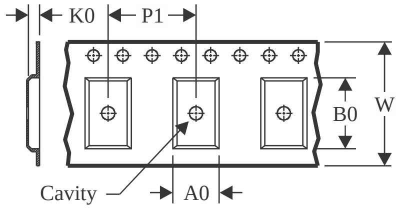
TAPE AND REEL INFORMATION

REEL DIMENSIONS

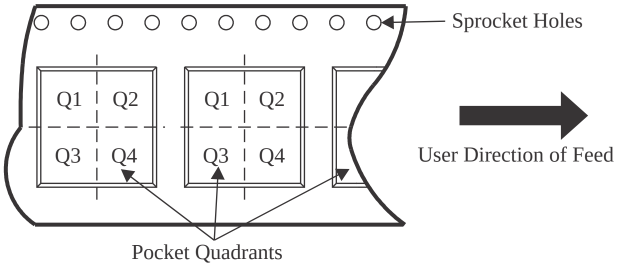


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

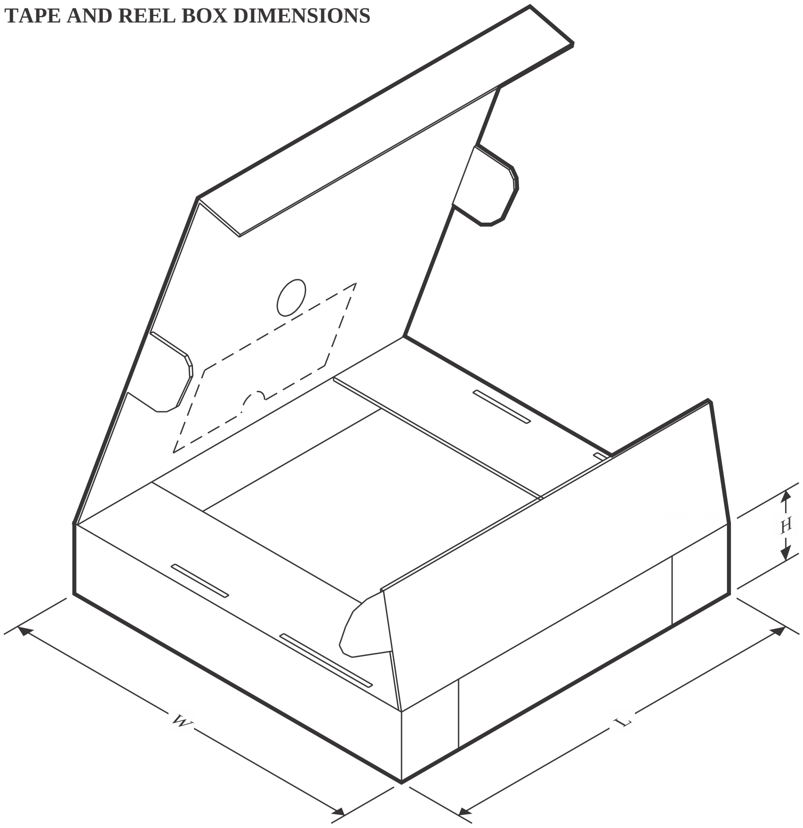
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54525PWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

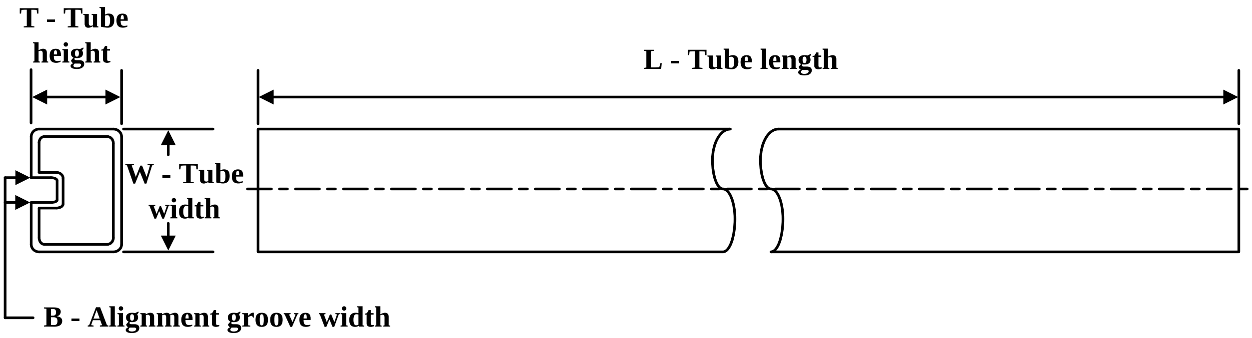
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54525PWPR	HTSSOP	PWP	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS54525PWP	PWP	HTSSOP	14	90	530	10.2	3600	3.5

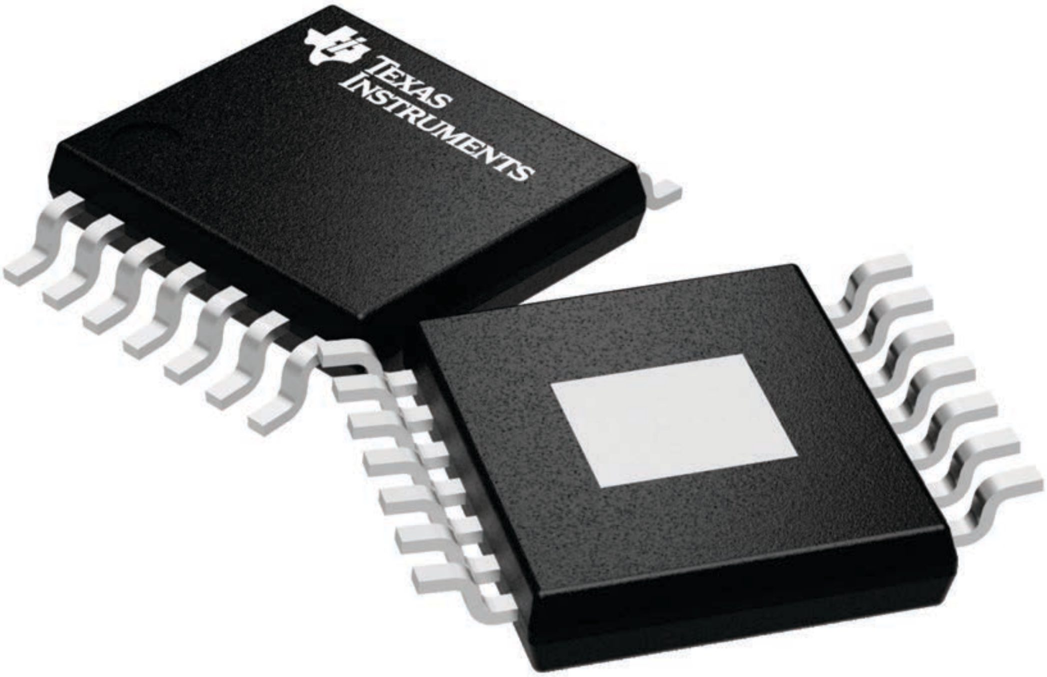
PWP 14

PowerPAD TSSOP - 1.2 mm max height

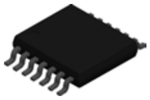
4.4 x 5.0, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



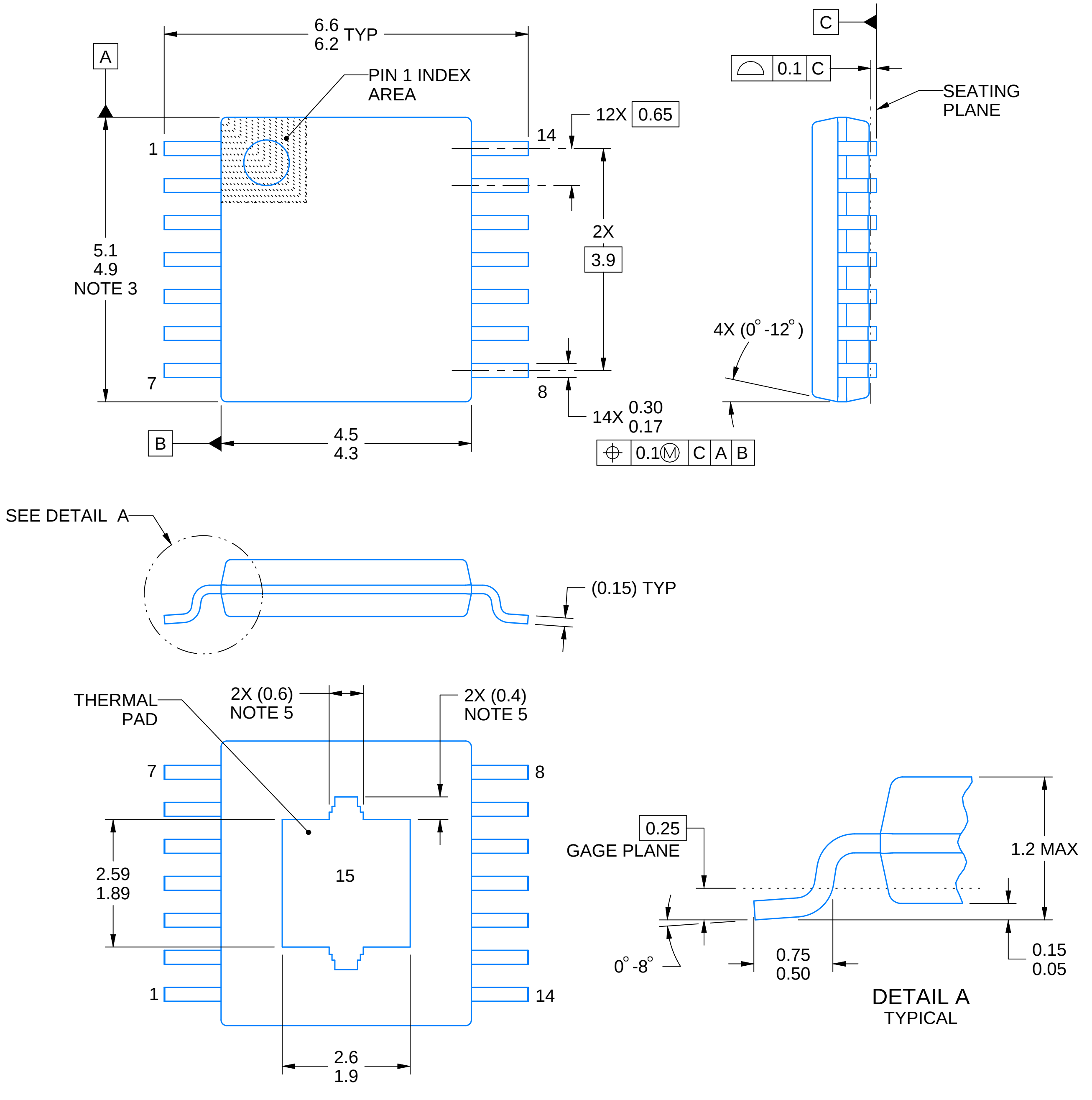
PACKAGE OUTLINE



PWP0014K

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

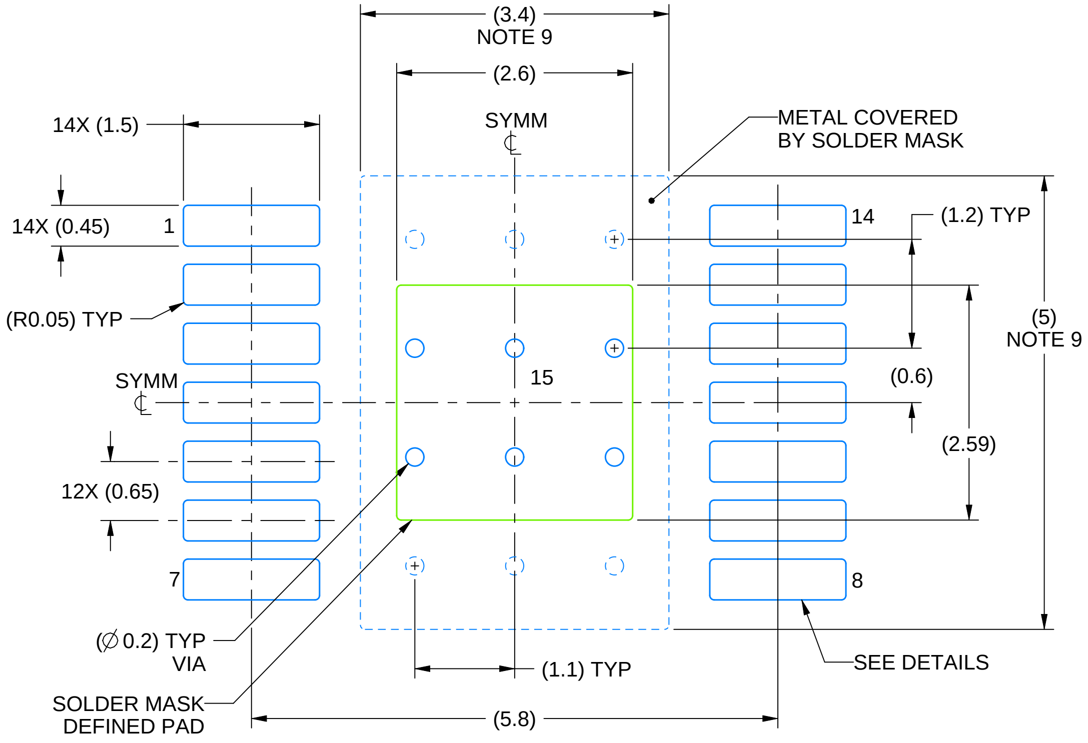


4229706/B 12/2023

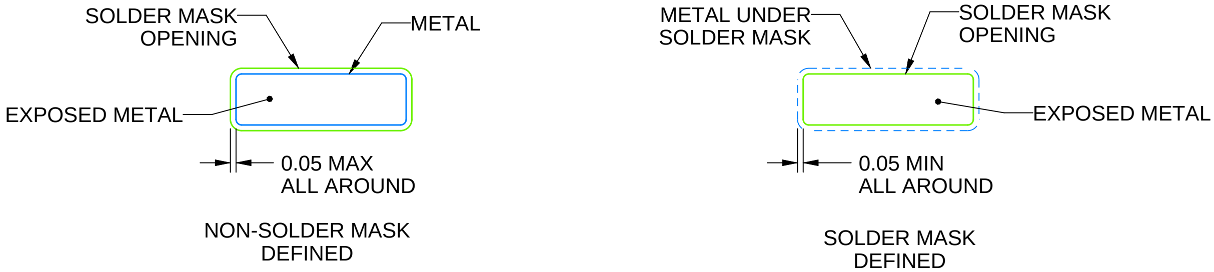
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

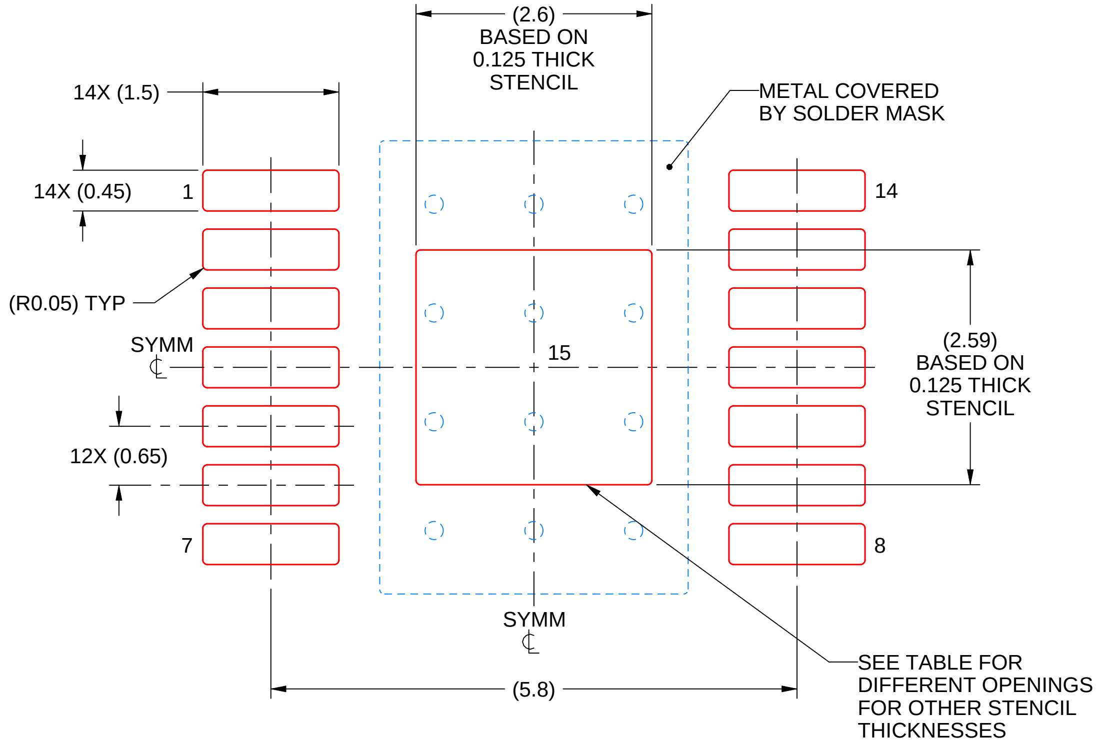


SOLDER MASK DETAILS

4229706/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 2.90
0.125	2.60 X 2.59 (SHOWN)
0.15	2.37 X 2.36
0.175	2.20 X 2.19

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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