

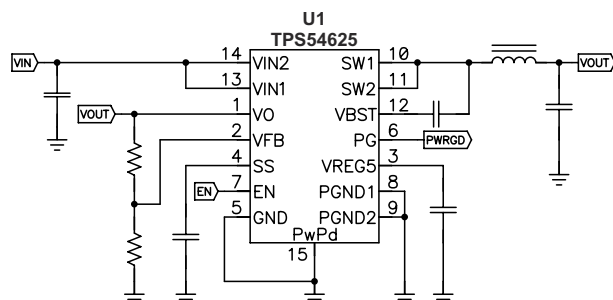
## 4.5V~18V 入力、6.5A 同期整流降圧コンバータ

### 1 特長

- 高速過渡応答を可能にする D-CAP2™ モード
- 低出力リップル、セラミック出力コンデンサを使用可能
- 広い  $V_{IN}$  入力電圧範囲: 4.5V~18V
- 出力電圧範囲: 0.76V~5.5V
- 低デューティ・サイクルのアプリケーションに対して最適化された、高効率の内蔵 FET – 36m $\Omega$  (ハイサイド) および 28m $\Omega$  (ローサイド)
- 高効率、シャットダウン時 10 $\mu$ A 未満
- 高い初期バンドギャップ・リファレンス精度
- 調整可能なソフト・スタート
- プリバイアス・ソフト・スタートに対応
- スwitching 周波数 ( $f_{SW}$ ): 650kHz
- サイクル毎の過電流制限
- パワー・グッド出力

### 2 アプリケーション

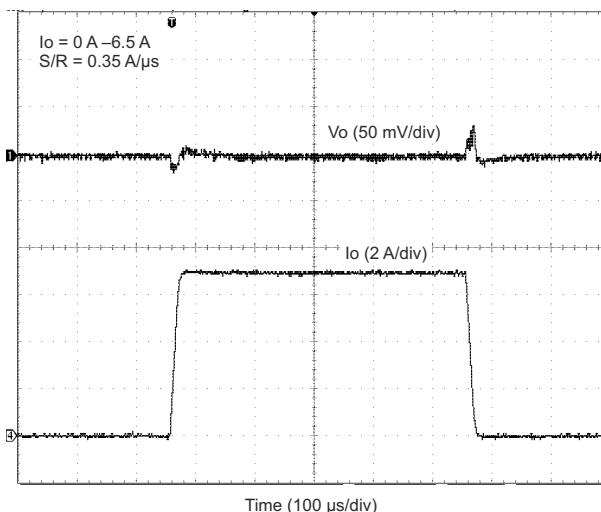
- 幅広い範囲の低電圧システム用アプリケーション
  - デジタル・テレビ用電源
  - 高精細 Blu-ray Disc™ プレーヤ
  - ネットワーク・ホーム・ターミナル
  - デジタル・セットトップ・ボックス (STB)



### 3 概要

TPS54625 は、適応型オン時間 D-CAP2™ モードに対応した同期整流降圧コンバータです。このデバイスを採用することで、各種機器の電源バス・レギュレータに対して、コスト効果が高く、部品数の少ない、低スタンバイ電流のソリューションを実現できます。

本デバイスの主制御ループは、外部補償部品なしで非常に高速な過渡応答が得られる D-CAP2™ モード制御を使用しています。また、低 ESR (等価直列抵抗) の出力コンデンサ (たとえば、POSCAP または SP-CAP) と超低 ESR セラミック・コンデンサの両方をサポートできる独自の回路も備えています。このデバイスは、4.5V~18V の  $V_{IN}$  入力で作動します。出力電圧は、0.76V~5.5V の範囲でプログラミングできます。また、調整可能なソフト・スタート時間とパワー・グッド機能も備えています。TPS54625 は 14 ピンの HTSSOP パッケージで供給され、-40°C~85°C の温度範囲で動作するように設計されています。



L004\_SLVSC33



## 4 ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACKAGE <sup>(2) (3)</sup>	ORDERABLE PART NUMBER	PIN	TRANSPORT MEDIA, QUANTITY
-45°C to 85°C	PowerPAD™ (HTSSOP) – PWP	TPS54625PWP	14	Tube
		TPS54625PWPR		Tape and Reel

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).
- (3) All package options have Cu NIPDAU lead/ball finish.

## 5 絶対最大定格

自由気流での動作温度範囲内 (特に記述のない限り) <sup>(1)</sup>

		数値	単位	
V <sub>I</sub>	入力電圧範囲	VIN1, VIN2, EN	-0.3~20	V
		VBST	-0.3~26	V
		VBST (10ns の過渡)	-0.3~28	V
		VBST (SW1, SW2 に対して)	-0.3~6.5	V
		VFB, VO, SS, PG	-0.3~6.5	V
		SW1, SW2	-2~20	V
		SW1, SW2 (10ns の過渡)	-3~22	V
V <sub>O</sub>	出力電圧範囲	VREG5	-0.3~6.5	V
		PGND1, PGND2	-0.3~0.3	V
V <sub>diff</sub>	GND と POWERPAD の間の電圧	-0.2~0.2	V	
ESD レーテ ィング	静電気放電	人体モデル (HBM)	2	kV
		デバイス帯電モデル (CDM)	500	V
T <sub>J</sub>	動作時接合部温度	-40~150	°C	
T <sub>stg</sub>	保存温度	-55~150	°C	

- (1) 絶対最大定格を上回るストレスが加わった場合、デバイスに永続的な損傷が発生する可能性があります。これはストレスの定格のみについて示しており、このデータシートの「推奨動作条件」に示された値と等しい、またはそれを超える条件で本製品が正しく動作することを暗に示すものではありません。絶対最大定格の状態に長時間置くと、本製品の信頼性に影響を与えることがあります。

## 6 THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		TPS54625	UNITS
		PWP (14 PINS)	
θ <sub>JA</sub>	Junction-to-ambient thermal resistance	40.5	°C/W
θ <sub>JCtop</sub>	Junction-to-case (top) thermal resistance	28.7	
θ <sub>JB</sub>	Junction-to-board thermal resistance	24.2	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.8	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	23.9	
θ <sub>JCbot</sub>	Junction-to-case (bottom) thermal resistance	2.4	

- (1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

## 7 RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
$V_{IN}$	Supply input voltage range	4.5	18	V	
$V_I$	Input voltage range	VBST	-0.1	24	V
		VBST(10 ns transient)	-0.1	27	
		VBST (vs SW)	-0.1	6.0	
		SS, PG	-0.1	5.7	
		EN	-0.1	18	
		VO, VFB	-0.1	5.5	
		SW1, SW2	-1.8	18	
		SW1, SW2 (10 ns transient)	-3	21	
	PGND1, PGND2	-0.1	0.1		
$V_O$	Output voltage range	VREG5	-0.1	5.7	V
$I_O$	Output Current range	$I_{VREG5}$	0	5	mA
$R_{EN}$	Power Good Resistor		25	150	k $\Omega$
$T_A$	Operating free-air temperature		-40	85	$^{\circ}$ C
$T_J$	Operating junction temperature		-40	150	$^{\circ}$ C

## 8 ELECTRICAL CHARACTERISTICS

over operating free-air temperature range,  $V_{IN} = 12V$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENT</b>						
$I_{VIN}$	Operating - non-switching supply current	$V_{IN}$ current, $T_A = 25^{\circ}$ C, EN = 5 V, $V_{VFB} = 0.8$ V		950	1400	$\mu$ A
$I_{VINSDN}$	Shutdown supply current	$V_{IN}$ current, $T_A = 25^{\circ}$ C, EN = 0 V		3.6	10	$\mu$ A
<b>LOGIC THRESHOLD</b>						
$V_{ENH}$	EN high-level input voltage	EN	1.6			V
$V_{ENL}$	EN low-level input voltage	EN			0.6	V
$R_{EN}$	EN pin resistance to GND	$V_{EN} = 12$ V	200	400	800	k $\Omega$
<b>VFB VOLTAGE AND DISCHARGE RESISTANCE</b>						
$V_{VFBTH}$	VFB threshold voltage	$T_A = 25^{\circ}$ C, $V_O = 1.05$ V, continuous mode	757	765	773	mV
		$T_A = 0^{\circ}$ C to $85^{\circ}$ C, $V_O = 1.05$ V, continuous mode <sup>(1)</sup>	753		777	
		$T_A = -40^{\circ}$ C to $85^{\circ}$ C, $V_O = 1.05$ V, continuous mode <sup>(1)</sup>	751		779	
$I_{VFB}$	VFB input current	VFB = 0.8 V, $T_A = 25^{\circ}$ C		0	$\pm 0.15$	$\mu$ A
$R_{Dischg}$	$V_O$ discharge resistance	$V_{EN} = 0$ V, $V_O = 0.5$ V, $T_A = 25^{\circ}$ C		100	150	$\Omega$
<b>VREG5 OUTPUT</b>						
$V_{VREG5}$	VREG5 output voltage	$T_A = 25^{\circ}$ C, $6.0$ V < $V_{IN}$ < 18 V, $0 < I_{VREG5} < 5$ mA	5.2	5.5	5.7	V
$I_{VREG5}$	Output current	$V_{IN} = 6$ V, $V_{VREG5} = 4$ V, $T_A = 25^{\circ}$ C	20			mA
<b>MOSFET</b>						
$R_{dsonh}$	High side switch resistance	$T_A = 25^{\circ}$ C, $V_{BST} - V_{SW1,2} = 5.5$ V		36		m $\Omega$
$R_{dsonl}$	Low side switch resistance	$T_A = 25^{\circ}$ C		28		m $\Omega$

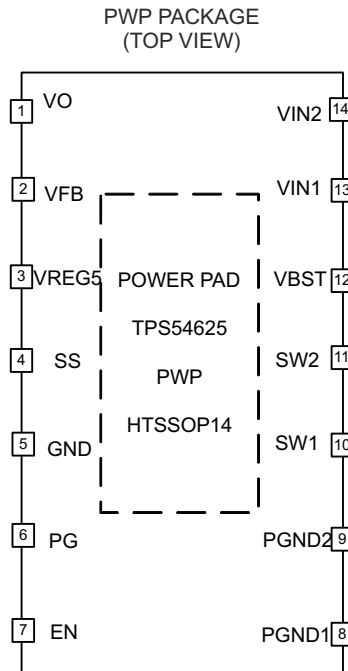
## 8 ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range,  $V_{IN} = 12V$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>CURRENT LIMIT</b>						
$I_{ocL}$	Current limit	$L_{OUT} = 1.5 \mu H^{(1)}$	7.2	8.2	9.5	A
<b>THERMAL SHUTDOWN</b>						
$T_{SDN}$	Thermal shutdown threshold	Shutdown temperature <sup>(1)</sup>		165		°C
		Hysteresis <sup>(1)</sup>		35		
<b>ON-TIME TIMER CONTROL</b>						
$T_{ON}$	On time	$V_{IN} = 12V, V_O = 1.05V$		150		ns
$T_{OFF(MIN)}$	Minimum off time	$T_A = 25^\circ C, V_{VFB} = 0.7V$		260	310	ns
<b>SOFT START</b>						
$I_{SSC}$	SS charge current	$V_{SS} = 1V$	4.2	6.0	7.8	$\mu A$
$I_{SSD}$	SS discharge current	$V_{SS} = 0.5V$	1.5	3.3		mA
<b>POWER GOOD</b>						
$V_{THPG}$	PG threshold	$V_{VFB}$ rising (good)	85%	90%	95%	
		$V_{VFB}$ falling (fault)		85%		
$I_{PG}$	PG sink current	$V_{PG} = 0.5V$	2.5	5		mA
<b>OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION</b>						
$V_{OVP}$	Output OVP trip threshold	OVP detect	120%	125%	130%	
$T_{OVPDEL}$	Output OVP prop delay			10		$\mu s$
$V_{UVP}$	Output UVP trip threshold	UVP detect	60%	65%	70%	
		Hysteresis		10%		
$T_{UVPDEL}$	Output UVP delay			0.25		ms
$T_{UVPEN}$	Output UVP enable delay	Relative to soft-start time		X 1.7		
<b>UVLO</b>						
$V_{UVLO}$	UVLO threshold	Wake up VREG5 voltage	3.45	3.75	4.05	V
		Hysteresis VREG5 voltage	0.13	0.32	0.48	

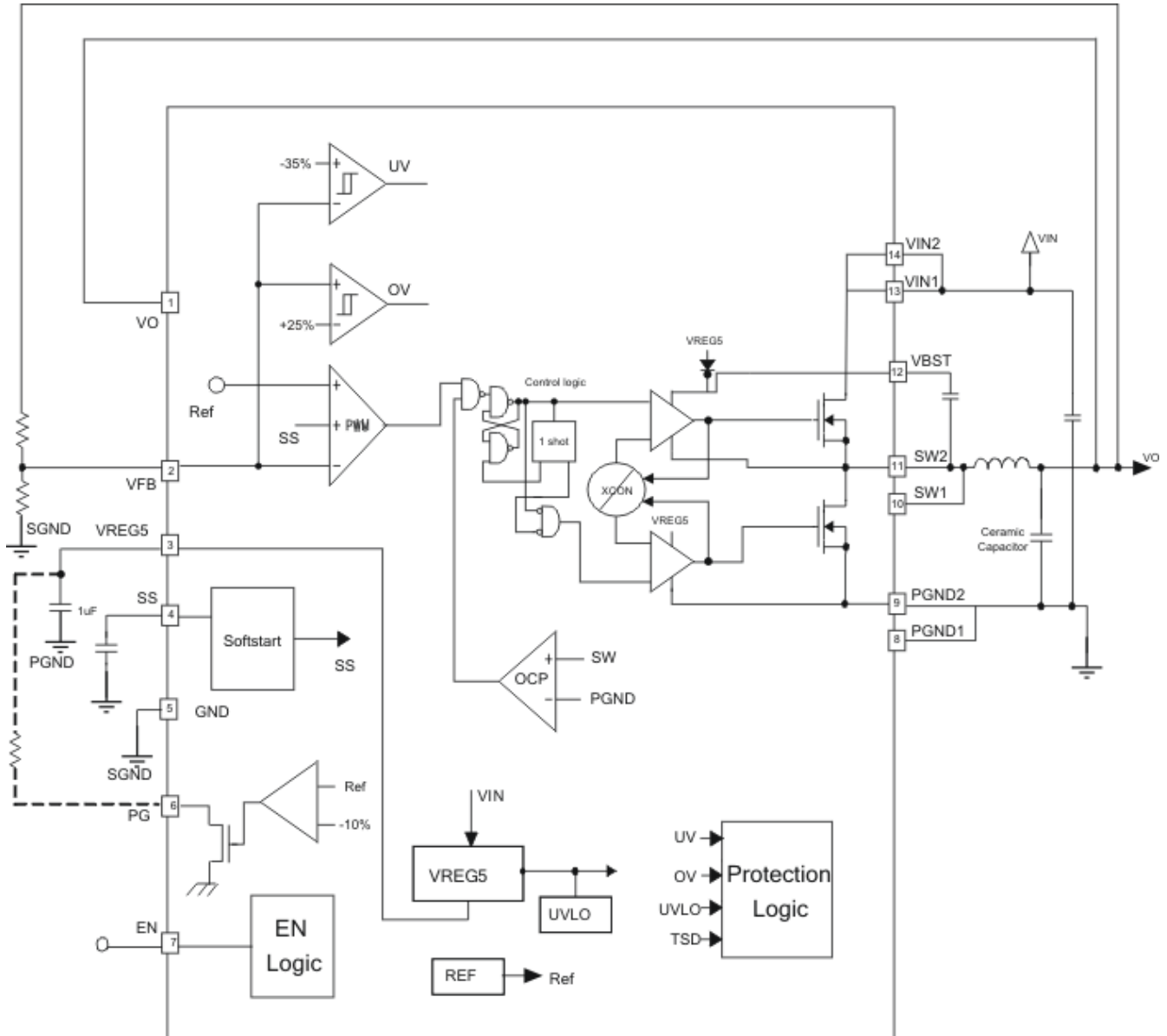
(1) Not production tested.

## 9 DEVICE INFORMATION



### Pin Functions

PIN		DESCRIPTION
NAME	NUMBER	
VO	1	Connect to output of converter. This pin is used for output discharge function.
VFB	2	Converter feedback input. Connect with feedback resistor divider.
VREG5	3	5.5V power supply output. An external capacitor (typical 1uF) should be connected to GND. VREG5 is not active when EN is low.
SS	4	Soft start control. An external capacitor should be connected to GND.
GND	5	Signal ground pin.
PG	6	Open drain power good output
EN	7	Enable control input. EN is active high and must be pulled up to enable the device.
PGND1, PGND2	8, 9	Ground returns for low-side MOSFET. Also serve as inputs of current comparators. Connect PGND and GND strongly together near the IC.
SW1,SW2	10, 11	Switch node connection between high-side NFET and low-side NFET. Also serve as inputs to current comparator.
VBST	12	Supply input for high-side NFET gate driver (boost terminal). Connect capacitor from this pin to respective SW1, SW2 terminals. An internal PN diode is connected between VREG5 and VBST pin.
VIN1, VIN2	13, 14	Power Input and connected to high side NFET drain. Supply Input for 5V internal linear regulator for the control circuitry
PowerPAD™	Back side	Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Should be connected to PGND



**9-1. FUNCTIONAL BLOCK DIAGRAM (HTSSOP)**

## 10 OVERVIEW

The TPS54625 is a 6.5A synchronous step-down (buck) converter with two integrated N-channel MOSFETs, using Forced Continuous Conduction Mode (FCCM) at light load for small output voltage ripple. It operates using D-CAP2™ mode control. The fast transient response of D-CAP2™ control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types.

## 11 DETAILED DESCRIPTION

### 11.1 PWM Operation

The main control loop of the TPS54625 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. D-CAP2™ mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot is set by the converter input voltage, VIN, and the output voltage, VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

### 11.2 PWM Frequency and Adaptive On-Time Control

TPS54625 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS54625 runs with a pseudo-constant frequency of 650 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage. The actual frequency may vary from 650kHz depending on the off time, which is ended when the feed back portion of the output voltage falls to the V<sub>FB</sub> threshold voltage.

### 11.3 Soft Start and Pre-Biased Soft Start

The soft start function is adjustable. When the EN pin becomes high, 6-μA current begins charging the capacitor which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start up. The equation for the slow start time is shown in 式 1. VFB voltage is 0.765 V and SS pin source current is 6 μA.

$$t_{SS}(\text{ms}) = \frac{C_{SS}(\text{nF}) \times V_{REF} \times 1.1}{I_{SS}(\mu\text{A})} = \frac{C_{SS}(\text{nF}) \times 0.765 \times 1.1}{6} \quad (1)$$

TPS54625 contains a unique circuit to prevent current from being pulled from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft-start becomes greater than feedback voltage V<sub>FB</sub>), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensure that the out voltage (VO) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation .

### 11.4 Power Good

TPS54625 has power-good open drain output. The power-good function is activated after soft start has finished. The power good function becomes active after 1.7 times soft-start time. When the output voltage becomes within –10% of the target value, internal comparators detect power good state and the power good signal becomes high. Rpg resistor value, which is connected between PG and VREG5, is required from 25 kΩ to 150 kΩ. If the feedback voltage goes under 15% of the target value, the power good signal becomes low.

## 11.5 Output Discharge Control

TPS54625 discharges the output when EN is low, or the controller is turned off by the protection functions (UVP, UVLO and thermal shutdown). The device discharges the output using an internal 100-Ω MOSFET which is connected to VO and GND. The internal low-side MOSFET is not turned on for the output discharge operation to avoid the possibility of causing negative voltage at the output.

## 11.6 Current Protection

The output over-current protection(OCP) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the SW and GND. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by  $V_{in}$ ,  $V_{out}$ , the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current  $I_{out}$ . The TPS54625 constantly monitors the low-side FET switch voltage, which is proportional to the switch current, during the low-side on-time. If the measured voltage is above the voltage proportional to the current limit, an internal counter is incremented per each SW cycle and the converter maintains the low-side switch on until the measured voltage is below the voltage corresponding to the current limit at which time the switching cycle is terminated and a new switching cycle begins. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of over-current protection. The load current one half of the peak-to-peak inductor current is higher than the over-current threshold. Also, when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall.

## 11.7 Over/Under Voltage Protection

TPS54625 detects over and under voltage conditions by monitoring the feedback voltage (VFB). This function is enabled after approximately 1.7 x times the softstart time.

When the feedback voltage becomes higher than 125% of the target voltage, the OVP comparator output goes high and the circuit latches and both the high-side MOSFET driver and the low-side MOSFET driver turn off.

When the feedback voltage becomes lower than 65% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins. After 250us, the device latches off both internal top and bottom MOSFET.

## 11.8 UVLO Protection

Under voltage lock out protection (UVLO) monitors the voltage of  $V_{REG5, pin}$ . When the VREG5 voltage is lower than UVLO threshold voltage, The TPS54625 is shut off. This protection is non-latching.

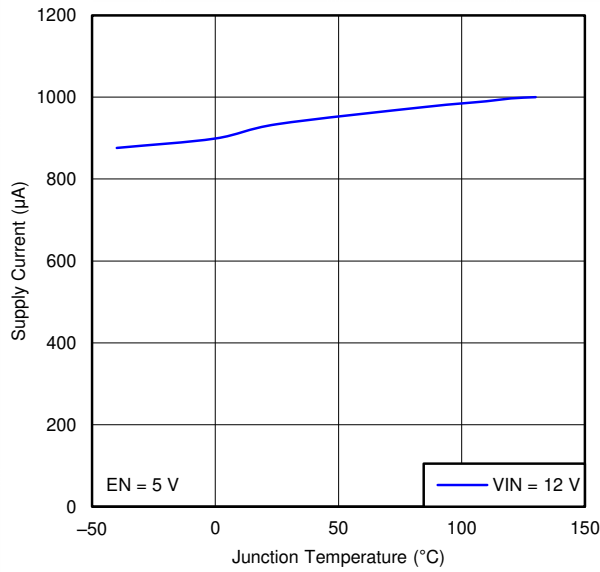
## 11.9 Thermal Shutdown

Thermal protection is self-activating. If the junction temperature exceeds the threshold value (typically 165°C), the TPS54625 is shut off. This is non-latch protection.

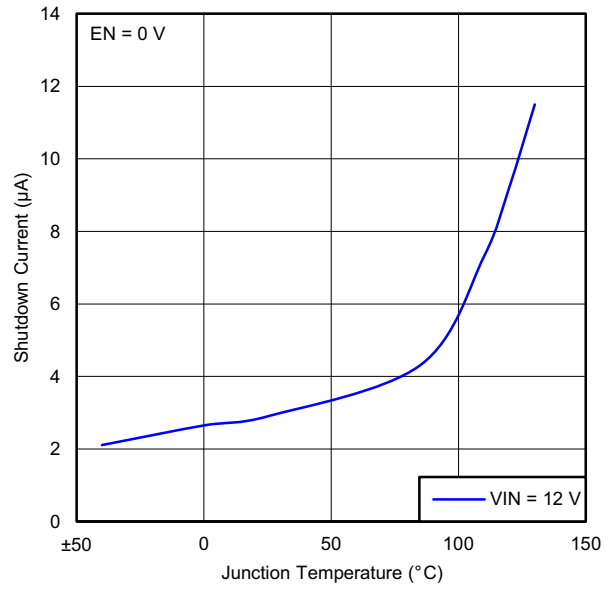


## 12 TYPICAL CHARACTERISTICS

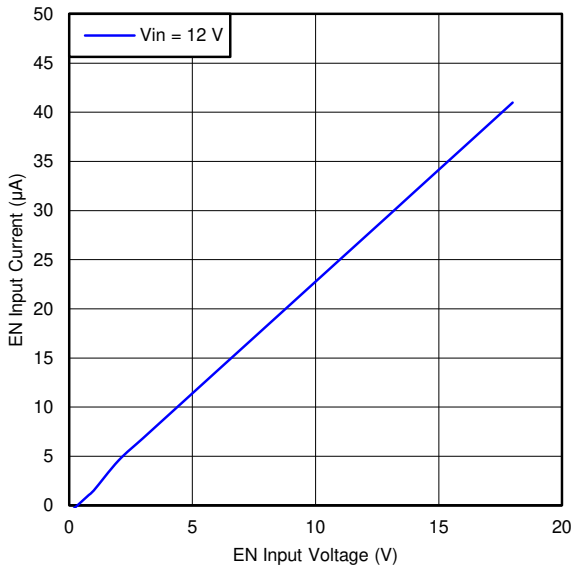
$V_{IN} = 12\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$  (unless otherwise noted)



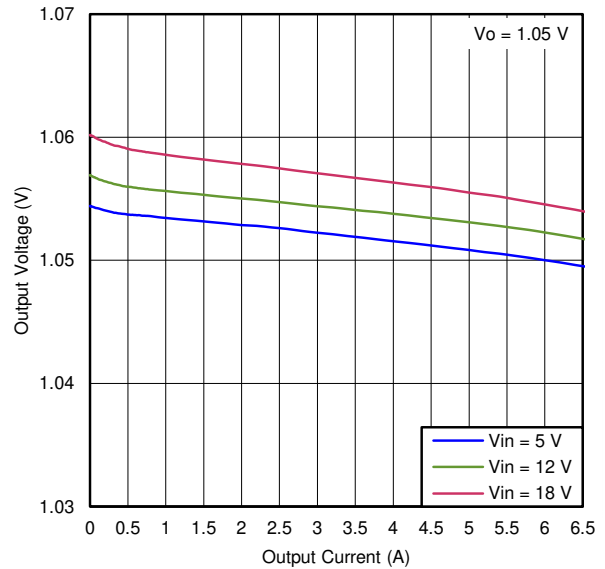
12-1.  $V_{IN}$  CURRENT vs JUNCTION TEMPERATURE



12-2.  $V_{IN}$  SHUTDOWN CURRENT vs JUNCTION TEMPERATURE



12-3. EN CURRENT vs EN VOLTAGE



12-4. 1.05-V OUTPUT VOLTAGE vs OUTPUT CURRENT

## 12 TYPICAL CHARACTERISTICS (continued)

$V_{IN} = 12\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$  (unless otherwise noted)

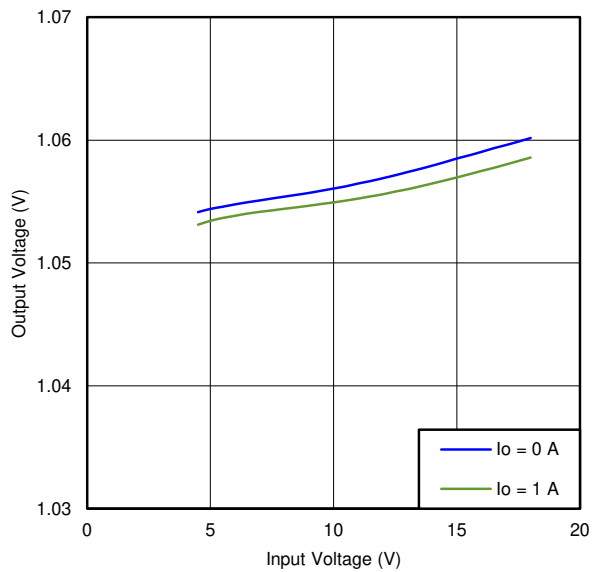


FIG 12-5. 1.05-V OUTPUT VOLTAGE vs INPUT VOLTAGE

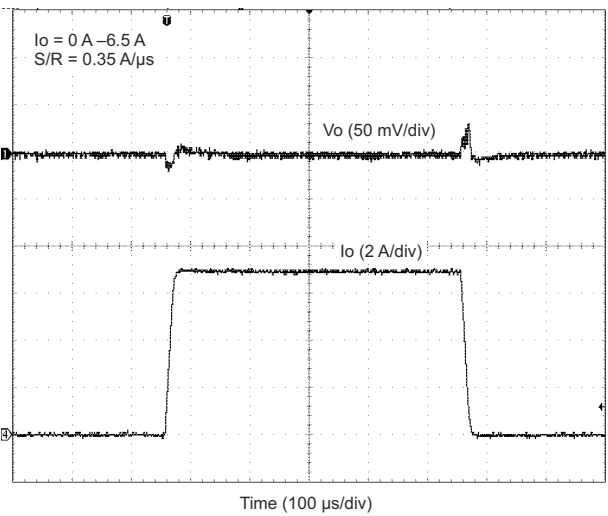


FIG 12-6. 1.05-V, 0-mA to 6.5-A LOAD TRANSIENT RESPONSE

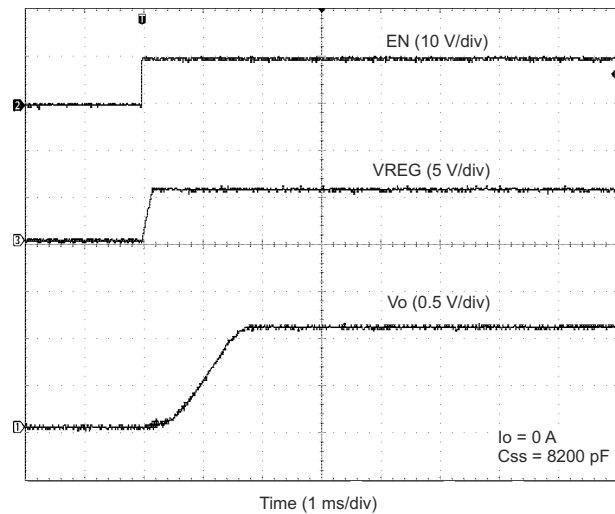


FIG 12-7. START-UP WAVE FORM

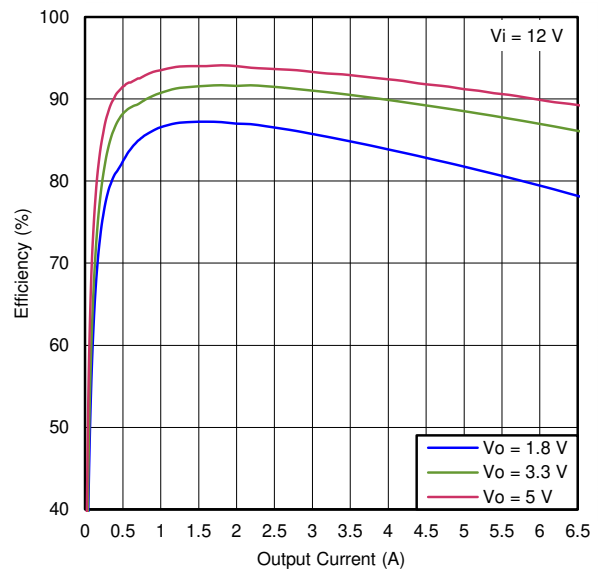
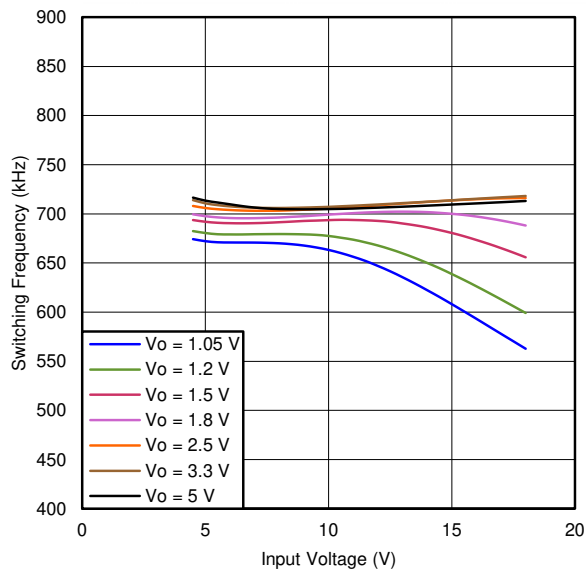


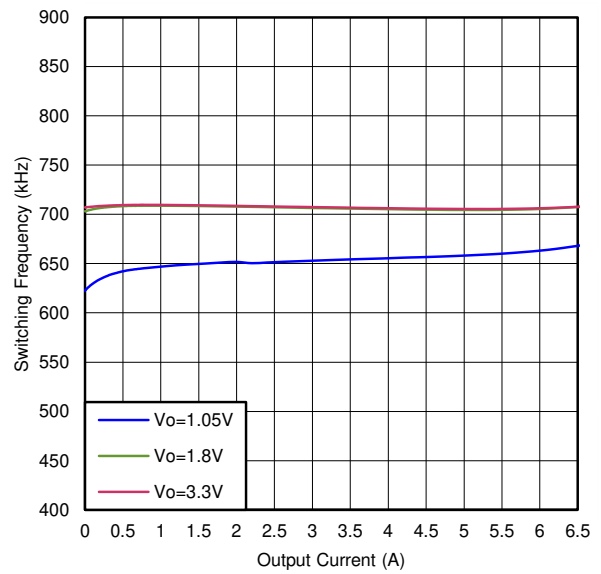
FIG 12-8. EFFICIENCY vs OUTPUT CURRENT (12 V)

## 12 TYPICAL CHARACTERISTICS (continued)

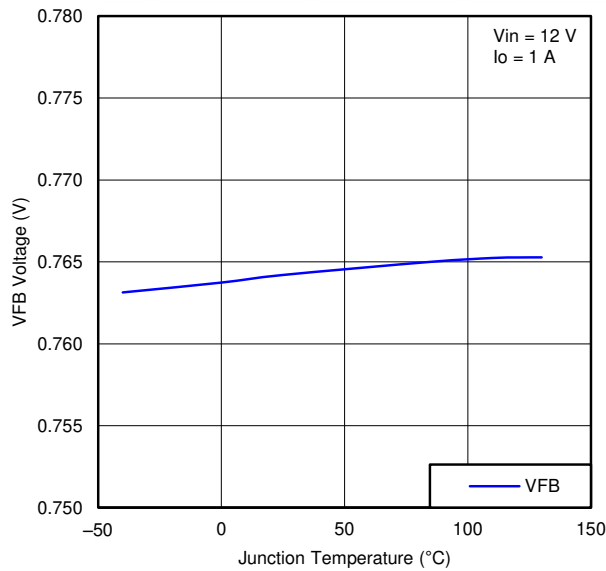
$V_{IN} = 12\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$  (unless otherwise noted)



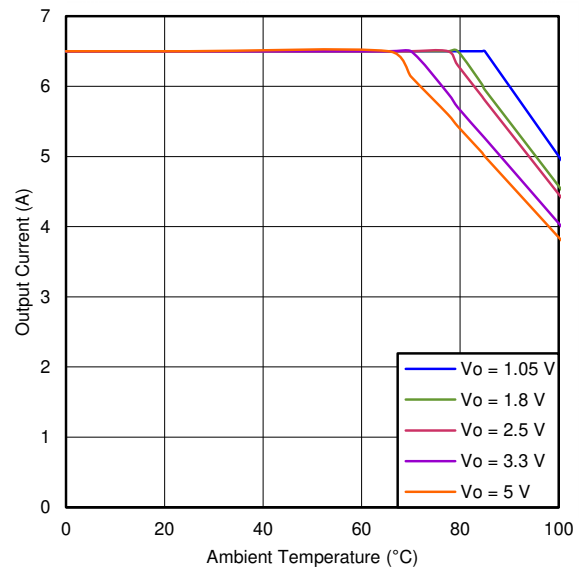
12-9. SWITCHING FREQUENCY vs INPUT VOLTAGE ( $I_o = 1\text{ A}$ )



12-10. SWITCHING FREQUENCY vs OUTPUT CURRENT



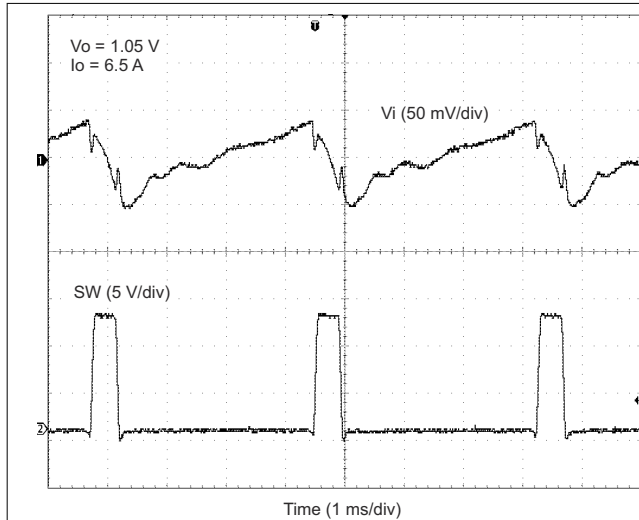
12-11. VFB VOLTAGE vs JUNCTION TEMPERATURE



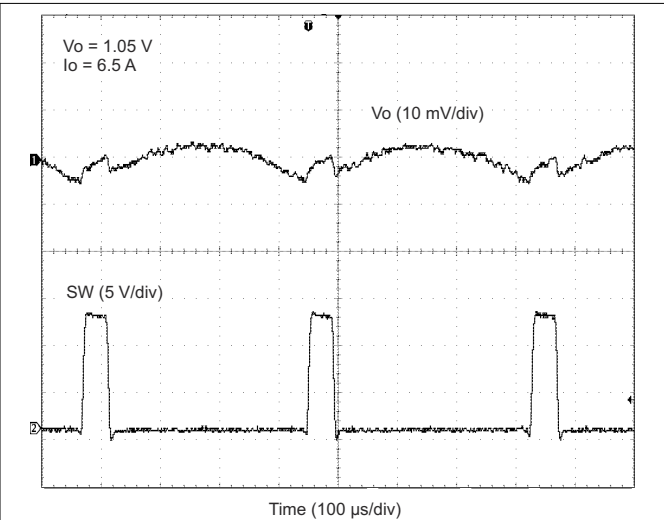
12-12. OUTPUT CURRENT vs AMBIENT TEMPERATURE

## 12 TYPICAL CHARACTERISTICS (continued)

$V_{IN} = 12\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$  (unless otherwise noted)



⊠ 12-13. VOLTAGE RIPPLE AT INPUT ( $I_O = 6.5\text{ A}$ )



⊠ 12-14. VOLTAGE RIPPLE AT OUTPUT ( $I_O = 6.5\text{ A}$ )

## 13 DESIGN GUIDE

### 13.1 Step By Step Design Procedure

To begin the design process, you must know a few application parameters:

- Input voltage range
- Output voltage
- Output current
- Output voltage ripple
- Input voltage ripple

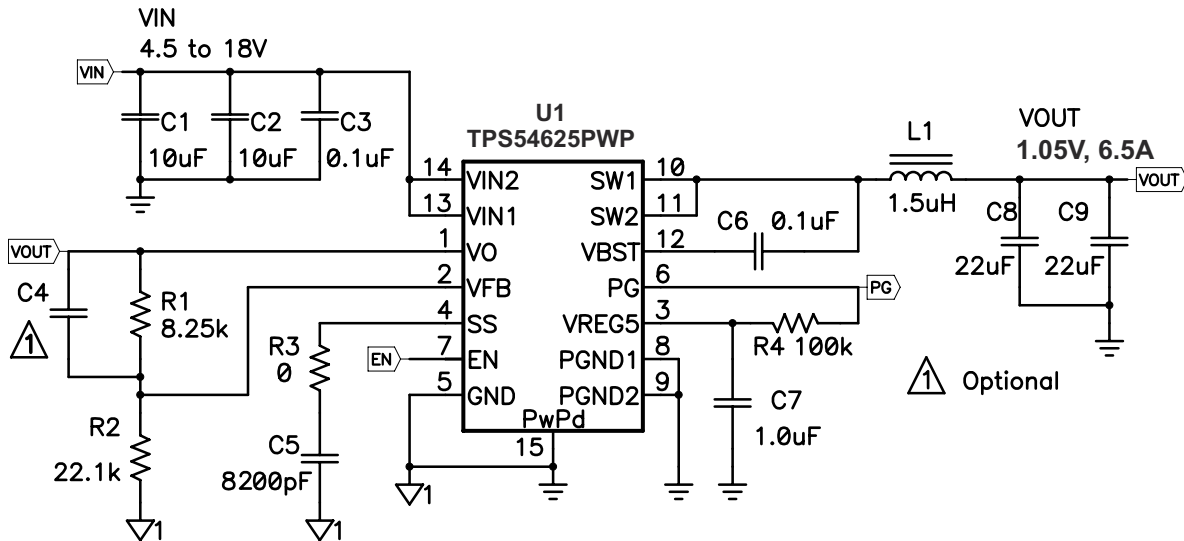


图 13-1. Schematic

### 13.2 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using 式 2 to calculate  $V_{OUT}$ .

To improve efficiency at very light loads consider using larger value resistors, too high of resistance will be more susceptible to noise and voltage errors from the VFB input current will be more noticeable.

$$V_{OUT} = 0.765 \cdot \left(1 + \frac{R1}{R2}\right) \quad (2)$$

### 13.3 Output Filter Selection

The output filter used with the TPS54625 is an LC circuit. This LC filter has double pole at:

$$F_p = \frac{1}{2\pi \sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS54625. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a  $-40$  dB per decade rate and the phase drops rapidly. D-CAP2™ introduces a high frequency zero that reduces the gain roll off to  $-20$  dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of 式 3 is located below the high frequency zero but close enough that the phase boost provided by the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in 表 13-1

**表 13-1. Recommended Component Values**

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	C4 (pF)	L1 (μH)	C8 + C9 (μF)
1	6.81	22.1	5 - 220	1.0 - 1.5 - 4.7	22 - 68
1.05	8.25	22.1	5 - 220	1.0 - 1.5 - 4.7	22 - 68
1.2	12.7	22.1	5 - 100	1.0 - 1.5 - 4.7	22 - 68
1.5	21.5	22.1	5 - 68	1.0 - 1.5 - 4.7	22 - 68
1.8	30.1	22.1	5 - 22	1.2 - 1.5 - 4.7	22 - 68
2.5	49.9	22.1	5 - 22	1.5 - 2.2 - 4.7	22 - 68
3.3	73.2	22.1	5 - 22	1.8 - 2.2 - 4.7	22 - 68
5	124	22.1	5 - 22	2.5 - 3.3 - 4.7	22 - 68

For higher output voltages at or above 1.8 V, additional phase boost can be achieved by adding a feed forward capacitor (C4) in parallel with R1.

Since the DC gain is dependent on the output voltage, the required inductor value will increase as the output voltage increases. For higher output voltages at or above 1.8 V, additional phase boost can be achieved by adding a feed forward capacitor (C4) in parallel with R1

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using 式 4, 式 5 and 式 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 650 kHz for  $f_{SW}$ .

Use 650 kHz for  $f_{SW}$  and also use 1.5μH for  $L_o$ . Make sure the chosen inductor is rated for the peak current of 式 5 and the RMS current of 式 6.

$$I_{lp-p} = \frac{V_{OUT}}{V_{IN(max)}} \cdot \frac{V_{IN(max)} - V_{OUT}}{L_o \cdot f_{SW}} \quad (4)$$

$$I_{lpeak} = I_o + \frac{I_{lp-p}}{2} \quad (5)$$

$$I_{Lo(RMS)} = \sqrt{I_o^2 + \frac{1}{12} I_{lp-p}^2} \quad (6)$$

For this design example, the calculated peak current is 7.01 A and the calculated RMS current is 6.51 A. The inductor used is a TDK SPM6530-1R5M100 with a peak current rating of 11.5 A and an RMS current rating of 11 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS54625 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 22μF to 68μF. Use 式 7 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{\sqrt{12} \cdot V_{IN} \cdot L_o \cdot f_{SW}} \quad (7)$$

For this design two TDK C3216X5R0J226M 22μF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.286 A and each output capacitor is rated for 4A.

### 13.4 Input Capacitor Selection

The TPS54625 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 μF is recommended for the decoupling capacitor. An additional 0.1 μF capacitor from pin 14 to ground is recommended to improve the EMI performance. The capacitor voltage rating needs to be greater than the maximum input voltage.

### 13.5 Bootstrap Capacitor Selection

A 0.1  $\mu\text{F}$  ceramic capacitor must be connected between the VBST to SW pin for proper operation. It is recommended to use a ceramic capacitor.

### 13.6 VREG5 Capacitor Selection

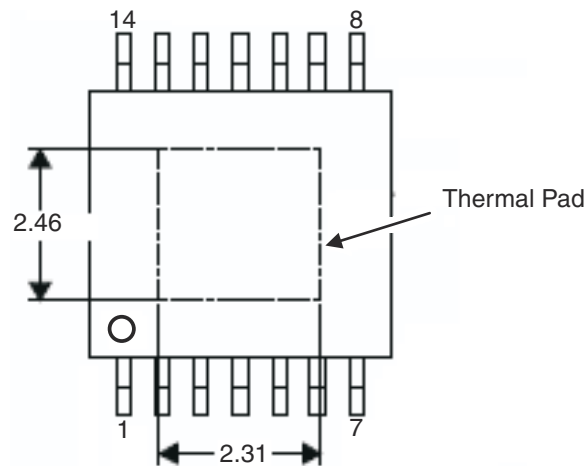
A 1.0  $\mu\text{F}$  ceramic capacitor must be connected between the VREG5 to GND pin for proper operation. It is recommended to use a ceramic capacitor.

## 14 THERMAL INFORMATION

This PowerPad™ package incorporates an exposed thermal pad that is designed to be directly to an external heatsink. The thermal pad must be soldered directly to the printed board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD™ package and how to use the advantage of its heat dissipating abilities, refer to Technical Brief, *PowerPAD™ Thermally Enhanced Package*, Texas Instruments Literature No. [SLMA002](#) and Application Brief, *PowerPAD™ Made Easy*, Texas Instruments Literature No. [SLMA004](#).

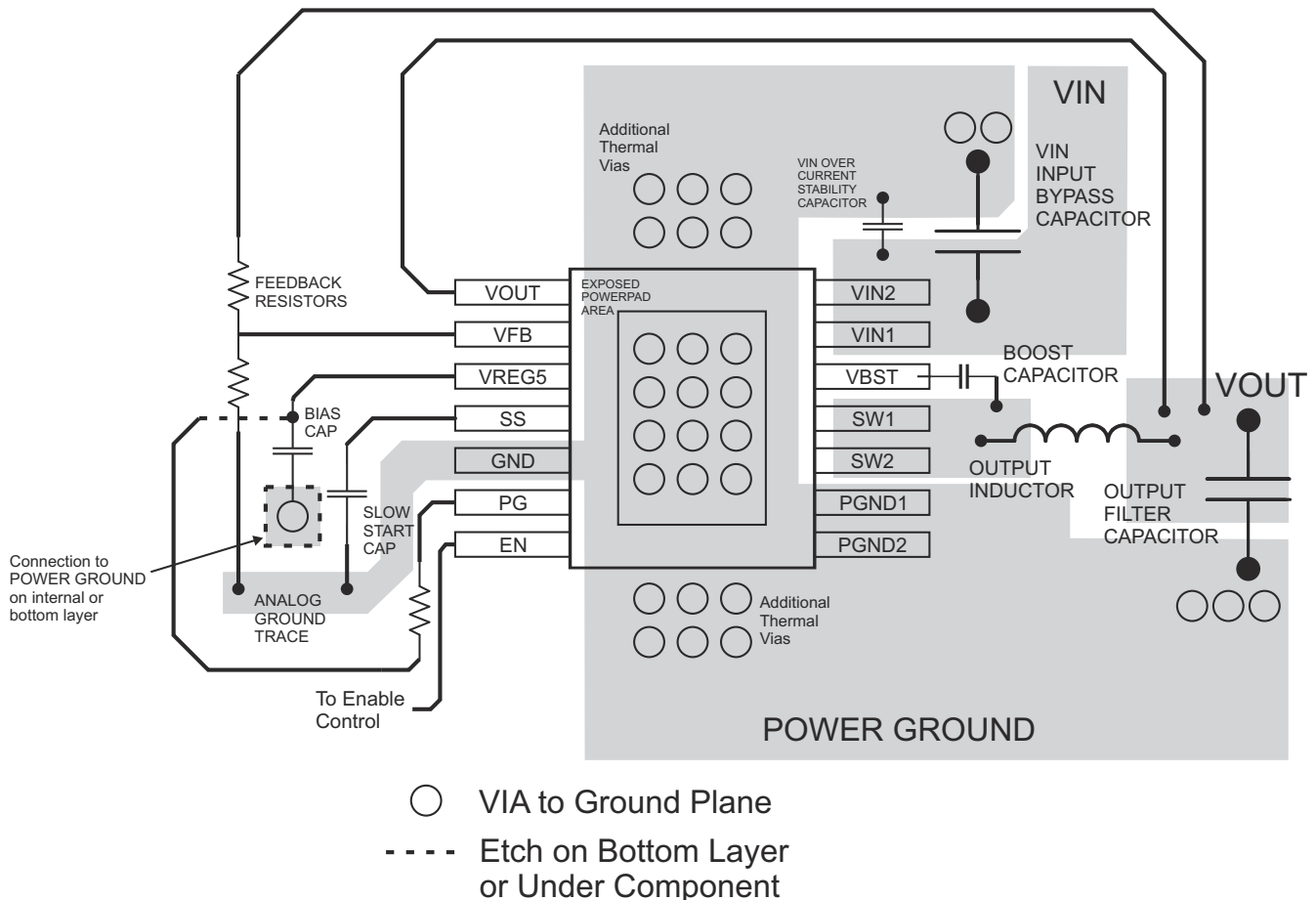
The exposed thermal pad dimensions for this package are shown in the following illustration.



✶ 14-1. Thermal Pad Dimensions

## 15 LAYOUT CONSIDERATIONS

1. A top side area should be filled with ground as much as possible due to relatively higher current output device.
2. The ground area under the device thermal pad should be large as possible and directly connect to the thermal pad. Also 2<sup>nd</sup>, 3<sup>rd</sup> and 4<sup>th</sup> PCB layer should be connected to ground directly from the thermal pad.
3. Keep the input switching current loop as small as possible.
4. Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin of the device.
5. Keep analog and non-switching components away from switching components.
6. Make a single point connection from the signal ground to power ground.
7. Do not allow switching current to flow under the device.
8. Keep the pattern lines for VIN and PGND broad.
9. Exposed pad of device must be connected to PGND with solder.
10. VREG5 capacitor should be placed near the device, and connected PGND.
11. Output capacitor should be connected to a broad pattern of the PGND.
12. Voltage feedback loop should be as short as possible, and preferably with ground shield.
13. Lower resistor of the voltage divider which is connected to the VFB pin should be tied to SGND.
14. Providing sufficient via is preferable for VIN, SW and PGND connection.
15. PCB pattern for VIN, SW, and PGND should be as broad as possible.
16. VIN Capacitor should be placed as near as possible to the device.



15-1. PCB Layout



## 16 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

<b>Changes from Revision * (August 2013) to Revision A (October 2022)</b>	<b>Page</b>
• 文書全体にわたって表、図、相互参照の採番方法を更新.....	<a href="#">1</a>
• Updated the light load mode to Forced Continuous Conduction Mode (FCCM).....	<a href="#">7</a>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54625PWP	ACTIVE	HTSSOP	PWP	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS54625	<a href="#">Samples</a>
TPS54625PWPR	ACTIVE	HTSSOP	PWP	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS54625	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54625PWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54625PWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPS54625PWP	PWP	HTSSOP	14	90	530	10.2	3600	3.5

## GENERIC PACKAGE VIEW

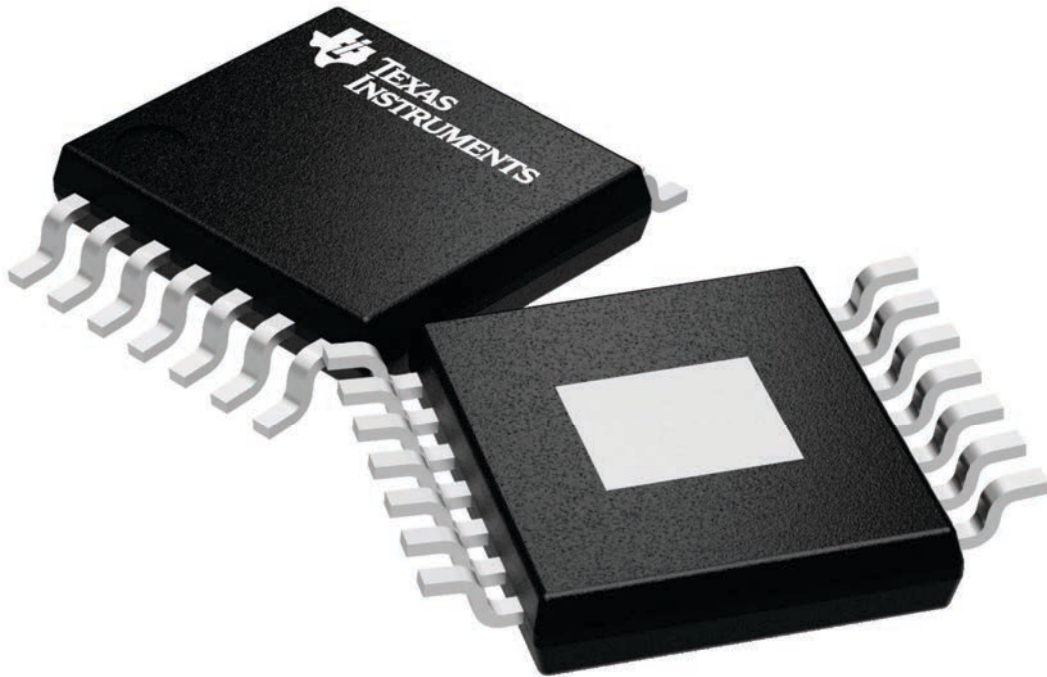
**PWP 14**

**PowerPAD TSSOP - 1.2 mm max height**

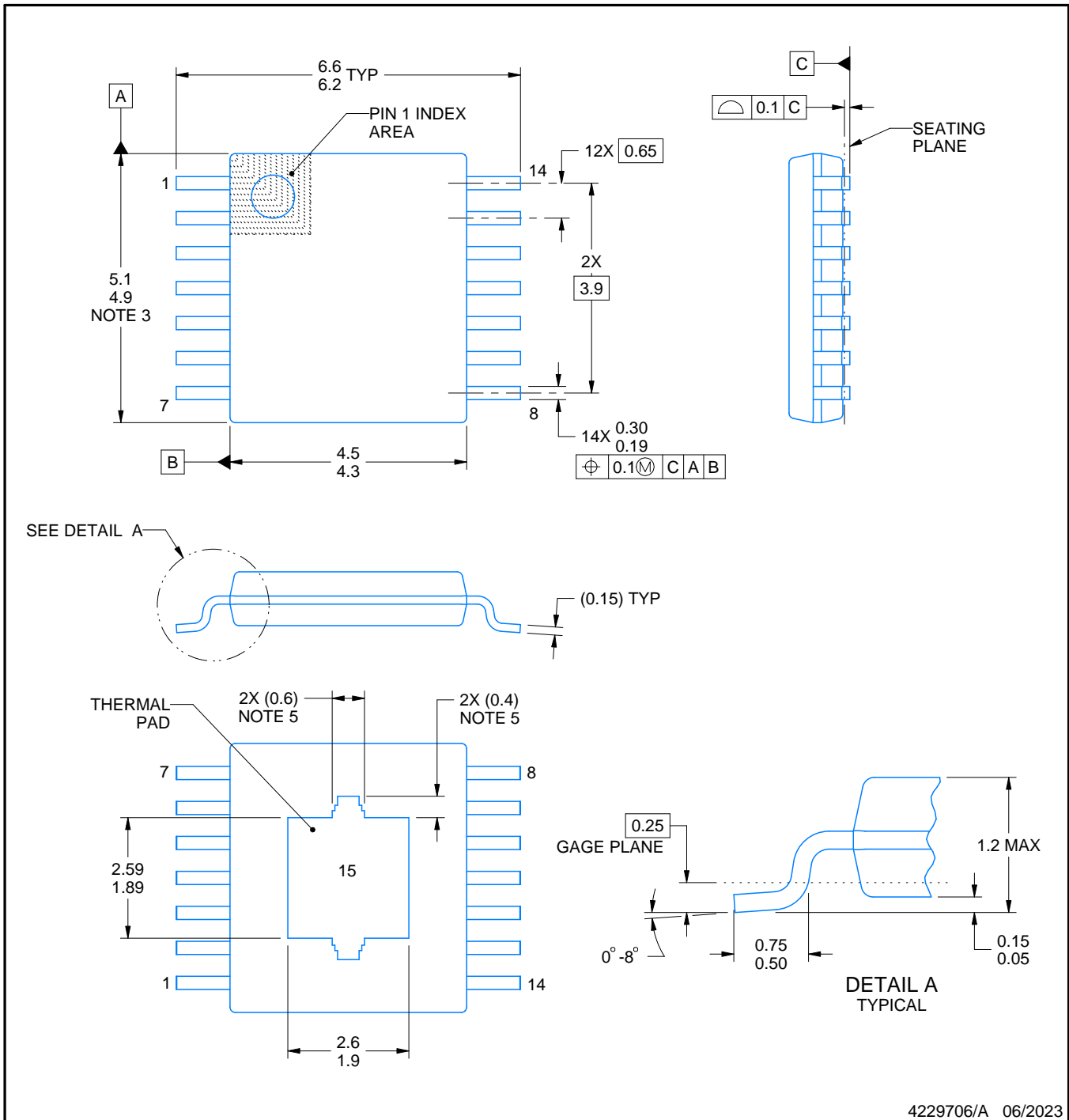
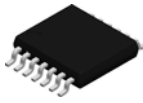
4.4 x 5.0, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224995/A



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NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

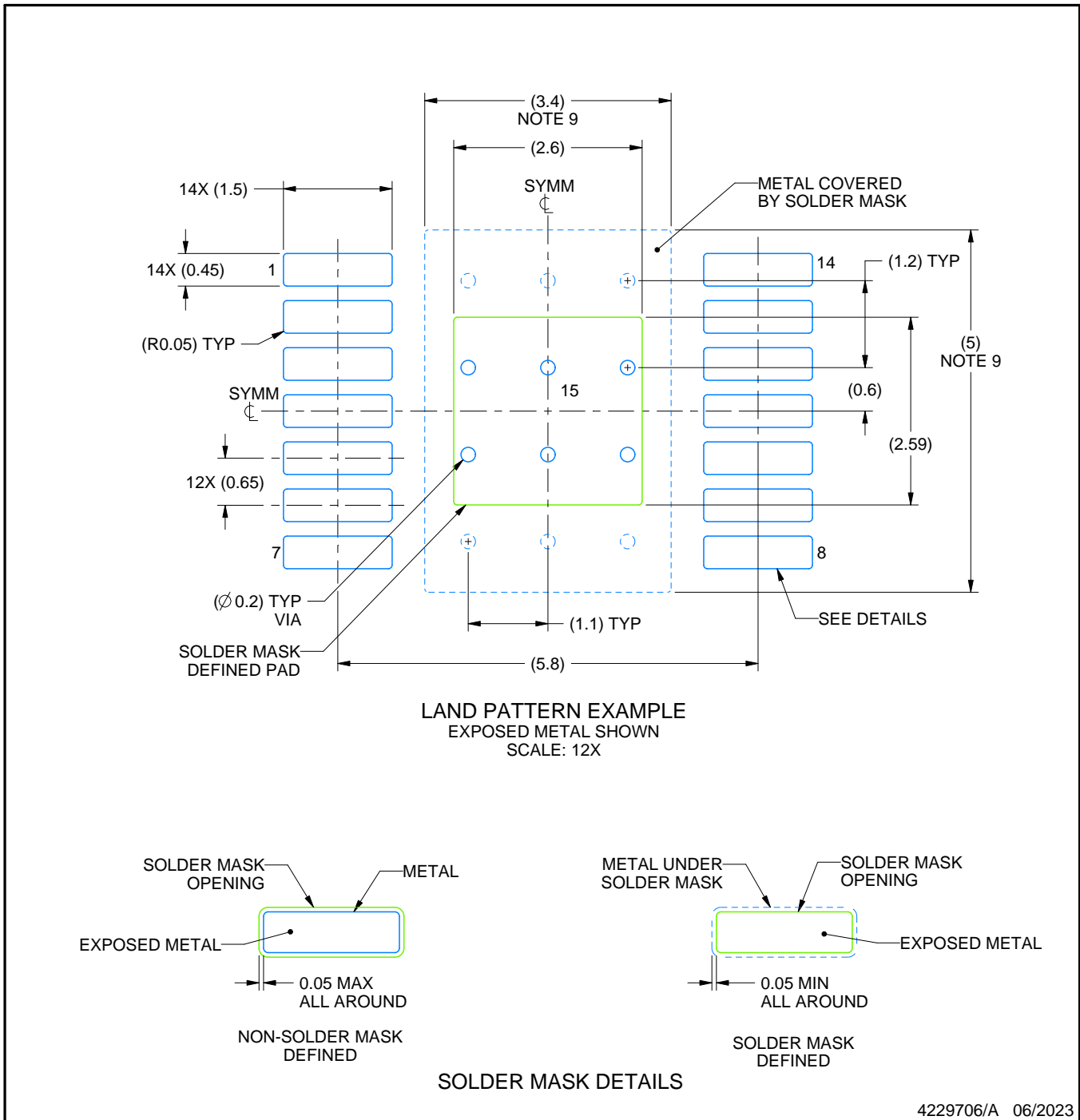


# EXAMPLE BOARD LAYOUT

PWP0014K

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

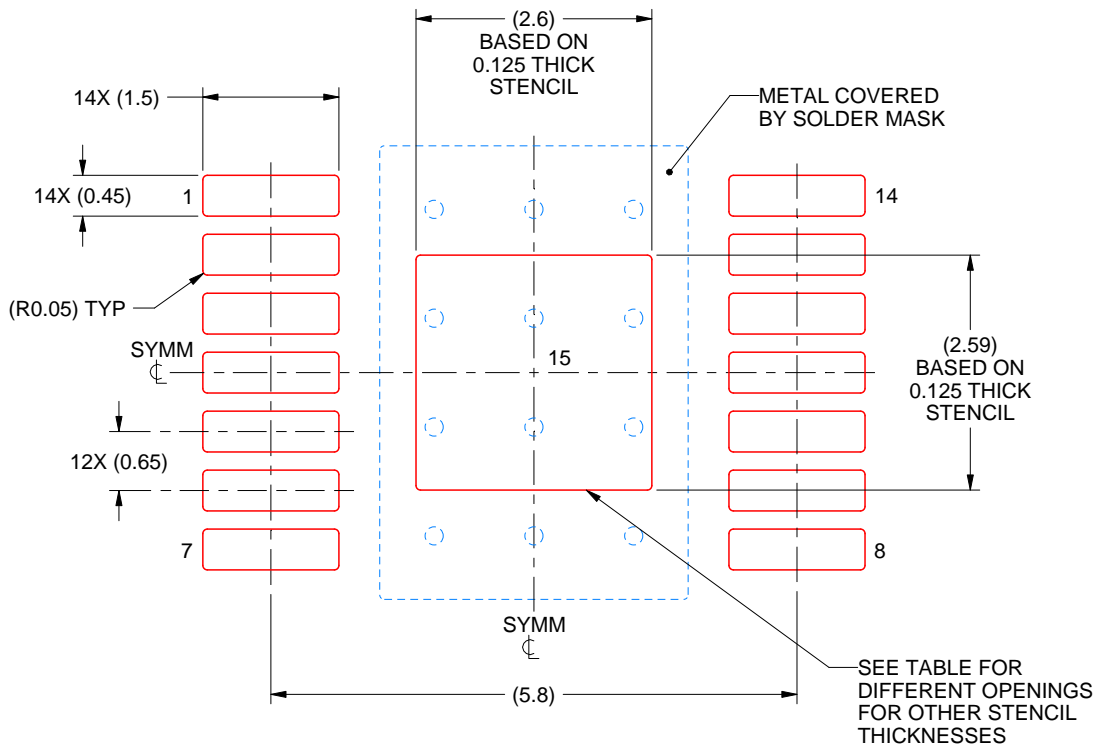
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

PWP0014K

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 2.90
0.125	2.60 X 2.59 (SHOWN)
0.15	2.37 X 2.36
0.175	2.20 X 2.19

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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