TEXAS INSTRUMENTS
TPS55160-Q1, TPS55162-Q1, TPS55165-Q1
JAJSE62A – NOVEMBER 2017 – REVISED DECEMBER 2021

TPS5516x-Q1 36V、1A 出力、2MHz、シングル・インダクタ、同期整流昇降圧レギュレータ

1 特長

- 車載アプリケーション認定済み
- 下記内容で AEC-Q100 認定済み:
  - デバイス温度グレード 1:–40℃～+125℃の動作時周囲温度範囲
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C4B
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- V_{OUT} = 5V 時の入力電圧範囲:2V～36V
- 5V または 12V の固定出力電圧 (TPS55165-Q1)
- 5.7V～9V の可変出力電圧オプション (TPS55160-Q1 および TPS55162-Q1)
- 最大 85% の効率
- V_{OUT} = 5V および V_{IN} ≧ 5.3V 時の出力電流:1A
- V_{OUT} = 5V および V_{IN} ≧ 3.8V 時の出力電流:0.8A
- V_{OUT} = 5V および V_{IN} ≧ 2.3V 時の出力電流:0.4A
- 降圧モードと昇圧モードの自動遷移
- 低消費電力モードにより軽負荷条件での効率性が向上 (TPS55160-Q1 および TPS55165-Q1)
- 低消費電力モードでのデバイス静止電流:15μA 未満 (TPS55160-Q1 および TPS55165-Q1)
- デバイス・シャットダウン時電流:3μA 未満
- 2MHz の強制固定周波数動作
- 選択可能なスペクトラム拡散 (TPS55160-Q1 および TPS55165-Q1)
- 電力ラッチ機能を備えた IGN によるウェークアップ
- 遅延時間の設定が可能なスマート・パワー・グッド出力
- 過熱保護および出力過電圧保護
- 使いやすい 20 ピン HTSSOP PowerPAD™ パッケージで供給

2 アプリケーション

- 始動 / 停止時に影響を受けやすい車載用電源アプリケーション
  - インフォテインメントとクラスタ
  - ボディ・エレクトロニクスおよびゲートウェイ・モジュール
- 入力電圧が変動する産業用アプリケーション
  - ソーラー・バッテリ充電
  - リチウムイオン・バッテリ・パック

3 概要

TPS5516x-Q1 デバイス・ファミリは、高電圧同期整流式の昇降圧 DC/DC コンバータです。自動車用バッテリなど、多種多様な入力電源からの安定した電源出力を実現します。降圧 / 昇圧オーバーラップ制御により、降圧モードおよび昇圧モードに自動的に切り替わり、最適な水準まで効率を高めることができます。TPS55165-Q1 の出力電圧は固定レベルである 5V または 12V に設定できる一方、TPS55160-Q1 および TPS55162-Q1 デバイスの出力電圧は、外付け分圧抵抗回路を使って 5.7V～9V の範囲で設定可能です。

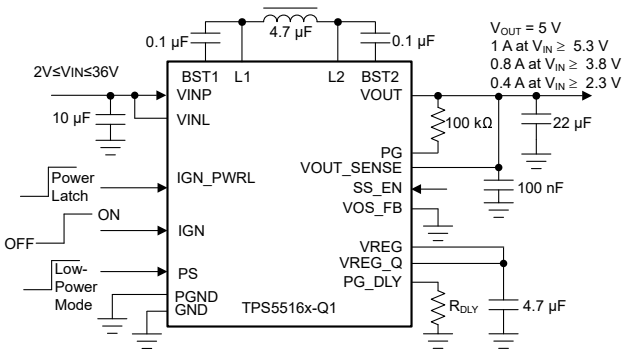
通常の自動車用バッテリ電圧における出力電流は最大 1A で、一般的なバッテリ・クランク・プロファイルのように低い入力電圧では 0.4A を維持できます。この昇降圧コンバータは、固定周波数のパルス幅変調 (PWM) 制御回路を基礎とし、同期整流を使用して最大の効率を実現しています。スイッチング周波数を 2MHz (標準値) に設定しているため、小型インダクタを使用して占有面積を低減できます。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TPS55160-Q1	HTSSOP (20)	6.50mm × 4.40mm
TPS55162-Q1		
TPS55165-Q1		

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図



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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (November 2017) to Revision A (December 2021)	Page
• 機能安全の箇条書き項目を追加	1
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• デバイス・ピンに対応した正しいオフ / オン波形を示すために図を変更	1
• プレビューの注を削除	1
• Updated *Overcurrent Protection* section	18
• Changed 式 5 solution from "0.458 A" to "0.229 A"	33

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5 概要 (続き)

選択可能なスペクトラム拡散オプションにより (TPS55160-Q1 および TPS55165-Q1)、放射電磁妨害 (EMI) の低減を支援します。ループ補償回路を内蔵しているため、外付け補償部品は不要です。低消費電力モードでは (TPS55160-Q1 および TPS55165-Q1)、静止電流が 15µA 未満となり、車載電子制御ユニット (ECU) をスタンバイ・モード (listen-to-CAN モードなど) に維持しながら、OEM の静止電流要件を満たすことができます。低消費電力モードをディスエーブルにし、全負荷電流範囲にわたり固定スイッチング周波数 2MHz (標準値) で、コンバータをフル連続モードで動作させることも可能です。インダクタの最大平均電流は、標準値 2A に制限されています。

バッテリの消耗を最小限に抑えるために、コンバータをディスエーブルできます。さらに、パワー・グッド (PG) ピンにより、出力レールが規定の許容値を下回った場合にそれが示されます。また、電力ラッチ機能を備えているため、外付けマイクロコントローラ・ユニット (MCU) で出力電圧を必要な期間利用できるようにすることも可能です。

このデバイスは、20 ピン HTSSOP PowerPAD パッケージで供給されます。

6 Pin Configuration and Functions

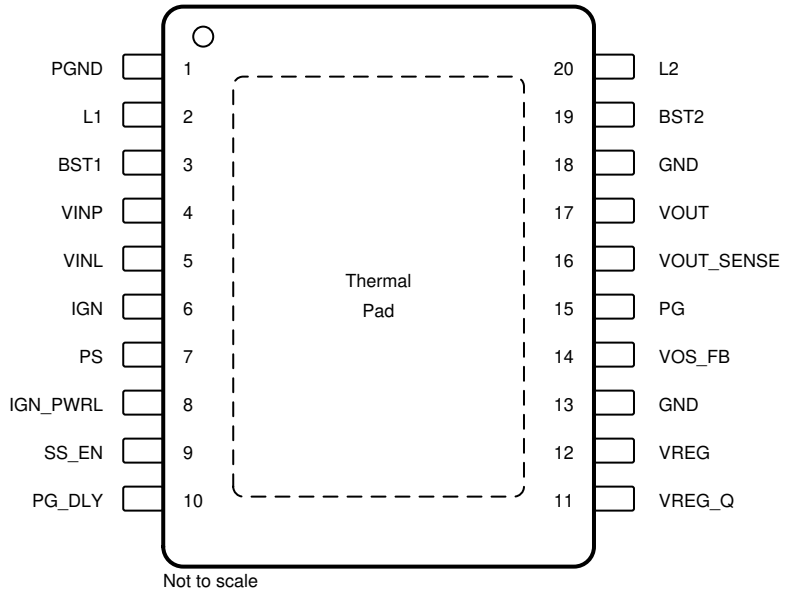

図 6-1. PWP PowerPAD™ Package 20-Pin HTSSOP With Exposed Thermal Pad Top View

表 6-1. Pin Functions

PIN		I/O(1)	TYPE(2)	DESCRIPTION
NAME	NO.			
PGND	1	—	G	Power-ground pin
L1	2	I	A	Buck power-stage switch node. Connect an inductor with a nominal value of 4.7 µH between the L1 and L2 pins.
BST1	3	I	A	Bootstrap node for the buck power stage. Connect a 100-nF capacitor between this pin and the L1 pin.
VINP	4	—	P	Supply-power input voltage. Connect this pin to the input supply line.
VINL	5	—	P	Supply-input voltage for internal biasing. Connect this pin to the input supply line.
IGN	6	I	D	Ignition-enable input signal. The ignition is enabled when this pin is high (1) and is disabled when this pin is low (0).
PS	7	I	D	Logic-level input signal to enable and disable low-power mode. The power mode is low-power mode when this pin is high (1) and is normal mode when this pin is low (1).
IGN_PWRL	8	I	D	Logic-level IGN power-latch signal. The IGN pin is latched when this pin is high (1) and is not latched when this pin is low (0).

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表 6-1. Pin Functions (continued)

PIN		I/O[1]	TYPE[2]	DESCRIPTION
NAME	NO.			
SS_EN	9	I	D	Configuration pin to enable and disable the spread-Spectrum. The spread-spectrum feature is enabled when this pin is open and disabled when this pin is low.
PG_DLY	10	I	A	Configuration pin for power-good delay time. Connect this pin to a resistor with a value from 10kΩ to 100kΩ to configure the PG delay time from 0.5 ms to 40 ms. Connect this pin to ground for the default PG delay time which is 2 ms (typical).
VREG_Q[3]	11	I	A	Quiet feedback pin for the gate-drive supply of the buck-boost power stages. This pin must be connected close to the top side of the 4.7-µF (typical) decoupling capacitor at the VREG output pin.
VREG	12	O	A	Gate-drive supply for the buck-boost power stages. Apply a 4.7-µF (typical) decoupling capacitor at this pin to the power ground. The VREG pin cannot drive external loads in the application.
GND	13	—	G	Analog ground
VOS_FB	14	I	A	For the TPS55160-Q1 and TPS55162-Q1 devices, this pin is used to adjust the VOUT configuration. Connect this pin to a resistive feedback network with less than 1-MΩ total resistance between the VOUT pin, FB pin, and GND pin (analog ground). For the TPS55165-Q1 device, this pin is used to select the output voltage. The output voltage is set to 5 V when this pin is connected to the GND pin. The output voltage is 12 V when this pin is connected to the VREG pin.
PG	15	O	D	Output power good pin. This pin is an open-drain pin. The status of the power-good output is good when this pin is high (1) and has a failure when this pin is low (0)
VOUT_SENSE	16	I	A	Sense pin for the buck-boost converter output voltage. This pin must be connected to the VOUT pin.
VOUT	17	O	A	Buck-boost converter output voltage
GND	18	—	G	Analog ground
BST2	19	I	A	Bootstrap node for the boost power-stage. Connect a typical 100-nF capacitor between this pin and the L2 pin.
L2	20	I	A	Boost power-stage switch node. Connect an inductor with a nominal value of 4.7 µH between the L1 and L2 pins.
PowerPAD		—	—	The thermal pad must be soldered to the power ground to achieve the appropriate power dissipation through the analog ground plane.

(1) I = Input Pin, O = Output Pin
(2) A = Analog Pin, D = Digital Pin, G = Ground Pin, P = Power Pin
(3) The VREG_Q pin must be connected to the VREG pin at all times while the device is in operation to prevent possible electrostatic overstress (EOS) damage to the device.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

POS			MIN	MAX	UNIT
M1.1	Protected battery voltage	VINP, VINL	–0.3	40	V
M1.2	Feedback voltage	VOS_FB	–0.3	5.5	V
M1.3	Low-power mode input	PS	-0.3	40	V
M1.4	Low-voltage inputs	IGN_PWRL, SS_EN, PG_DLY	–0.3	5.5	V
M1.5	Ignition enable input	IGN	–7	40	V
M1.6	Buck-boost output voltage	VOUT, VOUT_SENSE	–0.3	20	V
M1.7	Gate-driver supply	VREG, VREG_Q	–0.3	5.5	V
M1.8	Buck switching node voltage	L1	–0.3	40	V
M1.9	Boost switching node voltage	L2	–0.3	20	V
M1.10	Boot-strap overdrive voltage	BST1-L1, BST2-L2	–0.3	5.5	V
M1.11	Power-good output voltage	PG	-0.3	15	V
M1.12	Ground	PGND, GND	–0.3	0.3	V
M2	Junction temperature, T_J		–40	150	°C
M3	Storage temperature, T_{stg}		–65	175	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted

7.2 ESD Ratings

					VALUE	UNIT
M4	$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
M5.1			Charged-device model (CDM), per AEC Q100-011	All pins	±500	
M5.2				Corner pins (1, 10, 11, and 20)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

POS			MIN	MAX	UNIT
R1.1a	Supply voltage at VINP and VINL pins (after wake-up)	TPS55165-Q1 with VOS_FB pin connected to GND	2	36	V
R1.1b		TPS55165-Q1 with VOS_FB pin connected to VREG	4	36	V
R1.1c		TPS55160-Q1 and TPS55162-Q1	3.6	36	V
R1.2a	Output voltage at VOUT and VOUT_SENSE pins		0	12	V
R1.2b	Output voltage at PG pin		0	5	V
R1.3	Input voltage on IGN pin		0	36	V
R1.4	Input voltage on logic pins IGN_PWRL, PS and SS_EN		0	5	V
R1.5a	Input voltage on VOS_FB pin	TPS55165-Q1	0	5	V
R1.5b		TPS55160/2-Q1	0	0.8	V
R2.1	Operating free air temperature, T_A		–40	125	℃
R2.2	Operating virtual junction temperature, T_J		–40	150	℃

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7.4 Thermal Information

THERMAL METRIC[1]		TPS5516x-Q1 PWP (HTSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics — External Components

Over operating free air temperature range –40°C ≤ T_A ≤ 125°C and maximum junction temperature T_J = 150°C and recommended operating input supply range (unless otherwise noted)[1]

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AN.1	C_{OUT}	Value of output ceramic capacitor	Connect between VOUT and PGND	18	22	47	µF
AN.1a	ESR C_{OUT}	Value of ESR of output capacitor, C_{OUT}		0		100	mΩ
AN.2	C_{BST}	Value of bootstrap ceramic capacitor	ESR < 10 mΩ. Connect between BST1 and L1 with respect to BST2 and L2		100		nF
AN.2a	ESR C_{BST}	Value of ESR of bootstrap ceramic capacitor, C_{BST}		0		10	mΩ
AN3	L	Value of inductor	Saturation current > 2.5 A, ESR < 30 mΩ	3.3	4.7	6.2	µH
AN.3a	DCR L	Value of DCR of inductor		0		40	mΩ
AN.4	C_{IN}	Value of supply input ceramic capacitor	40-V compliant. Connect between VIN and PGND	8.2	10		µF
AN.4a	ESR C_{IN}	Value of ESR of input capacitor, C_{IN}		0		100	mΩ
AN.5	C_{VREG}	Decoupling capacitor on VREG pin to ground	Connect between VREG and PGND	3.9	4.7	5.6	µF
AN.5a	ESR C_{VREG}	Value of ESR of input capacitor, C_{VREG}		0		10	mΩ

(1) The term V_{IN} refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).

7.6 Electrical Characteristics — Supply Voltage (VINP, VINL pins)

Over operating free air temperature range –40°C ≤ T_A ≤ 125°C and maximum junction temperature T_J = 150°C and recommended operating input supply range (unless otherwise noted)[1]

POS	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
1.1a	V_{IN}	Operating supply input voltage	Applied at VINP and VINL pins, after device startup	TPS55165-Q1 with VOS_FB pin connected to GND	2	14	36	V
1.1b				TPS55165-Q1 with VOS_FB pin connected to VREG	4	14	36	
1.1c				TPS55160/2-Q1	3.6	14	36	V
1.2	$V_{IN\_startup}$	Minimum input voltage for startup	Applied at VINP and VINL pins; T_J = 25°C. This minimum voltage is required until VOUT > PG_{TH_UV}; I_{VOUT} < 400 mA, C_{VOUT} = 22 µF		5.3			V
1.3	I_{SD}	VIN Shutdown supply current	V_{IN} = 12 V, V_{IGN}= 0 V, V_{PS}= 0 V, V_{IGN_PWRL} = 0 V, T_J = 25°C				3	µA

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Over operating free air temperature range –40°C ≤ T_A ≤ 125°C and maximum junction temperature T_J = 150°C and recommended operating input supply range (unless otherwise noted)(1)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.4	I_Q	VIN Quiescent supply current	TPS55165-Q1: V_{IN} = V_{IGN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 0 mA, T_J = 25°C Device in low-power mode, Non-switching VOS_FB pin connected to GND	0		15	µA

(1) The term V_{IN} refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).

7.7 Electrical Characteristics — Reference Voltage (VOS_FB Pin) and Output Voltage (VOUT Pin)

Over operating free air temperature range –40°C ≤ T_A ≤ 125°C and maximum junction temperature T_J = 150°C and recommended operating input supply range (unless otherwise noted)(1)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
2.1a	$V_{FB\_NM\_adj}$	Feedback voltage in normal mode for adjustable V_{OUT} setting(2)	TPS55160/2-Q1: Measured at VOS_FB pin Resistive divider with total resistance < 1 MΩ connected between VOUT, VOS_FB, and GND pins	0.784	0.8	0.816	V
2.1b	$V_{FB\_NM\_5V}$	Feedback voltage in normal mode for V_{OUT} in fixed 5-V setting(2)	TPS55165-Q1: Measured at VOUT_SENSE pin VOS_FB pin connected to GND; VOUT pin connected to VOUT_SENSE	4.9	5	5.1	V
2.1c	$V_{FB\_NM\_12V}$	Feedback voltage in normal mode for V_{OUT} in fixed 12-V setting(2)	TPS55165-Q1: Measured at VOUT_SENSE pin VOS_FB pin connected to VREG; VOUT pin connected to VOUT_SENSE	11.76	12	12.24	V
2.2a	$V_{FB\_PS\_adj}$	Feedback voltage in low-power mode for adjustable V_{OUT} setting(3)	TPS55160/2-Q1: Measured at VOS_FB pin Resistive divider with total resistance < 1 MΩ connected between VOUT, VOS_FB, and GND pins	0.776	0.8	0.824	V
2.2b	$V_{FB\_PS\_5V}$	Feedback voltage in low-power mode for V_{OUT} in 5-V setting(3)	TPS55165-Q1: Measured at VOUT_SENSE pin VOS_FB pin connected to GND; VOUT pin connected to VOUT_SENSE	4.85	5	5.15	V
2.2c	$V_{FB\_PS\_12V}$	Feedback voltage in low-power mode for V_{OUT} in 12-V setting(3)	TPS55165-Q1: Measured at VOUT_SENSE pin VOS_FB pin connected to VREG; VOUT pin connected to VOUT_SENSE	11.64	12	12.36	V
2.3	V_{OUT_OL}	Adjustable output voltage range	TPS55160/2-Q1: Measured at VOUT_SENSE pin	5.7		9	V
2.6	Rpd_{VOUT}	Pulldown discharge resistance at VOUT	Device in OFF state, INIT state, or PRE_RAMP state; V_{IGN} = 0 V, V_{PS} = 0 V, V_{IGN_PWRL} = 0 V	250	365	850	Ω

(1) The term V_{IN} refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).
(2) V_{PS}= 0 V; Average DC value excluding ripple and load transients for V_{IN} and load current ranges as specified in I_{VOUT}. Inclusive DC line and load regulation, temperature drift, and long term drift.
(3) V_{PS}= 5 V; Average DC value excluding ripple and load transients for V_{IN} and load current ranges as specified in I_{VOUT}. Inclusive DC line and load regulation, temperature drift, and long term drift.

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7.8 Electrical Characteristics — Buck-Boost

Over operating free air temperature range –40°C ≤ T_A ≤ 125°C and maximum junction temperature T_J = 150°C and recommended operating input supply range (unless otherwise noted)(1)

POS	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
3.1a	I_{OUT_5V}	Max output current in normal operation for VOUT in 5-V setting	TPS55165-Q1 with VOS_FB pin connected to GND	6 V ≤ V_{IN}; DCR ≤ 40 mΩ	1			A
3.1b				3.8 V ≤ V_{IN} ≤ 6 V; DCR ≤ 40 mΩ	800			mA
3.1c				2.3 V ≤ V_{IN} < 3.8 V; DCR ≤ 40 mΩ	400			
3.1d				2 V ≤ V_{IN} < 2.3 V; DCR ≤ 40 mΩ	200			
3.1e	I_{OUT_12V}	Max output current in normal operation for VOUT in 12-V setting	TPS55165-Q1 with VOS_FB pin connected to VREG	14 V ≤ V_{IN}; DCR ≤ 40 mΩ	800			mA
3.1f				9.2 V≤ V_{IN} ≤ 14 V; DCR ≤ 40 mΩ	600			
3.1g				5.6 V≤ V_{IN} < 9.2 V; DCR ≤ 40 mΩ	300			
3.1h				4 V ≤ V_{IN} < 5.6 V; DCR ≤ 40 mΩ	150			
3.2a	$I_{OUT\_adj\_VoutH}$	Max output current in normal operation for adjustable configuration, 8V < V_{OUT} ≤ 9V	TPS55160-Q1 and TPS55162-Q1, 8V < V_{OUT} ≤ 9V	(V_{OUT} + 2V) ≤ V_{IN}; DCR ≤ 40 mΩ	800			mA
3.2b				0.76 * V_{OUT} ≤ V_{IN} ≤ (V_{OUT} + 2V); DCR ≤ 40 mΩ	600			
3.2c				0.46 * V_{OUT} ≤ V_{IN} < 0.76 * V_{OUT}; DCR ≤ 40 mΩ	300			mA
3.2d				3.6 V ≤ V_{IN} < 0.46 * V_{OUT}; DCR ≤ 40 mΩ	150			mA
3.2e	$I_{OUT\_adj\_VoutL}$	Max output current in normal operation for adjustable configuration, 5.7V ≤ V_{OUT} ≤ 8V	TPS55160-Q1 and TPS55162-Q1, 5.7V ≤ V_{OUT} ≤ 8V	(V_{OUT} + 1V) ≤ V_{IN}; DCR ≤ 40 mΩ	800			mA
3.2f				0.76 * V_{OUT} ≤ V_{IN} < (V_{OUT} + 1V); DCR ≤ 40 mΩ	600			
3.2g				3.6 V ≤ V_{IN} < 0.76 * V_{OUT}; DCR ≤ 40 mΩ	300			
3.11	I_{OUT_PS}	Max output current in low-power mode			50			
3.3	$R_{dson\_BUCK\_HS}$	On-resistance buck-stage high-side (HS) FET				150	300	mΩ
3.4	$R_{dson\_BUCK\_LS}$	On-resistance buck-stage low-side (LS) FET				150	300	mΩ
3.5	$R_{dson\_BOOST\_HS}$	On-resistance boost-stage HS FET				150	300	mΩ
3.6	$R_{dson\_BOOST\_LS}$	On-resistance boost-stage LS FET				150	300	mΩ
3.7	I_{SW_limit}	Peak current limit for HS buck, LS buck, and LS boost	Device in normal operating mode		2	3.5	4.5	A
3.9	$I_{CoilAvglimit}$	Average coil current limit	Device in normal operating mode; L = 4.7 µH			2	2.8	A
3.20a	$V_{TLDSR\_5V\_100}$	Transient load step response for VOUT in 5-V setting	TPS55165-Q1: Measured at VOUT_SENSE pin; VOS_FB pin connected to GND; V_{IN} = 12 V, I_{OUT} = 0.1 A to 0.5 A, T_R = T_F = 1 µs, C_{OUT} = 47 µF			5		
3.20b	$V_{TLDSR\_5V\_500}$	Transient load step response for VOUT in 5-V setting	TPS55165-Q1: Measured at VOUT_SENSE pin; VOS_FB pin connected to GND; V_{IN} = 12 V, I_{OUT} = 0.5 A to 1 A, T_R = T_F = 1 µs, C_{OUT} = 47 µF			5		
3.21a	V_{RIPPLE_5V}	Output ripple for VOUT in 5-V setting	TPS55165-Q1: Measured at VOUT_SENSE pin; VOS_FB pin connected to GND; V_{IN} = 12V, I_{OUT} = 1 A, SS_EN = low			5.5		mVpp
3.21b	V_{RIPPLE_12V}	Output ripple for VOUT in 12-V setting	TPS55165-Q1: Measured at VOUT_SENSE pin; VOS_FB pin connected to VREG; V_{IN} = 14V, I_{OUT} = 0.8 A, SS_EN = low			5		mVpp

(1) The term V_{IN} refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).

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7.9 Electrical Characteristics — Undervoltage and Overvoltage Lockout

Over operating free air temperature range –40°C ≤ T_A ≤ 125°C and maximum junction temperature T_J = 150°C and recommended operating input supply range (unless otherwise noted)(1)

POS	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
4.1a	UVLO	V_{IN} Undervoltage (UV) lockout threshold	V_{IN} voltage decreasing; Device turned-off when V_{IN} < UVLO Device is in normal operating mode	TPS55165-Q1 with VOS_FB pin connected to GND	1.8		2	V
4.1b				TPS55165-Q1 with VOS_FB pin connected to VREG	3.6		4	V
4.1c	UVLO	V_{IN} Undervoltage (UV) lockout threshold	V_{IN} voltage decreasing; Device turned-off when V_{IN} < UVLO Device is in normal operating mode	TPS55160-Q1 and TPS55162-Q1	1.8		2	V
4.2	OVLO	V_{IN} Overvoltage (OV) lockout threshold	V_{IN} voltage increasing; Device stops switching when V_{IN} > OVLO, and recovers when V_{IN} < OVLO and IGN = 1 Device is in normal operating mode		36		40	V
4.9	$V_{OUT\_PROT\_OV}$	VOUT OV protection	Device is in normal operating mode		110%		125%	

(1) The term V_{IN} refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).

7.10 Electrical Characteristics — IGN Wakeup

Over operating free air temperature range –40°C ≤ T_A ≤ 125°C and maximum junction temperature T_J = 150°C and recommended operating input supply range (unless otherwise noted)(1)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
5.1a	IGN_{WAKE}	IGN wake-up threshold	V_{IGN} voltage increasing to wake-up device	2.5	3.1	3.7	V
5.1b	IGN_{PD}	IGN power-down threshold	V_{IGN} voltage decreasing to power-down device	1.5	2.1	2.7	V
5.2	IGN_{HYST}	IGN wake-up hysteresis		0.76	1	1.35	V
5.3a	I_IGN_{36V}	IGN pin forward input current at 36 V	V_{IGN} = 36 V	11	17	30	µA
5.3b	I_IGN_{12V}	IGN pin forward input current at 12 V	V_{IGN} = 12 V	2.3	3.7	7.1	µA
5.5	I_IGN_{rev}	IGN pin reverse current	V_{IGN} = –7 V		370	650	µA

(1) The term V_{IN} refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).

7.11 Electrical Characteristics — Logic Pins PS, IGN_PWRL, SS_EN

Over operating free air temperature range –40°C ≤ T_A ≤ 125°C and maximum junction temperature T_J = 150°C and recommended operating input supply range (unless otherwise noted)(1)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
6.1	$V_{LOGIC\_IN\_HIGH}$	Logic input low-to-high threshold for pins IGN_PWRL PS, and SS_EN	Device in power-up condition	2			V
6.2	$V_{LOGIC\_IN\_LOW}$	Logic Input high-to-low threshold for pins IGN_PWRL, PS, and SS_EN	Device in power-up condition			0.74	V
6.3	$V_{LOGIC\_IN\_HYST}$	Logic input hysteresis for pins IGN_PWRL, PS, and SS_EN	Device in power-up condition	0.15		0.39	V
6.4	$R_{LOGIC\_IN\_PD}$	Pulldown resistance on PS pin to GND		35	70	111	kΩ
6.5	$I_{pull\text{-}up\_SS\_EN}$	Pullup current on SS_EN pin		85		266	µA

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Over operating free air temperature range –40°C ≤ T_A ≤ 125°C and maximum junction temperature T_J = 150°C and recommended operating input supply range (unless otherwise noted)(1)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
6.6	$I_{pull-up\_IGN\_PWRL}$	Pullup current on IGN_PWRL pin		1		8	µA

(1) The term V_{IN} refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).

7.12 Electrical Characteristics – Overtemperature Protection

Over operating free air temperature range –40°C ≤ T_A ≤ 125°C and maximum junction temperature T_J = 150°C and recommended operating input supply range (unless otherwise noted)(1)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
7.1	T_{PROT}	Overtemperature shutdown protection threshold		175		210	℃
7.2	T_{HYS}	Overtemperature shutdown hysteresis			30		

(1) The term V_{IN} refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).

7.13 Electrical Characteristics – Power Good

Over operating free air temperature range –40°C ≤ T_A ≤ 125°C and maximum junction temperature T_J = 150°C and recommended operating input supply range (unless otherwise noted)(1)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
8.1	PG_{TH_UV}	PG threshold undervoltage	Deviation from nominal V_{OUT} to assert PG low, in normal mode	–10%		–5%	
			Deviation from nominal V_{OUT} to assert PG low, during low power mode to normal mode transition		-12%		
			Deviation from nominal V_{OUT} to assert PG low, in low power mode	-20%		-5%	
8.2	V_{PG_LOW}	PG output-low voltage	IPGL ≤ 1mA			0.4	V

(1) The term V_{IN} refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).

7.14 Switching Characteristics — Reference Voltage (VOS_FB Pin) and Output Voltage (VOUT Pin)

Over operating free air temperature range –40°C ≤ T_A ≤ 125°C and maximum junction temperature T_J = 150°C and recommended operating input supply range (unless otherwise noted)(1)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
2.5	t_{start_VOUT}	VOUT startup time	L = 4.7 µH, C_{OUT} = 22 µF; V_{OUT} rising from 10% to 90% of final value		1.5		ms

(1) The term V_{IN} refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).

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7.15 Switching Characteristics — Buck-Boost

Over operating free air temperature range –40°C ≤ T_A ≤ 125°C and maximum junction temperature T_J = 150°C and recommended operating input supply range (unless otherwise noted)(1)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
3.8	t_{blank_Iswlim}	Time until peak current limit is active	V_{IN} = 14 V	40		70	ns
3.11	f_{SW}	Switching frequency without Spread-Spectrum	V_{IN_max} = 27 V	1860	2000	2140	kHz
3.12	f_{SW_SS}	Switching frequency with Spread-Spectrum Enabled	V_{IN_max} = 27 V; SS_EN pin not connected to GND; Device in buck operation	1800	2100	2400	kHz
3.14	$t_{on\_Min\_Buck}$	Minimum on time in buck operation	Device in normal operation mode		55	65	ns
3.15	$t_{on\_Max\_Boost}$	Maximum on time in boost operation	Device in normal operation mode	350	400	450	ns
3.16	$t_{on\_Max\_Bst\_LPM}$	Maximum boost on time in power save mode			4		µs

(1) The term V_{IN} refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).

7.16 Switching Characteristics — Undervoltage and Overvoltage Lockout

Over operating free air temperature range –40°C ≤ T_A ≤ 125°C and maximum junction temperature T_J = 150°C and recommended operating input supply range (unless otherwise noted)(1)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.3	$t_{degl\_VINUVOV}$	V_{IN} UV and OV deglitch time		40	50	60	µs
4.8	$t_{degl\_VREGUVOV}$	VREG UV and OV deglitch time			10		µs

(1) The term V_{IN} refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).

7.17 Switching Characteristics — IGN Wakeup

Over operating free air temperature range –40°C ≤ T_A ≤ 125°C and maximum junction temperature T_J = 150°C and recommended operating input supply range (unless otherwise noted)(1)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
5.6	IGN_deg	IGN deglitch filter time		7.5		22	ms
5.7	$IGN_{startup\_time}$	Time from IGN high till VOUT crossing 95% of the end-value				25	ms

(1) The term VIN refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).

7.18 Switching Characteristics — Logic Pins PS, IGN_PWRL, SS_EN

Over operating free air temperature range –40°C ≤ T_A ≤ 125°C and maximum junction temperature T_J = 150°C and recommended operating input supply range (unless otherwise noted)(1)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
6.7	$t_{Delay\_IGN\_PWRL}$	Input Delay time for IGN_PWRL pin	Delay time betweein the toggling of the IGN_PWRL pin and the state change of the signal inside the device	213	256	272	µs
6.8a	$t_{Delay\_PS\_L2H}$	Input Delay time for PS pin pulling high	Delay time between pullping the PS high and the device enters low-power mode	59		136	µs
6.8b	$t_{Delay\_PS\_H2L}$	Input Delay time for PS pin going low	Delay time between releasing the PS pin and the device enters normal mode from low-power mode	262		510	µs

(1) The term V_{IN} refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).

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7.19 Switching Characteristics – Power Good

Over operating free air temperature range –40°C ≤ T_A ≤ 125°C and maximum junction temperature T_J = 150°C and recommended operating input supply range (unless otherwise noted)(1)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
8.3	$PG_{Deglitch}$	PG deglitch filter time		45	50	55	µs
8.4a	$PG_{exttime}$	PG extension time (rising edge only)	PG_DLY Shorted to VREG		40		ms
8.4b			100 kΩ between PG_DLY and GND		30		
8.4c			10 kΩ between PG_DLY and GND		4		ms
8.4d			PG_DLY grounded		0.7		ms

(1) The term V_{IN} refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).

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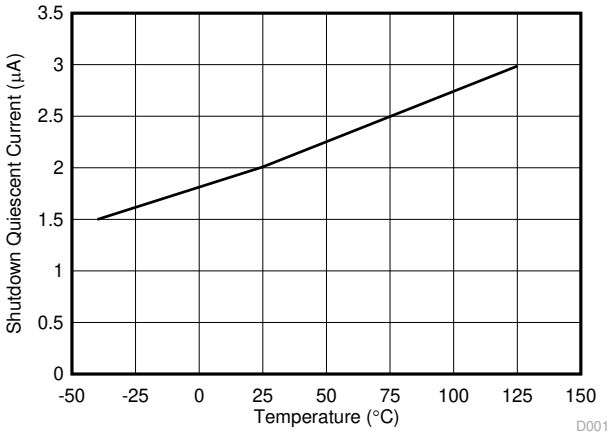
7.20 Typical Characteristics



V_{IN} = 12 V

図 7-1. Shutdown I_Q vs Temperature

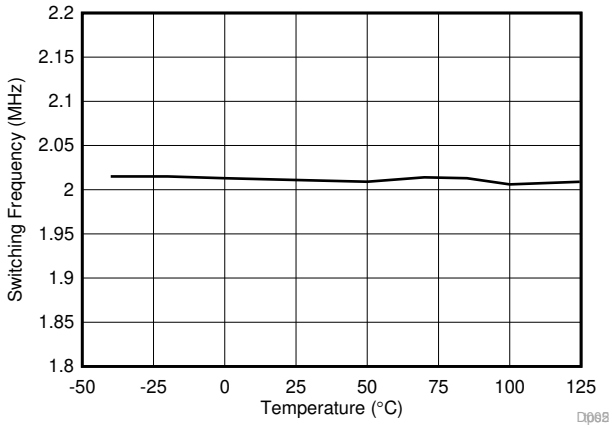


図 7-2. Switching Frequency vs Temperature

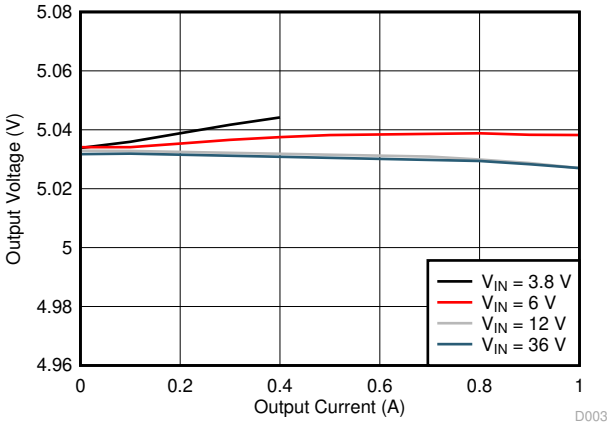


図 7-3. 5-V Output Regulation vs Load Current

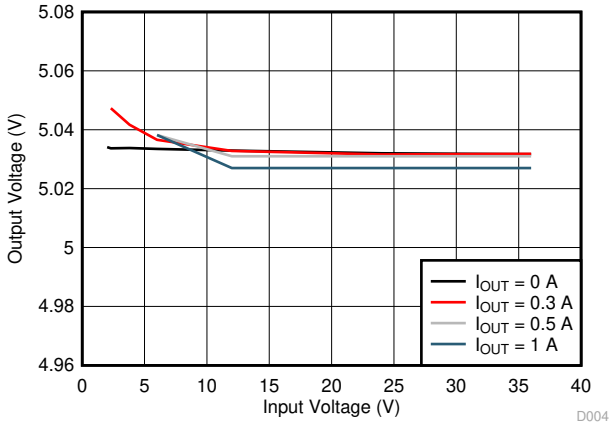


図 7-4. 5-V Output Regulation vs Input Voltage

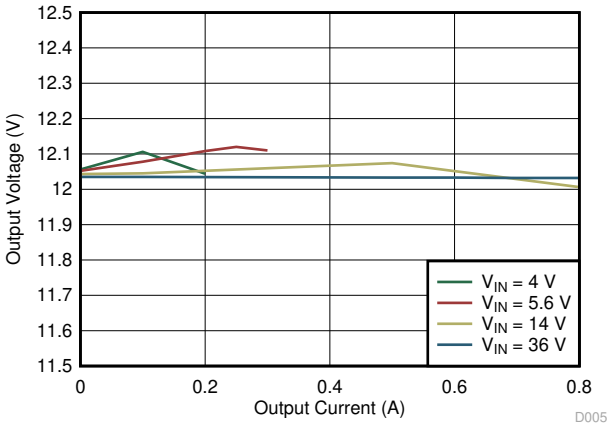


図 7-5. 12-V Output Regulation vs Load Current

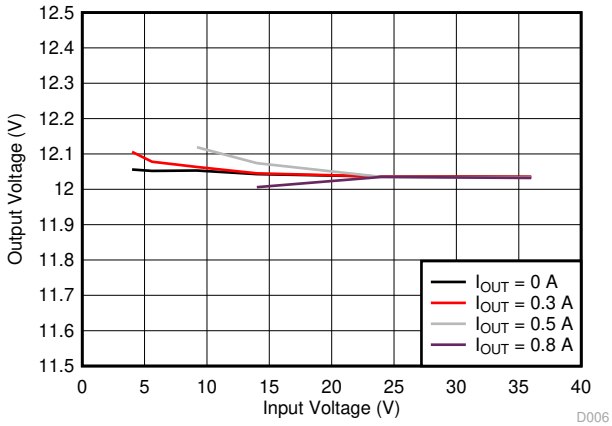


図 7-6. 12-V Output Regulation vs Input Voltage

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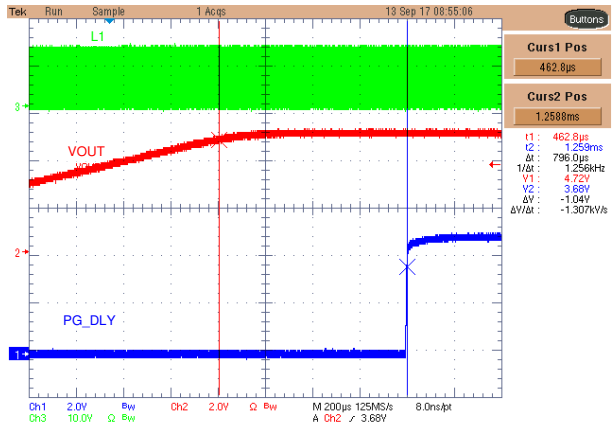
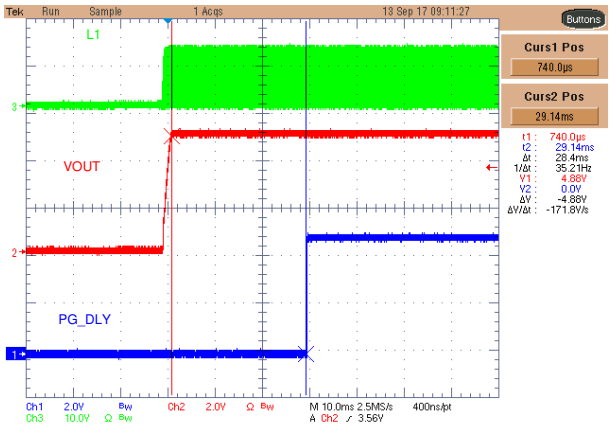
7.20 Typical Characteristics (continued)



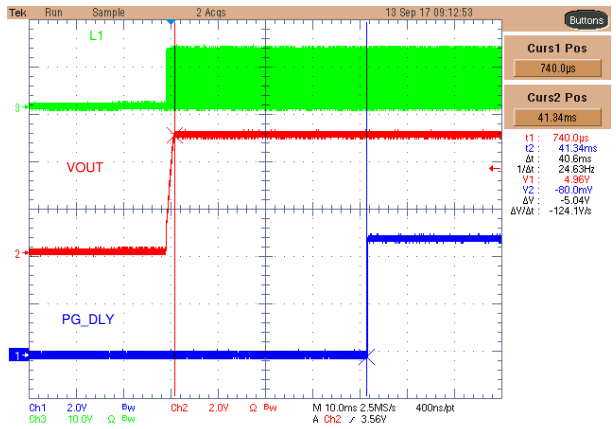
V_{IN} = 12 V V_{OUT} = 5 V

図 7-7. Power-Good Delay When PGDLY Is Grounded



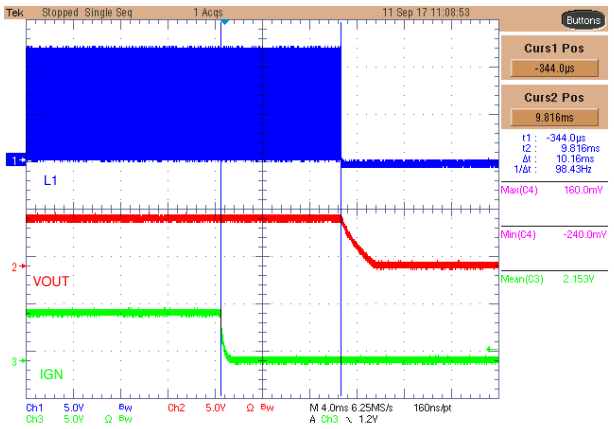
V_{IN} = 12 V V_{OUT} = 5 V

図 7-8. Power-Good Delay When PGDLY Connects to 100-kΩ Resistor



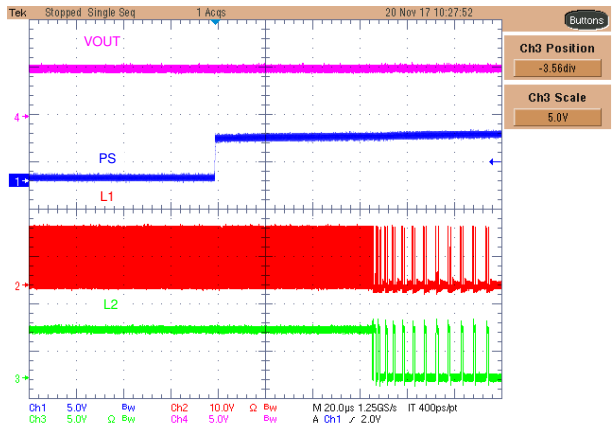
V_{IN} = 12 V V_{OUT} = 5 V

図 7-9. Power-Good Delay When PGDLY Connects to VREG



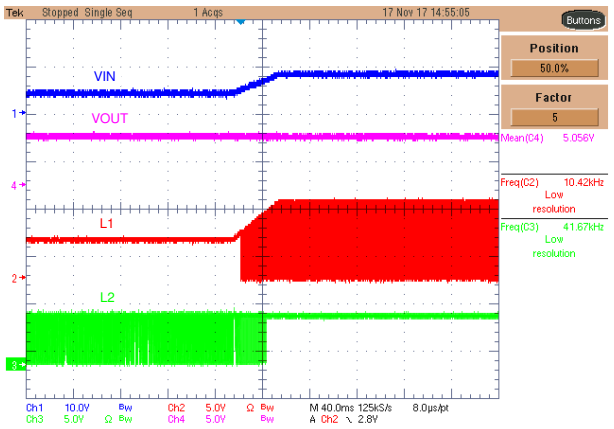
V_{IN} = 14 V V_{OUT} = 5 V I_{OUT} = 0 A

図 7-10. Ignition Shutdown Sequence



V_{IN} = 12 V V_{OUT} = 5 V I_{OUT} = 50 mA

図 7-11. Low-Power Mode Enabling



4 V ≤ V_{IN} ≤ 12 V V_{OUT} = 5 V I_{OUT} = 0.5 A

図 7-12. Step-Up to Step-Down Mode Transition

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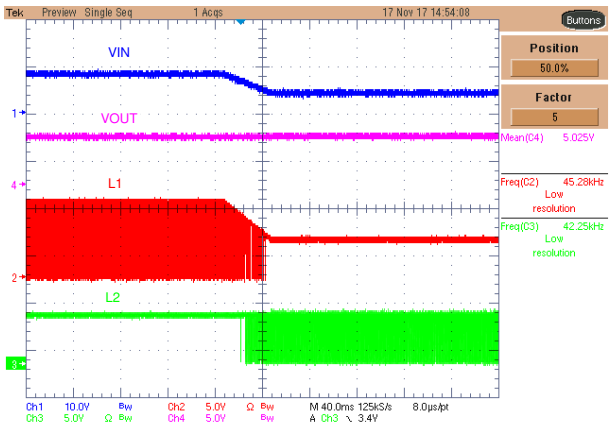
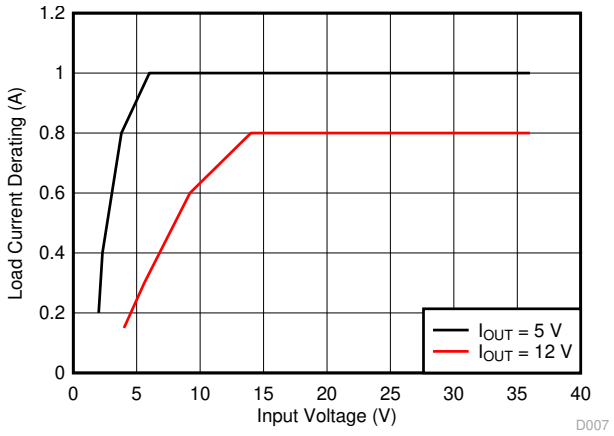
7.20 Typical Characteristics (continued)



$4\ V \le V_{IN} \le 8\ V$ $V_{OUT} = 5\ V$ $I_{OUT} = 0.5\ A$

図 7-13. Step-Down to Step-Up Mode Transition



A.

図 7-14. Load Current Derating vs Input Voltage

8 Detailed Description

8.1 Overview

The control circuit of the TPS5516x-Q1 buck-boost converter is based on an average current-mode topology. The control circuit also uses input and output voltage feedforward. Changes of input and output voltage are monitored and the duty cycle in the modulator is immediately adapted to achieve a fast response to those changes. The voltage error amplifier gets its feedback input from the VOS_FB pin. The feedback voltage is compared with the internal reference voltage to generate a stable and accurate output voltage.

The buck-boost converter uses four internal N-channel MOSFETs to maintain synchronous power conversion at all possible operating conditions. This feature enables the device to keep high efficiency over a wide input voltage and output power range. To avoid ground shift problems caused by the high currents in the switches, separate ground pins (GND and PGND) are used. The reference for all control functions are the GND pins. The power switches are connected to the PGND pins. Both grounds must be connected on the PCB at only one point which is ideally close to the GND pin. Because of the 4-switch topology, the load is always disconnected from the input during shutdown of the converter.

To drive the high-side switches of the buck and the boost power stages, the buck-boost converter requires external boot-strapping ceramic capacitors with low ESR. These bootstrap capacitors are charged by the VREG supply. The VREG supply requires a low-ESR ceramic capacitor for loop stabilization, and must not be loaded by the external application. The VREG supply is also used to drive the low-side switches of the buck and boost power stages. At device start-up, the VREG pin is supplied by the input voltage. When the buck-boost output voltage is greater than its power-good threshold (the PG pin is high), the VREG pin is supplied by the output voltage to reduce power dissipation.

The device can be enabled with the IGN pin, and, when enabled, the device has a power-latch function which can be selected with the IGN_PWRL pin. This function allows an external MCU to keep TPS5516x-Q1 device on even after the IGN pin goes low.

For the TPS55160-Q1 and TPS55165-Q1 devices, the operation mode of the buck-boost converter can be selected through the PS pin. When the PS pin is low, the buck-boost operates in normal mode with a constant fixed switching frequency. When the PS pin is high, the buck-boost operates in low-power mode with pulse-frequency modulation.

The TPS55160-Q1 and TPS55165-Q1 devices also have a frequency spread-spectrum option that can be enabled or disabled through the SS_EN pin.

The output voltage of the TPS55165-Q1 device is selected as a fixed 5 V or fixed 12 V through the VOS_FB pin. The TPS55160-Q1 and TPS55162-Q1 devices have an adjustable output voltage from 5.7 V to 9 V through an external feedback network.

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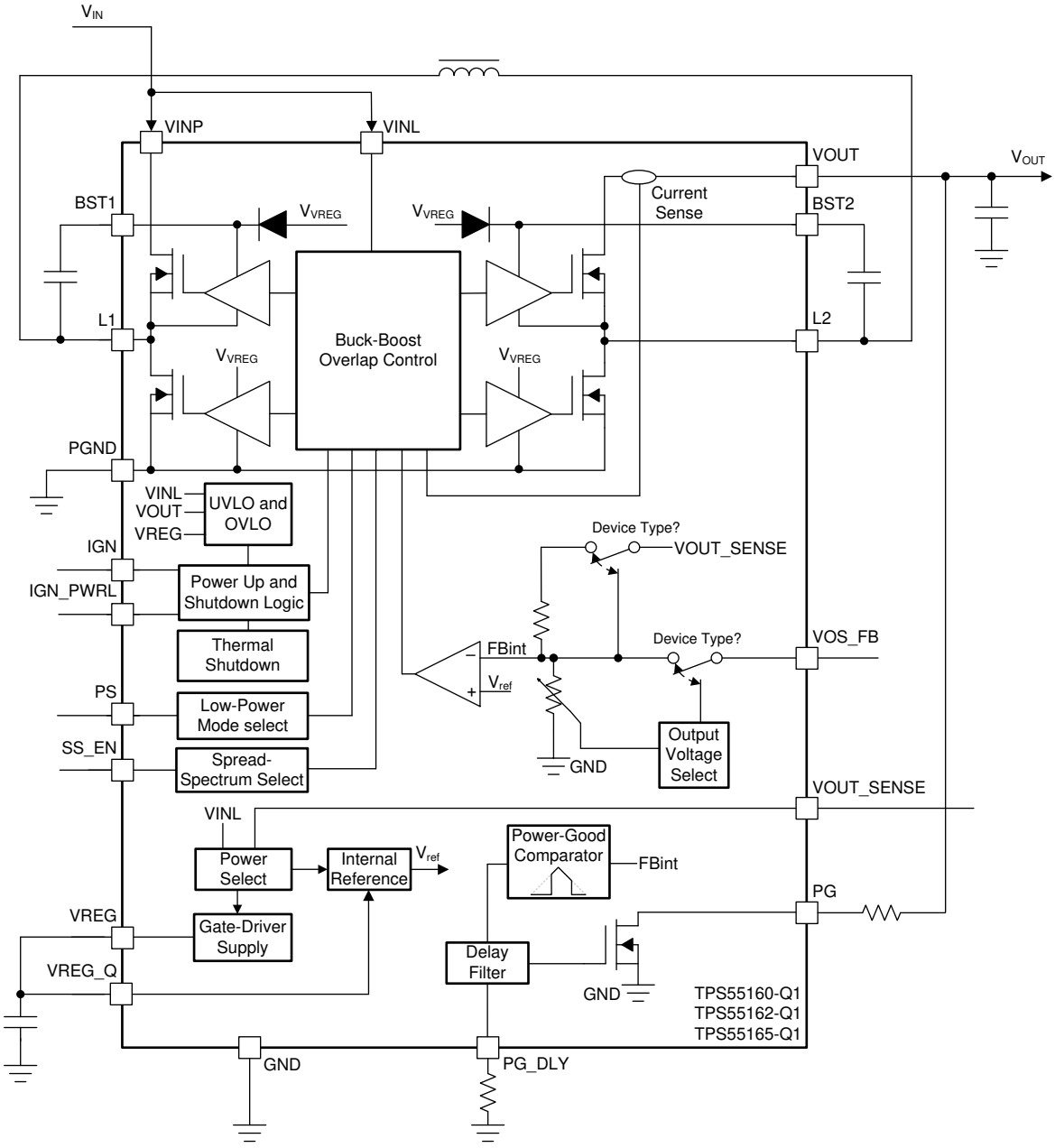
8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Spread-Spectrum Feature

The TPS55160-Q1 and TPS55165-Q1 devices have a spread-spectrum feature to modulate the switching frequency through a pseudo-random algorithm.

This spread-spectrum feature is enabled and disabled through the SS_EN pin. When the SS_EN pin is unconnected, the spread-spectrum feature is enabled. The SS_EN pin is internally pulled up with a pullup current between 100 µA and 200 µA. When the SS_EN pin is connected to ground, the spread-spectrum feature is disabled.

This feature can only be enabled when the device is in normal mode with step-down operation. This feature cannot be enabled in low-power mode.

8.3.2 Overcurrent Protection

The buck-boost regulator has two ways of protecting against overcurrent conditions. When the buck-boost is in regulation (essentially the output voltage is at the target voltage), the average current limit provides the protection against overcurrent conditions. When the average current limit is activated (essentially the maximum inductor average current is reached), the output voltage gradually decreases, but the control loop tries to maintain the target output voltage. So when the overcurrent condition clears before the buck-boost control circuit gets too far out of regulation, the output voltage gradually reaches its target voltage level again.

The buck-boost regulator limits the peak-overcurrent in the power MOSFETs. When such a peak-overcurrent event occurs, the device goes into the PRE_RAMP state and a 12-ms time-out is started. The device restarts and goes from the PRE_RAMP state to the RAMP state after this 12-ms time-out expires and the IGN pin is high.

When the device operates in low-power mode, both the average current limit and the peak-current limit protection functions are disabled.

8.3.3 Overtemperature Protection

The internal power MOSFETs are protected against excess power dissipation with junction overtemperature protection. In case of a detected overtemperature condition, the TPS55165-Q1 device goes to the PRE_RAMP state (the buck-boost regulator is switched off and the VREG supply is enabled) and a 12-ms time-out is started when the overtemperature condition is cleared. The device restarts in the PRE_RAMP state after this 12-ms time-out expires, the overtemperature condition disappeared, and the IGN pin is high.

When the device operates in low-power mode, this overtemperature protection function is disabled.

8.3.4 Undervoltage Lockout and Minimum Start-Up Voltage

The TPS55165-Q1 device has an undervoltage lockout (UVLO) function. When the device operates in normal mode (the PS pin is low), this UVLO function puts the device in the OFF state when the input voltage is less than the UVLO threshold. The device restarts when the IGN pin is high and the input voltage is greater than or equal to the minimum input voltage for start-up, which must be maintained until the output voltage is greater than the PG undervoltage threshold.

When the device operates in low-power mode, this UVLO function is disabled.

8.3.5 Overvoltage Lockout

The TPS55165-Q1 device has an overvoltage lockout (OVLO) function. When the input voltage is greater than the OVLO threshold while the device operates in normal mode (the PS pin is low), this OVLO function puts the device in the PRE_RAMP state (the buck-boost regulator is switched off and the VREG supply is enabled), and a 12-ms time-out starts. The device restarts in the PRE_RAMP state after this 12-ms time-out expires, the input voltage is less than the OVLO threshold, and the IGN pin is high.

When the device operates in low-power mode, this OVLO function is disabled.

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8.3.6 VOUT Overvoltage Protection

When the device operates in normal mode (the PS pin is low) and the output voltage is greater than or equal to the VOUT overvoltage protection, the device goes to the PRE_RAMP state (the buck-boost regulator is switched-off and the VREG supply is enabled) and a 12-ms time-out starts when the output voltage is less than the VOUT overvoltage protection. The device restarts in the PRE_RAMP state after this 12-ms time-out expires, the output voltage is less than the VOUT overvoltage protection, and the IGN pin is high.

When the device operates in low-power mode, this VOUT overvoltage protection function is disabled.

8.3.7 Power-Good Pin

The power-good (PG) pin is a low-side FET open-drain output which is released as soon as the output voltage is greater than the PG undervoltage threshold (essentially the output voltage is rising) and the extension time ($PG_{exttime}$) is expired. The intended usage of this pin is to release the reset of an external MCU. Therefore, the logic-input signals (IGN_PWRL and PS) are considered to be valid only when the PG pin reaches the high level.

When the output voltage is less than the PG undervoltage threshold (essentially the output voltage is falling) for a time longer than the PG deglitch filter time, the PG pin is pulled low. When the PG pin is low, the level of the PS and IGN_PWRL pins is interpreted as low, regardless of the actual level. The device goes to the OFF state if the IGN pin is low under this condition. For more information on the behavior of the PG pin for rising and falling output voltage, see 図 8-2 through 図 8-6.

The PG pin is operational in low-power mode. The PG extension time can be configured by connecting the PG_DLY pin to the VREG pin, the GND pin, or through an external resistor with a value from 10 kΩ to 100 kΩ to the GND pin. The extension time is as follows for the listed configurations:

- When the PG_DLY pin is shorted to the VREG pin, the typical PG extension time is 40 ms.
- When the PG_DLY pin is connected to the GND pin, the typical PG extension time is 0.6 ms.
- When the external resistor between the PG_DLY and GND pins has a value of 10 kΩ, the typical PG extension time is 3 ms.
- When the external resistor between pin the PG_DLY and GND pins has a value of 100 kΩ, the typical PG extension time is 30 ms.

8.4 Device Functional Modes

8.4.1 State Diagram

図 8-1 shows the state diagram.

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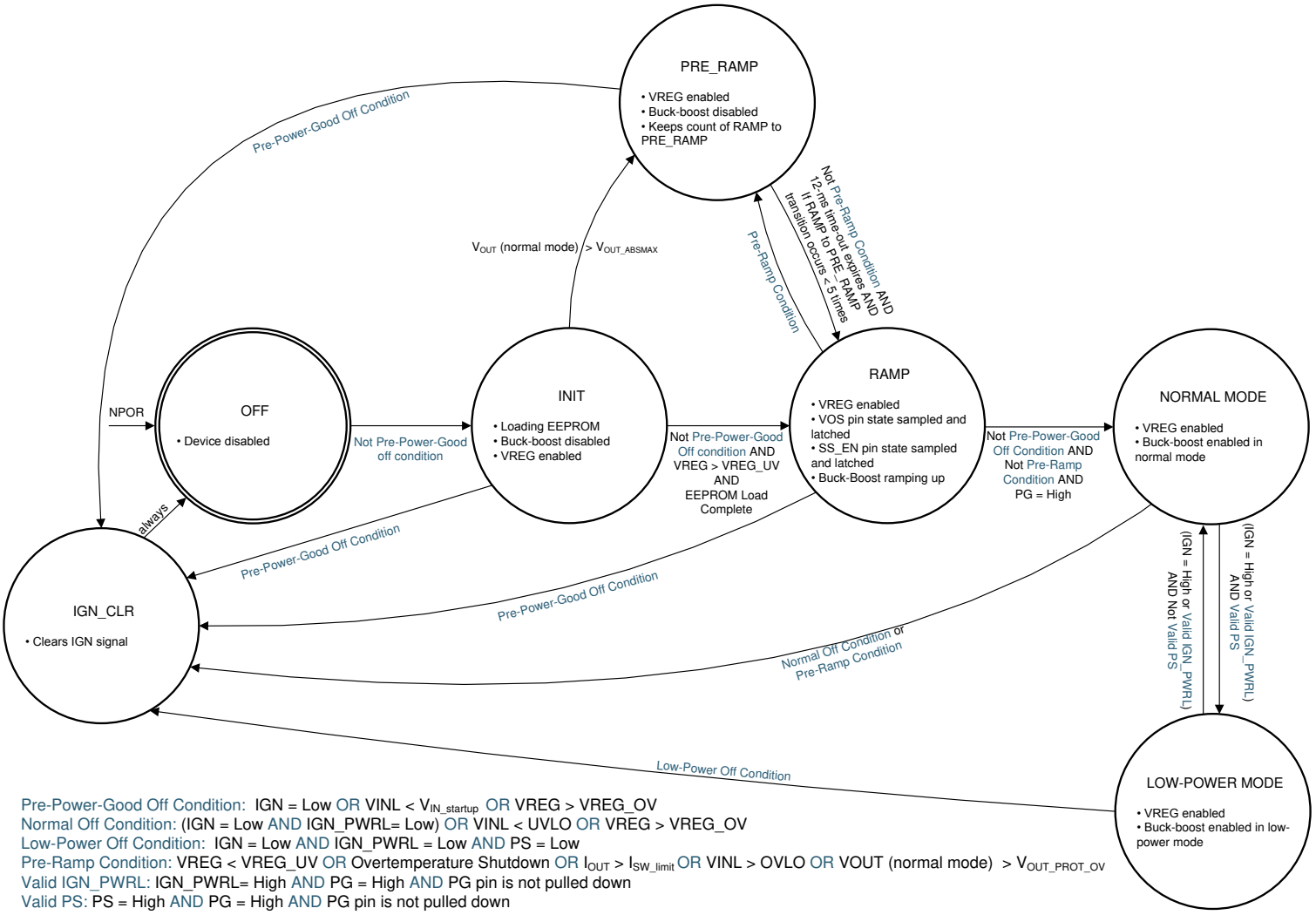

Pre-Power-Good Off Condition: IGN = Low OR VINL < $V_{IN\_startup}$ OR VREG > VREG_OV
Normal Off Condition: (IGN = Low AND IGN_PWRL= Low) OR VINL < UVLO OR VREG > VREG_OV
Low-Power Off Condition: IGN = Low AND IGN_PWRL = Low AND PS = Low
Pre-Ramp Condition: VREG < VREG_UV OR Overtemperature Shutdown OR I_{OUT} > I_{SW_limit} OR VINL > OVLO OR VOUT (normal mode) > $V_{OUT\_PROT\_OV}$
Valid IGN_PWRL: IGN_PWRL= High AND PG = High AND PG pin is not pulled down
Valid PS: PS = High AND PG = High AND PG pin is not pulled down

- The 12-ms time-out from the PRE_RAMP state to the RAMP state starts only when all conditions for going to the RAMP state are satisfied. As soon as one of these conditions is violated, the 12-ms time-out is reset.
- The oscillator is turned off in low-power mode. The oscillator is turned back on upon detecting a negative edge on the PS pin, or a negative edge on the PG pin which requires the device to go out of low-power mode and enter normal mode again.

図 8-1. State Diagram

8.4.2 Modes of Operation

The operational mode of the buck-boost converter is selected through the PS pin. When the PS pin is low, the buck-boost operates in normal mode with a constant fixed switching frequency. When the PS pin is high, the buck-boost operates in low-power mode with pulse-frequency modulation.

8.4.2.1 Normal Mode

To regulate the output voltage at all possible input voltage conditions, the buck-boost converter automatically switches from step-down operation to boost operation and back as required by the configuration. The regulator always uses one active switch, one rectifying switch, one always-on switch, and one always-off switch. Therefore, the regulator operates as a step-down converter (buck) when the input voltage is higher than the output voltage, and as a boost converter when the input voltage is lower than the output voltage. In normal mode, no mode of operation is available in which all four switches are permanently switching. Controlling the switches in this way allows the converter to maintain high efficiency at the most important point of operation; when the input voltage is close to the output voltage. The RMS current through the switches and the inductor is

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kept at a minimum to minimize switching and conduction losses. For the remaining two switches, one is kept permanently on and the other is kept permanently off which causes no switching losses.

In normal mode, the converter operates in full continuous mode at a fixed switching frequency of 2 MHz (typical) for the entire load-current range, even with no load at the output. No pulse-skipping should occur for supply voltages from 2 V to 27 V.

8.4.2.2 Low-Power Mode

When the buck-boost converter is in low-power mode, the output voltage is monitored with a comparator with its threshold at the regulation target voltage. When the buck-boost regulator goes to low-power mode, the converter temporary stops operating and the output voltage drops. The slope of the output voltage depends on the load and output capacitance. As the output voltage decreases to less than the regulation target voltage, the device ramps up the output voltage again by giving one or several pulses until the output voltage exceeds the regulation target voltage. In low-power mode, the buck-boost operates in 4-switch mode, which allows regulation at the target output voltage regardless of whether the input voltage is greater than or less than the target output voltage value.

After the device enters low-power mode, the internal oscillator is turned off. As a result of the oscillator being turned off, all signal deglitching functions are disabled while the device is in low-power mode. These functions include the V_{IN} and VREG OV and UV signal deglitch functions, and the IGN input signal deglitch function.

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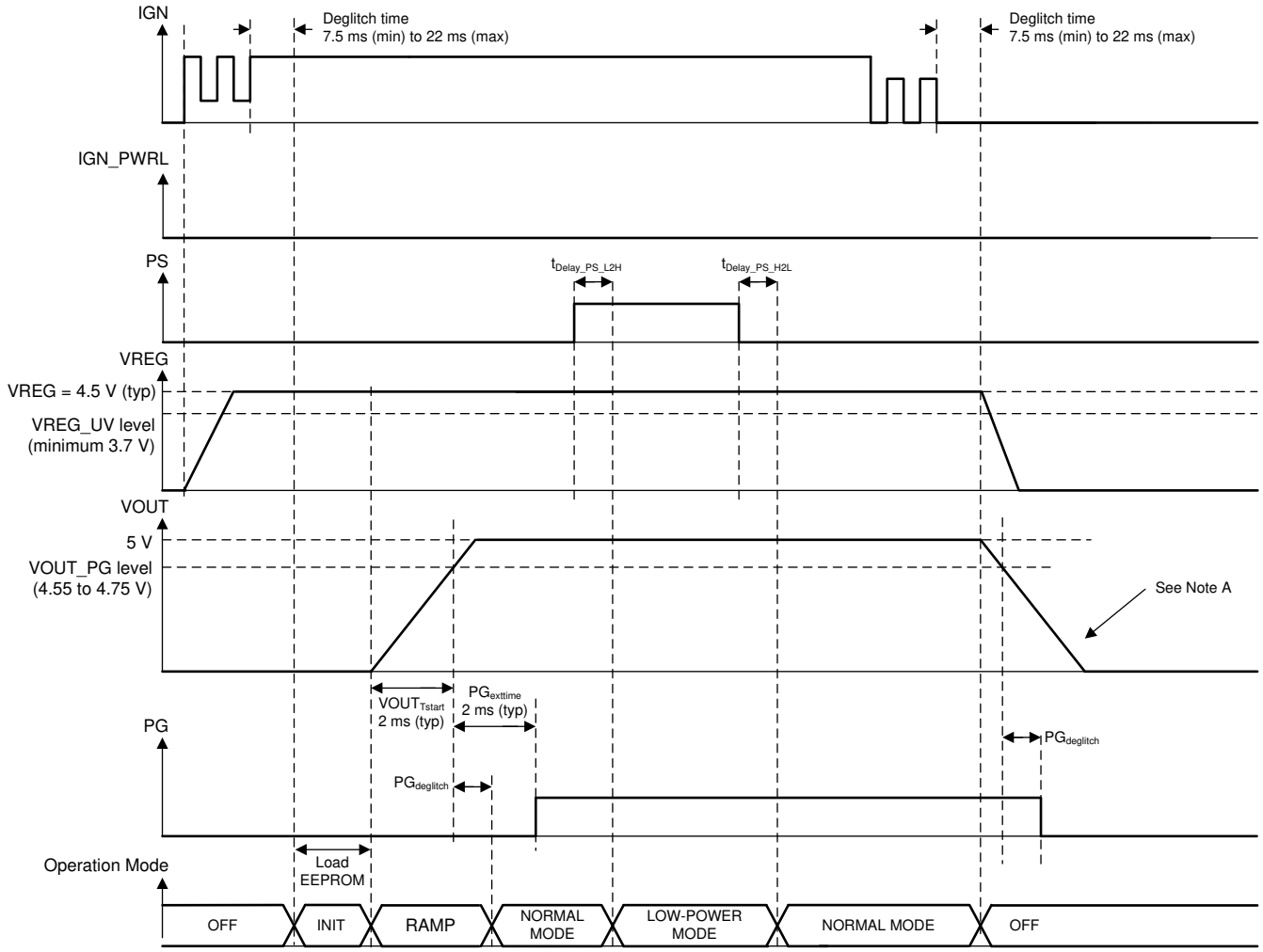
8.4.3 Power-Up and Power-Down Sequences

図 8-2 shows the power-up and power-down sequence without the usage of the IGN_PWRL pin.



A. The actual ramp-down time of the output voltage depends on external load conditions.

図 8-2. Power-Up and Power-Down Sequence With Normal Mode and Low-Power Mode, Without Usage of IGN_PWRL

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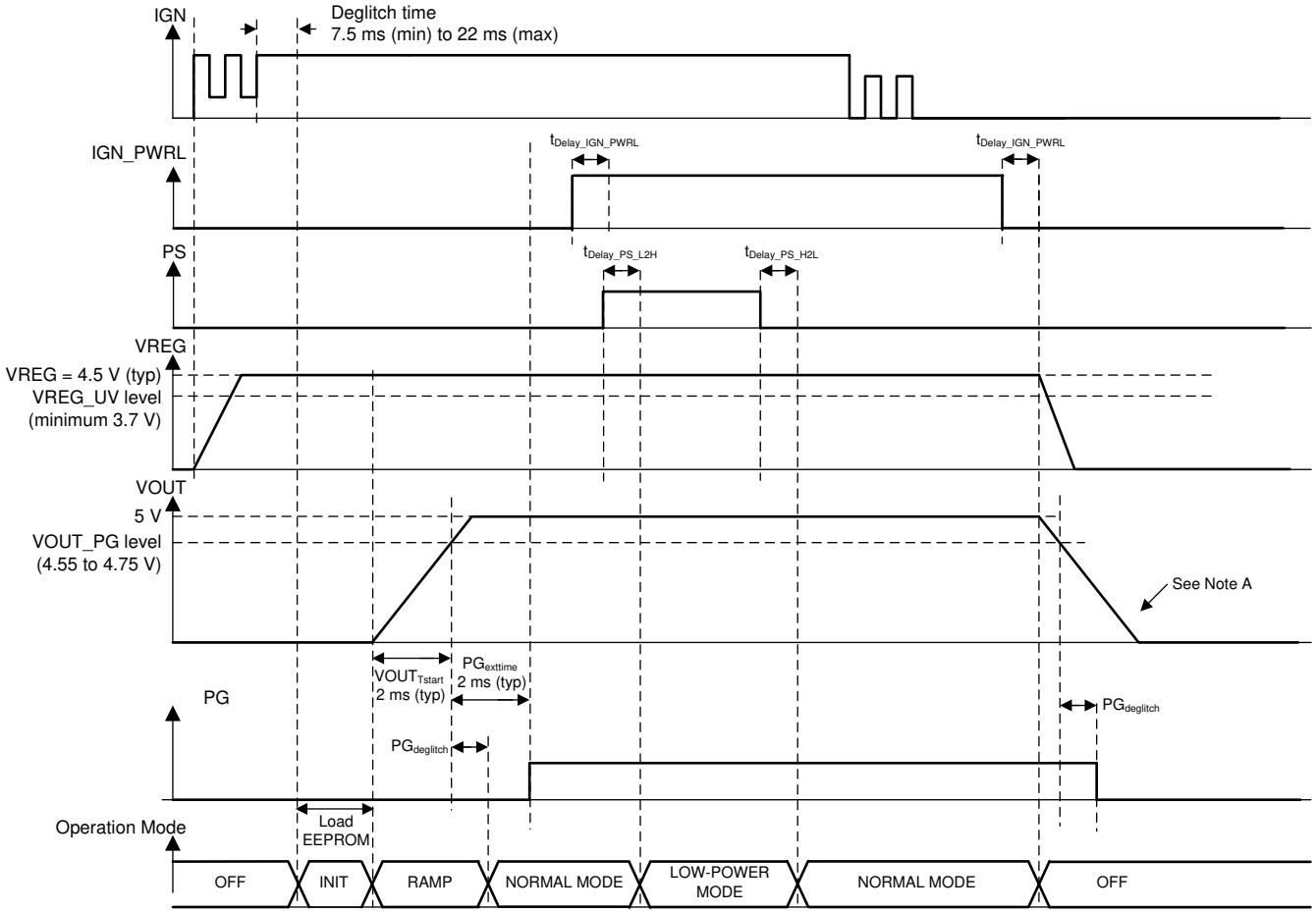
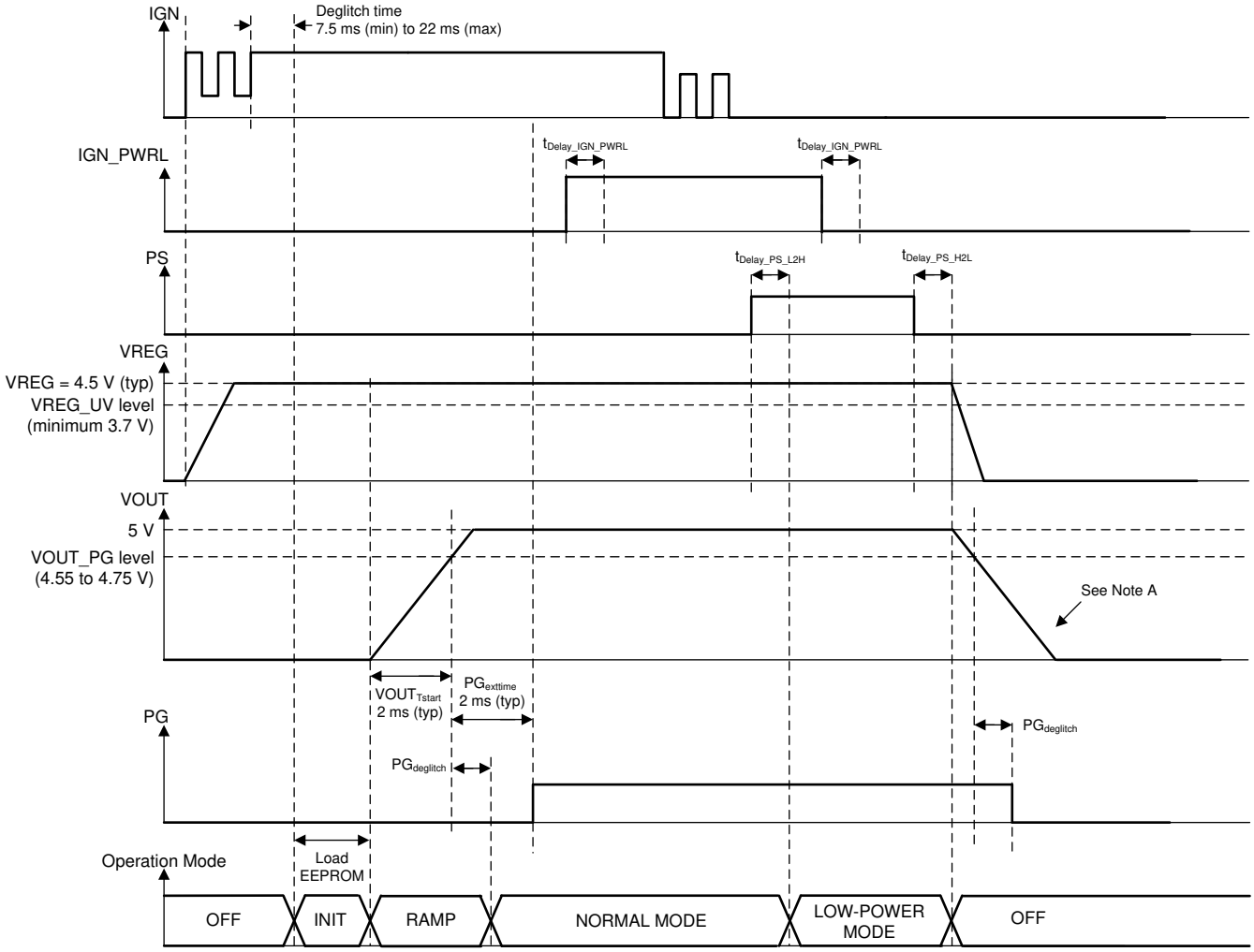
図 8-3 shows the power-up and power-down sequence with usage of the IGN_PWRL pin.



A. The actual ramp-down time of the output voltage depends on external load conditions.

図 8-3. Power-Up and Power-Down Sequence With Normal Mode and Low-Power Mode, With Usage of IGN_PWRL

図 8-4 shows a power-up and power-down sequence in low-Power mode with the IGN pin low. 図 8-4 shows that after the device is powered on in the OFF state, the device is in low-power mode when the PS pin is high regardless of what was applied on the IGN and IGN_PWRL input pins.



A. The actual ramp-down time of the output voltage depends on external load conditions.

図 8-4. Power-Up and Power-Down Sequence With Low-Power Mode When IGN and IGN_PWRL are Low (Essentially When the ECU is in Sleep or Standby Mode)

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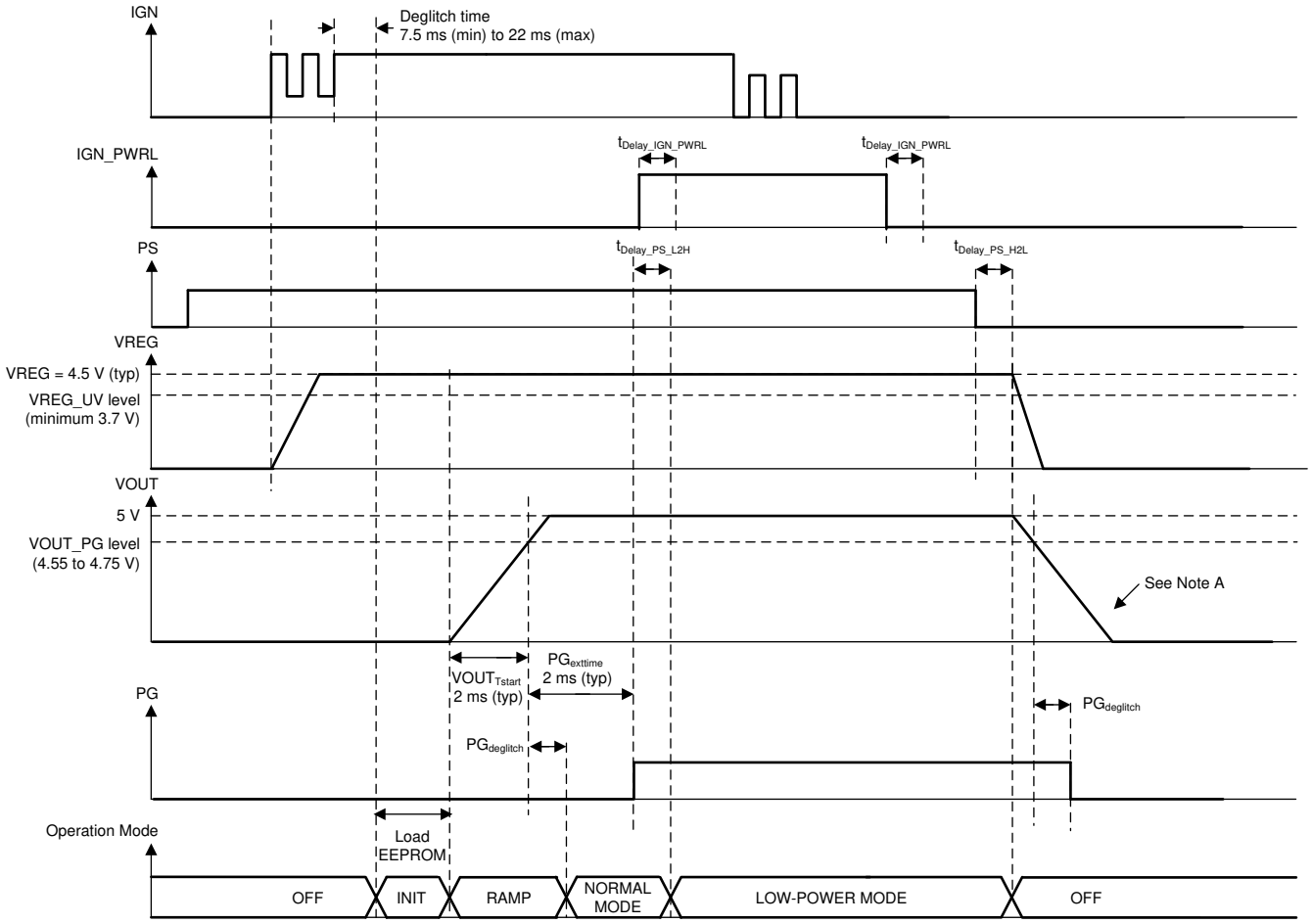
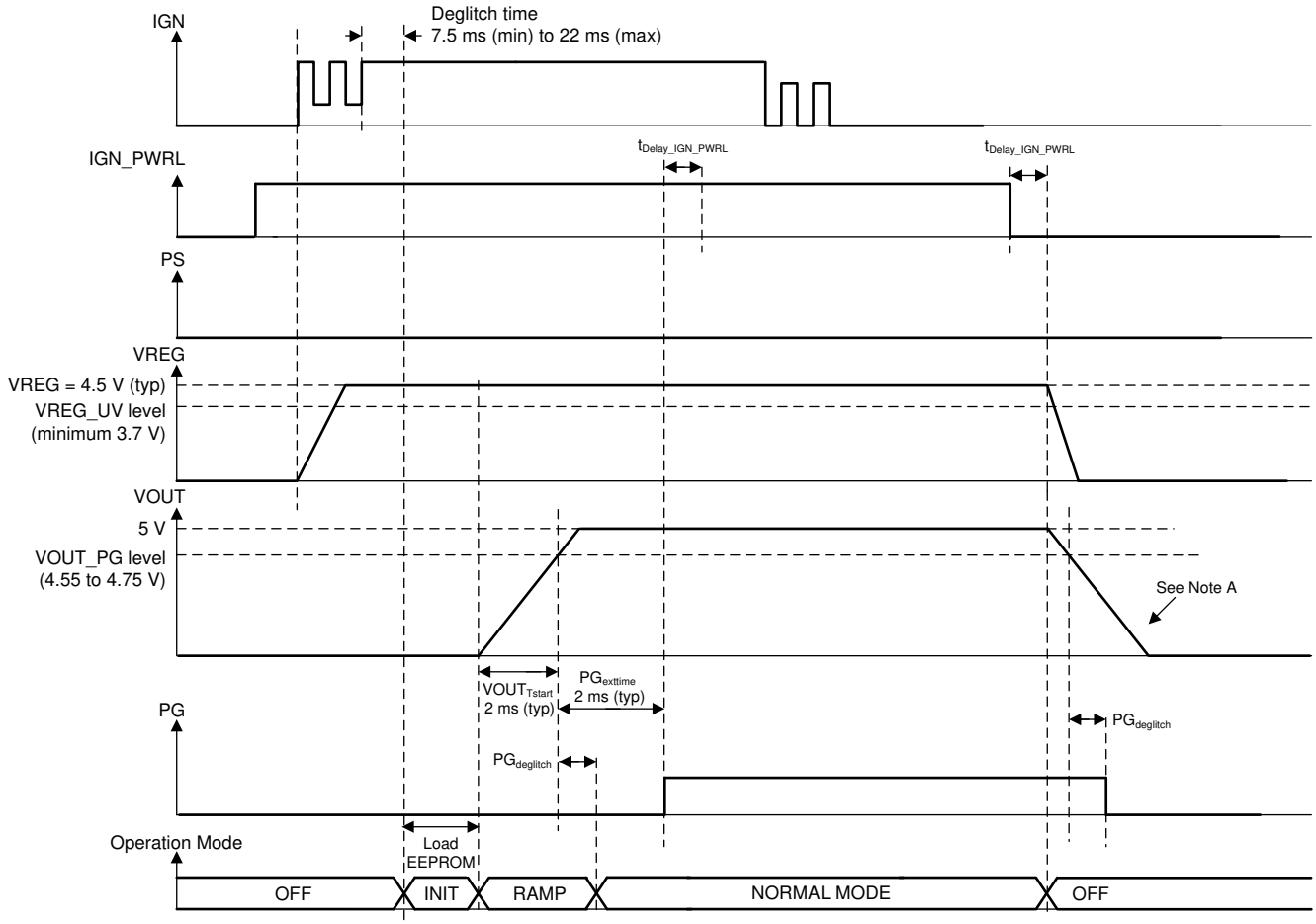
図 8-5 shows that when the device starts in the OFF state, the buck-boost converter always enters normal mode first, even when the PS pin was previously set high. The device can only enter low-power mode when the PG output pin is set high. 図 8-5 also shows that the device does not start-up as long as the IGN pin is low.



A. The actual ramp-down time of the output voltage depends on external load conditions.
The buck-boost converter always enters normal mode first after ramp up before it can enter low-power mode.

図 8-5. Power-Up Behavior With PS Pin Previously Set High

図 8-6 shows that the device only can start-up in the OFF state when the IGN pin is high. Setting the IGN_PWRL pin before the IGN pin is high does not start-up the device. 図 8-6 also shows that the IGN_PWRL signal is only valid after the PG pin is high and the $PG_{Deglitch}$ time has elapsed.



A. The actual ramp-down time of the output voltage depends on external load conditions.
The device does not start-up until the IGN pin is high. The IGN power-latch is only be set after the PG pin is high.

図 8-6. Power-Up Behavior With IGN_PWRL Set High Prior to High IGN

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8.4.4 Soft-Start Feature

On power up, the device has a soft-start feature which ramps the output of the regulator at a steady slew rate. The soft-start ramp time is 0.5 ms by default. When the device pulls the PG pin low because of a V_{OUT} undervoltage condition while the device is in normal mode, the device stays in normal mode and tries to get to the VOUT level again without soft-start slew-ramp control.

8.4.5 Pulldown Resistor on VOUT

When the buck-boost regulator is disabled (in the OFF state, INIT state, and PRE_RAMP state), an internal active pulldown circuit (specified as Rpd_{VOUT} in *セクション 7.7*) pulls down the VOUT pin.

8.4.6 Output Voltage Selection

The configuration of the output voltage is selectable through the VOS_FB pin.

The fixed output voltage of the TPS55165-Q1 device is 5 V when the VOS_FB pin is connected to ground and is 12 V when the VOS_FB pin is connected to the VREG pin. For the TPS55165-Q1 device in the 5-V configuration (VOS_FB pin connected to ground), the UVLO threshold is set to less than 2 V. When the TPS55165-Q1 device is in the 12-V configuration (VOS_FB pin connected to the VREG pin), the UVLO threshold is set to less than 3.6 V. For the TPS55162-Q1 device, the UVLO threshold is also set to less than 3.6 V.

For the adjustable output voltage of the TPS55160-Q1 and TPS55162-Q1 devices, connect the VOS_FB pin to the external feedback network. The total resistance of this external feedback network must be less than 1 MΩ (essentially, this value must be similar to or less than the implemented total resistance of the implemented internal feedback network for the 12 V setting).

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9 Application and Implementation

Note

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9.1 Application Information

The TPS5516x-Q1 family of devices is a high-voltage synchronous buck-boost DC-DC converter with all four power MOSFETs integrated. Each device in the device family can produce a well-regulated output voltage from a widely-varying input voltage source such as an automotive car battery. If the input voltage is higher than the output voltage, the TPS5516x-Q1 device operates in step-down mode. If the input voltage is lower than the output, the device operates in step-up mode. If the input voltage is equal or close to the output voltage, the device operates between the step-down and step-up mode. The buck-boost overlap control ensures automatic and smooth transition between step-down and step-up (this is okay. Step-up and step-down modes were mentioned in the first page of the spec) modes with optimal efficiency. The output voltage of the TPS55165-Q1 device can be set to a fixed level of 5 V or 12 V. The output voltage of the TPS55160-Q1 and TPS55162-Q1 devices is programmable from 5.7 V to 9 V.

9.1.1 Application Circuits for Output Voltage Configurations

図 9-1 and 図 9-2 show the application diagrams for the adjustable output configuration.

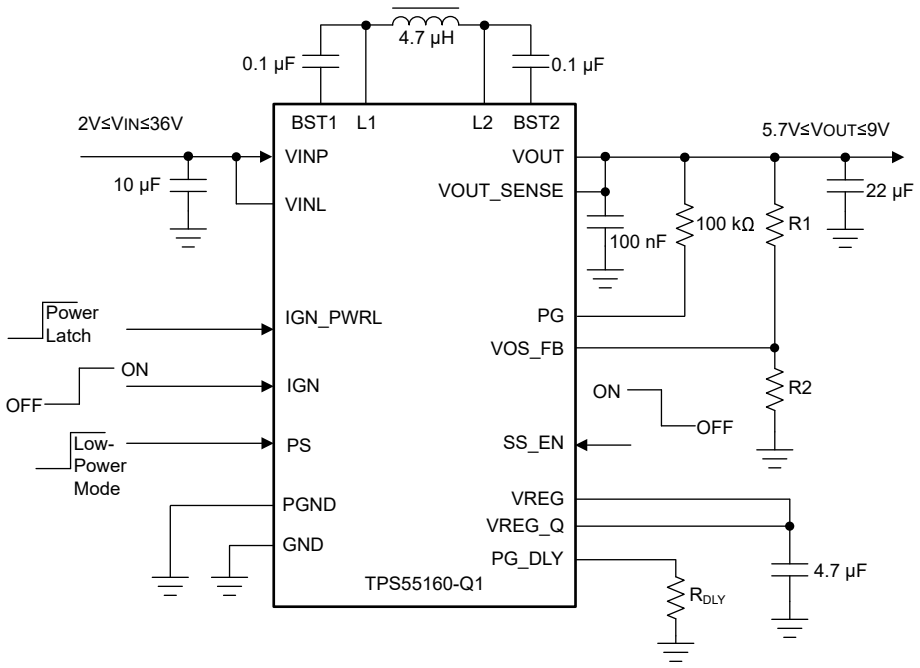

図 9-1. TPS55160-Q1 Application Diagram for Adjustable Output Voltage

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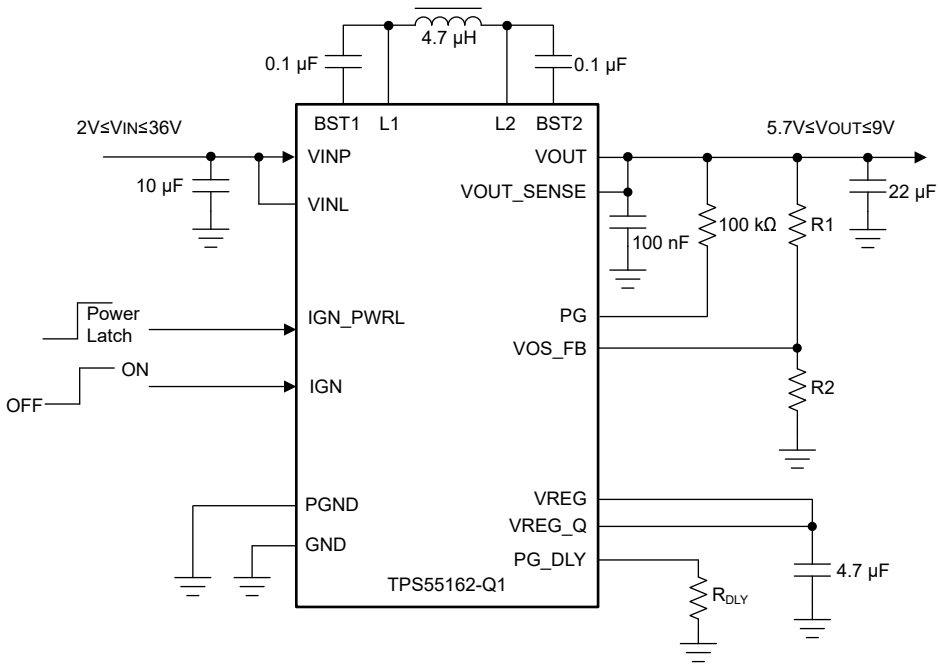

図 9-2. TPS55162-Q1 Application Diagram for Adjustable Output Voltage

Use 式 1 to calculate the output voltage.

$$V_{OUT} = \frac{R1 + R2}{R2} \times V_{FB} \quad (1)$$

where

- V_{FB} is 0.8 V (see セクション 7.7).

図 9-3 shows the TPS55165-Q1 device in the 5-V configuration.

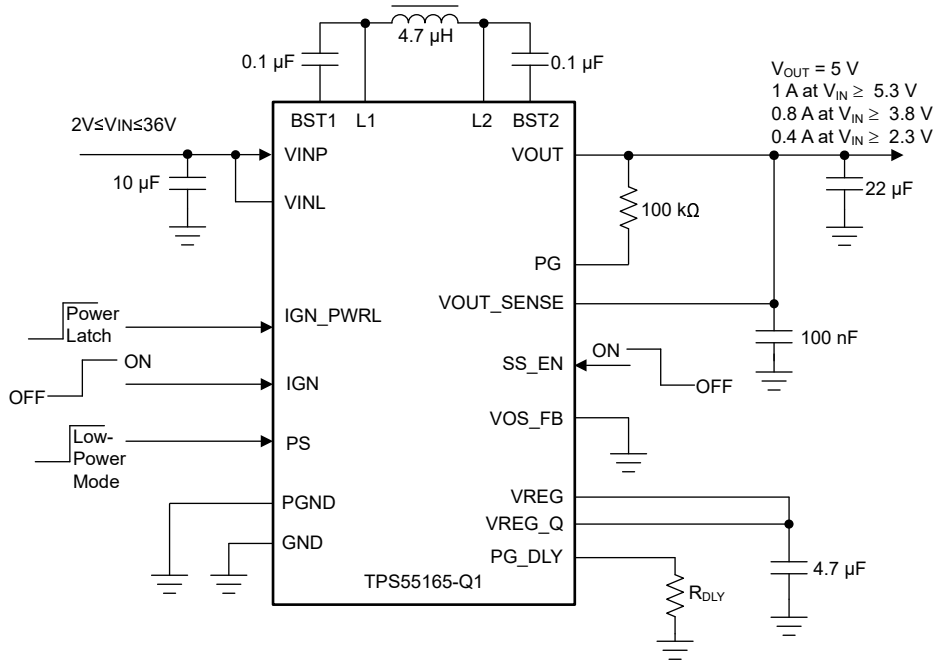

図 9-3. TPS55165-Q1 Application Diagram for 5-V Voltage

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図 9-4 shows the TPS55165-Q1 device in the 12-V configuration.

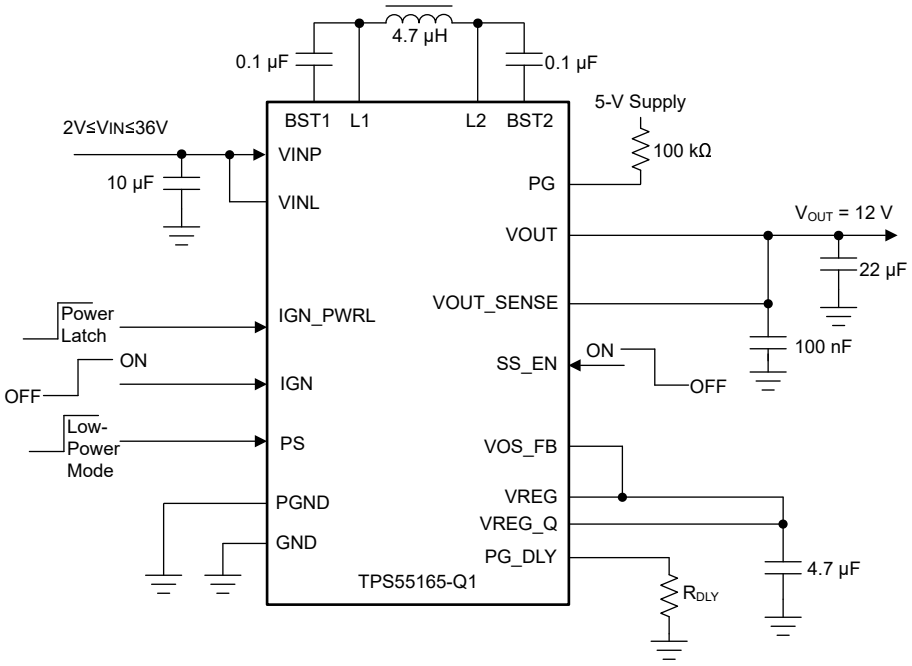

図 9-4. TPS55165-Q1 Application Diagram for 12-V Voltage

CAUTION

For TPS55165-Q1 in 12-V configuration (VOS_FB is shorted to VREG), the PG pin must be tied to an external 5-V supply through a pullup resistor. Tying the PG pin to a supply greater than 5.5 V could damage the device in the unlikely event of a shortage between the PG pin and the adjacent VOS_FB pin, which is tied to the VREG pin in the 12-V output configuration. The absolute-maximum voltage rating of the VREG pin is 5.5 V.

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9.2 Typical Application

The TPS5516x-Q1 family of devices requires a minimum number of external components to implement a buck-boost converter. 図 9-5 shows the typical schematic for the TPS55165-Q1 device in the 5-V configuration.

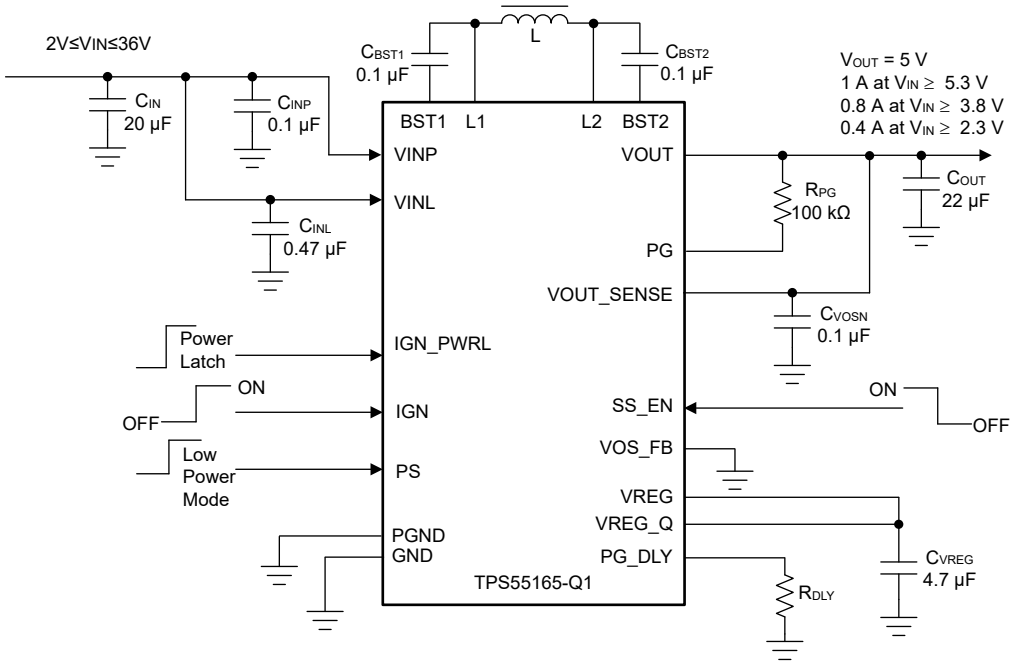

図 9-5. TPS55165-Q1 Buck-Boost Converter for Fixed 5-V Output

9.2.1 Design Requirements

表 9-1 lists the design requirements for 図 9-5.

表 9-1. Design Requirements

PARAMETER		VALUE
V_{IN_MIN}	The least input voltage after start-up. The I_{OUT_MAX} load current deratings listed in this table apply for V_{IN} < 5.3 V.	2 V
$V_{IN\_startup}$	The minimum input voltage required for start-up	> 5.3 V
V_{IN_MAX}	The greatest input voltage after start-up	36 V
V_{OUT}	The output voltage	5 V
I_{OUT_MAX}	The maximum output current at V_{IN} ≥ 5.3 V	1 A
	The maximum output current at 3.8 V ≤ V_{IN} < 5.3 V	0.8 A
	The maximum output current at 2.3 V ≤ V_{IN} < 3.8 V	0.4 A

9.2.2 Detailed Design Procedure

9.2.2.1 Power-Circuit Selections: C_{IN}, L, C_{OUT}

The TPS5516x-Q1 family of devices integrates not only the power switches but also the loop compensation network as well as many other control circuits which reduces the number of required external components. For the internal loop compensation to be effective, the selection of the external power circuits (power inductor and capacitor) must be confined. TI strongly recommends users selecting the component values as follows: 3.3-µH to 6.2-µH power inductor, 18-µF to 47-µF output capacitor, and 8.2-µF or greater input capacitor. Because the TPS5516x-Q1 device switches at about 2 MHz, a shielded inductor and X5R-type or X7R-type ceramic capacitors should be used for the power circuit.

Considering the component tolerance, the following power component values were selected for this design example:

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- C_{IN} = 20 µF
- C_{OUT} = 22 µF
- L = 4.7 µH

For the input capacitor (C_{IN}), the voltage rating should be greater than the maximum input voltage (V_{IN_MAX}). Therefore, two, 10-µF X7R capacitors rated for 50 V were selected for this design example. Adding a small, high-frequency decoupling ceramic capacitor (C_{VINP} with a value of 100 nF typical) in parallel with the input capacitor is recommended to better filter out the switching noises at the VINP pin. Adding another decoupling ceramic capacitor (C_{VINL} with a value of 470 nF typical) is also recommended for the VINL pin.

The output capacitor (C_{OUT}), receives a voltage of 5 V. Considering some voltage-rating margin, two 10-µF X7R capacitors rater for 10 V or greater and one, 2.2-µF X7R-type capacitor rated for 10 V or greater in parallel were selected for the output capacitor. Adding a small, high-frequency decoupling ceramic capacitor (C_{VOSN} with a value of 100 nF typical) in parallel with the output capacitor is recommended to better filter out the switching noises at the VOUT_SENSE pin.

The power inductor (L) should be a shielded type, and it should not saturate during operation. The inductor should also be able to support the power dissipation under the maximum load. Use the calculations in the following sections to find the required current capabilities for the inductor.

9.2.2.1.1 Inductor Current in Step-Down Mode

Use 式 2 to calculate inductor peak-ripple current in the step-down, or buck, mode (I_{pk_buck}).

$$I_{pk\_buck} = \frac{1}{2} \times \frac{V_{OUT}}{L} \times \frac{1 - D_{buck}}{f_S} \tag{2}$$

where

- V_{OUT} is the output voltage.
- L is the value of the inductor.
- D_{buck} is the duty cycle (refer to 式 3).
- f_S is the switching frequency.

$$D_{buck} = \frac{V_{OUT}}{V_{IN}} \tag{3}$$

The maximum peak-ripple current of the inductor (I_{pk}) occurs when the duty cycle is at the minimum value, specifically when the input voltage (V_{IN}) is at the maximum value which yields the value shown in 式 4.

$$D_{buck} = \frac{5\ V}{36\ V} = 0.139 \tag{4}$$

Substitute the values for f_S, L, and D_{buck}, in 式 2 to find the peak-ripple current as shown in 式 5.

$$I_{pk\_buck} = \frac{1}{2} \times \frac{5\ V}{4.7\ \mu H} \times \frac{1 - 0.139}{2\ MHz} = 0.229\ A \tag{5}$$

The power dissipations can be determined by the RMS current of the inductor. Use 式 6 to calculate the RMS current of the inductor in buck mode (I_{rms_buck}).

$$I_{rms\_buck} = \sqrt{I_{OUT}^2 + \frac{1}{3} \times I_{pk\_buck}^2} = \sqrt{1\ A^2 + \frac{1}{3} \times 0.458\ A^2} = 1.1\ A \tag{6}$$

Use 式 7 to calculate the approximate power dissipation of the inductor in buck-mode ($P_{loss\_L\_buck}$).

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$$P_{loss\_L\_buck} = I^2_{rms\_buck} \times R_{dc} \quad (7)$$

9.2.2.1.2 Inductor Current in Step-Up Mode

Use 式 8 to calculate the inductor peak-ripple current in the step-up, or boost, mode (I_{pk_boost}).

$$I_{pk\_boost} = \frac{1}{2} \times \frac{V_{IN}}{L} \times \frac{D_{boost}}{fsw} \quad (8)$$

where

- D_{boost} is the duty cycle in boost mode (refer to 式 9).

$$D_{boost} = \frac{V_{OUT} - V_{IN}}{V_{VOUT}} \quad (9)$$

In general, the maximum peak-ripple current occurs at 50% duty cycle. In this example, because of the power derating versus the input voltage, a few calculations can find that the maximum RMS current occurs when the input voltage is approximately 3.8 V, of which the load current is 0.8 A, according to 表 9-1. 式 10 and 式 11 show the peak-ripple current under this condition.

$$D_{boost} = \frac{5\ V - 3.8\ V}{5\ V} = 0.240 \quad (10)$$

$$I_{pk\_boost} = \frac{1}{2} \times \frac{3.8\ V}{4.7\ \mu H} \times \frac{0.240}{2\ MHz} = 0.049\ A \quad (11)$$

The power dissipations can be determined by the RMS current of the inductor. Use 式 12 to calculate the RMS current of the inductor in buck mode (I_{rms_boost}).

$$I_{rms\_boost} = \sqrt{\left(\frac{I_{OUT}}{1 - D_{boost}}\right)^2 + \frac{1}{3} \times I_{pk\_boost}^2} = \sqrt{\left(\frac{0.8\ A}{1 - 0.24}\right)^2 + \frac{1}{3} \times 0.049\ A^2} = 1.053\ A \quad (12)$$

Use 式 13 to calculate the approximate power dissipation of the inductor in boost-mode ($P_{loss\_L\_boost}$).

$$P_{loss\_L\_boost} = I^2_{rms\_boost} \times R_{dc} \quad (13)$$

9.2.2.1.3 Inductor Current in Buck-Boost Overlap Mode

When input voltage is very close to the output voltage, the device operates in buck-boost overlap mode, and the L1 and L2 pins are switched alternatively in consecutive cycles. The small voltage difference between the input and output voltage leads to a small amount of ripple current through the inductor. Therefore, the total inductor current is essentially the load current with small ripples superimposed onto it, and the RMS current is approximately the same as the load current, which is 1 A.

$$P_{loss\_L\_buckboost} = I^2_o \times R_{dc} \quad (14)$$

9.2.2.1.4 Inductor Peak Current

Because the TPS5516x-Q1 device has internal peak current limit (I_{SW_limit}) of 4.5 A (maximum), this current should be considered when selecting the power inductor. Select the inductor of the saturation current (I_{SAT}) with a minimum value of 4.5 A so that the inductor never gets saturated. TI recommends using a shielded inductor.

For this design example, select an AEC-Q200 Grade 0, shielded inductor with the following characteristics:

- Is a surface-mount device (SMD)

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- Has an inductance of 4.7 µH
- Supports a saturation current (I_{SAT}) of 4.8 A
- Is rated for an RMS current (I_{rms}) of 1.5 A or larger
- Is rated for a DC load (R_{dc}) of 0.04 Ω or smaller

9.2.2.2 Control-Circuit Selections

9.2.2.2.1 Bootstrap Capacitors

The bootstrap capacitors (C_{BST1} and C_{BST2}) supply the internal high-side MOSFET driver. TI recommends using a 0.1-µF, X7R-type ceramic capacitor rated for 15 V or larger for the bootstrap capacitors.

9.2.2.2.2 VOUT-Sense Bypass Capacitor

To improve noise immunity, connect a 0.1-µF, X7R-type ceramic capacitor rated for 25 V or greater to the VOUT pin.

9.2.2.2.3 VREG Bypass Capacitor

The VREG supplies the internal control circuit as well as the drivers for the integrated low-side driver. To improve noise immunity and stabilize the internal VREG regulator, TI recommends connecting a 4.7-µF, X7R-type ceramic capacitor rated for 25 V or greater between the VREG and GND pins.

9.2.2.2.4 PG Pullup Resistor and Delay Time

The power-good indicator pin (PG) is an open-drain output pin. The PG pin requires an external pullup resistor to flag the power-good status. For this design example, select a 100-kΩ resistor to pull up the PG pin from the output rail.

The PG_DLY pin sets the delay time for the PG status to flip. Follow the instructions listed in the *セクション 8.3.7* to program the delay.

9.2.3 Application Curves

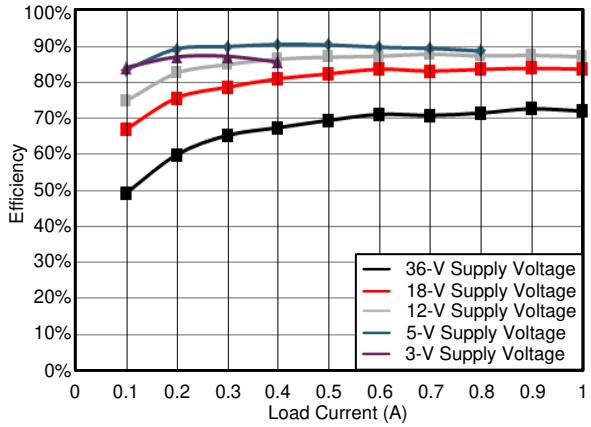
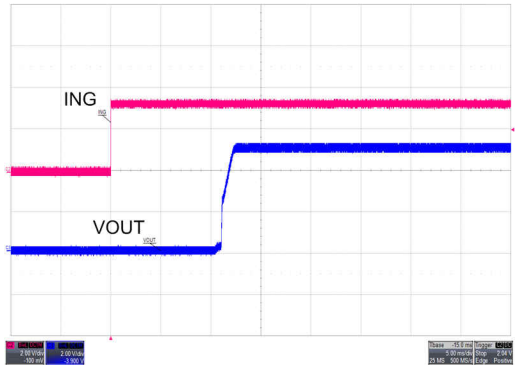
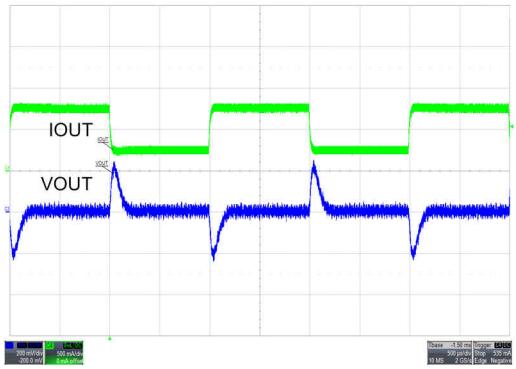


図 9-6. Efficiency vs Load



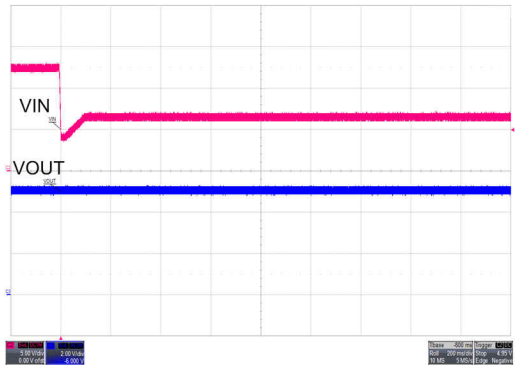
V_{IN} = 12 V I_{OUT} = 1 A

図 9-7. Start-Up Procedure



V_{IN} = 12 V I_{OUT} step change from 0.25 A to 0.75 A

図 9-8. Step Load Response



I_{OUT} = 0.5 A V_{IN} transient rom 12 V to 4 V

図 9-9. Battery-Voltage Cranking Response

10 Power Supply Recommendations

The TPS5516x-Q1 family of devices is a power-management device. The power supply for the device is any DC-voltage source within the specified input range. The supply should also be capable of supplying sufficient current based on the maximum inductor current in boost-mode operation. When connecting to the power supply and load, try to use short and solid wires. Twisting the pair of wires for the input and output helps minimize the line impedance and avoid adversary interference with the circuit operation.

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11 Layout

11.1 Layout Guidelines

The layout of the printed-circuit board (PCB) is critical to achieve low EMI and stable power-supply operation as well as optimal efficiency. Make the high frequency current loops as small as possible, and follow these guidelines of good layout practices;

- The TPS5516x-Q1 family of devices is a high-frequency switching converter. Because the four switch MOSFETs are integrated, the device should be located at the center of the DC-DC power stage. Separate the power ground and analog ground such that the control circuit can be connected to the relatively quieter analog ground without being contaminated by the noisy power ground. Use the PGND pin, GND pin, and the device PowerPAD as the single-point connection between the analog and power grounds.
- Identify the high-frequency switched AC-current loops. In step-down mode, the AC current loop is along the path of the input capacitor (C_{IN}), L1 pin, internal buck-switch leg, and PGND pin, and closes at the input capacitor. In step-up mode, the AC current loop is along the path of the output capacitor (C_{OUT}), L2 pin, internal boost-switch leg, and PGND pin, and closes at the output capacitor. These two AC-current loops are both involved in buck-boost overlap mode.
- Optimize component placement and orientation before routing any traces. Place the input and output filter capacitors, the device, and the power inductor close together such that the AC-current loops are short, direct, and the spatial areas enclosed by the loops are minimized. Make the power flow in a straight path rather than a zigzag path on the board.
- Place the high frequency decoupling ceramic capacitors for the input and output as close as possible to the device with the main input and output ceramic capacitors placed next to the high-frequency capacitors. This placement helps confine the high switching noises within a very small area around the device.
- Place the VREG decoupling capacitor close to the VREG pin because it serves as the supply to the internal low-side MOSFETs drivers. Because the VREG pin receives power from the output rail, the ground lead of the VREG decoupling capacitor should connect directly to the C_{OUT} ground to improve device noise immunity.

Note

The VREG_Q pin must always connect to the VREG pin. Both pins should have a Kelvin connection to the decoupling capacitor.

- Place the bootstrap capacitors (C_{BST1} and C_{BST2}) close to the device with short and direct traces to connect to the corresponding device pins becuase these capacitors serve as the supplies to the internal high-side MOSFETs drivers
- Place the VOUT_SENSE decoupling capacitor (C_{VOSN}) close to the device. Give the placement of this capacitor priority over the main output capacitors.
- For TPS55160-Q1 or TPS55162-Q1, place the sense-resistor divider for the output voltage close to the device.
- Use eight to nine via holes with a 0.3 mm diameter in the device PowerPAD to help dissipate heat through the layers of the ground plane. Additional vias holes around the device PowerPAD can further enhance heat dissipation.
- Use at least ten via holes with a 0.3 mm diameter around the input and output capacitors that are connected to ground-plane layers to minimize the PCB impedance for power current flows.

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11.2 Layout Example

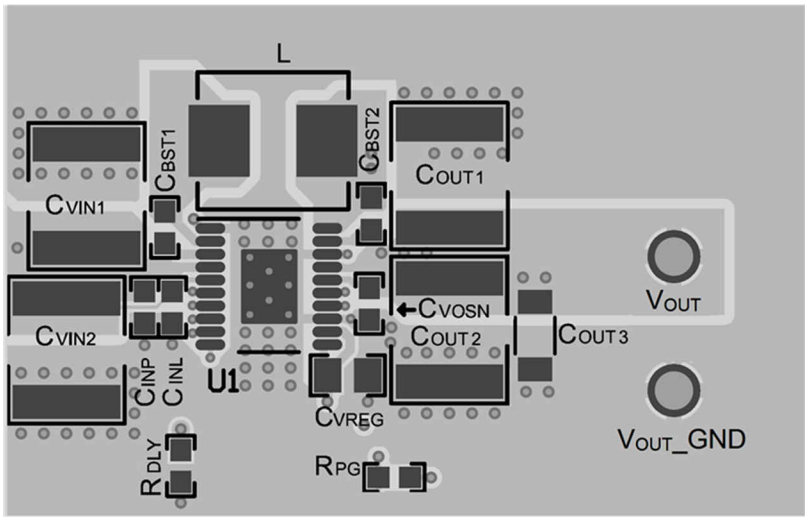

図 11-1. Example Circuit Layout

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

For development support, refer to:

TPS55160-Q1 PSpice Transient Model

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

Texas Instruments, *TPS5516xQ1-EVM Evaluation Module for 1-A Single- Inductor Buck-Boost-Converter* user's guide

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 サポート・リソース

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12.5 Trademarks

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TI E2E™ is a trademark of Texas Instruments.
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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS55160QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS55160	Samples
TPS55160QPWPTQ1	ACTIVE	HTSSOP	PWP	20	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS55160	Samples
TPS55162QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS55162	Samples
TPS55162QPWPTQ1	ACTIVE	HTSSOP	PWP	20	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS55162	Samples
TPS55165QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS55165	Samples
TPS55165QPWPTQ1	ACTIVE	HTSSOP	PWP	20	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS55165	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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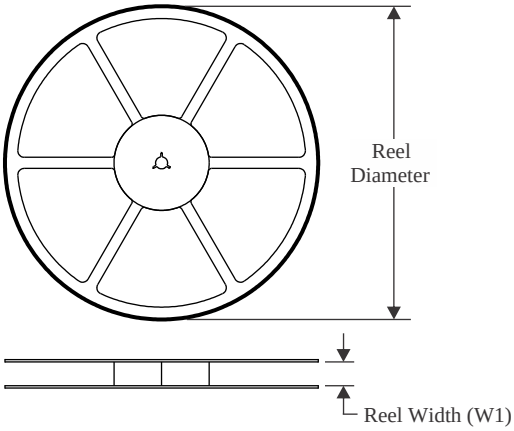
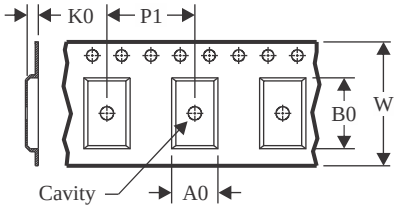
TAPE AND REEL INFORMATION

REEL DIMENSIONS

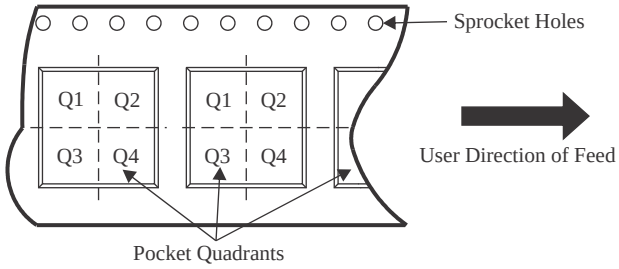


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

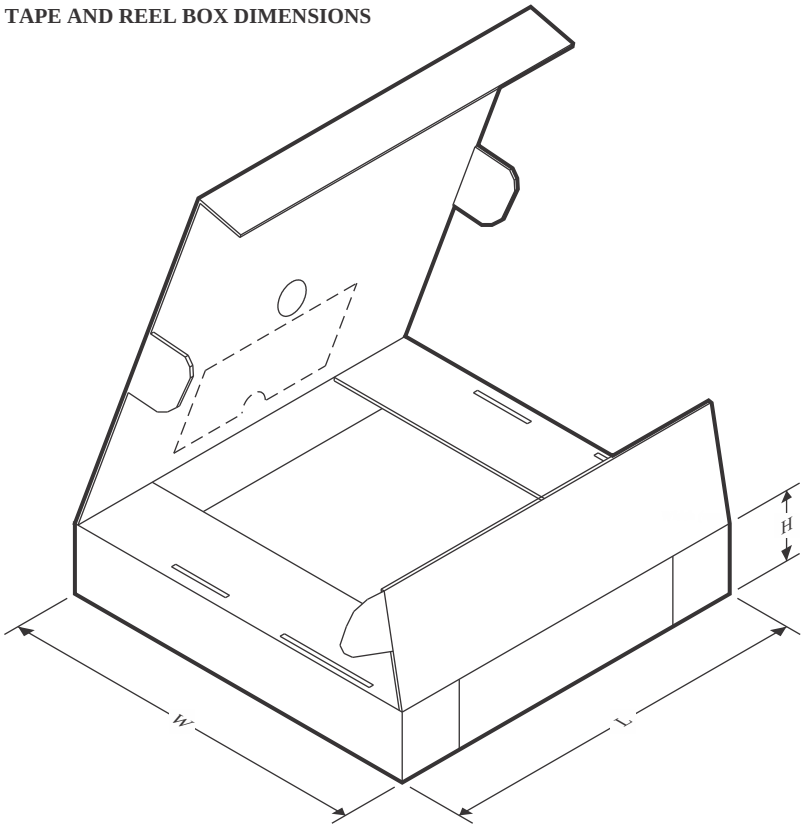
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS55160QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS55162QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS55165QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS55160QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS55162QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS55165QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

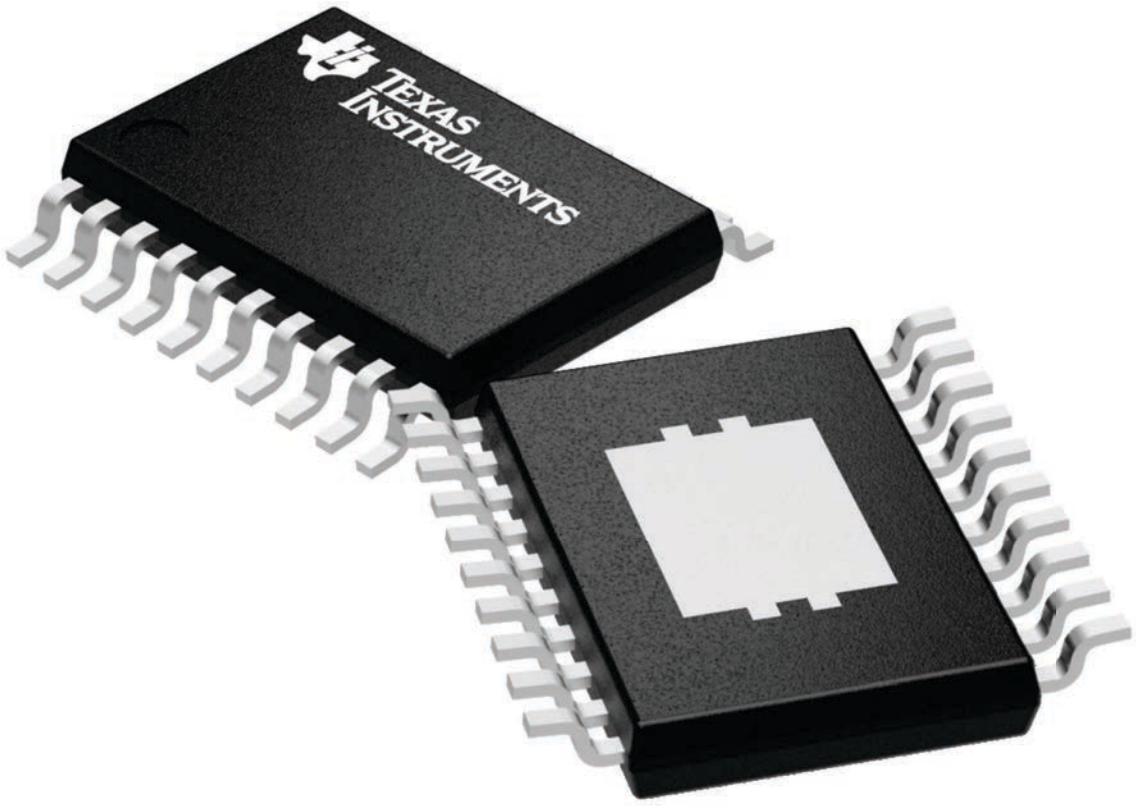
PWP 20

HTSSOP - 1.2 mm max height

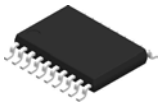
6.5 x 4.4, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224669/A

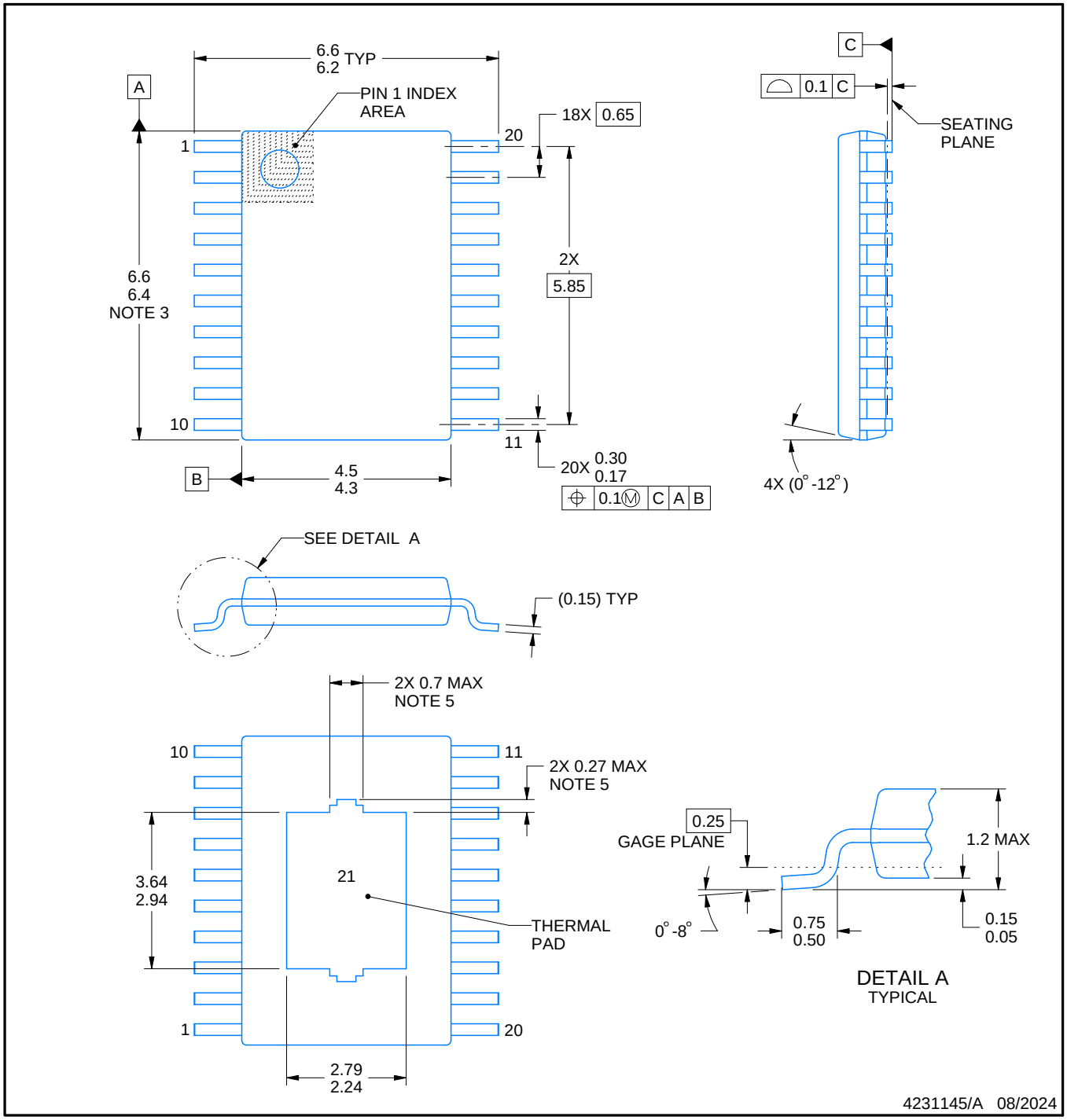


PACKAGE OUTLINE

PWP0020W

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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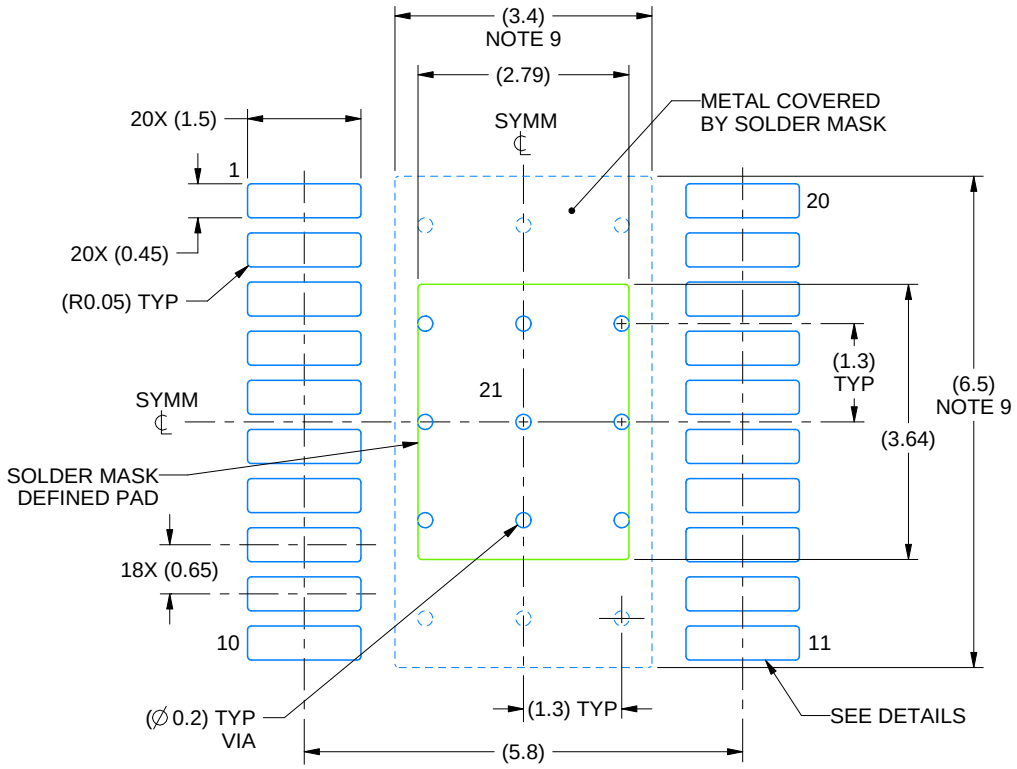
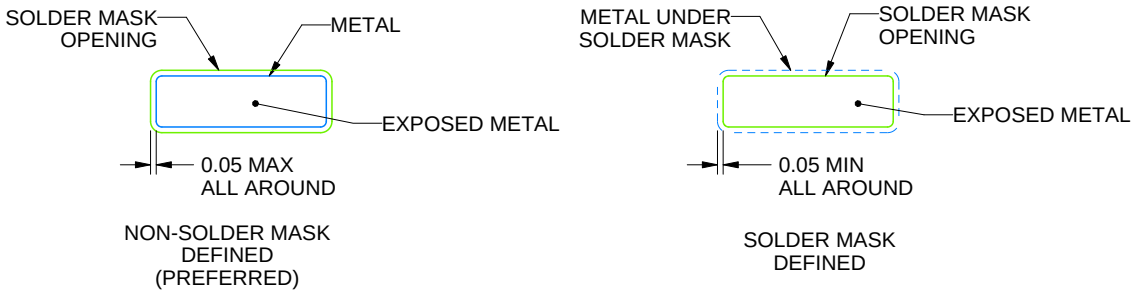
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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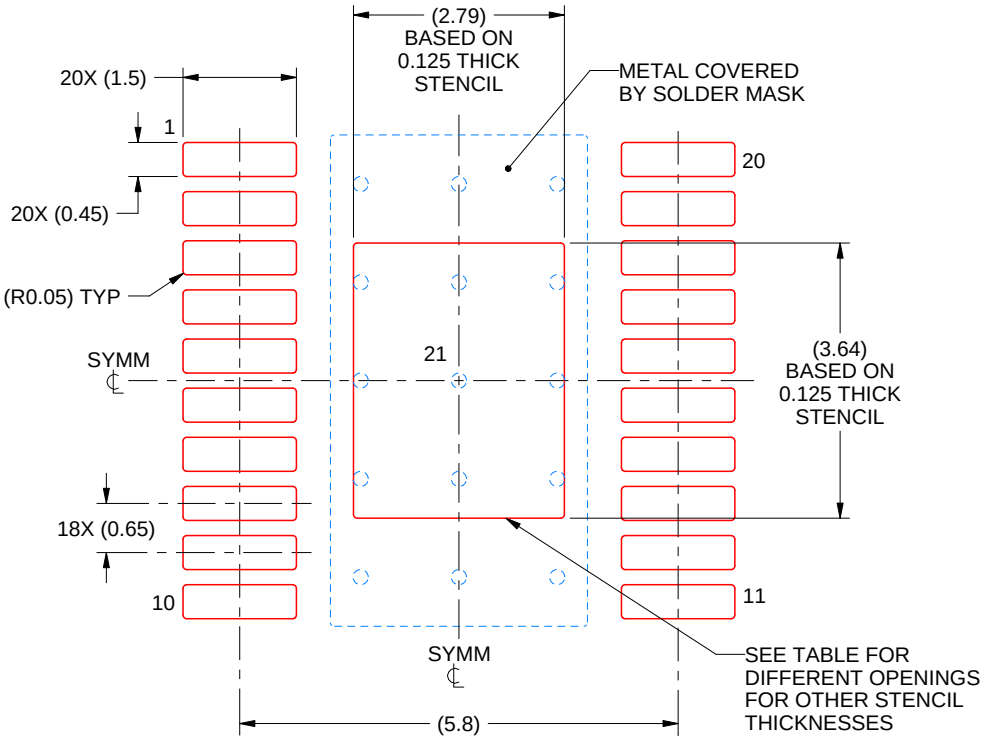
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.12 X 4.07
0.125	2.79 X 3.64 (SHOWN)
0.15	2.55 X 3.32
0.175	2.36 X 3.08

4231145/A 08/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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