TPS552882-Q1 36V、16A 昇降圧コンバータ

1 特長

- AEC-Q100 認定済み:
  - デバイス温度グレード 1:–40℃～+125℃の動作時周囲温度範囲
- 広い入出力電圧範囲
  - 広い入力電圧範囲:2.7V～36V
  - 広い出力電圧範囲:0.8V～22V
- 全負荷範囲にわたって高効率を実現
  - V_{IN} = 12V、V_{OUT} = 20V、I_{OUT} = 3A の条件下で 97% の効率
- 周波数干渉とクロストークを回避
  - (オプション) クロック同期
  - プログラム可能なスイッチング周波数:200kHz～2.2MHz
- EMI 低減
  - (オプション) プログラム可能な拡散スペクトラム
  - リードレス・パッケージ
- 豊富な保護機能
  - 出力過電圧保護
  - 出力を短絡から保護するためのヒカップ・モード
  - サーマル・シャットダウン保護機能
  - プログラム可能な平均インダクタ電流制限機能:最大 16A
- 小型ソリューション・サイズ
  - 最大 2.2MHz のスイッチング周波数
  - 4.0mm × 3.5mm HotRod™ QFN パッケージ (オプション:ウェッタブル・フランク)
- ケーブルの電圧ドループに対する可変出力電圧補償
- 軽負荷時のプログラム可能な PFM および FPWM モード
- センシング抵抗によるプログラム可能な出力電流制限
- ±1% の基準電圧精度
- 4ms の固定ソフトスタート時間
- WEBENCH® Power Designer により TPS552882-Q1 を使用するカスタム設計を作成

2 アプリケーション

- USB PD
- 車載用インフォテインメントおよびクラスタ
- 自動車用チャージャ

3 概要

TPS552882-Q1 は同期整流 4 スイッチ昇降圧コンバータであり、出力電圧を入力電圧と同じ値、より高い値、より低い値のいずれにも制御できます。TPS552882-Q1 は 2.7V～36V の広い入力電圧範囲で動作し 0.8V～22V の電圧を出力できるため、各種アプリケーションをサポートできます。

ソリューションのサイズと効率のバランスを確保するために、TPS552882-Q1 は昇圧レッグの 16A MOSFET を 2 個統合しています。TPS552882-Q1 は、1.2V の内部基準電圧で出力電圧を設定するために外付け抵抗分圧器を使用します。TPS552882-Q1 は 12V の入力電圧から 100W を供給できます。

TPS552882-Q1 は平均電流モード制御方式を採用しています。スイッチング周波数は、外付け抵抗で 200kHz～2.2MHz に設定することも、外部クロック信号に同期させることもできます。TPS552882-Q1 は、ピーク EMI を最小限に抑えるための拡散スペクトラム・オプション機能も備えています。

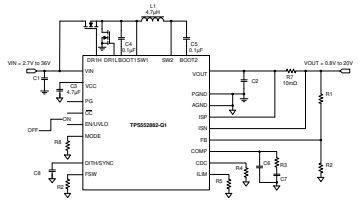
TPS552882-Q1 は出力過電圧保護、平均インダクタ電流制限、サイクルごとのピーク電流制限、出力短絡保護機能を備えています。また TPS552882-Q1 は、持続的な過負荷状態での出力電流制限およびヒカップ・モード保護オプション機能により、安全な動作を確保しています。

TPS552882-Q1 は、高いスイッチング周波数で動作できるため小型のインダクタとコンデンサが使えます。本デバイスは 4.0mm × 3.5mm の QFN パッケージで供給されます。

製品情報

部品番号	パッケージ(1)	本体サイズ
TPS552882-Q1	VQFN-HR	4.00mm × 3.50mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション回路

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4 Revision History

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5 Pin Configuration and Functions

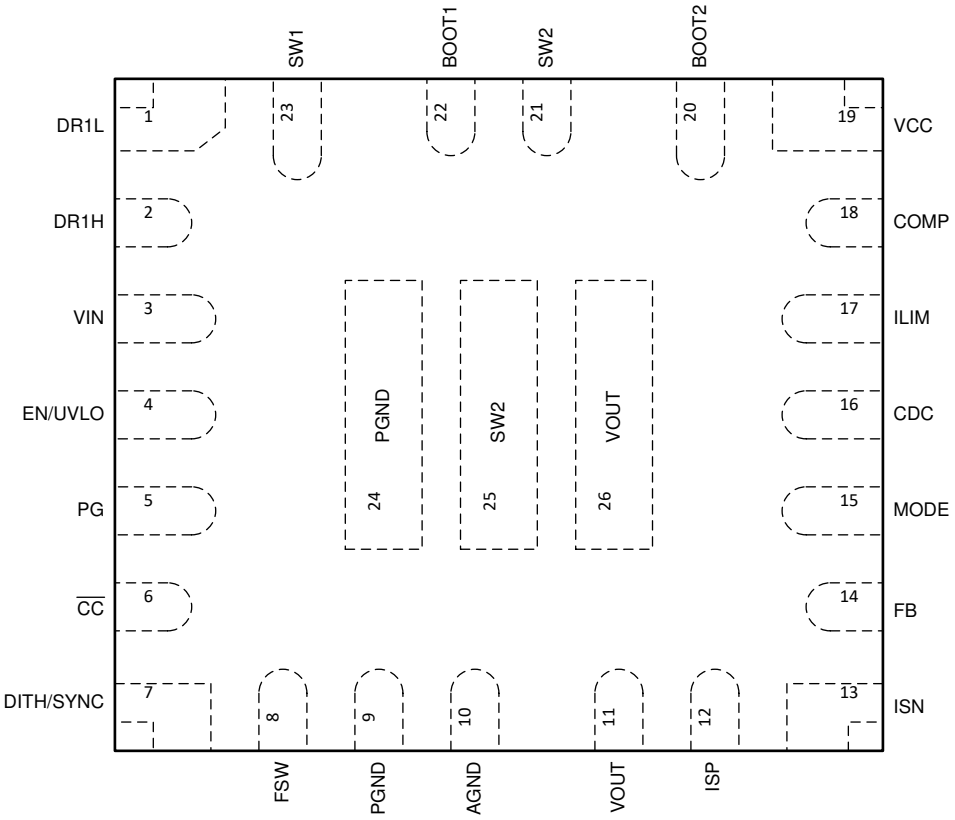


図 5-1. 26-pin VQFN-HR RPM Transparent (Top View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	DR1L	O	Gate driver output for low-side MOSFET in buck side
2	DR1H	O	Gate driver output for high-side MOSFET in buck side
3	VIN	PWR	Power supply to the IC from input voltage
4	EN/UVLO	I	Enable logic input and programmable input voltage undervoltage lockout (UVLO) input. Logic high level enables the device. Logic low level disables the device and turns it into shutdown mode. After the voltage at the EN/UVLO pin is above the logic high voltage of 1.15 V, this pin acts as programmable UVLO input with 1.23-V internal reference.
5	PG	O	Power good indication. When the output voltage is above 95% of the setting output voltage, this pin outputs high impedance. When the output voltage is below 90% of the setting output voltage, this pin outputs low level
6	$\overline{CC}$	O	Constant current output indication
7	DITH/SYNC	I	Dithering frequency setting and synchronous clock input. Use a capacitor between this pin and ground to set the dithering frequency. When this pin is short to ground or pulled above 1.2 V, there is no dithering function. An external clock can be applied at this pin to synchronize the switching frequency.
8	FSW	I	The switching frequency is programmed by a resistor between this pin and the AGND pin.
9, 24	PGND	PWR	Power ground of the IC. It is connected to the source of the low-side MOSFET.
10	AGND	PWR	Signal ground of the IC
11, 26	VOUT	PWR	Output of the buck-boost converter

表 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
12	ISP	I	Positive input of the current sense amplifier. An optional current sense resistor connected between the ISP pin and the ISN pin can limit the output current. If the sensed voltage reaches the current limit setting value in the register, a slow constant current control loop becomes active and starts to regulate the voltage between the ISP pin and the ISN pin. Connecting the ISP pin and the ISN pin together with the VOUT pin can disable the output current limit function.
13	ISN	I	Negative input of the current sense amplifier. An optional current sense resistor connected between the ISP pin and the ISN pin can limit the output current. If the sensed voltage reaches the current limit setting value in the register, a slow constant current control loop becomes active and starts to regulate the voltage between the ISP pin and the ISN pin. Connecting the ISP pin and the ISN pin together with the VOUT pin can disable the output current limit function.
14	FB	I	Connect to the center of a resistor divider to program the output voltage.
15	MODE	I	Setting the operation modes of the TPS55288x to select PFM mode or forced PWM mode in light load condition and to select the internal LDO or external 5 V for VCC by a resistor between this pin and AGND.
16	CDC	O	Voltage output proportional to the sensed voltage between the ISP pin and the ISN pin. Use a resistor between this pin and AGND to increase the output voltage to compensate voltage droop across the cable caused by the cable resistance.
17	ILIM	O	Average inductor current limit setting pin. Connect an external resistor between this pin and the AGND pin.
18	COMP	I	Output of the internal error amplifier. Connect the loop compensation network between this pin and the AGND pin.
19	VCC	O	Output of the internal regulator. A ceramic capacitor of more than 4.7 µF is required between this pin and the AGND pin.
20	BOOT2	O	Power supply for high-side MOSFET gate driver in boost side. A ceramic capacitor of 0.1 µF must be connected between this pin and the SW2 pin.
21, 25	SW2	I	The switching node pin of the boost side. It is connected to the drain of the internal low-side power MOSFET and the source of internal high-side power MOSFET.
22	BOOT1	I	Power supply for high-side MOSFET gate driver in buck side. A ceramic capacitor of 0.1 µF must be connected between this pin and the SW1 pin.
23	SW1	I	The switching node pin of the buck side. It is connected to the drain of the external low-side power MOSFET and the source of external high-side power MOSFET.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range at terminals(2)	VIN, SW1	–0.3	40	V
	DRH1, BOOT1	SW1–0.3	SW1+6	V
	VCC, DRL1, PG, $\overline{CC}$, ILIM, FSW, COMP, FB, MODE, CDC, DITH/SYNC	–0.3	6	V
	VOUT, SW2, ISP, ISN	–0.3	25	V
	ISP, ISN	VOUT-6	VOUT+6	V
	EN	-0.3	20	V
	BOOT2	SW2–0.3	SW2+6	V
	DRL1, $\overline{CC}$, ILIM, FSW, COMP, FB, MODE, CDC, DITH/SYNC	–0.3	VCC+0.3	V
T_J	Operating Junction, T_J (3)	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ (1)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(2)	±2000	V
		Charged-device model (CDM), per AEC Q100-011, all pins (3)	±500	
$V_{(ESD)}$ (1)	Electrostatic discharge	Charged-device model (CDM), per AEC Q100-011, corner pins (3)	±750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.7		36	V
V_{OUT}	Output voltage range	0.8		22	V
L	Effective inductance range	1	4.7	10	µH
C_{IN}	Effective input capacitance range	4.7	22		µF
C_{OUT}	Effective output capacitance range	10	100	1000	µF
T_J	Operating junction temperature	–40		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS552882-Q1 VQFN-HR (RPM)-26 PINS Standard	TPS552882-Q1 VQFN-HR (RPM)-26 PINS EVM(2)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.5	25.8	°C/W

THERMAL METRIC[1]		TPS552882-Q1 VQFN-HR (RPM)-26 PINS Standard	TPS552882-Q1 VQFN-HR (RPM)-26 PINS EVM[2]	UNIT
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.8	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.8	N/A	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	0.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	12.7	11.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.8	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Simulated on TPS552882-Q1EVM-045, 4-layer, 2-oz/2-oz/2-oz/2-oz copper 112-mm×71-mm PCB.

6.5 Electrical Characteristics

T_J = -40°C to 125°C, V_{IN} = 12 V and V_{OUT} = 20 V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		2.7		36	V
V_{VIN_UVLO}	Under voltage lockout threshold	V_{IN} rising	2.8	2.9	3.0	V
		V_{IN} falling	2.6	2.65	2.7	V
I_Q	Quiescent current into the VIN pin	IC enabled, no load, no switching. V_{IN} = 3 V to 24 V, V_{OUT} = 0.8 V, V_{FB} = V_{REF} + 0.1 V, R_{FSW}=100 kΩ, T_J up to 125°C		760	860	µA
	Quiescent current into the VOUT pin	IC enabled, no load, no switching, V_{IN} = 2.9 V, V_{OUT} = 3 V to 20 V, V_{FB} = V_{REF} + 0.1 V, R_{FSW}=100 kΩ, T_J up to 125°C		760	860	µA
I_{SD}	Shutdown current into VIN pin	IC disabled, V_{IN} = 2.9 V to 14 V, T_J up to 125°C		7	10	µA
V_{CC}	Internal regulator output	I_{VCC} = 50 mA, V_{IN} = 8 V, V_{OUT} = 20 V	5.0	5.2	5.4	V
V_{CC_DO}	VCC dropout	V_{IN} = 5.0 V, V_{OUT} = 20 V, I_{VCC} = 60 mA		200	320	mV
		V_{IN} = 14 V, V_{OUT} = 5.0 V, I_{VCC} = 60 mA		110	170	mV
EN/UVLO						
V_{EN_H}	EN Logic high threshold	VCC = 2.7 V to 5.5 V			1.15	V
V_{EN_L}	EN Logic low threshold	VCC = 2.7 V to 5.5 V	0.4			V
V_{EN_HYS}	Enable threshold hysteresis	VCC = 2.7 V to 5.5 V	0.05	0.12		V
V_{UVLO}	UVLO rising threshold at the EN/UVLO pin	VCC = 3.0 V to 5.5 V	1.20	1.23	1.26	V
V_{UVLO_HYS}	UVLO threshold hysteresis	VCC = 3.0 V to 5.5 V	8	14	20	mV
I_{UVLO}	Sourcing current at the EN/UVLO pin	V_{UVLO} = 1.3 V	4.5	5	5.5	µA
OUTPUT						
V_{OUT}	Output voltage range		0.8		22	V
V_{OVP}	Output overvoltage protection threshold		22.5	23.5	24.5	V
V_{OVP_HYS}	Over voltage protection hysteresis			1		V
I_{FB_LKG}	Leakage current at the FB pin	T_J up to 125°C			100	nA
I_{VOUT_LKG}	Leakage current into the VOUT pin	IC disabled, V_{OUT} = 20 V, V_{SW2} = 0 V, T_J up to 125°C		1	20	µA
REFERENCE VOLTAGE						
V_{REF}	Reference voltage at the FB pin		1.188	1.2	1.212	V
POWER SWITCH						

6.5 Electrical Characteristics (continued)

T_J = -40°C to 125°C, V_{IN} = 12 V and V_{OUT} = 20 V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS(on)}$	Low-side MOSFET on resistance on boost side	V_{OUT} = 20 V, V_{CC} = 5.2 V		7.1		mΩ
	High-side MOSFET on resistance on boost side	V_{OUT} = 20 V, V_{CC} = 5.2 V		7.6		mΩ
INTERNAL CLOCK						
f_{SW}	Switching frequency	R_{FSW} = 100 kΩ	180	200	220	kHz
		R_{FSW} = 9.09 kΩ	2000	2200	2400	kHz
t_{OFF_min}	Min. off time	Boost mode		100	145	ns
t_{ON_min}	Min. on-time	Buck mode		90	130	ns
V_{FSW}	Voltage at the FSW pin			1		V
CURRENT LIMIT						
I_{LIM_AVG}	Average inductor current limit	R_{ILIM} = 20 kΩ, V_{IN} = 8 V, V_{OUT} = 20 V, f_{SW} = 500 kHz, FPWM	14	16.5	19	A
		R_{ILIM} = 20 kΩ, V_{IN} = 8 V, V_{OUT} = 20 V, f_{SW} = 500 kHz, PFM	14	16.5	19	A
		R_{ILIM} = 60 kΩ, V_{IN} = 5 V, V_{OUT} = 14 V, f_{SW} = 2.2 MHz, FPWM	4	5.5		A
		R_{ILIM} = 60 kΩ, V_{IN} = 5 V, V_{OUT} = 14 V, f_{SW} = 2.2 MHz, PFM	4	5.5		A
I_{LIM_PK}	Peak inductor current limit at high side	R_{ILIM} = 20 kΩ, V_{IN} = 8 V, V_{OUT} = 20 V, f_{SW} = 500 kHz, FPWM		25		A
		R_{ILIM} = 20 kΩ, V_{IN} = 8 V, V_{OUT} = 20 V, f_{SW} = 500 kHz, PFM		25		A
V_{ILIM}	Voltage at the ILIM pin	VOUT = 3 V		0.6		V
V_{SNS}	Current loop regulation voltage between the ISP and ISN pins	V_{ISN} = 2 V to 21 V	48	50	52	mV
		V_{ISN} = 2 V to 21 V	28	30	32	mV
CABLE VOLTAGE DROP COMPENSATION						
V_{CDC}	Voltage at the CDC pin	R_{CDC} = 20 kΩ or floating, V_{ISP} – V_{ISN} = 50 mV	0.95	1	1.05	V
		R_{CDC} = 20 kΩ or floating, V_{ISP} – V_{ISN} = 2 mV		40	75	mV
I_{FB_CDC}	FB pin sinking current	External output feedback, R_{CDC} = 20 kΩ, V_{ISP} – V_{ISN} = 50 mV	7.23	7.5	7.87	µA
		External output feedback, R_{CDC} = 20 kΩ, V_{ISP} – V_{ISN} = 0 mV		0	0.3	µA
		External output feedback, R_{CDC} = floating, V_{ISP} – V_{ISN} = 50 mV		0	0.3	µA
ERROR AMPLIFIER						
I_{SINK}	COMP pin sink current	V_{FB} = V_{REF} + 400 mV, V_{COMP} = 1.5 V, VCC = 5 V		20		µA
I_{SOURCE}	COMP pin source current	V_{FB} = V_{REF} - 400 mV, V_{COMP} = 1.5 V, VCC = 5 V		60		µA
V_{CCLPH}	High clamp voltage at the COMP pin			1.8		V
V_{CCLPL}	Low clamp voltage at the COMP pin			0.7		V
G_{EA}	Error amplifier transconductance			190		µA/V
SOFT START						
t_{SS}	Soft-start time		3	4	5	ms
DR1H GATE DRIVER						
V_{DR1H_L}	Low-state voltage drop	V_{DR1H} – V_{SW1}, 100-mA sinking		0.1		V

6.5 Electrical Characteristics (continued)

T_J = -40°C to 125°C, V_{IN} = 12 V and V_{OUT} = 20 V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DR1H_H}	High-state voltage drop	$V_{BOOT1} – V_{DR1H}$, 100-mA sourcing		0.2		V
DR1L GATE DRIVER						
V_{DR1L_L}	Low-state voltage drop	100-mA sinking		0.1		V
V_{DR1L_H}	High-state voltage drop	$V_{CC} – V_{DR1L}$, 100-mA sourcing		0.2		V
SPREAD SPECTRUM						
I_{DITH_CHG}	Dithering charge current	$V_{DITH/SYNC}$ = 1.0 V, R_{FSW} = 49.9 kΩ; voltage rising from 0.85 V		2		µA
I_{DITH_DIS}	Dithering discharge current	$V_{DITH/SYNC}$ = 1.0 V, R_{FSW} = 49.9 kΩ; voltage falling from 1.15 V		2		µA
V_{DITH_H}	Dither high threshold			1.07		V
V_{DITH_L}	Dither low threshold			0.93		V
SYNCHRONOUS CLOCK						
V_{SNYC_H}	Sync clock high voltage threshold				1.2	V
V_{SYNC_L}	Sync clock low voltage threshold		0.4			V
t_{SYNC_MIN}	Minimum sync clock pulse width		50			ns
HICCUP						
t_{HICCUP}	Hiccup off time			76		ms
MODE RESISTANCE DETECTION						
I_{MODE}	Sourcing current from the MODE pin	V_{MODE} = 2.5 V	9	10	11	µA
V_{MODE_DT1}	Detection threshold voltage at the MODE pin		0.571	0.614	0.657	V
V_{MODE_DT2}			0.322	0.351	0.380	V
V_{MODE_DT3}			0.169	0.189	0.209	V
LOGIC INTERFACE						
I_{PG_H}	Leakage current into PG pin when outputting high impedance	V_{PG} = 5 V			100	nA
V_{PG_L}	Output low voltage range of the PG pin	Sinking 4-mA current		0.1	0.2	V
$I_{\overline{CC}\_H}$	Leakage current into $\overline{CC}$ pin when outputting high impedance	$V_{\overline{CC}}$ = 5 V			100	nA
$V_{\overline{CC}\_L}$	Output low voltage range of the $\overline{CC}$ pin	Sinking 4-mA current		0.1	0.2	V
PROTECTION						
T_{SD}	Thermal shutdown threshold	T_J rising		175		°C
T_{SD_HYS}	Thermal shutdown hysteresis	T_J falling below TSD		20		°C

6.6 Typical Characteristics

V_{IN} = 12 V, T_A = 25°C, f_{SW} = 400 kHz, unless otherwise noted.

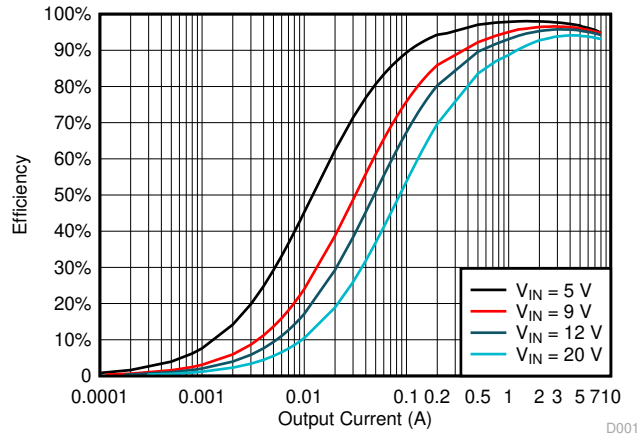


図 6-1. Efficiency vs Output Current, V_{OUT} = 5 V, FPWM

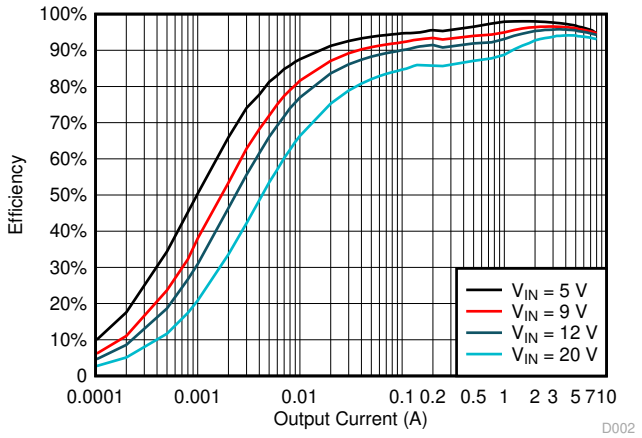


図 6-2. Efficiency vs Output Current, V_{OUT} = 5 V, PFM

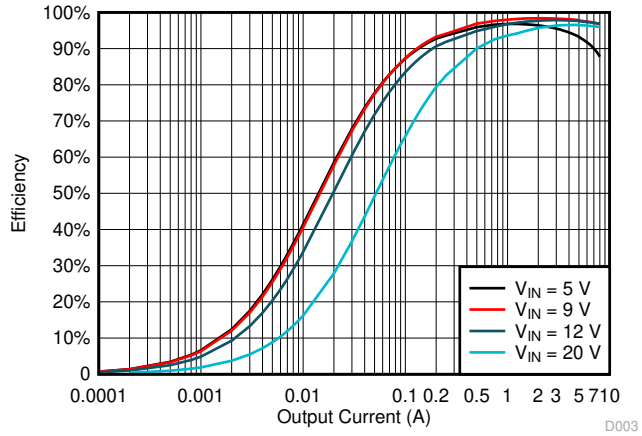


図 6-3. Efficiency vs Output Current, V_{OUT} = 9 V, FPWM

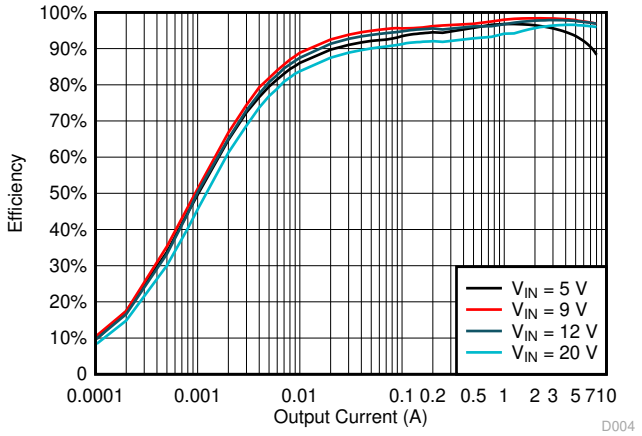


図 6-4. Efficiency vs Output Current, V_{OUT} = 9 V, PFM

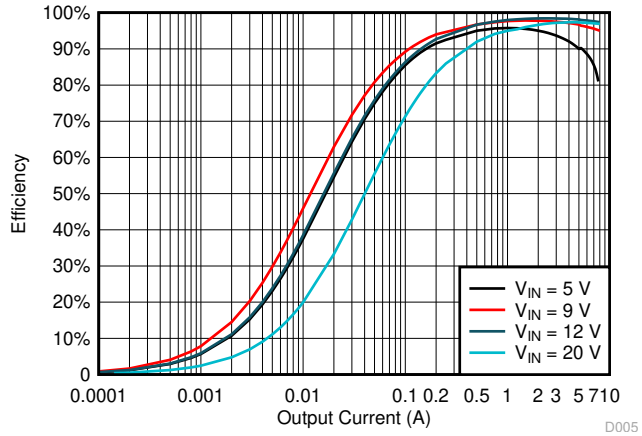


図 6-5. Efficiency vs Output Current, V_{OUT} = 12 V, FPWM

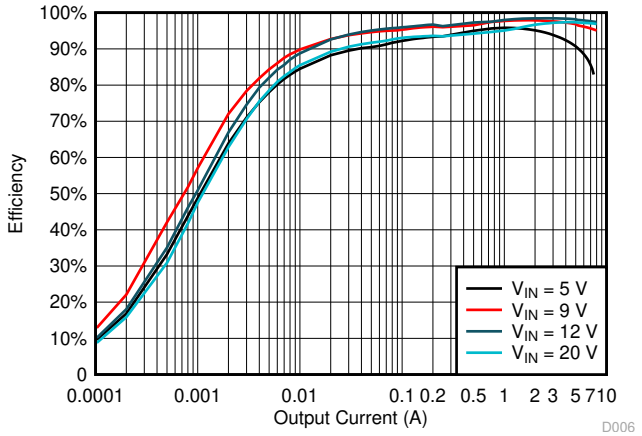


図 6-6. Efficiency vs Output Current, V_{OUT} = 12 V, PFM

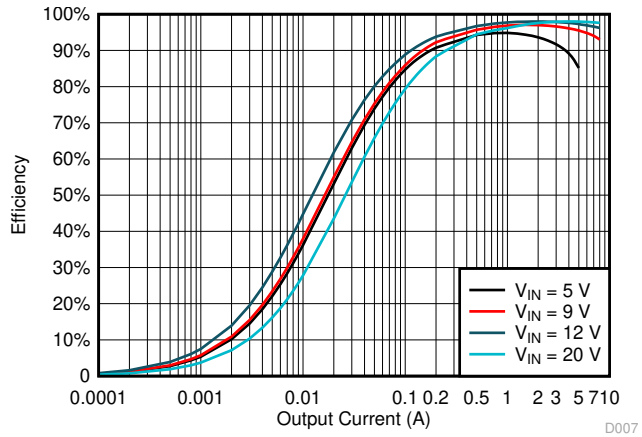


図 6-7. Efficiency vs Output Current, V_{OUT} = 15 V, FPWM

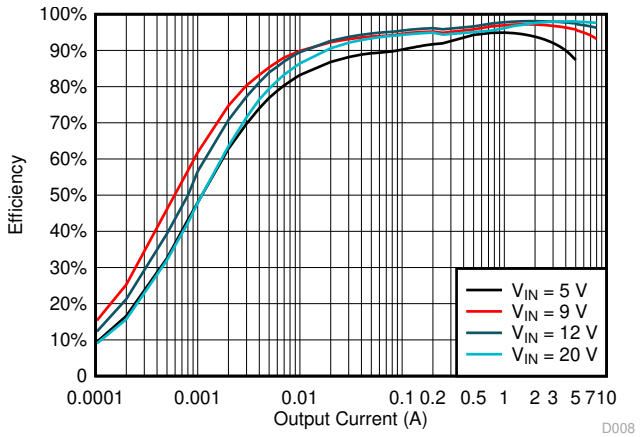


図 6-8. Efficiency vs Output Current, V_{OUT} = 15 V, PFM

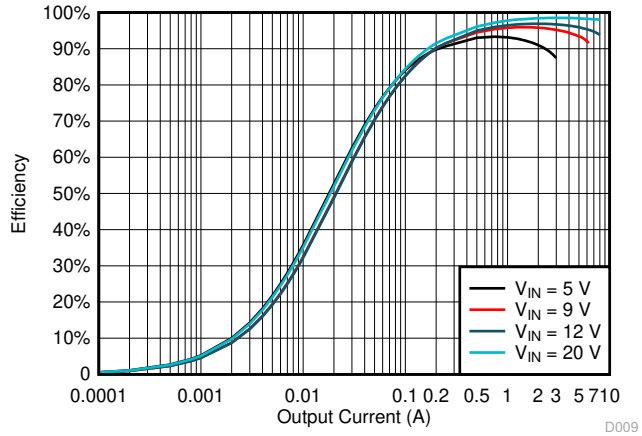


図 6-9. Efficiency vs Output Current, V_{OUT} = 20 V, FPWM

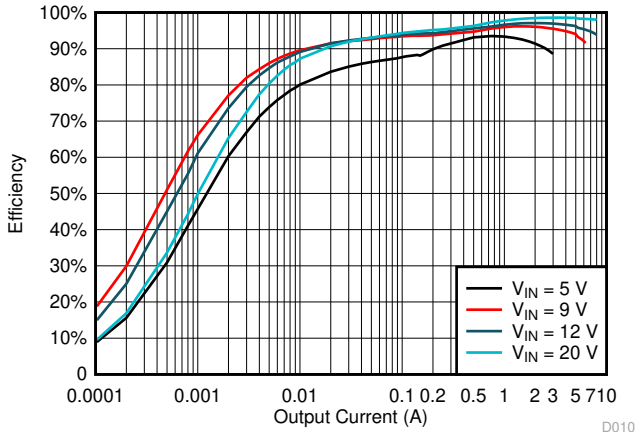


図 6-10. Efficiency vs Output Current, V_{OUT} = 20 V, PFM

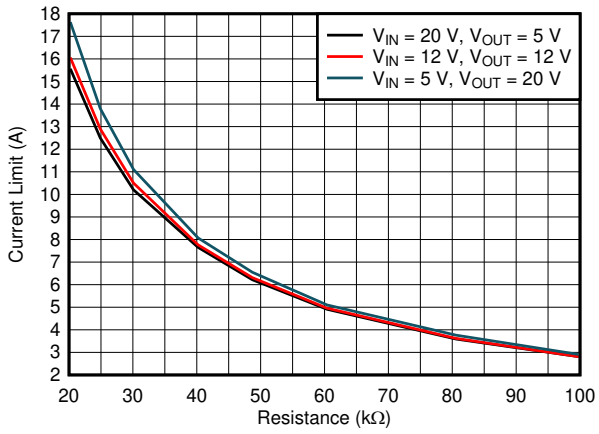


図 6-11. Average Inductor Current Limit vs Setting Resistance

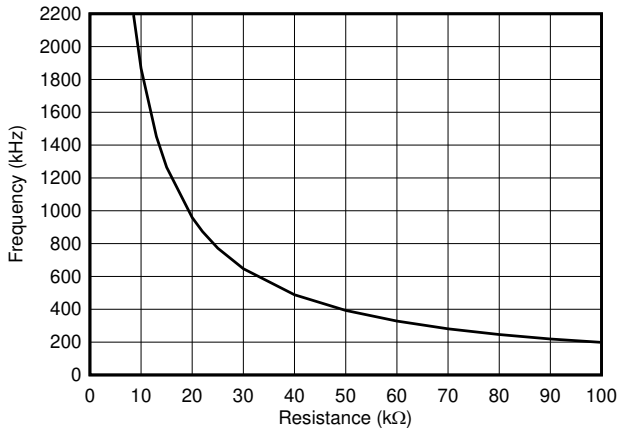


図 6-12. Switching Frequency vs Setting Resistance

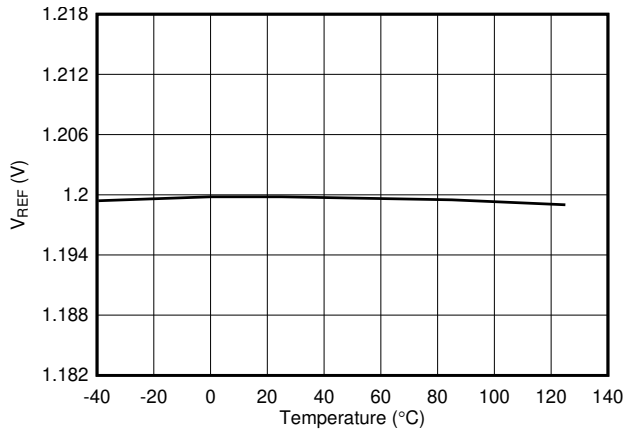


図 6-13. Reference Voltage vs Temperature (V_{REF} = 1.2 V)

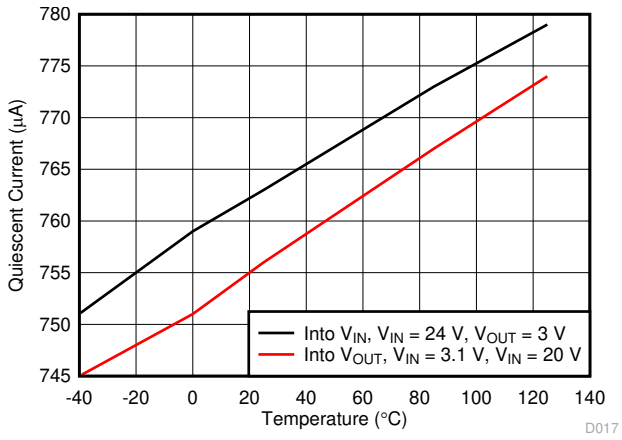


図 6-14. Quiescent Current vs Temperature

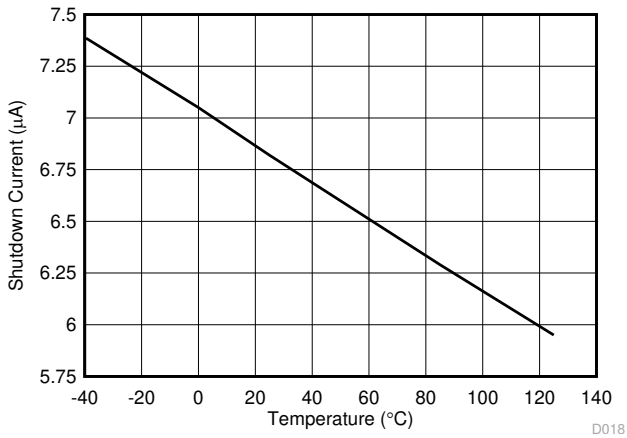


図 6-15. Shutdown Current vs Temperature

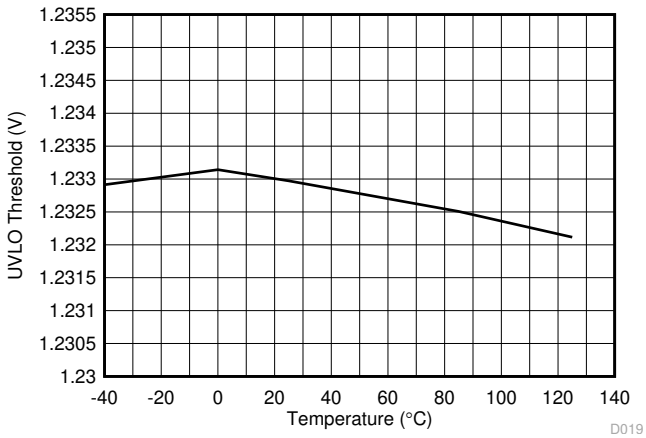


図 6-16. ENABLE/UVLO Rising Threshold vs Temperature

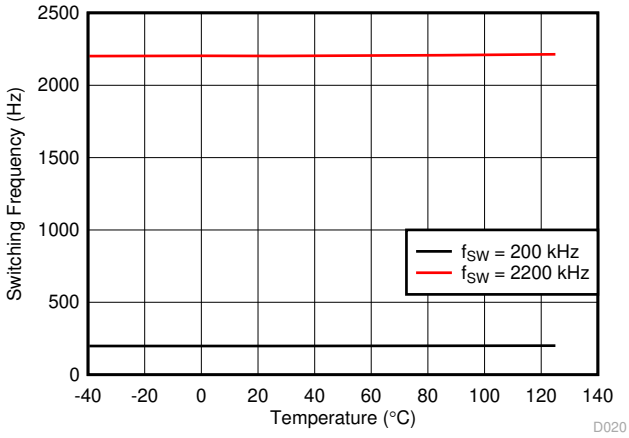


図 6-17. Switching Frequency vs Temperature

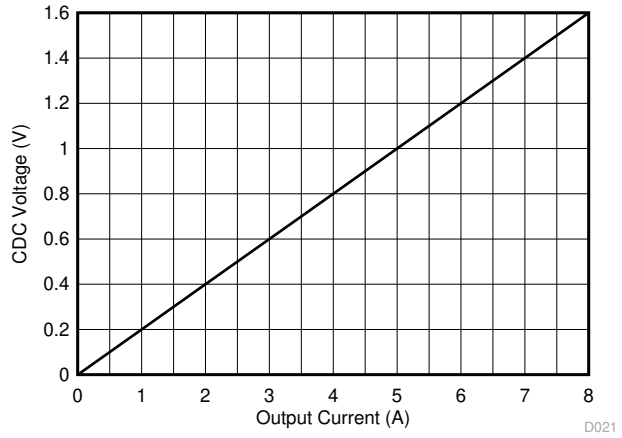


図 6-18. CDC Voltage vs Output Current with R_{SENSE} = 10 mΩ

7 Detailed Description

7.1 Overview

The TPS552882-Q1 is a 16-A buck-boost DC-to-DC converter with the two boost MOSFETs integrated. The TPS552882-Q1 can operate over a wide range of 2.7-V to 36-V input voltage and 0.8-V to 22-V output voltage. It can transition among buck mode, buck-boost mode, and boost mode smoothly according to the input voltage and the set output voltage. The TPS552882-Q1 operates in buck mode when the input voltage is greater than the output voltage and in boost mode when the input voltage is less than the output voltage. When the input voltage is close to the output voltage, the TPS552882-Q1 operates in one-cycle buck and one-cycle boost mode alternately.

The TPS552882-Q1 uses an average current mode control scheme. Current mode control provides simplified loop compensation, rapid response to the load transients, and inherent line voltage rejection. An error amplifier compares the feedback voltage with the internal reference voltage. The output of the error amplifier determines the average inductor current.

An internal oscillator can be configured to operate over a wide range of frequency from 200 kHz to 2.2 MHz. The internal oscillator can also synchronize to an external clock applied to the DITH/SYNC pin. To minimize EMI, the TPS552882-Q1 can dither the switching frequency at ±7% of the set frequency.

The TPS552882-Q1 works in fixed-frequency PWM mode at moderate to heavy load currents. In light load condition, the TPS552882-Q1 can be configured to automatically transition to PFM mode or be forced in PWM mode by either connecting a resistor at the MODE pin or setting the corresponding bit in an internal register.

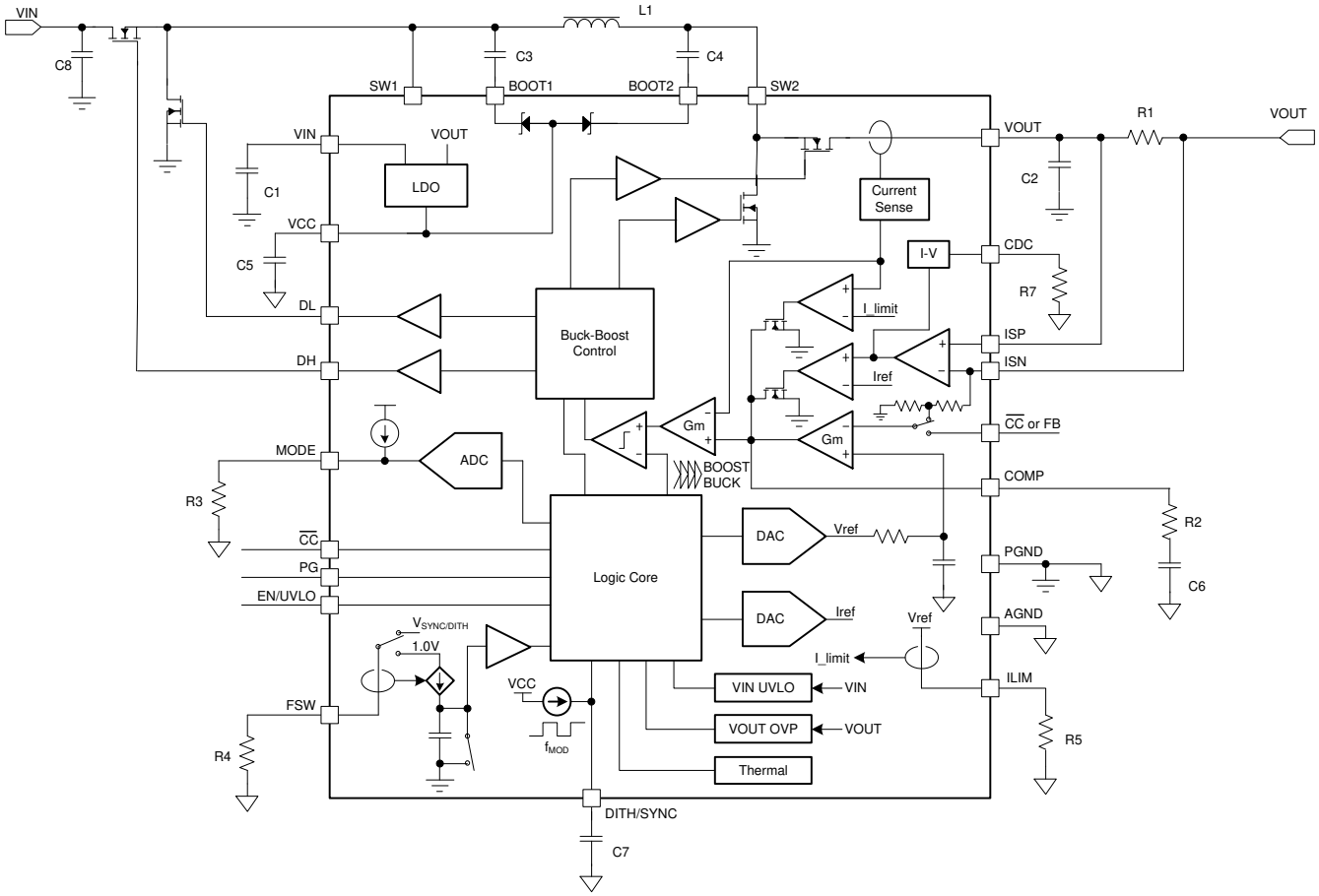
On TPS552882-Q1, you can use an external resistor divider to program the output voltage. The TPS552882-Q1 also can limit the output current by placing a current sense resistor in the output path. These two functions support the programmable power supply (PPS) feature of the USB-PD.

The TPS552882-Q1 provides average inductor current limit set by a resistor at the ILIM pin. In addition, it provides cycle-by-cycle peak inductor current limit during transient to protect the device against overcurrent condition beyond the capability of the device.

A precision voltage threshold of 1.23 V with 5-µA sourcing current at the EN/UVLO pin supports programmable input undervoltage lockout (UVLO) with hysteresis. The output overvoltage protection (OVP) feature turns off the high-side FETs to prevent damage to the devices powered by the TPS552882-Q1.

The device provides hiccup mode option to reduce the heating in the power components when output short circuit happens. When the hiccup mode is enabled, the TPS552882-Q1 turns off for 76 ms and restarts at soft start-up.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 VCC Power Supply

An internal LDO to supply the TPS552882-Q1 outputs regulated 5.2-V voltage at the VCC pin with 60-mA output current capability. When V_{IN} is less than V_{OUT}, the internal LDO selects the power supply source by comparing V_{IN} to a rising threshold of 6.2 V with 0.3-V hysteresis. When V_{IN} is higher than 6.2 V, the supply for LDO is V_{IN}. When V_{IN} is lower than 5.9 V, the supply for LDO is V_{OUT}. When V_{OUT} is less than V_{IN}, the internal LDO selects the power supply source by comparing V_{OUT} to a rising threshold of 6.2 V with 0.3-V hysteresis. When V_{OUT} is higher than 6.2 V, the supply for LDO is V_{OUT}. When V_{OUT} is lower than 5.9 V, the supply for LDO is V_{IN}. 表 7-1 shows the supply source selection for the internal LDO.

表 7-1. V_{CC} Power Supply Logic

V_{IN}	V_{OUT}	INPUT for V_{CC} LDO
V_{IN} > 6.2 V	V_{OUT}>V_{IN}	V_{IN}
V_{IN} < 5.9 V	V_{OUT}>V_{IN}	V_{OUT}
V_{IN} > V_{OUT}	V_{OUT}> 6.2 V	V_{OUT}
V_{IN} > V_{OUT}	V_{OUT}< 5.9 V	V_{IN}

To minimize the power dissipation of the internal LDO when both input voltage and output voltage are high, an external 5-V power source can be applied at the VCC pin to supply the TPS552882-Q1. The external 5-V power supply must have at least 100-mA output current capability and must be within the 4.75-V to 5.5-V regulation range. To use an external power supply for V_{CC}, a resistor with proper resistance must be connected to the MODE pin.

7.3.2 Operation Mode Setting

By placing different resistors between the MODE pin and the AGND pin, the TPS552882-Q1 selects the internal power supply or external power supply for V_{CC}, and also selects the PFM mode or forced PWM mode in light load conditions.表 7-2 shows the resistance values for each selection.

表 7-2. V_{CC} Source and PFM/PWM Programming

RESISTOR VALUE (kΩ)	V_{CC} SOURCE	OPERATING MODE AT LIGHT LOAD
0	Internal	PWM
24.9	Internal	PFM
51.1	External	PWM
Open	External	PFM

7.3.3 Input Undervoltage Lockout

When the input voltage is below 2.6 V, the TPS552882-Q1 is disabled. When the input voltage is above 3 V, the TPS552882-Q1 can be enabled by pulling the EN pin to a high voltage above 1.3 V.

7.3.4 Enable and Programmable UVLO

The TPS552882-Q1 has a dual function enable and undervoltage lockout (UVLO) circuit. When the input voltage at the VIN pin is above the input UVLO rising threshold of 3 V and the EN/UVLO pin is pulled above 1.15 V but less than the enable UVLO threshold of 1.23 V, the TPS552882-Q1 is enabled but still in standby mode. The TPS552882-Q1 starts to detect the resistance between the MODE pin and ground. After that, the TPS55288x selects the power supply for V_{CC} and the PFM or FPWM mode for light load condition accordingly.

The EN/UVLO pin has an accurate UVLO voltage threshold to support programmable input undervoltage lockout with hysteresis. When the EN/UVLO pin voltage is greater than the UVLO threshold of 1.23 V, the TPS552882-Q1 is enabled for switching operation. A hysteresis current I_{UVLO_HYS} of 5 µA is sourced out of the EN/UVLO pin to provide hysteresis that prevents on/off chattering in the presence of noise with a slowly changing input voltage.

By using resistor divider as shown in 図 7-1, the turnon threshold is calculated using 式 1.

$$V_{IN(UVLO\_ON)} = V_{UVLO} \times (1 + \frac{R1}{R2}) \quad (1)$$

where

- V_{UVLO} is the UVLO threshold of 1.23 V at the EN/UVLO pin

The hysteresis between the UVLO turnon threshold and turnoff threshold is set by the upper resistor in the EN/UVLO resistor divider and is given by the 式 2.

$$\Delta V_{IN(UVLO)} = I_{UVLO\_HYS} \times R1 \quad (2)$$

where

- I_{UVLO_HYS} is the sourcing current from the EN/UVLO pin when the voltage at the EN/UVLO pin is above V_{UVLO}

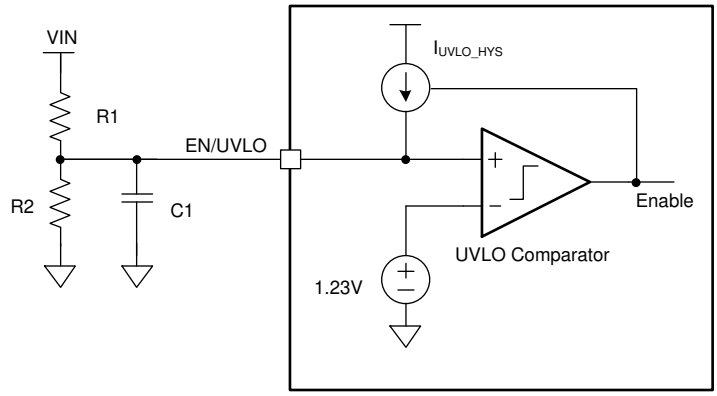


図 7-1. Programmable UVLO With Resistor Divider at the EN/UVLO Pin

Using an NMOS FET together with resistor divider can implement both logic enable and programmable UVLO as shown in 図 7-2. The EN logic high level must be greater than enable threshold plus the V_{th} of the NMOSFET Q1. The Q1 also eliminates the leakage current from VIN to ground through the UVLO resistor divider during shutdown mode.

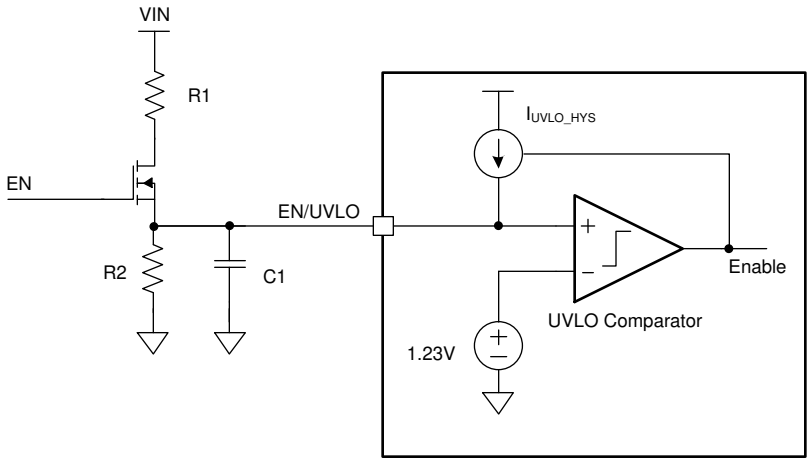


図 7-2. Logic Enable and Programmable UVLO

7.3.5 Soft Start

When the input voltage is above the UVLO threshold and the voltage at the EN/UVLO pin is above the enable UVLO threshold, the TPS552882-Q1 starts to ramp up the output voltage by ramping an internal reference voltage from 0 V to a voltage which is set by 1.2 V on the TPS552882-Q1 within 4 ms.

7.3.6 Shutdown

When the EN pin voltage is pulled below 0.4 V, the TPS552882-Q1 is in shutdown mode, and all functions are disabled.

7.3.7 Switching Frequency

The TPS552882-Q1 uses a fixed frequency average current control scheme. The switching frequency is between 200 kHz and 2.2 MHz set by placing a resistor at the FSW pin. An internal amplifier holds this pin at a fixed voltage of 1 V. The setting resistance is between maximum of 100 kΩ and minimum of 9.09 kΩ. Use 式 3 to calculate the resistance by a given switching frequency.

$$f_{SW} = \frac{1000}{0.05 \times R_{FSW} + 20} \text{ (MHz)} \quad (3)$$

where

- R_{FSW} is the resistance at the FSW pin

For noise-sensitive applications, the TPS552882-Q1 can be synchronized to an external clock signal applied to the DITH/SYNC pin. The duty cycle of the external clock is recommended in the range of 30% to 70%. A resistor also must be connected to the FSW pin when the TPS552882-Q1 is switching by the external clock. The external clock frequency at the DITH/SYNC pin must have lower than 0.4-V low level voltage and must be within ±30% of the corresponding frequency set by the resistor. 図 7-3 is a recommended configuration.

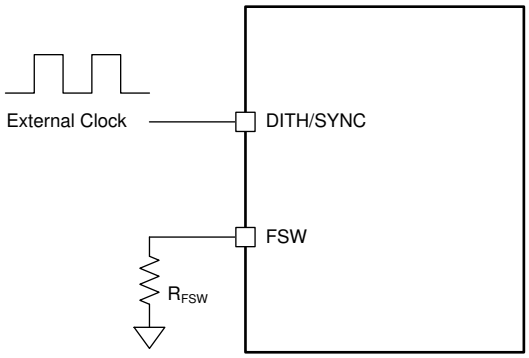


図 7-3. External Clock Configuration

7.3.8 Switching Frequency Dithering

The TPS552882-Q1 provides an optional switching frequency dithering that is enabled by connecting a capacitor from the DITH/SYNC pin to ground. 図 7-4 illustrates the dithering circuit. By charging and discharging the capacitor, a triangular waveform centered at 1 V is generated at the DITH/SYNC pin. The triangular waveform modulates the oscillator frequency by ±7% of the nominal frequency set by the resistance at the FSW pin. The capacitance at the DITH/SYNC pin sets the modulation frequency. A small capacitance modulates the oscillator frequency at a fast rate than a large capacitance. For the dithering circuit to effectively reduce peak EMI, the modulation rate normally is below 1 kHz. Equation 4 calculates the capacitance required to set the modulation frequency, F_{MOD}.

$$C_{DITH} = \frac{1}{2.8 \times R_{FSW} \times F_{MOD}} (F) \quad (4)$$

where

- R_{FSW} is the switching frequency setting resistance (Ω) at the FSW pin
- F_{MOD} is the modulation frequency (Hz) of the dithering

Connecting the DITH/SYNC pin below 0.4 V or above 1.2 V disables switching frequency dithering. The dithering function also is disabled when an external synchronous clock is used.

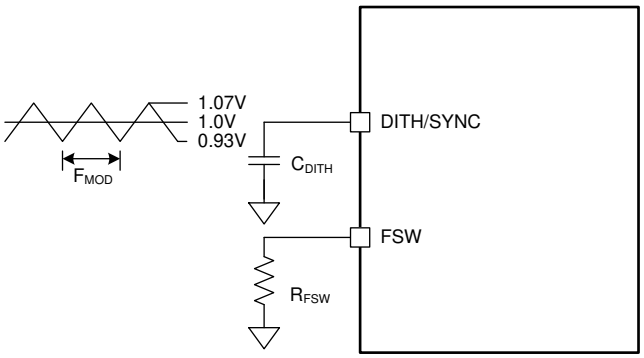


図 7-4. Switching Frequency Dithering

7.3.9 Inductor Current Limit

The TPS552882-Q1 implements both peak current and average inductor current limit by a resistor connected to the ILIM pin. The average current mode control loop uses the current sense information at the high-side MOSFET of the boost leg to clamp the maximum average inductor current to 16.5 A (typical) when the resistor is 20 kΩ. Use 式 5 to calculate the resistance for a desired average inductor current limit.

$$I_{AVG\_LIMIT} = \frac{\min(1, 0.6 \times V_{OUT}) \times 330000}{R_{ILIM}} (A) \quad (5)$$

where

- I_{AVG_LIMIT} is the average inductor current limit
- R_{ILIM} is the resistance (Ω) between the ILIM pin and analog ground

Besides the average current limit, a peak current limit protection is implemented during transient to protect the device against over current condition beyond the capability of the device.

7.3.10 Internal Charge Path

Each of the two high-side MOSFET drivers is biased from its floating bootstrap capacitor, which is normally re-charged by V_{CC} through both the external and internal bootstrap diodes when the low-side MOSFET is turned on. When the TPS55288 operates exclusively in the buck or boost regions, one of the high-side MOSFETs is constantly on. An internal charge path, from VOUT and BOOT2 to BOOT1 or from VIN and BOOT1 to BOOT2, charges the bootstrap capacitor to V_{CC} so that the high-side MOSFET remains on.

7.3.11 Output Voltage Setting

There are two ways to set the output voltage: changing the feedback ratio and changing the reference voltage. The TPS552882-Q1 uses an external resistor divider to change the feedback ratio with fixed 1.2-V reference voltages at the FB pin.

When using external output voltage feedback resistor divider as shown in 図 7-5. Use 式 6 to calculate the output voltage with the reference voltage at the FB pin.

$$V_{OUT} = V_{REF} \times (1 + \frac{R_{FB\_UP}}{R_{FB\_BT}}) \quad (6)$$

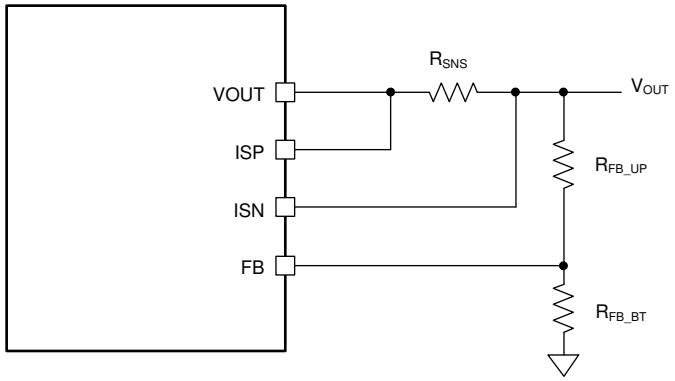


図 7-5. Output Voltage Setting by External Resistor Divider

TI recommends using 100 kΩ for the up resistor R_{FB_UP}. The reference voltage V_{REF} at the FB pin is 1.2 V.

7.3.12 Output Current Indication and Cable Voltage Drop Compensation

The TPS55288 outputs a voltage at the CDC pin proportional to the sensed voltage across a output current sensing resistor between the ISP pin and the ISN pin. 式 7 shows the exact voltage at the CDC pin related to the sensed output current.

$$V_{CDC} = 20 \times (V_{ISP} - V_{ISN}) \quad (7)$$

To compensate the voltage drop across a cable from the terminal of the USB port to its powered device, the TPS552882-Q1 can lift its output voltage in proportion to the load current by placing a resistor between the CDC pin and AGND pin.

When using external output voltage feedback on the TPS552882-Q1, the output voltage rises in proportional to the current sourcing from the CDC pin through the resistor at the CDC pin. It is recommended to use 100-kΩ resistance for the up resistor of the resistor divider. 式 8 shows the output voltage rise versus the sensed output current, resistance at the CDC pin and the up resistor of the output voltage feedback resistor divider.

$$V_{OUT\_CDC} = 3 \times R_{FB\_UP} \times \left(\frac{V_{ISP} - V_{ISN}}{R_{CDC}}\right) \quad (8)$$

where

- R_{FB_UP} is the up resistor of the resistor divider between the output and the FB/$\overline{INT}$ pin
- R_{CDC} is the resistor at the CDC pin

When RFB_UP is 100 kΩ, the output voltage rise versus the sensed output current and the resistor at the CDC pin is shown in 図 7-6

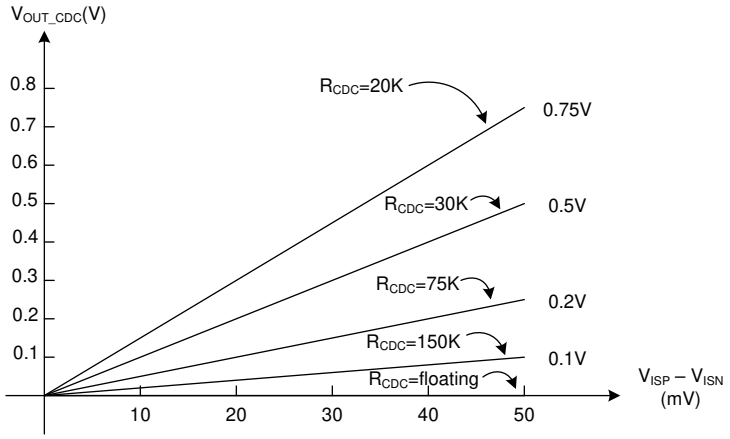


図 7-6. Output Voltage Rise versus Output Current

7.3.13 Integrated Gate Drivers

The TPS552882-Q1 provides two N-channel MOSFET gate drivers for buck side. Each driver is capable of sourcing 1-A and sinking 1.8-A peak current. In buck operation, the DR1H pin and the DR1L pin are switched by the PWM controller. In boost mode, the DR1H pin remains at continuously high voltage to turn on the high-side MOSFET of the buck side, and the DR1L pin remains at continuously low voltage to turn off the low-side MOSFET of the buck side.

In DCM buck mode operation, the DR1L turns off the low-side FET when the inductor current drops to zero.

The low-side gate driver is powered from the VCC pin, and the high-side gate driver is powered from the bootstrap capacitor C_{BOOT1}, which is between the BOOT1 pin and the SW1 pin.

7.3.14 Output Current Limit

The output current limit is programmable by placing a current sensing resistor between the ISP pin and ISN pin. The voltage limit between the ISP pin and the ISN pin is set to 50 mV. Thus a smaller resistance gets higher current limit and a bigger resistance gets lower current limit.

Connecting the ISP pin and ISN pin together to the VOUT pin disables the current limit function.

7.3.15 Overvoltage Protection

The TPS552882-Q1 has output overvoltage protection. When the output voltage at the VOUT pin is detected above 23.5 V typically, the TPS552882-Q1 turns off two high-side FETs and turns on two low-side FETs until its output voltage drops the hysteresis value lower than the output overvoltage protection threshold. This function prevents overvoltage on the output and secures the circuits connected to the output from excessive overvoltage.

7.3.16 Output Short Circuit Protection

In addition to the average inductor current limit, the TPS552882-Q1 implements the output short-circuit protection by entering the hiccup mode. When the output short circuit happens, the TPS552882-Q1 goes into output current limit first. If the output voltage is below 0.8 V and the average inductor current is above the setting value, the TPS552882-Q1 shuts down the switching for 76 ms (typical) and restarts the soft start repeatedly. The hiccup mode helps reduce the total power dissipation on the TPS552882-Q1 in the output short-circuit or overcurrent condition.

7.3.17 Thermal Shutdown

The TPS552882-Q1 is protected by a thermal shutdown circuit that shuts down the device when the internal junction temperature exceeds 175°C (typical). The internal soft-start circuit is reset but all internal registers values remain unchanged when thermal shutdown is triggered. The converter automatically restarts when the junction temperature drops below the thermal shutdown hysteresis of 20°C below the thermal shutdown threshold.

7.4 Device Functional Modes

In light load condition, the TPS552882-Q1 can work in PFM or forced PWM mode to meet different application requirements. The PFM mode decreases switching frequency to reduce the switching loss thus it gets high efficiency at light load condition. The FPWM mode keeps the switching frequency unchanged to avoid undesired low switching frequency but the efficiency becomes lower than that of PFM mode.

7.4.1 PWM Mode

In FPWM mode, the TPS552882-Q1 keeps the switching frequency unchanged in light load condition. When the load current decreases, the output of the internal error amplifier decreases as well to reduce the average inductor current down to deliver less power from input to output. When the output current further reduces, the current through the inductor decreases to zero during the switch-off time. The high-side N-MOSFET is not turned off even if the current through the MOSFET is zero. Thus, the inductor current changes its direction after it runs to zero. The power flow is from output side to input side. The efficiency is low in this condition. However, with the fixed switching frequency, there is no audible noise or other problems that might be caused by low switching frequency in light load condition.

7.4.2 Power Save Mode

The TPS552882-Q1 improves the efficiency at light load condition with the PFM mode. By connecting an appropriate resistor at the MODE pin or enabling the PFM function in the internal register, the TPS552882-Q1 can work in PFM mode at light load condition. When the TPS552882-Q1 operates at light load condition, the output of the internal error amplifier decreases to make the inductor peak current down to deliver less power to the load. When the output current further reduces, the current through the inductor will decrease to zero during the switch-off time. When the TPS552882-Q1 works in buck mode, once the inductor current becomes zero, the low-side switch of the buck side is turned off to prevent the reverse current from output to ground. When the TPS552882-Q1 works in boost mode, once the inductor current becomes zero, the high side-switch of the boost side is turned off to prevent the reverse current from output to input. The TPS552882-Q1 resumes switching until

the output voltage drops. Thus the PFM mode reduces switching cycles and eliminates the power loss by the reverse inductor current to get high efficiency in light load condition.

8 Application and Implementation

Note

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8.1 Application Information

The TPS552882-Q1 can operate over a wide range of 2.7-V to 36-V input voltage and output 0.8 V to 22 V. It can transition among buck mode, buck-boost mode, and boost mode smoothly according to the input voltage and the setting output voltage. The TPS552882-Q1 operates in buck mode when the input voltage is greater than the output voltage and in boost mode when the input voltage is less than the output voltage. When the input voltage is close to the output voltage, the TPS552882-Q1 operates in one-cycle buck and one-cycle boost mode alternately. The switching frequency is set by an external resistor. To reduce the switching power loss in high power conditions, it is recommended to set the switching frequency below 500 kHz. If a system requires higher switching frequency above 500 kHz, it is recommended to set the lower switch current limit for better thermal performance.

8.2 Typical Application

The TPS552882-Q1 provides a small size solution for USB PD power supply application with the input voltage ranging from 9 V to 36 V.

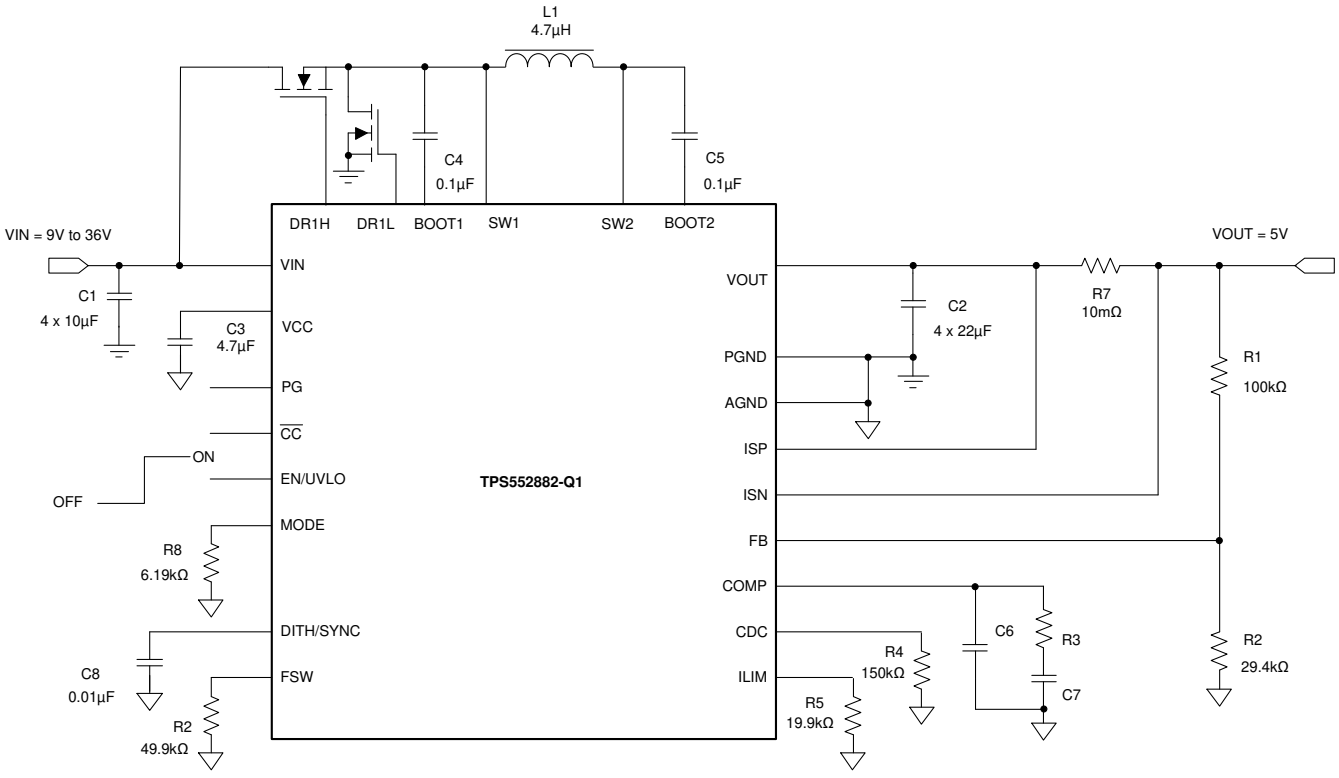

図 8-1. 5-V Power Supply With 9-V to 36-V Input Voltage

8.2.1 Design Requirements

The design parameters are listed in 表 8-1:

表 8-1. Design Parameters

PARAMETERS	VALUES
Input voltage	9 V to 36 V
Output voltage	5 V to 20 V
Output current limit	5 A
Output voltage ripple	±50 mV
Operating mode at light load	PFM

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS552882-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Switching Frequency

The switching frequency of the TPS552882-Q1 is set by a resistor at the FSW pin. Use 式 3 to calculate the resistance for the desired frequency. To reduce the switching power loss with such a high current application, a 1% standard resistor of 49.9 kΩ is selected for 400-kHz switching frequency for this application.

8.2.2.3 Output Voltage Setting

An external resistor divider is used to program the output voltage.

8.2.2.4 Inductor Selection

Since the selection of the inductor affects steady state operation, transient behavior, and loop stability, the inductor is the most important component in power regulator design. There are three important inductor specifications: inductance, saturation current, and DC resistance.

The TPS552882-Q1 is designed to work with inductor values between 1 µH and 10 µH. The inductor selection is based on consideration of both buck and boost modes of operation.

For buck mode, the inductor selection is based on limiting the peak-to-peak current ripple to the maximum inductor current at the maximum input voltage. In CCM, 式 9 shows the relationship between the inductance and the inductor ripple current.

$$L = \frac{(V_{IN(MAX)} - V_{OUT}) \times V_{OUT}}{\Delta I_{L(P-P)} \times f_{SW} \times V_{IN(MAX)}} \quad (9)$$

where

- $V_{IN(MAX)}$ is the maximum input voltage
- V_{OUT} is the output voltage
- $\Delta I_{L(P-P)}$ is the peak to peak ripple current of the inductor
- f_{SW} is the switching frequency

For a certain inductor, the inductor ripple current achieves maximum value when V_{OUT} equals half of the maximum input voltage. Choosing higher inductance gets smaller inductor current ripple while smaller inductance gets larger inductor current ripple.

For boost mode, the inductor selection is based on limiting the peak-to-peak current ripple to the maximum inductor current at the maximum output voltage. In CCM, 式 10 shows the relationship between the inductance and the inductor ripple current.

$$L = \frac{V_{IN} \times (V_{OUT(MAX)} - V_{IN})}{\Delta I_{L(P-P)} \times f_{SW} \times V_{OUT(MAX)}} \quad (10)$$

where

- V_{IN} is the input voltage
- $V_{OUT(MAX)}$ is the maximum output voltage
- $\Delta I_{L(P-P)}$ is the peak to peak ripple current of the inductor
- f_{SW} is the switching frequency

For a certain inductor, the inductor ripple current achieves maximum value when V_{IN} equals to the half of the maximum output voltage. Choosing higher inductance gets smaller inductor current ripple while smaller inductance gets larger inductor current ripple.

For this application example, a 4.7-µH inductor is selected, which produces approximate maximum inductor current ripple of 50% of the highest average inductor current in buck mode and 50% of the highest average inductor current in boost mode.

In buck mode, the inductor DC current equals to the output current. In boost mode, the inductor DC current can be calculated with 式 11.

$$I_{L(DC)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (11)$$

where

- V_{OUT} is the output voltage
- I_{OUT} is the output current
- V_{IN} is the input voltage
- η is the power conversion efficiency

For a given maximum output current of the buck-boost converter TPS552882-Q1, the maximum inductor DC current happens at the minimum input voltage and maximum output voltage. Set the inductor current limit of the TPS552882-Q1 higher than the calculated maximum inductor DC current to make sure the TPS552882-Q1 has the desired output current capability.

In boost mode, the inductor ripple current is calculated with 式 12.

$$\Delta I_{L(P-P)} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{L \times f_{SW} \times V_{OUT}} \quad (12)$$

where

- $\Delta I_{L(P-P)}$ is the inductor ripple current
- L is the inductor value
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Therefore, the inductor peak current is calculated with 式 13.

$$I_{L(P)} = I_{L(DC)} + \frac{\Delta I_{L(P-P)}}{2} \quad (13)$$

Normally, it is advisable to work with an inductor peak-to-peak current of less than 40% of the average inductor current for maximum output current. A smaller ripple from a larger valued inductor reduces the magnetic hysteresis losses in the inductor and EMI, but in the same way, load transient response time is increased. The selected inductor must have higher saturation current than the calculated peak current.

The conversion efficiency is dependent on the resistance of its current path. The switching loss associated with the switching MOSFETs, and the inductor core loss. Therefore, the overall efficiency is affected by the inductor DC resistance (DCR), equivalent series resistance (ESR) at the switching frequency, and the core loss. 表 8-2 lists recommended inductors for the TPS552882-Q1. In this application example, the Coilcraft inductor XAL1010-472 is selected for its small size, high saturation current, and small DCR.

表 8-2. Recommended Inductors

PART NUMBER	L (µH)	DCR (MAXIMUM) (mΩ)	SATURATION CURRENT / HEAT RATING CURRENT (A)	SIZE (L x W x H mm)	VENDOR(1)
XAL1010-472ME	4.7	10	25.4/17.5	11.3 × 10 × 10	Coilcraft
IHLP5050EZER4R7	4.7	10.1	17.8/15.3	13.5 × 12.9 × 5	Vishay
125CDMCCDS-4R7MC	4.7	10	22/14	13.5 × 12.6 × 5	Sumida

(1) See the *Third-Party Products Disclaimer*.

8.2.2.5 Input Capacitor

In buck mode, the input capacitor supplies high ripple current. The RMS current in the input capacitors is given by 式 14.

$$I_{CIN(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times V_{IN}}} \quad (14)$$

where

- $I_{CIN(RMS)}$ is the RMS current through the input capacitor
- I_{OUT} is the output current

The maximum RMS current occurs at the output voltage is half of the input voltage, which gives $I_{CIN(RMS)} = I_{OUT} / 2$. Ceramic capacitors are recommended for their low ESR and high ripple current capability. A total of 20 µF effective capacitance is a good starting point for this application.

8.2.2.6 Output Capacitor

In boost mode, the output capacitor conducts high ripple current. The output capacitor RMS ripple current is given by 式 15, where the minimum input voltage and the maximum output voltage correspond to the maximum capacitor current.

$$I_{COUT(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} - 1} \quad (15)$$

where

- $I_{COUT(RMS)}$ is the RMS current through the output capacitor
- I_{OUT} is the output current

In this example, the maximum output ripple RMS current is 5.5 A.

The ESR of the output capacitor causes an output voltage ripple given by 式 16 in boost mode.

$$V_{RIPPLE(ESR)} = \frac{I_{OUT} \times V_{OUT}}{V_{IN}} \times R_{COUT} \quad (16)$$

where

- R_{COUT} is the ESR of the output capacitance

The capacitance also causes a capacitive output voltage ripple given by 式 17 in boost mode. When input voltage reaches the minimum value and the output voltage reaches the maximum value, there is the largest output voltage ripple caused by the capacitance.

$$V_{RIPPLE(CAP)} = \frac{I_{OUT} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right)}{C_{OUT} \times f_{SW}} \quad (17)$$

Typically, a combination of ceramic capacitors and bulk electrolytic capacitors is needed to provide low ESR, high ripple current, and small output voltage ripple. From the required output voltage ripple, use 式 16 and 式 17 to calculate the minimum required effective capacitance of the C_{OUT}.

8.2.2.7 Output Current Limit Sense Resistor

The output current limit is implemented by putting a current sense resistor between the ISP and ISN pins. The value of the limit voltage between the ISP and ISN pins is 50 mV. The current sense resistor between the ISP and ISN pins should be selected to ensure that the output current limit is set high enough for output. The output current limit setting resistor is given by 式 18.

$$R_{SNS} = \frac{V_{SNS}}{I_{OUT\_LIMIT}} \quad (18)$$

where

- V_{SNS} is the current limit setting voltage between the ISP and ISN pin
- I_{OUT_LIMIT} is the desired output current limit

Because the power dissipation is large, make sure the current sense resistor has enough power dissipation capability with large package.

8.2.2.8 Loop Stability

The TPS55288 uses average current control scheme. The inner current loop uses internal compensation and requires the inductor value must be larger than $1.2/f_{SW}$. The outer voltage loop requires an external compensation. The COMP pin is the output of the internal voltage error amplifier. An external compensation network comprised of resistor and ceramic capacitors is connected to the COMP pin.

The TPS55288 operates in buck mode or boost mode. Therefore, both buck and boost operating modes require loop compensations. The restrictive one of both compensations is selected as the overall compensation from a loop stability point of view. Typically for a converter designed either work in buck mode or boost mode, the boost mode compensation design is more restrictive due to the presence of a right half plane zero (RHPZ).

The power stage in boost mode can be modeled by 式 19.

$$G_{PS}(s) = \frac{R_{LOAD} \times (1-D)}{2 \times R_{SENSE}} \times \frac{\left(1 + \frac{s}{2\pi \times f_{ESRZ}}\right) \times \left(1 - \frac{s}{2\pi \times f_{RHPZ}}\right)}{1 + \frac{s}{2\pi \times f_P}} \quad (19)$$

where

- R_{LOAD} is the output load resistance
- D is the switching duty cycle in boost mode

- R_{SENSE} is the equivalent internal current sense resistor, which is 0.055 Ω

The power stage has two zeros and one pole generated by the output capacitor and load resistance. Use 式 20 to 式 22 to calculate them.

$$f_P = \frac{2}{2\pi \times R_{LOAD} \times C_{OUT}} \tag{20}$$

$$f_{ESRZ} = \frac{1}{2\pi \times R_{COUT} \times C_{OUT}} \tag{21}$$

$$f_{RHPZ} = \frac{R_{LOAD} \times (1-D)^2}{2\pi \times L} \tag{22}$$

The internal transconductance amplifier together with the compensation network at the COMP pin constitutes the control portion of the loop. The transfer function of the control portion is shown by 式 23.

$$G_C(s) = \frac{G_{EA} \times R_{EA} \times V_{REF}}{V_{OUT}} \times \frac{\left(1 + \frac{s}{2\pi \times f_{COMZ}}\right)}{\left(1 + \frac{s}{2\pi \times f_{COMP1}}\right) \times \left(1 + \frac{s}{2\pi \times f_{COMP2}}\right)} \tag{23}$$

where

- G_{EA} is the transconductance of the error amplifier
- R_{EA} is the output resistance of the error amplifier
- V_{REF} is the reference voltage input to the error amplifier
- V_{OUT} is the output voltage
- f_{COMP1} and f_{COMP2} are the pole's frequency of the compensation network
- f_{COMZ} is the zero's frequency of the compensation network

The total open-loop gain is the product of $G_{PS}(s)$ and $G_C(s)$. The next step is to choose the loop crossover frequency, f_C, at which the total open-loop gain is 1, namely 0 dB. The higher in frequency that the loop gain stays above 0 dB before crossing over, the faster the loop response. It is generally accepted that the loop gain cross over 0 dB at the frequency no higher than the lower of either 1/10 of the switching frequency, f_{SW} or 1/5 of the RHPZ frequency, f_{RHPZ}.

Then, set the value of R_C, C_C and C_P by 式 24 to 式 26.

$$R_C = \frac{2\pi \times V_{OUT} \times R_{SENSE} \times C_{OUT} \times f_C}{(1-D) \times V_{REF} \times G_{EA}} \tag{24}$$

where

- f_C is the selected crossover frequency

$$C_C = \frac{R_{LOAD} \times C_{OUT}}{2 \times R_C} \tag{25}$$

$$C_P = \frac{R_{COUT} \times C_{OUT}}{R_C} \tag{26}$$

If the calculated C_P is less than 10 pF, it can be left open.

Designing the loop for greater than 45° of phase margin and greater than 10-dB gain margin eliminates output voltage ringing during the line and load transient.

8.2.3 Application Curves

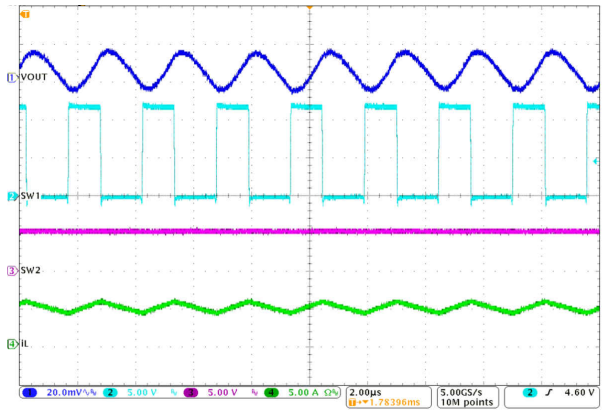

図 8-2. Switching Waveforms in V_{IN} = 12 V, V_{OUT} = 5 V, I_O = 5 A, FPWM

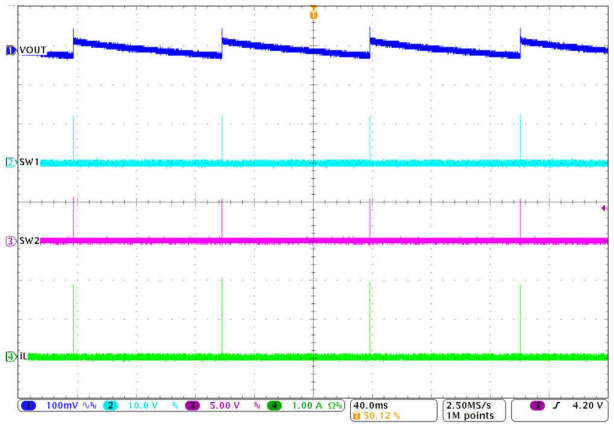

図 8-3. Switching Waveforms in V_{IN} = 12 V, V_{OUT} = 5 V, I_O = 0 A, PFM

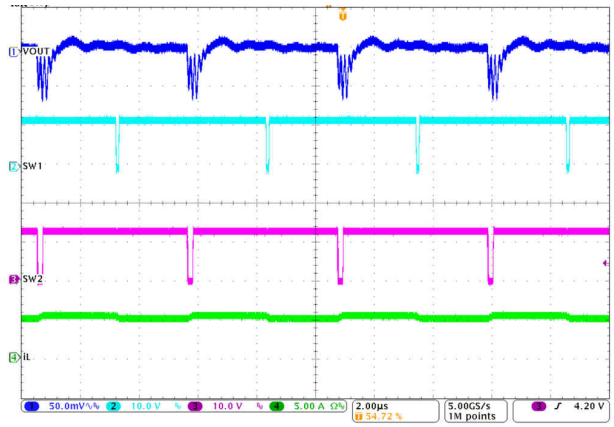

図 8-4. Switching Waveforms in V_{IN} = 12 V, V_{OUT} = 12 V, I_O = 5 A, FPWM

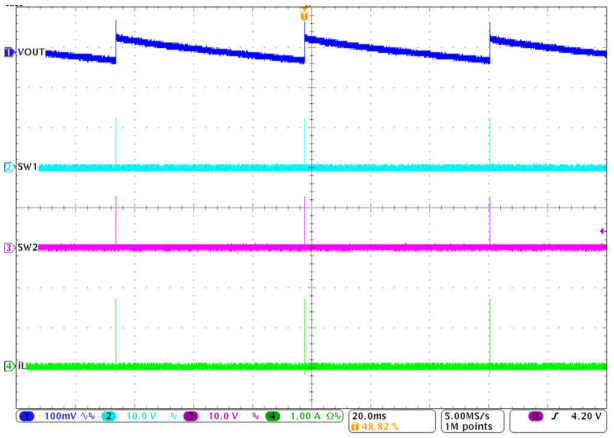

図 8-5. Switching Waveforms in V_{IN} = 12 V, V_{OUT} = 12 V, I_O = 0 A, PFM

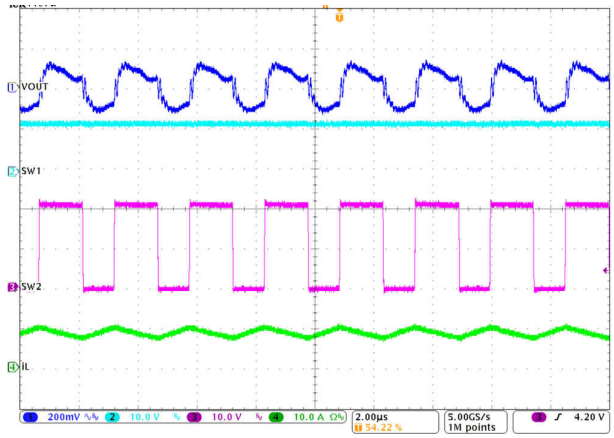

図 8-6. Switching Waveforms in V_{IN} = 12 V, V_{OUT} = 20 V, I_O = 5 A, FPWM

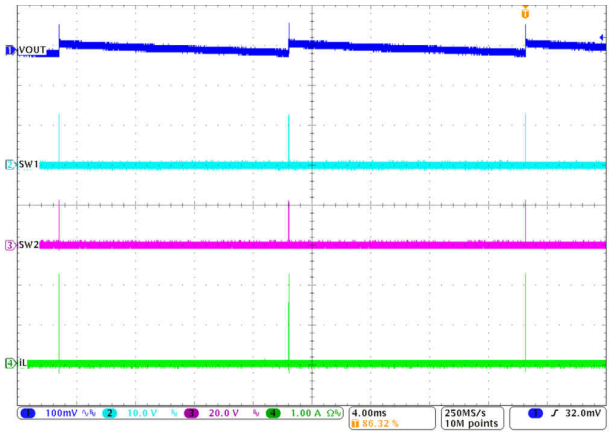

図 8-7. Switching Waveforms in V_{IN} = 12 V, V_{OUT} = 20 V, I_O = 0 A, PFM

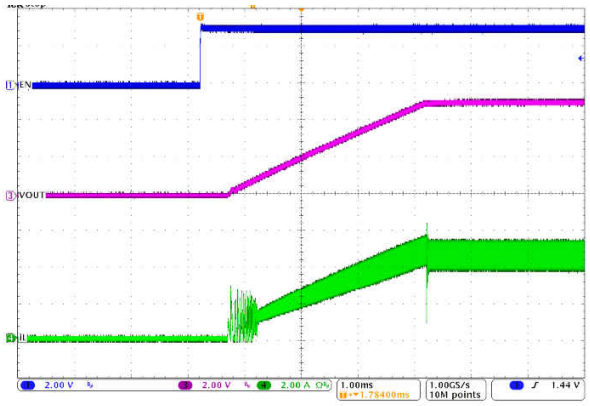

図 8-8. Start-up Waveforms in V_{IN} = 12 V, V_{OUT} = 5 V, I_O = 5 A, FPWM

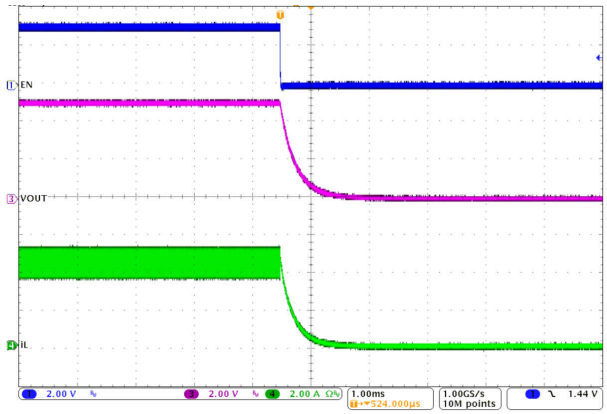

図 8-9. Shutdown Waveforms in V_{IN} = 12 V, V_{OUT} = 5 V, I_O = 5 A, FPWM

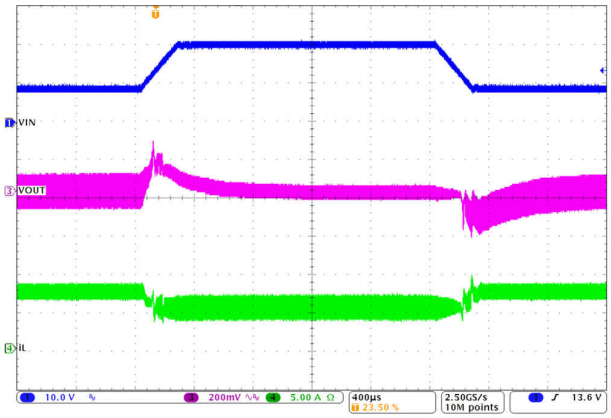

図 8-10. Line Transient Waveforms in V_{IN} = 9 V to 20 V, V_{OUT} = 12 V, I_O = 5 A with 200-µs Slew Rate, FPWM

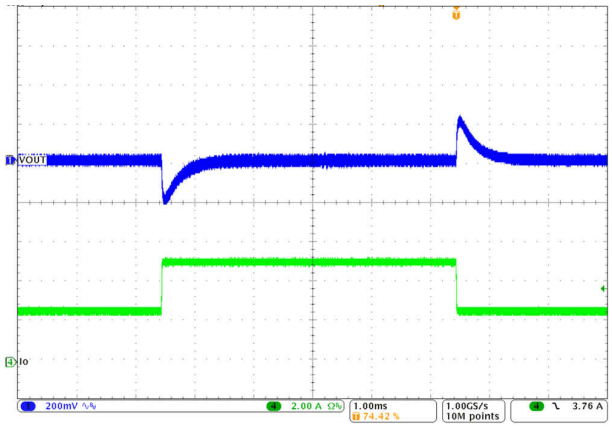

図 8-11. Load Transient Waveforms in V_{IN} = 12 V, V_{OUT} = 5 V, I_O = 2.5 A to 5 A with 20-µs Slew Rate, FPWM

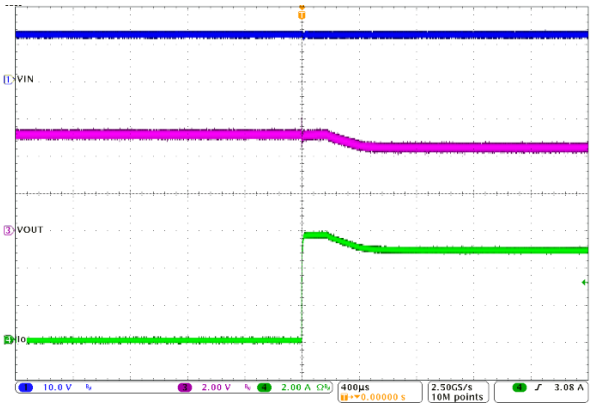

図 8-12. Output Current Limit Waveforms in V_{IN} = 12 V, V_{OUT} = 5 V, R_{LOAD} = 0.9 Ω, R_{SNS} = 10 mΩ, FPWM

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.7 V to 36 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. A typical choice is an aluminum electrolytic capacitor with a value of 100 µF.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If layout is not carefully done, the regulator can suffer from instability and noise problems. To maximize efficiency, switching rise time and fall time are very fast. To prevent radiation of high-frequency noise (for example, EMI), proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW1 and SW2 pins, and always use a ground plane under the switching regulator to minimize interplane coupling. The input capacitor needs to be close to the VIN pin and the PGND to reduce the input supply current ripple.

The most critical current path for buck converter portion is from the switching FET at the buck side, through the rectifier FET at the buck side to the PGND, then the input capacitors, and back to the input of the switching FET. This high current path contains nanosecond rise time and fall time, and should be kept as short as possible. Therefore, the input capacitor for power stage must be close to the input of the switching FET and the PGND terminal of the rectifier FET.

The most critical current path for boost converter portion is from the switching FET at the boost side, through the rectifier FET at boost side, then the output capacitors, and back to ground of the switching FET. This high current path contains nanosecond rise time and fall time, and should be kept as short as possible. Therefore, the output capacitor needs not only to be close to the VOUT pin, but also to the PGND pin to reduce the overshoot at the SW2 pin and the VOUT pin.

The traces from the output current sensing resistor to the ISP pin and the ISN pin must be in parallel and close to each other to avoid noise coupling.

The PGND plane and the AGND plane are connected at the terminal of the capacitor at the VCC pin. Thus the noise caused by the MOSFET driver and parasitic inductance does not interfere with the AGND and internal control circuit.

To get good thermal performance, it is recommended to use thermal vias beneath the TPS552882-Q1 connecting the PGND pin to the PGND plane, and the VOUT pin to a large VOUT area separately.

10.2 Layout Example

trace on bottom layer

AGND plane on an inner layer

The first inner layer is the PGND plane

AGND plane connects to PGND plane at the terminal of the capacitor at the VCC pin

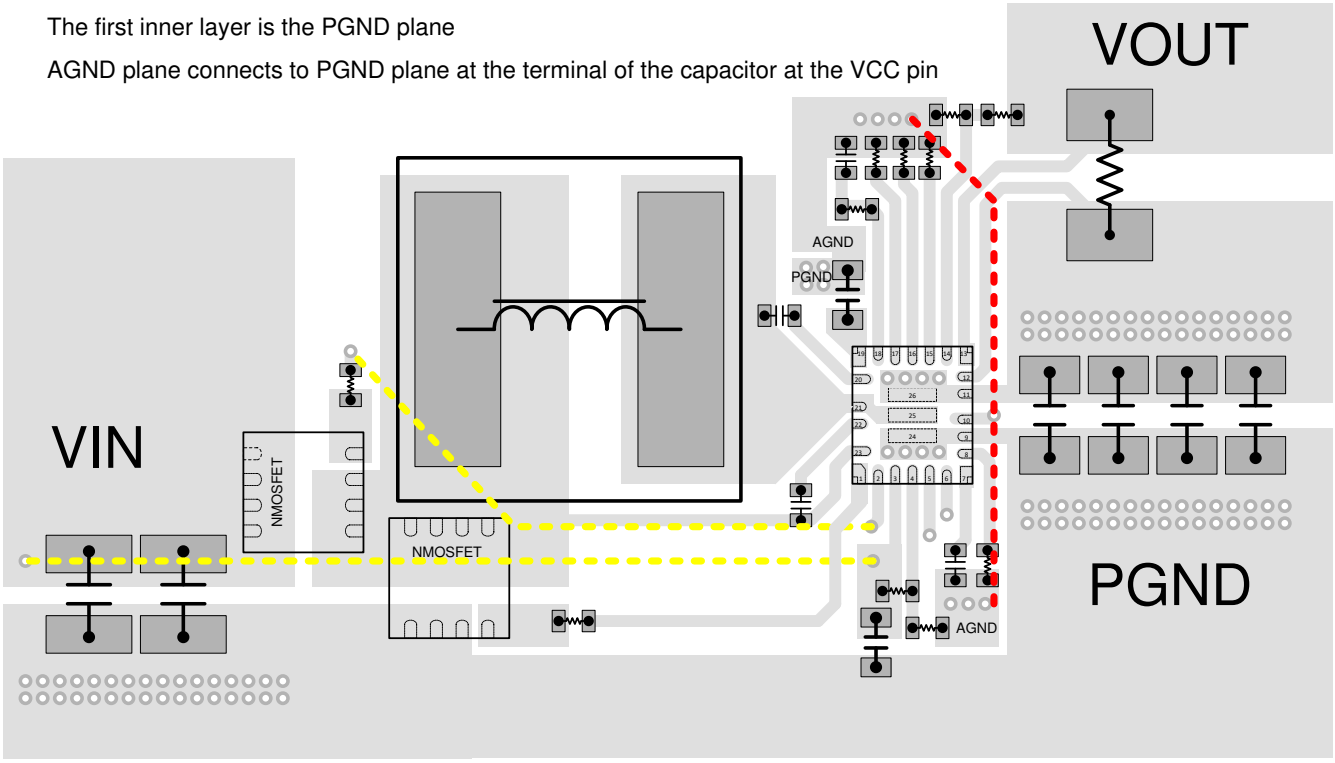

図 10-1. Example Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Development Support

11.1.2.1 Custom Design With WEBENCH® Tools

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1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
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- Print PDF reports for the design, and share the design with colleagues

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS552882QRPMRQ1	ACTIVE	VQFN-HR	RPM	26	3000	RoHS & Green	Call TI | SN	Level-2-260C-1 YEAR	-40 to 150	2882Q	Samples
TPS552882QWRPMRQ1	ACTIVE	VQFN-HR	RPM	26	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	52882W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS552882-Q1 :

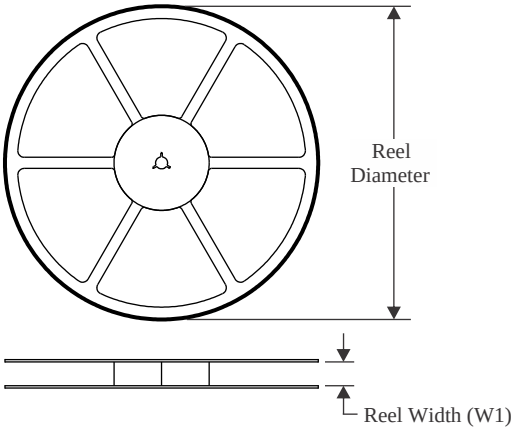
- Catalog : TPS552882

NOTE: Qualified Version Definitions:

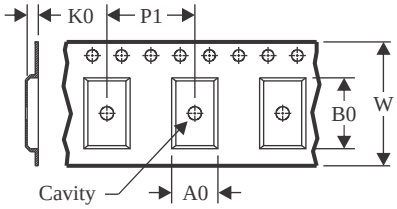
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

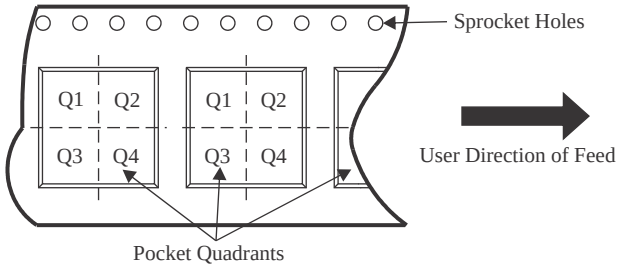


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

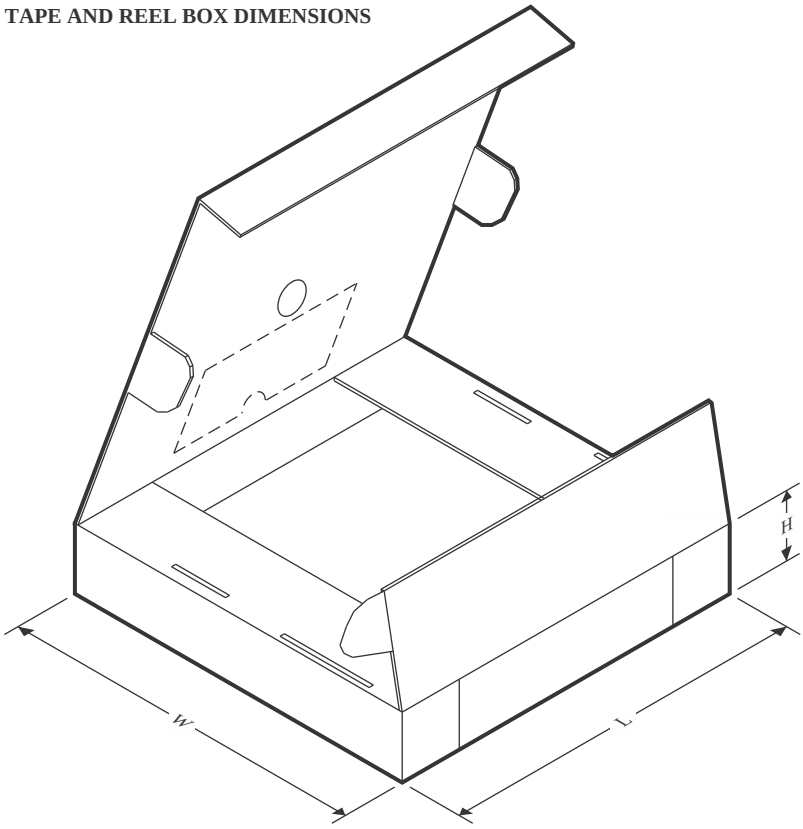
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS552882QRPMRQ1	VQFN-HR	RPM	26	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q2
TPS552882QRPMRQ1	VQFN-HR	RPM	26	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q2
TPS552882QWRPMRQ1	VQFN-HR	RPM	26	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS552882QRPMRQ1	VQFN-HR	RPM	26	3000	367.0	367.0	35.0
TPS552882QRPMRQ1	VQFN-HR	RPM	26	3000	367.0	367.0	35.0
TPS552882QWRPMRQ1	VQFN-HR	RPM	26	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

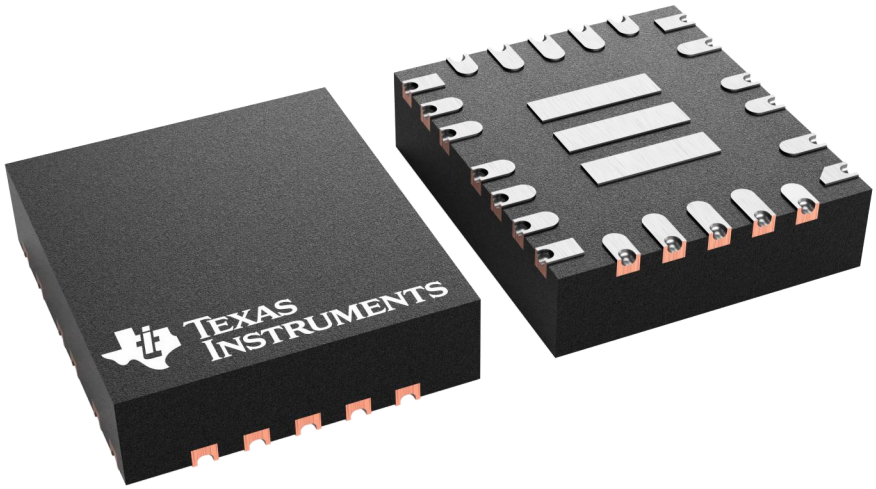
RPM 26

VQFN-HR - 1 mm max height

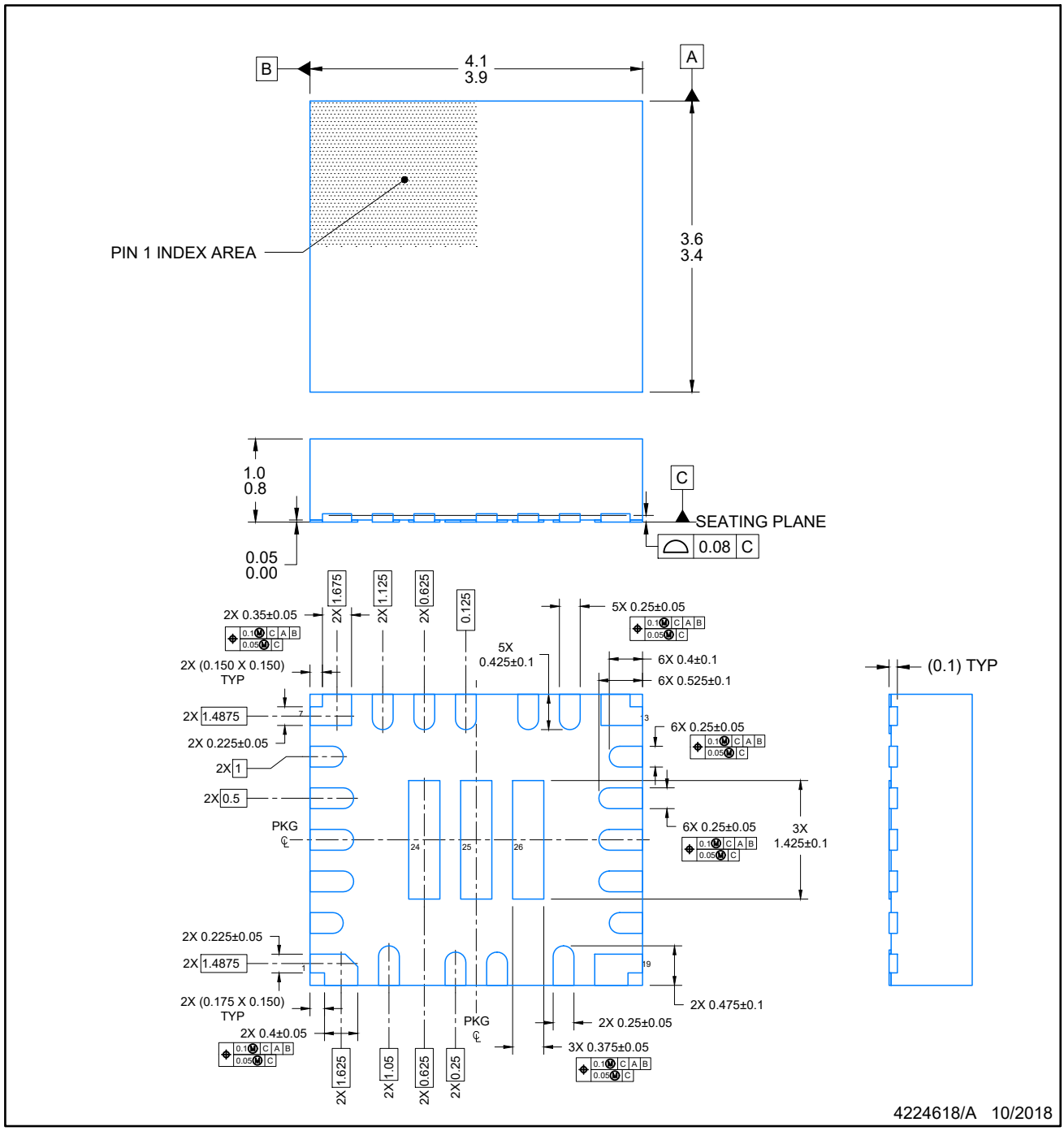
3.5 x 4, 0.5 mm pitch

VERY THIN QUAD FLATPACK-HotRod

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

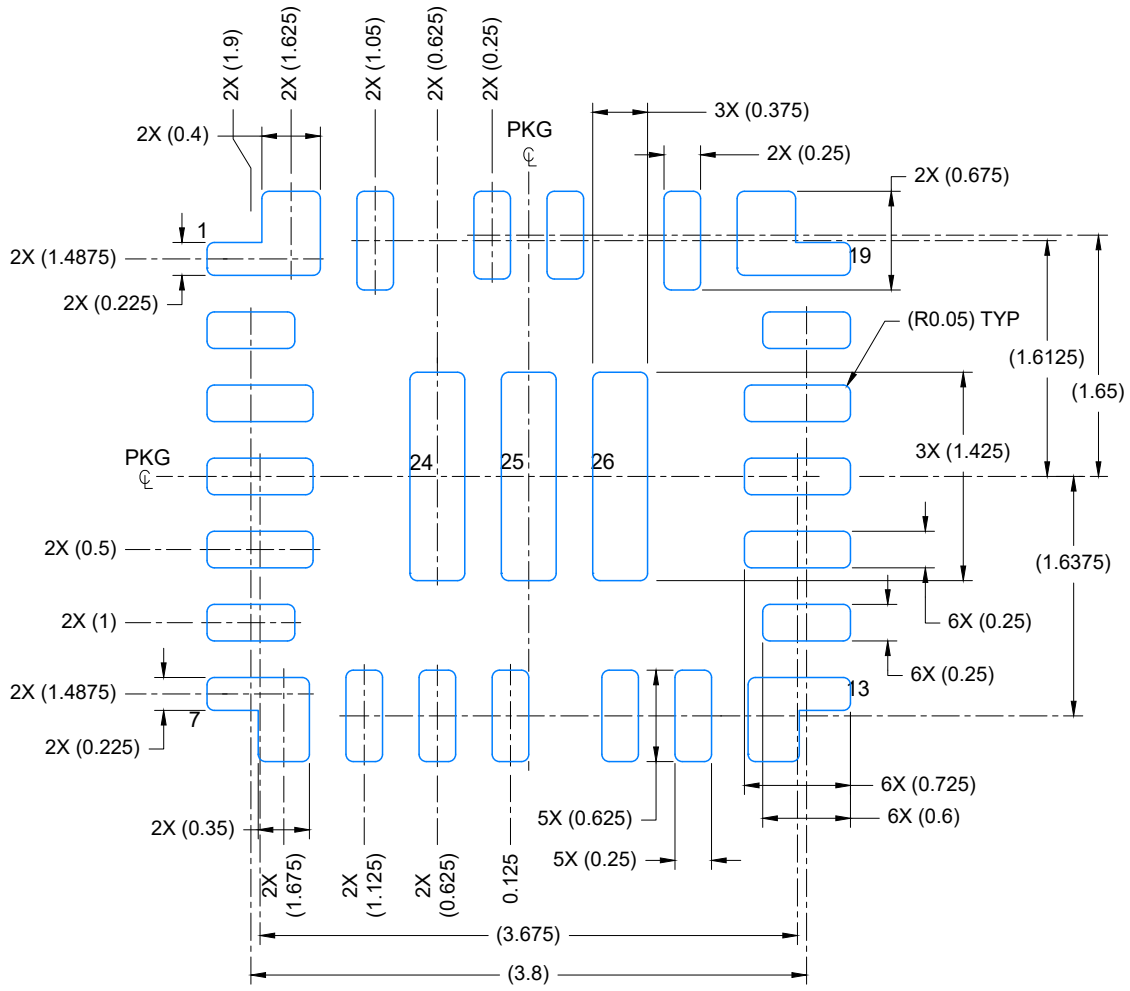


4226451/A

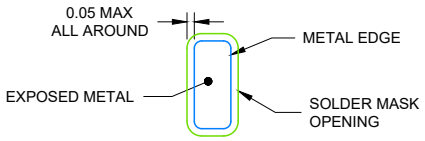


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



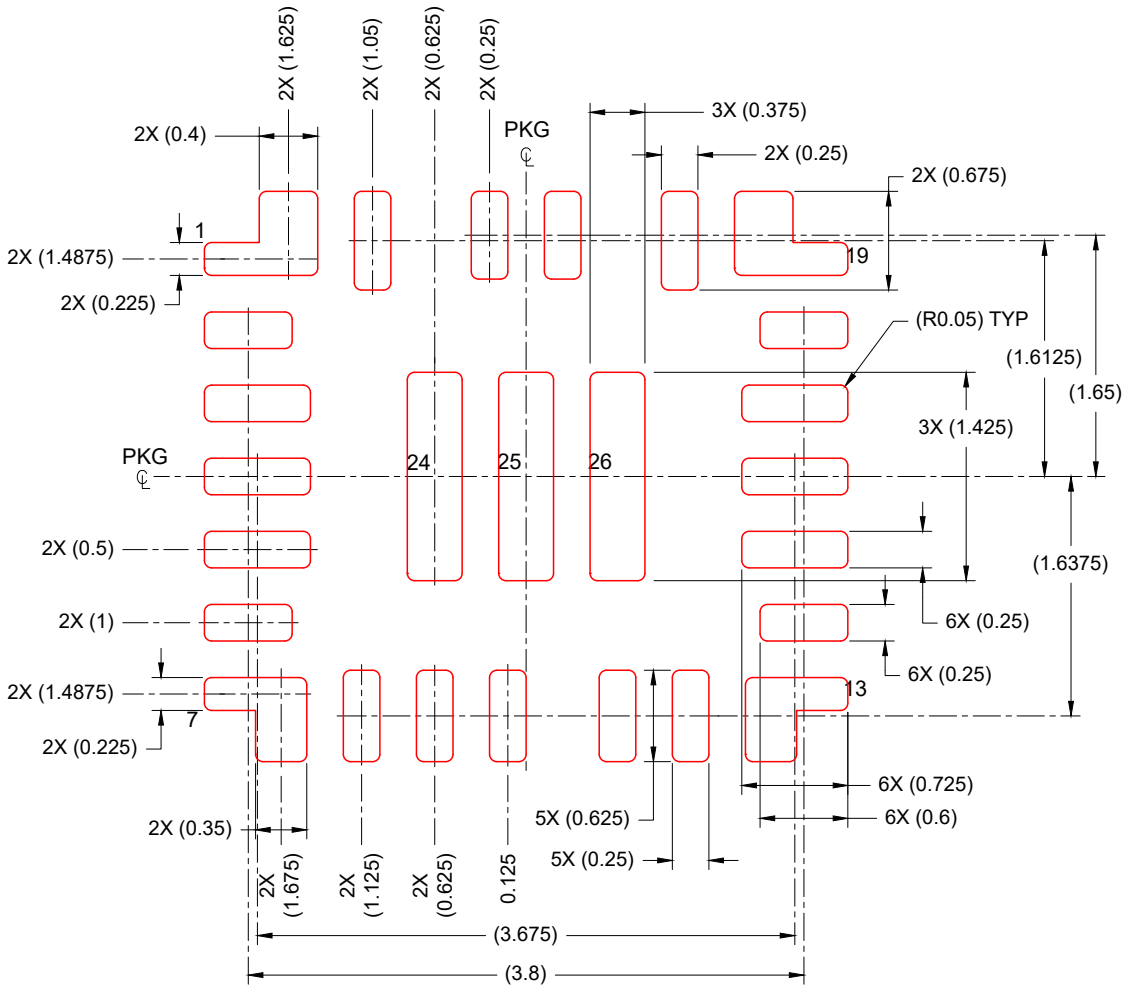
NON SOLDER MASK
DEFINED

SOLDER MASK DETAIL

4224618/A 10/2018

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 20X

4224618/A 10/2018

NOTES: (continued)

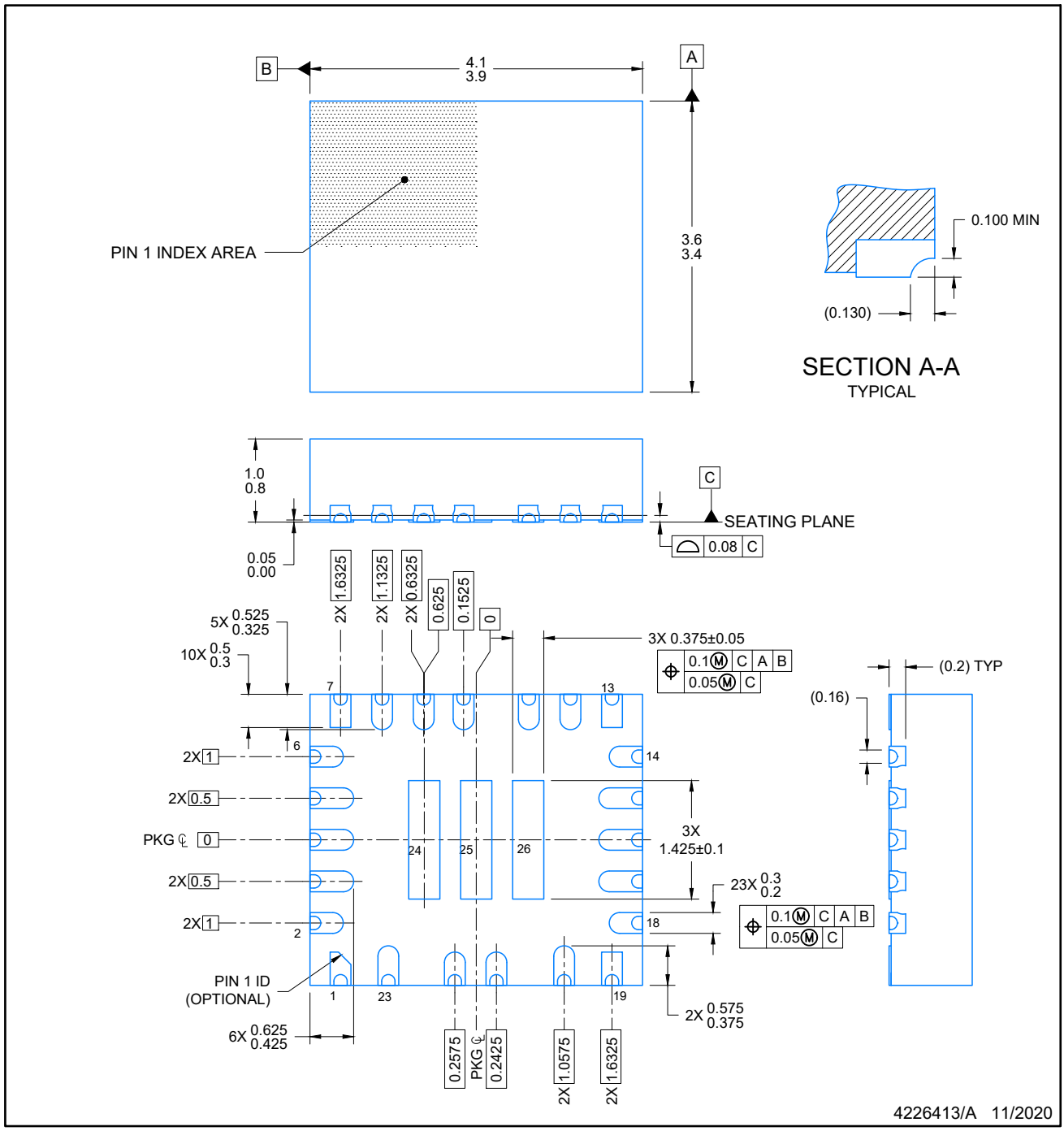
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

RPM0026B

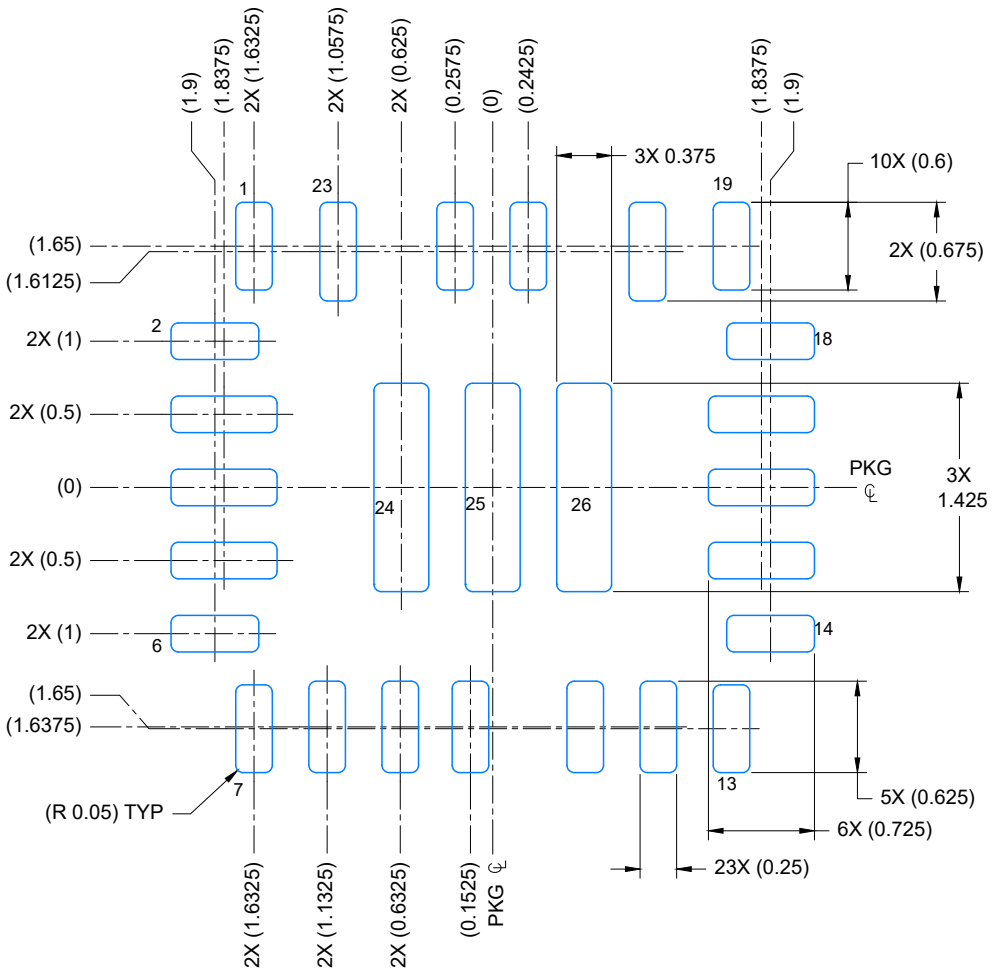
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD

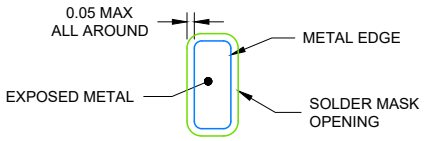


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



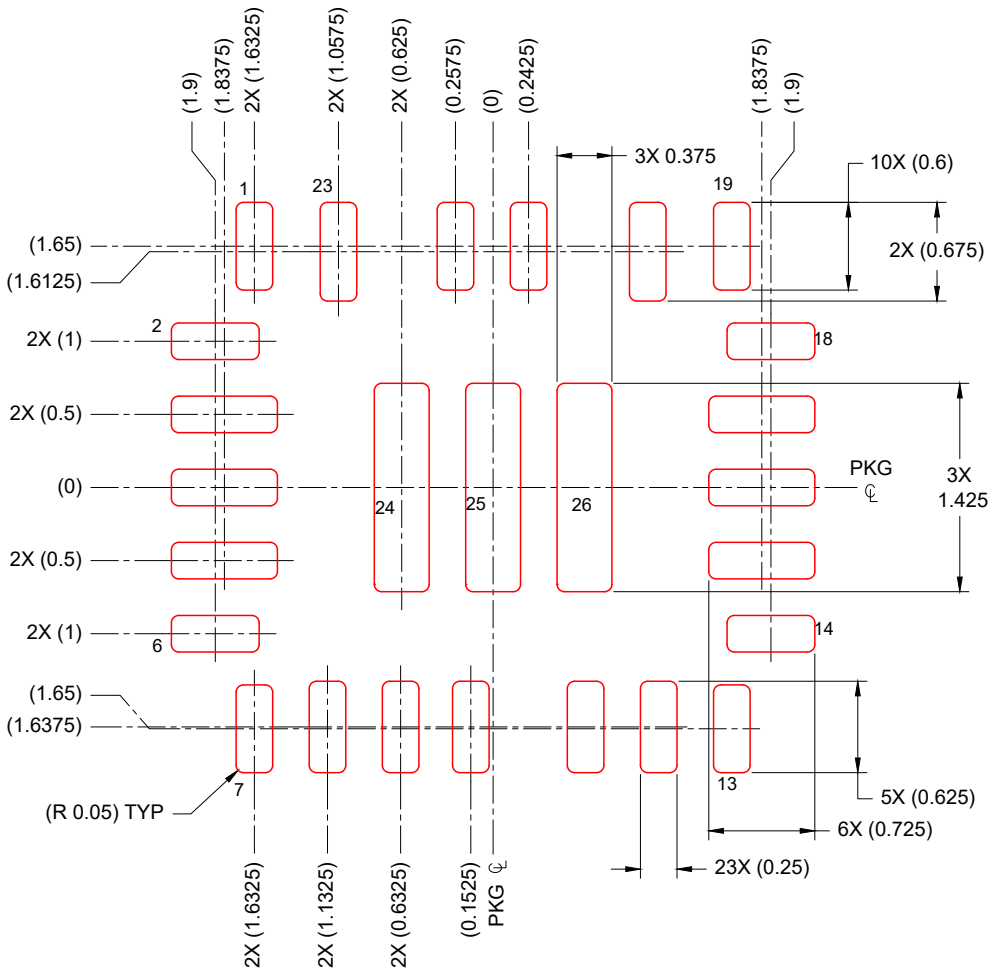
NON SOLDER MASK
DEFINED

SOLDER MASK DETAIL

4226413/A 11/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 20X

4226413/A 11/2020

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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