TEXAS INSTRUMENTS
TPS55289-Q1
JAJSO91 – DECEMBER 2023

TPS55289-Q1 I²C インターフェイス搭載 36V、8A 昇降圧コンバータ

1 特長

- AEC-Q100 認定済み:
  - デバイス温度グレード 1:動作時周囲温度範囲:-40℃～+125℃
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- USB パワー・デリバリ (USB PD)用のプログラマブル電源 (PPS)サポート
  - 幅広い入力電圧範囲:3.0V～36V
  - プログラム可能な出力電圧範囲:0.8V～22V (10mV 刻み)
  - 基準電圧精度:±1%
  - ケーブルの電圧ドループに対する可変出力電圧補償
  - 最大 6.35A の出力電流制限を 50mA 刻みでプログラム可能
  - ±5% 精度の出力電流監視
  - I²C インターフェイス
- 全負荷範囲にわたって高効率を実現
  - V_{IN} = 12V、V_{OUT} = 20V、I_{OUT} = 3A で 96% の効率
  - 軽負荷時の PFM および FPWM モードをプログラム可能
- 周波数干渉とクロストークを回避
  - クロック同期 (オプション)
  - プログラム可能なスイッチング周波数:200kHz～2.2MHz
- EMI 低減
  - プログラム可能なスペクトラム拡散 (オプション)
  - 鉛レス・パッケージ
- 豊富な保護機能
  - 出力過電圧保護
  - ヒカップ・モードによる出力短絡保護
  - サーマル・シャットダウン保護機能
  - 8A の平均インダクタ電流制限
- 小型のソリューション・サイズ
  - 最大 2.2MHz のスイッチング周波数
  - 3.0mm × 5.0mm HotRod™ QFN パッケージ

2 アプリケーション

- 車両充電器
- USB PD
- ワイヤレス充電器
- 車載用インフォテインメントおよびクラスタ
- 車載テール ライト
- 先進運転支援システム (ADAS)

3 概要

TPS55289-Q1 は、バッテリ電圧やアダプタ電圧を複数の電源レール向けに変換するように最適化された同期整流昇降圧コンバータです。TPS55289-Q1 は、4 個の MOSFET スイッチを内蔵しており、USB Power Delivery (USB PD) アプリケーション向けのコンパクトなソリューションを実現します。

TPS55289-Q1 は最大で 36V の入力電圧に対応できます。I²C インターフェイスにより、TPS55289-Q1 の出力電圧は、0.8V～22V の範囲で 10mV 刻みにプログラム可能です。昇圧モードでの動作時には、12V 入力電圧から 60W を供給できます。9V の入力電圧からは 45W を供給できます。

TPS55289-Q1 は平均電流モード制御方式を採用しています。スイッチング周波数は、外付け抵抗により 200kHz～2.2MHz の範囲でプログラム可能であり、外部クロックに同期させることができます。TPS55289-Q1 は、ピーク EMI を最小限に抑えるための拡散スペクトラム オプション機能も備えています。

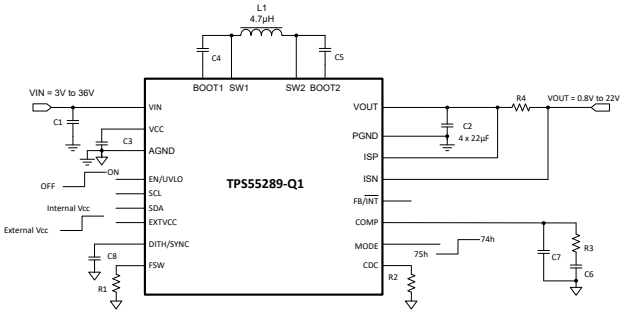
TPS55289-Q1 は出力過電圧保護、平均インダクタ電流制限、サイクルごとのピーク電流制限、出力短絡保護機能を備えています。また TPS55289-Q1 は、持続的な過負荷状態での出力電流制限およびヒカップ モード保護オプション機能により、安全な動作を保証します。

TPS55289-Q1 はスイッチング周波数が高いため、小型のインダクタとコンデンサを使用できます。本デバイスは 3.0mm × 5.0mm の QFN パッケージで供給されます。

製品情報

部品番号	パッケージ(1)	本体サイズ
TPS55289-Q1	VQFN-HR	3.0mm × 5.0mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



代表的なアプリケーション回路

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4 Pin Configuration and Functions

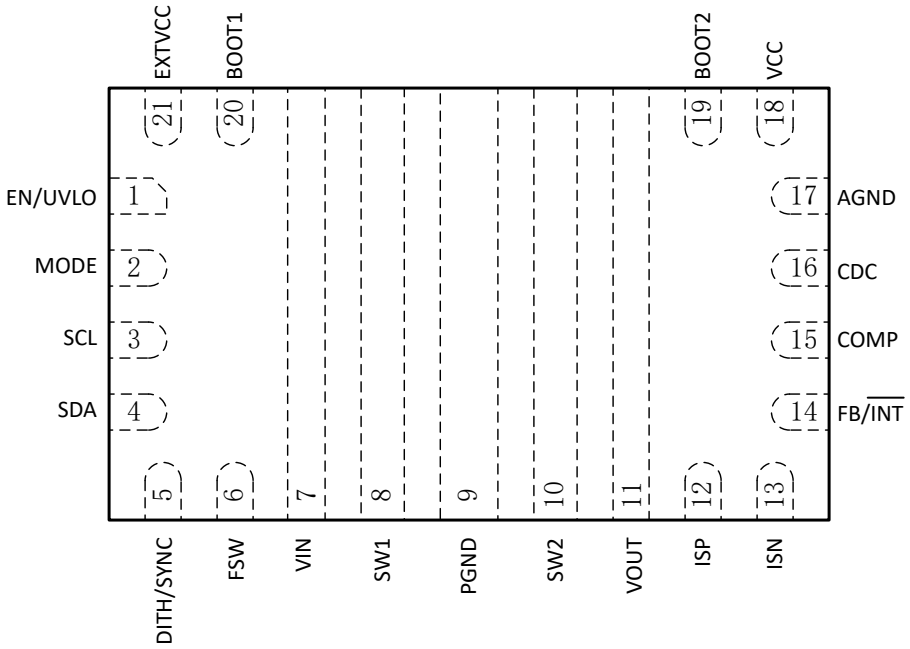


図 4-1. 21-pin VQFN-HR, RYQ Package (Transparent Top View)

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	EN/UVLO	I	Enable logic input and programmable input voltage undervoltage lockout (UVLO) input. Logic high level enables the device. Logic low level disables the device and turns it into shutdown mode. After the voltage at the EN/UVLO pin is above the logic high voltage of 1.15V, this pin acts as programmable UVLO input with 1.23V internal reference.
2	MODE	I	I^2C target address selection. When it is connected to logic high voltage, the I^2C target address is 74H. When it is connected to logic low voltage, I^2C target address is 75H.
3	SCL	I	Clock of I^2C interface.
4	SDA	I/O	Data of I^2C interface.
5	DITH/SYNC	I	Dithering frequency setting and synchronous clock input. Use a capacitor between this pin and ground to set the dithering frequency. When this pin is short to ground or pulled above 1.2V, there is no dithering function. An external clock can be applied at this pin to synchronize the switching frequency.
6	FSW	I	The switching frequency is programmed by a resistor between this pin and the AGND pin.
7	VIN	PWR	Input of the buck-boost conveter.
8	SW1	PWR	The switching node pin of the buck side. It is connected to the drain of the internal buck low-side power MOSFET and the source of internal buck high-side power MOSFET.
9	PGND	PWR	Power ground of the device.
10	SW2	PWR	The switching node pin of the boost side. It is connected to the drain of the internal boost low-side power MOSFET and the source of internal boost high-side power MOSFET.
11	VOUT	PWR	Output of the buck-boost converter.
12	ISP	I	Positive input of the current sense amplifier. An optional current sense resistor connected between the ISP pin and the ISN pin can limit the output current. If the sensed voltage reaches the current limit setting value in the register, a slow constant current control loop becomes active and starts to regulate the voltage between the ISP pin and the ISN pin. Connecting the ISP pin and the ISN pin together with the VOUT pin can disable the output current limit function. It must not be left open.

表 4-1. Pin Functions (続き)

PIN		I/O	DESCRIPTION
NO.	NAME		
13	ISN	I	Negative input of the current sense amplifier. An optional current sense resistor connected between the ISP pin and the ISN pin can limit the output current. If the sensed voltage reaches the current limit setting value in the register, a slow constant current control loop becomes active and starts to regulate the voltage between the ISP pin and the ISN pin. Connecting the ISP pin and the ISN pin together with the VOUT pin can disable the output current limit function. It must not be left open.
14	FB/$\overline{\text{INT}}$	I/O	When the device is set to use external output voltage feedback, connect to the center tap of a resistor divider to program the output voltage. When the device is set to use internal feedback, this pin is a fault indicator open-drain output. When there is an internal fault happening, this pin outputs logic low level.
15	COMP	O	Output of the internal error amplifier. Connect the loop compensation network between this pin and the AGND pin.
16	CDC	O	Voltage output proportional to the sensed voltage between the ISP pin and the ISN pin. Use a resistor between this pin and AGND to increase the output voltage to compensate voltage droop across the cable caused by the cable resistance. This pin can be left open if using internal cable voltage droop compensation.
17	AGND	-	Signal ground of the device.
18	VCC	O	Output of the internal regulator. A ceramic capacitor of more than 4.7µF is required between this pin and the AGND pin.
19	BOOT2	O	Power supply for high-side MOSFET gate driver in boost side. A ceramic capacitor of 0.1µF must be connected between this pin and the SW2 pin.
20	BOOT1	O	Power supply for high-side MOSFET gate driver in buck side. A ceramic capacitor of 0.1µF must be connected between this pin and the SW1 pin.
21	EXTVCC	I	Select the internal LDO or external 5V for VCC. When it is connected to VCC pin, logic high voltage or is left floating, select the internal LDO. When it is connected to logic low voltage, select the external 5V for VCC.

5 Specifications

5.1 Absolute Maximum Ratings

over the recommended operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range at terminals (2)	VIN, SW1	–0.3	42	V
	BOOT1	SW1–0.3	SW1+6	V
	VCC, SCL, SDA, FSW, COMP, FB/$\overline{\text{INT}}$, MODE, CDC, DITH/SYNC, EXTVCC	–0.3	6	V
	VOUT, SW2, ISP, ISN	–0.3	25	V
	EN	-0.3	20	V
	BOOT2	SW2–0.3	SW2+6	V
	SCL, SDA, FSW, COMP, FB/$\overline{\text{INT}}$, MODE, CDC, DITH/SYNC, EXTVCC	–0.3	VCC+0.3	V
T_J	Operating Junction, T_J (3)	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal.
(3) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011, all pins(2)	±500	
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per AEC Q100-011, corner pins(2)	±750	V

(1) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	3.0		36	V
V_{OUT}	Output voltage range	0.8		22	V
L	Effective inductance range	1	4.7	10	µH
C_{IN}	Effective input capacitance range	4.7	22		µF
C_{OUT}	Effective output capacitance range	10	100	1000	µF
T_J	Operating junction temperature(1)	–40		150	°C

(1) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

5.4 Thermal Information

THERMAL METRIC[1]		RYQ (VQFN) 21 PINS Standard	RYQ (VQFN) 21 PINS EVM [2]	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.4	27.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.3	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.4	N/A	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.7	0.7	°C/W
Y_{JB}	Junction-to-board characterization parameter	7.2	11.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Measured on TPS55289Q1EVM-011, 4-layer, 2-oz/1-oz/1-oz/2-oz copper 91-mmx66-mm PCB.

5.5 Electrical Characteristics

T_J = -40°C to 125°C, V_{IN} = 12 V and V_{OUT} = 20 V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		3.0		36	V
V_{VIN_UVLO}	Under voltage lockout threshold	V_{IN} rising	2.8	2.9	3.0	V
		V_{IN} falling	2.6	2.65	2.7	V
I_Q	Quiescent current into VIN pin	IC enabled, no load, no switching. V_{IN} = 3.0V to 24V, V_{OUT} = 0.8V, V_{FB} = V_{REF} + 0.1V, R_{FSW} = 100kΩ		760	860	μA
	Quiescent current into VOUT pin	IC enabled, no load, no switching. V_{IN} = 3.0V, V_{OUT} = 3V to 20V, V_{FB} = V_{REF} + 0.1V, R_{FSW} = 100kΩ		760	860	μA
I_{SD}	Shutdown current into VIN pin	IC disabled, V_{IN} = 3.0V to 14V, T_J up to 125°C, EXTVCC pin floating		0.8	3	μA
V_{CC}	Internal regulator output	I_{VCC} = 50mA, V_{IN} = 8V, V_{OUT} = 20V	5.0	5.2	5.4	V
EN/UVLO						
V_{EN_H}	EN Logic high threshold	V_{CC} = 3.0V to 5.5V			1.15	V
V_{EN_L}	EN Logic low threshold	V_{CC} = 3.0V to 5.5V	0.4			V
V_{EN_HYS}	Enable threshold hysteresis	V_{CC} = 3.0V to 5.5V	0.04			V
V_{UVLO}	UVLO rising threshold at the EN/UVLO pin	V_{CC} = 3.0V to 5.5V	1.20	1.23	1.26	V
V_{UVLO_HYS}	UVLO threshold hysteresis	V_{CC} = 3.0V to 5.5V		10		mV
I_{UVLO}	Sourcing current at the EN/UVLO pin	$V_{EN/UVLO}$ = 1.3V	4.4	5	5.6	μA
OUTPUT						
V_{OUT}	Output voltage range		0.8		22	V
V_{OVP}	Output overvoltage protection threshold		22.5	23.5	24.5	V
V_{OVP_HYS}	Overvoltage protection hysteresis			1		V
I_{FB_LKG}	Leakage current at FB pin	T_J up to 125°C			100	nA
I_{VOUT_LKG}	Leakage current into VOUT pin	IC disabled, V_{OUT} = 20V, V_{SW2} = 0V, T_J up to 125°C		1	20	μA
I_{DISCHG}	Output discharge current	V_{OUT} = 20V, V_{CC} = 5.2V	40	100	170	mA
INTERNAL REFERENCE DAC						

T_J = -40°C to 125°C, V_{IN} = 12 V and V_{OUT} = 20 V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT_FULL}	Output voltage when V_{REF} is set to 1.129V	VOUT_FS = 03h, REF = 0780h, V_{REF} = 1.129V	19.7	20	20.3	V
		VOUT_FS = 02h, REF = 0780h, V_{REF} = 1.129V	14.78	15	15.22	V
		VOUT_FS = 01h, REF = 0780h, V_{REF} = 1.129V	9.85	10	10.15	V
		VOUT_FS = 00h, REF = 0780h, V_{REF} = 1.129V	4.93	5	5.07	V
V_{OUT_ZERO}	Output voltage when V_{REF} is set to 45mV	VOUT_FS = 03h, REF = 0000h, V_{REF} = 45mV	0.74	0.8	0.86	V
		VOUT_FS = 02h, REF = 0000h, V_{REF} = 45mV	0.55	0.6	0.65	V
		VOUT_FS = 01h, REF = 0000h, V_{REF} = 45mV	0.36	0.4	0.44	V
		VOUT_FS = 00h, REF = 0000h, V_{REF} = 45mV	0.18	0.2	0.22	V
REFERENCE VOLTAGE						
V_{REF}	Reference voltage at the FB/$\overline{INT}$ pin when using external feedback	External feedback with REF = 0780h	1.117	1.129	1.141	V
		External feedback with REF = 058Ch	0.837	0.846	0.855	V
		External feedback with REF = 0334h	0.502	0.508	0.514	V
		External feedback with REF = 01A4h	0.276	0.282	0.288	V
POWER SWITCH						
$R_{DS(on)}$	Low-side MOSFET on resistance at buck side	V_{OUT} = 20V, V_{CC} = 5.2V		22		mΩ
	High-side MOSFET on resistance at buck side	V_{OUT} = 20V, V_{CC} = 5.2V		14		mΩ
	Low-side MOSFET on resistance at boost side	V_{OUT} = 20V, V_{CC} = 5.2V		11		mΩ
	High-side MOSFET on resistance at boost side	V_{OUT} = 20V, V_{CC} = 5.2V		11		mΩ
INTERNAL CLOCK						
f_{SW}	Switching frequency	R_{FSW} = 100k	180	200	220	kHz
		R_{FSW} = 8.4k	2000	2200	2400	kHz
t_{OFF_min}	Minimum off time	Boost mode		90	145	ns
t_{ON_min}	Minimum on time	Buck mode		90	130	ns
V_{SW}	Voltage at the FSW pin			1		V
CURRENT LIMIT						
I_{LIM_AVG}	Average inductor current limit	V_{IN} = 8V, V_{OUT} = 20V, F_{SW} = 400kHz	7	8	9	A
$I_{LIM\_PK\_H}$	Peak inductor current limit at boost high side	V_{IN} = 8V, V_{OUT} = 20V, F_{SW} = 400kHz		13		A
$I_{LIM\_PK\_L}$	Peak inductor current limit at boost low side	V_{IN} = 8V, V_{OUT} = 20V, F_{SW} = 400kHz		12		A
V_{SNS}	Current loop regulation voltage between ISP and ISN pin	V_{ISN} = 2V to 21V, IOUT_LIMIT Register = 10111100b	28.5	30	31.5	mV
		V_{ISN} = 2V to 21V, IOUT_LIMIT Register = 11100100b	48	50	52	mV
CABLE VOLTAGE DROOP COMPENSATION						

T_J = -40°C to 125°C, V_{IN} = 12 V and V_{OUT} = 20 V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CDC}	Voltage at the CDC pin	R_{CDC} = 20kΩ or floating, V_{ISP} – V_{ISN} = 50mV	0.95	1	1.05	V
		R_{CDC} = 20kΩ or floating, V_{ISP} – V_{ISN} = 2mV		40	75	mV
V_{OUT_CDC}	VOUT increase for cable droop compensation	Internal output feedback, CDC[2:0] = 111, V_{ISP} – V_{ISN} = 50mV	640	700	750	mV
		Internal output feedback, CDC[2:0] = 111, V_{ISP} – V_{ISN} = 2mV		30	60	mV
		Internal output feedback, CDC[2:0] = 001, V_{ISP} – V_{ISN} = 50mV	70	100	130	mV
		Internal output feedback, CDC[2:0] = 001, V_{ISP} – V_{ISN} = 10mV		20	40	mV
I_{FB_CDC}	FB/$\overline{INT}$ pin sinking current	External output feedback, R_{CDC} = 20kΩ, V_{ISP} – V_{ISN} = 50mV	7.23	7.5	7.87	µA
		External output feedback, R_{CDC} = 20kΩ, V_{ISP} – V_{ISN} = 0mV		0	0.3	µA
		External output feedback, R_{CDC} = floating, V_{ISP} – V_{ISN} = 50mV		0	0.3	µA
ERROR AMPLIFIER						
I_{SINK}	COMP pin sink current	V_{FB} = V_{REF} + 400mV, V_{COMP} = 1.5V, V_{CC}=5V		20		µA
I_{SOURCE}	COMP pin source current	V_{FB} = V_{REF} - 400mV, V_{COMP} = 1.5V, V_{CC}=5V		60		µA
V_{CCLPH}	High clamp voltage at the COMP pin	FPWM mode, VOUT = 1.8V to 22V		1.3		V
V_{CCLPL}	Low clamp voltage at the COMP pin	FPWM mode, VOUT = 1.8V to 22V		0.7		V
G_{EA}	Error amplifier transconductance			190		µA/V
SOFT START						
t_{SS}	Soft-start time		2.5	3.6	5	ms
SPREAD SPECTRUM						
I_{DITH_CHG}	Dithering charge current	$V_{DITH/SYNC}$ = 1.0V, R_{FSW} = 49.9kΩ, voltage rising from 0.9V		2		µA
I_{DITH_DIS}	Dithering discharge current	$V_{DITH/SYNC}$ = 1.0V, R_{FSW} = 49.9kΩ, voltage falling from 1.1V		2		µA
V_{DITH_H}	Dithering high threshold			1.07		V
V_{DITH_L}	Dithering low threshold			0.93		V
SYNCHRONOUS CLOCK						
V_{SNYC_H}	Sync clock high voltage threshold				1.2	V
V_{SYNC_L}	Sync clock low voltage threshold		0.4			V
t_{SYNC_MIN}	Minimum sync clock pulse width		50			ns
HICCUP						
t_{HICCUP}	Hiccup off time			76		ms
MODE						
V_{MODE}	MODE logic high threshold	V_{CC} = 3.0V to 5.5V			1.2	V
V_{MODE}	MODE logic low threshold	V_{CC} = 3.0V to 5.5V	0.4			V
EXTVCC						
V_{EXTVCC}	EXTVCC Logic high threshold	V_{CC} = 3.0V to 5.5V			1.2	V
V_{EXTVCC}	EXTVCC Logic Low threshold	V_{CC} = 3.0V to 5.5V	0.4			V
LOGIC INTERFACE						
V_{I2C_IO}	IO voltage range for I^2C		1.7		5.5	V

T_J = -40°C to 125°C, V_{IN} = 12 V and V_{OUT} = 20 V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{I2C_H}	I^2C input high threshold	V_{CC} = 3.0V to 5.5V			1.2	V
V_{I2C_L}	I^2C input low threshold	V_{CC} = 3.0V to 5.5V	0.4			V
$I_{FB/\overline{INT}\_H}$	Leakage current into FB/$\overline{INT}$ pin when outputting high impedance	$V_{FB/\overline{INT}}$ = 5V			100	nA
$V_{FB/\overline{INT}\_L}$	Output low voltage range of the FB/$\overline{INT}$ pin	Sinking 4mA current		0.03	0.1	V
PROTECTION						
T_{SD}	Thermal shutdown threshold	T_J rising		175		°C
T_{SD_HYS}	Thermal shutdown hysteresis	T_J falling below Tsd		20		°C

5.6 I^2C Timing Characteristics

T_J = -40°C to 125°C, V_{IN} = 12 V and V_{OUT} = 20 V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I^2C TIMING						
f_{SCL}	SCL clock frequency		100		1000	kHz
t_{BUF}	Bus free time between a STOP and START condition	Fast mode plus	0.5			µs
$t_{HD(STA)}$	Hold time (repeated) START condition		260			ns
t_{LOW}	Low period of the SCL clock		0.5			µs
t_{HIGH}	High period of the SCL clock		260			ns
$t_{SU(STA)}$	Setup time for a repeated START condition		260			ns
$t_{SU(DAT)}$	Data setup time		50			ns
$t_{HD(DAT)}$	Data hold time		0			µs
t_{RCL}	Rise time of SCL signal				120	ns
t_{RCL1}	Rise time of SCL signal after a repeated START condition and after an ACK bit				120	ns
t_{FCL}	Fall time of SCL signal				120	ns
t_{RDA}	Rise time of SDA signal				120	ns
t_{FDA}	Fall time of SDA signal				120	ns
$t_{SU(STO)}$	Setup time of STOP condition		260			ns
C_B	Capacitive load for SDA and SCL				200	pF

5.7 Typical Characteristics

V_{IN} = 12V, T_A = 25°C, f_{SW} = 400kHz, unless otherwise noted.

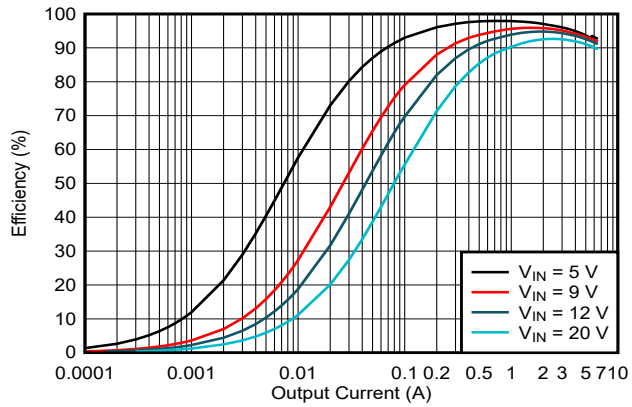


図 5-1. Efficiency vs Output Current, V_{OUT} = 5V, FPWM

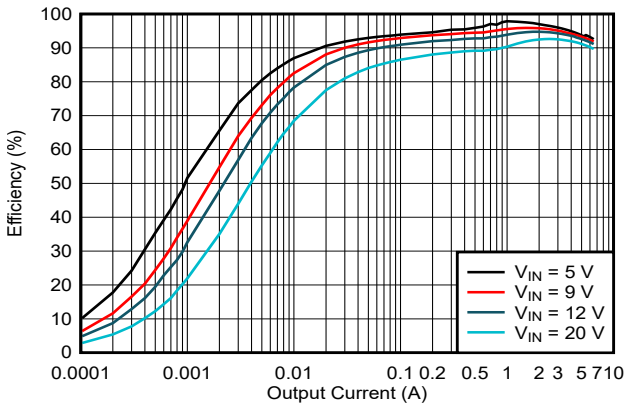


図 5-2. Efficiency vs Output Current, V_{OUT} = 5V, PFM

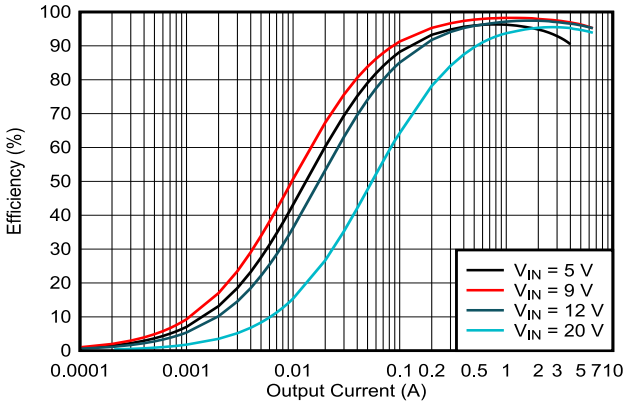


図 5-3. Efficiency vs Output Current, V_{OUT} = 9V, FPWM

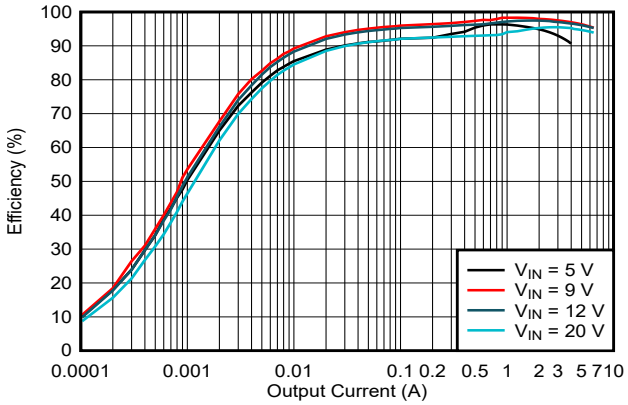


図 5-4. Efficiency vs Output Current, V_{OUT} = 9V, PFM

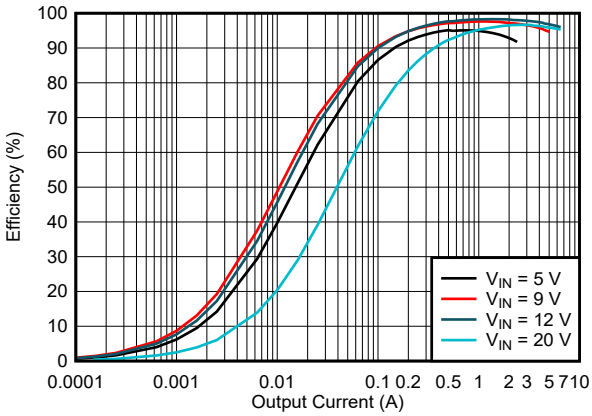


図 5-5. Efficiency vs Output Current, V_{OUT} = 12V, FPWM

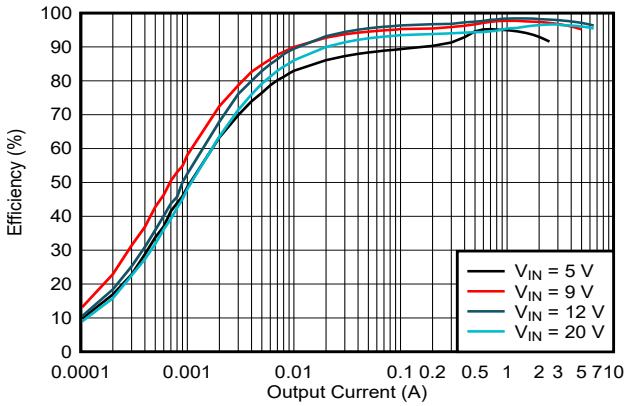


図 5-6. Efficiency vs Output Current, V_{OUT} = 12V, PFM

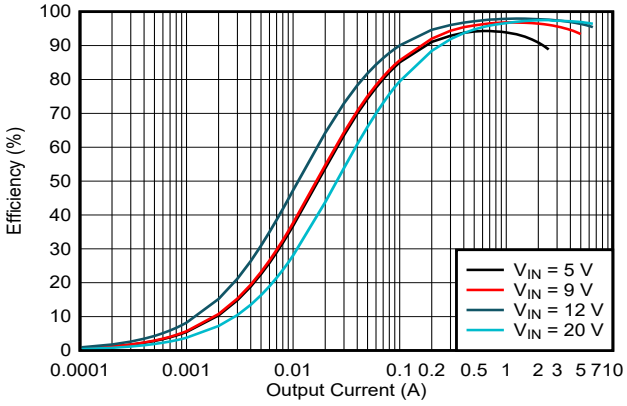


図 5-7. Efficiency vs Output Current, V_{OUT} = 15V, FPWM

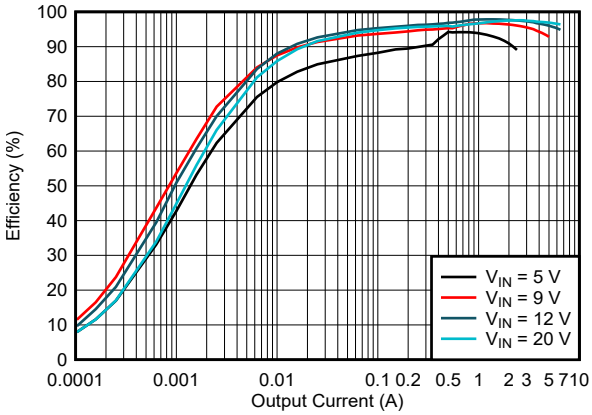


図 5-8. Efficiency vs Output Current, V_{OUT} = 15V, PFM

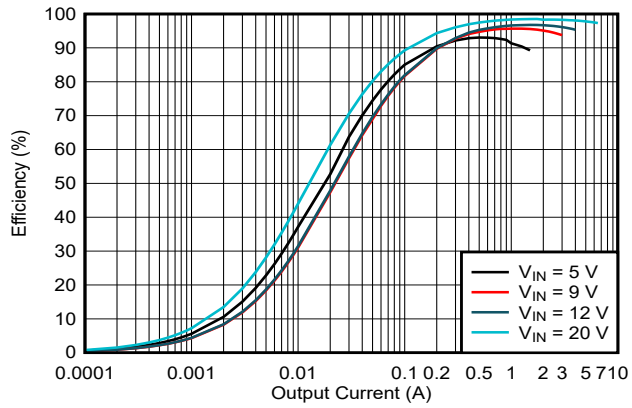


図 5-9. Efficiency vs Output Current, V_{OUT} = 20V, FPWM

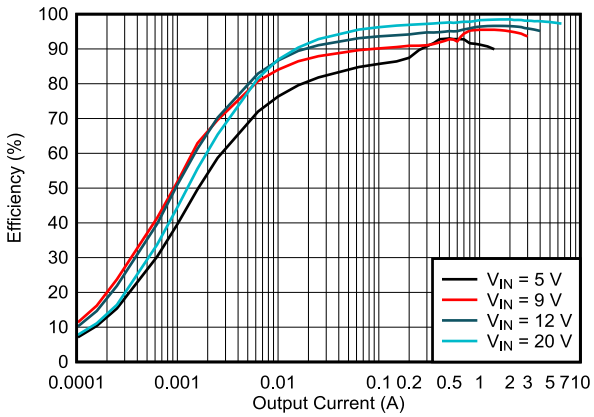


図 5-10. Efficiency vs Output Current, V_{OUT} = 20V, PFM

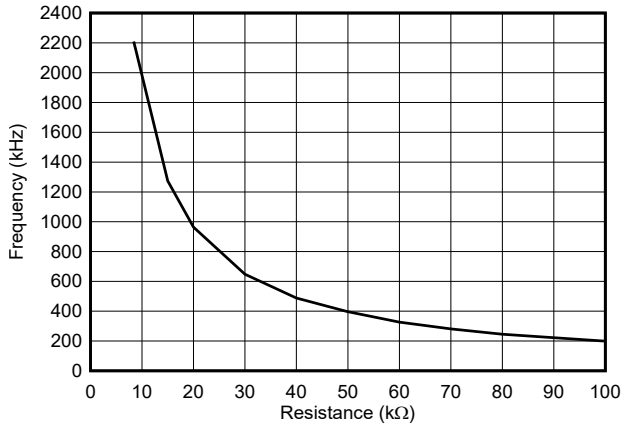


図 5-11. Switching Frequency vs Setting Resistance

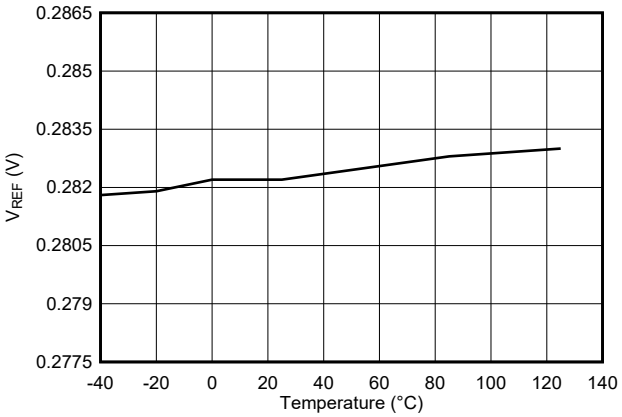


図 5-12. Reference Voltage vs Temperature (V_{REF} = 0.282V)

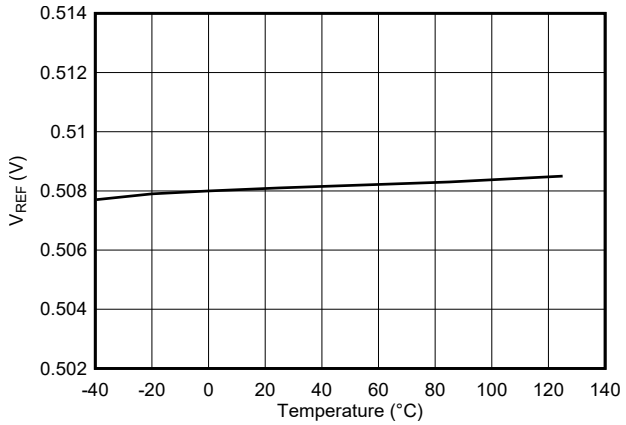


図 5-13. Reference Voltage vs Temperature (V_{REF} = 0.508V)

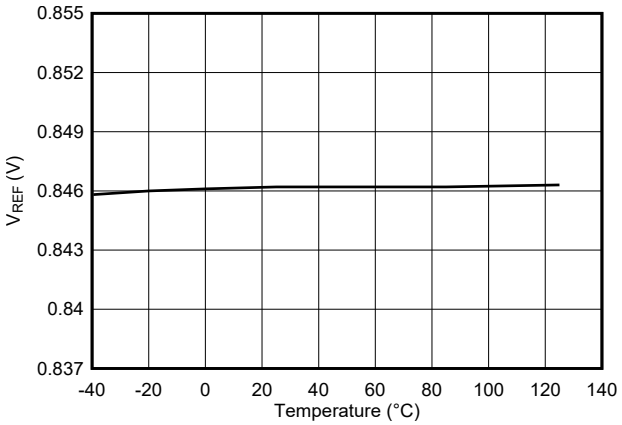


図 5-14. Reference Voltage vs Temperature (V_{REF} = 0.846V)

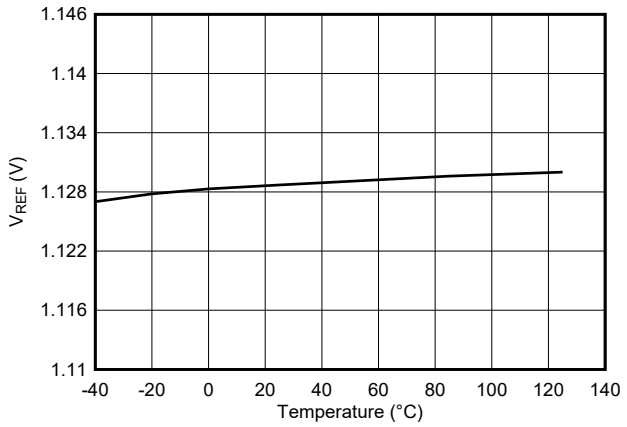


図 5-15. Reference Voltage vs Temperature (V_{REF} = 1.129V)

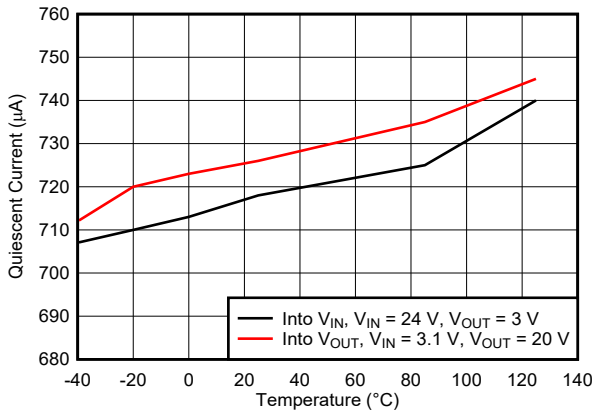


図 5-16. Quiescent Current vs Temperature

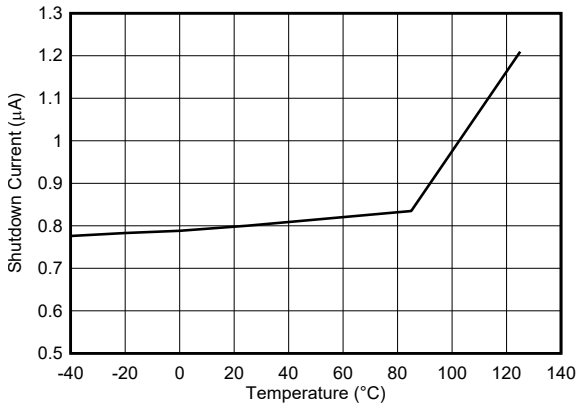


図 5-17. Shutdown Current vs Temperature

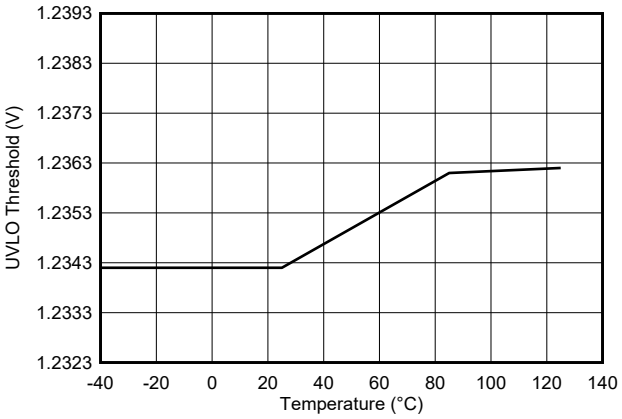


図 5-18. ENABLE/UVLO Rising Threshold vs Temperature

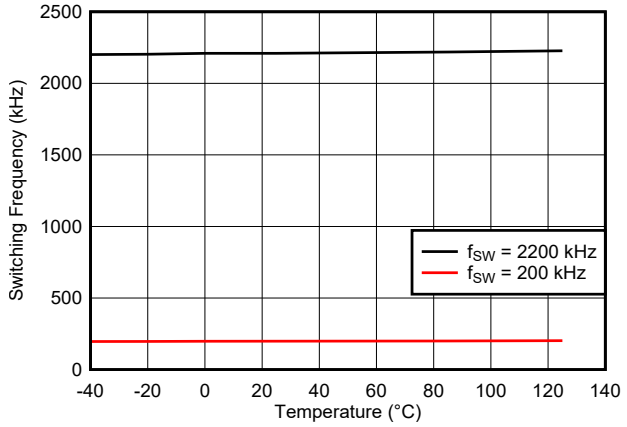


図 5-19. Switching Frequency vs Temperature

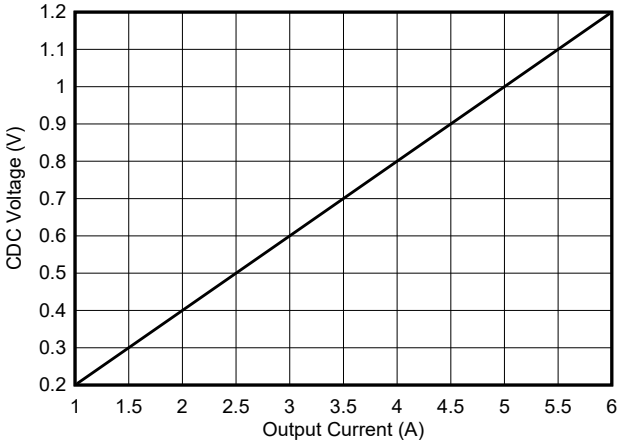


図 5-20. CDC Voltage vs Output Current with R_{SENSE} = 10mΩ

6 Detailed Description

6.1 Overview

The TPS55289-Q1 is an 8A buck-boost DC-to-DC converter with the four MOSFETs integrated. The TPS55289-Q1 can operate over a wide range of 3.0V to 36V input voltage and 0.8V to 22V output voltage. It can transition among buck mode, buck-boost mode and boost mode smoothly according to the input voltage and the set output voltage. The TPS55289-Q1 operates in buck mode when the input voltage is greater than the output voltage and in boost mode when the input voltage is less than the output voltage. When the input voltage is close to the output voltage, the TPS55289-Q1 operates in one-cycle buck and one-cycle boost mode alternately.

The TPS55289-Q1 uses an average current mode control scheme. Current mode control provides simplified loop compensation, rapid response to the load transients, and inherent line voltage rejection. An error amplifier compares the feedback voltage with the internal reference voltage. The output of the error amplifier determines the average inductor current.

An internal oscillator can be configured to operate over a wide range of switching frequency from 200kHz to 2.2MHz. The internal oscillator can also synchronize to an external clock applied to the DITH/SYNC pin. To minimize EMI, the TPS55289-Q1 can dither the switching frequency at ±7% of the set frequency.

The TPS55289-Q1 works in fixed-frequency PWM mode at moderate to heavy load currents. In light load condition, the TPS55289-Q1 can be configured to automatically transition to PFM mode or be forced in PWM mode by setting the corresponding bit in an internal register.

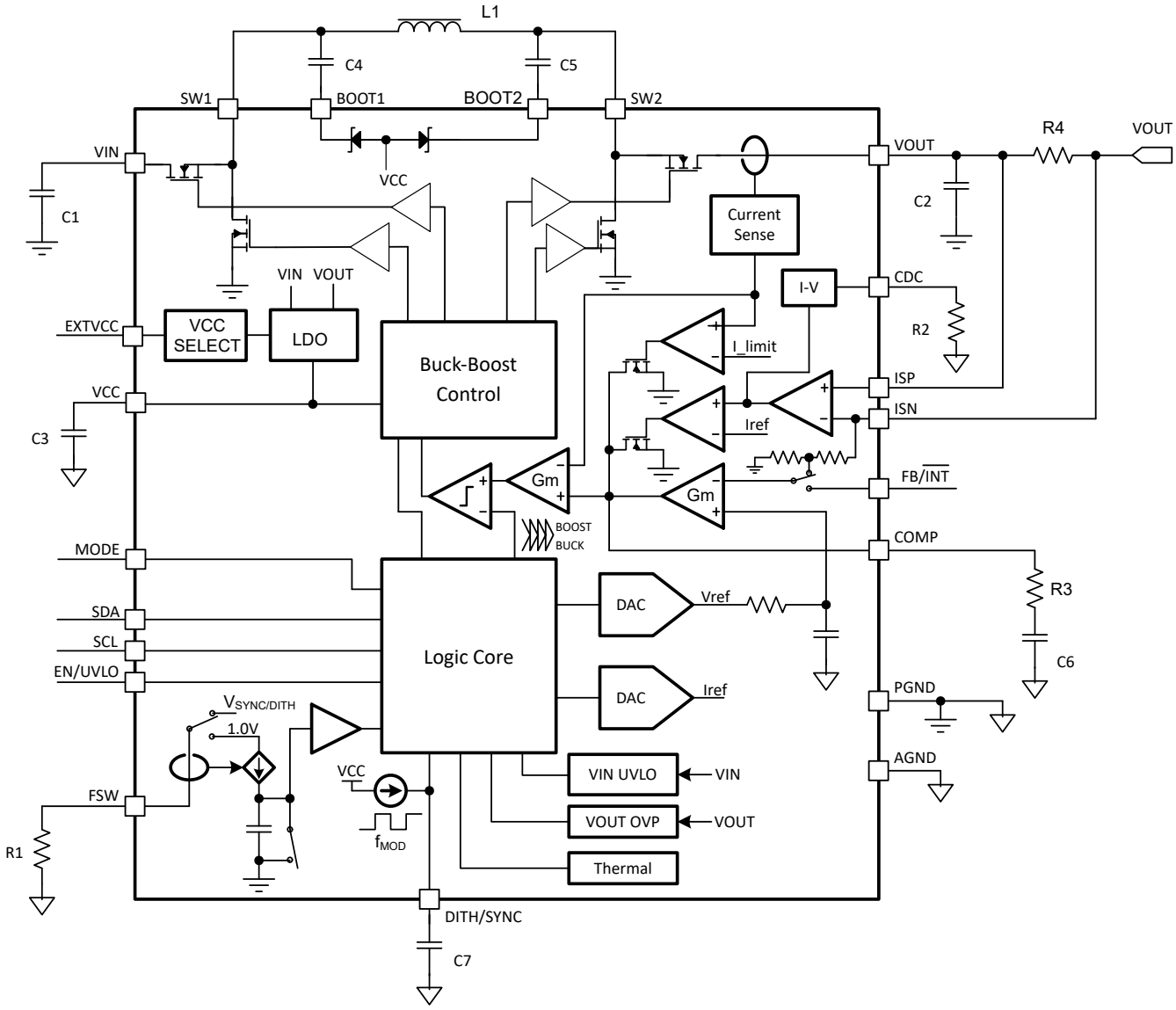
The output voltage of the TPS55289-Q1 is adjustable by setting the internal register through I^2C interface. An internal 11-bit DAC adjusts the reference voltage related to the value written into the REF register. The device can also limit the output current by placing a current sense resistor in the output path. These two functions support the programmable power supply (PPS) feature of the USB PD.

The TPS55289-Q1 provides average inductor current limit of 8A typically. In addition, it provides cycle-by-cycle peak inductor current limit during transient to protect the device against overcurrent condition beyond the capability of the device.

A precision voltage threshold of 1.23V with 5μA sourcing current at the EN/UVLO pin supports programmable input undervoltage lockout (UVLO) with hysteresis. The output overvoltage protection (OVP) feature turns off the high-side FETs to prevent damage to the devices powered by the TPS55289-Q1.

The device provides hiccup mode option to reduce the heating in the power components when output short circuit happens. When the hiccup mode is enabled, the TPS55289-Q1 turns off for 76ms and restarts at soft start-up.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 VCC Power Supply

An internal LDO to supply the TPS55289-Q1 outputs regulated 5.2V voltage at the VCC pin. When V_{IN} is less than V_{OUT}, the internal LDO selects the power supply source by comparing V_{IN} to a rising threshold of 6.2V with 0.3V hysteresis. When V_{IN} is higher than 6.2V, the supply for LDO is V_{IN}. When V_{IN} is lower than 5.9V, the supply for LDO is V_{OUT}. When V_{OUT} is less than V_{IN}, the internal LDO selects the power supply source by comparing V_{OUT} to a rising threshold of 6.2V with 0.3V hysteresis. When V_{OUT} is higher than 6.2V, the supply for LDO is V_{OUT}. When V_{OUT} is lower than 5.9V, the supply for LDO is V_{IN}. 表 6-1 shows the supply source selection for the internal LDO.

表 6-1. V_{CC} Power Supply Logic

V_{IN}	V_{OUT}	INPUT for V_{CC} LDO
V_{IN} > 6.2V	V_{OUT} > V_{IN}	V_{IN}
V_{IN} < 5.9V	V_{OUT} > V_{IN}	V_{OUT}
V_{IN} > V_{OUT}	V_{OUT} > 6.2V	V_{OUT}
V_{IN} > V_{OUT}	V_{OUT} < 5.9V	V_{IN}

6.3.2 EXTVCC Power Supply

To minimize the power dissipation of the internal LDO when both input voltage and output voltage are high, an external 5V power source can be applied at the VCC pin to supply the TPS55289-Q1. The external 5V power supply must have at least 100mA output current capability and must be within the 4.75V to 5.5V regulation range. When the EXTVCC pin is connected to logic low, the device selects the external power supply to supply the device through VCC pin. When the EXTVCC pin is connected to VCC pin, logic high or is left floating, the device selects internal LDO.

6.3.3 I²C Address Selection

By configuring MODE pin logic status, the TPS55289-Q1 selects two different I²C address. 表 6-2 shows the I²C target address setting

表 6-2. I²C target Address Setting

MODE pin	I²C target ADDRESS
Low	75h
High	74h

6.3.4 Input Undervoltage Lockout

When the input voltage is below 2.6V, the TPS55289-Q1 is disabled. When the input voltage is above 3V, the TPS55289-Q1 can be enabled by pulling the EN pin to a high voltage above 1.3V.

6.3.5 Enable and Programmable UVLO

The TPS55289-Q1 has a dual function enable and undervoltage lockout (UVLO) circuit. When the input voltage at the VIN pin is above the input UVLO rising threshold of 3V and the EN/UVLO pin is pulled above 1.15V but less than the enable UVLO threshold of 1.23V, the TPS55289-Q1 is enabled but still in standby mode. The TPS55289-Q1 starts to detect the MODE pin logic status and select the I^2C target address.

The EN/UVLO pin has an accurate UVLO voltage threshold to support programmable input undervoltage lockout with hysteresis. When the EN/UVLO pin voltage is greater than the UVLO threshold of 1.23V, the TPS55289-Q1 is enabled for I^2C communication and switching operation. A hysteresis current I_{UVLO_HYS} is sourced out of the EN/UVLO pin to provide hysteresis that prevents on/off chattering in the presence of noise with a slowly changing input voltage.

By using resistor divider as shown in 図 6-1, the turn-on threshold is calculated using 式 1.

$$V_{IN(UVLO\_ON)} = V_{UVLO} \times (1 + \frac{R1}{R2}) \quad (1)$$

where

- V_{UVLO} is the UVLO threshold of 1.23V at the EN/UVLO pin

The hysteresis between the UVLO turn-on threshold and turn-off threshold is set by the upper resistor in the EN/UVLO resistor divider and is given by the Equation 2.

$$\Delta V_{IN(UVLO)} = I_{UVLO\_HYS} \times R1 \quad (2)$$

where

- I_{UVLO_HYS} is the sourcing current from the EN/UVLO pin when the voltage at the EN/UVLO pin is above V_{UVLO}

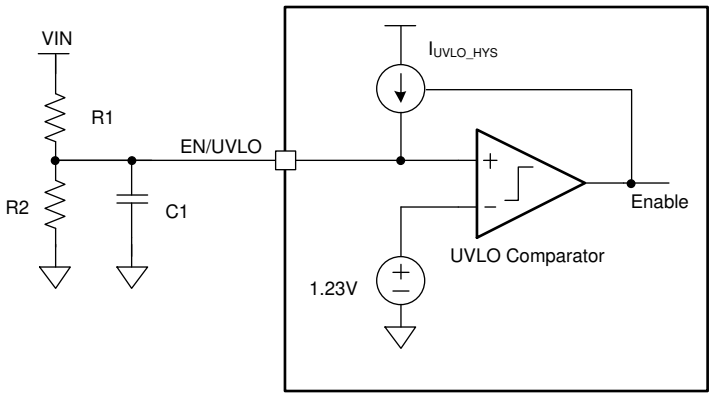


図 6-1. Programmable UVLO With Resistor Divider at the EN/UVLO Pin

Using an NMOSFET together with a resistor divider can implement both logic enable and programmable UVLO as shown in 図 6-2. The EN logic high level must be greater than enable threshold plus the V_{th} of the NMOSFET Q1. The Q1 also eliminates the leakage current from VIN to ground through the UVLO resistor divider during shutdown mode.

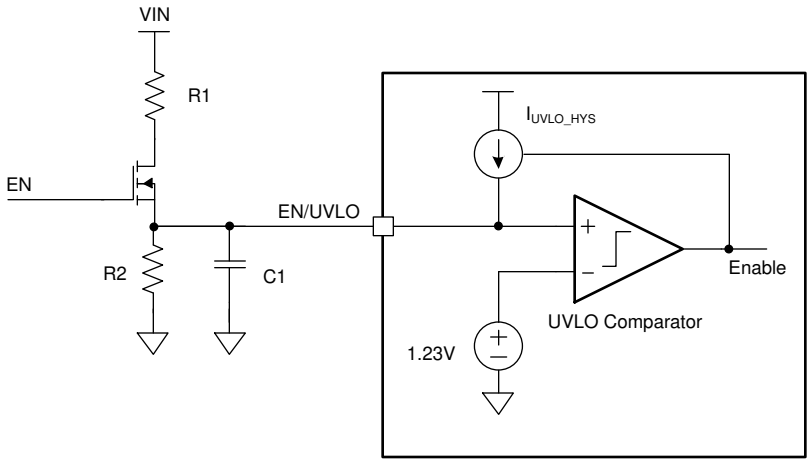


図 6-2. Logic Enable and Programmable UVLO

6.3.6 Soft Start

When the input voltage is above the UVLO threshold and the voltage at the EN/UVLO pin is above the enable UVLO threshold, the TPS55289-Q1 is ready to accept the command from I^2C controller device. An I^2C controller device can configure the internal registers of the TPS55289-Q1 before setting the OE bit of the register 06h. Once an I^2C controller device sets the OE bit to 1, the TPS55289-Q1 starts to ramp up the output voltage by ramping an internal reference voltage from 0V to a voltage set in the internal registers 00h and 01h within typical 3.6ms.

6.3.7 Shutdown and Load Discharge

When the EN/UVLO pin voltage is pulled below 0.4V, the TPS55289-Q1 is in shutdown mode, and all functions are disabled. All internal registers are reset to default values.

When the EN/UVLO pin is at high logic level and the OE bit is cleared to 0, the TPS55289-Q1 turns off the switching operation but keeps the I^2C interface active. Simultaneously, if the DISCHG bit in the register 06h is set to 1, the TPS55289-Q1 discharges the output voltage below 0.8V by an internal 100mA constant current.

When the EN/UVLO pin is at high logic level, the TPS55289-Q1 output discharge current can also be enabled by setting the Force_DISCHG bit in the register 06h to 1. During output voltage transient from high voltage to low voltage, the output discharge current helps reduce the VOUT falling time in auto PFM mode or reduces the reverse current in FPWM mode. It's not recommended to enable the discharge FET longer than 10ms due to high power loss.

6.3.8 Switching Frequency

The TPS55289-Q1 uses a fixed frequency average current control scheme. The switching frequency is between 200kHz and 2.2MHz set by placing a resistor at the FSW pin. An internal amplifier holds this pin at a fixed voltage of 1V. The setting resistance is between maximum of 100kΩ and minimum of 8.4kΩ. Use 式 3 to calculate the resistance by a given switching frequency.

$$f_{SW} = \frac{1000}{0.05 \times R_{FSW} + 35}(\text{MHz}) \quad (3)$$

where

- R_{FSW} is the resistance at the FSW pin (Ω)

For noise-sensitive applications, the TPS55289-Q1 can be synchronized to an external clock signal applied to the DITH/SYNC pin. The duty cycle of the external clock is recommended in the range of 30% to 70%. A resistor must also be connected to the FSW pin when the TPS55289-Q1 is switching by the external clock. The external clock frequency at the DITH/SYNC pin must have lower than 0.4V low level voltage and must be within ±30% of the corresponding frequency set by the resistor. 図 6-3 is a recommended configuration.

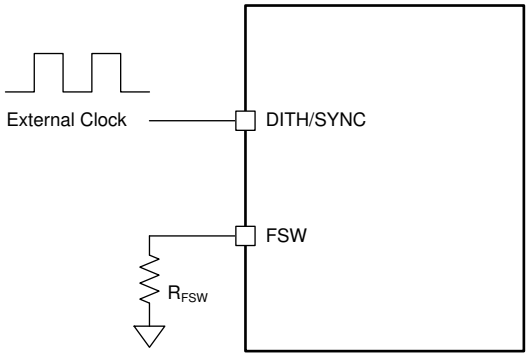


図 6-3. External Clock Configuration

6.3.9 Switching Frequency Dithering

The TPS55289-Q1 provides an optional switching frequency dithering that is enabled by connecting a capacitor from the DITH/SYNC pin to ground. 図 6-4 illustrates the dithering circuit. By charging and discharging the capacitor, a triangular waveform centered at 1V is generated at the DITH/SYNC pin. The triangular waveform modulates the oscillator frequency by ±7% of the nominal frequency set by the resistance at the FSW pin. The capacitance at the DITH/SYNC pin sets the modulation frequency. A small capacitance modulates the oscillator frequency at a fast rate than a large capacitance. For the dithering circuit to effectively reduce peak EMI, the modulation rate normally is below 1kHz. Equation 4 calculates the capacitance required to set the modulation frequency, F_{MOD}.

$$C_{DITH} = \frac{1}{2.8 \times R_{FSW} \times F_{MOD}} (F) \quad (4)$$

where

- R_{FSW} is the switching frequency setting resistance (Ω) at the FSW pin
- F_{MOD} is the modulation frequency (Hz) of the dithering

Connecting the DITH/SYNC pin below 0.4V or above 1.2V disables switching frequency dithering. The dithering function is also disabled when an external synchronous clock is used.

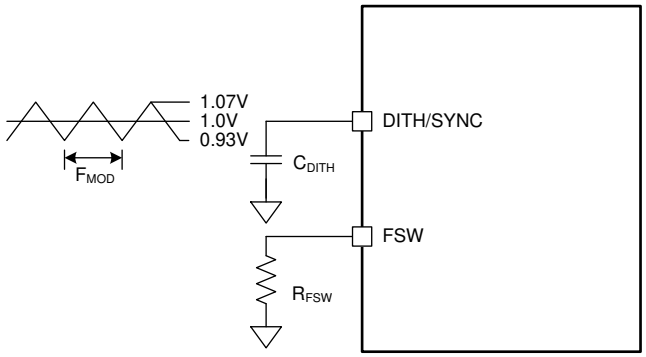


図 6-4. Switching Frequency Dithering

6.3.10 Inductor Current Limit

The TPS55289-Q1 implements both peak current and average inductor current limit. The average current mode control loop uses the current sense information at the high-side MOSFET of the boost leg to clamp the maximum average inductor current to 8A (typical).

Besides the average current limit, a peak current limit protection is implemented during transient to protect the device against over current condition beyond the capability of the device.

6.3.11 Internal Charge Path

Each of the two high-side MOSFET drivers is biased from its floating bootstrap capacitor, which is normally re-charged by V_{CC} through both the external and internal bootstrap diodes when the low-side MOSFET is turned on. When the TPS55289-Q1 operates exclusively in the buck or boost regions, one of the high-side MOSFETs is constantly on. An internal charge path, from VOUT and BOOT2 to BOOT1 or from VIN and BOOT1 to BOOT2, charges the bootstrap capacitor to V_{CC} so that the high-side MOSFET remains on.

6.3.12 Output Voltage Setting

There are two ways to set the output voltage: changing the feedback ratio and changing the reference voltage. The TPS55289-Q1 has a 11-bit DAC to program the reference voltage from 45mV to 1.2V. The TPS55289-Q1 also can select an internal feedback resistor divider or an external resistor divider by setting the FB bit in register 04h. When the FB bit is set to 0, the output voltage feedback ratio is set in internal register 04h. When the FB bit is set to 1, the output voltage feedback ratio is set by an external resistor divider.

When using internal output voltage feedback settings, there are four feedback ratios programmable by writing the INTFB[1:0] bits of register 04h. With this function, the TPS55289-Q1 can limit the maximum output voltage to different values. In addition, the minimum step of the output voltage change is also programmed to 10mV, 7.5mV, 5mV, and 2.5mV, accordingly.

When using an external output voltage feedback resistor divider as shown in 図 6-5, use 式 5 to calculate the output voltage with the reference voltage at the FB/$\overline{\text{INT}}$ pin.

$$V_{OUT} = V_{REF} \times (1 + \frac{R_{FB\_UP}}{R_{FB\_BT}}) \quad (5)$$

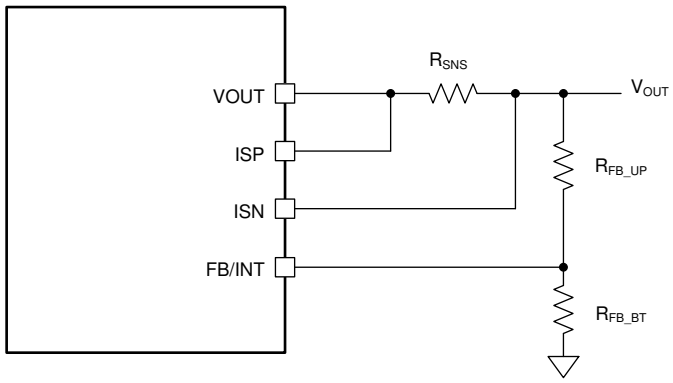


図 6-5. Output Voltage Setting by External Resistor Divider

TI recommends using 100kΩ for the up resistor R_{FB_UP}. The reference voltage V_{REF} at the FB/$\overline{\text{INT}}$ pin is programmable from 45mV to 1.2V by writing a 11-bit data into register 00h and 01h.

6.3.13 Output Current Monitoring and Cable Voltage Droop Compensation

The TPS55289-Q1 outputs a voltage at the CDC pin proportional to the sensed voltage across an output current sensing resistor between the ISP pin and the ISN pin. 式 6 shows the exact voltage at the CDC pin related to the sensed output current.

$$V_{CDC} = 20 \times (V_{ISP} - V_{ISN}) \quad (6)$$

To compensate the voltage droop across a cable from the output of the USB port to its powered device, the TPS55289-Q1 can lift its output voltage in proportion to the load current. There are two methods in the TPS55289-Q1 to implement the compensation: by setting internal register 05h or by placing a resistor between the CDC pin and AGND pin.

When using internal output voltage feedback, it is recommended to use the internal compensation setting. When using an external resistor divider at the FB/$\overline{INT}$ pin to set the output voltage, it is recommended to use the external compensation setting by placing a resistor at the CDC pin.

By default, the internal cable voltage droop compensation function is enabled with 0V added to the output voltage. Write the value into the bit CDC [2:0] in register 05h to get the desired voltage compensation.

When using external output voltage feedback, external compensation is better than the internal register for its high accuracy. The output voltage rises in proportion to the current sourcing from the CDC pin through the resistor at the CDC pin. It is recommended to use 100kΩ resistance for the up resistor of the feedback resistor divider. 式 7 shows the output voltage rise related to the sensed output current, the resistance at the CDC pin, and the up resistor of the output voltage feedback resistor divider.

$$V_{OUT\_CDC} = 3 \times R_{FB\_UP} \times \left(\frac{V_{ISP} - V_{ISN}}{R_{CDC}}\right) \quad (7)$$

where

- R_{FB_UP} is the up resistor of the resistor divider between the output and the FB/$\overline{INT}$ pin
- R_{CDC} is the resistor at the CDC pin

When RFB_UP is 100kΩ, the output voltage rise versus the sensed output current and the resistor at the CDC pin is shown in 図 6-6.

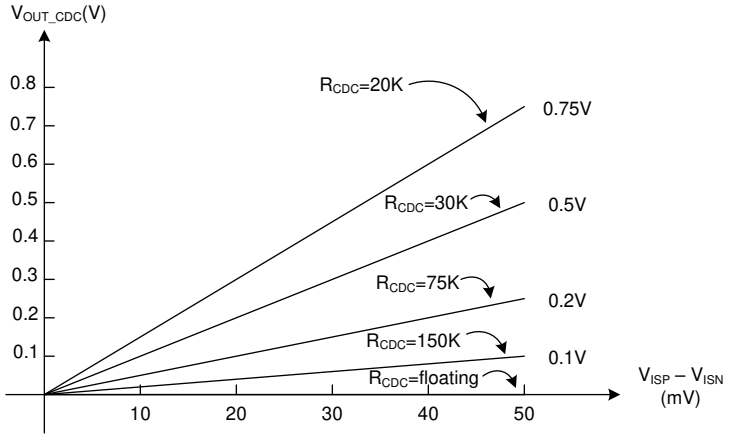


図 6-6. Output Voltage Rise versus Output Current

6.3.14 Output Current Limit

The output current limit is programmable from 0A to 6.35A by placing a 10mΩ current sensing resistor between the ISP pin and the ISN pin. Smaller resistance results in a higher current limit and bigger resistance results in a lower current limit. An internal register sets the current sense voltage across the ISP pin and the ISN pin. The programmable voltage step between the ISP pin and the ISN pin is 0.5mV.

Connecting the ISP and the ISN pin together to the VOUT pin disables the output current limit because the sensed voltage is always zero. The output current limit can also be disabled by reset the Current_Limit_EN bit in the Current_Limit register to 0.

6.3.15 Overvoltage Protection

The TPS55289-Q1 has output overvoltage protection. When the output voltage at the VOUT pin is detected above 23.5V typically, the TPS55289-Q1 turns off two high-side FETs and turns on two low-side FETs until its output voltage drops the hysteresis value lower than the output overvoltage protection threshold. This function prevents overvoltage on the output and secures the circuits connected to the output from excessive overvoltage.

6.3.16 Output Short Circuit Protection

In addition to the average inductor current limit, the TPS55289-Q1 implements the output short-circuit protection by entering hiccup mode. To enable hiccup mode, the HICCUP bit in register 06h must be set. After soft start-up time of 3.6ms, the TPS55289-Q1 monitors the average inductor current and output voltage. Whenever the output short circuit happens, causing the average inductor current hitting the set limit and the output voltage below 0.8V for 2ms, the TPS55289-Q1 shuts down the switching for 76ms (typical) and then repeats the soft start for 3.6ms. The hiccup mode helps reduce the total power dissipation on the TPS55289-Q1 in the output short-circuit or overcurrent condition.

6.3.17 Thermal Shutdown

The TPS55289-Q1 is protected by a thermal shutdown circuit that shuts down the device when the internal junction temperature exceeds 175°C (typical). The internal soft-start circuit is reset but all internal registers values remain unchanged when thermal shutdown is triggered. The converter automatically restarts when the junction temperature drops below the thermal shutdown hysteresis of 20°C below the thermal shutdown threshold.

6.4 Device Functional Modes

In light load condition, the TPS55289-Q1 can work in PFM or forced PWM mode to meet different application requirements. PFM mode decreases switching frequency to reduce the switching loss thus it gets high efficiency at light load condition. The FPWM mode keeps the switching frequency unchanged to avoid undesired low switching frequency but the efficiency becomes lower than that of PFM mode.

By default, the TPS55289-Q1 works in PFM mode. To set the device works in forced PWM mode, set the 01 bit of the register 06h to 1.

6.4.1 PWM Mode

In FPWM mode, the TPS55289-Q1 keeps the switching frequency unchanged in light load condition. When the load current decreases, the output of the internal error amplifier decreases as well to reduce the average inductor current down to deliver less power from input to output. When the output current further reduces, the current through the inductor decreases to zero during the switch-off time. The high-side N-MOSFET is not turned off even if the current through the MOSFET is zero. Thus, the inductor current changes its direction after it runs to zero. The power flow is from output side to input side. The efficiency is low in this condition. However, with the fixed switching frequency, there is no audible noise or other problems that might be caused by low switching frequency in light load condition.

6.4.2 Power Save Mode

The TPS55289-Q1 improves the efficiency at light load condition with PFM mode. By enabling the PFM function in the internal register, the TPS55289-Q1 can work in PFM mode at light load condition. When the TPS55289-Q1 operates at light load condition, the output of the internal error amplifier decreases to make the inductor peak current down to deliver less power to the load. When the output current further reduces, the current through the inductor will decrease to zero during the switch-off time. When the TPS55289-Q1 works in buck mode, once the inductor current becomes zero, the low-side switch of the buck side is turned off to prevent the reverse current from output to ground. When the TPS55289-Q1 works in boost mode, once the inductor current becomes zero, the high side-switch of the boost side is turned off to prevent the reverse current from output to input. The TPS55289-Q1 resumes switching until the output voltage drops. Thus PFM mode reduces switching cycles and eliminates the power loss by the reverse inductor current to get high efficiency in light load condition.

6.5 Programming

The TPS55289-Q1 uses I^2C interface for flexible converter parameter programming. I^2C is a bi-directional 2-wire serial interface. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). I^2C devices can be considered as controllers or targets when performing data transfers. A controller is the device that initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a target.

The TPS55289-Q1 operates as a target device with address 74h and 75h set by MODE pin. Receiving control inputs from the controller device like a microcontroller or a digital signal processor reads and writes the internal registers 00h through 07h. The I^2C interface of the TPS55289-Q1 supports both standard mode (up to 100 kbit/s) and fast mode plus (up to 1000 kbit/s). Both SDA and SCL must be connected to the positive supply voltage through current sources or pullup resistors. When the bus is free, both lines are in high voltage.

6.5.1 Data Validity

The data on the SDA line must be stable during the high level period of the clock. The high level or low level state of the data line can only change when the clock signal on the SCL line is low level. One clock pulse is generated for each data bit transferred.

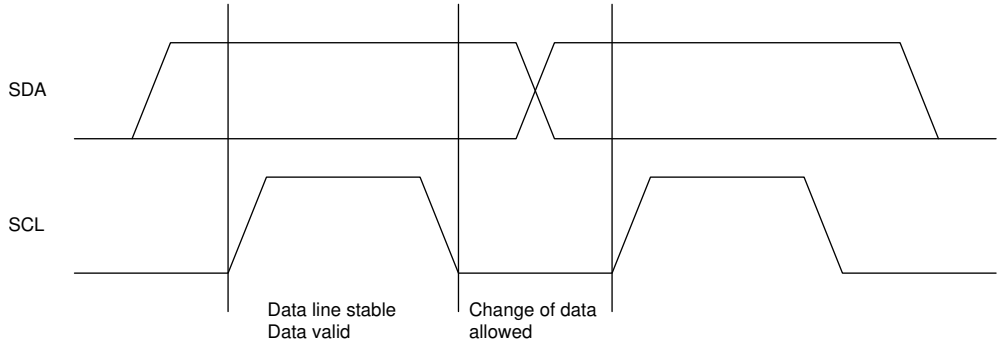


図 6-7. I²C Data Validity

6.5.2 START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A high level to low level transition on the SDA line while SCL is at high level defines a START condition. A low level to high level transition on the SDA line when the SCL is at high level defines a STOP condition.

START and STOP conditions are always generated by the controller. The bus is considered busy after the START condition, and free after the STOP condition.

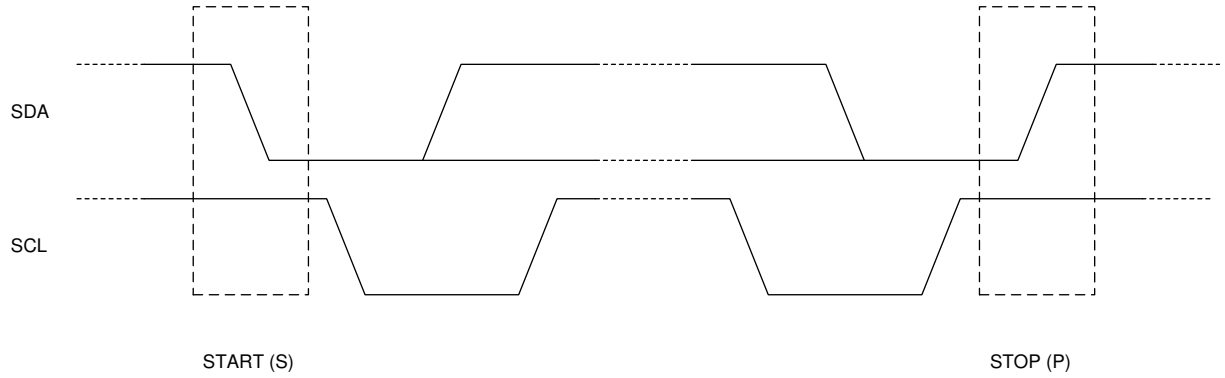


図 6-8. I²C START and STOP Conditions

6.5.3 Byte Format

Every byte on the SDA line must be eight bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first. If a target cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the controller into a wait state (clock stretching). Data transfer then continues when the target is ready for another byte of data and release the clock line SCL.

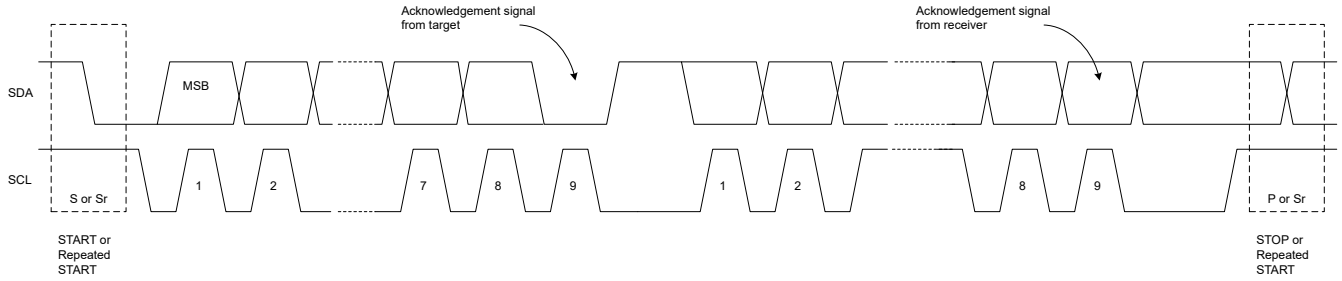


図 6-9. Byte Format

6.5.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the controller.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line to low level and it remains stable low level during the high level period of this clock pulse.

The Not Acknowledge signal is when SDA remains high level during the 9th clock pulse. The controller can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

6.5.5 target Address and Data Direction Bit

After the START, a target address is sent. This address is seven bits long followed by the eighth bit as a data direction bit (bit R/$\overline{W}$). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

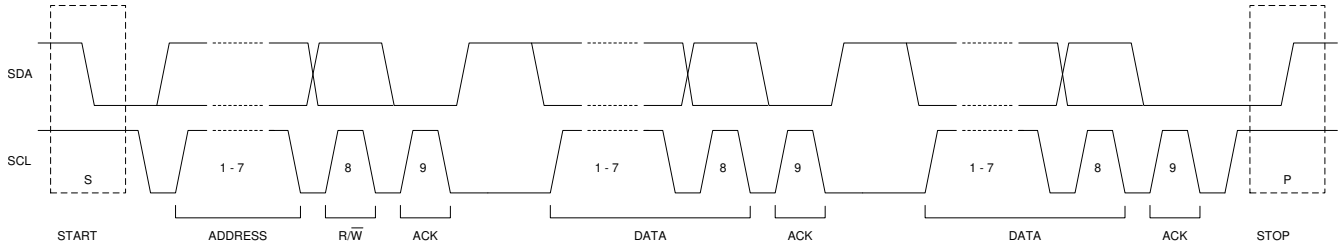


図 6-10. target Address and Data Direction

6.5.6 Single Read and Write

図 6-11 and 図 6-12 show the single-byte write and single-byte read format of the I²C communication.

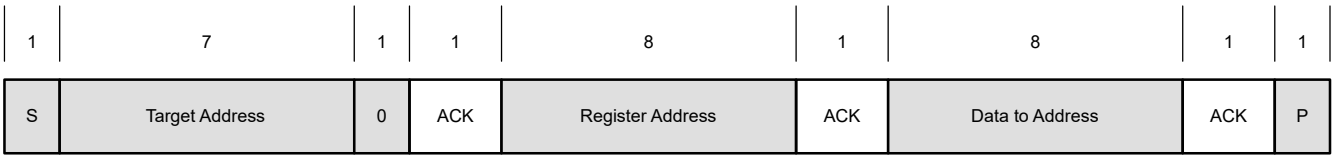


図 6-11. Single-byte Write

図 6-12. Single-byte Read

If the register address is not defined, the TPS55289-Q1 sends back NACK and goes back to the idle state.

6.5.7 Multi-Read and Multi-Write

The TPS55289-Q1 supports multi-read and multi-write.

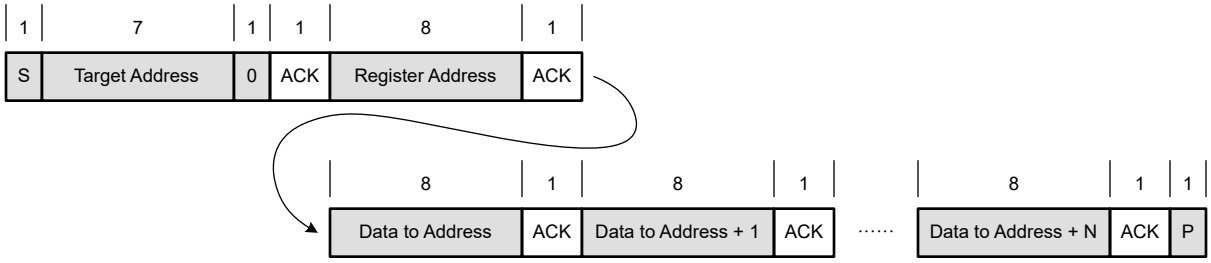


図 6-13. Multi-byte Write

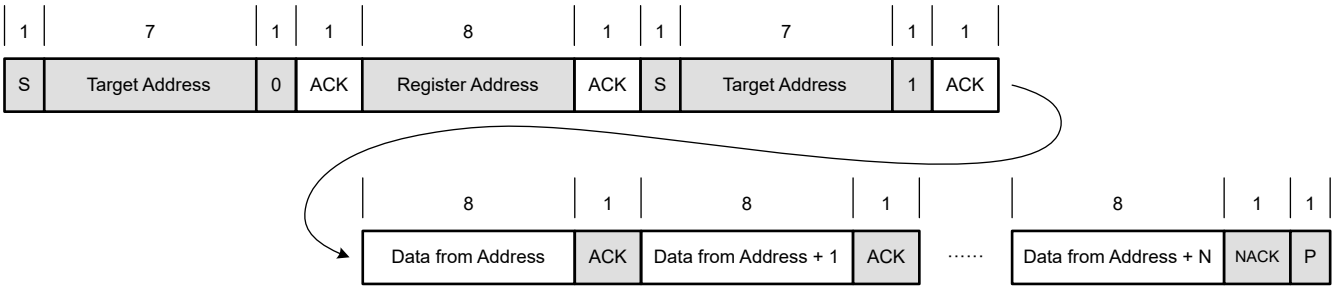


図 6-14. Multi-byte Read

7 Register Maps

表 7-1 lists the memory-mapped registers for the device registers. All register offset addresses not listed in 表 7-1 should be considered as reserved locations, and the register contents should not be modified.

表 7-1. Device Registers

Address	Acronym	Register Name	Section
0h, 1h	REF	Reference Voltage	Go
2h	IOUT_LIMIT	Current Limit Setting	Go
3h	VOUT_SR	Slew Rate	Go
4h	VOUT_FS	Feedback Selection	Go
5h	CDC	Cable Compensation	Go
6h	MODE	Mode Control	Go
7h	STATUS	Operating Status	Go

7.1 REF Register (Address = 0h, 1h) [reset = 10100100b, 00000001b]

REF is shown in 図 7-1 and 図 7-2 described in 表 7-2.

Return to Summary Table.

REF sets the internal reference voltage of the TPS55289-Q1. The 01h register is the high byte and the 00h register is the low byte. One LSB of register 00h stands for 0.5645mV of the internal reference voltage. The default register value is 00000001 10100100b of 282mV. When the register value is 00000000 00000000b, the reference voltage is 45mV. When the register value is 00000111 10000000b, the reference voltage is 1.129V. The output voltage of the TPS55289-Q1 also depends on the output feedback ratio, which is either set in register 04h or set by an external resistor divider.

When using internal output voltage feedbcak divider, the output voltage V_{OUT} is calculated by 式 8

$$V_{OUT} = \frac{V_{REF}}{INTFB} \quad (8)$$

The REF register can be configured by an I^2C controller before setting the OE bit in register 06h. For 5V output voltage, set the REF register value to 00000001 10100100b. To set the internal reference voltage, write the register 00h first, then write the register 01h.

図 7-1. REF_LSB

7	6	5	4	3	2	1	0
VREF							
R/W-10100100b							

図 7-2. REF_MSB

15	14	13	12	11	10	9	8
Reserved					VREF		
R-00000b					R/W-001b		

表 7-2. REF Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	Reserved	R	00000b	Reserved
10-0	VREF	R/W	001 10100100b	Sets the internal reference voltage 000 00000000b = 45mV reference voltage 000 00000001b = 45.5645mV reference voltage 000 00000010b = 46.129mV reference voltage ..... = ... 001 10100100b = 282mV reference voltage (Default) ..... = ... 011 00110100b = 508mV reference voltage ..... = ... 101 10001100b = 846mV reference voltage ..... = ... 111 10000000b = 1129mV reference voltage ..... = ... 111 11111110b = 1200mV reference voltage

7.2 IOUT_LIMIT Register (Address = 2h) [reset = 11100100b]

IOUT_LIMIT is shown in 図 7-3 and described in 表 7-3.

Return to Summary Table.

IOUT_LIMIT sets the current limit target voltage between the ISP pin and the ISN pin. The default value in the current limit register is 11100100b standing for 50mV. 1 LSB stands for 0.5mV. The bit7 enables the current limit or disables the current limit.

図 7-3. IOUT_LIMIT Register

7	6	5	4	3	2	1	0
Current_Limit_EN	Current_Limit_Setting						
R/W-1b	R/W-1100100b						

表 7-3. IOUT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Current_Limit_EN	R/W	1b	Enable or disable current limit. 0b = Current limit disabled 1b = Current limit enabled (Default)
6-0	Current_Limit_Setting	R/W	1100100b	Sets the current limit target voltage between the ISP pin and the ISN pin 0000000b = V_{ISP}-V_{ISN} = 0 (mV) 0000001b = V_{ISP}-V_{ISN} = 0.5 (mV) 0000010b = V_{ISP}-V_{ISN} = 1 (mV) 0000011b = V_{ISP}-V_{ISN} = 1.5 (mV) 0000100b = V_{ISP}-V_{ISN} = 2.0 (mV) …… = …… 1100100b = V_{ISP}-V_{ISN} = 50.0 (mV) (Default) …… = …… 1111111b = V_{ISP}-V_{ISN} = 63.5 (mV)

7.3 VOUT_SR Register (Address = 3h) [reset = 00000001b]

VOUT_SR is shown in 図 7-4 and described in 表 7-4.

Return to Summary Table.

Register 03h sets the slew rate of the output voltage change and the response delay time after the output current exceeds the setting output current limit.

The OCP_DELAY [1:0] bits set the response time of the TPS55289-Q1 when the output overcurrent limit is hit. This allows the TPS55289-Q1 to output high current in a relative short duration time. The default setting is 128µs so that the TPS55289-Q1 immediately limits the output current.

The SR [1:0] bits set 1.25mV/µs, 2.5mV/µs, 5mV/µs, and 10mV/µs slew rate for output voltage change.

図 7-4. VOUT_SR Register

7	6	5	4	3	2	1	0
RESERVED		OCP_DELAY		RESERVED		SR	
R-0b		R/W-00b		R-00b		R/W-01b	

表 7-4. VOUT_SR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved
5-4	OCP_DELAY	R/W	00b	Sets the response time of the device when the output overcurrent limit is reached. 00b = 128 µs (Default) 01b = Delay 1.024 x 3 ms 10b = Delay 1.024 x 6 ms 11b = Delay 1.024 x 12 ms
3-2	RESERVED	R	00b	Reserved
1-0	SR	R/W	01b	Sets slew rate for output voltage change. 00b = 1.25 mV/µs output change slew rate 01b = 2.5 mV/µs output change slew rate (Default) 10b = 5 mV/µs output change slew rate 11b = 10 mV/µs output change slew rate

7.4 VOUT_FS Register (Address = 4h) [reset = 00000011b]

VOUT_FS is shown in 図 7-5 and described in 表 7-5.

Return to Summary Table.

Register 04h sets the selection for the output feedback voltage, either by an internal resistor divider or external resistor divider, and sets the internal feedback ratio when using internal feedback resistor divider.

図 7-5. VOUT_FS Register

7	6	5	4	3	2	1	0
FB	RESERVED					INTFB	
R/W-0b	R-00000b					R/W-11b	

表 7-5. VOUT_FS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FB	R/W	0b	Output feedback voltage 0b = Use internal output voltage feedback. The FB/$\overline{\text{INT}}$ pin is the indicator for output short circuit protection, overcurrent status, and overvoltage status (Default). 1b = Use external output voltage feedback. The FB/$\overline{\text{INT}}$ pin is the feedback input of the output voltage.
6-2	RESERVED	R	00000b	Reserved
1-0	INTFB	R/W	11b	Internal feedback ratio 00b = Set internal feedback ratio to 0.2256 01b = Set internal feedback ratio to 0.1128 10b = Set internal feedback ratio to 0.0752 11b = Set internal feedback ratio to 0.0564(Default)

表 7-6. Output Voltage vs Internal Reference

INTFB1	INTFB0	REF=0000h	REF=001Ah	REF=0050h	REF=00F0h	REF=0780h	Output Voltage Step
0	0				0.8V	5V	2.5mV
0	1			0.8V		10V	5mV
1	0		0.8V			15V	7.5mV
1	1	0.8V				20V	10mV

7.5 CDC Register (Address = 5h) [reset = 11100000b]

CDC is shown in 図 7-6 and described in 表 7-7.

Return to Summary Table.

Register 05h sets masks for SC bit, OCP bit, and OVP bit in register 07h. In addition, register 05h sets the voltage rise added to the setting output voltage with respect to the sensed differential voltage between the ISP pin and the ISN pin.

図 7-6. CDC Register

7	6	5	4	3	2	1	0
SC_MASK	OCP_MASK	OVP_MASK	RESERVED	CDC_OPTION	CDC		
R/W-1b	R/W-1b	R/W-1b	R-0b	R/W-0b	R/W-000b		

表 7-7. CDC Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SC_MASK	R/W	1b	Short circuit mask 0b = Disabled SC indication 1b = Enable SC indication (Default)
6	OCP_MASK	R/W	1b	Over current mask 0b = Disabled OCP indication 1b = Enable OCP indication (Default)
5	OVP_MASK	R/W	1b	Over voltage mask 0b = Disabled OVP indication 1b = Enable OVP indication (Default)
4	RESERVED	R	0b	Reserved
3	CDC_OPTION	R/W	0b	Select the cable voltage droop compensation approach. 0b = Internal CDC compensation by the register 05H (Default) 1b = External CDC compensation by a resistor at the CDC pin
2-0	CDC	R/W	000b	Compensation for voltage droop over the cable 000b = 0-V output voltage rise with 50mV at V_{ISP} - V_{ISN} (Default) 001b = 0.1V output voltage rise with 50mV at V_{ISP} - V_{ISN} 010b = 0.2V output voltage rise with 50 mV at V_{ISP} - V_{ISN} 011b = 0.3V output voltage rise with 50mV at V_{ISP} - V_{ISN} 100b = 0.4V output voltage rise with 50mV at V_{ISP} - V_{ISN} 101b = 0.5V output voltage rise with 50mV at V_{ISP} - V_{ISN} 110b = 0.6V output voltage rise with 50mV at V_{ISP} - V_{ISN} 111b = 0.7V output voltage rise with 50mV at V_{ISP} - V_{ISN}

7.6 MODE Register (Address = 6h) [reset = 00100000b]

MODE is shown in 図 7-7 and described in 表 7-8.

Return to Summary Table.

MODE controls the operating mode of the TPS55289-Q1.

図 7-7. MODE Register

7	6	5	4	3	2	1	0
OE	FSW	HICCUP	DISCHG	Force_DISCHG	Reserved	FPWM	Reserved
R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-0b	R-0b	R/W-0b	R-0b

表 7-8. MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OE	R/W	0b	Output enable 0b = Output disabled (Default) 1b = Output enable
6	FSWDBL	R/W	0b	Switching frequency doubling in buck-boost mode 0b = Keep the switching frequency unchanged during buck-boost mode (Default) 1b = Double the switching frequency during buck-boost mode
5	HICCUP	R/W	1b	Hiccup mode 0b = Disable the hiccup during output short circuit protection. 1b = Enable the hiccup during output short circuit protection (Default)
4	DISCHG	R/W	0b	Output discharge 0b = Disabled VOUT discharge when the device is in shutdown mode (Default) 1b = Enable VOUT discharge. VOUT is discharged to ground by an internal 100mA current sink in shutdown mode (OE bit is cleared to 0)
3	Force_DISCHG	R/W	0b	Force output dischage Force output discharge helps reduce the VOUT falling time in auto PFM mode when set VOUT to lower voltage. TI does not recommend enabling this bit longer than 10ms at high VOUT range (>10V) due to high power loss. 0b = Disabled VOUT discharge FET(Default) 1b = Force enable VOUT discharge FET. VOUT is discharged to ground by an internal 100mA current sink
2	RESERVED	R	0b	Reserved
1	FPWM	R/W	0b	Select operating mode at light load condition 0b = PFM operating mode at light load condition (Default) 1b = FPWM operating mode at light load condition
0	RESERVED	R	0b	Reserved

7.7 STATUS Register (Address = 7h) [reset = 00000011b]

STATUS is shown in 図 7-8 and described in 表 7-9.

Return to Summary Table.

The STATUS register stores the operating status of the TPS55289-Q1. When any of the SCP bit, the OCP bit, or the OVP bit are set, and the corresponding mask bit in register 05h is set as well, the FB/$\overline{INT}$ pin outputs low logic level to indicate the situation. Reading register 07h clears the SCP bit, OCP bit, and OVP bit. After the SCP bit, OCP bit, or OVP bit is set, it does not reset until the register is read. If the situation still exists, the corresponding bit is set again.

図 7-8. STATUS Register

7	6	5	4	3	2	1	0
SCP	OCP	OVP	Reserved	Reserved	Reserved	STATUS	
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-11b	

表 7-9. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SCP	R	0b	Short circuit protection 0b = No short circuit 1b = Short circuit happens. Does not reset until it is read.
6	OCP	R	0b	Overcurrent protection 0b = No output overcurrent 1b = Output current hits the current limit sensed at the ISP and the ISN pin. Does not reset until it is read.
5	OVP	R	0b	Overvoltage protection 0b = No OVP 1b = Output voltage exceeds the OVP threshold. Does not reset until it is read.
4	RESERVED	R	0b	Reserved
3	RESERVED	R	0b	Reserved
2	RESERVED	R	0b	Reserved
1-0	STATUS	R	11b	Operating status 00b = Boost 01b = Buck 10b = Buck-Boost 11b = Reserved

7.8 Register Summary

The 表 7-10 summarizes the default settings of the registers in the TPS55289-Q1.

表 7-10. Default Settings of Registers

Register Address	Register Name	R/W	Default Values
00h	VREF_LSB	R/W	10100100
01h	VREF_MSB	R/W	00000001
02h	IOUT_LIMIT	R/W	11100100
03h	VOUT_SR	R/W	00000001
04h	VOUT_FS	R/W	00000011
05h	CDC	R/W	11100000
06h	MODE	R/W	00100000
07h	STATUS	R	00000011

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS55289-Q1 can operate over a wide range of 3.0V to 36V input voltage and output 0.8V to 22V. It can transition among buck mode, buck-boost mode, and boost mode smoothly according to the input voltage and the setting output voltage. The TPS55289-Q1 operates in buck mode when the input voltage is greater than the output voltage and in boost mode when the input voltage is less than the output voltage. When the input voltage is close to the output voltage, the TPS55289-Q1 operates in one-cycle buck and one-cycle boost mode alternately. The switching frequency is set by an external resistor. To reduce the switching power loss in high power conditions, it is recommended to set the switching frequency below 500kHz. If a system requires higher switching frequency above 500kHz, it is recommended to operate at lower switch current for better thermal performance.

8.2 Typical Application

The TPS55289-Q1 provides a small size solution for USB PD power supply application with the input voltage ranging from 9V to 36V.

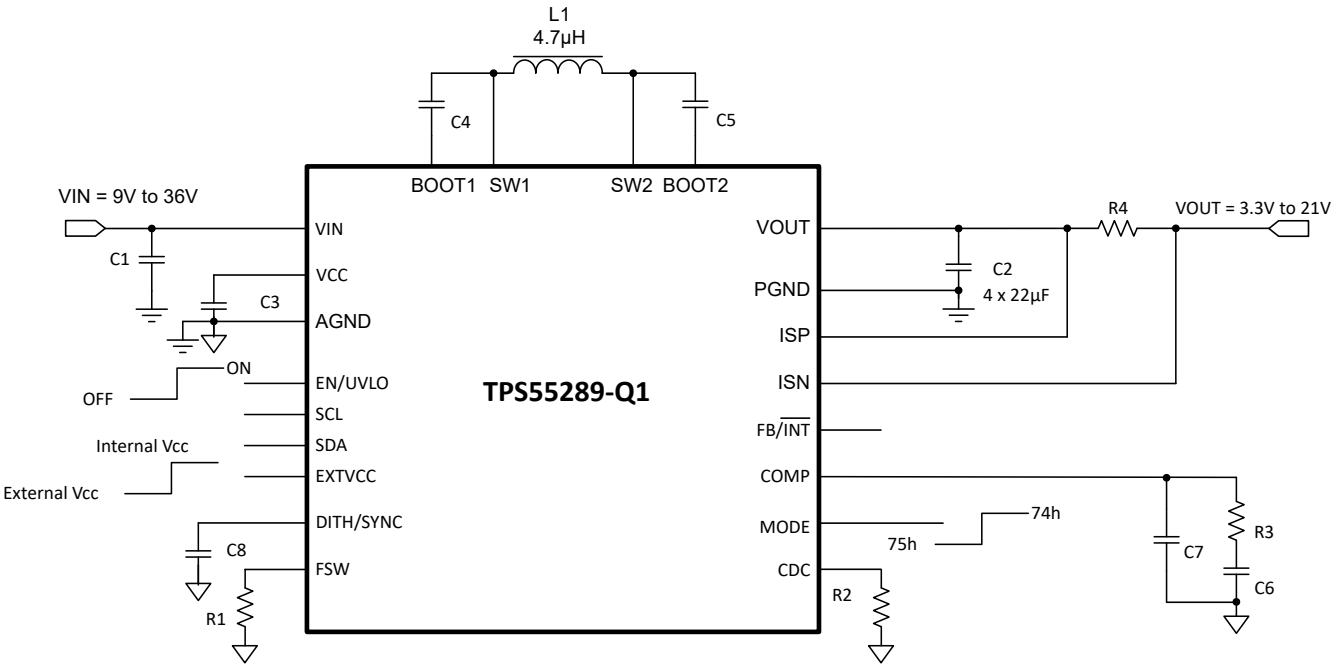


図 8-1. USB PD Power Supply With 9V to 36V Input Voltage

8.2.1 Design Requirements

The design parameters are listed in 表 8-1:

表 8-1. Design Parameters

PARAMETERS	VALUES
Input voltage	9V to 36V
Output voltage	3.3V to 20V
Output current limit	2.5A
Output voltage ripple	±50mV
Operating mode at light load	FPWM

8.2.2 Detailed Design Procedure

8.2.2.1 Switching Frequency

The switching frequency of the TPS55289-Q1 is set by a resistor at the FSW pin. Use 式 3 to calculate the resistance for the desired frequency. To reduce the switching power loss with such a high current application, a 1% standard resistor of 49.9kΩ is selected for 400kHz switching frequency for this application.

8.2.2.2 Output Voltage Setting

The TPS55289-Q1 has I^2C interface to set the internal reference voltage. A microcontroller can easily set the desired output voltage by writing the proper data into the reference voltage registers through I^2C bus.

8.2.2.3 Inductor Selection

Since the selection of the inductor affects steady state operation, transient behavior, and loop stability, the inductor is the most important component in power regulator design. There are three important inductor specifications: inductance, saturation current, and DC resistance.

The TPS55289-Q1 is designed to work with inductor values between 1µH and 10µH. The inductor selection is based on consideration of both buck and boost modes of operation.

For buck mode, the inductor selection is based on limiting the peak-to-peak current ripple to the maximum inductor current at the maximum input voltage. In CCM, Equation 9 shows the relationship between the inductance and the inductor ripple current.

$$L=\frac{(V_{IN(MAX)}-V_{OUT})\times V_{OUT}}{\Delta I_{L(P-P)}\times f_{SW}\times V_{IN(MAX)}} \quad (9)$$

where

- $V_{IN(MAX)}$ is the maximum input voltage
- V_{OUT} is the output voltage
- $\Delta I_{L(P-P)}$ is the peak to peak ripple current of the inductor
- f_{SW} is the switching frequency

For a certain inductor, the inductor ripple current achieves maximum value when VOUT equals half of the maximum input voltage. Choosing higher inductance gets smaller inductor current ripple while smaller inductance gets larger inductor current ripple.

For boost mode, the inductor selection is based on limiting the peak-to-peak current ripple to the maximum inductor current at the maximum output voltage. In CCM, Equation 10 shows the relationship between the inductance and the inductor ripple current.

$$L=\frac{V_{IN}\times(V_{OUT(MAX)}-V_{IN})}{\Delta I_{L(P-P)}\times f_{SW}\times V_{OUT(MAX)}} \quad (10)$$

where

- V_{IN} is the input voltage
- $V_{OUT(MAX)}$ is the maximum output voltage
- $\Delta I_{L(P-P)}$ is the peak to peak ripple current of the inductor
- f_{SW} is the switching frequency

For a certain inductor, the inductor ripple current achieves maximum value when V_{IN} equals to the half of the maximum output voltage. Choosing higher inductance gets smaller inductor current ripple while smaller inductance gets larger inductor current ripple.

For this application example, a 4.7µH inductor is selected, which produces approximate maximum inductor current ripple of 50% of the highest average inductor current in buck mode and 50% of the highest average inductor current in boost mode.

In buck mode, the inductor DC current equals to the output current. In boost mode, the inductor DC current can be calculated with Equation 11.

$$I_{L(DC)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \tag{11}$$

where

- V_{OUT} is the output voltage
- I_{OUT} is the output current
- V_{IN} is the input voltage
- η is the power conversion efficiency

For a given maximum output current of the buck-boost converter TPS55289-Q1, the maximum inductor DC current happens at the minimum input voltage and maximum output voltage. Set the inductor current limit of the TPS55289-Q1 higher than the calculated maximum inductor DC current to make sure the TPS55289-Q1 has the desired output current capability.

In boost mode, the inductor ripple current is calculated with Equation 12.

$$\Delta I_{L(P-P)} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{L \times f_{SW} \times V_{OUT}} \tag{12}$$

where

- $\Delta I_{L(P-P)}$ is the inductor ripple current
- L is the inductor value
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Therefore, the inductor peak current is calculated with Equation 13.

$$I_{L(P)} = I_{L(DC)} + \frac{\Delta I_{L(P-P)}}{2} \tag{13}$$

Normally, it is advisable to work with an inductor peak-to-peak current of less than 40% of the average inductor current for maximum output current. A smaller ripple from a larger valued inductor reduces the magnetic hysteresis losses in the inductor and EMI, but in the same way, load transient response time is increased. The selected inductor must have higher saturation current than the calculated peak current.

The conversion efficiency is dependent on the resistance of its current path. The switching loss associated with the switching MOSFETs, and the inductor core loss. Therefore, the overall efficiency is affected by the inductor

DC resistance (DCR), equivalent series resistance (ESR) at the switching frequency, and the core loss. 表 8-2 lists recommended inductors for the TPS55289-Q1. In this application example, the Coilcraft inductor XAL7070-472 is selected for its small size, high saturation current, and small DCR.

表 8-2. Recommended Inductors

PART NUMBER	L (µH)	DCR (MAXIMUM) (mΩ)	SATURATION CURRENT / HEAT RATING CURRENT (A)	SIZE (L x W x H mm)	VENDOR(1)
XAL7070-472ME	4.7	14.3	15.2/10.5	7.5 × 7.2 × 7.0	Coilcraft
VCHA085D-4R7MS6	4.7	15.6	16.0/8.8	8.7 × 8.2 × 5.2	Cyntec
IHLP4040DZER4R7M01	4.7	16.5	17/9.5	10.2 × 10.2 × 4.0	Vishay

(1) See the *Third-party Products* disclaimer.

8.2.2.4 Input Capacitor

In buck mode, the input capacitor supplies high ripple current. The RMS current in the input capacitors is given by Equation 14.

$$I_{CIN(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times V_{IN}}} \quad (14)$$

where

- $I_{CIN(RMS)}$ is the RMS current through the input capacitor
- I_{OUT} is the output current

The maximum RMS current occurs at the output voltage is half of the input voltage, which gives $I_{CIN(RMS)} = I_{OUT} / 2$. Ceramic capacitors are recommended for their low ESR and high ripple current capability. A total of 20µF effective capacitance is a good starting point for this application.

8.2.2.5 Output Capacitor

In boost mode, the output capacitor conducts high ripple current. The output capacitor RMS ripple current is given by Equation 15, where the minimum input voltage and the maximum output voltage correspond to the maximum capacitor current.

$$I_{COUT(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} - 1} \quad (15)$$

where

- $I_{COUT(RMS)}$ is the RMS current through the output capacitor
- I_{OUT} is the output current

In this example, the maximum output ripple RMS current is 2.8A.

The ESR of the output capacitor causes an output voltage ripple given by Equation 16 in boost mode.

$$V_{RIPPLE(ESR)} = \frac{I_{OUT} \times V_{OUT}}{V_{IN}} \times R_{COUT} \quad (16)$$

where

- R_{COUT} is the ESR of the output capacitance

The capacitance also causes a capacitive output voltage ripple given by Equation 17 in boost mode. When input voltage reaches the minimum value and the output voltage reaches the maximum value, there is the largest output voltage ripple caused by the capacitance.

$$V_{RIPPLE(CAP)} = \frac{I_{OUT} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right)}{C_{OUT} \times f_{SW}} \quad (17)$$

Typically, a combination of ceramic capacitors and bulk electrolytic capacitors is needed to provide low ESR, high ripple current, and small output voltage ripple. From the required output voltage ripple, use Equation 16 and Equation 17 to calculate the minimum required effective capacitance of the C_{OUT}.

8.2.2.6 Output Current Limit

The output current limit is implemented by putting a current sense resistor between the ISP and ISN pins along with setting a limit voltage between the ISP pin and the ISN pin through register 02h. The maximum value of the limit voltage between the ISP and ISN pins is 63.5mV. The default limit voltage is 50mV. The current sense resistor between the ISP and ISN pins should be selected to ensure that the output current limit is set high enough for output. The output current limit setting resistor is given by Equation 18.

$$R_{SNS} = \frac{V_{SNS}}{I_{OUT\_LIMIT}} \quad (18)$$

where

- V_{SNS} is the current limit setting voltage between the ISP and ISN pins
- I_{OUT_LIMIT} is the desired output current limit

Because the power dissipation is large, make sure the current sense resistor has enough power dissipation capability with large package.

8.2.2.7 Loop Stability

The TPS55289-Q1 uses average current control scheme. The inner current loop uses internal compensation and requires the inductor value must be larger than $1.2/f_{SW}$. The outer voltage loop requires an external compensation. The COMP pin is the output of the internal voltage error amplifier. An external compensation network comprised of resistor and ceramic capacitors is connected to the COMP pin.

The TPS55289-Q1 operates in buck mode or boost mode. Therefore, both buck and boost operating modes require loop compensations. The restrictive one of both compensations is selected as the overall compensation from a loop stability point of view. Typically for a converter designed either work in buck mode or boost mode, the boost mode compensation design is more restrictive due to the presence of a right half plane zero (RHPZ).

The power stage in boost mode can be modeled by Equation 19.

$$G_{PS}(s) = \frac{R_{LOAD} \times (1-D)}{2 \times R_{SENSE}} \times \frac{\left(1 + \frac{s}{2\pi \times f_{ESRZ}}\right) \times \left(1 - \frac{s}{2\pi \times f_{RHPZ}}\right)}{1 + \frac{s}{2\pi \times f_P}} \quad (19)$$

where

- R_{LOAD} is the output load resistance
- D is the switching duty cycle in boost mode
- R_{SENSE} is the equivalent internal current sense resistor, which is 0.055Ω

The power stage has two zeros and one pole generated by the output capacitor and load resistance. Use 式 20 to Equation 22 to calculate them.

$$f_P = \frac{2}{2\pi \times R_{LOAD} \times C_{OUT}} \quad (20)$$

$$f_{ESRZ} = \frac{1}{2\pi \times R_{COUT} \times C_{OUT}} \quad (21)$$

$$f_{RHPZ} = \frac{R_{LOAD} \times (1-D)^2}{2\pi \times L} \quad (22)$$

The internal transconductance amplifier together with the compensation network at the COMP pin constitutes the control portion of the loop. The transfer function of the control portion is shown by Equation 23.

$$G_C(s) = \frac{G_{EA} \times R_{EA} \times V_{REF}}{V_{OUT}} \times \frac{\left(1 + \frac{s}{2\pi \times f_{COMZ}}\right)}{\left(1 + \frac{s}{2\pi \times f_{COMP1}}\right) \times \left(1 + \frac{s}{2\pi \times f_{COMP2}}\right)} \quad (23)$$

where

- G_{EA} is the transconductance of the error amplifier
- R_{EA} is the output resistance of the error amplifier
- V_{REF} is the reference voltage input to the error amplifier
- V_{OUT} is the output voltage
- f_{COMP1} and f_{COMP2} are the pole's frequency of the compensation network
- f_{COMZ} is the zero's frequency of the compensation network

The total open-loop gain is the product of $G_{PS}(s)$ and $G_C(s)$. The next step is to choose the loop crossover frequency, f_C, at which the total open-loop gain is 1, namely 0dB. The higher in frequency that the loop gain stays above 0 dB before crossing over, the faster the loop response. It is generally accepted that the loop gain cross over 0dB at the frequency no higher than the lower of either 1/10 of the switching frequency, f_{SW} or 1/5 of the RHPZ frequency, f_{RHPZ}.

Then, set the value of R_C, C_C, and C_P by Equation 24 to Equation 26.

$$R_C = \frac{2\pi \times V_{OUT} \times R_{SENSE} \times C_{OUT} \times f_C}{(1-D) \times V_{REF} \times G_{EA}} \quad (24)$$

where

- f_C is the selected crossover frequency

$$C_C = \frac{R_{LOAD} \times C_{OUT}}{2 \times R_C} \quad (25)$$

$$C_P = \frac{R_{COUT} \times C_{OUT}}{R_C} \quad (26)$$

If the calculated C_P is less than 10pF, it can be left open.

Designing the loop for greater than 45° of phase margin and greater than 10dB gain margin eliminates output voltage ringing during the line and load transient.

8.2.3 Application Curves

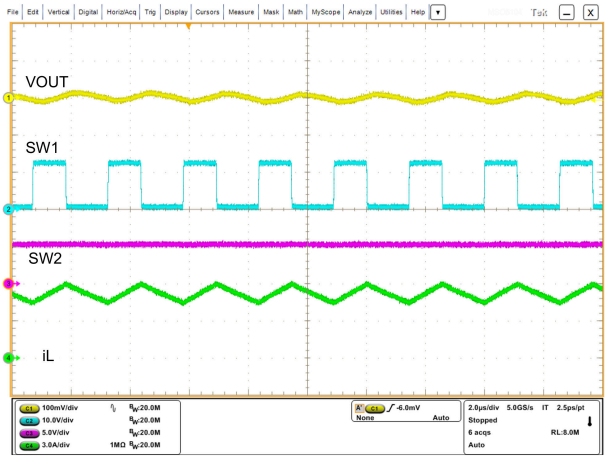


図 8-2. Switching Waveforms in V_{IN} = 12V, V_{OUT} = 5V, I_O = 5A, FPWM

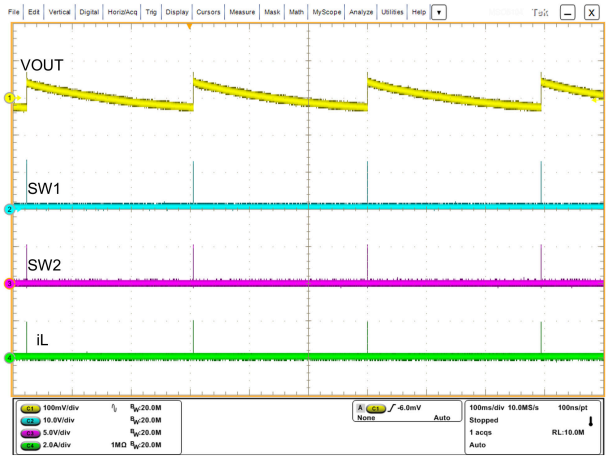


図 8-3. Switching Waveforms in V_{IN} = 12V, V_{OUT} = 5V, I_O = 0A, PFM

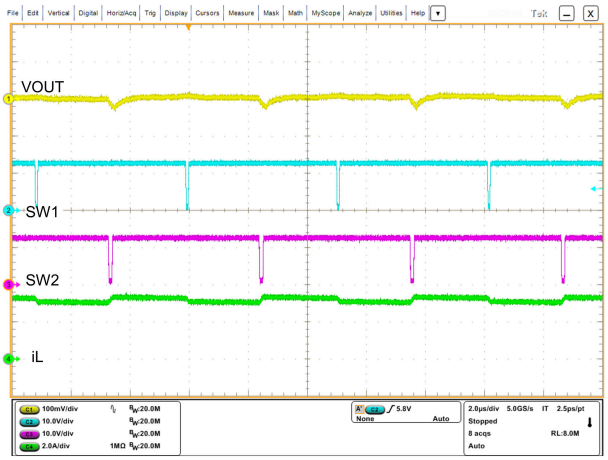


図 8-4. Switching Waveforms in V_{IN} = 12V, V_{OUT} = 12V, I_O = 3A, FPWM

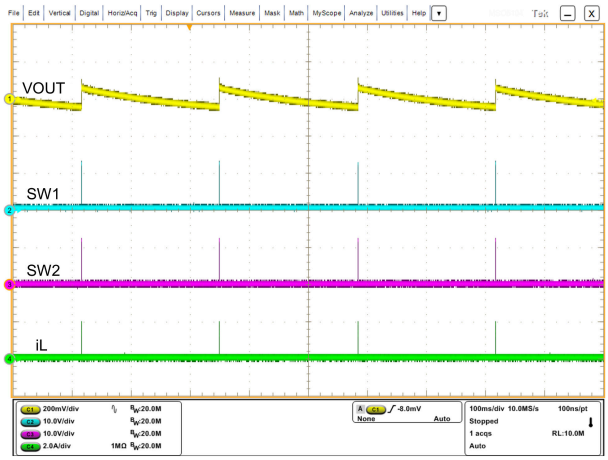


図 8-5. Switching Waveforms in V_{IN} = 12V, V_{OUT} = 12V, I_O = 0A, PFM

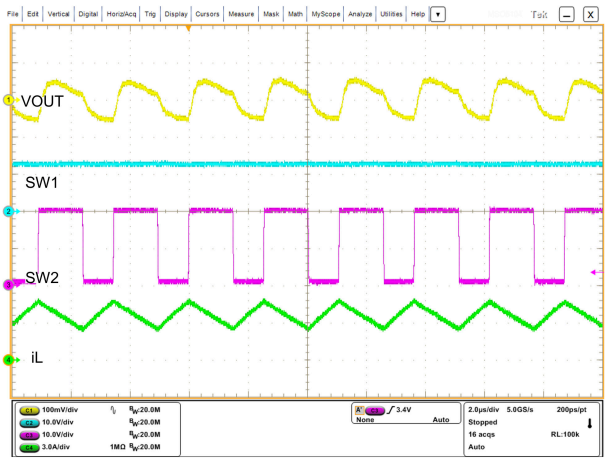


図 8-6. Switching Waveforms in V_{IN} = 12V, V_{OUT} = 20V, I_O = 2A, FPWM

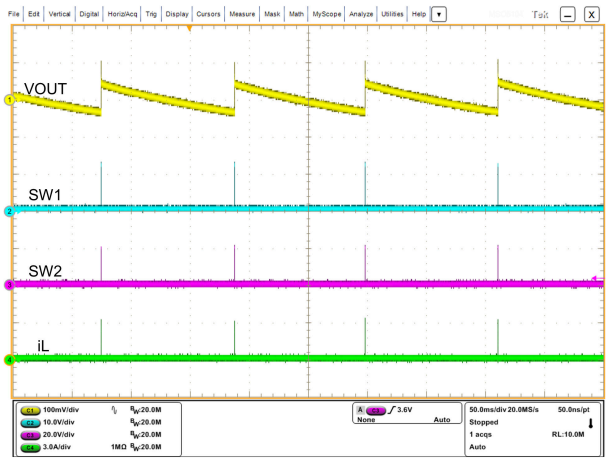


図 8-7. Switching Waveforms in V_{IN} = 12V, V_{OUT} = 20V, I_O = 0A, PFM

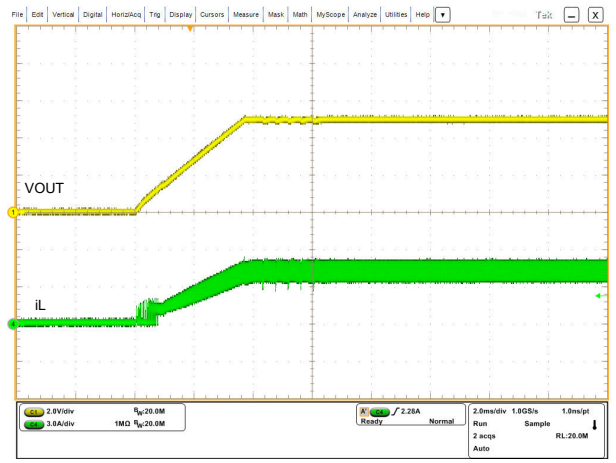


図 8-8. Start-up Waveforms in V_{IN} = 12V, V_{OUT} = 5V, R_{LOAD} = 1.2Ω, FPWM

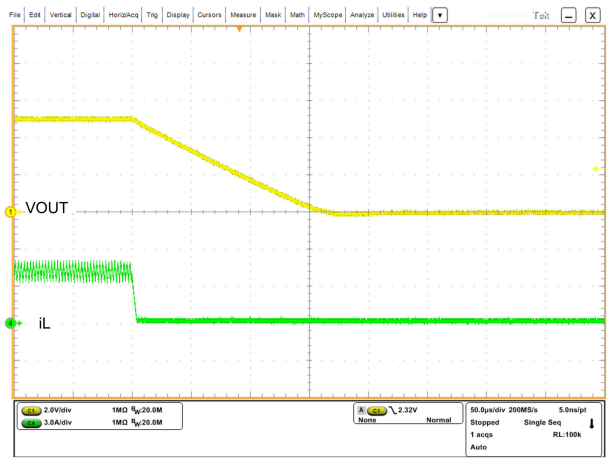


図 8-9. Shutdown Waveforms in V_{IN} = 12V, V_{OUT} = 5V, R_{LOAD} = 1.2Ω, FPWM

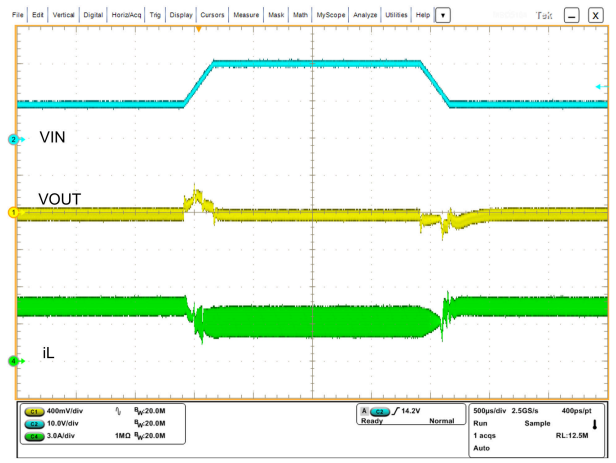


図 8-10. Line Transient Waveforms in V_{IN} = 9V to 20V, V_{OUT} = 12V, I_O = 3A with 200µs Slew Rate, FPWM

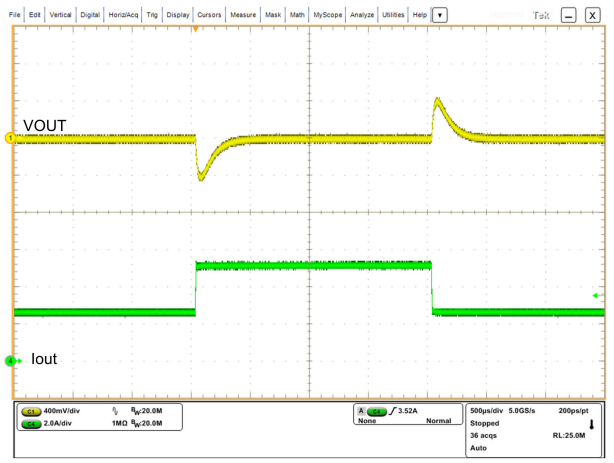


図 8-11. Load Transient Waveforms in V_{IN} = 12V, V_{OUT} = 5V, I_O = 2.5A to 5A with 20µs Slew Rate, FPWM

図 8-12. 3A Output Current Limit Waveforms in V_{IN} = 12V, V_{OUT} = 5V, R_{LOAD} = 1Ω, R_{SNS} = 10mΩ FPWM

8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 3.0V to 36V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. A typical choice is an aluminum electrolytic capacitor with a value of 100µF.

8.4 Layout

8.4.1 Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If layout is not carefully done, the regulator can suffer from instability and noise problems.

1. Place the 0.1-µF small package (0402) ceramic capacitors close to the VIN/VOUT pins to minimize high frequency current loops. This improves the radiation of high-frequency noise (EMI) and efficiency.
2. Use multiple GND vias near PGND pin to connect the PGND to the internal ground plane. This also improves thermal performance.
3. Minimize the SW1 and SW2 loop areas as these are high dv/dt nodes. Use a ground plane under the switching regulator to minimize interplane coupling.
4. Use Kelvin connections to RSENSE for the current sense signals ISP and ISN and run lines in parallel from the RSENSE terminals to the IC pins. Place the filter capacitor for the current sense signal as close to the IC pins as possible.
5. Place the BOOT1 bootstrap capacitor close to the IC and connect directly to the BOOT1 to SW1 pins. Place the BOOT2 bootstrap capacitor close to the IC and connect directly to the BOOT2 and SW2 pins.
6. Place the VCC capacitor close to the IC with wide and short trace. The GND terminal of the VCC capacitor should be directly connected with PGND plane through three to four vias.
7. Isolate the power ground from the analog ground. The PGND plane and AGND plane are connected at the terminal of the VCC capacitor. Thus the noise caused by the MOSFET driver and parasitic inductance does not interface with the AGND and internal control circuit.
8. Place the compensation components as close to the COMP pin as possible. Keep the compensation components, feedback components, and other sensitive analog circuitry far away from the power components, switching nodes SW1 and SW2, and high-current trace to prevent noise coupling into the analog signals.
9. To improve thermal performance, it is recommended to use thermal vias beneath the TPS55289-Q1 connecting the VIN pin to a large VIN area, and the VOUT pin to a large VOUT area separately.

8.4.2 Layout Example

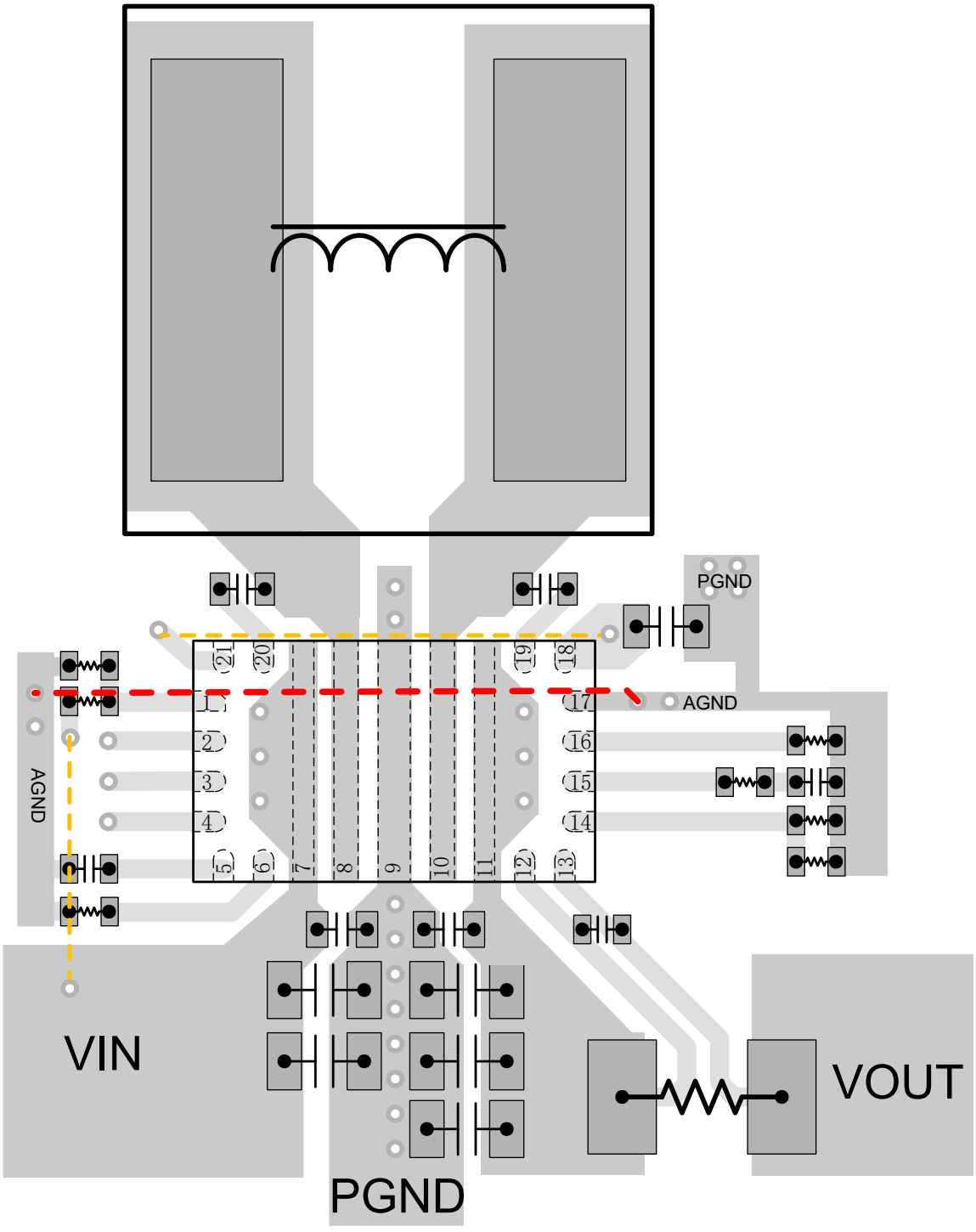


図 8-13. Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

9.1.2 Development Support

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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9.4 Trademarks

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9.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

DATE	REVISION	NOTES
December 2023	*	Initial release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS55289QWRYQRQ1	ACTIVE	VQFN-HR	RYQ	21	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	S55289Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS55289-Q1 :

- Catalog : TPS55289

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GENERIC PACKAGE VIEW

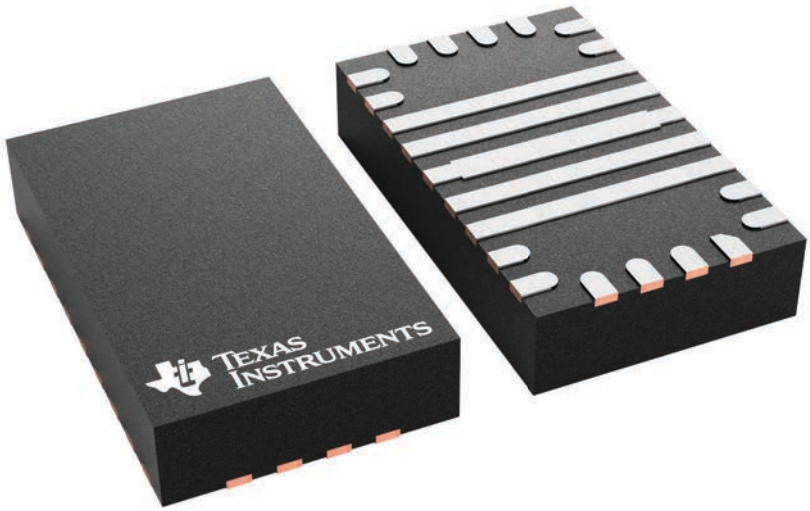
RYQ 21

VQFN - 1 mm max height

5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



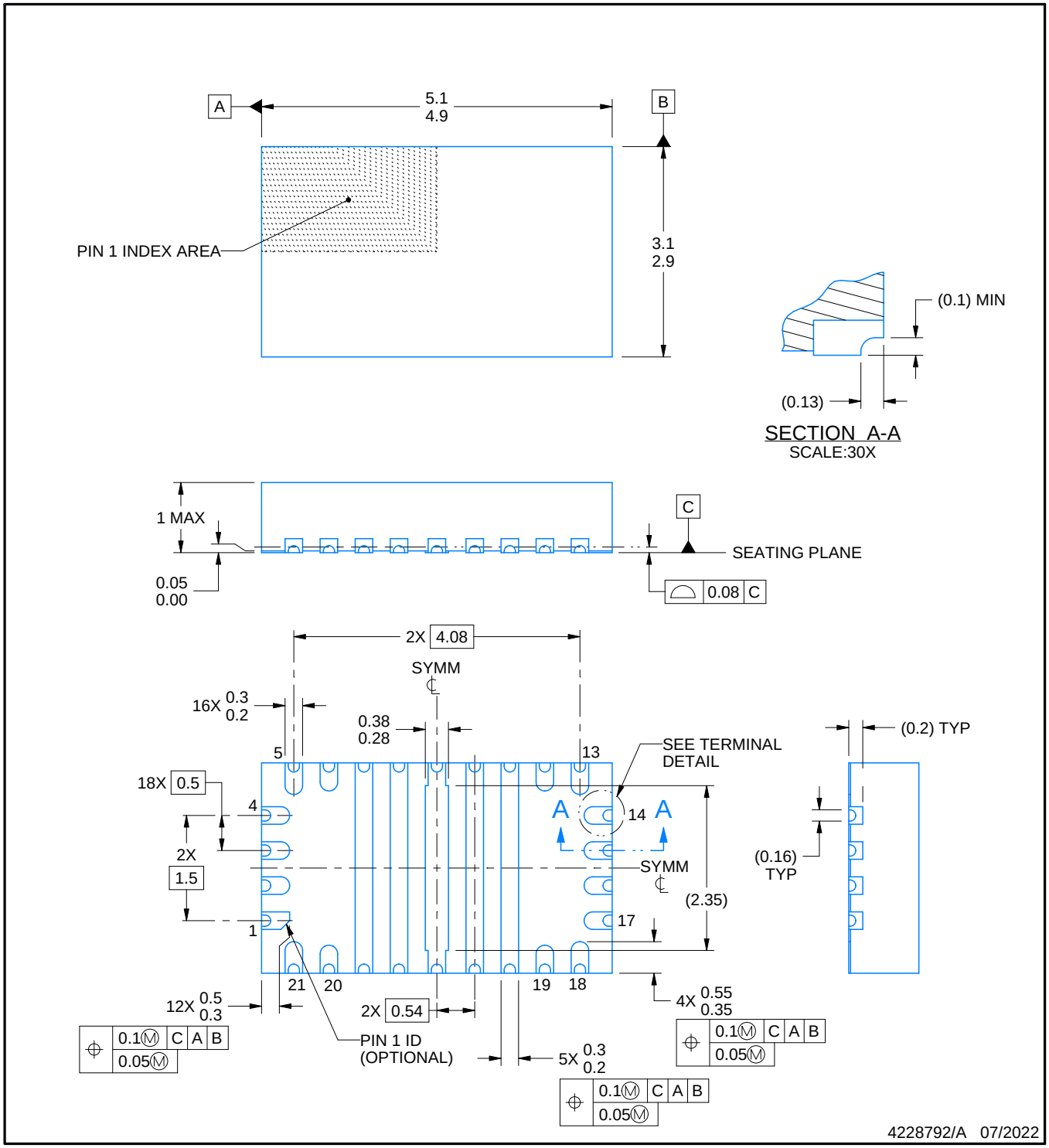
4228970/A

PACKAGE OUTLINE

RYQ0021B

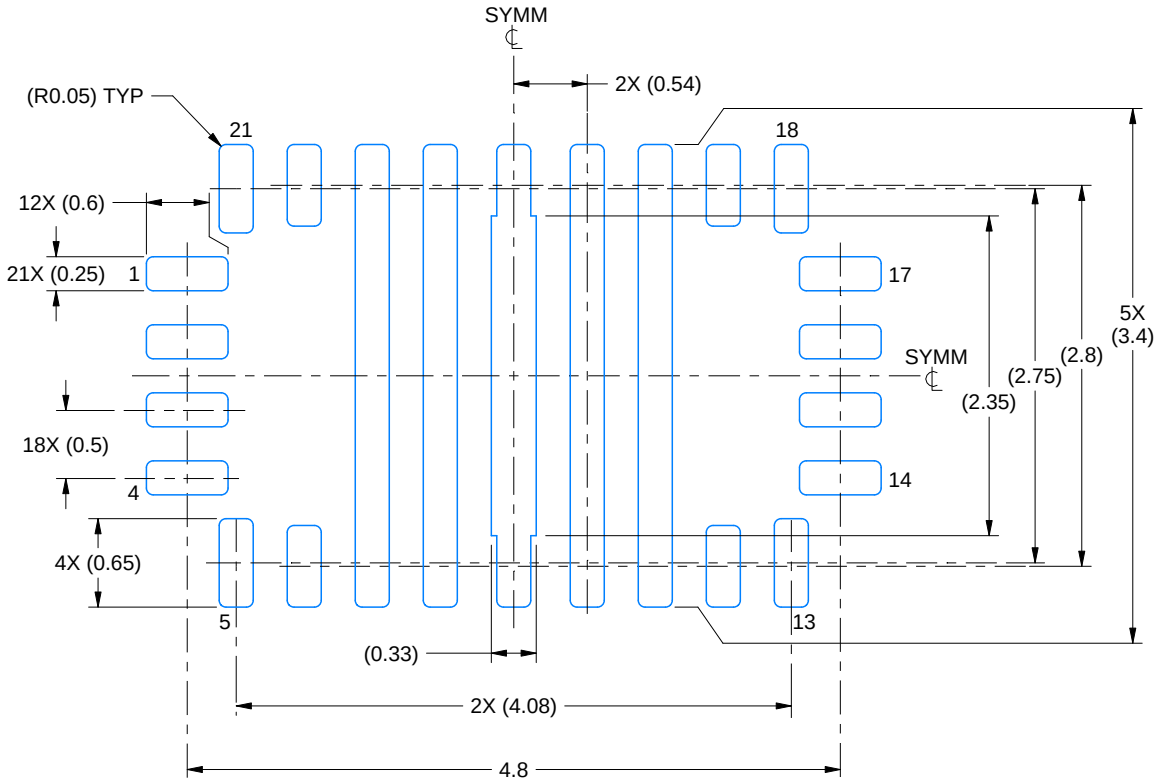
VQFN - 1.0 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

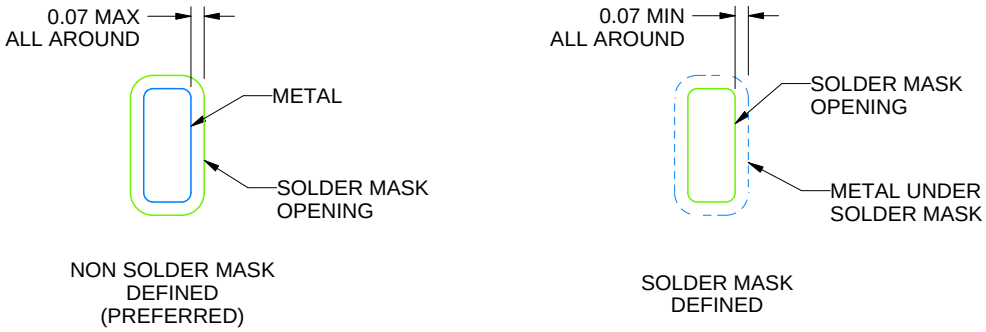


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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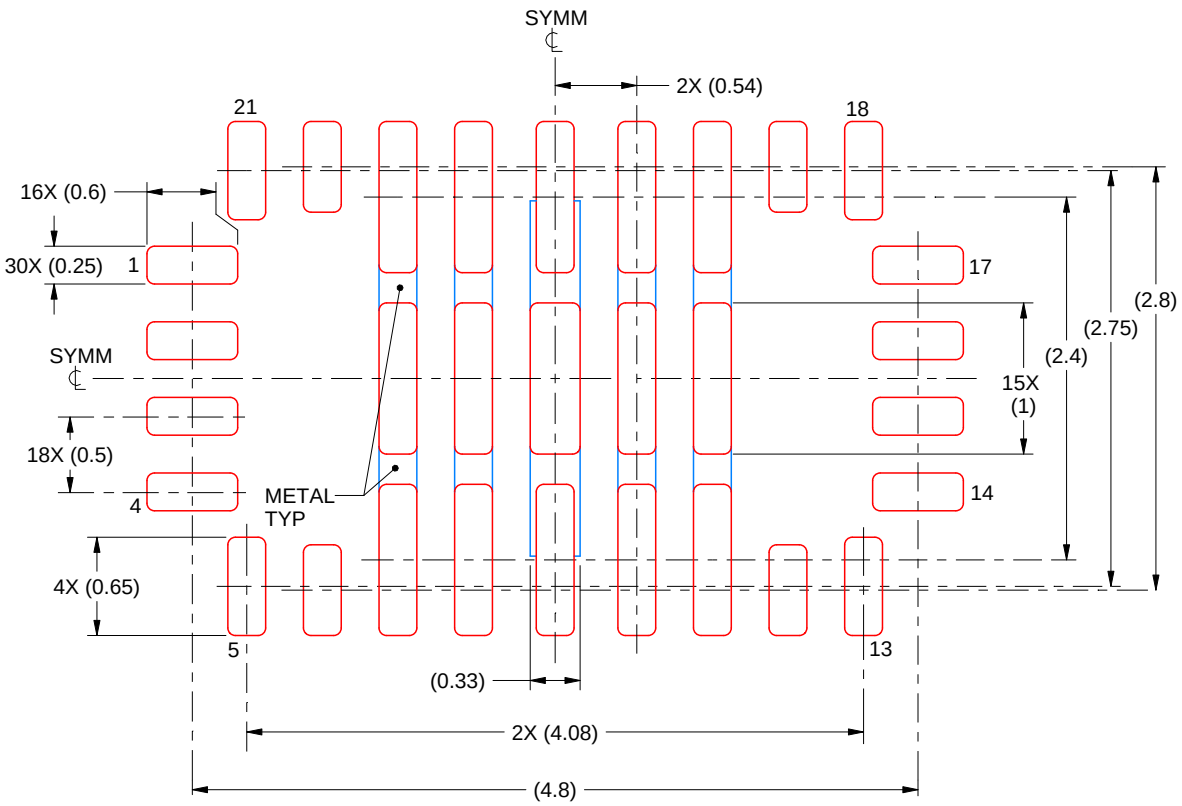
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PIN 7,8, 10 & 11 SOLDER COVERAGE = 88%
PIN 9 SOLDER COVERAGE = 64%
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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