TPS56339 4.5V～24V 入力、3A 出力の同期整流降圧コンバータ

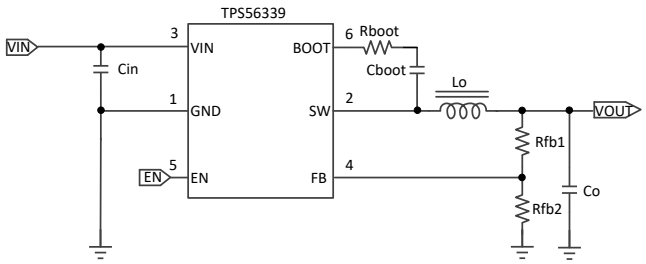
1 特長

- 入力電圧範囲: 4.5V～24V
- 出力電圧範囲: 0.8V～16V
- 最大連続出力電流：3A
- 500kHz の固定スイッチング周波数
- 最大 97% のデューティ・サイクルをサポート
- 70mΩ/35mΩ の MOSFET を内蔵
- 標準 3μA のシャットダウン電流
- 標準 98μA の静止電流
- 5ms の内部ソフトスタート
- 内部ループ補償により使用が簡単
- ハイサイドとローサイド両方の MOSFET でサイクル単位の電流制限
- ラッチなしの UVP、UVLO、および TSD 保護
- SOT-23 (6) パッケージ
- WEBENCH® Power Designer により、TPS56339 を使用するカスタム設計を作成

2 アプリケーション

- 12V、19V の分散パワー・バス電源
- 産業用アプリケーション
  - ビデオ監視およびセキュリティ・システム
  - 家電製品
- 消費者向けアプリケーション
  - デジタル TV および LCD モニタ
  - ワイヤレスおよびインテリジェント・スピーカー

概略回路図



3 概要

TPS56339 は入力電圧範囲が 4.5V～24V で、3A の同期整流降圧コンバータです。このデバイスには 2 つの内蔵スイッチング MOSFET、内部的なループ補償、および 5ms の内部ソフトスタートが搭載されているため、部品数を減らすことができます。SOT-23 (6) パッケージの採用により、高い電力密度を実現し、PCB 上でわずかな面積しか占有しません。

TPS56339 は高度なエミュレート電流モード (AECM) 制御を採用しているため、固定周波数で高速な過渡応答が得られます。内部の適応型ループ調整により、広い出力電圧範囲にわたって外部補償が不要です。

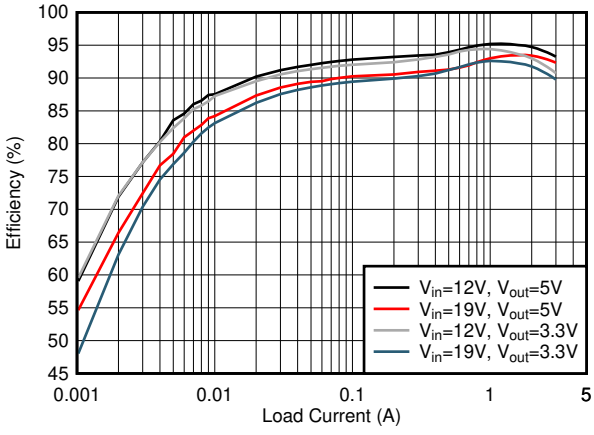
ハイサイドにサイクル単位の電流制限を適用してデバイスを電流過負荷状態から保護し、ローサイドのソース電流制限で電流暴走を防ぐことによって、さらに保護を強化しています。低電圧およびサーマル・シャットダウン保護状態になると、ヒカップ保護が作動します。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS56339	SOT-23 (6)	1.60mm×2.90mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

TPS56339 の効率



目次

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 改訂履歴 ... 2
5 **Pin Configuration and Functions** ... 3
6 **Specifications** ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Timing Requirements ... 5
6.7 Typical Characteristics ... 6
7 **Detailed Description** ... 9
7.1 Overview ... 9
7.2 Functional Block Diagram ... 10
7.3 Feature Description ... 11
7.4 Device Functional Modes ... 14
7.5 Light-Load Operation ... 14
8 **Application and Implementation** ... 15
8.1 Application Information ... 15
8.2 Typical Application ... 15
9 **Power Supply Recommendations** ... 21
10 **Layout** ... 22
10.1 Layout Guidelines ... 22
10.2 Layout Example ... 22
11 デバイスおよびドキュメントのサポート ... 24
11.1 ドキュメントの更新通知を受け取る方法 ... 24
11.2 関連リンク ... 24
11.3 コミュニティ・リソース ... 24
11.4 商標 ... 24
11.5 静電気放電に関する注意事項 ... 24
11.6 Glossary ... 24
12 メカニカル、パッケージ、および注文情報 ... 24

4 改訂履歴

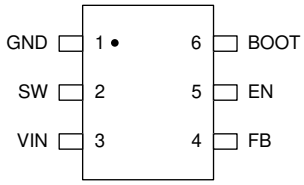
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2018年11月発行のものから更新 **Page**

- マーケティング・ステータスを「事前情報」から「初版」に 変更 ... 1

5 Pin Configuration and Functions

DDC Package
6-Pin SOT
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
BOOT	6	O	A 30-Ω boot resistor and a 0.1-μF bootstrap cap are required between BOOT and SW. The voltage on this cap carries the gate drive voltage for the high-side MOSFET.
EN	5	I	Enable pin. Float to enable. Adjust the input undervoltage lockout with two resistors.
FB	4	I	Converter feedback input. Connect to output voltage with feedback resistor divider.
GND	1	G	Ground pin. Source terminal of low-side MOSFET as well as the ground terminal for controller circuit. Connect sensitive FB to this GND at a single point.
SW	2	O	Switch node connection between high-side MOSFET and low-side MOSFET.
VIN	3	I	Input voltage supply pin. The drain terminal of high-side MOSFET.

(1) I = Input, O = Output, G = GND

6 Specifications

6.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to +125°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltages	VIN	–0.3	26	V
	EN	–0.3	6	
	BOOT	–0.3	SW+6	
	FB	–0.3	6	
Output voltages	BOOT-SW	–0.3	6	V
	SW	–0.3	26	
	SW (<10 ns transient)	–3	26	
T_J	Operating junction temperature(2)	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Operating at junction temperatures greater than 125°C, although possible, degrades the lifetime of the device.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to +125°C (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input voltage	V_{IN}	4.5		24	V
	EN	–0.1		5.5	V
	FB	–0.1		5.5	V
Output voltage	BOOT-SW	–0.1		5.5	V
	SW	–0.1		24	V
Ouput Current	I_{OUT}	0		3	A
Temperature	Operating junction temperature, T_J	–40		125	°C

(1) Conditions for which the device is intended to be functional, but do not ensure specific performance limits.

6.4 Thermal Information

THERMAL METRIC(1)		TPS56339 DDC (SOT23) 6 PINS	UNIT
$R_{\theta JA}$(2)(3)	Junction-to-ambient thermal resistance	119.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953
(2) The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were simulated on a standard JEDEC board. They do not represent the performance obtained in an actual application.
(3) The real $R_{\theta JA}$ on TPS56339EVM is about 62.4 ℃/W, test condition: V_{IN} = 19 V, V_{OUT} = 5 V, I_{OUT} = 3 A, T_A = 25 ℃.

Thermal Information (continued)

THERMAL METRIC(1)		TPS56339 DDC (SOT23) 6 PINS	UNIT
Ψ_{JT}	Junction-to-top characterization parameter	9.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	36.2	°C/W

6.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25 °C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 4.5 V to 24 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VIN PIN)						
V_{IN}	Operation input voltage		4.5		24	V
I_Q	Non switching quiescent current	First power on with no load, then force V_{FB} to 1.2 V, V_{IN} = 12 V		98		µA
I_{SHDN}	Shutdown supply current	V_{IN} = 12 V, V_{EN} = 0 V		3		µA
VIN_UVLO	Undervoltage lockout thresholds	VIN Rising threshold	3.9	4.2	4.4	V
VIN_UVLO		VIN Falling threshold	3.5	3.7	3.9	V
ENABLE (EN PIN)						
V_{EN_RISE}	Enable threshold	EN rising threshold		1.18	1.28	V
V_{EN_FALL}		EN falling threshold	1.08	1.12		V
I_{EN_INPUT}	Input current	V_{EN} = 1.0 V		1.2		µA
I_{EN_HYS}	Hysteresis current	V_{EN} = 1.5 V		3.1		µA
VOLTAGE REFERENCE (FB PIN)						
V_{REF}	Reference voltage	T_J = 25 °C	0.790	0.802	0.814	V
		T_J = -40 °C to 125 °C	0.782	0.802	0.822	V
INTEGRATED MOSFETS						
$R_{DS\_ON\_HS}$	High-side MOSFET On-resistance	T_J = 25 °C, $V_{BOOT-SW}$ = 5 V		70		mΩ
$R_{DS\_ON\_LS}$	Low-side MOSFET On-resistance	T_J = 25 °C, V_{IN} = 12 V		35		mΩ
CURRENT LIMIT						
I_{HS_LIMIT}	High-side MOSFET current limit		3.9	4.7	5.4	A
I_{LS_LIMIT}	Low-side MOSFET current limit	V_{IN} = 12 V	2.7	3.6	4.7	A
OUTPUT UNDERVOLTAGE PROTECTION						
V_{UVP_HYS}	Output UVP threshold	Hiccup detect (H→L)		62.5		%
	Hysteresis			5		%
BOOT UVLO						
$V_{BOOT-SW}$	BOOT UVLO threshold			2.2		V
OSCILLATOR						
f_{SW}	Switching frequency		420	500	600	KHz
THERMAL SHUTDOWN						
T_{SHDN}(1)	Thermal shutdown threshold			160		°C
T_{HYS}(1)	Hysteresis			20		°C

(1) Not production tested

6.6 Timing Requirements

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25 °C, and are provided for reference purposes only. Unless otherwise stated, the following

Timing Requirements (continued)

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25 °C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 4.5 V to 24 V.

conditions apply: V_{IN} = 4.5 V to 24 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ON TIMER CONTROL						
T_{ON_MIN} (1)	Minimum on time			55		ns
T_{ON_MAX}	Maximum on time			5		µs
T_{OFF_MIN}	Minimum off time			115		ns
SOFT START						
T_{SS}	Internal soft-start time			5		ms
OUTPUT UNDERVOLTAGE PROTECTION						
T_{HIC_WAIT}	Hiccup on time			120		µs
T_{HIC_RE}	Hiccup time before restart			38		ms

(1) Not production tested

6.7 Typical Characteristics

V_{IN} = 12 V (unless otherwise noted)

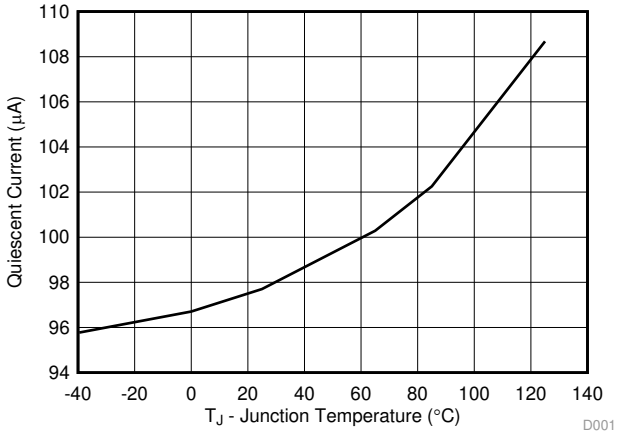


図 1. Quiescent Current VS Junction Temperature

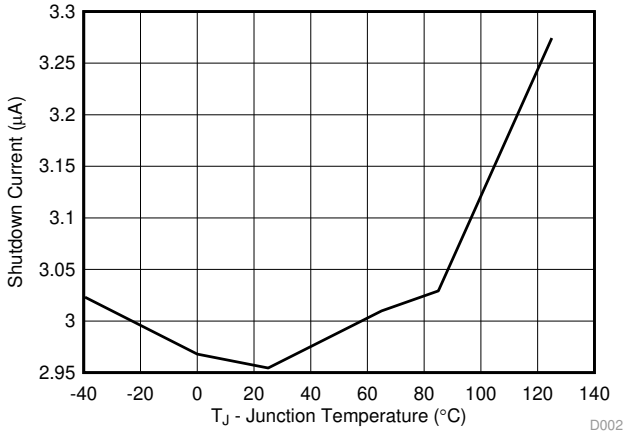


図 2. Shutdown Current VS Junction Temperature

Typical Characteristics (continued)

V_{IN} = 12 V (unless otherwise noted)

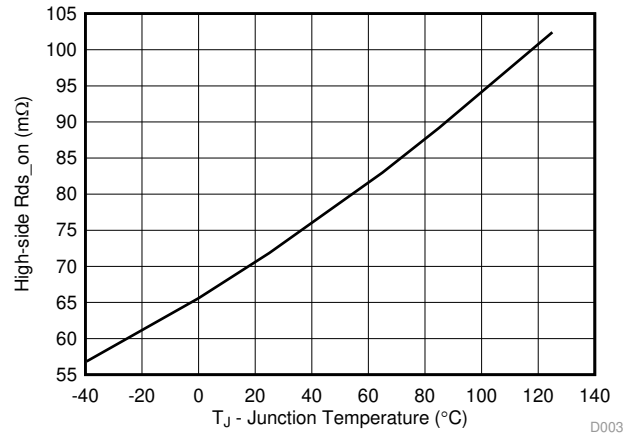


図 3. High-side R_{ds-On} VS Junction Temperature

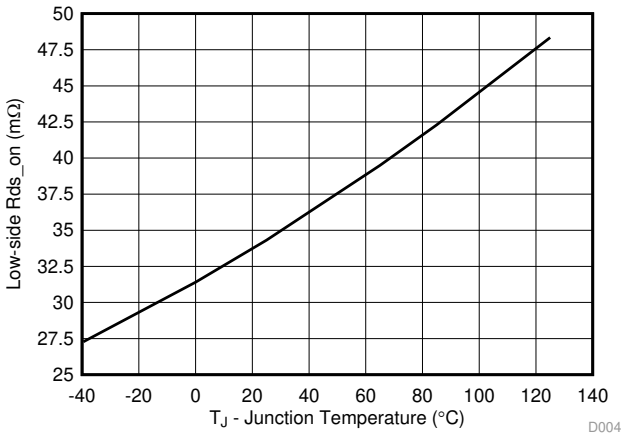


図 4. Low-side R_{ds-On} VS Junction Temperature

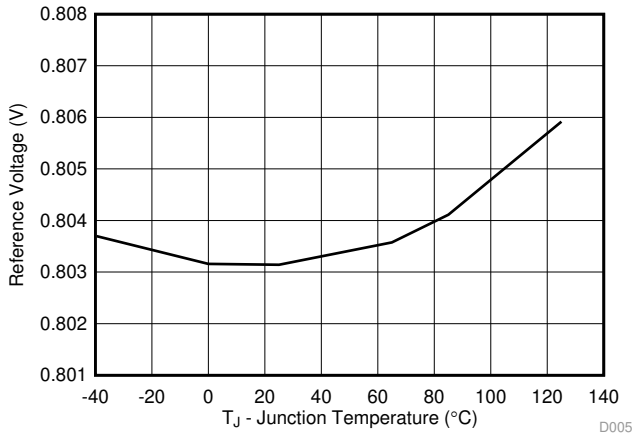


図 5. Reference Voltage VS Junction Temperature

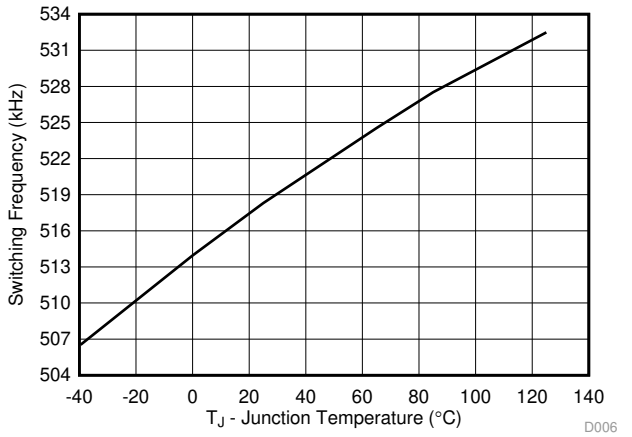


図 6. Switching Frequency VS Junction Temperature

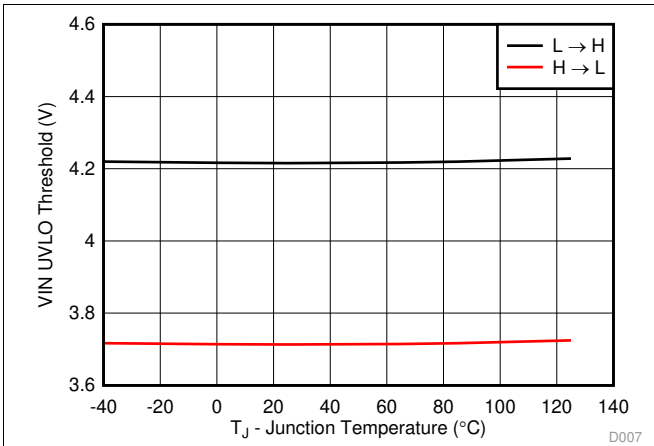


図 7. VIN UVLO Threshold VS Junction Temperature

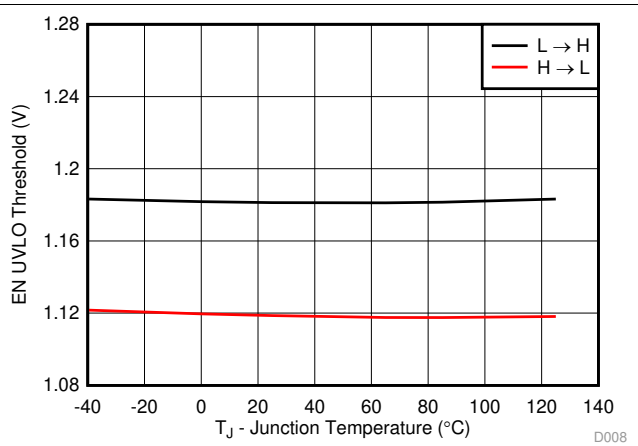


図 8. EN Threshold VS Junction Temperature

Typical Characteristics (continued)

V_{IN} = 12 V (unless otherwise noted)

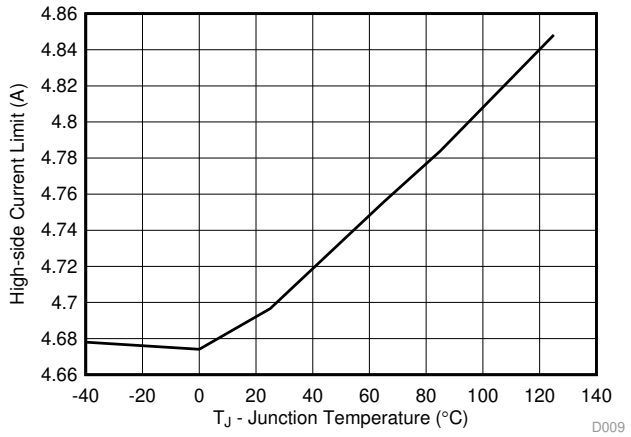


図 9. High-side Current Limit Threshold VS Junction Temperature

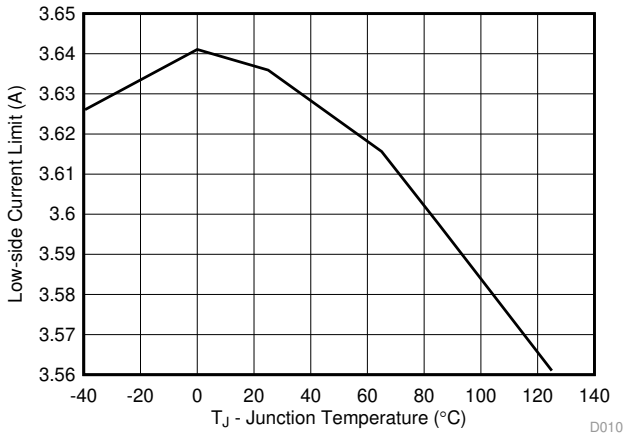


図 10. Low-side Current Limit Threshold VS Junction Temperature

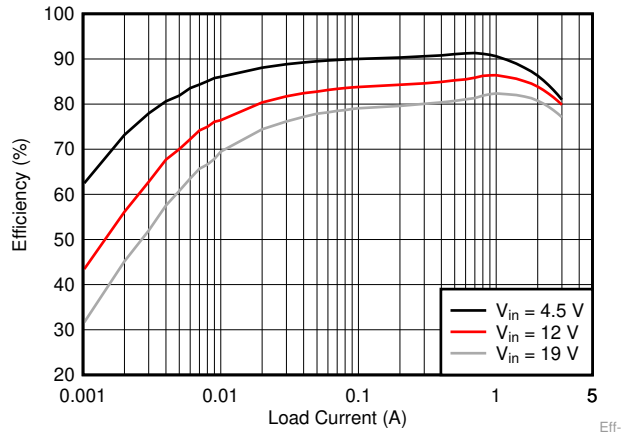


図 11. V_{OUT}=1.05 V Efficiency, L=1.5 µH

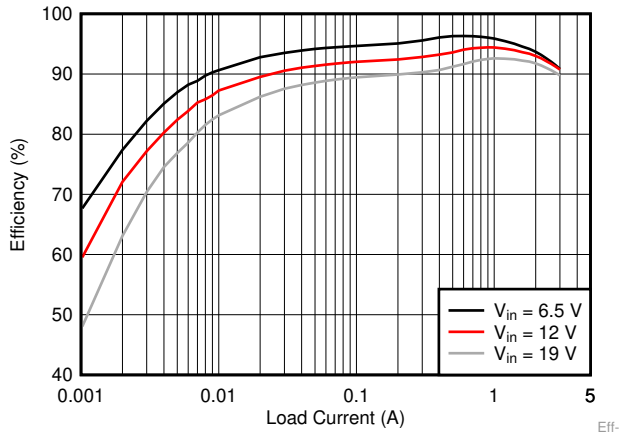


図 12. V_{OUT}=3.3 V Efficiency, L=4.7 µH

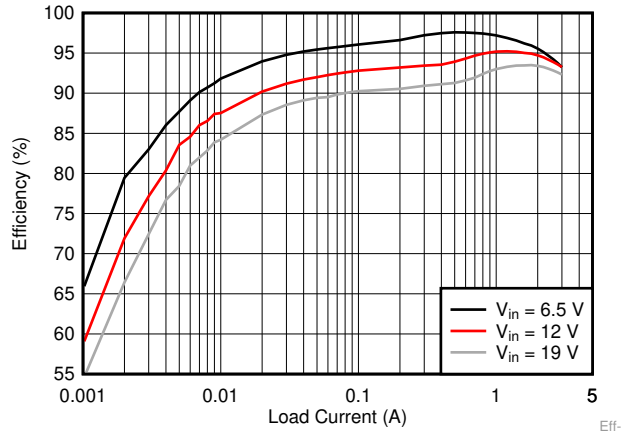


図 13. V_{OUT}=5 V Efficiency, L=5.6 µH

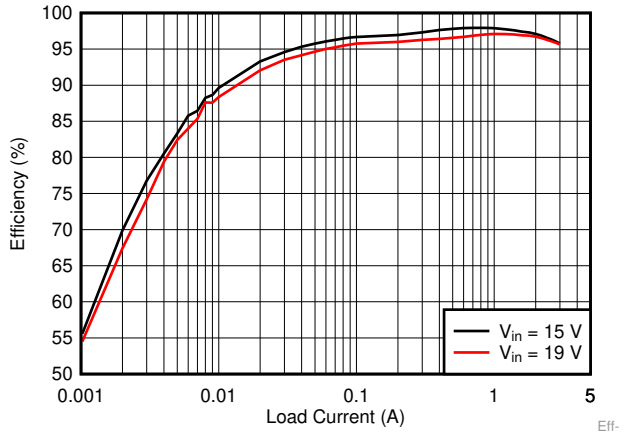


図 14. V_{OUT}=12 V Efficiency, L=6.8 µH

7 Detailed Description

7.1 Overview

The TPS56339 is a 24-V, 3-A, synchronous buck (step-down) converter with two integrated n-channel MOSFETs. The device implements an AECM control which can get fast transient response with fixed frequency. The fast transient response results in low voltage drop and the fixed frequency brings a better jitter permanence and predictable frequency for EMI design. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

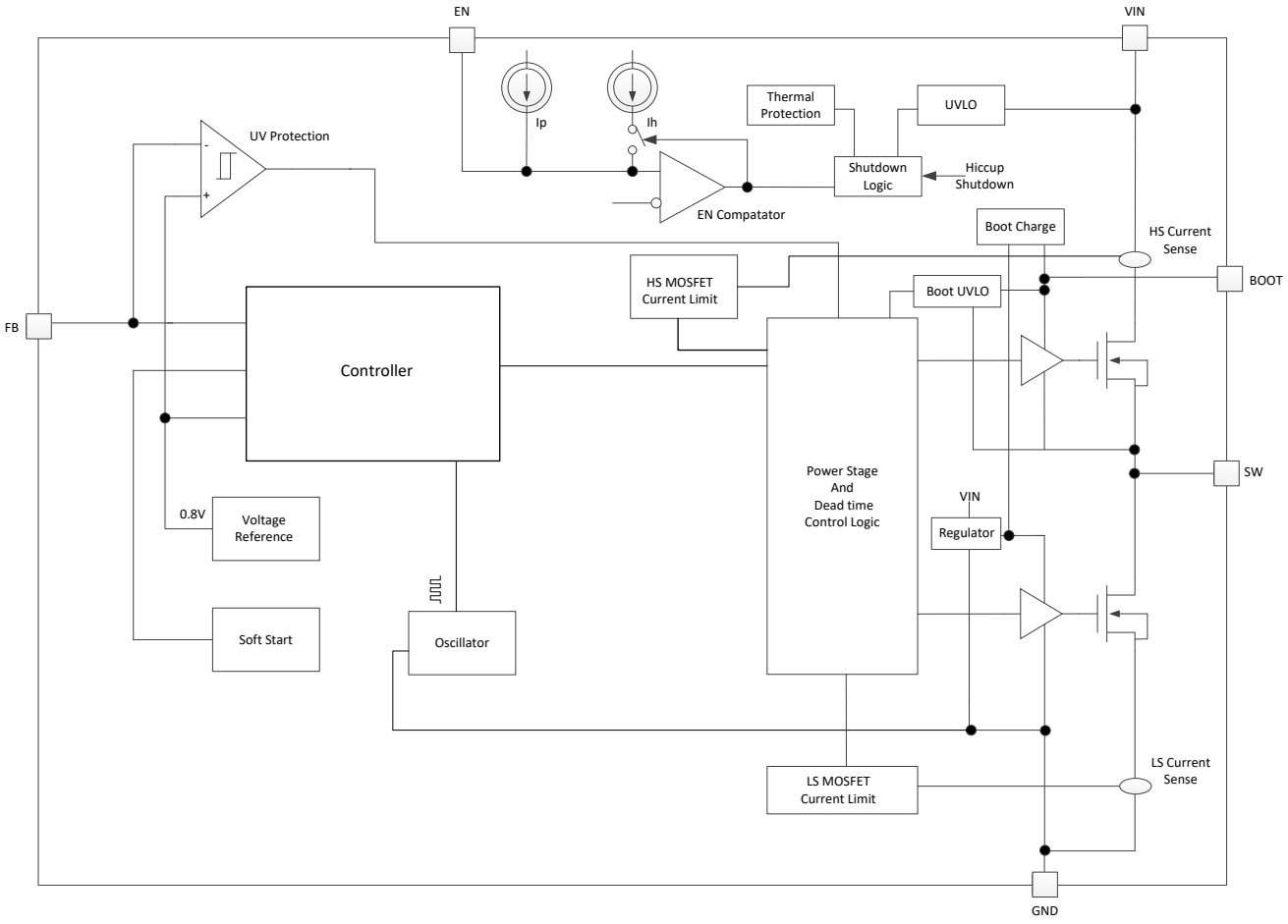
The TPS56339 is designed for safe monotonic start-up into pre-biased loads. The default start-up is when VIN is typically 4.5 V. The EN pin has an internal pull-up current source that can be used to adjust the input voltage undervoltage lockout (UVLO) with two external resistors. In addition, the EN pin can be floating for the device to operate with the internal pull-up current. The total operating current for the device is approximately 98 μA when not switching and under no load. When the device is disabled, the supply current is approximately 3 μA. The integrated 70-mΩ high-side MOSFET and 35-mΩ allow for high efficiency power supply designs with continuous output currents up to 3 A.

The TPS56339 reduces the external component count by integrating the boot recharge circuit. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BOOT and SW pins. The boot capacitor voltage is monitored by a BOOT to SW UVLO (BOOT-SW UVLO) circuit allowing SW pin to be pulled low to recharge the boot capacitor. The device has a on-time extension function with a maximum on time of 5 μs to keep the boot capacitor voltage higher than the preset BOOT-SW UVLO threshold which is typically 2.2 V. During low dropout operation, large duty cycle is needed. The high-side MOSFET could turn on up to 5 μs. Then the high-side MOSFET turns off and the low-side MOSFET turns on with a minimum off time of 115 ns, supporting a maximum duty cycle of 97%.

The TPS56339 integrates output undervoltage protection. When the regulated output voltage is lower than 62.5% of the nominal voltage due to over current triggered, the undervoltage comparator is activated. 120 μs deglitch timer later, both the high-side and low-side MOSFET turn off, the device steps into hiccup mode.

The TPS56339 has internal 5-ms soft-start time to minimize inrush currents.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Advanced Emulated Current Mode Control

The TPS56339 uses an Advanced Emulated Current Mode (AECM) control, which is an emulated current control topology. The TPS56339 uses an internal oscillator to generate clock to trigger high-side MOSFET turn on. Once the emulated inductor current ramp up trigger internal reference, the high-side MOSFET turns off and the low-side MOSFET turns on. Until the next clock coming, the low-side MOSFET turns off and the high-side MOSFET turns on again. The switching frequency is controlled by the oscillator clock and is fixed that provides ease of filter design to overcome EMI noise. The internal adaptive loop adjustment eliminates the need for external compensation over a wide voltage output range up to 16V. However, dynamic adjustment output voltage is not supported.

7.3.2 Enable and Adjusting Undervoltage Lockout

The EN pin provides electrical on and off control of the device. When the EN pin voltage exceeds the threshold voltage, the TPS56339 begins operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters the shutdown mode.

The EN pin has an internal pull-up current source which allows the user to float the EN pin to enable the device. If an application requires control of the EN pin, use open-drain or open-collector output logic to interface with the pin.

The TPS56339 implements internal undervoltage-lockout (UVLO) circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 510 mV.

If an application requires a higher UVLO threshold on the VIN pin, the EN pin can be configured as shown in 図 15. When using the external UVLO function, setting the hysteresis at a value greater than 510 mV is recommended.

The EN pin has a small pull-up current, I_p, which sets the default state of the EN pin to enable when no external components are connected. The pull-up current is also used to control the voltage hysteresis for the UVLO function because it increases by I_h when the EN pin crosses the enable threshold. Use 式 1 , and 式 2 to calculate the values of R1 and R2 for a specified UVLO threshold. Once R1, R2 were settled down, the V_{EN} voltage can be calculated by 式 3, which should be lower than 5.5V with max V_{IN}.

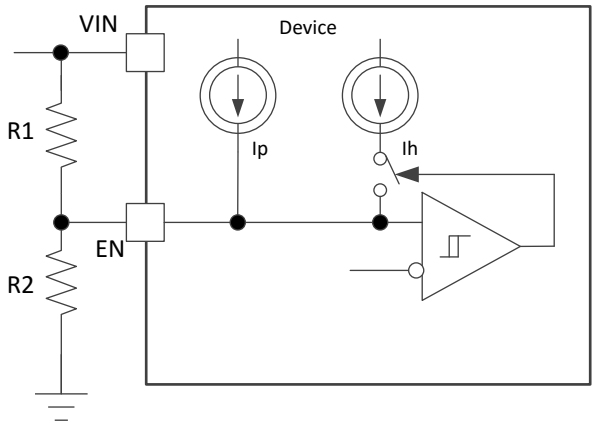


図 15. Adjustable VIN Undervoltage Lockout

$$R_1 = \frac{V_{SATART}\frac{V_{EN\_FALL}}{V_{EN\_RISE}} - V_{STOP}}{I_p\left(1 - \frac{V_{EN\_FALL}}{V_{EN\_RISE}}\right) + I_h} \quad (1)$$

Feature Description (continued)

$$R_2 = \frac{R_1 \cdot V_{EN\_FALL}}{V_{STOP} - V_{EN\_FALL} + R_1 \cdot \left(I_p + I_h\right)} \quad (2)$$

$$V_{EN} = \frac{R_2 \cdot V_{IN} + R_1 R_2 \left(I_p + I_h\right)}{R_1 + R_2}$$

where

- I_p = 1.2 µA
- I_h = 3.1 µA
- V_{EN_FALL} = 1.12 V
- V_{EN_RISE} = 1.18 V
- V_{SATRT}, the input voltage enabling the device
- V_{STOP}, the input voltage disabling the device (3)

7.3.3 Soft Start and Pre-Biased Soft Start

The TPS56339 has an internal 5-ms soft-start. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator.

The TPS56339 has been designed to prevent the low-side MOSFET from discharging a pre-biased output. During monotonic pre-biased startup, both high-side and low-side MOSFET are not allowed to be turned on until the internal soft-start voltage is higher than FB pin voltage. This scheme ensures that the converters ramp up smoothly into regulation point.

7.3.4 Voltage Reference

The voltage reference system produces a precise ±2.5% voltage reference over full temperature by scaling the output of a temperature stable bandgap circuit. The typical voltage reference is designed at 0.802 V.

7.3.5 Minimum ON-time, Minimum OFF-time and Frequency Foldback at Dropout Conditions

Minimum ON-time, T_{ON_MIN}, is the smallest duration of time that the high-side MOSFET can be on. T_{ON_MIN} is typically 55ns in the TPS56339. Minimum OFF-time, T_{OFF_MIN}, is the smallest duration that the high-side MOSFET can be off. T_{OFF_MIN} is typically 115 ns in the TPS56339. In CCM operation, T_{ON_MIN} and T_{OFF_MIN} limit the voltage conversion range given a fixed switching frequency.

The minimum duty cycle allowed is:

$$D_{MIN} = T_{ON\_MIN} \times f_{SW} \quad (4)$$

And the maximum duty cycle allowed is:

$$D_{MAX} = 1 - T_{OFF\_MIN} \times f_{SW} \quad (5)$$

In the TPS56339, a frequency foldback scheme is employed to extend the maximum duty cycle when T_{OFF_MIN} is reached. The switching frequency decreases once longer duty cycle is needed under low V_{IN} conditions. With the duty increase, the on time will increase, until up to the Maximum ON-time, 5 µs. Wide range of frequency foldback allows the TPS56339 output voltage stay in regulation with a much lower supply voltage V_{IN}. This leads to a lower effective dropout voltage.

Given an output voltage, the maximum operation supply voltage can be found by:

$$V_{IN\_MAX} = \frac{V_{OUT}}{f_{SW} \cdot T_{ON\_MIN}} \quad (6)$$

At lower supply voltage, the switching frequency decreases once T_{OFF_MIN} is triggered. The minimum V_{IN} without frequency foldback can be approximated by:

Feature Description (continued)

$$V_{IN\_MIN} = \frac{V_{OUT}}{(1\text{-}f_{SW} \cdot T_{OFF\_MIN})} \quad (7)$$

Taking considerations of power losses in the system with heavy load operation, V_{IN_MAX} is higher than the result calculated in 式 6. With frequency foldback, V_{IN_MIN} is lowered by decreased f_{SW}, as shown in 図 16 .

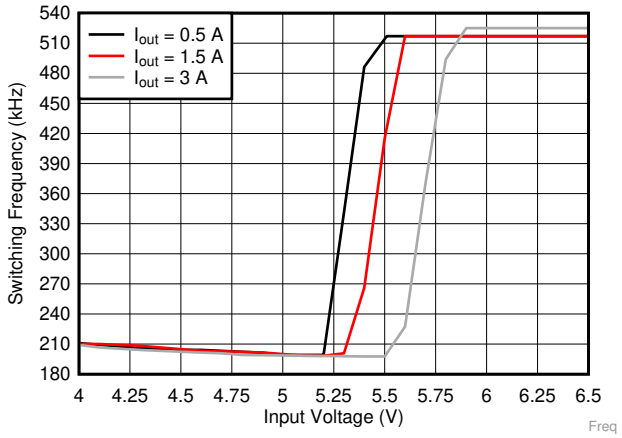


図 16. Frequency Foldback at Dropout (V_{OUT} = 5 V)

7.3.6 Overcurrent and Undervoltage Protection

The TPS56339 is protected from overcurrent conditions by cycle-by-cycle current limiting on both the peak and valley of the inductor current.

During the on time of the high-side MOSFET switch, the inductor current flow through high-side FET and increases at a linear rate determined by V_{IN}, V_{OUT}, the on-time and the output inductor value. The high-side switch current is sensed when the high-side is turned on after a set blanking time and then compared with the high-side MOSFET current limit every switching cycle. If the cross-limit event detected after the minimum On-time, the high-side MOSFET is turned off immediately and the high-side MOSFET current is limited by a clamped maximum peak current threshold I_{HS_LIMIT} which is constant.

The current going through low-side MOSFET is also sensed and monitored. When the low-side MOSFET turns on, the inductor current begins to ramp down. The low-side MOSFET is not turned OFF at the end of a switching cycle if its current is above the low-side current limit I_{LS_LIMIT}. The low-side MOSFET is kept ON for the next cycle so that inductor current keeps ramping down, until the inductor current ramps below the low-side current limit I_{LS_LIMIT} and the subsequent switching cycle comes, the low-side MOSFET is turned OFF, and the high-side MOSFET is turned on after a dead time.

There are some important considerations for this type of overcurrent protection. The load current is higher than the overcurrent threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. When the V_{FB} voltage falls below the UVP threshold voltage, the UVP comparator detects it. The device will shut down after the UVP delay time (typically 120 μs) and re-start after the hiccup time (typically 38 ms). The hiccup mode helps to reduce the device power dissipation under severe overcurrent conditions.

When the over current condition is removed, the output voltage returns to the regulated value.

7.3.7 Thermal Shutdown

The internal thermal shutdown circuitry forces the TPS56339 to stop switching if the junction temperature exceeds 160°C typically. The device reinitiates the power-up sequence when the junction temperature drops below 140°C typically.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN pin provides electrical ON and OFF control for the device. When V_{EN} is below 1.12 V (typical), the TPS56339 is in shutdown mode with a shutdown current of 3 μA (typical). The device also employs VIN UVLO protection. If VIN voltage is below their respective UVLO level, the regulator is turned off.

7.4.2 Active Mode

The TP56339 is in active mode when V_{EN} is above the precision enable threshold, V_{IN} is above its respective UVLO level. The simplest way to enable the device is to float the EN pin. This allows self startup when the input voltage is in the operating range 4.5 V to 24 V.

In active mode, depending on the load current, the device is in one of there modes:

1. Continuous Conduction Mode (CCM) with fixed switching frequency when load current is above half of the peak-to-peak inductor current ripple.

2. Discontinuous Conduction Mode (DCM) with fixed switching frequency when load current is lower than half of the peak-to-peak inductor current ripple in CCM operation.

3. Pulse Frequency Modulation Mode (PFM) when switching frequency is decreased at very light load.

7.4.3 CCM Operation

CCM operation is employed in the TPS56339 when the load current is higher than half of the peak-to-peak inductor current. In CCM operation, the frequency of operation is fixed, output voltage ripple is at a minimum in this mode, and the maximum continuous output current of 3 A can be supplied by the TPS56339.

7.5 Light-Load Operation

The light load running includes Discontinuous Conduction Mode (DCM) and Pulse Frequency Modulation Mode (PFM).

As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between CCM and DCM. The low-side MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into DCM.

At even lighter current loads, PFM is activated to maintain high efficiency operation. The On-time is kept almost the same as it was in the CCM so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in 式 8.

$$I_{OUT(LL)} = \frac{0.75^2}{2 \cdot L_1 \cdot f_{sw}} \cdot \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{V_{IN}} \quad (8)$$

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS56339 is a highly-integrated, synchronous, step-down, DC-DC converter. This device is used to convert a higher DC input voltage to a lower DC output voltage, with a maximum output current of 3 A.

8.2 Typical Application

The application schematic of 図 17 was developed to meet the requirements of the device. This circuit is available as the TPS56339EVM evaluation module. The design procedure is given in this section.

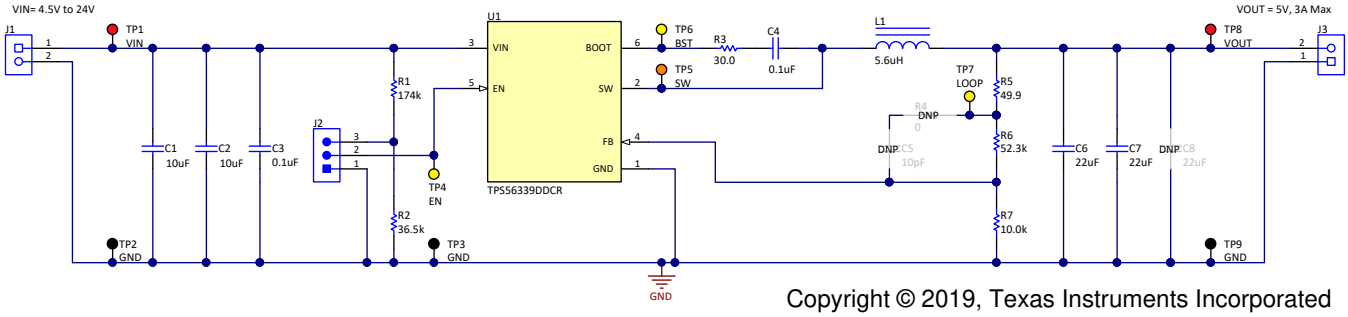


図 17. TPS56339 5-V, 3-A Reference Design

8.2.1 Design Requirements

表 1 shows the design parameters for this application.

表 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage	12 V nominal, 5.5 V to 24 V
Output voltage	5 V
Output current rating	3 A
Transient response, 2A load step	ΔV_{OUT} / V_{OUT} = ±5%
Output ripple voltage	30 mV
Input ripple voltage	300 mV
Start Input Voltage (Rising Vin)	6.6 V
Stop Input Voltage (Falling Vin)	5.7 V
Operating frequency	500 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS56339 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the FB pin. TI recommends using 1% tolerance or better divider resistors. Referring to the application schematic of 図 17, start with a 10 kΩ for R7 and use 式 9 to calculate R6. To improve efficiency at light loads consider using larger value resistors. If the values are too high the regulator is more susceptible to noise and voltage errors from the FB input current are noticeable.

$$R_6 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \cdot R_7 \tag{9}$$

表 2 shows the recommended components value for common output voltages.

8.2.2.3 Output Inductor Selection

To calculate the value of the output inductor, use 式 10. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impact the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer. For this part, TI recommends the range of K_{IND} from 30% to 50%.

$$L_{MIN} = \frac{V_{OUT}}{V_{IN\_MAX}} \cdot \frac{V_{IN\_MAX} - V_{OUT}}{K_{IND} \cdot I_{OUT} \cdot f_{SW}} \tag{10}$$

where

- I_{OUT} = 3 A, the rated output current of the device

For this design example, use K_{IND} = 50% and the inductor value is calculated to be 5.28 µH. For this design, a nearest standard value was chosen: 5.6 µH. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The inductor peak-to-peak ripple current, peak current and RMS current are calculated using 式 11, 式 12, and 式 13.

$$I_{RIPPLE} = \frac{V_{OUT}}{V_{IN\_MAX}} \cdot \frac{V_{IN\_MAX} - V_{OUT}}{L_1 \cdot f_{SW}} \tag{11}$$

$$I_{LPEAK} = I_{OUT} + \frac{I_{RIPPLE}}{2} \tag{12}$$

$$I_{LRMS} = \sqrt{I_{OUT}^2 + \frac{1}{12} I_{RIPPLE}^2} \tag{13}$$

For this design example, the calculated peak current is 4 A and the calculated RMS current is 3.03 A. The chosen inductor is a Vishay-Dale IHLP3232DZER5R6M11 5.6-µH. It has a saturation current rating of 7.6 A and a RMS current rating of 7.4 A.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

8.2.2.4 Output Capacitor Selection

After selecting the inductor, the output capacitor needs to be optimized. The LC filter used as the output filter has double pole at:

$$f_P = \frac{1}{2\pi\sqrt{L_1 \cdot C_{OUT\_E}}} \tag{14}$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180°. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. A high frequency zero introduced by internal circuit that reduces the gain roll off to –20 dB per decade and increases the phase to 90° one decade above the zero frequency. The inductor and capacitor for the output filter must be selected so that the double pole of 式 14 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement, make sure that the $L1 \cdot C_{OUT\_E}$ value meets the range of $L1 \cdot C_{OUT\_E}$ value recommended in 表 2.

表 2. Recommended Component Values

OUTPUT VOLTAGE(1) (V)	R6(2) (kΩ)	R7 (kΩ)	L1(3) (µH)	C_{OUT}(4) (µF)	Range of $L1 \cdot C_{OUT\_E}$(5) (µH×µF)
1.05	3.16	10.0	1.5	2×22	48 to 188
1.8	12.4	10.0	2.2	2×22	64 to 250
2.5	21.5	10.0	3.3	2×22	87 to 334
3.3	31.6	10.0	4.7	2×22	107 to 404
5	52.3	10.0	5.6	2×22	93 to 334
12	140	10.0	6.8	3×22	45 to 137

(1) Please use the recommended L1 and C_{OUT} combination of the higher and closest output rail for the unlisted output rails.
(2) R6 = 0 Ω for V_{OUT} = 0.8 V.
(3) Inductance values are calculated based on V_{IN}=19V, but they can also be used for other input voltages. Users can calculate their preferred inductance value per 式 10.
(4) The C_{OUT} is the sum of nominal output capacitance. Two 22-uF, 0805, 16V capacitors are recommended for $V_{OUT} \le 5V$, three 22-uF, 0805, 25VDC capacitors are recommended for $V_{OUT} > 5V$.
(5) The C_{OUT_E} is the effective value after derating, the value of $L1 \cdot C_{OUT\_E}$ should be within in the range.

The capacitor value and ESR determines the amount of output voltage ripple. TheTPS56339 is intended for use with ceramic or other low ESR capacitors. Use 式 15 to determine the required RMS current rating for the output capacitor.

$$I_{CORMS} = \frac{V_{OUT} \cdot (V_{IN\_MAX} - V_{OUT})}{\sqrt{12} \cdot V_{IN\_MAX} \cdot L_1 \cdot f_{SW}} \tag{15}$$

For this design two Murata GRM21BR61C226ME44 22-uF, 0805, 16-V output capacitors are used. From the data sheet the estimated DC derating of 51.8% at room temperature with AC voltage of 0.2V. The total output effective capacitance is approximately 22.8 µF. The value of $L1 \cdot C_{OUT\_E}$ is 127.7 µH×µF, which is within the recommended range.

8.2.2.5 Input Capacitor Selection

The TPS56339 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10 µF for the decoupling capacitor. An additional 0.1-µF capacitor (C3) from VIN pin to ground is recommended to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS56339. The input ripple current can be calculated using 式 16.

$$I_{CIRMS} = I_{OUT} \cdot \sqrt{\frac{V_{OUT}}{V_{IN\_MIN}} \cdot \frac{V_{IN\_MIN} - V_{OUT}}{V_{IN\_MIN}}} \tag{16}$$

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases. For this example design, a ceramic capacitor with at least a 35-V voltage rating is required to support the maximum input voltage. For this example, two Murata GRM21BR6YA106KE43L (10-µF, 35-V, 0805, X5R) capacitors have been selected. The effective capacitance under input voltage of 12 V for each one is 0.269 × 10 = 2.69 µF. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using 式 17. Using the design example values, I_{OUT_MAX} = 3 A, C_{IN_E} = 2 × 2.69 = 5.38 µF, f_{SW} = 500 kHz, yields an input voltage ripple of 279 mV and a RMS input ripple current of 1.48 A.

$$\Delta V_{IN} = \frac{I_{OUT\_MAX} \cdot 0.25}{C_{IN} \cdot f_{SW}} + \left(I_{OUT\_MAX} \cdot R_{ESR\_MAX}\right) \tag{17}$$

where

- R_{ESR_MAX} is the maximum series resistance of the input capacitor

8.2.2.6 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BOOT to SW pin for proper operation. TI recommends to use a ceramic capacitor with X5R or better grade dielectric. The capacitor must have a 10-V or higher voltage rating. In addition, TI recommends in series one boot resistor to make the device more robust, so a 30-Ω of R3 are required to be used between BOOT to bootstrap capacitor, C4.

8.2.3 Undervoltage Lockout Set Point

The undervoltage lockout (UVLO) can be adjusted using the external voltage divider network of R1 and R2. R1 is connected between VIN and the EN pin of the TPS56339 and R2 is connected between EN and GND . The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brownouts when the input voltage is falling. For the example design, the supply should turn on and start switching when the input voltage increases above 6.6 V (UVLO start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below 5.7 V (UVLO stop or disable). 式 1 and 式 2 can be used to calculate the values for the upper and lower resistor values. For the stop voltages specified the nearest standard resistor value for R1 is 174 kΩ and for R2 is 36.5 kΩ.

8.2.4 Application Curves

V_{IN} = 12 V, L_1= 5.6 µH, C_{OUT} = 44 µF, T_A = 25 °C. (unless otherwise noted)

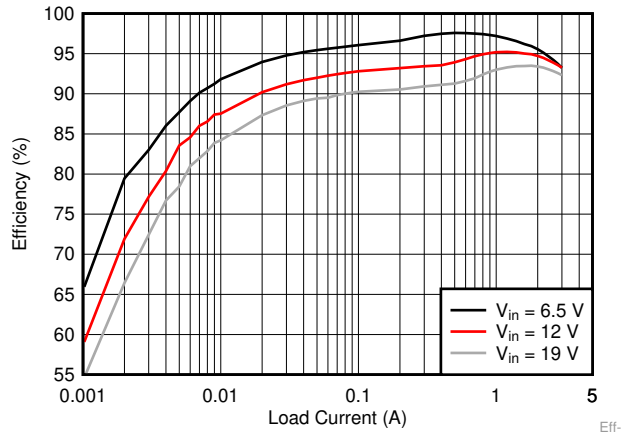


図 18. Efficiency

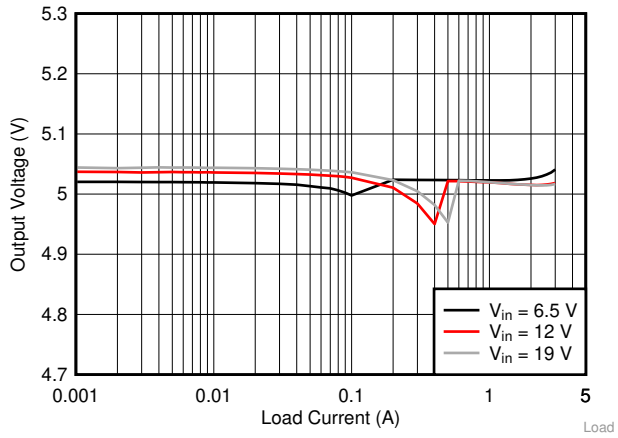


図 19. Load Regulation

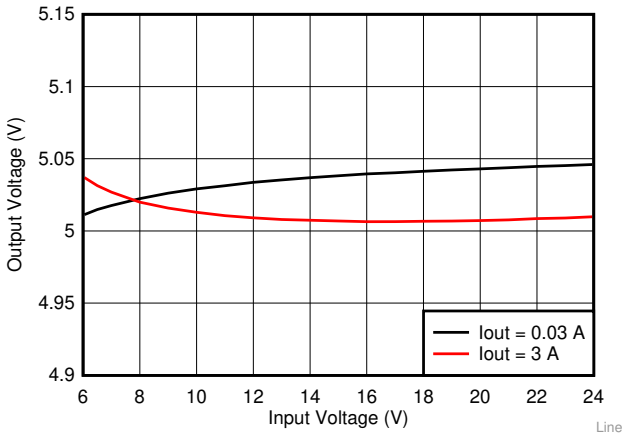


図 20. Line Regulation

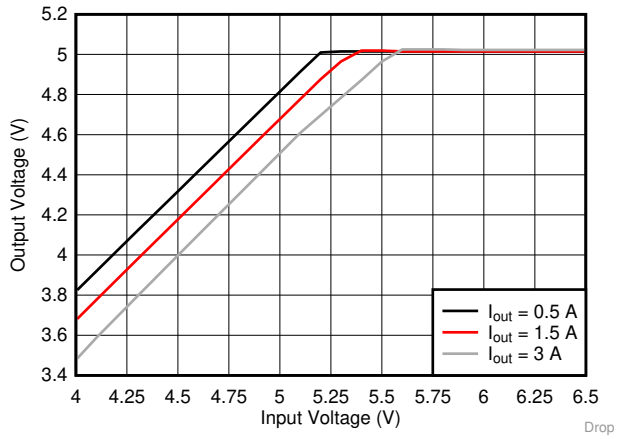


図 21. Dropout Curve

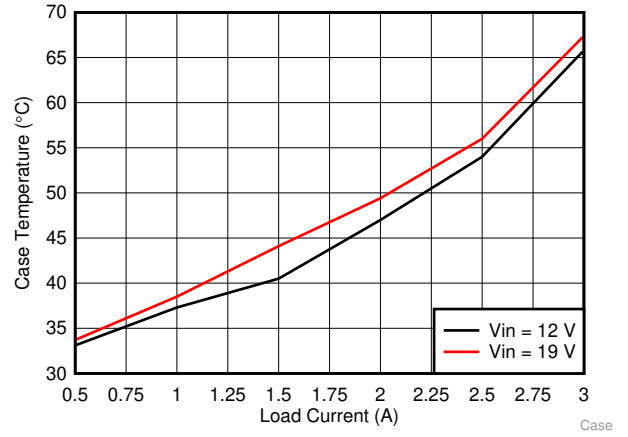


図 22. Case Temperature Rise vs Load Current

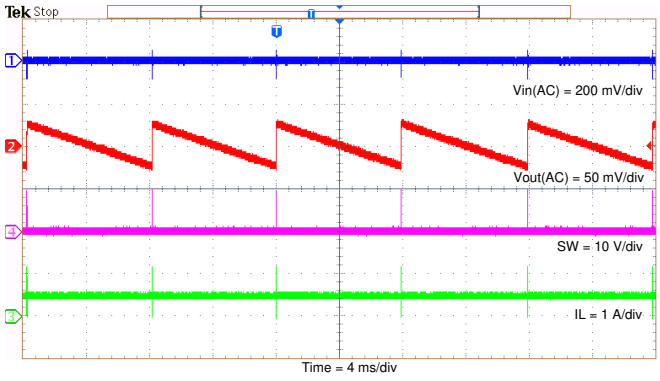


図 23. Steady State Waveforms, I_{OUT} = 0 A

V_{IN} = 12 V, L_1= 5.6 µH, C_{OUT} = 44 µF, T_A = 25 °C. (unless otherwise noted)

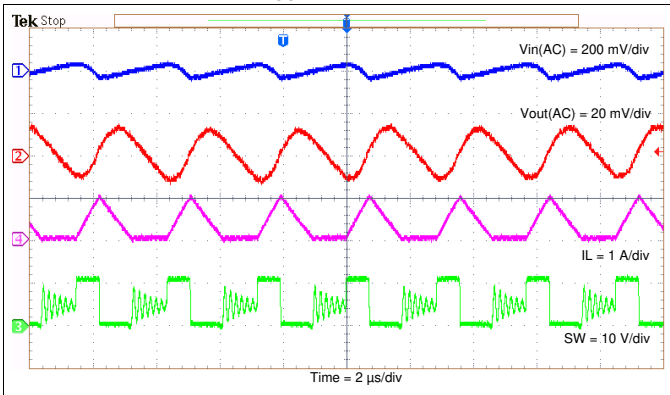


図 24. Steady State Waveforms, I_{OUT} = 0.3 A

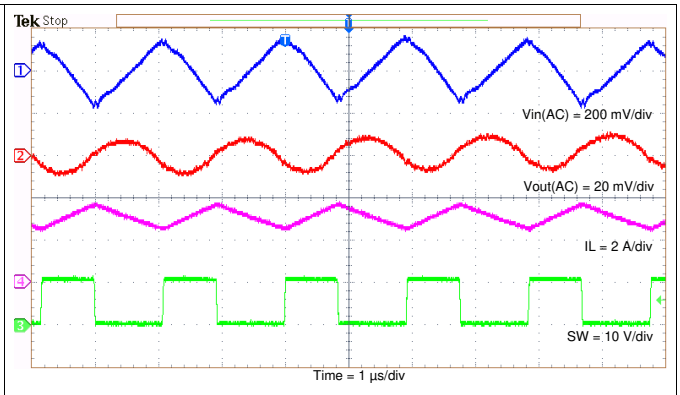


図 25. Steady State Waveforms, I_{OUT} = 3 A

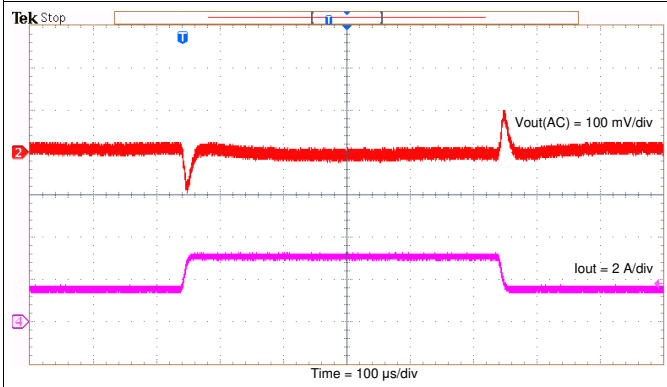


図 26. Transient Response 1.5 to 3 A

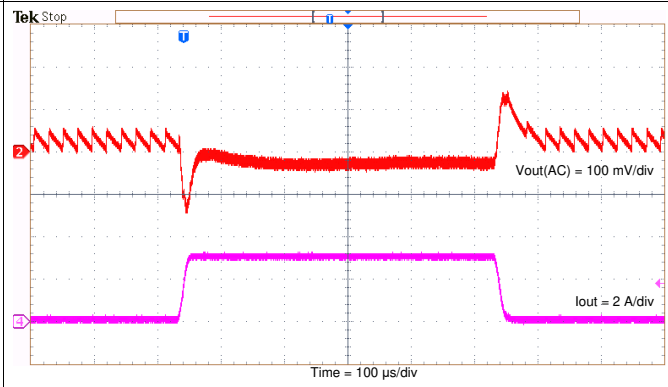


図 27. Transient Response 0.3 to 2.7 A

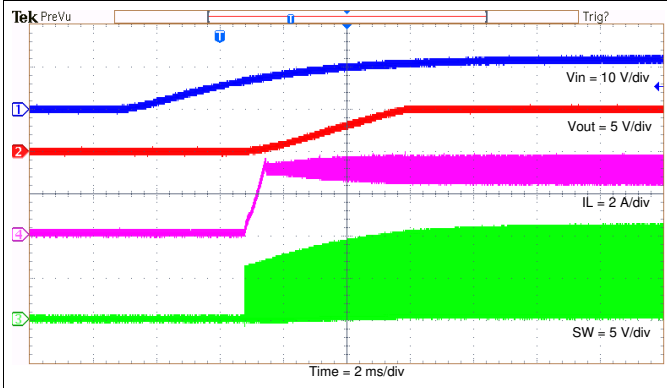


図 28. Startup Relative to V_{IN}

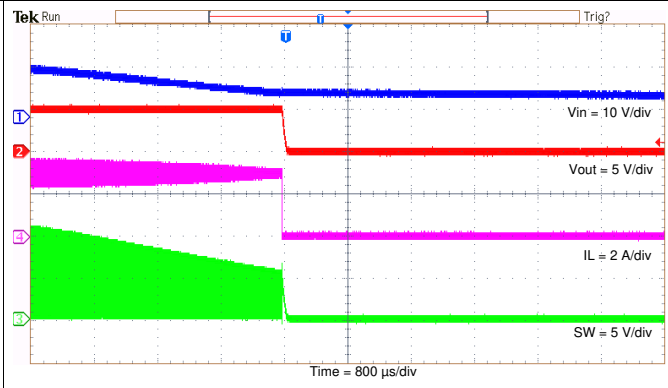


図 29. Shutdown Relative to V_{IN}

V_{IN} = 12 V, L_1= 5.6 µH, C_{OUT} = 44 µF, T_A = 25 °C. (unless otherwise noted)

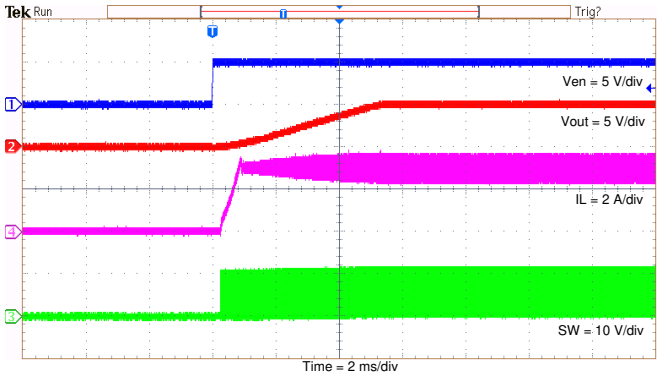


図 30. Enable Relative to EN

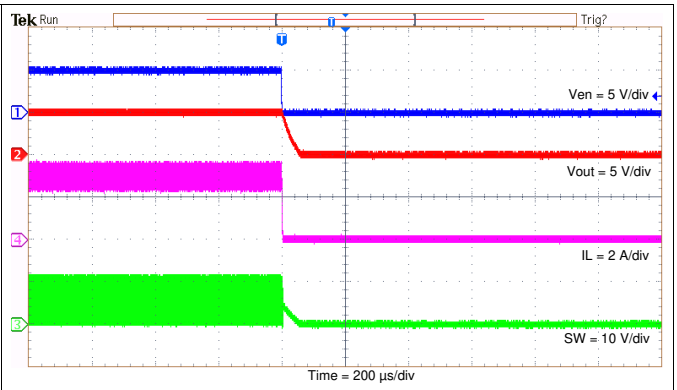


図 31. Disable Relative to EN

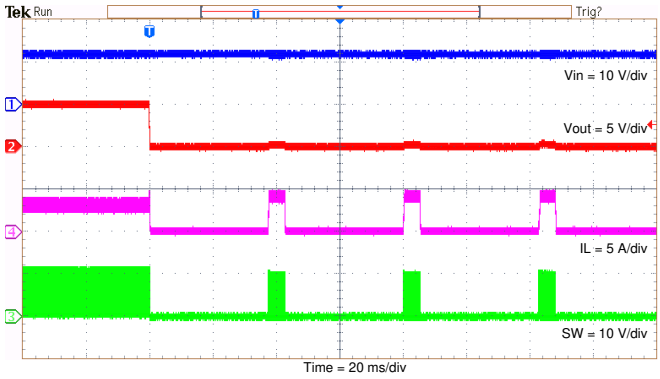


図 32. Short Protection

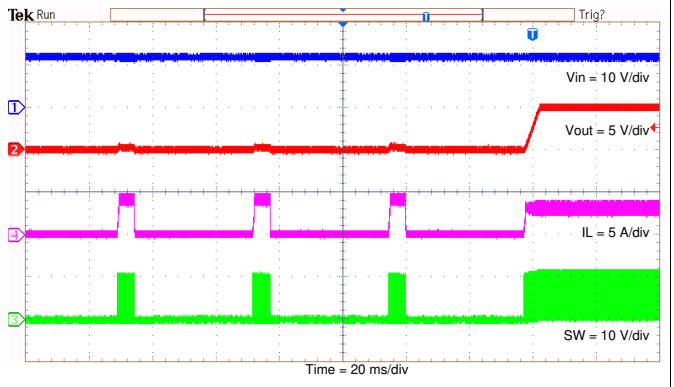


図 33. Short Recovery

9 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 4.5 V and 24 V. This input supply must be well regulated. If the input supply is located more than a few inches from the device or converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitor. An electrolytic capacitor with a value of 47 µF is a typical choice. The 0.1-µF ceramic bypass capacitor should be as close as possible to VIN and GND pins.

10 Layout

10.1 Layout Guidelines

1. VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
2. The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
3. The 0.1-µF ceramic bypass capacitor should be as close as possible to VIN and GND pins.
4. Provide sufficient vias for the input capacitor and output capacitor.
5. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
6. Do not allow switching current to flow under the device.
7. A separate VOUT path should be connected to the upper feedback resistor.
8. Make a Kelvin connection to the GND pin for the feedback path.
9. Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
10. The trace of the VFB node should be as small as possible to avoid noise coupling.
11. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

10.2 Layout Example

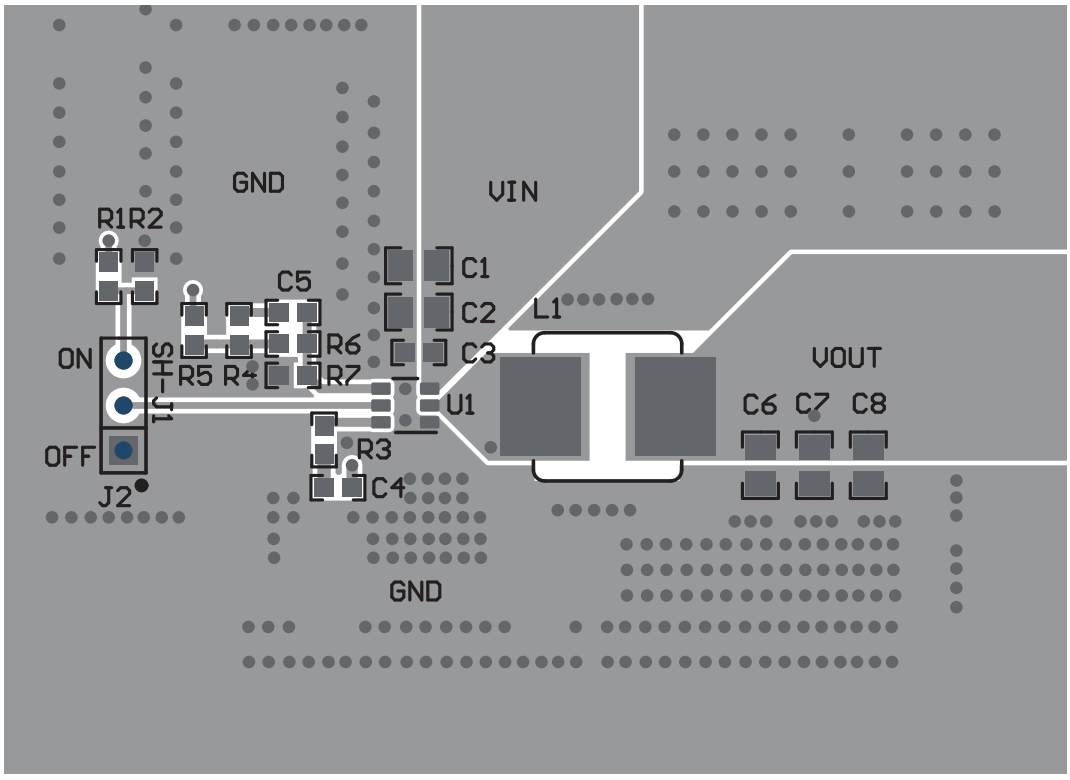


図 34. TPS56339 Top Layout Example

Layout Example (continued)

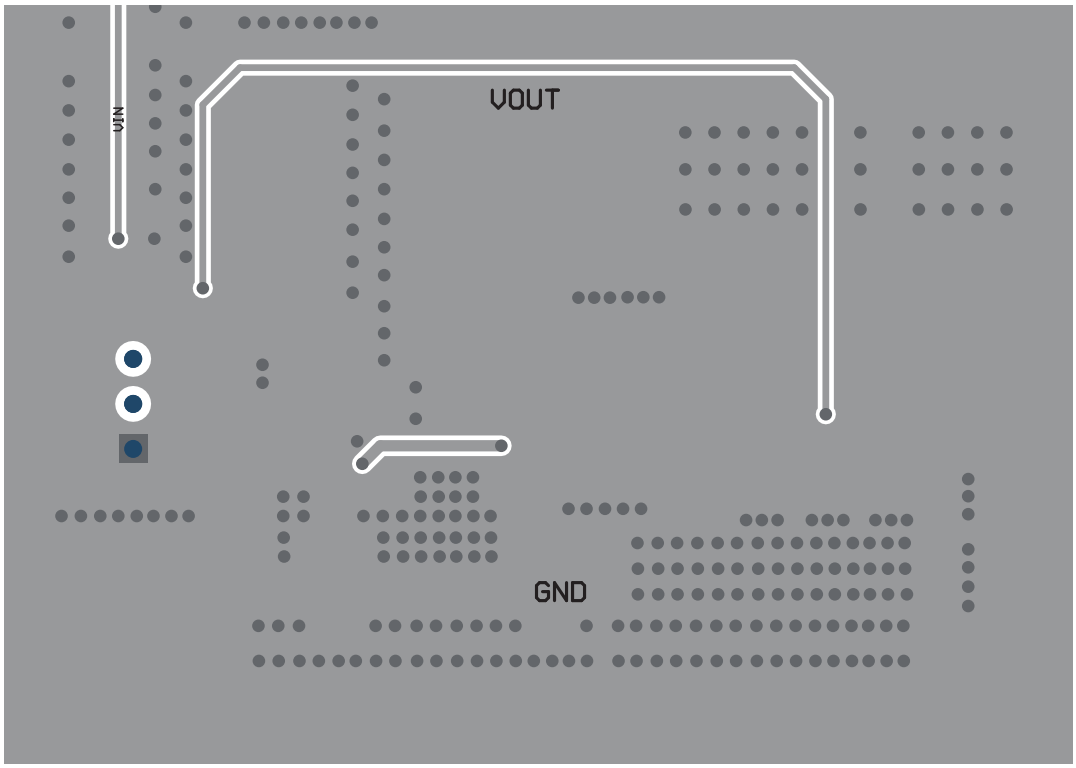


図 35. TPS56339 Bottom Layout Example

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.2 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商標

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.

11.5 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS56339DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	T6339	Samples
TPS56339DDCT	ACTIVE	SOT-23-THIN	DDC	6	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	T6339	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

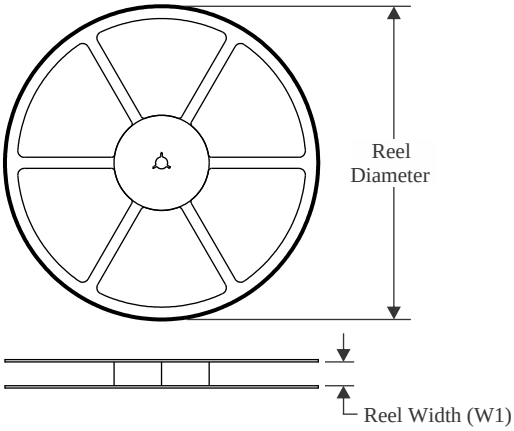
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

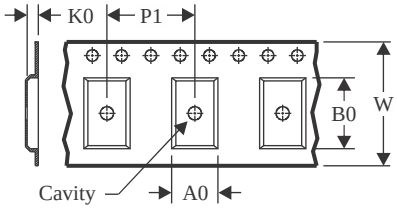
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

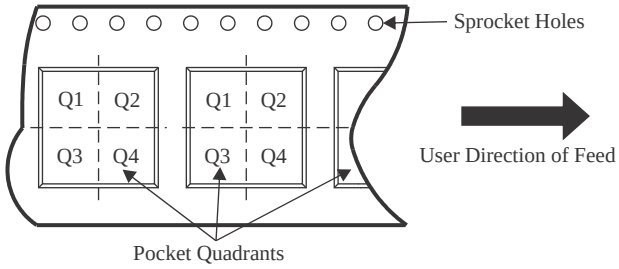


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

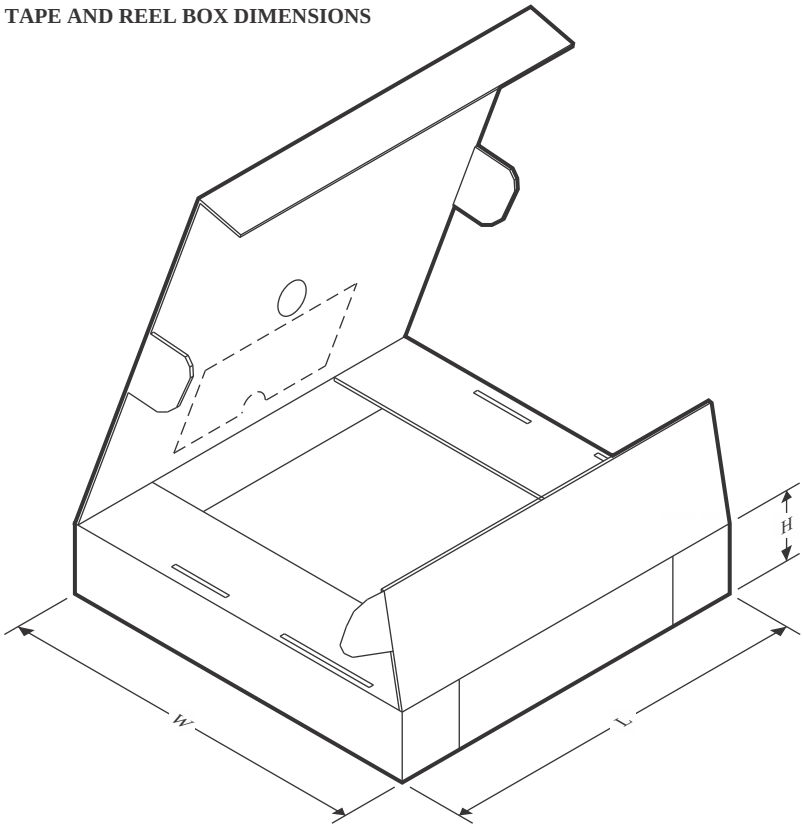
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS56339DDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS56339DDCT	SOT-23-THIN	DDC	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

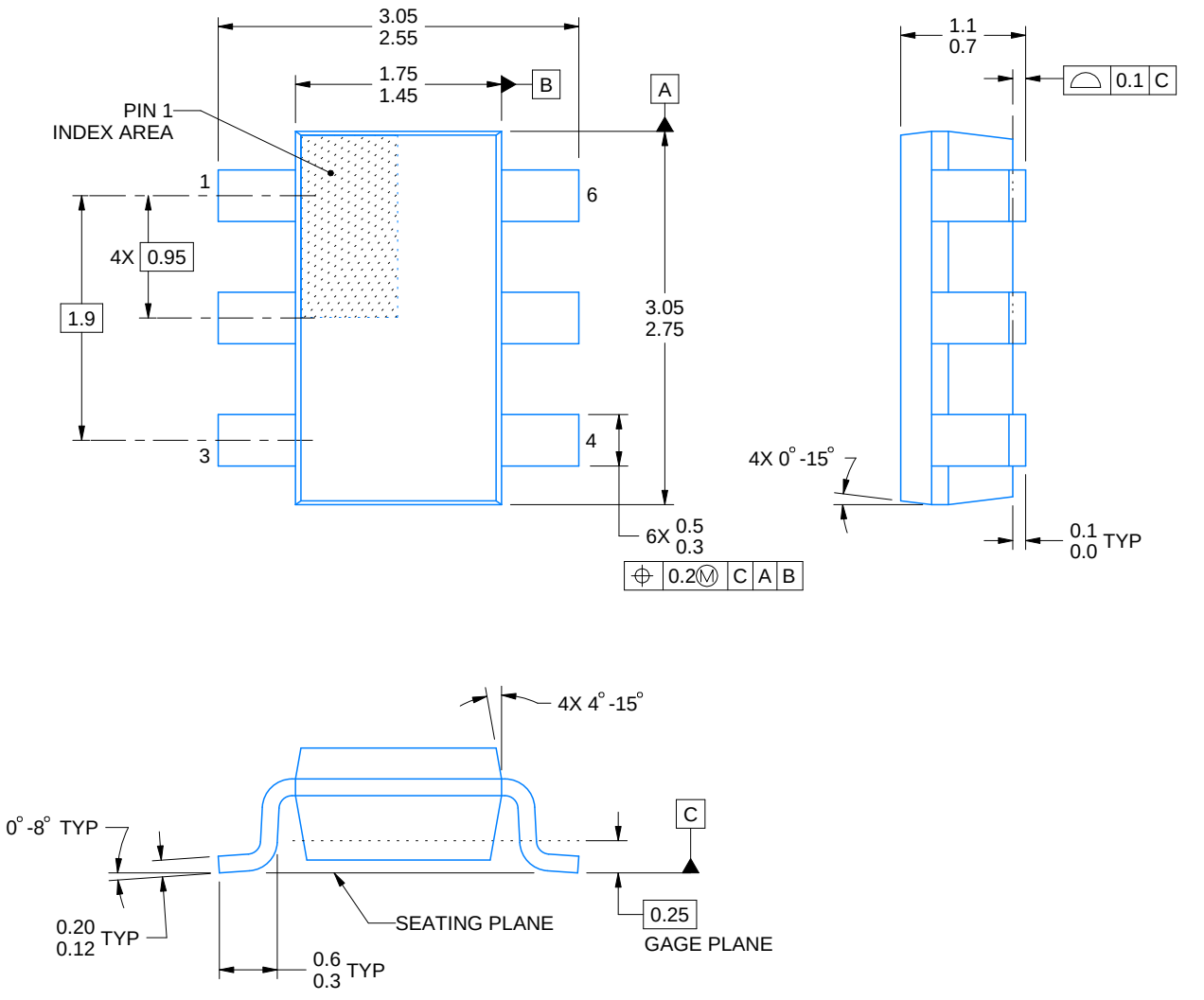
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS56339DDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
TPS56339DDCT	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0

PACKAGE OUTLINE

DDC0006A

SOT-23 - 1.1 max height

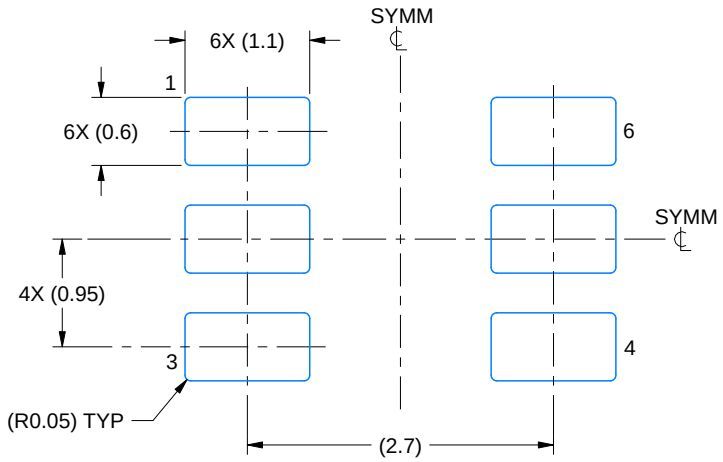
SMALL OUTLINE TRANSISTOR



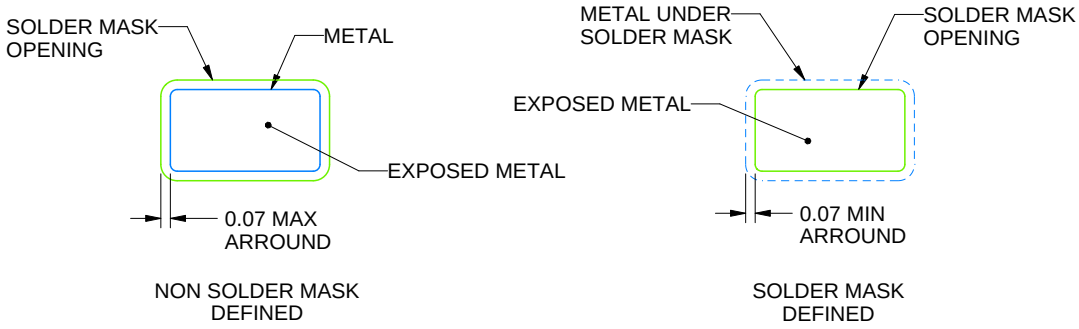
4214841/E 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

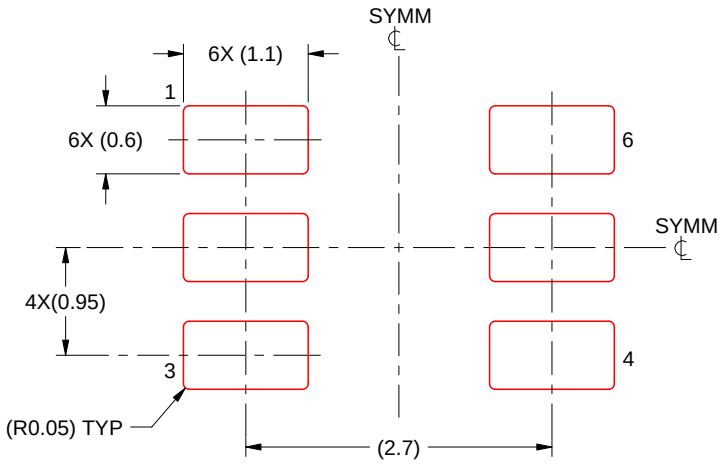


SOLDERMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/E 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265