

## TPS56C230 4.5V~18V、12A の同期整流降圧コンバータ

### 1 特長

- 入力電圧範囲: 4.5V~18V
- 出力電圧範囲: 0.6V~5.5V
- 12A の連続出力電流をサポート
- D-CAP3™アーキテクチャ制御による高速過渡応答
- $\pm 1\%$  の帰還電圧精度 (25°C)
- 17m $\Omega$  および 5.9m $\Omega$  の FET を内蔵
- MODE ピンで Eco-mode™または強制連続導通モード (FCCM) を選択可能
- 500kHz のスイッチング周波数
- ソフトスタート時間を変更可能、デフォルトは 1.2ms
- パワー・グッド・インジケータを内蔵
- 出力放電機能を内蔵
- サイクル単位の過電流保護
- ラッチなしの過電圧、低電圧、過熱、および低電圧誤動作防止保護機能
- 動作時の接合部温度: -40°C~125°C
- 20 ピン、3.0mm x 3.0mm の HotRod™ VQFN パッケージ
- 8A の [TPS568230](#) とピン互換
- [WEBENCH® Power Designer](#) により、TPS56C230 を使用するカスタム設計を作成

### 2 アプリケーション

- DTV およびセットトップ・ボックス
- PC および産業用 PC
- 有線ネットワーク
- 分散電源システム

### 3 概要

TPS56C230 は、FET を内蔵した高効率の同期整流降圧コンバータです。スタンバイ時消費電流が小さく、必要な外付け部品が少ないため、システム設計者は広範なアプリケーションにこのデバイスを使用できます。

TPS56C230 は、内部補償を使用して高速な過渡応答と非常に優れたラインおよび負荷レギュレーションを実現する D-CAP3 制御を採用しています。また、低 ESR (等価直列抵抗) の出力コンデンサ (例: 特殊ポリマー・コンデンサ、超低 ESR セラミック・コンデンサ) をサポートできる独自の回路も備えています。

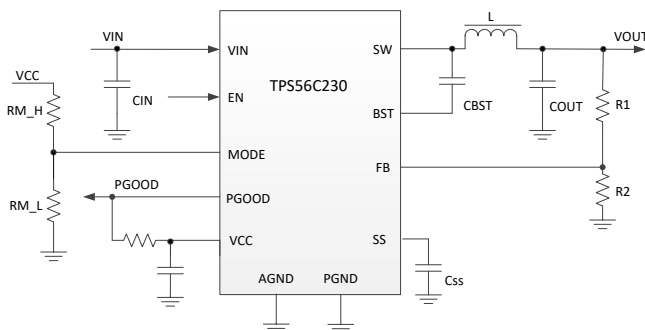
TPS56C230 の MODE ピンを使用して、軽負荷時の動作を Eco-mode と FCCM モードのどちらかに設定できます。Eco-mode では軽負荷動作中も高効率を維持し、FCCM モード動作では軽負荷時でも出力リップルを小さく保ちます。このデバイスは、内部ソフト・スタート時間と外部ソフト・スタート時間を選択できます。内部ソフト・スタート時間は 1.2ms に固定されていますが、アプリケーションでこれより長いソフト・スタート時間が必要な場合、SS ピンに外付けのコンデンサを接続して、長いソフト・スタート時間を実現できます。

#### 製品情報<sup>(1)</sup>

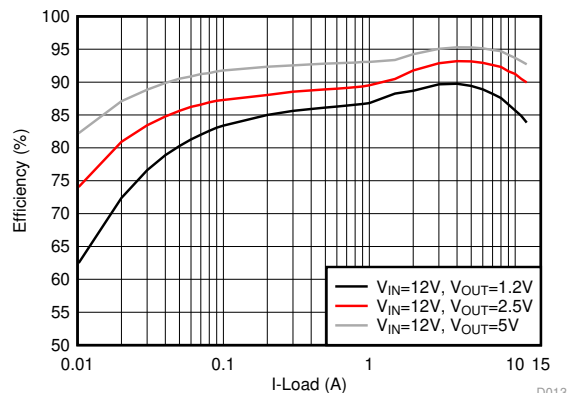
型番	パッケージ	本体サイズ(公称)
TPS56C230	VQFN (20)	3.00mmx3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

概略回路図



効率と出力電流との関係、Eco-mode



D013



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## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

### 2019年8月発行のものから更新

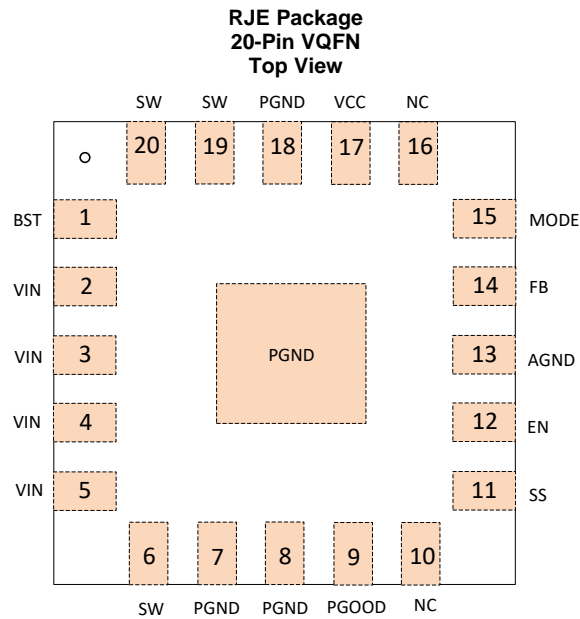
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- マーケティング・ステータスを「事前情報」から「量産データ」に変更..... **1**

## 5 概要（続き）

TPS56C230 はパワー・グッド・インジケータを内蔵しており、出力放電機能を備えています。また、OVP、UVP、OCP、OTP、UVLO を含む完全な保護機能を備えています。このデバイスは、20 ピンの 3.0mm × 3.0mm HotRod パッケージで供給され、-40°C～125°C の接合部温度で動作が規定されています。

## 6 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BST	1	I	Supply input for the gate drive voltage of the high-side MOSFET. Connect the bootstrap capacitor between BST and SW, 0.1 uF is recommended.
VIN	2,3,4,5	P	Input voltage supply pin for the control circuitry. Connect the input decoupling capacitors between VIN and PGND.
SW	6,19,20	O	Switching node connection to the inductor and bootstrap capacitor for buck. This pin voltage swings from a diode voltage below the ground up to input voltage of buck.
PGND	7,8,18,Pad	G	Power GND terminal for the controller circuit and the internal circuitry.
PGOOD	9	O	Open drain power good indicator. It is asserted low if output voltage is out of PG threshold, over voltage or if the device is under thermal shutdown, EN shutdown or during soft start.
SS	11	I	Soft-Start time selection pin. Connecting an external capacitor sets the soft-start time and if no external capacitor is connected, the soft-start time is about 1.2ms.
NC	10,16		Not connect. Can be connected to GND plane for better thermal achieved.
EN	12	I	Enable input of buck converter
AGND	13	G	Ground of internal analog circuitry. Connect AGND to GND plane with a short trace.
FB	14	I	Feedback sensing pin for Buck output voltage. Connect this pin to the resistor divider between output voltage and AGND.
MODE	15	I	Light load operation mode selection pin. Connect this pin to a resistor divider from VCC and AGND for different MODE options shown in <a href="#">表 1</a>
VCC	17	O	The driver and control circuits are powered from this voltage. Decouple with a minimum 1 μF ceramic capacitor as close to VCC as possible.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
Input voltage	VIN	-0.3	20	V
	BST	-0.3	25	V
	BST-SW	-0.3	6	V
	EN, MODE, FB, SS	-0.3	6	V
	PGND, AGND,	-0.3	0.3	V
Output voltage	SW	-1	20	V
	SW (10-ns transient)	-3	22	V
	PGOOD	-0.3	6	V
T <sub>J</sub>	Operating junction temperature	-40	150	°C
T <sub>stg</sub>	Storage temperature	-55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

		VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22- V C101 <sup>(2)</sup>	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VIN	4.5	18	V
	BST	-0.3	23.5	V
	BST-SW	-0.3	5.5	V
	EN, MODE, FB, SS	-0.3	5.5	V
	PGND, AGND	-0.3	0.3	V
Output voltage	SW	-1	18	V
	PGOOD	-0.3	5.5	V
I <sub>OUT</sub>	Output current		12	A
T <sub>J</sub>	Operating junction temperature	-40	125	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS56C230	UNIT
		RJE (VQFN)	
		20 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance (standard board)	42.3	°C/W
R <sub>θJA_effective</sub>	Junction-to-ambient thermal resistance (4-layer custom board) <sup>(2)</sup>	28.2	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	26.2	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	13	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

(2) 70 mm x 70 mm, 4 layers, thickness: 1.5 mm. 2 oz. copper traces located on the top and bottom of the PCB. 4 thermal vias in the PowerPAD area under the device package.

**Thermal Information (continued)**

THERMAL METRIC <sup>(1)</sup>		TPS56C230	UNIT
		RJE (VQFN)	
		20 PINS	
$\Psi_{JB}$	Junction-to-board characterization parameter	12.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	16.1	°C/W

**7.5 Electrical Characteristics**
 $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{VIN} = 12\text{ V}$ , unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENT</b>						
$V_{IN}$	Input voltage range		4.5		18	V
$I_{VIN}$	Non-switching supply current	No load, $V_{EN}=5\text{V}$		400		$\mu\text{A}$
$I_{VINDN}$	Shutdown supply current	No load, $V_{EN}=0\text{V}$		2		$\mu\text{A}$
<b>VCC OUTPUT</b>						
$V_{CC}$	VCC output voltage	$V_{VIN}>5.0\text{V}$	4.85	5	5.15	V
		$V_{VIN}=4.5\text{V}$		4.5		
$I_{CC}$	VCC current limit		20			mA
<b>FEEDBACK VOLTAGE</b>						
$V_{FB}$	FB voltage	$T_J = 25^{\circ}\text{C}$	594	600	606	mV
		$T_J = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$	591	600	609	mV
<b>DUTY CYCLE and FREQUENCY CONTROL</b>						
$F_{SW}$	Switching frequency	$T_J = 25^{\circ}\text{C}$		500		kHz
$t_{ON(MIN)}$	SW minimum on time	$T_J = 25^{\circ}\text{C}$		60		ns
$t_{OFF(MIN)}$	SW minimum off time	$T_J = 25^{\circ}\text{C}$ , $V_{FB} = 0.5\text{ V}$			180	ns
<b>MOSFET and DRIVERS</b>						
$R_{DS(ON)H}$	High side switch resistance	$T_J = 25^{\circ}\text{C}$		17		$\text{m}\Omega$
$R_{DS(ON)L}$	Low side switch resistance	$T_J = 25^{\circ}\text{C}$		5.9		$\text{m}\Omega$
<b>OUTPUT DISCHARGE and SOFT START</b>						
$R_{DIS}$	Discharge resistance	$T_J=25^{\circ}\text{C}$ , $V_{EN}=0\text{V}$		350		$\Omega$
$t_{SS}$	Soft start time	Internal soft-start time, SS floating		1.2		ms
$I_{SS}$	Soft start charge current			5		$\mu\text{A}$
<b>POWER GOOD</b>						
$t_{PGDLY}$	PGOOD start-up delay	PGOOD from low to high		1		ms
$V_{PGTH}$	PGOOD threshold	VFB falling (fault)		85		%
		VFB rising (good)		90		%
		VFB rising (fault)		115		%
		VFB falling (good)		110		%
$V_{PG\_L}$	PGOOD sink current capability	$I_{OL} = 4\text{mA}$			0.4	V
$I_{PGLK}$	PGOOD leak current	$V_{PGOOD} = 5.5\text{V}$			1	$\mu\text{A}$
<b>CURRENT LIMIT</b>						
$I_{OCL}$	Over current threshold (valley)	$T_J = 25^{\circ}\text{C}$	14	15	16	A
		$T_J = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$	13	15	17.5	A
$I_{NOCL}$	Negative over current threshold			4		A
<b>LOGIC THRESHOLD</b>						
$V_{ENH}$	EN high-level input voltage		1.2	1.3	1.4	V
$V_{ENL}$	EN low-level input voltage		0.9	1.1	1.2	V
$I_{EN}$	Enable internal pull down current	$V_{EN}=0.8\text{V}$		2		$\mu\text{A}$
<b>OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION</b>						

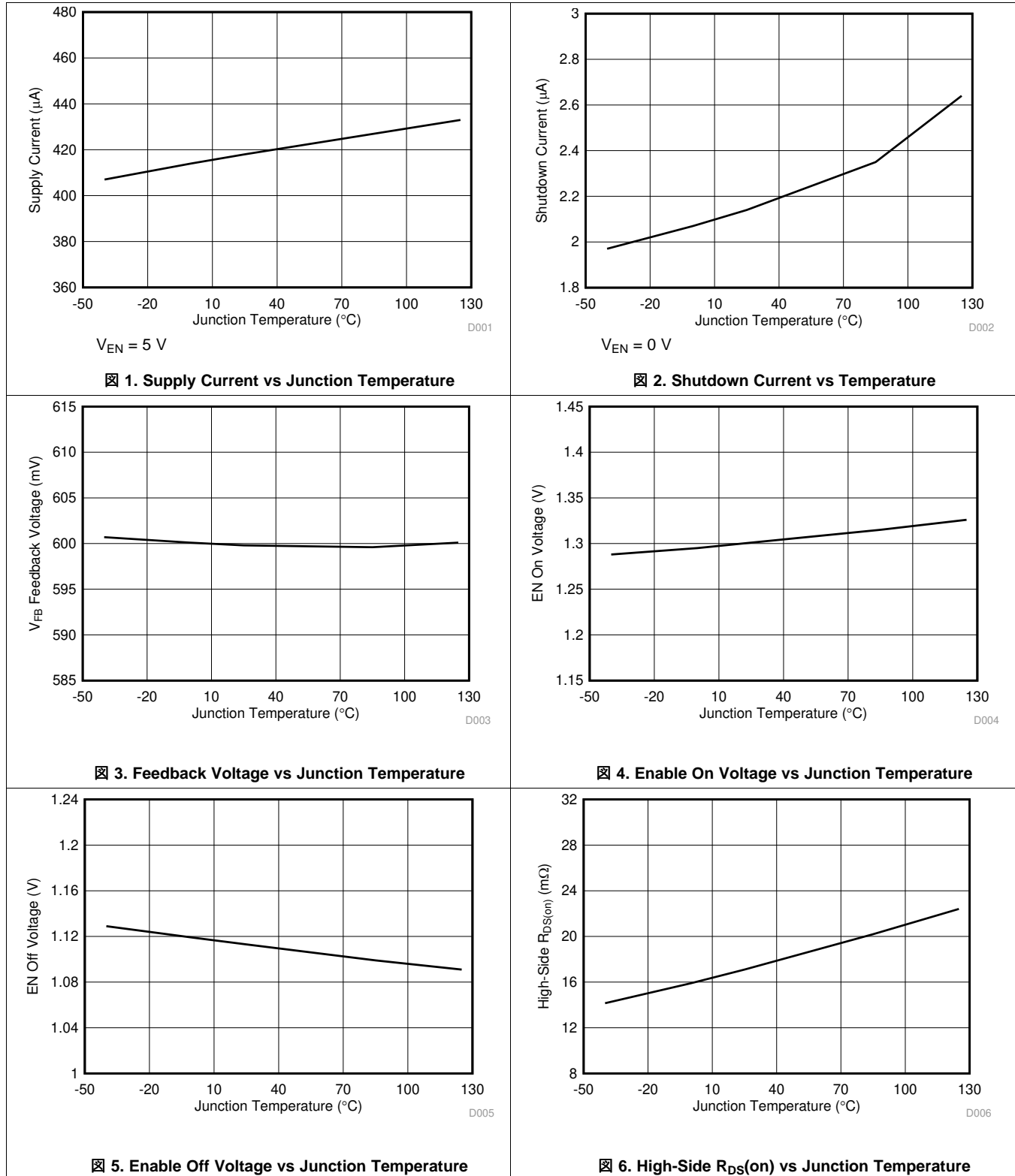
## Electrical Characteristics (continued)

$T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{VIN} = 12\text{ V}$ , unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{OVP}$	OVP trip threshold			125		%
$t_{OVPDLY}$	OVP prop deglitch			120		us
$V_{UVP}$	UVP trip threshold			60		%
$t_{UVPDLY}$	UVP prop deglitch			256		us
$t_{UVPDEL}$	Output Hiccup delay relative to SS time			1.5		cycle
$t_{UVPEN}$	Output Hiccup enable delay relative to SS time			10.5		cycle
<b>UVLO</b>						
$V_{UVLOVIN}$	VIN UVLO threshold	Wake up VIN voltage		4.2	4.4	V
		Shutdown VIN voltage	3.6	3.7		
		Hysteresis VIN voltage		0.5		V
<b>OVER TEMPERATURE PROTECTION</b>						
$T_{OTP}$	OTP trip threshold <sup>(1)</sup>	Shutdown temperature		150		$^{\circ}\text{C}$
$T_{OTPHSY}$	OTP hysteresis <sup>(1)</sup>	Hysteresis		20		$^{\circ}\text{C}$

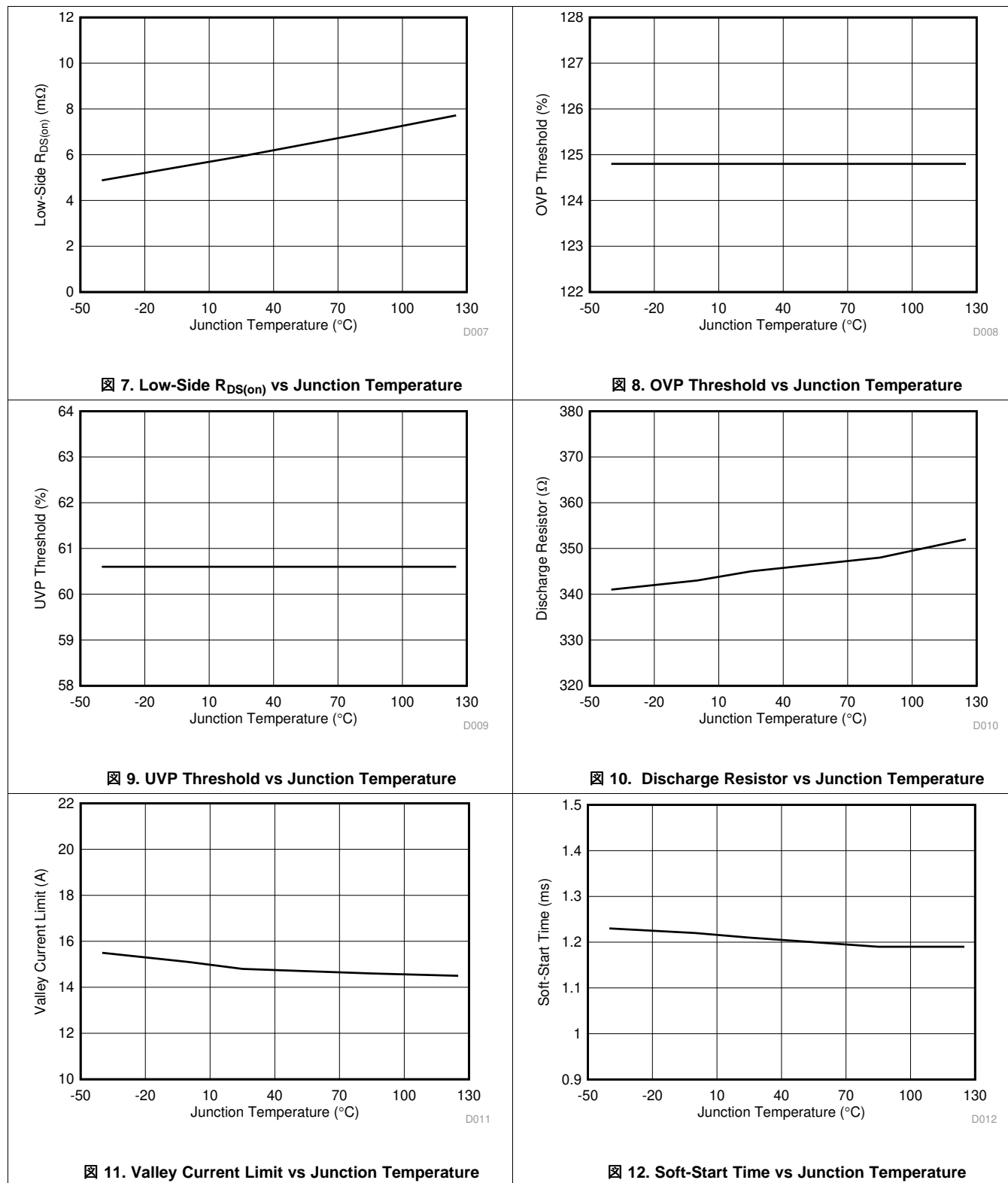
(1) Not production tested

## 7.6 Typical Characteristics





Typical Characteristics (continued)



Typical Characteristics (continued)

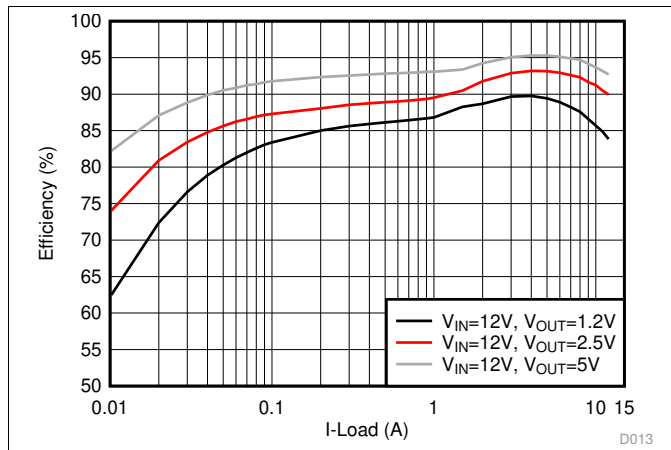


图 13. Efficiency vs Load Current, Eco-mode

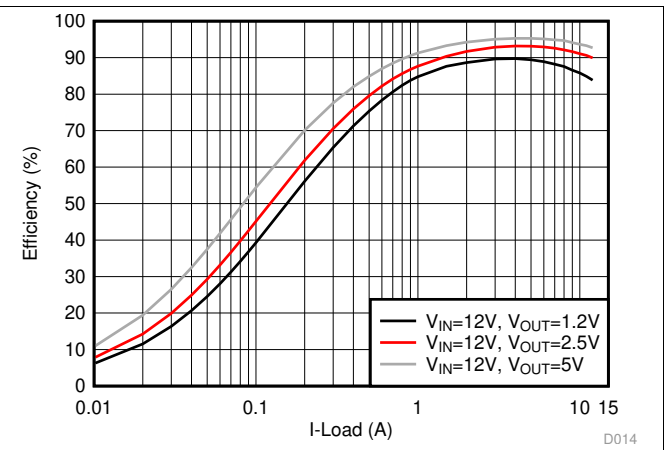


图 14. Efficiency vs Load Current, FCCM

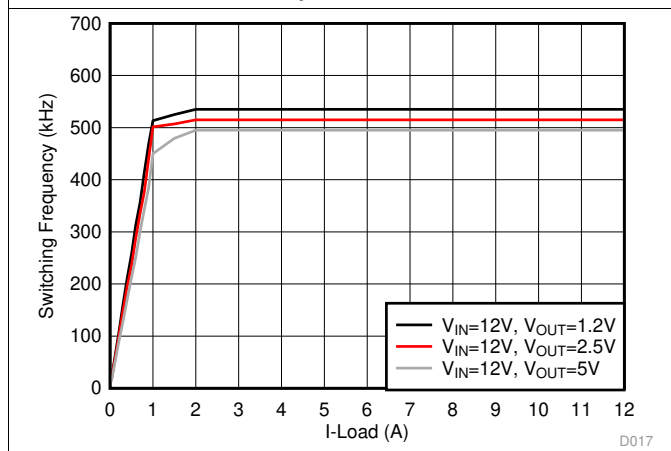


图 15. Switching Frequency vs Load Current, Eco-mode

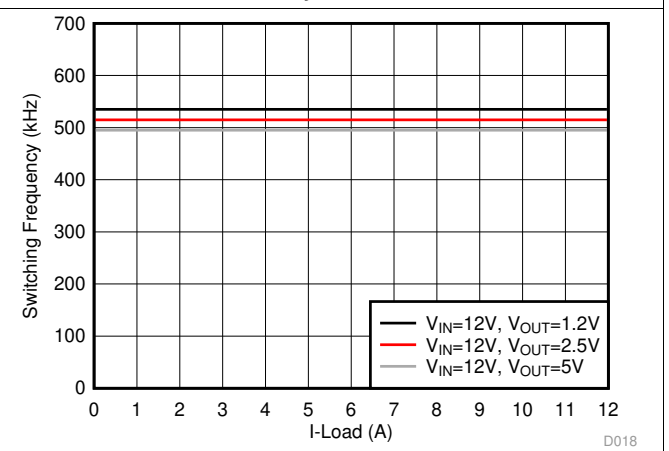


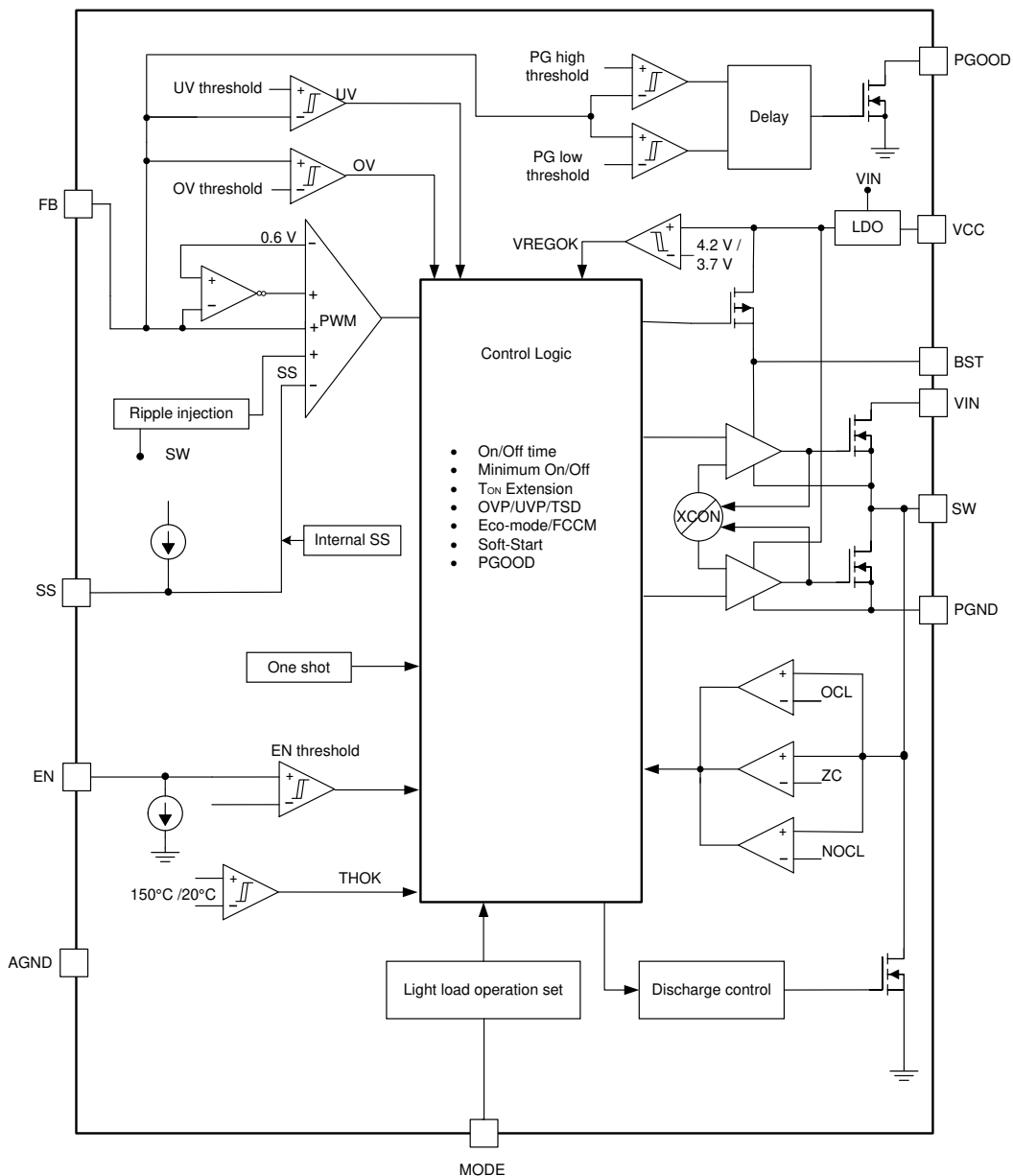
图 16. Switching Frequency vs Load Current, FCCM

## 8 Detailed Description

### 8.1 Overview

The TPS56C230 is high density synchronous buck converter which operates from 4.5-V to 18-V input voltage ( $V_{IN}$ ), and the output voltage range is from 0.6 V to 5.5 V. It has 17-m $\Omega$  and 5.9-m $\Omega$  integrated MOSFETs that enable high efficiency up to 12 A. The device employs D-CAP3 mode control that enables low external component count, ease of design, optimization of the power design for cost, size and efficiency, and provides fast transient response with no external compensation components and an accurate feedback voltage. The control topology supports seamless transition between CCM mode at heavy load conditions and DCM operation at light load conditions. Eco-mode allows the TPS56C230 to maintain high efficiency at light load and FCCM mode keeps the output ripple small at light load. The TPS56C230 is able to adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

### 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 PWM Operation and D-CAP3™ Control

The main control loop of the buck is adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP3 mode control. The D-CAP3 mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output. The TPS56C230 also includes an error amplifier that makes the output voltage very accurate.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one-shot timer expires. This one-shot duration is set proportional to the converter output voltage,  $V_{OUT}$ , and is inversely proportional to the input voltage,  $V_{IN}$ , to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ripple generation circuit is added to reference voltage for emulating the output ripple, this enables the use of very low-ESR output capacitors such as multi-layered ceramic caps (MLCC). No external current sense network or loop compensation is required for D-CAP3 control topology.

For any control topology that is compensated internally, there is a range of the output filter it can support. The output filter used with the TPS56C230 is a low-pass L-C circuit. This L-C filter has a double-pole frequency described in 式 1.

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (1)$$

At low frequencies, the overall loop gain is set by the internal output set-point resistor divider network and the internal gain of the TPS56C230. The low-frequency L-C double pole has a 180 degree drop in phase. At the output filter frequency, the gain rolls off at a  $-40$  dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from  $-40$  dB to  $-20$  dB per decade and increases the phase to 90 degree one decade above the zero frequency. The inductor and capacitor selected for the output filter must be such that the double pole is placed close enough to the high-frequency zero so that the phase boost provided by this high-frequency zero provides adequate phase margin for the stability requirement. The crossover frequency of the overall system should usually be targeted to be less than one-third of the switching frequency ( $F_{SW}$ ).

### 8.3.2 Soft Start

The TPS56C230 has an internal 1.2-ms soft-start time, and also an external SS pin is provided for setting longer soft start time if needed. When the EN pin becomes high, the soft-start function begins ramping up the reference voltage to the PWM comparator.

If the application needs a longer soft start time, it can be set by connecting a capacitor on SS pin. When the EN pin becomes high, the soft-start charge current ( $I_{SS}$ ) begins charging the external capacitor ( $C_{SS}$ ) connected between SS and AGND. The device tracks the lower of the internal soft-start voltage or the external soft-start voltage as the reference. The equation for the soft-start time ( $T_{SS}$ ) is shown in 式 2:

$$T_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)} \quad (2)$$

where

- $V_{REF}$  is 0.6 V and  $I_{SS}$  is 5  $\mu A$

### 8.3.3 Large Duty Operation

The TPS56C230 can support large duty operation by its internal  $T_{ON}$  extension function. When  $V_{IN}/V_{OUT} < 1.6$ , and the  $V_{FB}$  is lower than internal  $V_{REF}$ , the  $T_{ON}$  will be extended to implement the large duty operation and also improve the performance of the load transient performance.

### 8.3.4 Power Good

The Power Good (PGOOD) pin is an open-drain output. Once the  $V_{FB}$  is between 90% and 110% of the target output voltage, the PGOOD is de-asserted and floats after a 1-ms de-glitch time. A pullup resistor of 100 k $\Omega$  is recommended to pull the voltage up to VCC. The PGOOD pin is pulled low when:

## Feature Description (continued)

- the FB pin voltage is lower than 85% or greater than 115% of the target output voltage
- in an OVP, UVP, or thermal shutdown event
- during the soft-start period.

### 8.3.5 Overcurrent Protection and Undervoltage Protection

The TPS56C230 has the overcurrent protection and undervoltage protection. The output overcurrent limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-time of the high-side FET switch, the switch current increases at a linear rate determined by  $V_{in}$ ,  $V_{out}$ , the on-time and the output inductor value. During the on-time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current  $I_{OUT}$ . If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of overcurrent protection. When the load current is higher than the overcurrent threshold by one half of the peak-to-peak inductor ripple current, the OCL is triggered and the current is being limited, the output voltage tends to drop because the load demand is higher than what the converter can support. When the output voltage falls below 60% of the target voltage, the UVP comparator detects it, the output will shut off after a wait time of 256 $\mu$ s and then re-start after the hiccup time (typically  $10.5 \cdot T_{ss}$ ). When the over current condition is removed, the output voltage is recovered.

### 8.3.6 Overvoltage Protection

The TPS56C230 has the overvoltage protection feature and have the same implementation. When the output voltage becomes higher than 125% of the target voltage, the OVP comparator output goes high, the output will be discharged after a wait time of 120  $\mu$ s. When the over voltage condition is removed, the output voltage will be recovered.

### 8.3.7 Out-of-Bounds Operation

The TPS56C230 has an out-of-bounds (OOB) overvoltage protection that protects the output load at a much lower overvoltage threshold of 8% above the target voltage. OOB protection does not trigger an overvoltage fault, OOB protection operates as an early protection mechanism. During the OOB operation, the device operates in force PWM mode only by turning on the low-side FET. Turning on the low-side FET beyond the zero inductor current quickly discharges the output capacitor thus causing the output voltage to fall quickly towards the setpoint. During the operation, the cycle-by-cycle negative current limit is also activated to ensure the safe operation of the internal FETs.

### 8.3.8 UVLO Protection

The undervoltage lockout (UVLO) protection monitors the VCC pin voltage to protect the internal circuitry from low input voltages. When the voltage is lower than UVLO threshold voltage, the device shuts off and outputs are discharged to prevent mis-operation of the device. The converter begins operation again when the input voltage exceeds the threshold by a hysteresis of 500 mV (typical). This is a non-latch protection.

### 8.3.9 Output Voltage Discharge

The TPS56C230 has the discharge function by using internal MOSFET about 350 $\Omega$ , which is connected to the output terminal SW. The discharge is slow due to the lower current capability of the MOSFET.

### 8.3.10 Thermal Shutdown

The TPS56C230 monitors the internal die temperature. If the temperature exceeds the threshold value (typically 150°C), the device shuts off and the output will be discharged. This is a non-latch protection, the device restarts switching when the temperature goes below the thermal shutdown threshold.

## 8.4 Device Functional Modes

### 8.4.1 Light Load Operation

TPS56C230 has a MODE pin that can setup two different states of operation for light load operation. The light load running includes Eco-mode and FCCM mode.

### 8.4.2 Eco-mode™ Control

The Eco-mode control schemes to maintain high light load efficiency. As the output current decreases from heavy load conditions, the inductor current is also reduced and eventually comes to a point where the rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The light load current where the transition to Eco-mode operation happens (  $I_{OUT(LL)}$  ) can be calculated from 式 3.

$$I_{OUT(LL)} = \frac{1}{2 \times L_{OUT} \times F_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (3)$$

After identifying the application requirements, design the output inductance ( $L_{OUT}$ ) so that the inductor peak-to-peak ripple current is approximately between 20% and 30% of the  $I_{OUT(max)}$  (peak current in the application). It is also important to select the inductor properly so that the valley current does not hit the negative low-side current limit.

### 8.4.3 Force CCM

Force CCM(FCCM) mode keeps the converter to operate in continuous conduction mode during light-load conditions and allows the inductor current to become negative. During FCCM mode, the switching frequency (FSW) is maintained at an almost constant value over the full load range, which is suitable for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load.

### 8.4.4 Mode Selection

The device reads the voltage on the MODE pin during start-up and latches onto one of the MODE options listed below in 表 1 . The voltage on the MODE pin recommended to be set by connecting this pin to the center tap of a resistor divider connected between VCC and AGND. A guideline for the top resistor ( $R_{M,H}$ ) and the bottom resistor ( $R_{M,L}$ ) as 1% resistors is shown in 表 1. It is recommended to choose the resistor to set the voltage at around 5%\*VCC for Eco-mode or 15%\*VCC for FCCM. It is important that the voltage for the MODE pin is derived from the VCC rail only since internally this voltage is referenced to detect the MODE option, and not to leave the mode pin floating. The MODE pin setting can be reset only by a VIN power cycling or EN toggle.

**表 1. MODE Pin Resistor Settings**

Voltage on MODE	Recommended Resistor		LIGHT LOAD OPERATION
	$R_{M,H}(k\Omega)$	$R_{M,L}(k\Omega)$	
(0~10%)*VCC	330	15	Eco-mode
(10%~20%)*VCC	180	33	FCCM

Figure 17 below shows the typical start-up sequence of the device once the enable signal crosses the EN turn on threshold. After the voltage on VCC crosses the rising UVLO threshold it takes about 500us to read the first mode setting and approximately 100us from there to finish the last mode setting. The output voltage starts ramping after the mode reading is done.

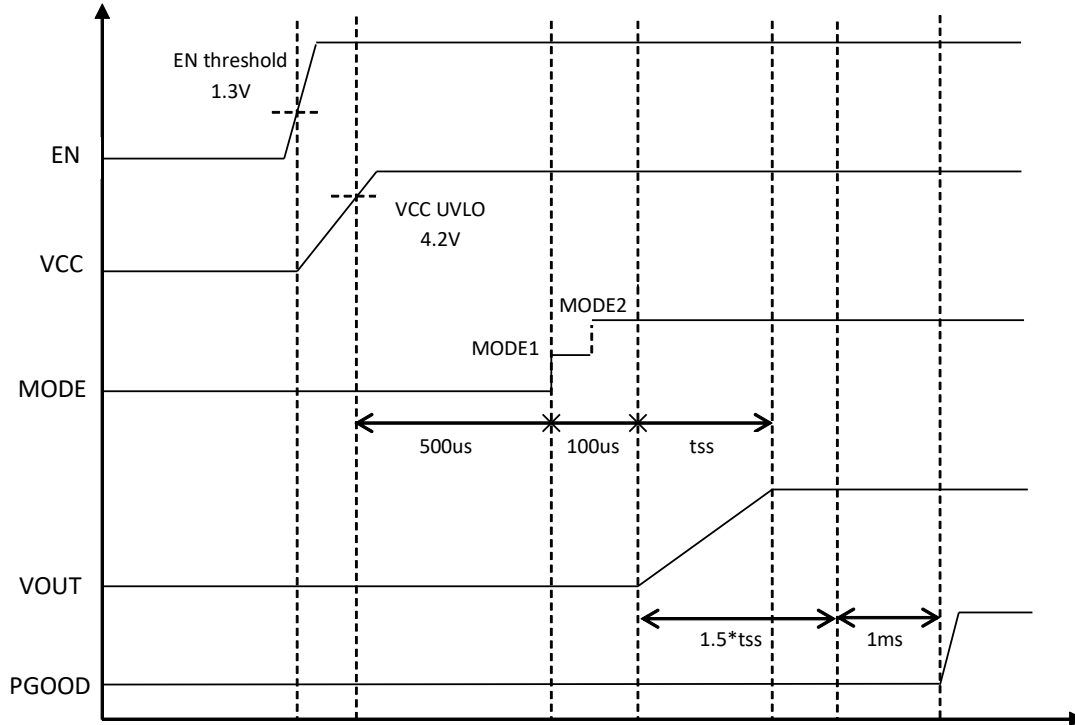


Figure 17. Power-Up Sequence

### 8.4.5 Standby Operation

The TPS56C230 can be placed in standby mode by pulling the EN pin low. The device operates with a shutdown current of 2  $\mu$ A when in standby condition. EN pin is pulled low internally, when floating, the part is disabled by default.

## 9 Application and Implementation

注

Information in the following application sections are not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The schematic of 18 shows a typical application for TPS56C230 with 1.2-V output. This design converts an input voltage range of 4.5 V to 18 V down to 1.2 V with a maximum output current of 12 A.

### 9.2 Typical Application

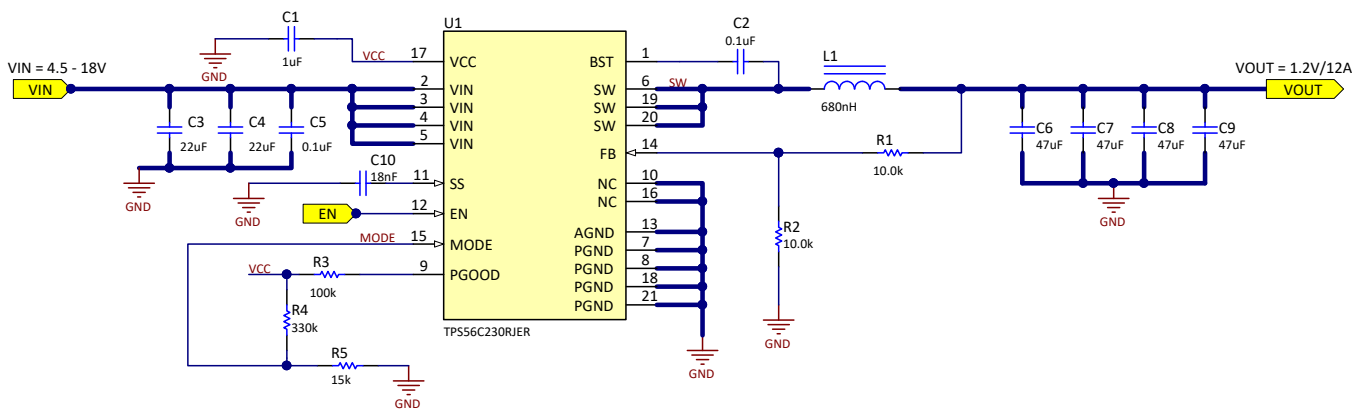


图 18. 1.2-V, 12-A Reference Design

#### 9.2.1 Design Requirements

表 2 lists the design parameters for this example.

表 2. Design Parameters

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OUT</sub>	Output voltage		1.2		V
I <sub>OUT</sub>	Output current		12		A
ΔV <sub>OUT</sub>	Transient response		±5% x V <sub>OUT</sub>		
V <sub>IN</sub>	Input voltage	4.5	12	18	V
V <sub>OUT(ripple)</sub>	Output voltage ripple		2% x V <sub>OUT</sub>		
F <sub>SW</sub>	Switching frequency		500		kHz
	Light load operating mode		Eco-mode		
T <sub>A</sub>	Ambient temperature		25		°C

#### 9.2.2 Detailed Design Procedure

##### 9.2.2.1 Custom Design With WEBENCH® Tools

Click [here](#) to create a custom design using the TPS56C230 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V<sub>IN</sub>), output voltage (V<sub>OUT</sub>), and output current (I<sub>OUT</sub>) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.



The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at [www.ti.com/WEBENCH](http://www.ti.com/WEBENCH).

### 9.2.2.2 Output Voltage Set Point

To change the output voltage of the application, it is necessary to change the value of the upper feedback resistor. By changing this resistor the user can change the output voltage above 0.6 V. See 式 4

$$V_{OUT} = 0.6 \times \left( 1 + \frac{R_{UPPER}}{R_{LOWER}} \right) \quad (4)$$

### 9.2.2.3 MODE Selection

The light load running mode (Eco-mode or FCCM ) are set by a voltage divider from VCC to GND connected to the MODE pin. See 表 1 for possible MODE pin configurations. For this design example ,the switching frequency is about 500kHz, the light load running mode is Eco-mode and the output current is 12 A.

### 9.2.2.4 Inductor Selection

The inductor ripple current is filtered by the output capacitor. A higher inductor ripple current means the output capacitor should have a ripple current rating higher than the inductor ripple current. See 表 3 for recommended inductor values.

The RMS and peak currents through the inductor can be calculated using 式 5 and 式 6. It is important that the inductor is rated to handle these currents.

$$I_{L(rms)} = \sqrt{I_{OUT}^2 + \frac{1}{12} \times \left( \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times L_{OUT} \times F_{SW}} \right)^2} \quad (5)$$

$$I_{L(peak)} = I_{OUT} + \frac{I_{OUT(ripple)}}{2} \quad (6)$$

During transient and short-circuit conditions, the inductor current can increase up to the current limit of the device, so it is safe to choose an inductor with a saturation current higher than the peak current under current limit condition.

### 9.2.2.5 Output Capacitor Selection

After selecting the inductor, the output capacitor needs to be optimized. In D-CAP3, the regulator reacts within one cycle to the change in the duty cycle, so the good transient performance can be achieved without large amounts of output capacitance. The recommended output capacitance range is given in 表 3. Ceramic capacitors have very low ESR, otherwise the maximum ESR of the capacitor should be less than  $V_{OUT(ripple)}/I_{OUT(ripple)}$ .

**表 3. Recommended Component Values**

V <sub>OUT</sub> (V)	R <sub>LOWER</sub> (kΩ)	R <sub>UPPER</sub> (kΩ)	F <sub>sw</sub> (kHz)	L <sub>OUT</sub> (μH)	C <sub>OUT(min)</sub> (μF)	C <sub>OUT(max)</sub> (μF)	C <sub>FF</sub> (PF)
0.6	10	0	500	0.47	66	330	-
1.2	10	10	500	0.68	66	330	-
2.5	20	63	500	1.2	66	330	
3.3	20	90	500	1.5	66	330	22-110
5.0	15	110	500	1.8	66	330	22-110

### 9.2.2.6 Input Capacitor Selection

The TPS56C230 requires input decoupling capacitors on power supply input VIN, and the bulk capacitors are needed depending on the application. The minimum input capacitance required is given in 式 7.

$$C_{IN(min)} = \frac{I_{OUT} \times V_{OUT}}{V_{IN(ripple)} \times V_{IN} \times F_{SW}} \tag{7}$$

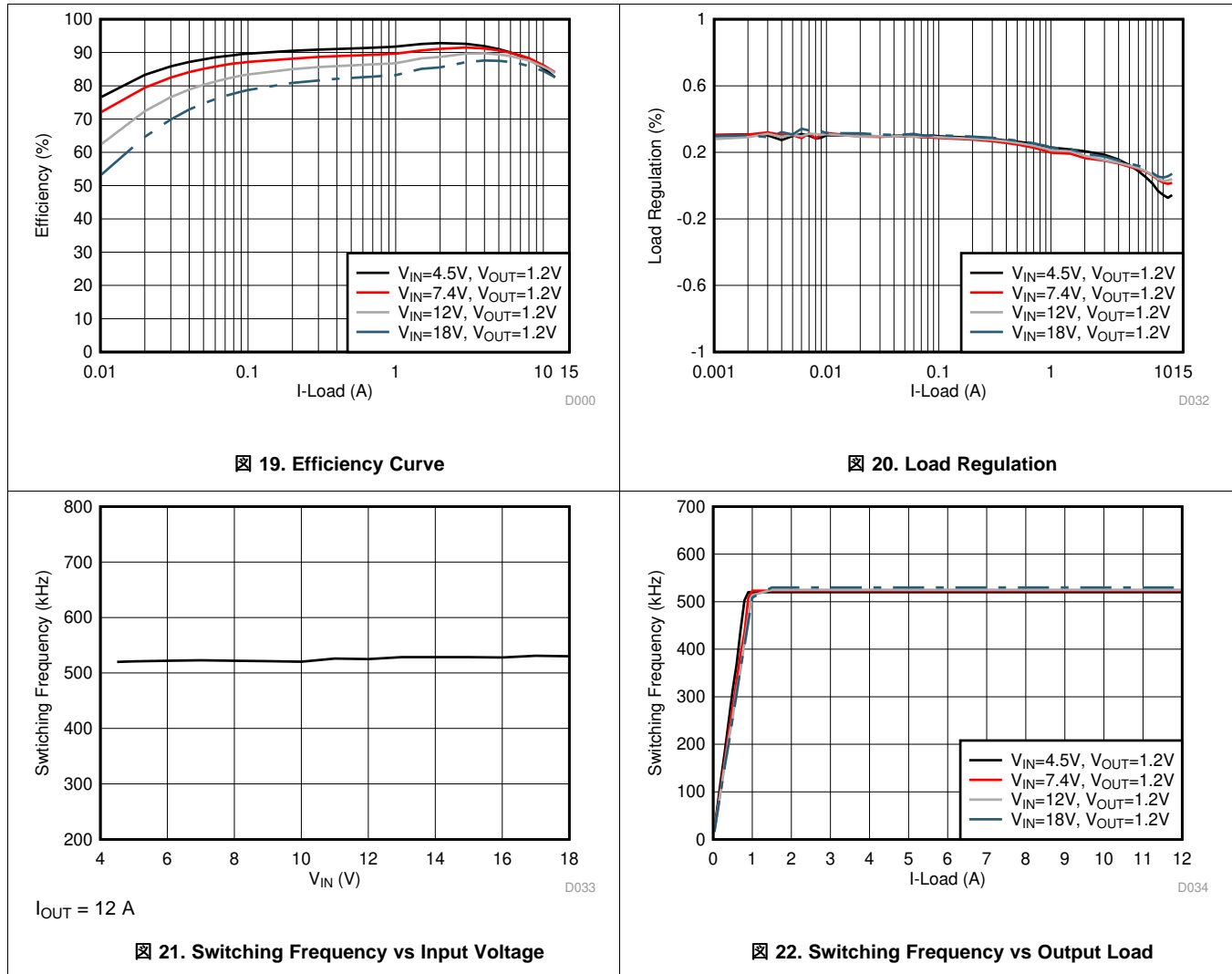
TI recommends using a high-quality X5R or X7R input decoupling capacitors of 40 μF on the input voltage pin VIN. The voltage rating on the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the application. The input ripple current is calculated by 式 8:

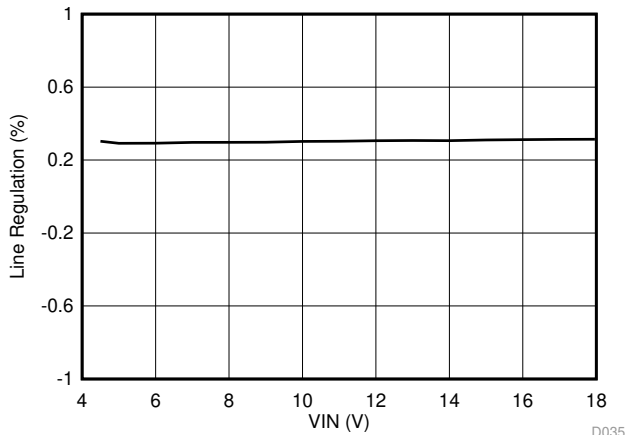
$$I_{CIN(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{(V_{IN(min)} - V_{OUT})}{V_{IN(min)}}} \tag{8}$$

A 1-μF ceramic capacitor is needed for the decoupling capacitor on VCC pin.

### 9.2.3 Application Curves

Figure 19 through Figure 34 apply to the circuit of Figure 18. VIN = 12 V. TA = 25°C unless otherwise specified.

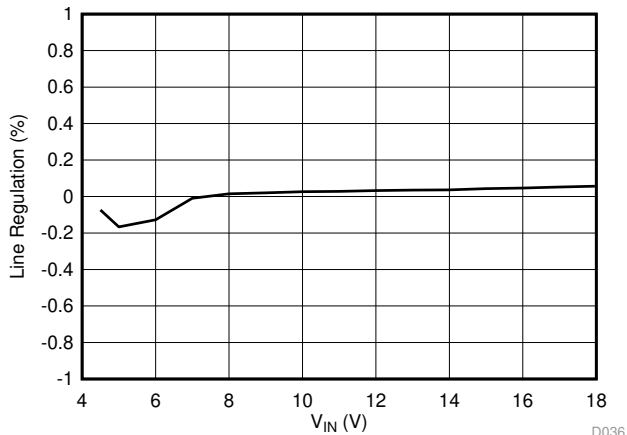




$I_{OUT}=0.1A$

D035

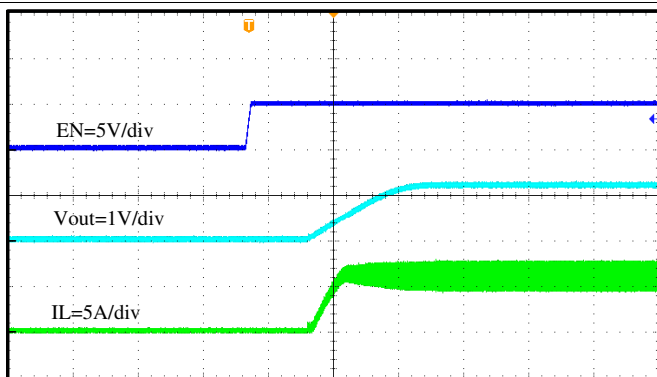
图 23. Line Regulation



$I_{OUT}=12A$

D036

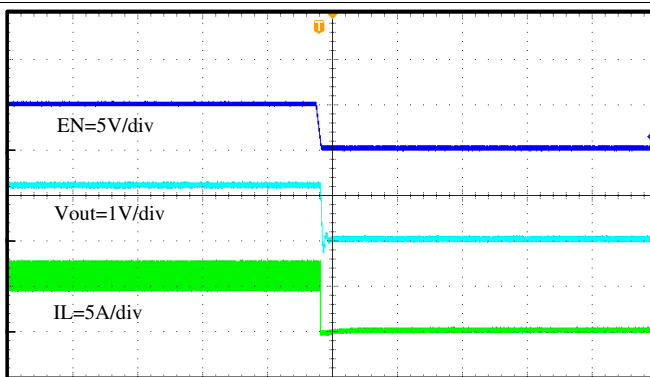
图 24. Line Regulation



$I_{OUT} = 6A$

800us/div

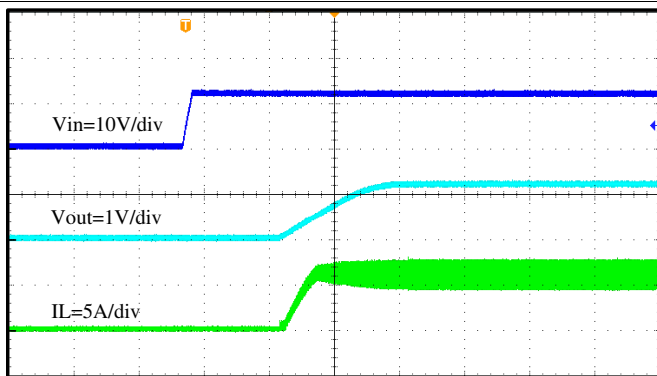
图 25. Start-Up Through EN



$I_{OUT} = 6A$

800us/div

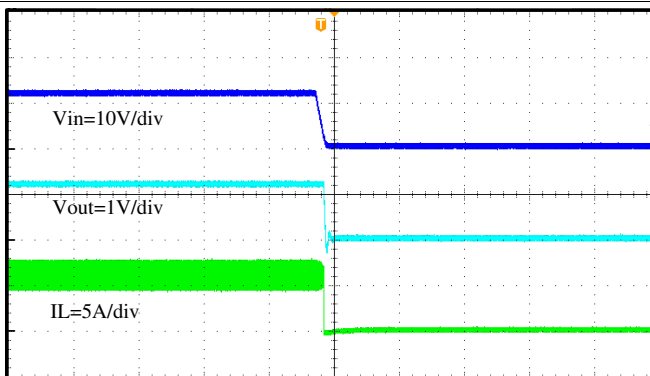
图 26. Shut-down Through EN



$I_{OUT} = 6 A$

800us/div

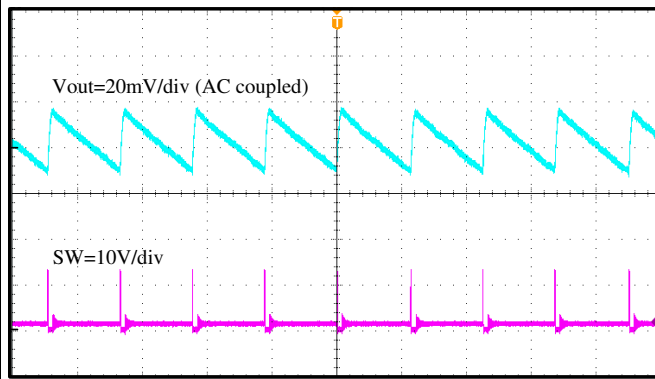
图 27. Start Up Relative to  $V_{IN}$  Rising



$I_{OUT} = 6 A$

800us/div

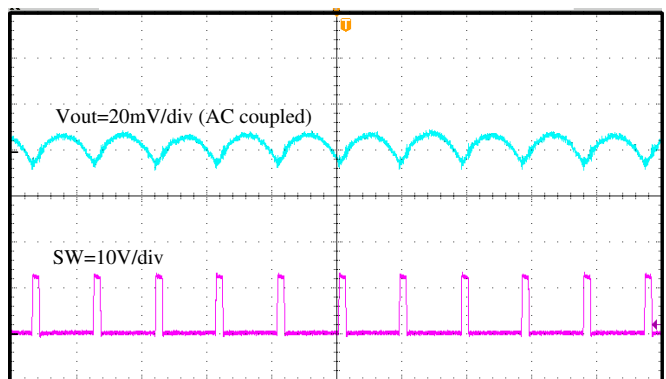
图 28. Shut Down Relative to  $V_{IN}$  Falling



$I_{OUT} = 0.1 \text{ A}$

20us/div

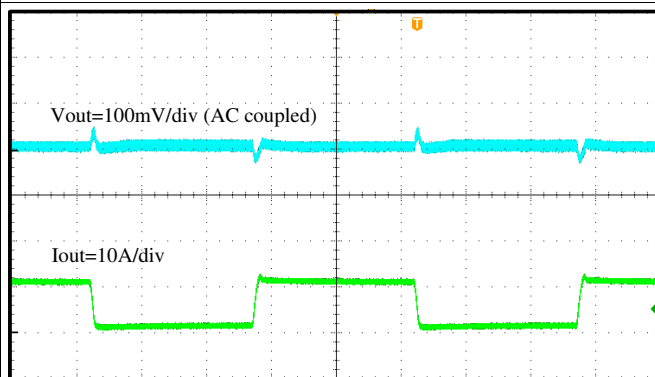
图 29. Output Voltage Ripple



$I_{OUT} = 12 \text{ A}$

2us/div

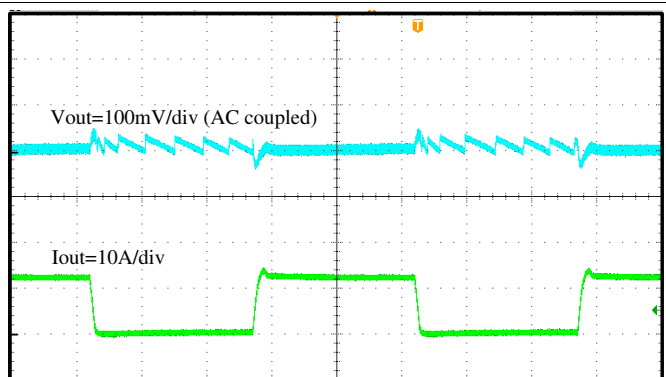
图 30. Output Voltage Ripple



1.2 A to 10.8 A

200us/div  
Slew Rate=2.5A/us

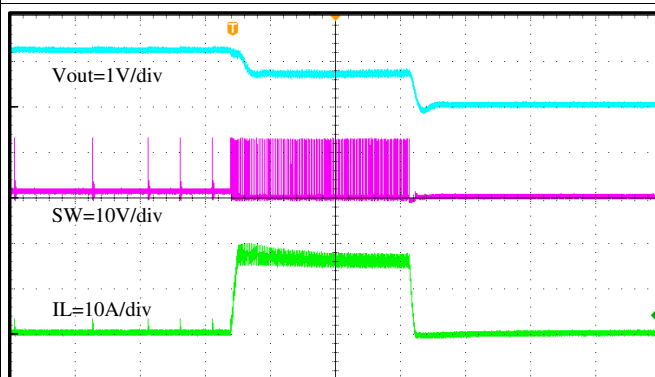
图 31. Transient Response



0 A to 12 A

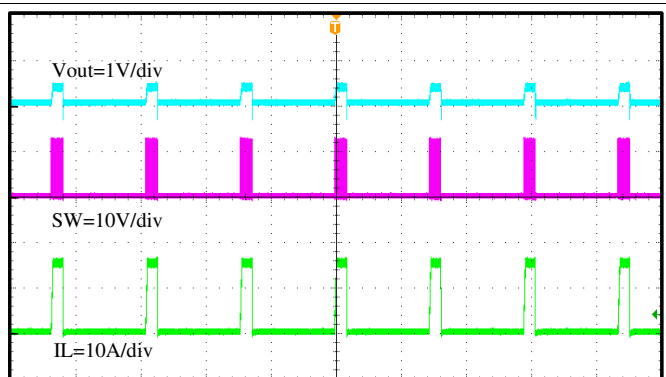
200us/div  
Slew Rate=2.5A/us

图 32. Transient Response



100us/div

图 33. Normal Operation to Output Hard Short



10ms/div

图 34. Output Hard Short Hiccup Protection

## 10 Power Supply Recommendations

The TPS56C230 is intended to be powered by a well regulated DC voltage. The input voltage range is 4.5 V to 18 V. TPS56C230 is a buck converter. The input supply voltage must be greater than the desired output voltage for proper operation. Input supply current must be appropriate for the desired output current. If the input voltage supply is located far from the TPS56C230 circuit, some additional input bulk capacitance is recommended. Typical values are 100  $\mu$ F to 470  $\mu$ F.

## 11 Layout

### 11.1 Layout Guidelines

- Recommend a four-layer PCB for good thermal performance and with maximum ground plane. 3-inch x 2.75-inch, two-layer PCB with 2-oz copper used as example.
- Place the decoupling capacitors right across VIN and VCC as close as possible.
- Place output inductors and capacitors with IC at the same layer, SW routing should be as short as possible to minimize EMI, and should be a width plane to carry big current, enough vias should be added to the GND connection of output capacitors and also as close to the output pin as possible.
- Place BST resistor and capacitor with IC at the same layer, close to BST and SW plane, >15 mil width trace is recommended to reduce line parasitic inductance.
- Feedback could be 20mil and must be routed away from the switching node, BST node or other high efficiency signal.
- VIN trace must be wide to reduce the trace impedance and provide enough current capability.
- Place multiple vias under the device near VIN and GND and near input capacitors to reduce parasitic inductance and improve thermal performance

### 11.2 Layout Example

Figure 35 shows the recommended top-side layout. Component reference designators are the same as the circuit shown in Figure 18.

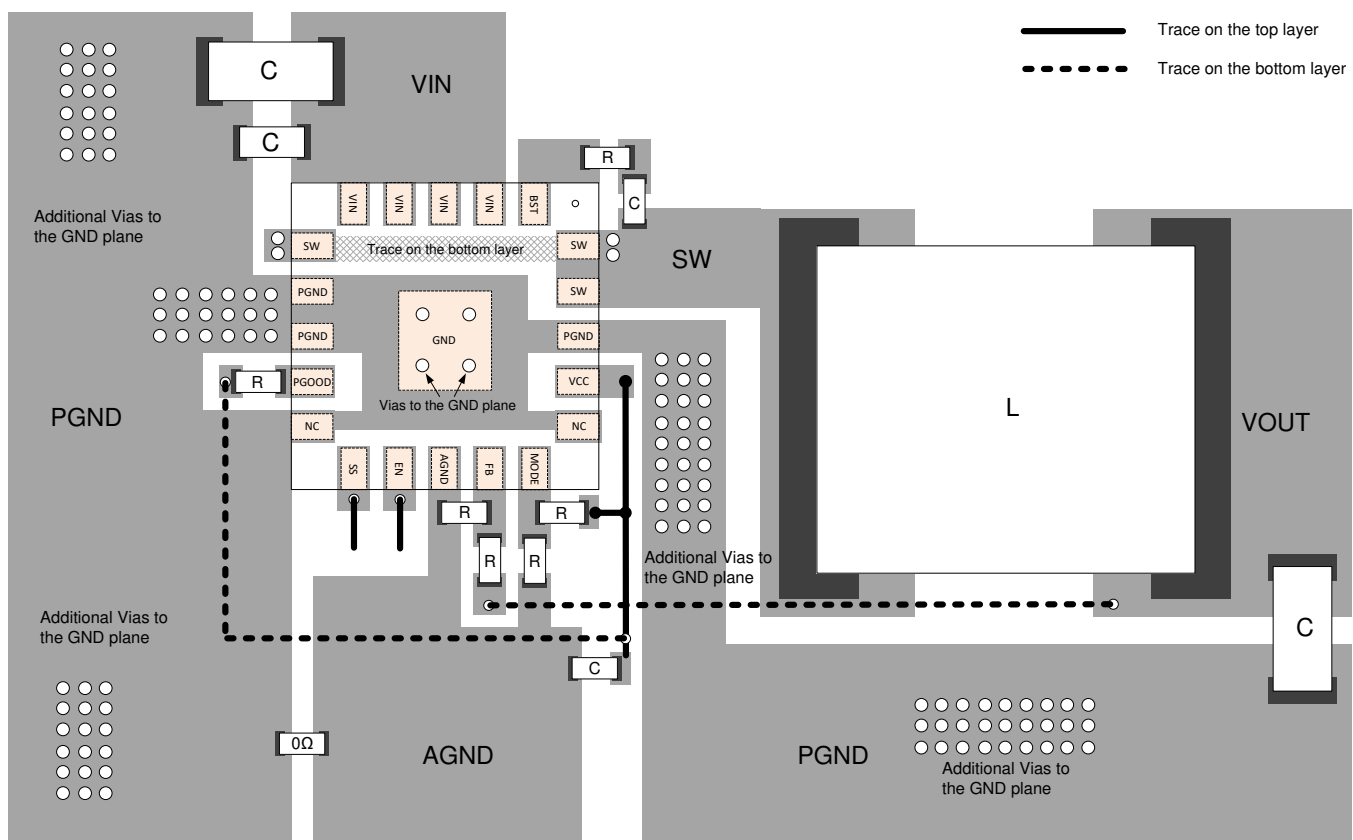


Figure 35. PCB Layout Recommendation Diagram

## 12 デバイスおよびドキュメントのサポート

### 12.1 デバイス・サポート

#### 12.1.1 デベロッパー・ネットワークの製品に関する免責事項

デベロッパー・ネットワークの製品またはサービスに関するTIの出版物は、単独またはTIの製品、サービスと一緒に提供される場合に関係なく、デベロッパー・ネットワークの製品またはサービスの適合性に関する是認、デベロッパー・ネットワークの製品またはサービスの是認の表明を意味するものではありません。

#### 12.1.2 開発サポート

##### 12.1.2.1 WEBENCH®ツールによるカスタム設計

[ここをクリック](#)すると、WEBENCH® Power Designer により、TPS56C230 デバイスを使用するカスタム設計を作成できます。

1. 最初に、入力電圧( $V_{IN}$ )、出力電圧( $V_{OUT}$ )、出力電流( $I_{OUT}$ )の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他の方式と比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

通常、次の操作を実行可能です。

- 電氣的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットで出力する。
- 設計のレポートをPDFで印刷し、設計を共有する。

WEBENCHツールの詳細は、[www.ti.com/WEBENCH](http://www.ti.com/WEBENCH)でご覧になれます。

### 12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com)のデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 12.3 コミュニティ・リソース

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 12.4 商標

D-CAP3, Eco-mode, HotRod, E2E are trademarks of Texas Instruments.

WEBENCH is a registered trademark of Texas Instruments.

### 12.5 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

### 12.6 Glossary

[SLYZ022](#) — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

### 13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

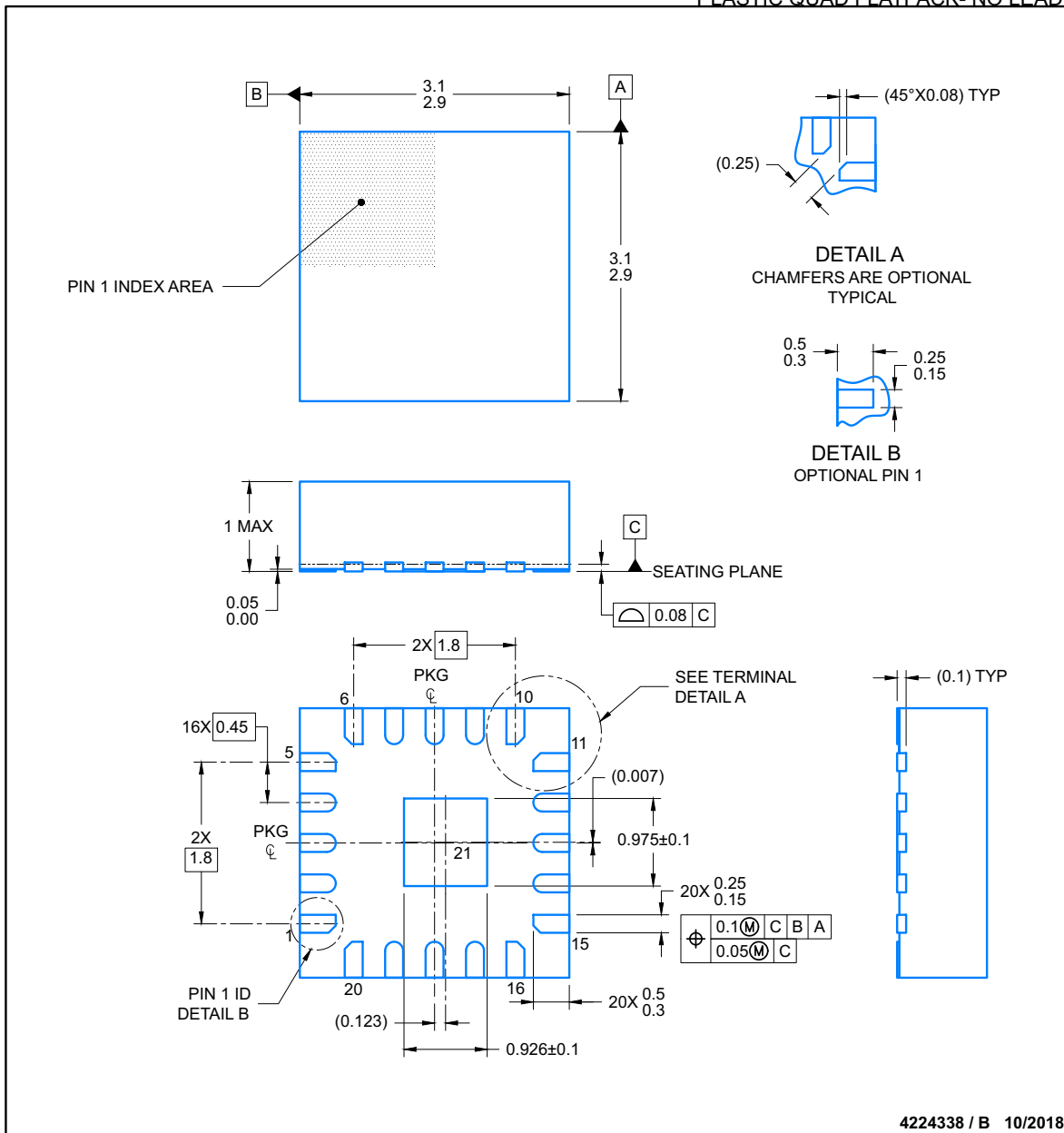


**PACKAGE OUTLINE**

**RJF0020B**

**VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK- NO LEAD



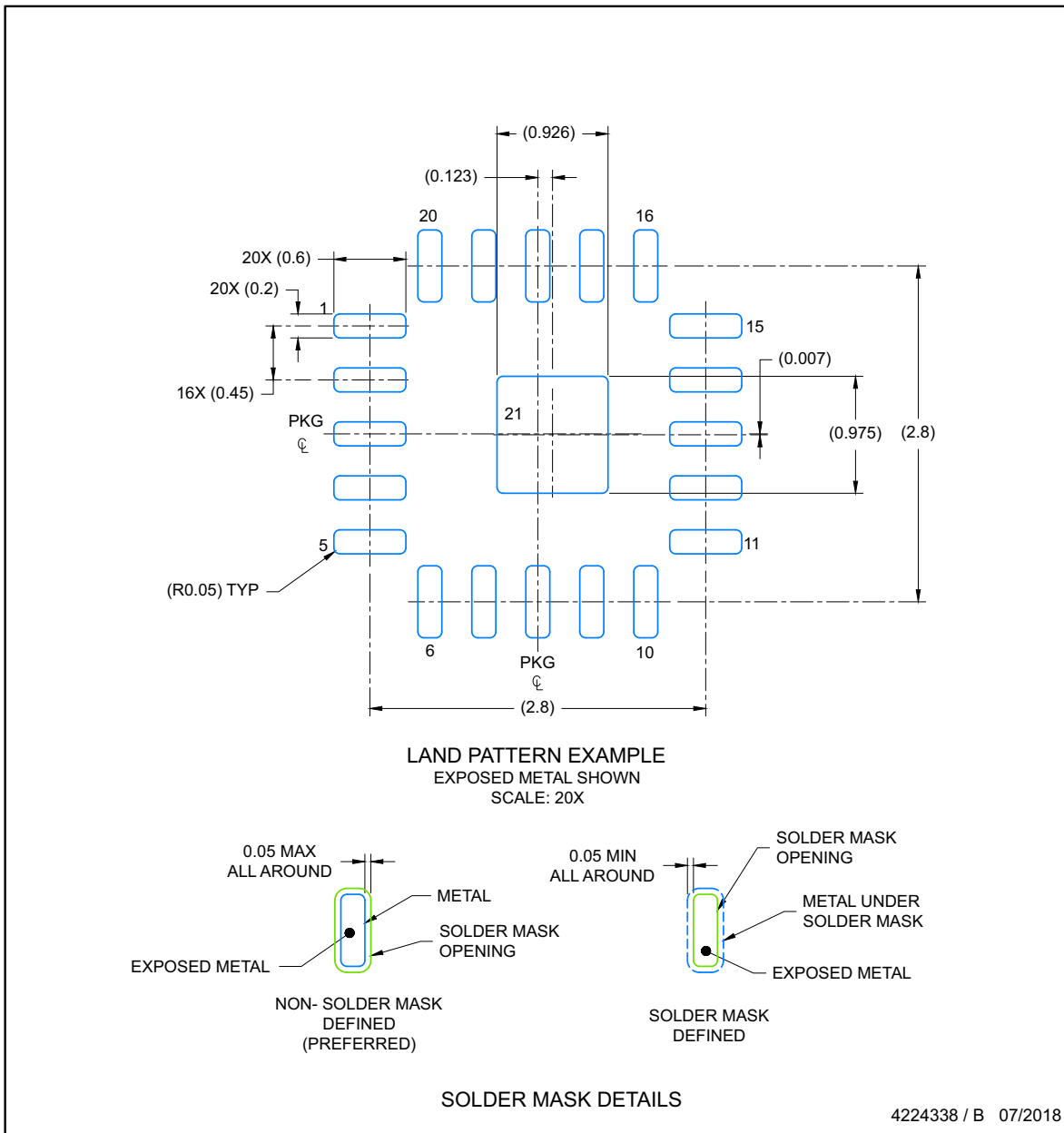
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

**EXAMPLE BOARD LAYOUT**  
**VQFN-HR - 1 mm max height**

**RJE0020B**

PLASTIC QUAD FLATPACK- NO LEAD



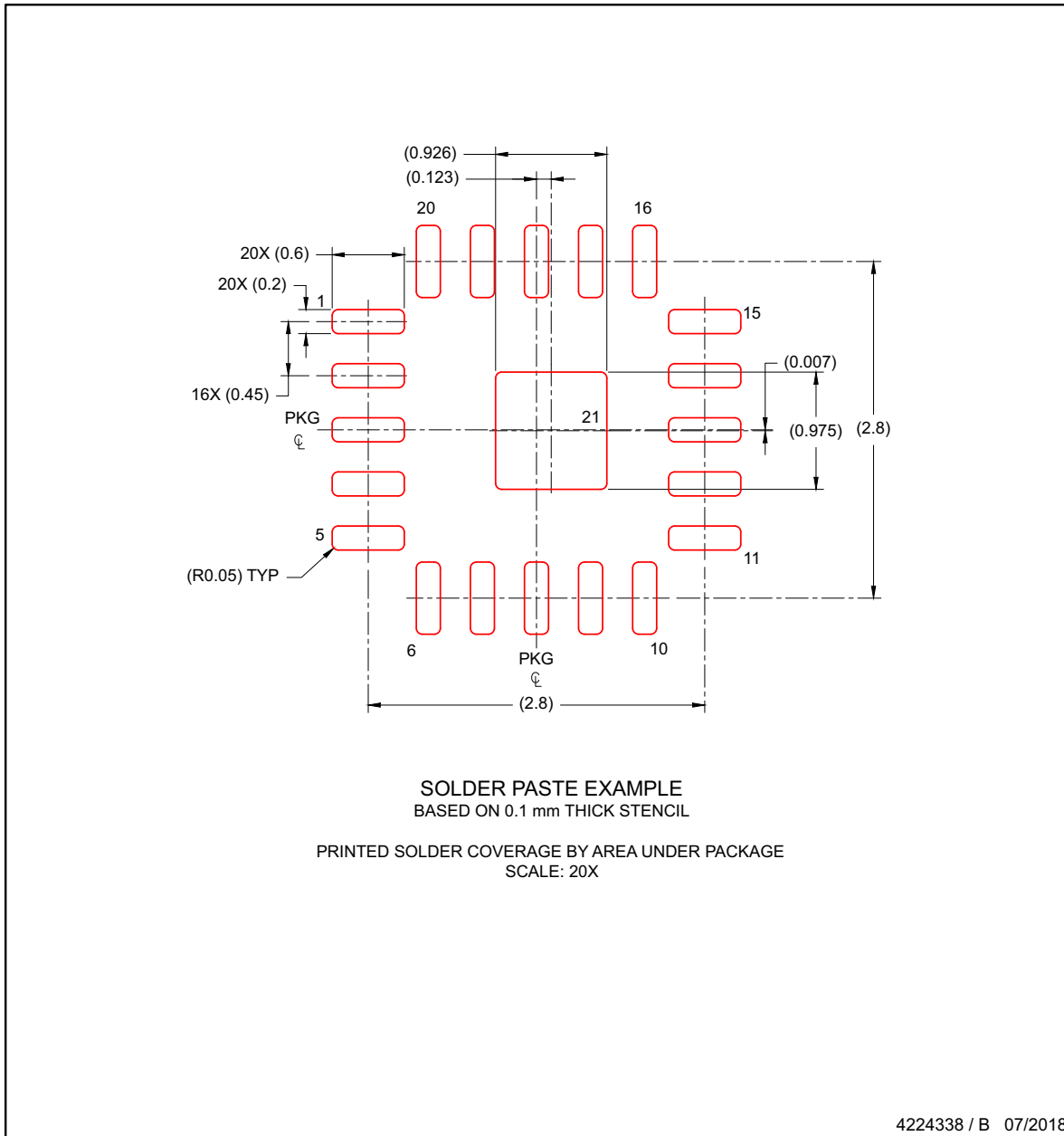
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN VQFN-HR - 1 mm max height

RJE0020B

PLASTIC QUAD FLATPACK- NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS56C230RJR	ACTIVE	VQFN-HR	RJE	20	3000	RoHS & Green	Call TI   SN   NIPDAU	Level-2-260C-1 YEAR	-40 to 125	56C230	<a href="#">Samples</a>
XTPS56C230RJET	OBSOLETE	VQFN-HR	RJE	20		TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS56C230RJR	VQFN-HR	RJE	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS56C230RJER	VQFN-HR	RJE	20	3000	346.0	346.0	33.0

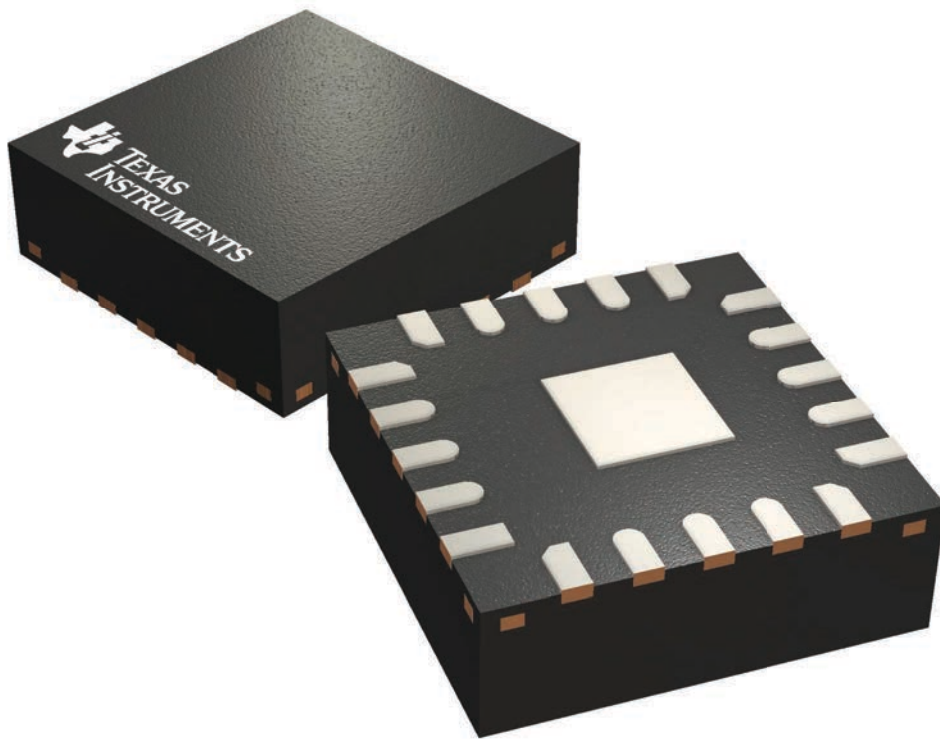
## GENERIC PACKAGE VIEW

**RJE 20**

**VQFN-HR - 1 mm max height**

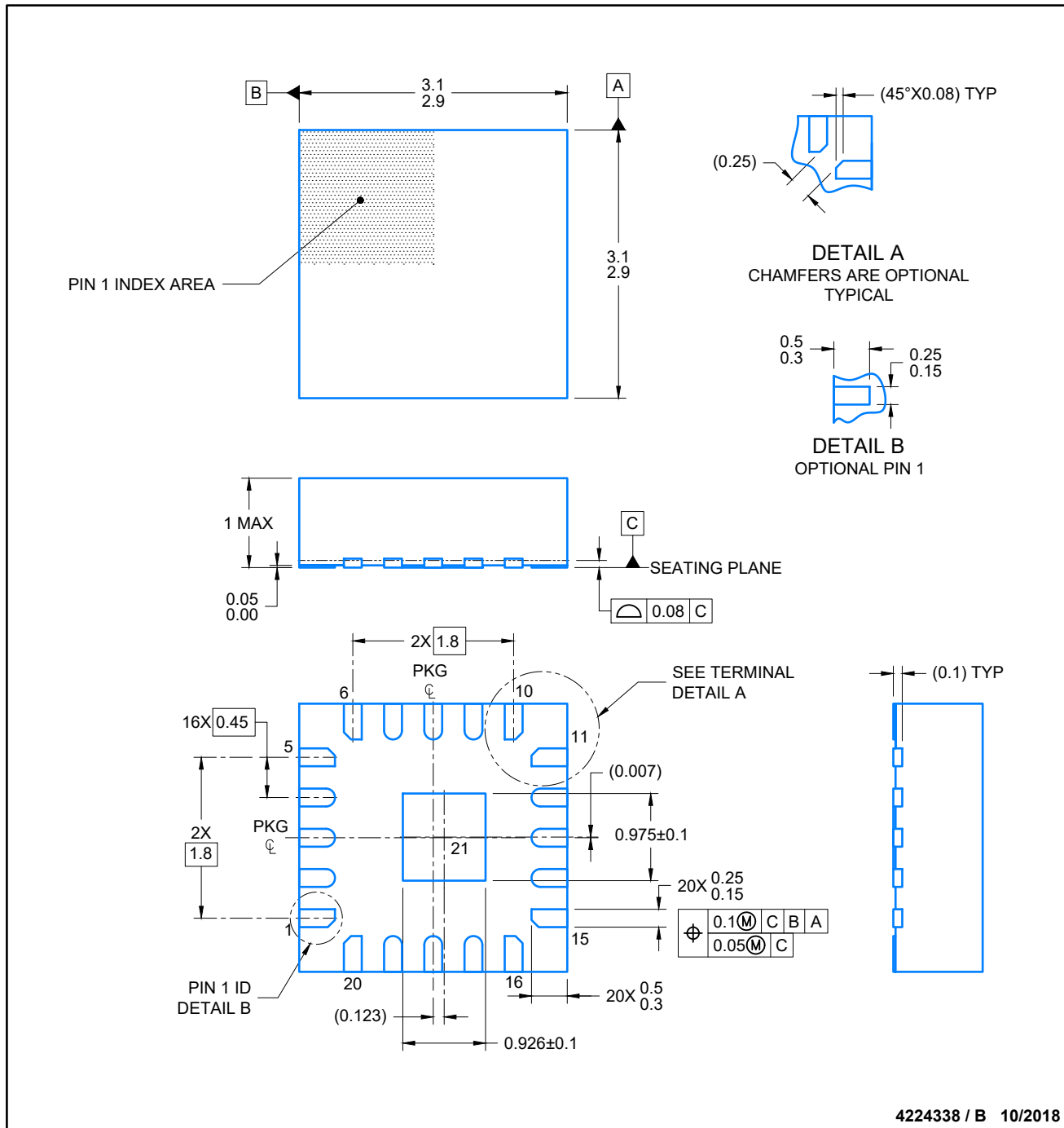
3 x 3, 0.45 mm pitch

QUAD FLATPACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

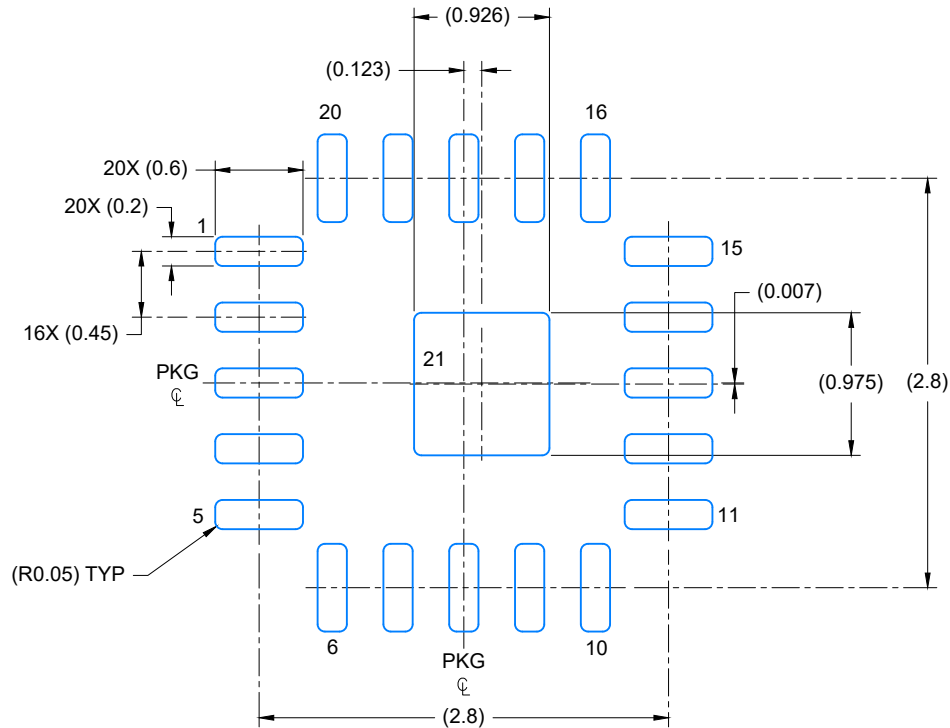
4224683/A



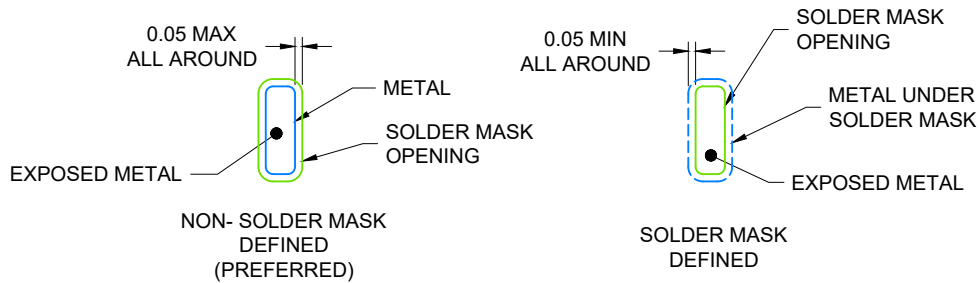
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.





LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X

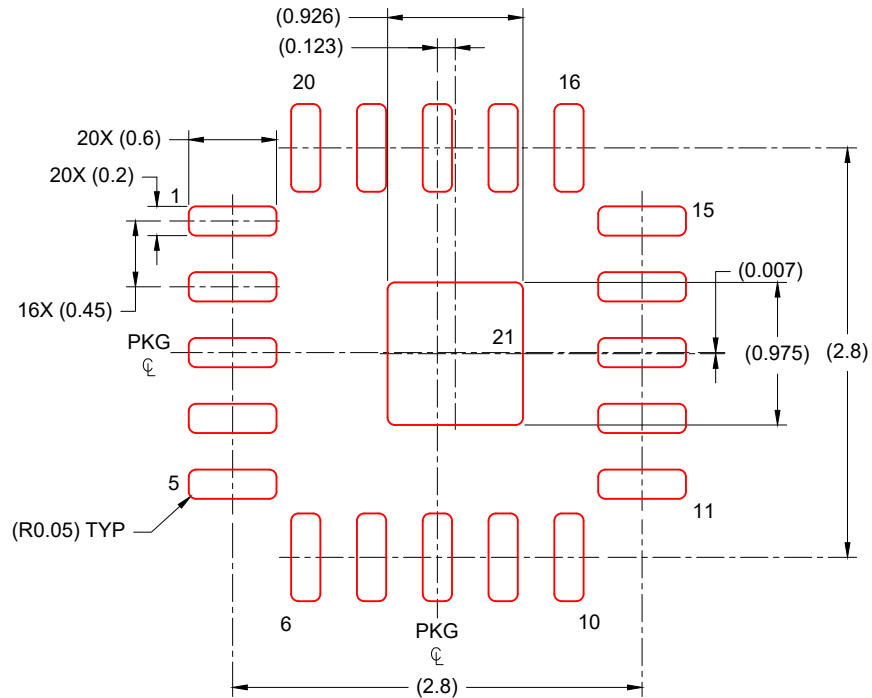


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
 BASED ON 0.1 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
 SCALE: 20X

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NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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