

# TPS59632-Q1 車載 ADAS アプリケーション用の 2.5V~24V、3 相、2 相、単相降圧型ドライバレス・コントローラ

## 1 特長

- 車載アプリケーション用に AEC-Q100 認定済み
  - 温度グレード 1: -40°C~125°C
  - 人体モデル ESD 分類レベル H2
  - 荷電デバイス・モデル ESD 分類レベル C3B
- 位相数 (3、2、1) を選択可能
- 2.5V~24V の変換電圧範囲 (位相数、スイッチング周波数、最大出力電圧によって制限されます)
- 7 ビット DAC 電圧範囲: 0.50V~1.52V
- 0.800V の DAC 電圧によるプリセット・ブート
- 高精度で調整可能な DC 負荷ライン (ドループ) またはゼロ勾配の負荷ライン
- D-CAP+™ 制御による高速な過渡応答
- 特許取得の AutoBalance™ フェーズ・バラランシング
- 300kHz~1MHz の 8 つのスイッチング周波数設定
- それぞれ 8 レベルの出力電圧オーバーシュート低減 (OSR) およびアンダーシュート低減 (USR)
- 8 レベルの電流制限を選択可能
- 負荷電流モニタ (アナログおよびデジタル)
- 8 レベルの電圧スルーレートを選擇可能
- 軽負荷と重負荷の両方で効率を最適化
- 8 つのデバイス・アドレスに対応した VID 制御、位相管理、テレメトリーのための I<sup>2</sup>C インターフェイス
- ウェットアップ・フランク付きの 5mm x 5mm、32 ピン、0.5mm ピッチの QFN パワーパッド・パッケージ

## 2 アプリケーション

- 先進運転支援システム (ADAS)
- 条件付き自動化ドライブ・コントローラ
- 車載インフォテインメントおよびクラスタ

## 3 概要

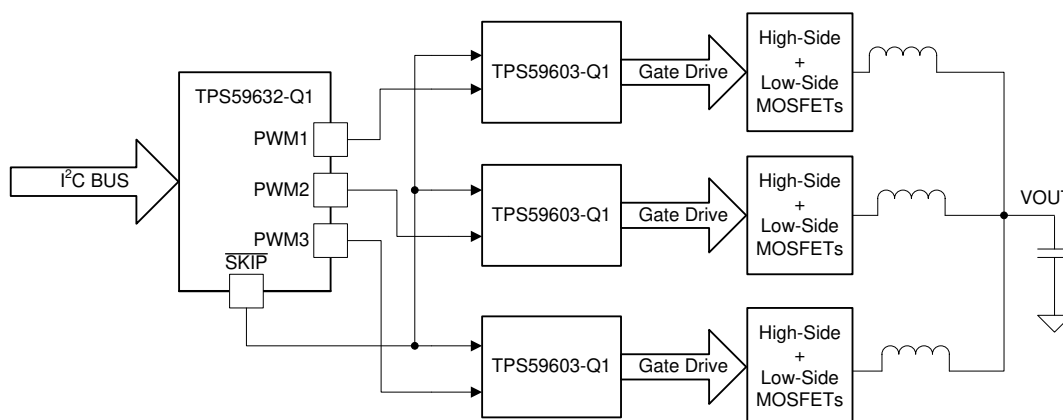
TPS59632-Q1 デバイスは、出力電圧オーバーシュート低減 (OSR) およびアンダーシュート低減 (USR) 機能によって非常に高速な過渡応答、最小限の出力容量、高い効率を実現する D-CAP+™ 制御アーキテクチャなどの先進機能を備えた 3 相ドライバレス降圧型コントローラです。このデバイスは、I<sup>2</sup>C による出力電圧の動的制御、位相管理による効率の最適化、電流モニタ・テレメトリーをサポートしています。TPS59603-Q1 の MOSFET ゲートドライバは、このコントローラと組み合わせて同期整流降圧型コンバータの電力段 MOSFET を駆動することに特化して設計されています。TPS59632-Q1 デバイスは 5mm x 5mm の省スペースで熱的に強化された 32 ピン、0.5mm ピッチの QFN パッケージで供給され、-40°C~125°C の温度範囲で動作が規定されています。

### 製品情報<sup>(1)</sup>

型番	パッケージ	本体サイズ (公称)
TPS59632-Q1	VQFN (32)	5mmx5mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

### アプリケーション概略図



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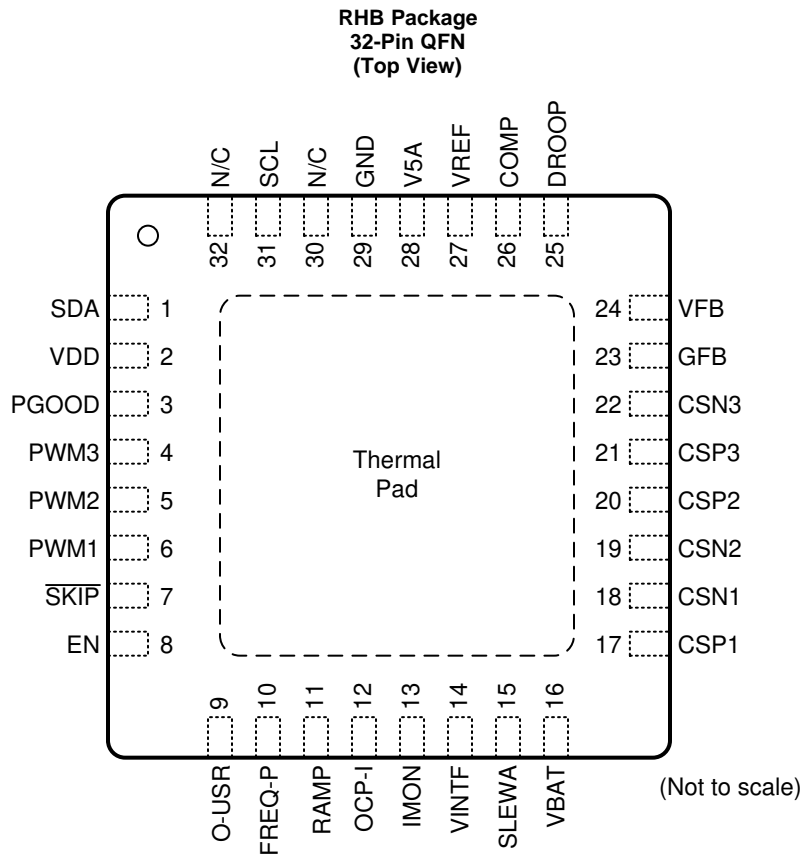
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## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

日付	リビジョン	注
2020年2月	*	初版

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COMP	26	I	Error amplifier summing node. Resistors from VREF to COMP ( $R_{COMP}$ ) and COMP to DROOP ( $R_{DROOP}$ ) set the droop gain.
CSP1	17	I	Positive current sense inputs. Connect to the most positive node of current sense resistor or inductor DCR sense network. Tie CSP3, CSP2, or CSP1 (in that order) to 3.3 V to disable the phase.
CSP2	20		
CSP3	21		
CSN1	18	I	Negative current sense inputs. Connect to the most negative node of current sense resistor or inductor DCR sense network. CSN1 has a secondary OVP comparator and includes the soft-stop pulldown transistor.
CSN2	19		
CSN3	22		
DROOP	25	O	Error amplifier output. A resistor pair from VREF to COMP to DROOP sets the droop gain. $A_{DROOP} = 1 + R_{DROOP} / R_{COMP}$ .
EN	8	I	Enable; 100-ns de-bounce. Regulator enters low-power mode, but retains start-up settings when brought low.
FREQ-P	10	I	R to GND sets the per phase switching frequency. MUST connect a resistor to VREF to ensure this pin voltage is above 0.8 V for proper operation.
GFB	23	I	Voltage sense return. Tie to GND on PCB with a 10- $\Omega$ resistor to provide feedback when $\mu$ P is not populated.
GND	29	–	Analog circuit reference; tie to a quiet point on the ground plane.
IMON	13	O	Analog current monitor output. $V_{IMON} = \sum V_{ISENSE} \times (1 + R_{IMON} / R_{OCP})$ .
OCP-I	12	I/O	Voltage divider to IMON. Resistor ratio sets the IMON gain (see IMON pin). R to GND ( $R_{OCP}$ ) selects 1 of 8 OCP levels (per phase, latched at start-up).

**Pin Functions (continued)**

PIN		I/O	DESCRIPTION
NAME	NO.		
O-USR	9	I	Voltage divider to the VREG pin. Connect a resistor to GND to select the pulse-truncation level and OSR level. Voltage at O-USR selects the USR level.
PU	9	I	Provides pullup resistance to VREF through 10-k $\Omega$ resistor.
PAD	GND	–	Thermal pad; tie to the ground plane with multiple vias.
PGOOD	3	O	Power Good output; Open-drain. PGOOD can be configured to go low when the current reaches 70% of the OCP setting value.
PWM1	6	O	PWM controls for the external driver; 5-V logic level. Controller forces signal to the 3-state level when needed.
PWM2	5		
PWM3	4		
RAMP	11	I	Voltage divider to VREF. Connect a resistor to GND to set the ramp setting voltage. The RAMP setting can override the factory ramp setting.
NC	30	NC	No connect. Leave pins floating.
	32		
SCL	31	I	I <sup>2</sup> C digital clock line.
SDA	1	I/O	I <sup>2</sup> C digital data line.
$\overline{\text{SKIP}}$	7	O	This pin is active high to operate synchronous buck MOSFETs in Forced Continuous Conduction Mode (FCCM) active low for skip mode operation. This pin must be connected to the corresponding pin of the drivers for this function.
SLEWA	15	I	The voltage sets the 3 LSBs of the I <sup>2</sup> C address. The resistance to GND selects 1 of 8 slew rates. The start-up slew rate (EN transitions high) is SLEWRATE / 2. The ADDRESS and SLEWRATE values are latched at start-up.
VINTF	14	I	Input voltage to power I <sup>2</sup> C interface logic. Can be tied to VDD if 3.3-V logic signals are needed.
V5A	28	I	5-V power input for analog circuits; connect through resistor to 5-V plane and bypass to GND with $\geq 1\text{-}\mu\text{F}$ ceramic capacitor
VBAT	16	I	10-k $\Omega$ resistor to VBAT provides VBAT information to the on-time circuits for both converters.
VDD	2	I	3.3-V digital power input; bypass to GND with $\geq 1\text{-}\mu\text{F}$ capacitor.
VFB	24	I	Voltage sense line. Tie directly to V <sub>OUT</sub> sense point of processor. Tie to V <sub>OUT</sub> on PCB with a 10- $\Omega$ resistor to provide feedback when the microprocessor is not populated. The resistance between VFB and GFB is $> 1\text{ M}\Omega$ .
VREF	27	O	1.7-V, 500- $\mu\text{A}$ reference. Bypass to GND with a 0.22- $\mu\text{F}$ ceramic capacitor.

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	V5A	-0.3	6.0	V
	VDD, O-USR, RAMP, OCP-I, VFB, CSP1, CSP2, CSP3, CSN1, CSN2, CSN3, VINTF, SDA, SCL, FREQ-P, SLEWA, EN, NC	-0.3	3.6	
	VBAT	-0.3	30	
	COMP	-0.3	3.6	
	GFB	-0.2	0.2	
Output voltage	PGOOD, IMON, VREF, DROOP	-0.3	3.6	V
	PWM3, PWM2, PWM1, $\overline{\text{SKIP}}$	-0.3	6.0	
Junction temperature range, $T_J$		-40	150	°C
Storage Temperature $T_{\text{stg}}$		-55	150	°C

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{\text{(ESD)}}$	Electrostatic Discharge	Human body model (HBM), per AEC-Q100 Classification Level H2	±2000
		Charged device model (CDM), per AEC-Q100 Classification Level C3B	±750

### 6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	V5A	-0.1	5.5	V
	VDD, O-USR, RAMP, OCP-I, VFB, CSP1, CSP2, CSP3, CSN1, CSN2, CSN3, VINTF, SDA, SCL, FREQ-P, SLEWA, EN, NC	-0.1	3.5	
	VBAT	-0.1	28	
	COMP	-0.1	3.5	
	GFB	-0.1	0.1	
Output voltage	PGOOD, IMON, VREF, DROOP	-0.1	3.5	V
	PWM3, PWM2, PWM1, $\overline{\text{SKIP}}$	-0.1	5.5	
Operating junction temperature, $T_J$		-40	125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS59632-Q1	UNITS
		RSM (VQFN)	
		32 PINS	
$R_{\theta\text{JA}}$	Junction-to-ambient thermal resistance	37.2	°C/W
$R_{\theta\text{Jctop}}$	Junction-to-case (top) thermal resistance	31.9	
$R_{\theta\text{JB}}$	Junction-to-board thermal resistance	8.1	
$\Psi_{\text{JT}}$	Junction-to-top characterization parameter	0.4	
$\Psi_{\text{JB}}$	Junction-to-board characterization parameter	7.9	
$R_{\theta\text{Jcbot}}$	Junction-to-case (bottom) thermal resistance	2.2	

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#)

## 6.5 Electrical Characteristics

Over recommended temperature range,  $4.5\text{ V} \leq V_{V5A} \leq 5.5\text{ V}$ ,  $3.0\text{ V} \leq V_{VDD} \leq 3.6\text{ V}$ ,  $V_{GFB} = \text{GND}$ ,  $V_{VFB} = V_{OUT}$ ,  $0.7 < \text{VFREQ}$ - $P \leq V_{VREF}$  (unless otherwise noted).

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT		
<b>POWER SUPPLY: CURRENTS, UVLO AND POWER-ON-RESET</b>							
$I_{V5-3P}$	V5A supply current, 3-phase	$V_{VDAC} < V_{VFB} < (V_{VDAC} + 100\text{ mV})$ , EN = 'HI'		3.6	6.0	mA	
$I_{VDD-3P}$	VDD supply current, 3-phase	$V_{VDAC} < V_{VFB} < (V_{VDAC} + 100\text{ mV})$ , EN = 'HI'; digital buses idle		0.2	0.8		
$I_{V5-1P}$	V5A supply current, 1-phase	$V_{VDAC} < V_{VFB} < (V_{VDAC} + 100\text{ mV})$ , EN = 'HI'		3.5	6.0		
$I_{VDD-1P}$	VDD supply current, 1-phase	$V_{VDAC} < V_{VFB} < (V_{VDAC} + 100\text{ mV})$ , EN = 'HI'; digital buses idle		0.2	0.8		
$I_{V5STBY}$	V5A standby current	EN = 'LO'		125	200	μA	
$I_{VDDSTBY}$	VDD standby current	EN = 'LO'		23	40		
$I_{VINTF}$	VINTF supply current	All conditions; digital buses idle		1.7	5.0	V	
$V_{UVLOH}$	V5A UVLO 'OK' threshold	$V_{VFB} < 200\text{ mV}$ . Ramp up; $V_{VDD} > 3\text{ V}$ ; EN = 'HI'; Switching begins.		4.2	4.4		4.52
$V_{UVLOL}$	V5A UVLO fault threshold	Ramp down; EN = 'HI'; $V_{VDD} > 3\text{ V}$ ; $V_{VFB} = 100\text{ mV}$ . Switching stops		4.00	4.2		4.35
$V_{5POR}$	V5A fault latch reset threshold	Ramp down. EN = 'HI'; $V_{VDD} > 3\text{ V}$ . Can restart if V5A rises to $V_{UVLOH}$ , and no other faults present.		1.2	1.9		2.5
$V_{3UVLOH}$	VDD UVLO 'OK' threshold	$V_{VFB} < 200\text{ mV}$ . Ramp up; $V_{V5A} > 4.5\text{ V}$ ; EN = 'HI'; Switching begins.		2.5	2.8		3.0
$V_{3UVLOL}$	Fault threshold	Ramp down; EN = 'HI'; $V_{V5A} > 4.5\text{ V}$ ; $V_{VFB} = 100\text{ mV}$ . Switching stops.		2.4	2.6		2.8
$V_{3POR}$	VDD fault latch	Ramp down. EN = 'HI'; $V_{V5A} > 4.5\text{ V}$ . Can restart if VDD goes up to $V_{3UVLOH}$ , and no other faults present.		1.2	1.9		2.5
$V_{INTFUUVLOH}$	VINTF UVLO OK	Ramp up; EN = 'HI'; $V_{V5A} > 4.5\text{ V}$ ; $V_{VFB} = 100\text{ mV}$ .		1.4	1.5		1.6
$V_{INTFUUVLOL}$	VINTF UVLO falling	Ramp down; EN = 'HI'; $V_{V5A} > 4.5\text{ V}$ ; $V_{VFB} = 100\text{ mV}$ .		1.3	1.4		1.5
<b>REFERENCES: VDAC, VREF, BOOT Voltage</b>							
$V_{VIDSTP}$	VID step size	Change VID0 HI to LO to HI		10		mV	
$V_{DAC1}$	VFB tolerance	$1.36\text{ V} \leq V_{VFB} \leq 1.52\text{ V}$ , $I_{OUT} = 0\text{ A}$		-9	9		
$V_{DAC2}$		$1.0\text{ V} \leq V_{VFB} \leq 1.35\text{ V}$ ; $I_{OUT} = 0\text{ A}$		-8	8		
$V_{DAC3}$		$0.5\text{ V} \leq V_{VFB} \leq 0.99\text{ V}$ ; $I_{OUT} = 0\text{ A}$		-7	7		
$V_{VREF}$	VREF output	$V_{VREF}$ output $4.5\text{ V} \leq V_{V5A} \leq 5.5\text{ V}$ , $I_{VREF} = 0\text{ A}$		1.66	1.700	1.74	V
$V_{VREFSRC}$	VREF output source	$0\text{ A} \leq I_{REF} \leq 500\text{ μA}$ , HP-2		-4	-3		mV
$V_{VREFSNK}$	VREF output sink	$-500\text{ A} \leq I_{REF} \leq 0\text{ A}$ , HP-2		3	4		
$V_{VBOOT}$	Internal VFB initial boot voltage	Initial DAC boot voltage		0.8			V
<b>DIFFERENTIAL VOLTAGE SENSE: VFB AND GFB</b>							
$R_{VFB}$	VFB/GFB Input resistance	Not in fault, disable, or UVLO, $V_{VFB} = V_{VDAC} = 1.5\text{ V}$ , $V_{GFB} = 0\text{ V}$ , measure from VFB to GFB		50			MΩ
$V_{DELGND}$	GFB Differential	GND to GFB		±100			mV
<b>ERROR AMPLIFIER, CURRENT AMPLIFIER, CURRENT SHARE</b>							
$A_{V-EA}$	Error amplifier total voltage gain <sup>(1)</sup>	VFB to DROOP		80			dB
$I_{EA\_SR}$	Error amplifier source current	$I_{DROOP}$ , $V_{VFB} = V_{VDAC} + 50\text{ mV}$ , $R_{COMP} = 1\text{ kΩ}$		1			mA
$I_{EA\_SK}$	Error amplifier sink current	$I_{DROOP}$ , $V_{VFB} = V_{VDAC} - 50\text{ mV}$ , $R_{COMP} = 1\text{ kΩ}$		-1			
$I_{CS}$	CS pin input bias current	CSPx and CSNx		-500	0.2	500	nA
$A_{CSINT}$	Internal current sense gain	Gain from CSPx – CSNx to PWM comparator, $R_{SKIP} = \text{Open}$		5.8	6.0	6.2	V/V
$I_{BAL\_TOL}$	Internal current share tolerance	$V_{VDAC} = 1.70\text{ V}$ , $V_{CSP1} - V_{CSN1} = V_{CSP2} - V_{CSN2} = V_{CSP3} - V_{CSN3} = V_{OCP\_MIN}$		-3%		+3%	

(1) Specified by design. Not production tested.

## Electrical Characteristics (continued)

Over recommended temperature range,  $4.5\text{ V} \leq V_{V5A} \leq 5.5\text{ V}$ ,  $3.0\text{ V} \leq V_{VDD} \leq 3.6\text{ V}$ ,  $V_{GFB} = \text{GND}$ ,  $V_{VFB} = V_{\text{OUT}}$ ,  $0.7 < \text{VFREQ}$ - $P \leq V_{VREF}$  (unless otherwise noted).

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
<b>RAMP SETTINGS</b>						
$V_{\text{RAMP}}$	Compensation ramp amplitude	$R_{\text{RAMP}} = 20\text{ k}\Omega \pm 1\%$		20		mV
		$R_{\text{RAMP}} = 30\text{ k}\Omega \pm 1\%$		60		
		$R_{\text{RAMP}} = 39\text{ k}\Omega \pm 1\%$		100		
		$R_{\text{RAMP}} \geq 150\text{ k}\Omega \pm 1\%$		40		
<b>SLEW SETTINGS</b>						
$SL_{\text{SET}}$	Slew rate setting for VID change	$R_{\text{SLEW}} = 20\text{ k}\Omega \pm 1\%$	6		10	mV/ $\mu\text{s}$
		$R_{\text{SLEW}} = 24\text{ k}\Omega \pm 1\%$	12		20	
		$R_{\text{SLEW}} = 30\text{ k}\Omega \pm 1\%$	18		30	
		$R_{\text{SLEW}} = 39\text{ k}\Omega \pm 1\%$	24		40	
$SL_{\text{START}}$	Slew rate setting for start-up <sup>(2)</sup>	EN goes high, $R_{\text{SLEW}} = 20\text{ k}\Omega$	3		5	mV/ $\mu\text{s}$
<b>ADDRESS SETTINGS</b>						
ADDR	Address setting 3 LSB of I <sup>2</sup> C Address (ADDR = 100 0xxx)	$V_{\text{SLEWA}} \leq 0.25\text{ V}$		000b		
		$0.35\text{ V} \leq V_{\text{SLEWA}} \leq 0.45\text{ V}$		001b		
		$0.55\text{ V} \leq V_{\text{SLEWA}} \leq 0.65\text{ V}$		010b		
		$0.75\text{ V} \leq V_{\text{SLEWA}} \leq 0.85\text{ V}$		011b		
		$0.95\text{ V} \leq V_{\text{SLEWA}} \leq 1.05\text{ V}$		100b		
		$1.15\text{ V} \leq V_{\text{SLEWA}} \leq 1.25\text{ V}$		101b		
		$1.35\text{ V} \leq V_{\text{SLEWA}} \leq 1.45\text{ V}$		110b		
		$1.55\text{ V} \leq V_{\text{SLEWA}} \leq V_{\text{VREF}}$		111b		
<b>OVERSHOOT REDUCTION (OSR) SETTINGS</b>						
$V_{\text{OSR}}$	Overshoot Reduction (OSR) Voltage set <sup>(3)</sup>	$R_{\text{O-USR}} = 20\text{ k}\Omega \pm 1\%$		100		mV
		$R_{\text{O-USR}} = 24\text{ k}\Omega \pm 1\%$		150		
		$R_{\text{O-USR}} = 30\text{ k}\Omega \pm 1\%$		200		
		$R_{\text{O-USR}} = 39\text{ k}\Omega \pm 1\%$		250		
		$R_{\text{O-USR}} = 56\text{ k}\Omega \pm 1\%$		300		
		$R_{\text{O-USR}} = 75\text{ k}\Omega \pm 1\%$		400		
		$R_{\text{O-USR}} = 100\text{ k}\Omega \pm 1\%$		500		
		$R_{\text{O-USR}} = 150\text{ k}\Omega \pm 1\%$		OFF		
<b>UNDERSHOOT REDUCTION (USR) SETTINGS</b>						
$V_{\text{USR}}$	Undershoot Reduction (USR) Voltage set <sup>(4)</sup>	$V_{\text{O-USR}} < 0.25\text{ V}$		40		mV
		$0.35 < V_{\text{O-USR}} < 0.45\text{ V}$		60		
		$0.55 < V_{\text{O-USR}} < 0.65\text{ V}$		80		
		$0.75 < V_{\text{O-USR}} < 0.85\text{ V}$		120		
		$0.95 < V_{\text{O-USR}} < 1.05\text{ V}$		160		
		$1.15 < V_{\text{O-USR}} < 1.25\text{ V}$		200		
		$1.35 < V_{\text{O-USR}} < 1.45\text{ V}$		240		
		$1.55 < V_{\text{O-USR}} < V_{\text{VREF}}$		OFF		
<b>OVER CURRENT PROTECTION (OCP) SETTINGS</b>						

(2) Specified by design. Not production tested.

(3) Specified by design. Not production tested.

(4) Specified by design. Not production tested.

**Electrical Characteristics (continued)**

Over recommended temperature range,  $4.5\text{ V} \leq V_{V5A} \leq 5.5\text{ V}$ ,  $3.0\text{ V} \leq V_{VDD} \leq 3.6\text{ V}$ ,  $V_{GFB} = \text{GND}$ ,  $V_{VFB} = V_{OUT}$ ,  $0.7 < VFREQ$ ,  $P \leq V_{VREF}$  (unless otherwise noted).

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OCP}$	OCP voltage (valley current limit at CSPx – CSNx)	$R_{OCP-I} = 20\text{ k}\Omega \pm 1\%$	5.0	7.0	9.0	mV
		$R_{OCP-I} = 24\text{ k}\Omega \pm 1\%$	7.0	10.0	13.0	
		$R_{OCP-I} = 30\text{ k}\Omega \pm 1\%$	10.0	14.0	18.0	
		$R_{OCP-I} = 39\text{ k}\Omega \pm 1\%$	15.0	19.0	23.0	
		$R_{OCP-I} = 56\text{ k}\Omega \pm 1\%$	21.0	25.0	29.0	
		$R_{OCP-I} = 75\text{ k}\Omega \pm 1\%$	28.0	32.0	36.0	
		$R_{OCP-I} = 100\text{ k}\Omega \pm 1\%$	36.0	40.0	44.0	
		$R_{OCP-I} = 150\text{ k}\Omega \pm 1\%$	45.0	49.0	53.0	



## Electrical Characteristics (continued)

Over recommended temperature range,  $4.5\text{ V} \leq V_{V5A} \leq 5.5\text{ V}$ ,  $3.0\text{ V} \leq V_{VDD} \leq 3.6\text{ V}$ ,  $V_{GFB} = \text{GND}$ ,  $V_{VFB} = V_{\text{OUT}}$ ,  $0.7 < \text{VFREQ}$ - $P \leq V_{\text{VREF}}$  (unless otherwise noted).

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT			
<b>CURRENT MONITOR (IMON)</b>								
VAL <sub>ADC</sub>	IMON ADC output	$\Sigma\Delta\text{CS} = 0\text{ mV}$ , $A_{\text{IMON}} = 3.867$	00h	00h	03h			
		$\Sigma\Delta\text{CS} = 4.5\text{ mV}$ , $A_{\text{IMON}} = 3.867$	12h	19h	20h			
		$\Sigma\Delta\text{CS} = 22\text{ mV}$ , $A_{\text{IMON}} = 3.867$	79h	80h	87h			
		$\Sigma\Delta\text{CS} = 44\text{ mV}$ , $A_{\text{IMON}} = 3.867$	FAh	FFh	FFh			
LR <sub>IMON</sub>	IMON linear range	Each phase, CSPx – CSNx			50	mV		
<b>PROTECTION: OVP, UVP, PGOOD</b>								
V <sub>OVP</sub> H	Fixed OVP voltage	$V_{\text{CSN1}} > V_{\text{OVP}}\text{H}$ for 1 $\mu\text{s}$			1.60	1.70	1.80	V
R <sub>SFTSTP</sub>	Soft-stop transistor resistance	Connected to CSN1				100	200	$\Omega$
V <sub>PGDH</sub>	PGOOD high threshold	Measured at the VFB pin with respect to VID code, device latches OFF			185		245	mV
V <sub>PGDL</sub>	PGOOD low threshold	Measured at the VFB pin with respect to VID code, device latches OFF			-348		-280	
<b>PWM AND SKIP OUTPUTS: I/O VOLTAGE AND CURRENT</b>								
V <sub>P-S_L</sub>	PWMx / SKIP – Low	$I_{\text{LOAD}} = \pm 1\text{ mA}$				0.15	0.3	V
V <sub>P-S_H</sub>	PWMx / SKIP – High	$I_{\text{LOAD}} = \pm 1\text{ mA}$			4.2			
V <sub>PW-SCLK</sub>	PWMx / SKIP 3-state	$I_{\text{LOAD}} = \pm 100\ \mu\text{A}$			1.6	1.7	1.8	
<b>LOGIC INTERFACE: VOLTAGE AND CURRENT</b>								
R <sub>VRTTL</sub>	Pulldown resistance	SDA, $V = 0.31\text{ V}$			4		15	$\Omega$
R <sub>VRPG</sub>		PGOOD, $V = 0.31\text{ V}$				36	50	
I <sub>VRTTLK</sub>	Logic leakage current	SDA, SCL = 1.8 V, PGOOD = 3.3 V			-2	0.2	2	$\mu\text{A}$
V <sub>IL,I2C</sub>	Low-level input voltage	SCL, SDA, VINTF = 1.8 V					0.6	V
V <sub>IH,I2C</sub>	High-level input voltage				1.2			
V <sub>IL,EN</sub>	EN Low-level input voltage						0.5	V
V <sub>IH,EN</sub>	EN High-level input voltage				1.3			
I <sub>ENH</sub>	I/O leakage, EN	Leakage current, $V_{\text{EN}} = 1.8\text{ V}$				24	40	$\mu\text{A}$
<b>VBAT INPUT RESISTANCE</b>								
R <sub>VBAT</sub>	VBAT resistance	EN = HI				550		k $\Omega$
		EN = LOW				50		M $\Omega$

## 6.6 Timing Requirements

The device, TPS59632Q1, requires the ENABLE signal on Pin 8 to go from low to high only after the V5A (5-V supply), the VDD (3.3-V supply) and the VBAT rails have gone high.

## 6.7 Switching Characteristics

Over recommended temperature range,  $4.5\text{ V} \leq V_{V5A} \leq 5.5\text{ V}$ ,  $3.0\text{ V} \leq V_{VDD} \leq 3.6\text{ V}$ ,  $V_{GFB} = \text{GND}$ ,  $V_{VFB} = V_{\text{CORE}}$  (unless otherwise noted).

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	
<b>TIMERS: START-UP, PWM ON-TIME AND I/O TIMING</b>						
t <sub>START-CB</sub>	Cold boot time	$V_{\text{BOOT}} > 0\text{ V}$ , EN = high, time from UVLO to VOUT ramp, $C_{\text{REF}} = 0.33\ \mu\text{F}$			1.2	ms
t <sub>STBY-E</sub>	STBY exit time	Time from EN assertion until PGOOD goes high. $V_{\text{VID}} = 1.28\text{ V}$ , $R_{\text{SLEW}} = 39\text{ k}\Omega$			250	$\mu\text{s}$
t <sub>PGDDGLTO</sub>	PGOOD deglitch time	Time from VFB out of 250 mV VDAC boundary to PGOOD low.			1	$\mu\text{s}$
t <sub>PGDDGLTU</sub>	PGOOD deglitch time	Time from VFB out of -300 mV VDAC boundary to PGOOD low.			31	

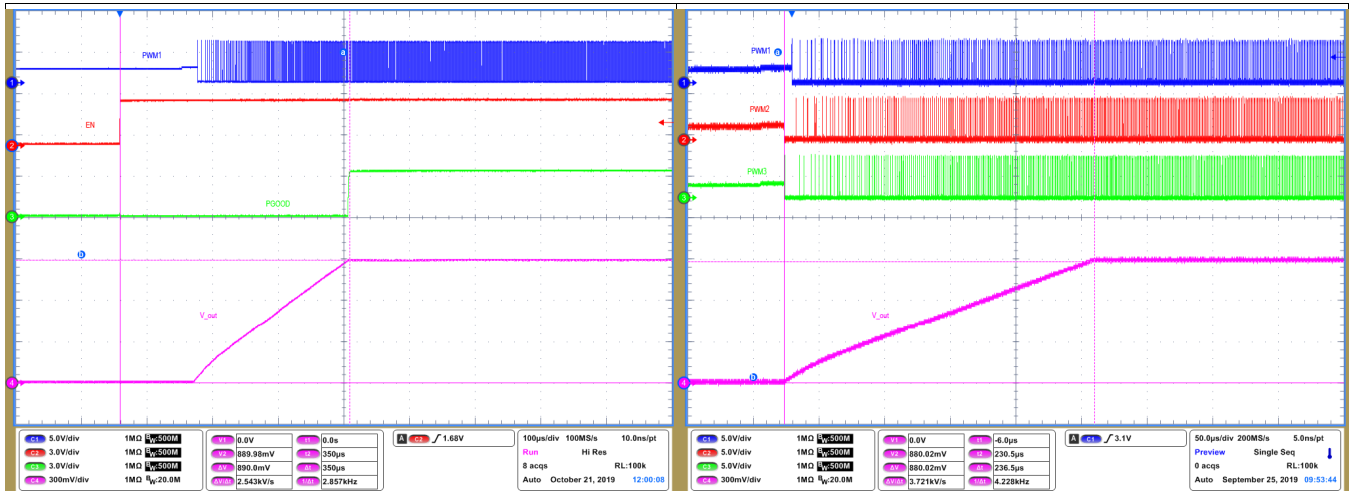
## Switching Characteristics (continued)

Over recommended temperature range,  $4.5\text{ V} \leq V_{V5A} \leq 5.5\text{ V}$ ,  $3.0\text{ V} \leq V_{VDD} \leq 3.6\text{ V}$ ,  $V_{GFB} = \text{GND}$ ,  $V_{VFB} = V_{\text{CORE}}$  (unless otherwise noted).

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	
$t_{\text{ON}}$	PWM ON-time		$R_F = 24\text{ k}\Omega$ , $V_{\text{BAT}} = 12\text{ V}$ , $V_{\text{VFB}} = 1\text{ V}$ (400 kHz)	230	ns	
			$R_F = 39\text{ k}\Omega$ , $V_{\text{BAT}} = 12\text{ V}$ , $V_{\text{VFB}} = 1\text{ V}$ (600 kHz)	164		
			$R_F = 75\text{ k}\Omega$ , $V_{\text{BAT}} = 12\text{ V}$ , $V_{\text{VFB}} = 1\text{ V}$ (800 kHz)	140		
			$R_F = 150\text{ k}\Omega$ , $V_{\text{BAT}} = 12\text{ V}$ , $V_{\text{VFB}} = 1\text{ V}$ (1 MHz)	122		
$t_{\text{OFF\_MIN}}$	Controller minimum OFF time	Fixed value	20		ns	
$t_{\text{ON\_MIN}}$	Controller minimum ON time	$R_{\text{CF}} = 150\text{ k}\Omega$ , $V_{\text{BAT}} = 20\text{ V}$ , $V_{\text{VFB}} = 0\text{ V}$	20			
$t_{\text{VCCVID}}$	VID change to VFB change <sup>(1)</sup>	ACK of VID change command to start of voltage ramp		1	$\mu\text{s}$	
$t_{\text{PG2}}$	PGOOD low after enable goes low	Low-state time after EN goes low.	225	250	275	$\mu\text{s}$
<b>PWM OUTPUTS: I/O VOLTAGE AND CURRENT</b>						
$t_{\text{P-S\_H-L}}$	PWMx H-L transition time	10 to 90%, both edges		7	20	ns
$t_{\text{P-S\_TRI}}$	PWMx 3-state transition	10 or 90% to 3-state level, both edges		5	20	

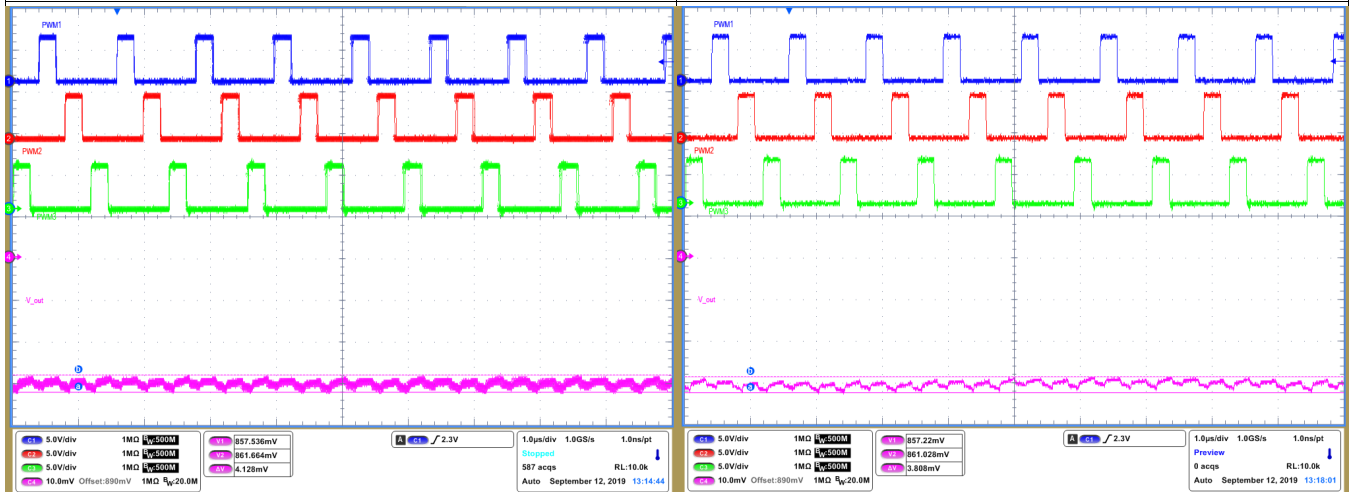
(1) Specified by design. Not production tested.

### 6.8 Typical Characteristics



**Figure 1. 3-phase start up behavior showing EN input and PGOOD output. Input Voltage = 5V, Load current = 10A.**

**Figure 2. 3-phase start up behavior showing switching at startup. Input Voltage = 5V, Load current = 10A.**



**Figure 3. 3-phase switching ripple at Input Voltage = 5 V, Load current = 50A, Switching Frequency = 800kHz. Persistence mode.**

**Figure 4. 3-phase switching ripple at Input Voltage = 5 V, Load current = 50A, Switching Frequency = 800kHz. Single mode.**

Typical Characteristics (continued)

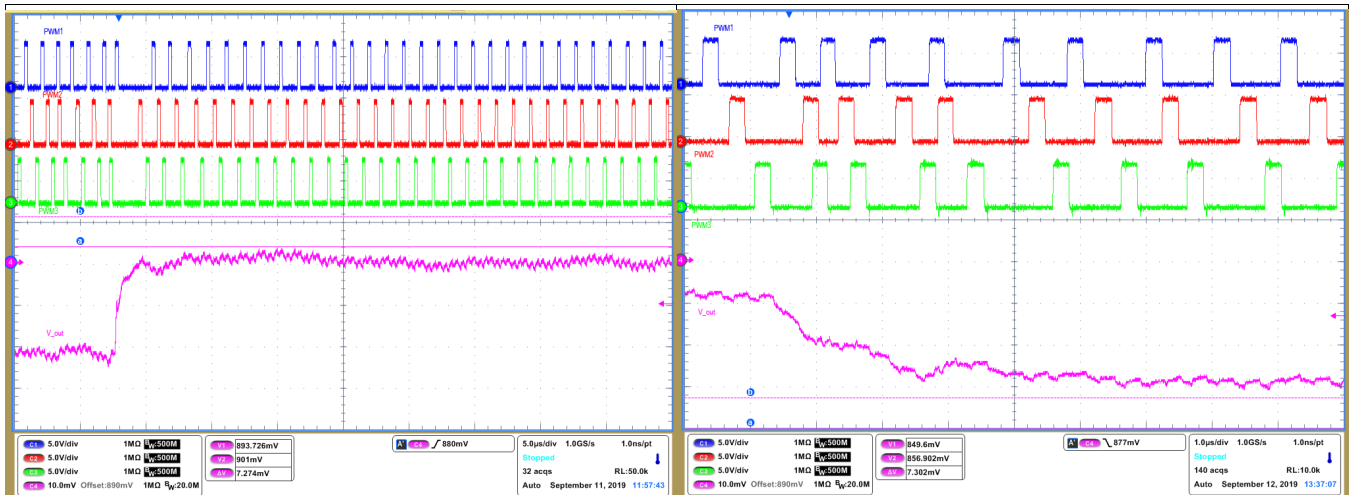


Figure 5. Load transient with a droop of 0.6mΩ load-line slope. Load transient = 36A to 0A. Single mode.

Figure 6. Load transient with a droop of 0.6mΩ load-line slope. Load transient = 14A to 50A. Single mode.

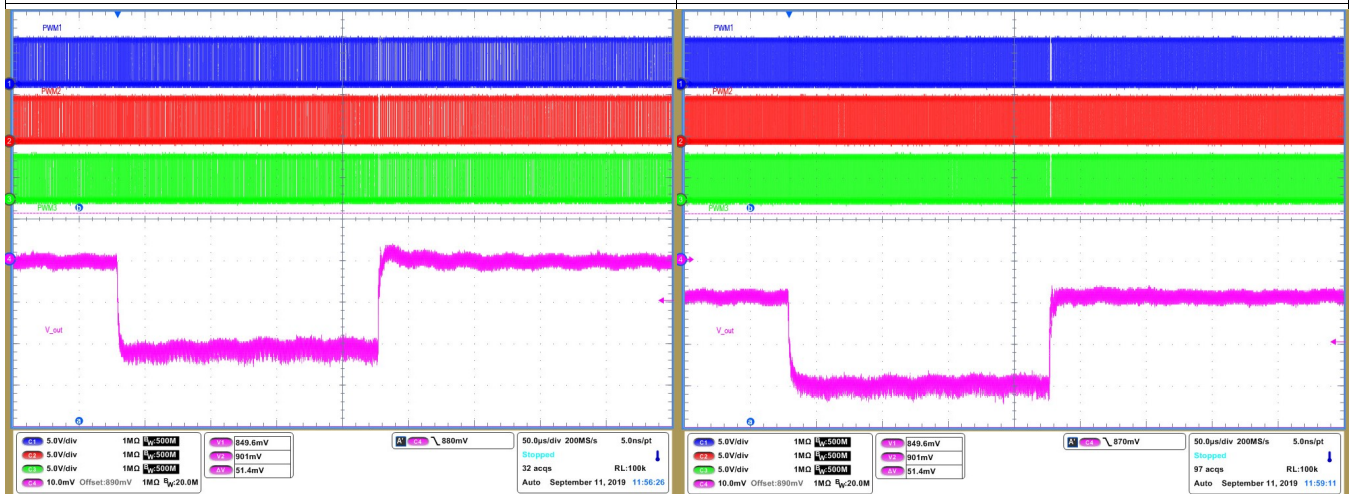


Figure 7. Load transient with a droop of 0.6mΩ load-line slope. Load transient = 0A to 36A. Persistence mode

Figure 8. Load transient with a droop of 0.6mΩ load-line slope. Load transient = 14A to 50A. Persistence mode

## 7 Detailed Description

### 7.1 Overview

The TPS59632-Q1 device is a DCAP+ mode adaptive on-time controller. The DAC outputs a reference in accordance with the 8-bit VID code, as defined in [Table 3](#). This DAC sets the output voltage.

In adaptive on-time converters, the controller varies the on-time as a function of input and output voltage to maintain a nearly constant frequency during steady-state conditions. With conventional voltage-mode constant on-time converters, each cycle begins when the output voltage crosses to a fixed reference level. However, in the TPS59632-Q1 device, the cycle begins when the current feedback reaches an error voltage level, which corresponds to the amplified difference between the DAC voltage and the feedback output voltage. In the case of 2-phase or 3-phase operation, the device sums the current feedback from all the phases at the output of the internal current-sense amplifiers.

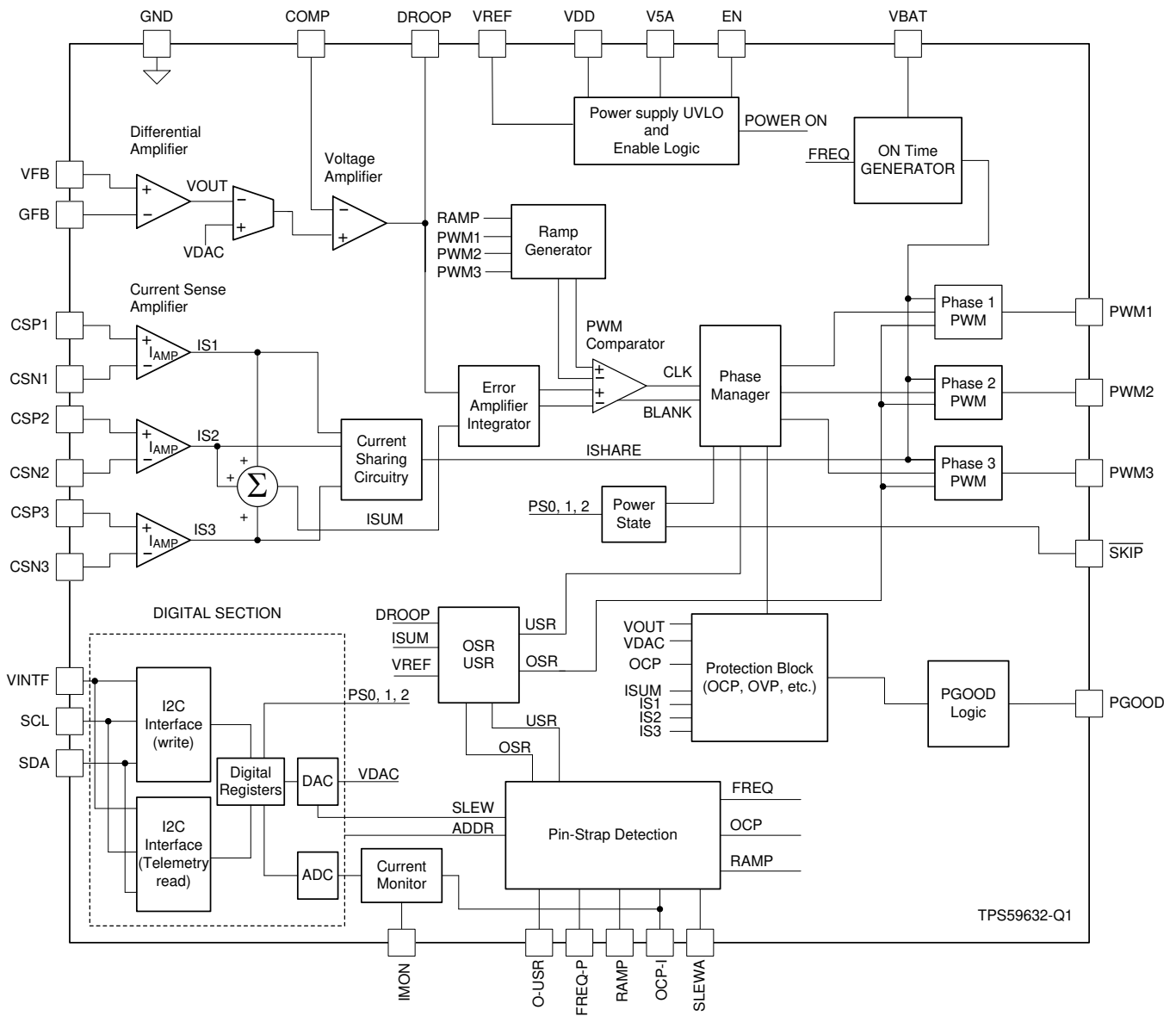
This approach has two advantages:

- The amplifier DC gain sets an accurate linear load-line slope, which is required for CPU core applications.
- The device filters the error voltage input to the PWM comparator to improve the noise performance.

In addition, the difference between the DAC-to-output voltage and the current feedback goes through an integrator to give an approximately linear load-line slope even at light loads where the inductor current is in discontinuous conduction mode (DCM).

During a steady-state condition, the phases of the TPS59632-Q1 device switch 180° phase-displacement for 2-phase mode and 120° phase-displacement for 3-phase mode. The phase displacement is maintained both by the architecture and current ripple. The architecture does not allow the high-side gate drive outputs of more than one phase to be ON in any condition except transients. The current ripple forces the pulses to be spaced equally. The controller forces current-sharing adjusting the ON time of each phase. Current balancing requires no user intervention, compensation, or extra components.

## 7.2 Functional Block Diagram

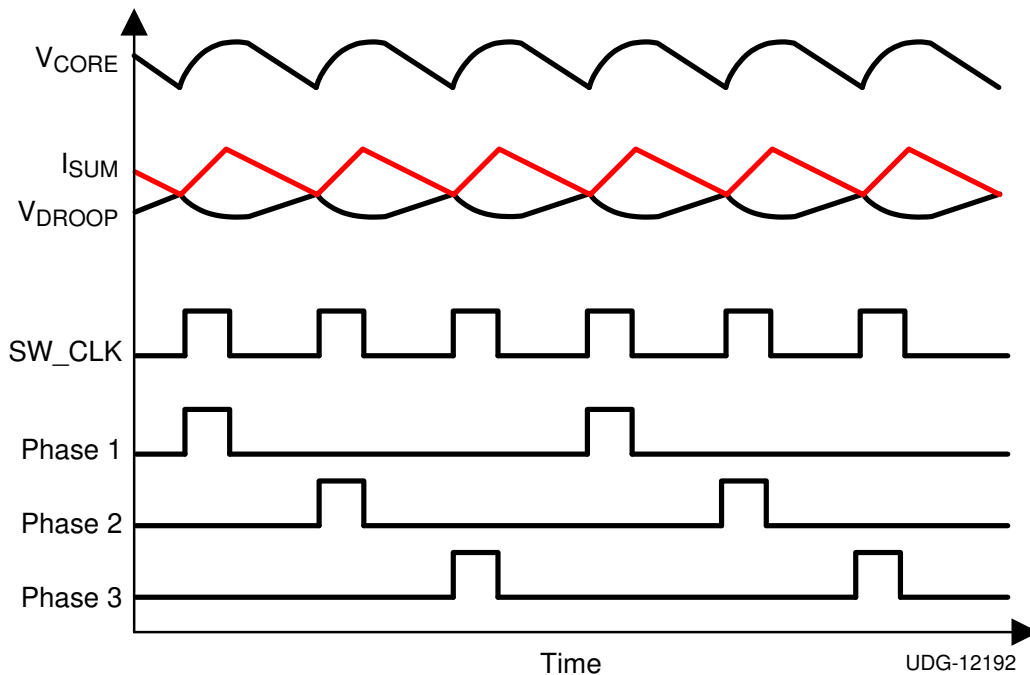


## 7.3 Feature Description

### 7.3.1 PWM Operation

The functional block diagram and [Figure 9](#) shows how the converter operates in CCM.

## Feature Description (continued)



**Figure 9. D-Cap+ Mode Basic Waveforms**

Starting with the condition that the high-side FETs are off and the low-side FETs are on, the summed current feedback ( $I_{SUM}$ ) is higher than the error amplifier output ( $V_{DROOP}$ ).  $I_{SUM}$  falls until it hits  $V_{DROOP}$ , which contains a component of the output ripple voltage. The PWM comparator senses where the two waveforms cross and triggers the on-time generator, which generates the internal SW\_CLK signal. Each SW\_CLK signal corresponds to one switching ON pulse for one phase.

During single-phase operation, every SW\_CLK signal generates a switching pulse on the same phase. Also,  $I_{SUM}$  voltage corresponds to a single-phase inductor current only.

During multi-phase operation, the controller distributes the SW\_CLK signal to each of the phases in a cycle. Using the summed inductor current and cyclically distributing the ON pulses to each phase automatically gives the required interleaving of  $360 / n$ , where  $n$  is the number of phases.

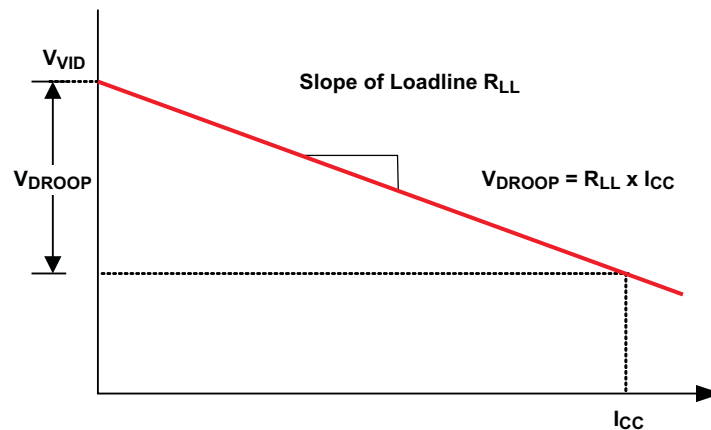
### 7.3.2 Current Sensing

The TPS59632-Q1 provides independent channels of current feedback for every phase, to increase the system accuracy and reduce the dependence of circuit performance on layout compared to an externally summed architecture. The design can use *inductor DCR sensing* to yield the best efficiency or *resistor current sensing* to yield the most accuracy across wide temperature ranges. As inductor DCR sensing is not suitable for automotive applications due to wide variation in current sensing across temperature, resistor sensing is recommended. This sense resistor must be connected in series with the inductor and requires Kelvin sensing terminals for improved current sense accuracy.

The pins CSP1, CSN1, CSP2, CSN2, CSP3, and CSN3 are the inductor current sensing pins for the each of the three phases of the converter.

### 7.3.3 Load-line (Droop)

The TPS59632-Q1 features programmable droop enabling significant reduction of output capacitors. [Figure 10](#) shows the output voltage droop with increasing load current.

**Feature Description (continued)**


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**Figure 10. Load-Line Slope**

$$V_{\text{DROOP}} = R_{\text{LL}} \times I_{\text{CC}} = \frac{R_{\text{CS(eff)}} \times A_{\text{CS}} \times I_{\text{CC}}}{A_{\text{DROOP}}}$$

where

- $R_{\text{CS(eff)}}$  is the effective current sense resistance, when using either a sense resistor or inductor DCR
- $A_{\text{CS}}$  is the gain of the current sense amplifier
- $I_{\text{CC}}$  is the load current
- $A_{\text{DROOP}}$  is the DROOP gain (see [Equation 2](#))

(1)

$$A_{\text{DROOP}} = 1 + \left( \frac{R_{\text{DROOP}}}{R_{\text{COMP}}} \right)$$

where

- resistor,  $R_{\text{DROOP}}$  is connected between the DROOP pin and the COMP pin
- resistor  $R_{\text{COMP}}$  is connected between the COMP pin and the VREF pin

(2)

This load-line aids in the transient performance as discussed in the following section.

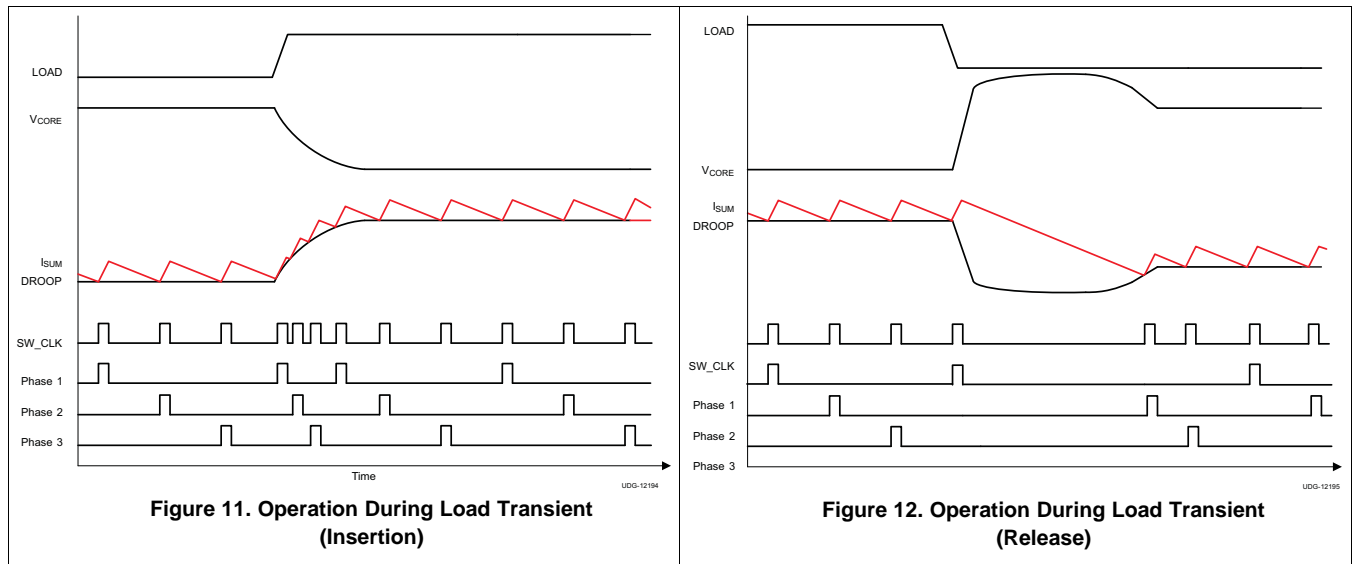
**7.3.4 Load Transients**

When the load increases suddenly, the output voltage immediately drops. This voltage drop is reflected as a rising voltage on the DROOP pin. This rising voltage forces the PWM to pulse sooner and more frequently, which causes the inductor current to rapidly increase. As the inductor current reaches the new load current, a steady-state operating condition is reached and the PWM switching resumes the steady-state frequency. Similarly, when the load releases suddenly, the output voltage rises. This rise is reflected as a falling voltage on the DROOP pin. This rising voltage forces a delay in the PWM pulses until the inductor current reaches the new load current, when the switching resumes and steady-state switching continues.

For simplicity, neither [Figure 11](#) or [Figure 12](#) show the ripple on the output  $V_{\text{CORE}}$  nor the DROOP waveform.



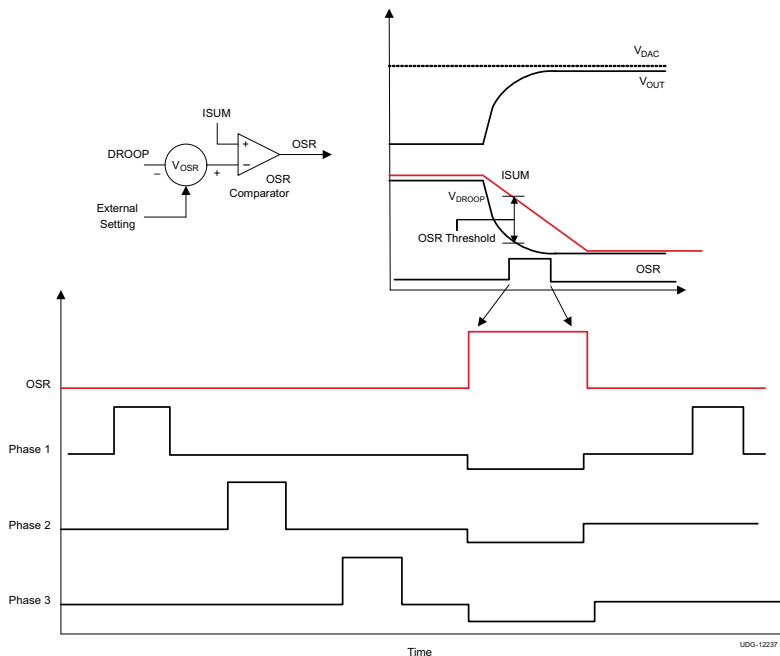
Feature Description (continued)



7.3.5 Overshoot Reduction (OSR)

The problem of overshoot in synchronous buck converters results from the output inductor having a small voltage ( $V_{OUT}$ ) with which to respond to a transient load release.

With overshoot reduction feature enabled, when the output voltage increases beyond a value that corresponds to a voltage difference between the ISUM voltage and the DROOP pin voltage exceeding the specified OSR voltage (as specified in the [Electrical Characteristics](#) table), at the instant that the low-side drivers are turned OFF. When the low-side driver is turned OFF, the energy in the inductor is partially dissipated by the body diodes. As the overshoot reduces, the low-side drivers are turned ON again. [Figure 13](#) shows overshoot reduction by turning off the low-side MOSFET during load transient release.



## Feature Description (continued)

### 7.3.6 Undershoot Reduction (USR)

When the transient load increase becomes quite large, it is difficult to meet the energy demanded by the load especially at lower input voltages. Then it is necessary to quickly increase the energy in the inductors during the transient load increase. This increase is achieved by enabling pulse overlapping. In order to maintain the interleaving of the multi-phase configuration while maintaining pulse-overlapping during load-insertion, the undershoot reduction (USR) mode is entered only when necessary. This device enters this mode is when the difference between DROOP voltage and ISUM voltage exceeds the USR voltage level specified in the [Electrical Characteristics](#) table.

Figure 14 shows the undershoot reduction operation. This feature allows for the use of reduced output capacitance while continuing to meet the specification. The device achieves undershoot reduction by overlapping of pulses on all the phases.

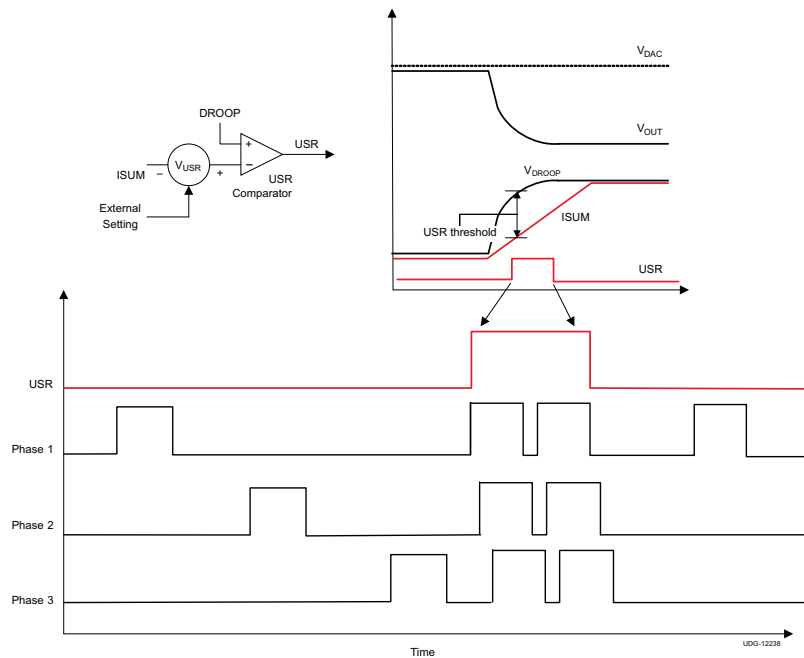


Figure 14. Undershoot Reduction

When the transient condition is completed, the interleaving of the phases is resumed.

It should be noted that single-phase mode there is no USR mode of operation.

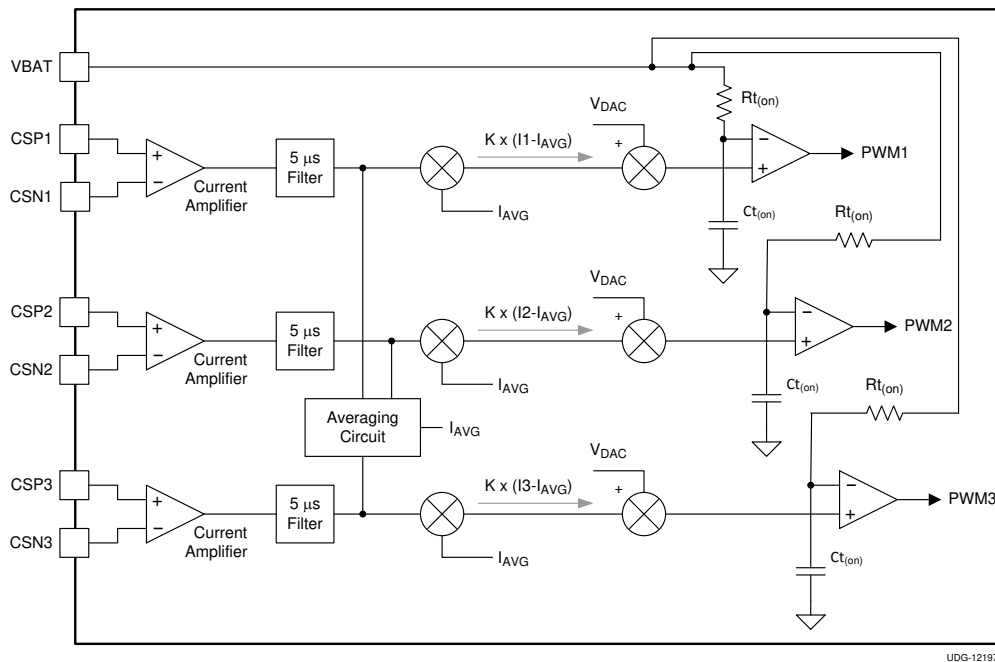
### 7.3.7 Autobalance Current Sharing

The basic mechanism for current sharing is to sense the average phase current, then adjust the pulse width of each phase to equalize the current in each phase.

The PWM comparator (not shown) starts a pulse when the feedback voltage equals the reference voltage. The VBAT voltage charges  $C_{t(on)}$  through the resistor  $R_{t(on)}$ . The pulse is terminated when the voltage at capacitor  $C_{t(on)}$  matches the on-time ( $t_{ON}$ ) reference, usually the DAC voltage ( $V_{DAC}$ ).

A current sharing circuit is shown in [Figure 15](#). For example, assume that the 5- $\mu$ s-averaged value of  $I_1 = I_2 = I_3$ . In this case, the PWM modulator terminates at  $V_{DAC}$ , and the typical pulse width is delivered to the system. If instead,  $I_1 > I_{AVG}$ , then an offset is subtracted from  $V_{DAC}$ , and the pulse width for phase one is shortened, reducing the current in phase one to compensate. If  $I_1 < I_{AVG}$ , then a longer pulse is produced, again compensating on a pulse-by-pulse basis.

## Feature Description (continued)



**Figure 15. Autobalance Current Sharing**

### 7.3.8 PWM And $\overline{\text{SKIP}}$ Signals

The PWM and  $\overline{\text{SKIP}}$  signals are outputs of the controller and serve as input to the MOSFET gate driver or DrMOS-type devices. Both signals are 5-V logic signals. The PWM signals are logic high to allow the high-side drive of the external gate driver to turn ON. The PWM signal must be low for the low-side drive of the external gate driver to turn ON. To drive both the signals are OFF, the PWM is set to tri-state. The  $\overline{\text{SKIP}}$  signal is active low to set all the phases in Continuous Conduction Mode (CCM) of operation. If  $\overline{\text{SKIP}}$  signal is high then the external gate driver turns OFF the Low-side drive to operate in the boundary of CCM and Discontinuous Conduction Mode (DCM).

### 7.3.9 Bias Power (V5A, VDD, And VINTF) UVLO

The TPS59632-Q1 device continuously monitors the voltage on the V5A, VDD, and VINTF pin to ensure a value high enough to bias the device properly and provide sufficient gate drive potential to maintain high efficiency. The converter starts with approximately 4.4 V and has a nominal 200 mV of hysteresis. Once the V5A, VDD, or VINTF goes below the  $V_{UVLOL}$ , the corresponding voltage must fall below  $V_{POR}$  (1.5 V) to reset the device.

The input ( $V_{BAT}$ ) does not include a UVLO function, so the circuit runs with power inputs as low as approximately  $3 \times V_{OUT}$ .

### 7.3.10 Start-Up Sequence

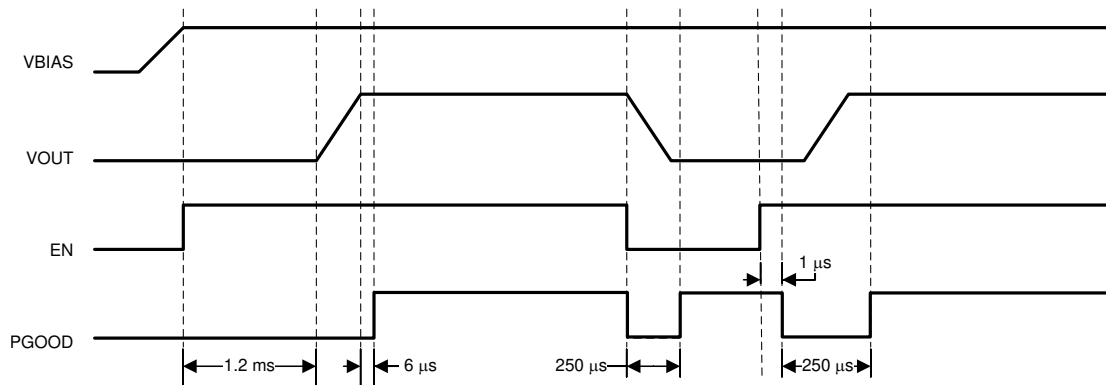
The TPS59632-Q1 device initializes when all of the supplies rise above the UVLO thresholds. This function is also known as a *cold boot*. The device then reads all of the various settings (such as frequency and overcurrent protection). This process takes less than 1.2 ms. During this time, the VSR initializes to the BOOT voltage. The output voltage rises to the VSR level when the EN pin (enable) goes high. Once the BOOT sequence completes, PGOOD is HIGH and the I<sup>2</sup>C interface can be used to change the voltage select register (VSR). The current VSR value is held when EN goes low and returns to a high state. This function is also known as a *warm boot*.

## Feature Description (continued)

### 7.3.11 Power Good Operation

PGOOD is an open-drain output pin that is designed to be pulled-up with an external resistor to a voltage 3.6 V or less. Normal PGOOD operation (exclusive of activation of any faults) is shown in Figure 16. On initial power-up PGOOD happens within 6  $\mu$ s of the DAC reaching its target value. When EN is brought low, PGOOD is also brought low for 250  $\mu$ s, then is allowed to float. The TPS59632-Q1 device pulls down the PGOOD signal when the EN signal subsequently goes high and returns high again within 6  $\mu$ s of the end of the DAC ramp. The delay period between EN going high and PGOOD going low in this case is less than 1  $\mu$ s. Figure 16 shows the power good operation at initial start-up and with falling and rising EN.

For applications where it is undesirable to have PGOOD high when EN is low, an alternate method of pulling up the open-drain PGOOD signal is possible. In this method, the PGOOD is pulled up to EN logic signal. This ensures that the PGOOD is low when EN goes low.



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**Figure 16. Power Good Operation**

### 7.3.12 Analog Current Monitor, IMON, And Corresponding Digital Output Current

The TPS59632-Q1 device includes a current monitor function. The current monitor supplies an analog voltage, proportional to the load current, on the IMON pin.

The current monitor function is related to the OCP selection resistors. The  $R_{OCP}$  is the resistor between the OCP-I pin and GND and  $R_{CIMON}$  is the resistor between the IMON pin to the OCP-I pin that sets the current monitor gain. Equation 3 shows the calculation for the current monitor gain.

$$V_{IMON} = 10 \times 1 + \frac{(R_{IMON})}{(R_{OCP})} \times \sum V_{CSn} \xrightarrow{\text{yields}} V$$

where

- $\sum V_{CS}$  is the sum of the DC voltages at the inputs to the current sense amplifiers (3)

To ensure stable current monitor operation, and at the same time, provide a fast dynamic response, connect a 4.7-nF to 10-nF capacitor from the IMON pin to GND. Connecting higher capacitance will reduce the response time accordingly.

The analog current monitor should be set so that at the maximum processor current ( $I_{CC(max)}$ ) the IMON voltage should be 1.7 V. This setting corresponds to a digital output current value of 'FF' in the telemetry register 03H through I2C. For any other IMON voltage output in the range of 0 to 1.7 V, the digital output varies linearly.

### 7.3.13 Fault Behavior

TPS59632-Q1 device has a complete suite of fault detection and protection functions, including input under-voltage lockout on all power inputs, over voltage and over current limiting, and output under voltage detection. The protection limits are given in the tables above. The converter suspends switching when the limits are exceeded and PGOOD goes low. In this state, the fault register 14h can be read. To exit fault protection mode, the bias power (V5A, VDD and VINTF) must be cycled as described in [Bias Power \(V5A, VDD, And VINTF\) UVLO](#).

## Feature Description (continued)

### 7.3.14 Output Under Voltage Protection (UVP)

Output undervoltage protection works in conjunction with the current protection described in the [Over Current Protection \(OCP\)](#) section. If  $V_{OUT}$  drops below the low PGOOD voltage threshold, then the PWM is tri-stated. The device stays off until the V5A, VDD or VINTF power is cycled and EN goes high.

### 7.3.15 Output Over Voltage Protection (OVP)

An OVP condition is detected when the output voltage is greater than the PGDH voltage, and greater than VDAC.  $V_{OUT} > +V_{PGDH}$  greater than VDAC. In this case, the controller device sets PGOOD inactive, and keeps all the PWM signals low so as to keep the low-side driver ON at the converter. The converter remains in this state until the controller device is reset by cycling V5A, VDD or VINTF. This is the first level of OVP. This first level of OVP is inactive during VID transitions. There is a second OVP level fixed at  $V_{OVPH}$  which is always active. If the fixed OVP condition is detected, the PGOOD is forced inactive and the PWM signals are kept low and the operation is similar to the first level of OVP detection

### 7.3.16 Over Current Protection (OCP)

The TPS59632-Q1 device uses a inductor valley current limiting scheme, so the ripple current must be considered. The DC current value at OCP is the OCP limit value plus half of the ripple current. Current limiting occurs on a phase-by-phase and pulse-by-pulse basis. Generally, the current is sensed using the sense resistor in series with the inductor for automotive applications giving a voltage between the CSPx and CSNx pins. If this sensed voltage is above the OCP limit, the converter delays the next ON pulse until that voltage difference drops below the OCP limit.

In OCP mode, the voltage drops until the UVP limit is reached. When UVP limit is reached the operation follows as described in the [Output Under Voltage Protection \(UVP\)](#).

### 7.3.17 Over Current Warning

I<sup>2</sup>C programming enables this function. The TPS59632-Q1 device pulls down the voltage on the PGOOD pin whenever the valley current reaches 70% of the OCP value (or higher). PGOOD resumes normal function when the value falls below 65% of the OCP value.

### 7.3.18 Input Voltage Limits

The minimum input voltage is limited by the number of input phases, the switching frequency and the output voltage. The minimum input voltage increases with required maximum output voltage and switching frequency. See [Table 1](#) for limits in 3-phase operating mode and [Table 2](#) for limits in 2-phase operating mode . In 1-phase mode, the operation is limited by controller's capability to 2.5 V for all output voltages and switching frequency.

**Table 1. Minimum Input Voltage ( $V_{IN, MIN}$ ) Limits Versus Switching Frequency ( $F_{SW}$ ) and Maximum Output Voltage ( $V_{OUT, MAX}$ ) in 3-phase operation**

$V_{OUT, MAX}$ (V)	$F_{SW}$ (kHz)	$V_{IN, MIN}$ (V)
0.8	800	3.6
	1000	4.0
0.9	800	4.0
	1000	4.5
1.0	800	4.5
	1000	5.0

**Table 2. Minimum Input Voltage ( $V_{IN, MIN}$ ) Limits Versus Switching Frequency ( $F_{SW}$ ) and Maximum Output Voltage ( $V_{OUT, MAX}$ ) in 2-phase operation**

$V_{OUT, MAX}$ (V)	$F_{SW}$ (kHz)	$V_{IN, MIN}$ (V)
0.8	1000	2.5
0.9	1000	2.5
1.0	1000	2.8

### 7.3.19 VID Table

The [Table 3](#) shows the VID table for all the programmable DAC voltage levels.

**Table 3. TPS59632-Q1 VID Table**

VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	VOLTAGE
0	0	1	1	0	0	1	19	0.5000
0	0	1	1	0	1	0	1A	0.5100
0	0	1	1	0	1	1	1B	0.5200
0	0	1	1	1	0	0	1C	0.5300
0	0	1	1	1	0	1	1D	0.5400
0	0	1	1	1	1	0	1E	0.5500
0	0	1	1	1	1	1	1F	0.5600
0	1	0	0	0	0	0	20	0.5700
0	1	0	0	0	0	1	21	0.5800
0	1	0	0	0	1	0	22	0.5900
0	1	0	0	0	1	1	23	0.6000
0	1	0	0	1	0	0	24	0.6100
0	1	0	0	1	0	1	25	0.6200
0	1	0	0	1	1	0	26	0.6300
0	1	0	0	1	1	1	27	0.6400
0	1	0	1	0	0	0	28	0.6500
0	1	0	1	0	0	1	29	0.6600
0	1	0	1	0	1	0	2A	0.6700
0	1	0	1	0	1	1	2B	0.6800
0	1	0	1	1	0	0	2C	0.6900
0	1	0	1	1	0	1	2D	0.7000
0	1	0	1	1	1	0	2E	0.7100
0	1	0	1	1	1	1	2F	0.7200
0	1	1	0	0	0	0	30	0.7300
0	1	1	0	0	0	1	31	0.7400
0	1	1	0	0	1	0	32	0.7500
0	1	1	0	0	1	1	33	0.7600
0	1	1	0	1	0	0	34	0.7700
0	1	1	0	1	0	1	35	0.7800
0	1	1	0	1	1	0	36	0.7900
0	1	1	0	1	1	1	37	0.8000
0	1	1	1	0	0	0	38	0.8100
0	1	1	1	0	0	1	39	0.8200
0	1	1	1	0	1	0	3A	0.8300
0	1	1	1	0	1	1	3B	0.8400
0	1	1	1	1	0	0	3C	0.8500
0	1	1	1	1	0	1	3D	0.8600
0	1	1	1	1	1	0	3E	0.8700
0	1	1	1	1	1	1	3F	0.8800
1	0	0	0	0	0	0	40	0.8900
1	0	0	0	0	0	1	41	0.9000
1	0	0	0	0	1	0	42	0.9100
1	0	0	0	0	1	1	43	0.9200
1	0	0	0	1	0	0	44	0.9300
1	0	0	0	1	0	1	45	0.9400
1	0	0	0	1	1	0	46	0.9500
1	0	0	0	1	1	1	47	0.9600

**Table 3. TPS59632-Q1 VID Table (continued)**

VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	VOLTAGE
1	0	0	1	0	0	0	48	0.9700
1	0	0	1	0	0	1	49	0.9800
1	0	0	1	0	1	0	4A	0.9900
1	0	0	1	0	1	1	4B	1.0000
1	0	0	1	1	0	0	4C	1.0100
1	0	0	1	1	0	1	4D	1.0200
1	0	0	1	1	1	0	4E	1.0300
1	0	0	1	1	1	1	4F	1.0400
1	0	1	0	0	0	0	50	1.0500
1	0	1	0	0	0	1	51	1.0600
1	0	1	0	0	1	0	52	1.0700
1	0	1	0	0	1	1	53	1.0800
1	0	1	0	1	0	0	54	1.0900
1	0	1	0	1	0	1	55	1.1000
1	0	1	0	1	1	0	56	1.1100
1	0	1	0	1	1	1	57	1.1200
1	0	1	1	0	0	0	58	1.1300
1	0	1	1	0	0	1	59	1.1400
1	0	1	1	0	1	0	5A	1.1500
1	0	1	1	0	1	1	5B	1.1600
1	0	1	1	1	0	0	5C	1.1700
1	0	1	1	1	0	1	5D	1.1800
1	0	1	1	1	1	0	5E	1.1900
1	0	1	1	1	1	1	5F	1.2000
1	1	0	0	0	0	0	60	1.2100
1	1	0	0	0	0	1	61	1.2200
1	1	0	0	0	1	0	62	1.2300
1	1	0	0	0	1	1	63	1.2400
1	1	0	0	1	0	0	64	1.2500
1	1	0	0	1	0	1	65	1.2600
1	1	0	0	1	1	0	66	1.2700
1	1	0	0	1	1	1	67	1.2800
1	1	0	1	0	0	0	68	1.2900
1	1	0	1	0	0	1	69	1.3000
1	1	0	1	0	1	0	6A	1.3100
1	1	0	1	0	1	1	6B	1.3200
1	1	0	1	1	0	0	6C	1.3300
1	1	0	1	1	0	1	6D	1.3400
1	1	0	1	1	1	0	6E	1.3500
1	1	0	1	1	1	1	6F	1.3600
1	1	1	0	0	0	0	70	1.3700
1	1	1	0	0	0	1	71	1.3800
1	1	1	0	0	1	0	72	1.3900
1	1	1	0	0	1	1	73	1.4000
1	1	1	0	1	0	0	74	1.4100
1	1	1	0	1	0	1	75	1.4200
1	1	1	0	1	1	0	76	1.4300



**Table 3. TPS59632-Q1 VID Table (continued)**

VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	VOLTAGE
1	1	1	0	1	1	1	77	1.4400
1	1	1	1	0	0	0	78	1.4500
1	1	1	1	0	0	1	79	1.4600
1	1	1	1	0	1	0	7A	1.4700
1	1	1	1	0	1	1	7B	1.4800
1	1	1	1	1	0	0	7C	1.4900
1	1	1	1	1	0	1	7D	1.5000
1	1	1	1	1	1	0	7E	1.5100
1	1	1	1	1	1	1	7F	1.5200

## 7.4 User Selections

After the V5A, VDD, and VINTF voltages are applied to the controller and all these voltage levels are above their respective UVLO levels, the following information is latched and cannot be changed during operation. The defines the values of the selections.

- **Operating Frequency.** The resistor from FREQ-P pin to GND sets the switching frequency. See the [Detailed Design Procedure](#) for the resistor settings corresponding to each frequency selection. Note that the operating frequency is a quasi-fixed frequency in the sense that the ON time is fixed based on the input voltage (at the VBAT pin) and output voltage (set by VID). The OFF time varies based on various factors such as load and power-stage components.
- **Overcurrent Protection (OCP) Level.** The resistor from OCP-I to GND sets the OCP level of the CPU channel. See the [Detailed Design Procedure](#) for the resistor settings corresponding to each OCP level.
- **IMON Gain.** The resistors from IMON to OCP-I and OCP-I to GND set the DC load current monitor (IMON) gain.
- **Slew Rate.** The SetVID fast slew rate is set by the resistor from SLEWA pin to GND. See the [Detailed Design Procedure](#) for the resistor settings corresponding to each slew rate setting.
- **Base Address.** The voltage on SLEWA pin sets the device base address.
- **Ramp Selection.** The resistor from RAMP to GND sets the ramp compensation level. See the [Detailed Design Procedure](#) for the resistor settings corresponding to each ramp level.
- **Overshoot Reduction (OSR) Level.** The resistor from O-USR to GND sets the OSR level. [Detailed Design Procedure](#) provides all the possible selections for OSR.
- **Undershoot Reduction Level (USR)** The voltage on O-USR pin sets the USR level. [Detailed Design Procedure](#) provides all the possible selections for USR.
- **Active Phases.** Normally, the controller is configured to operate in 3-phase mode. To enable 2-phase mode, tie the CSP3 pin to a 3.3-V supply and the CSN3 pin to GND. To enable 1-phase mode, tie the CSP2 and CSP3 pins to a 3.3-V supply and tie the CSN2 and CSN3 pins to GND.

## 7.5 I<sup>2</sup>C Interface Operation

The TPS59632-Q1 device includes a slave I<sup>2</sup>C interface accessed via the SCL (serial clock) and SDA (serial data) pins. The interface sets the base VID value, receives IMON telemetry, and controls functions described in this section. It operates with EN = low, with the bias supplies in regulation. It is compliant with I<sup>2</sup>C specification UM10204, Revision 3.0; characteristics are detailed as following:

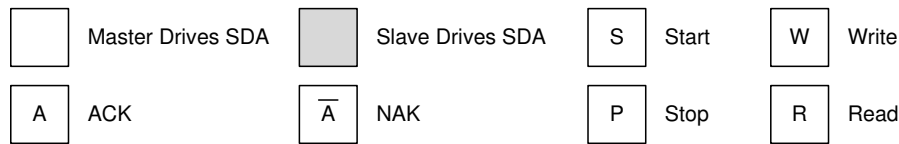
- Addressing
  - 7-bit addressing; address range is 100 0xxx (binary)
  - Last three bits are determined by the voltage on SLEWA pin at start-up
- Byte read and byte write protocols only (see the following figures)
- Frequency
  - 100 kHz
  - 400 kHz
  - 1 MHz
  - 3.4 MHz

## I<sup>2</sup>C Interface Operation (continued)

- Logic inputs are 1.8-V logic levels (3.3-V tolerant)

The TPS59632-Q1 device can be configured for eight different device addresses by setting a voltage on the SLEWA pin. Configure a resistor divider on SLEWA from VREF to GND. Once the slew rate resistor is selected, the resistor from the VREF pin to the SLEWA pin can be chosen based on the required device address. For a device address of 40h, the VREF to SLEWA resistor can be left open.

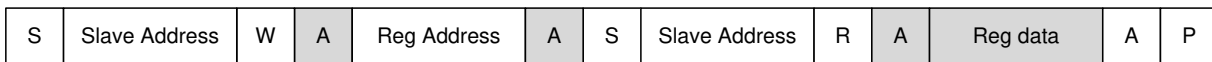
### 7.5.1 Key For Protocol Examples



UDG-13045

### 7.5.2 Protocol Examples

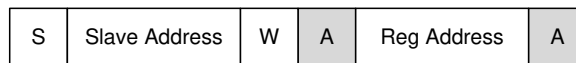
The good byte read transaction the controller ACKs and the master terminates with a NAK/stop



UDG-13046

**Figure 17. Good Byte Read Transaction**

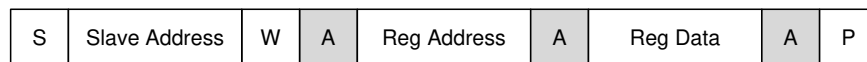
The controller NAKs a read with an invalid register address.



UDG-13047

**Figure 18. NAK Invalid Register Address**

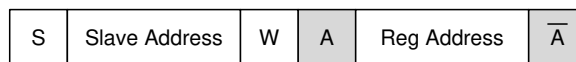
A good byte write is illustrated in [Figure 19](#).



UDG-13048

**Figure 19. Good Byte Write**

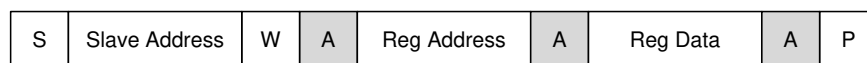
The controller NAKs a write with an invalid register address.



UDG-13049

**Figure 20. Invalid NAK Register Address**

The controller will NAK a write for the condition of invalid data.



UDG-13050

**Figure 21. Invalid NAK Register Data**

## 7.6 I<sup>2</sup>C Register Maps

The I<sup>2</sup>C interface shall support 400 kHz, 1 MHz, and 3.4-MHz clock frequencies. The I<sup>2</sup>C interface shall be accessible even when EN is low. The following registers are accessible via I<sup>2</sup>C.

### 7.6.1 Voltage Select Register (VSR) (Address = 00h)

- Type: read and write
- Power-up value: BOOT[6:0]
- EN rising (after power-up): prior programmed value
- See [Table 3](#) for exact values
- A command to set VSR < 19h (minimum VID) generates an NAK and the VBR remains at the prior value

b7	b6	b5	b4	b3	b2	b1	b0
—	VID6	—	—	—	—	—	VID0

### 7.6.2 IMON Register (Address = 03h)

- Type: read only
- Power-up value: 00h
- EN rising (after power-up): 00h

b7	b6	b5	b4	b3	b2	b1	b0
MSB	—	—	—	—	—	—	LSB

### 7.6.3 VMAX Register (Address = 04h)

- Type: read or write (see the following bit definitions)
- Power-up value: 7Fh
- EN rising (after power-up): last written value

b7	b6	b5	b4	b3	b2	b1	b0
Lock	MSB	—	—	—	—	—	LSB

Bit definitions:

**Table 4.**

BIT	NAME	DEFINITION
0 - 6	VMAX	Maximum VID setting
7	Lock	Access protection of the VMAX register 0: No protection, R/W access to bits 0-6 1: Access is read only; reset after UVLO event.

### 7.6.4 Power State Register (Address = 06h)

- Type: read and write
- Power-up value: 00h
- EN rising (after power-up): 00h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	MSB	LSB

Bit definitions:

VALUE	DEFINITION
b1 = 0, b0 = 0	Multi-phase CCM
b1 = 0, b0 = 1	Single-phase CCM

VALUE	DEFINITION
b1 = 1, b0 = 0	Single-phase DCM

### 7.6.5 Slew Register (Address = 07h)

- Type: read and write (see below)
- Power-up value: defined by SLEWA pin at power-up
- EN rising (after power-up): last written value
- Write only a single 1 for the minimum SLEW rate desired for voltage changes. The start-up slew rate is half of the normal voltage change slew rate.

b7	b6	b5	b4	b3	b2	b1	b0
48 mV/μs	42 mV/μs	36 mV/μs	30 mV/μs	24 mV/μs	18 mV/μs	12 mV/μs	6 mV/μs

### 7.6.6 Lot Code Registers (Address = 10-13h)

- Type: 8 bits, read only
- Power-up value: programmed at factory

### 7.6.7 Fault Register (Address = 14h)

- Type: 8 bits; read only
- Power-up value: 00h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	Device thermal shutdown	OVP	UVP	OCP

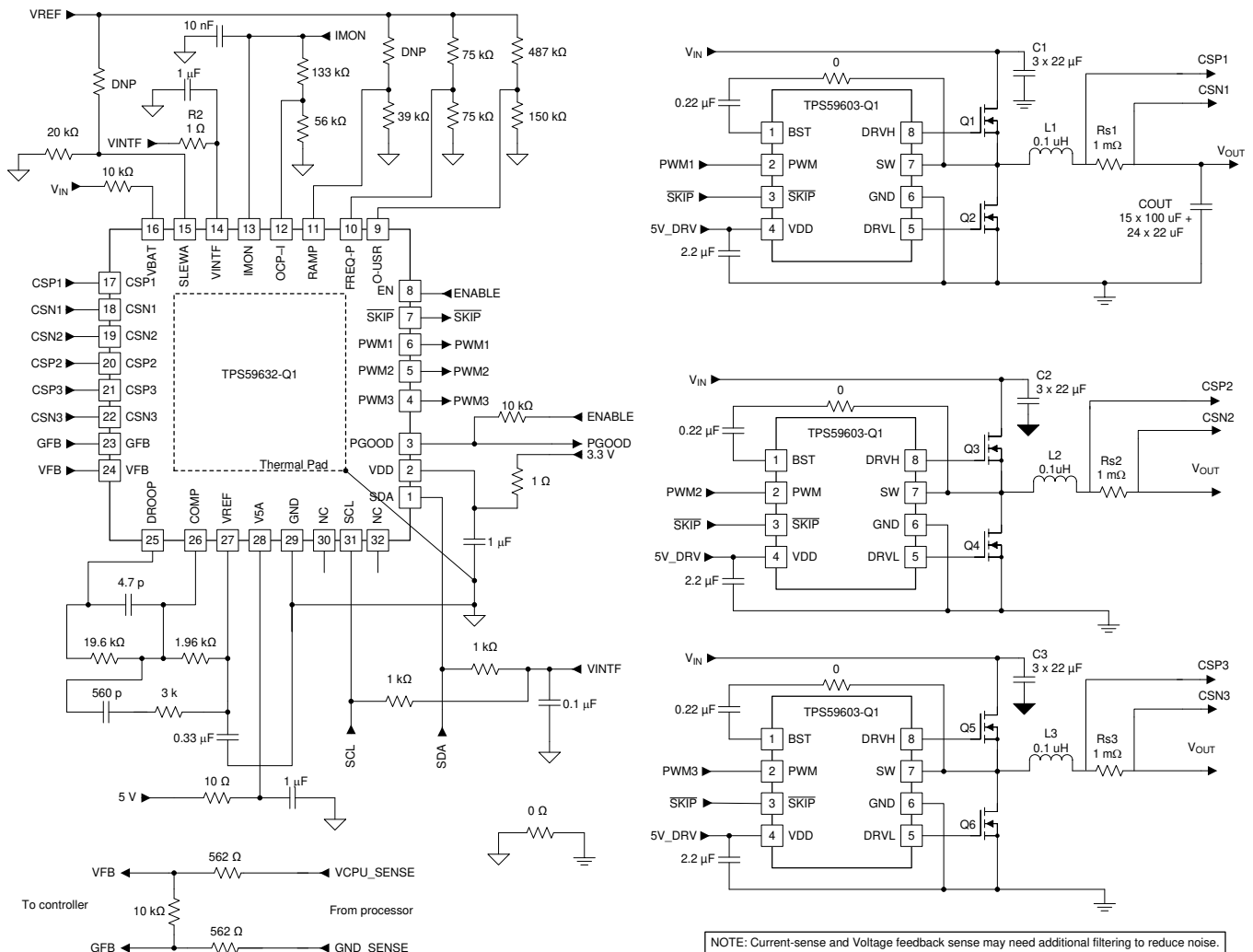
## 8 Applications and Implementation

### 8.1 Application Information

The TPS59632Q1 device has a very simple design procedure. A Microsoft Excel®-based component value calculation tool is available. Please contact your local TI representative to get a copy of the spreadsheet.

### 8.2 Typical Application

#### 8.2.1 3-Phase D-CAP+™, Step-Down Application



NOTE: Current-sense and Voltage feedback sense may need additional filtering to reduce noise.

Figure 22. 3-Phase D-CAP+™, Step-Down Application with Power Stages

#### 8.2.1.1 Design Requirements

Design example specifications:

- Number of phases,  $N_{ph}$ : 3
- Conversion Input voltage,  $V_{IN}$  range: 5 V +/- 10%
- Converter Output Voltage  $V_{OUT} = 0.875 \pm 3\% V$  (including DC and AC)
- Load Current,  $I_{CC(max)} = 50 A$
- Voltage Rise time (at start-up) > 100µs
- Load Transient step = 36A
- Load Transient Slew rate = 36A/µs

## Typical Application (continued)

- Effective Switching Frequency > 2.0 MHz

### 8.2.1.2 Detailed Design Procedure

#### 8.2.1.2.1 Step 1: Select Switching Frequency

The switching frequency is selected by a resistor ( $R_F$ ) between the FREQ\_P pin and GND. The frequency is approximate and expected to vary based on load and input voltage.

**Table 5. TPS59632-Q1 Device Frequency Selection Table**

SELECTION RESISTOR ( $R_F$ ) VALUE (k $\Omega$ )	OPERATING FREQUENCY ( $f_{sw}$ ) (kHz)
20	300
24	400
30	500
39	600
56	700
75	800
100	900
150	1000

For this design, choose a switching frequency of 800 kHz so that the effective switching frequency in 3-phase operation = 2.4 MHz. So,  $R_F = 75\text{ k}\Omega$ .

#### NOTE

The voltage on the FREQ-P pin MUST be set higher than 0.7V for proper operation of the device, TPS59632Q1. This can easily be achieved by connecting a resistor of the same value as  $R_F$  from FREQ-P to VREF (1.7 V).

As per the note above, in this design, a resistor of value 75 k $\Omega$  is connected from FREQ-P to VREF.

#### 8.2.1.2.2 Step 2: Set The Slew Rate

A resistor to GND ( $R_{SLEWA}$ ) on SLEWA pin sets the slew rate. For a minimum start-up time of 100  $\mu\text{s}$ , the maximum allowed slew rate would be  $V_{OUT}/100\ \mu\text{s}$ . This would mean a maximum start-up slew rate of 8.8 mV/ $\mu\text{s}$ . Hence, from Table 6 the maximum start-up slew rate setting of 5mV/ $\mu\text{s}$  is chosen. It should be noted that the slew rate corresponding to start-up rate is half of the slew rate during voltage changes due to VID changes as specified in the EC table. The table below provides the minimum and maximum start-up slew rate for each resistor selection. The resistor selection chosen for this design is  $R_{SLEWA} = 20\text{ k}\Omega$ .

**Table 6. Slew Rate Versus Selection Resistor**

SELECTION RESISTOR $R_{SLEWA}$ (k $\Omega$ )	MINIMUM START-UP SLEW RATE (mV/ $\mu\text{s}$ )	MAXIMUM START-UP SLEW RATE (mV/ $\mu\text{s}$ )
20	3	5
24	6	10
30	9	15
39	12	20

#### 8.2.1.2.3 Step 3: Set The I<sup>2</sup>C Address

The voltage on the SLEWA pin also sets the I<sup>2</sup>C address for the device. For an I<sup>2</sup>C address of 40, the SLEWA pin should only have a resistor,  $R_{SLEW}$  to GND and the SLEW pin to VREF pin should be left open. For other I<sup>2</sup>C addresses, a resistor must be connected between the SLEWA pin and the VREF pin (1.7 V). This resistor can be calculated to set the corresponding voltage for the required address listed in Table 7.

**Table 7. I<sup>2</sup>C Address Selection**

SLEWA VOLTAGE	I <sup>2</sup> C ADDRESS
$V_{SLEWA} \leq 0.30 \text{ V}$	0
$0.35 \text{ V} \leq V_{SLEWA} \leq 0.45 \text{ V}$	1
$0.55 \text{ V} \leq V_{SLEWA} \leq 0.65 \text{ V}$	2
$0.75 \text{ V} \leq V_{SLEWA} \leq 0.85 \text{ V}$	3
$0.95 \text{ V} \leq V_{SLEWA} \leq 1.05 \text{ V}$	4
$1.15 \text{ V} \leq V_{SLEWA} \leq 1.25 \text{ V}$	5
$1.35 \text{ V} \leq V_{SLEWA} \leq 1.45 \text{ V}$	6
$1.55 \text{ V} \leq V_{SLEWA} \leq 1.65 \text{ V}$	7

#### 8.2.1.2.4 Step 4: Determine Inductor Value And Choose Inductor

Applications with smaller inductor values have better transient performance but also have higher voltage ripple and lower efficiency. Applications with higher inductor values have the opposite characteristics. Choice of inductance is a trade off between transient, ripple, size, efficiency, cost and availability.

For this design, we chose an inductance value of 0.1  $\mu\text{H}$ . The chosen inductor should have the following characteristics:

- As flat as an inductance versus current curve as possible.
- Either high saturation or soft saturation. A saturation current of at least the per phase maximum current of  $I_{CC(max)} / N_{ph} + I_{ripple}/2$
- Low DCR for high efficiency.

#### 8.2.1.2.5 Step 5: Current Sensing Resistance

The TPS59632 device supports both resistor sensing and inductor DCR sensing. However, inductor DCR sensing is not suitable for automotive applications due to wide variation in current sensing across temperature. The sense resistance,  $R_S$  must be chosen large enough to give sufficient current signal to the controller and small enough to keep the power dissipation low. Choosing max power dissipation to about 0.5W per phase, we get  $R_S = 1 \text{ m}\Omega$ .

### 8.2.1.2.6 Step 6: Select Over Current Protection (OCP) Setting

The OCP level is chosen such that it is 30% above the maximum load current,  $I_{CC(max)}$ . In the equation, here  $R_{CS}$  is the current sense resistor. [Equation 4](#).  $I_{VALLEY}$  is the load current less half the ripple.

$$I_{VALLEY} \times R_{CS(eff)} = V_{CS(ocp)} \quad (4)$$

Set the OCP threshold level just greater than the calculated  $I_{VALLEY}$  for the required OCP level. [Equation 4](#). In this design, the minimum required OCP is 65A. Therefore, an OCP selection resistor of 56k is chosen to meet the requirement.

[Table 8](#) shows the minimum OCP level for all the selection resistors.

**Table 8. OCP Selection<sup>(1)</sup>**

SELECTION RESISTOR $R_{OCP}$ (k $\Omega$ )	Minimum $V_{CS(ocp)}$ (mV)
20	3
24	7
30	11
39	15
56	21
75	28
100	36
150	45

(1) If a corresponding match is not found, then select the next higher setting.

### 8.2.1.2.7 Step 7: Current Monitor (IMON) Setting

Set the analog current monitor so that at  $I_{CC(max)}$  the IMON pin voltage is 1.7 V. This corresponds to a digital  $I_{OUT}$  value of 'FF' in I<sup>2</sup>C register 03H. The voltage on the IMON pin is shown in [Equation 5](#).

$$1.7 = 10 \times \left( 1 + \frac{R_{IMON}}{R_{OCP}} \right) \times R_{CS(eff)} \times I_{CC(max)} \quad (5)$$

where,  $I_{CC(max)}$  is 50 A;  $R_{CS(eff)}$  is 1.0 m $\Omega$  and  $R_{OCP}$  is 56 k $\Omega$

Solving,  $R_{IMON} = 133$  k $\Omega$ .  $R_{IMON}$  is connected from IMON pin to OCP-I pin.



### 8.2.1.2.8 Step 8: Set the Load-Line Slope

Setting a load line slope is effective in significantly reducing the output capacitors. Therefore, although the design requirement does not call for a load-line, we use the output voltage tolerance specification to determine an appropriate load-line. Figure 23 shows how we first determine the load-line window.

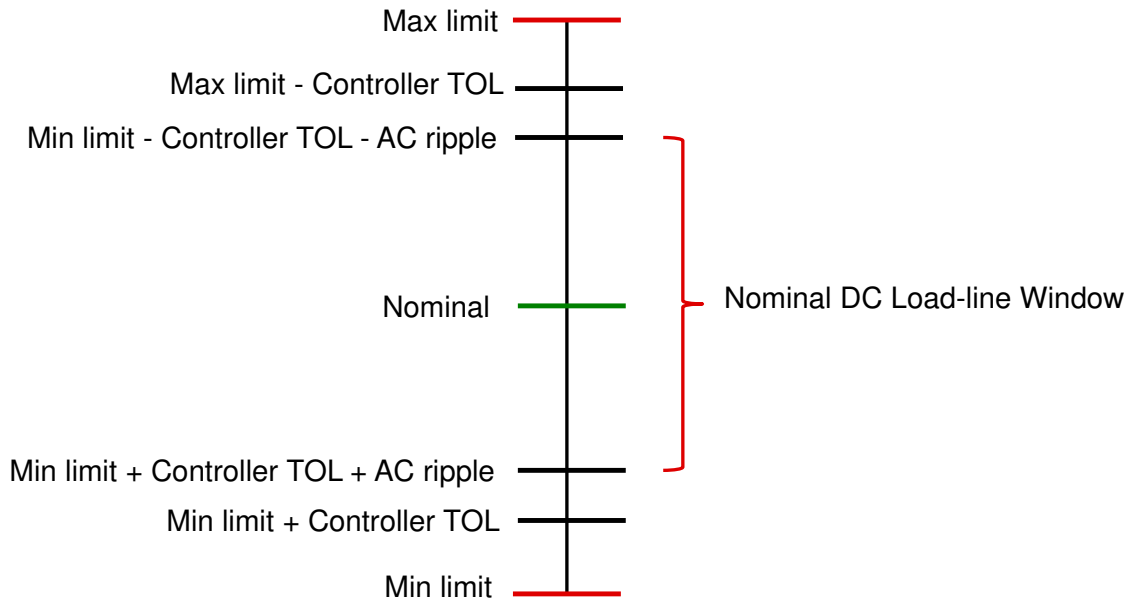


Figure 23. Determination of Nominal DC Load-line window

This nominal DC load-line window is now used to set the load-line slope across the range of load current from 0 to  $I_{cc,max}$  as shown in Figure 24.

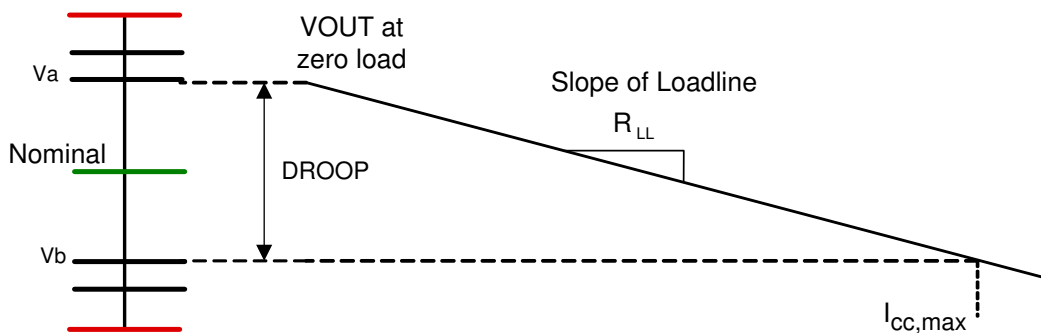


Figure 24. Determination of the Slope of the Load-line

The load-line slope  $R_{LL}$  is first determined as shown in Figure 24 using the equation in Equation 6. In the device, TPS59632-Q1, the load-line is determined by the current sense resistance,  $R_{CS}$ , the current sense amplifier gain,  $A_{CS}$ , and the gain of the droop amplifier ( $A_{DROOP}$ ) as shown in Equation 7.

$$R_{LL} = \frac{Va - Vb}{I_{cc\ max}} \quad (6)$$

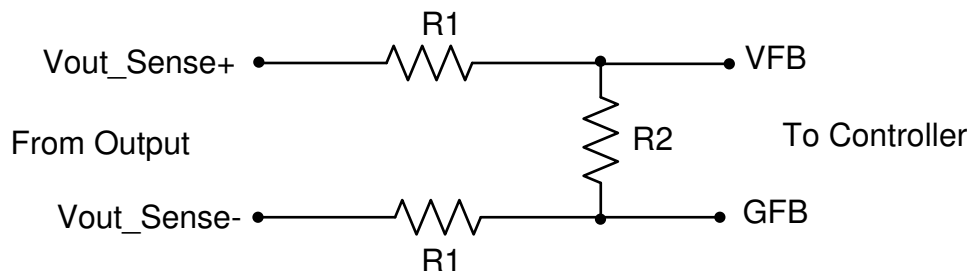
$$R_{LL} = \frac{R_{CS,eff} \times A_{CS}}{A_{DROOP}} \quad (7)$$

The gain of the droop amplifier, ( $A_{\text{DROOP}}$ ) can therefore be determined by Equation 7. This gain is set by the external resistors  $R_{\text{DROOP}}$  (between the DROOP pin and the COMP pin) and resistor  $R_{\text{COMP}}$  (between the COMP pin and the VREF pin) as shown in Equation 8. We fix the value of  $R_{\text{DROOP}}$  to 19.6 k $\Omega$ , and thereby  $R_{\text{COMP}}$  is calculated to 1.87 k $\Omega$ .

$$A_{\text{DROOP}} = \left( 1 + \left( \frac{R_{\text{DROOP}}}{R_{\text{COMP}}} \right) \right) \quad (8)$$

### 8.2.1.2.9 Step 9: Voltage Feedback Resistor Calculation

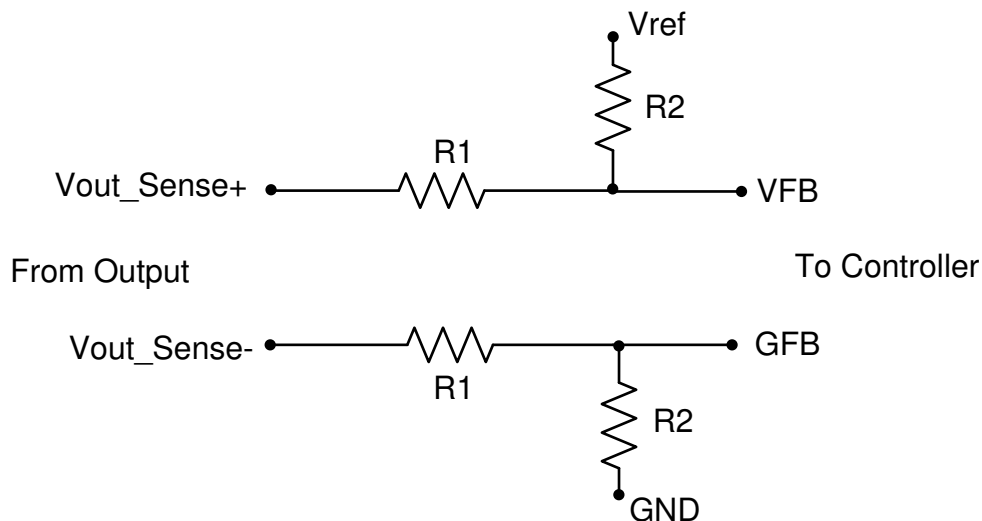
In the device TPS59632-Q1, the internal DAC voltage is set to 0.80 V. To adjust the output voltage above or below this voltage we need to use feedback resistor divider setting. Since we are sensing the voltage using differential remote sense we adopt the circuit shown in Figure 25 to increase the voltage above 0.80 V and the and circuit shown in Figure 26 to decrease the voltage below 0.80 V.



**Figure 25. Feedback resistor divider circuit to increase the output voltage above internal DAC voltage**

In this design, we need to calculate the feedback resistor values,  $R_1$  and  $R_2$ , to increase the voltage above the DAC, the equation shown in Equation 9 is used. Here,  $V_{\text{DAC}} = 0.80 \text{ V}$ , and  $V_a$  from load-line setting is determined as 0.890 V.  $R_2$  is set to 10 k $\Omega$  and  $R_1$  is calculated to 562.

$$V_a \frac{R_2}{R_2 + 2R_1} = V_{\text{DAC}} \quad (9)$$



**Figure 26. Feedback resistor divider circuit to decrease the output voltage above internal DAC voltage**

To calculate the feedback resistor values,  $R_1$  and  $R_2$ , to decrease the voltage below the DAC, the equation shown in Equation 10 is used. Here,  $V_{\text{DAC}} = 0.80 \text{ V}$ , and  $V_a$  from load-line setting for the specific application.  $V_{\text{ref}}$  is the TPS59632-Q1 reference voltage at Pin 27 (VREF) which is nominally 1.7 V. Using this, and setting  $R_2$  to 10 k $\Omega$ ,  $R_1$  can be determined.

$$\frac{V_{ref} - V_{DAC}}{R2} = \frac{V_{DAC} - V_a}{R1} \quad (10)$$

#### 8.2.1.2.10 Step 10: Ramp Compensation Selection

The Ramp compensation is selected to minimize the jitter. Higher ramp gives lower jitter but can worsen the transient response. The ramp compensation selection is a trade off between transient response and jitter.

Table 9 shows the available ramp selections.

**Table 9. Ramp Compensation Selection**

SELECTION RESISTOR $R_{RAMP}$ (k $\Omega$ )	RAMP COMPENSATION VOLTAGE (mV)
20	20
30	60
39	100
150	40

#### 8.2.1.2.11 Step 11 Overshoot Reduction (OSR) selection

The OSR level selection is based on the load-transient performance and amount of actual output capacitance to get the best performance with least output capacitance. The suggested method is to begin with OSR OFF and perform the load transient test based on a calculated amount of output capacitance. If the overshoot is higher than specified voltage limits, the OSR can be enabled by lowering the OSR threshold level. If the overshoot is acceptable with OSR OFF, then a reduction in output capacitance can be made and then an appropriate OSR level can be selected to meet the load transient specification. While reducing the output capacitance, other considerations like output ripple, undershoot, stability, and so on needs to be considered simultaneously.

Table 10 shows the available OSR selections.

**Table 10. OSR Selection**

SELECTION RESISTOR $R_{OSR}$ (k $\Omega$ )	OSR THRESHOLD LEVEL (mV)
20	100
24	150
30	200
39	250
56	300
75	400
100	500
150	OFF

#### 8.2.1.2.12 Step 12: Undershoot Reduction (USR) selection

Once the the  $R_{OSR}$  value is fixed, then the USR level can be set by the voltage on the O-USR pin. The resistor  $R_{USR}$  (between the O-USR pin and the VREF pin) sets the voltage.

**Table 11. USR Selection**

LEVEL	$V_{O-USR}$ SELECTION VOLTAGE (V)		$V_{USR}$ UNDERSHOOT REDUCTION LEVEL (mV)
	MIN	MAX	
1		0.25	60
2	0.35	0.45	90
3	0.55	0.65	120
4	0.75	0.85	180

**Table 11. USR Selection (continued)**

LEVEL	V <sub>O-USR</sub> SELECTION VOLTAGE (V)		V <sub>USR</sub> UNDERSHOOT REDUCTION LEVEL (mV)
	MIN	MAX	
5	0.95	1.05	240
6	1.15	1.25	420
7	1.35	1.45	480
8	1.55	V <sub>VREF</sub>	540

The USR level is also selected similar to the OSR setting. First, begin with least undershoot reduction and lower the level until pulse-overlap between two phases happens sufficiently to meet the load insertion transient requirement. The USR level can be approximately estimated by multiplying one-third of the droop voltage for the specified load transient with the A<sub>DRPOOP</sub> determined in [Step 8: Set the Load-Line Slope](#). The actual level needs to be tuned based on measurement. In this design, OSR is set to OFF and USR is set to 90-mV level. Therefore R<sub>OSR</sub> = 150k and R<sub>USR</sub> = 487k.

#### 8.2.1.2.13 Step 13: Loop Compensation

The controller device TPS59632-Q1 does not require any additional loop compensation for stability as the load-line setting droop amplifier gain automatically stabilizes the DCAP+ control loop. However, to further increase the response time to fast load transients, an additional resistor (3 kΩ) in series with a capacitor (560 pF) is placed from COMP to VREF. Frequency response is measured to ensure the stability while meeting the transient requirements. Some key results for this design are given in [Application Performance Plots](#).

8.2.1.3 Application Performance Plots

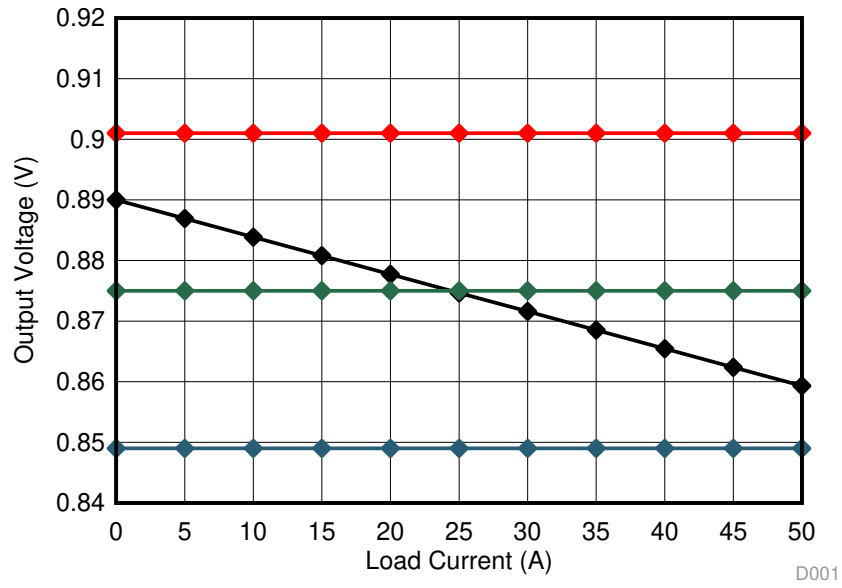


Figure 27. Output Voltage vs Output Current

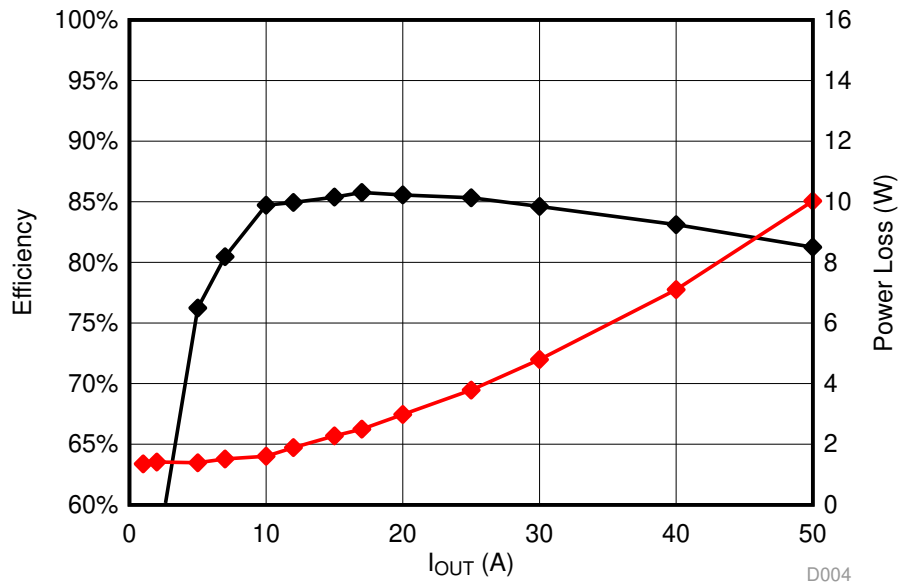


Figure 28. Efficiency and Power Loss Vs. Load Current

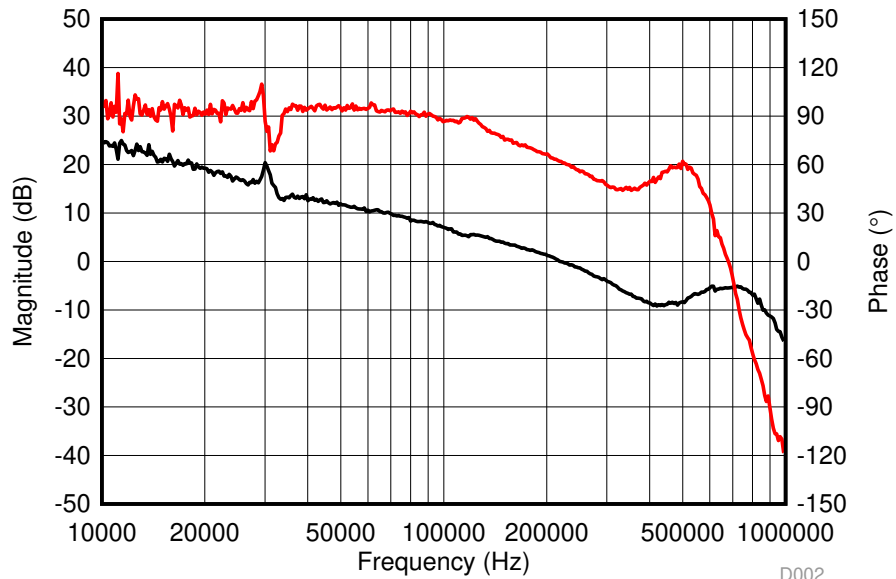


Figure 29. Control-loop Gain-Phase measurement Vs. frequency D002

## 9 Power Supply Recommendations

This device is designed to operate from a supply voltage at the V5A pin (5-V power input for analog circuits) from 4.5 V to 5.5 V and a supply voltage at the VDD pin (3.3-V digital power input) from 3.1 V to 3.5 V, and a supply voltage at VINTF from 1.7 V to 3.5 V. Use only a well-regulated supply. The VBAT input must be connected to the conversion input voltage and must not exceed 28 V. Proper bypassing of the V5A, VDD, and VINTF input supplies is critical for noise performance, as is PCB layout and grounding scheme. See the recommendations in the [Layout](#) section.

## 10 Layout

### 10.1 Layout Guidelines

- Confirm the pinout of the controller on schematic against the pinout of the data sheet.
- Have a component value calculator tool ready to check component values.
- Carefully check the choice of inductor and sense resistor.
- Carefully check the choice of output capacitors.
- Because the voltage and current feedback signals are fully differential, double check their polarity.
  - CSP1 / CSN1
  - CSP2 / CSN2
  - CSP3 / CSN3
  - VOUT\_SENSE to VFB / GND\_SENSE to GFB
- Make sure the pull up on the SDA, SCL lines are correct. Check if there is a bypass capacitor close to the device on the pull up VINTF rail to GND of the device.
- TI strongly recommends that the device GND be separate from the system and Power GND.

#### NOTE

Make sure to separate noisy driver interface lines. This is a critical layout rule.

The driver (TPS59603-Q1) is outside of the device. All gate-drive and switch-node traces must be local to the inductor and MOSFETs.

### 10.2 Layout Example

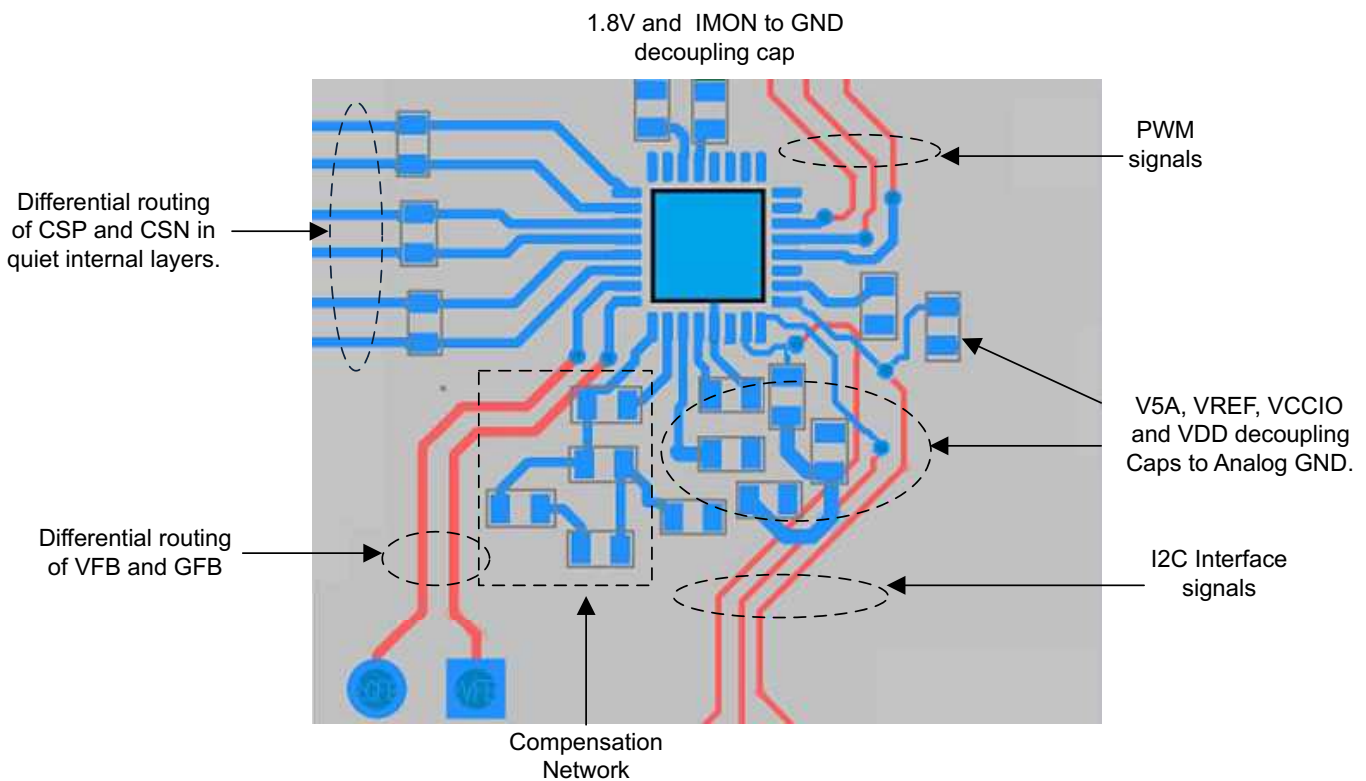


Figure 30. Example Layout

### 10.3 Current Sensing Lines

Given the physical layout of most systems, the current feedback (CSPx and CSNx) may have to pass near the power chain. Clean current feedback is required for good load-line, current sharing, and current limiting performance of the TPS59632-Q1 device, so take the following precautions:

- Ensure all vias in the CSPx and CSNx traces are isolated from all other signals.
- TI recommends dotted signal traces be run in internal planes.
- If possible, change the name of the CSNx trace if possible to prevent automatic ties to the  $V_{CORE}$  plane.
- Run CSPx and CSNx as a differential pair in a quiet layer to the device.
- Isolate the lines from noisy signals by a voltage or ground plane.
- Make a Kelvin connection to the pads of the resistor used for current sensing.
- Place any noise filtering capacitors directly under or near the TPS59632-Q1 device and connect to the CS pins with the shortest trace length possible.

### 10.4 Feedback Voltage Sensing Lines

The voltage feedback coming from the CPU socket must be routed as a differential pair all the way to the VFB and GFB pins of the TPS59632-Q1 device. Care should be taken to avoid routing over switch-node and gate-drive traces.

### 10.5 PWM And $\overline{SKIP}$ Lines

The PWM and  $\overline{SKIP}$  lines should be routed from the TPS59632-Q1 device to the MOSFET gate driver without crossing any switch-node or the gate drive signals.

### 10.6 Power Chain Symmetry

The TPS59632-Q1 device does not require special care in the layout of the power chain components because independent isolated current feedback is provided. Lay out the phases in a symmetrical manner, if possible. The rule is: the current feedback from each phase needs to be clean of noise and have the same effective current-sense resistance.

### 10.7 Component Location

Place components as close to the device in the following order:

1. CS pin noise filtering components
2. COMP pin and DROOP pin compensation components
3. Decoupling capacitors for VREF, VDD, V5A
4. Decoupling cap for VINTF rail, which is pullup voltage for the digital lines. This decoupling should be placed near the device to have good signal integrity.
5. OCP-I resistors, FREQ-P resistors, SLEWA resistors, RAMP resistors, and O-USR resistors



## 10.8 Grounding Recommendations

The TPS59632-Q1 device has an analog ground and a thermal pad. The usual procedure for connecting these is:

- Keep the analog GND of the device and the power GND of the power circuit separate. The device analog GND and the power circuit power GND can be connected at one single quiet point in the layout.
- The thermal pad does not have an electrical connection to device. But, the thermal pad must be connected to pin 29 GND of the device to give good ground shielding. Do not connect this to system GND.
- Tie the thermal pad to a ground island with at least 4 vias. All the analog components can connect to this analog ground island.
- The analog ground can be connected to any quiet spot on the system ground. A quiet spot is defined as a spot where no power supply switching currents are likely to flow. Use a single point connection from analog ground to the system ground.
- Make sure the bottom FET source connection and the input decoupling capacitors have plenty of vias.

## 10.9 Decoupling Recommendations

- Decouple V5A and VDD to GND with a ceramic capacitor (with a value of at least 1  $\mu\text{F}$ ).
- Decouple VINTF to GND with a capacitor (with a value of at least 0.1  $\mu\text{F}$ ) to GND.

## 10.10 Conductor Widths

- Maximize the widths of power, ground, and drive signal connections.
- For conductors in the power path, be sure there is adequate trace width for the amount of current flowing through the traces.
- Make sure there are sufficient vias for connections between layers. Use 1 via minimum per ampere of current.

## 11 デバイスおよびドキュメントのサポート

### 11.1 ドキュメントのサポート

『[TPS59603-Q1 Synchronous Buck FET Driver for High-Frequency CPU Core Power in Automotive Applications](#)』  
データシート (英語)

### 11.2 商標

D-CAP+, AutoBalance, D-CAP+ are trademarks of Texas Instruments.  
Excel is a registered trademark of Microsoft Corporation.  
All other trademarks are the property of their respective owners.

### 11.3 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

### 11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

## 13 Package Option Addendum

### 13.1 Packaging Information

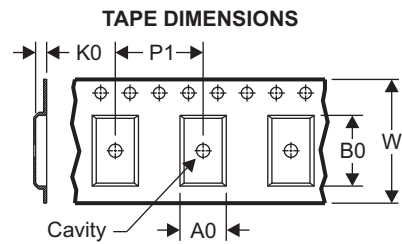
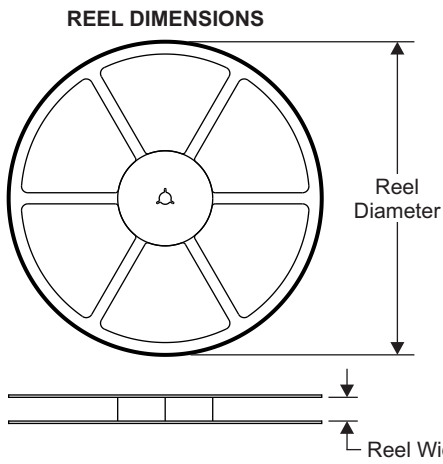
Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>	Op Temp (°C)	Device Marking <sup>(4)(5)</sup>
TPS59632QRHBRQ1	PREVIEW	QFN	RHB	32	3000	GREEN (RoHS and no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	–40 to 125	TPS59632Q
TPS59632QRHBTQ1	PREVIEW	QFN	RHB	32	250	GREEN (RoHS and no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	–40 to 125	TPS59632Q

- (1) The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.  
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.  
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.  
**PRE\_PROD** Unannounced device, not in production, not available for mass market, nor on the web, samples not available.  
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.  
**OBSELETE:** TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.  
**TBD:** The Pb-Free/Green conversion plan has not been defined.  
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.  
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.  
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device
- (5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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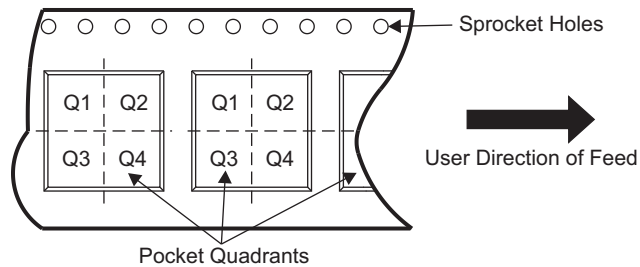
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### 13.2 Tape And Reel Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

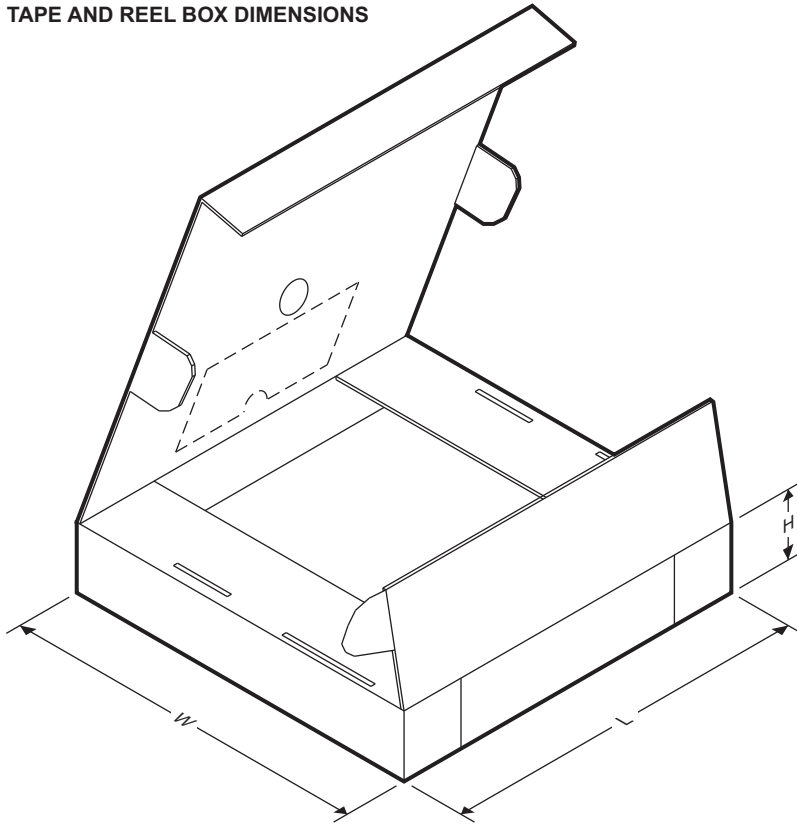
#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS59632QRHBRQ1	QFN	RHB	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS56632QRHBTQ1	QFN	RHB	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

**TPS59632-Q1**

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**TAPE AND REEL BOX DIMENSIONS**


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS59632QRHBRQ1	QFN	RHB	32	3000	367.0	367.0	35.0
TPS59632QRHBTQ1	QFN	RHB	32	250	210.0	185.0	35.0

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS59632QRHBRQ1	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	TPS 59632	<a href="#">Samples</a>
TPS59632QRHBTQ1	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	TPS 59632	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

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**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

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**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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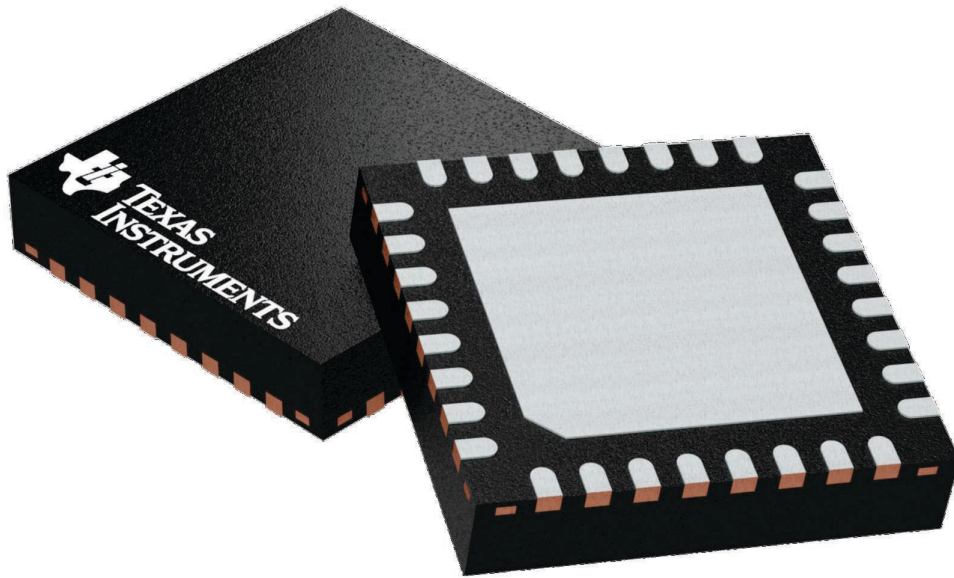
## GENERIC PACKAGE VIEW

**RHB 32**

**VQFN - 1 mm max height**

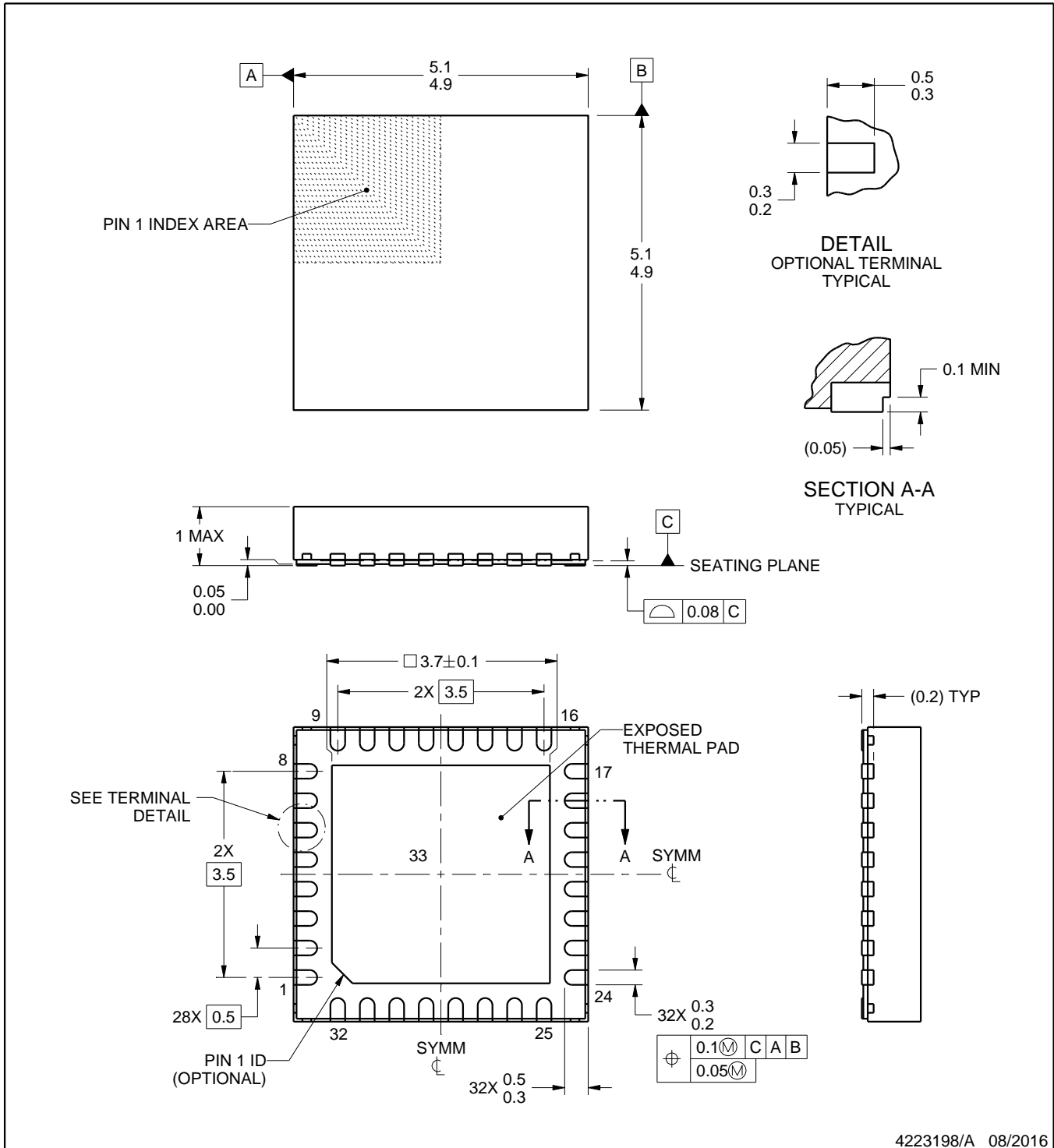
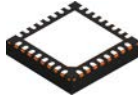
5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224745/A



4223198/A 08/2016

NOTES:

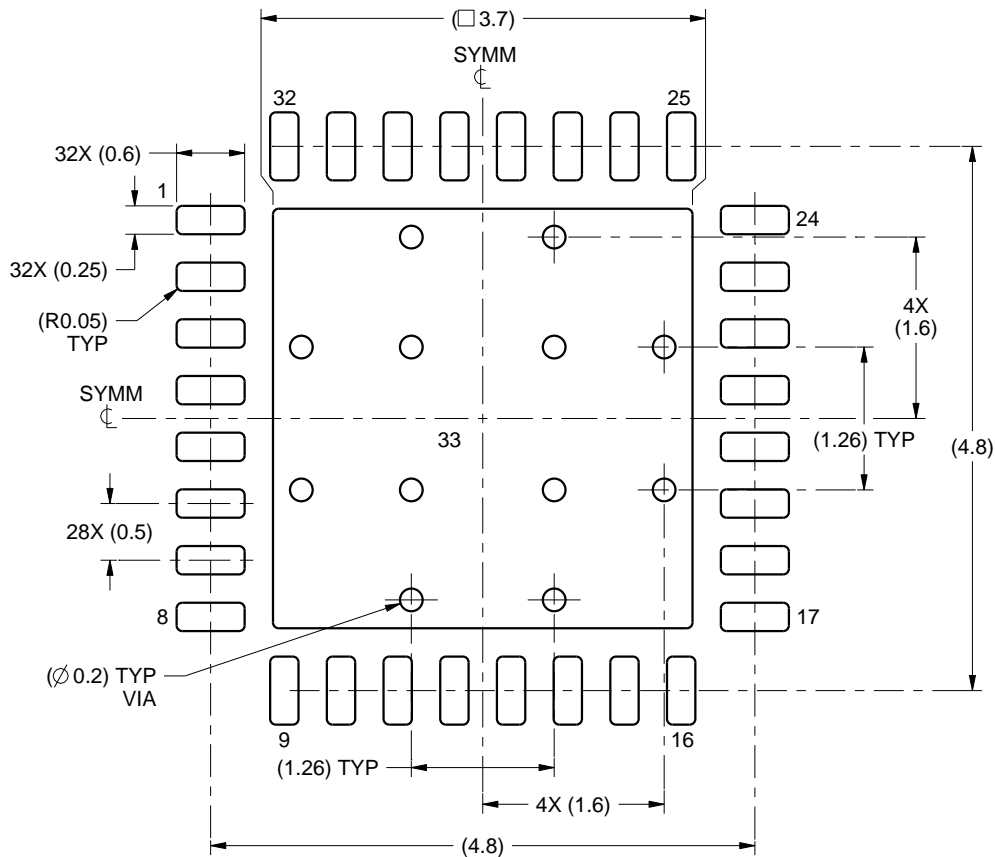
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

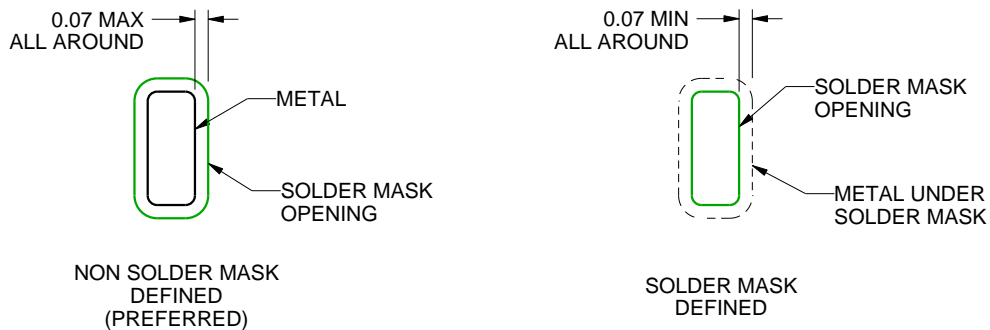
RHB0032P

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:15X



SOLDER MASK DETAILS

4223198/A 08/2016

NOTES: (continued)

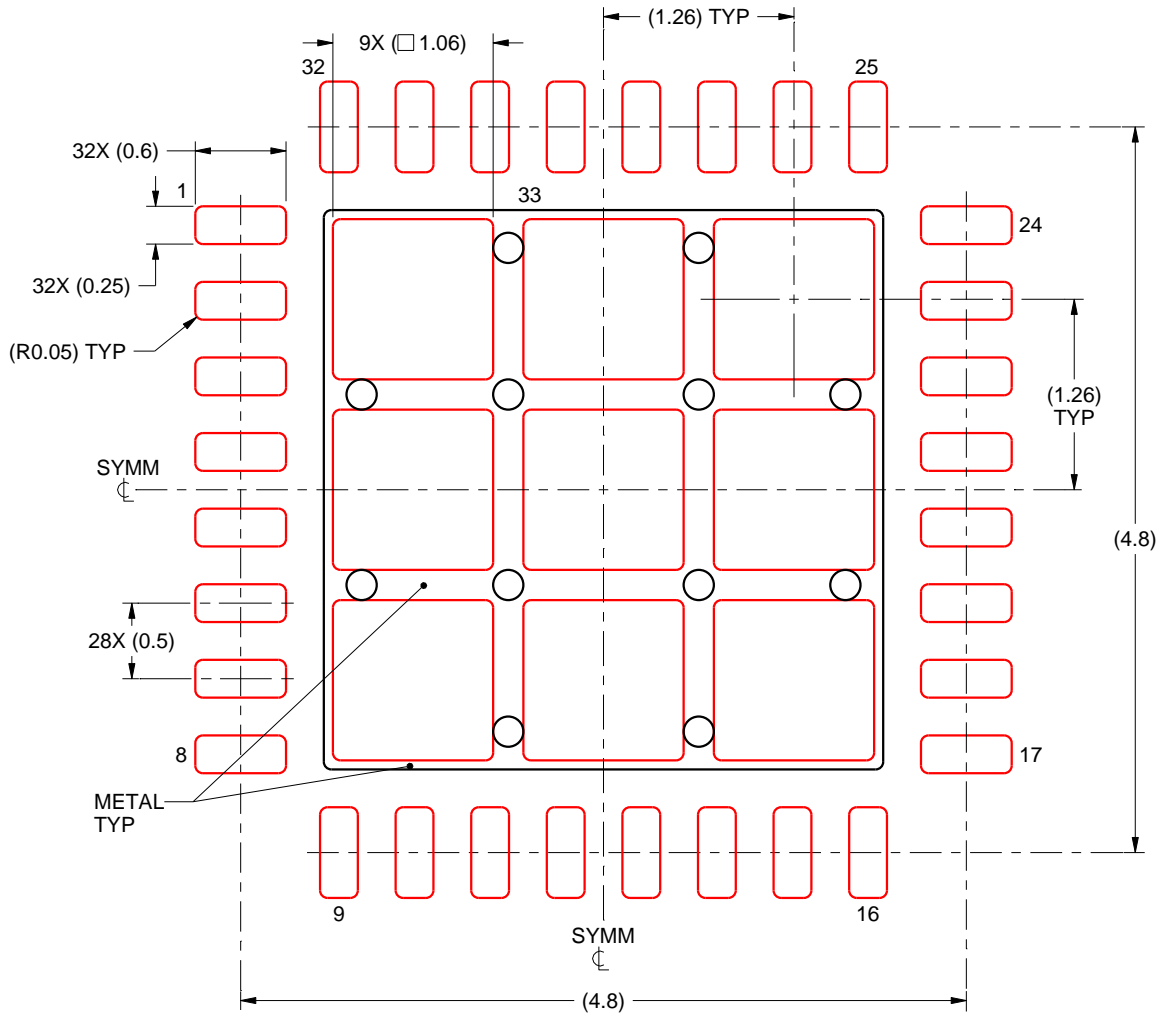
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RHB0032P

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



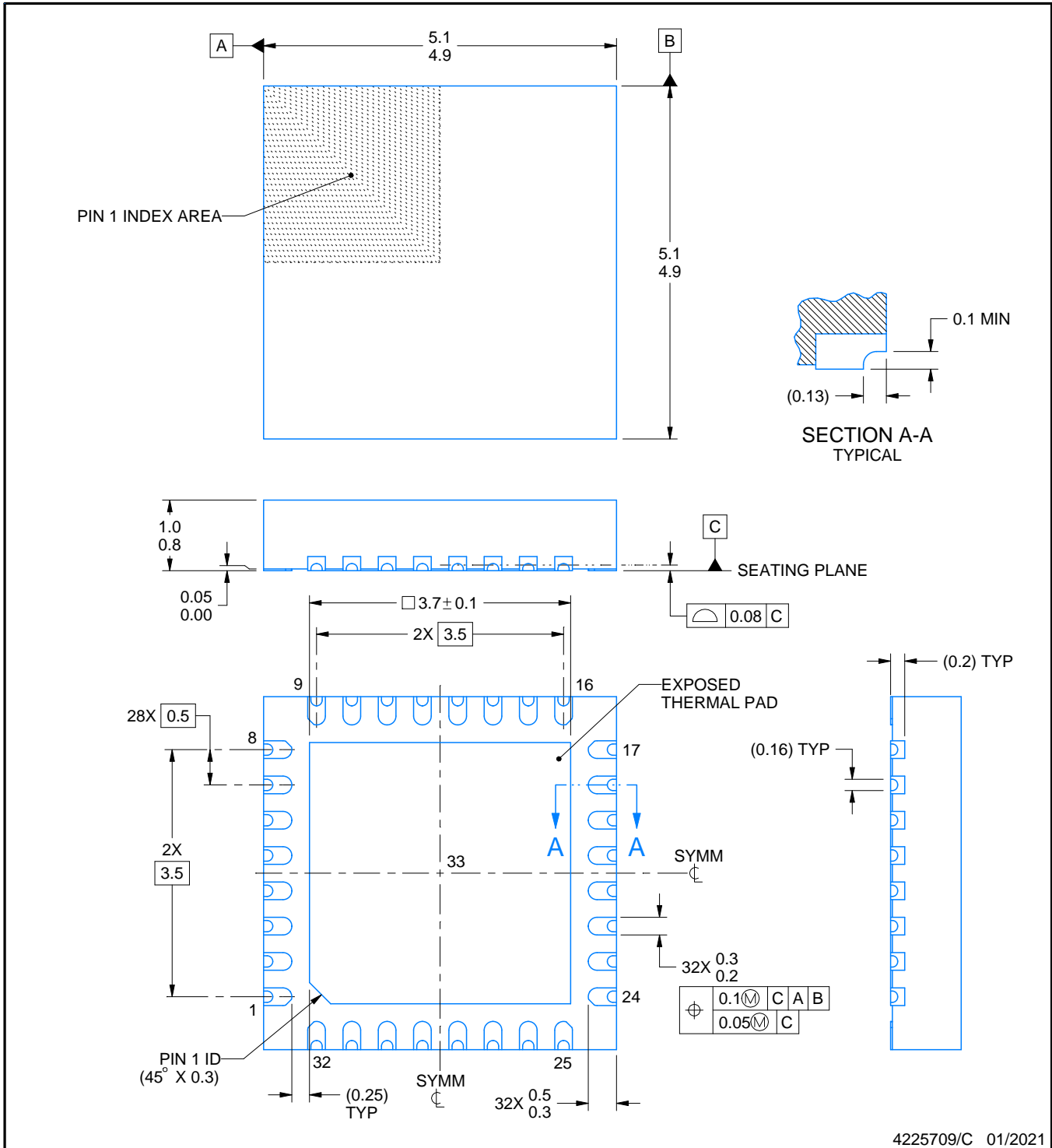
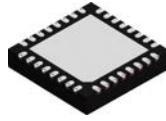
**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33  
 74% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
 SCALE:20X

4223198/A 08/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



NOTES:

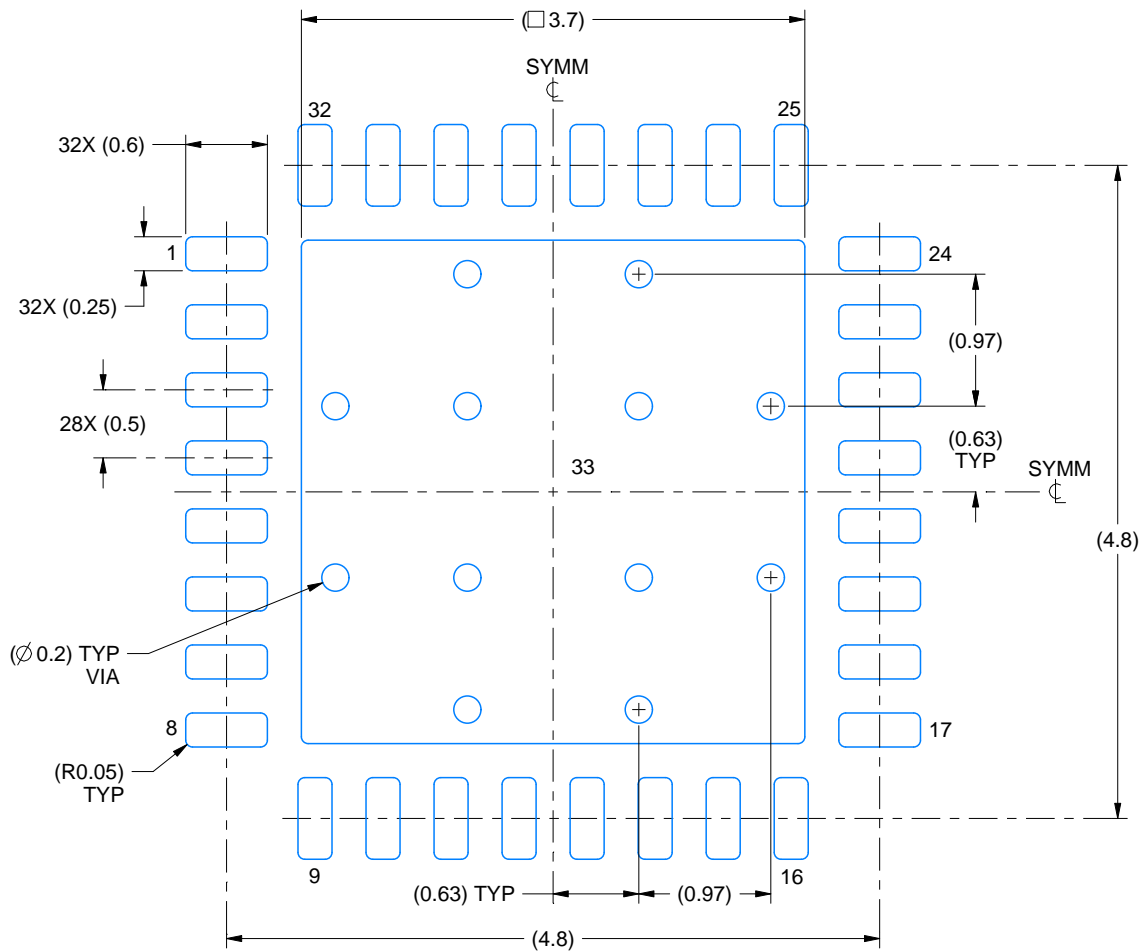
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

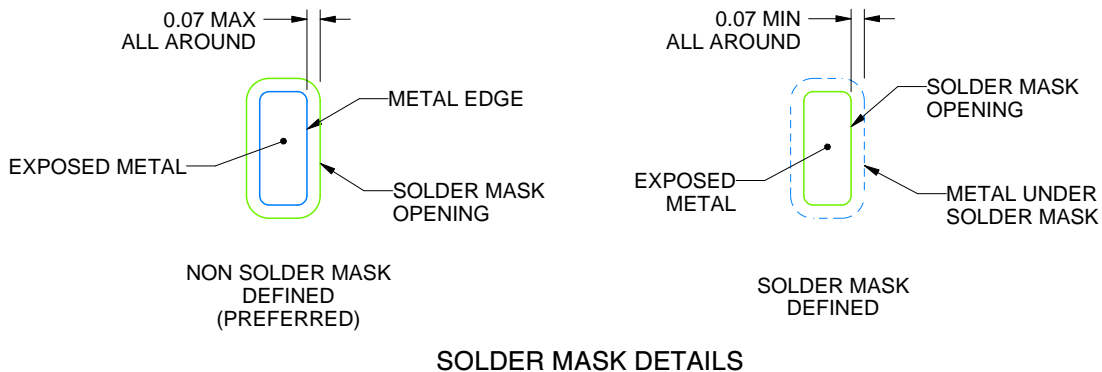
RHB0032U

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4225709/C 01/2021

NOTES: (continued)

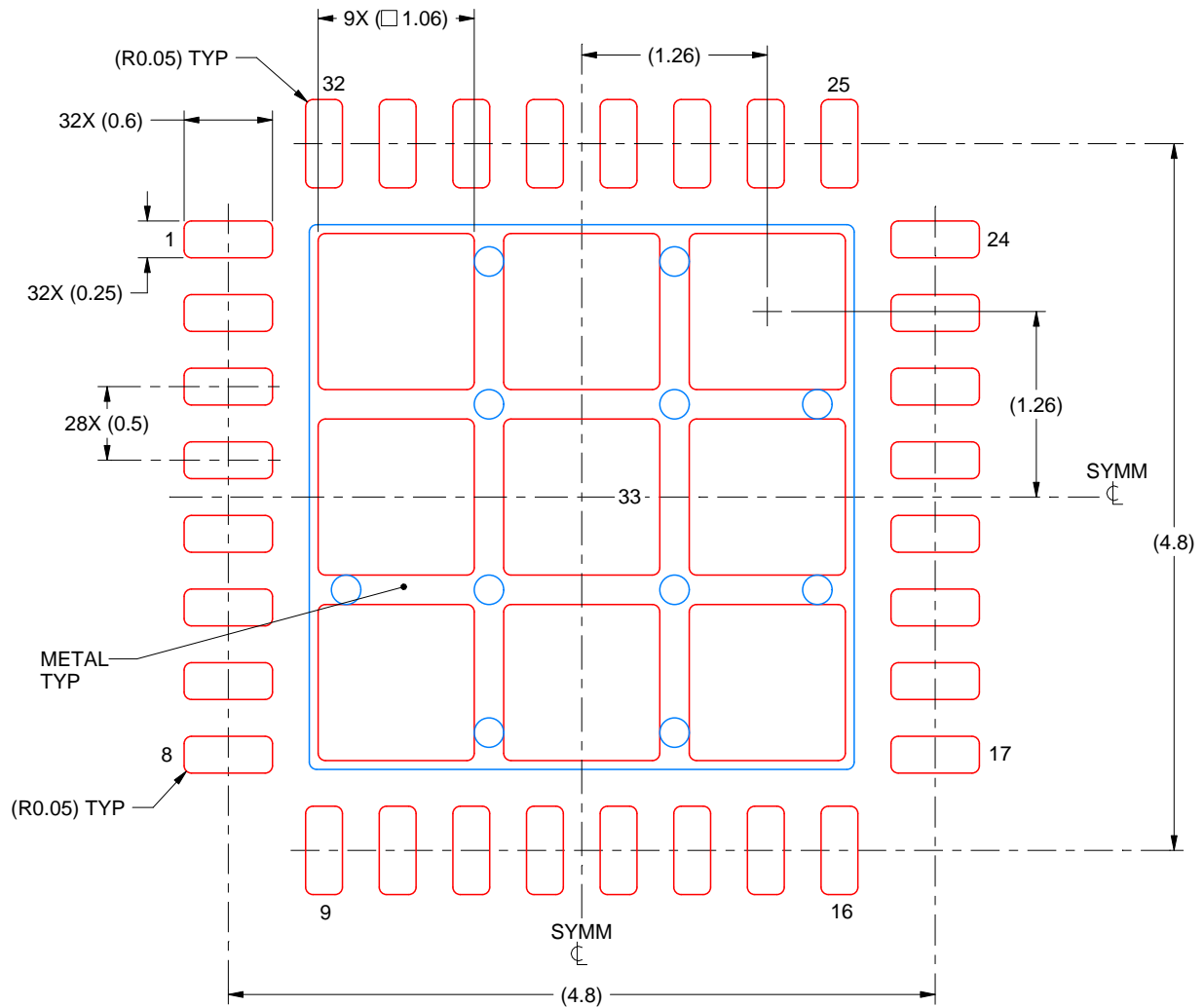
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RHB0032U

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:  
 74% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
 SCALE:20X

4225709/C 01/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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