TPS61287 23V_{IN}、25V_{OUT}、20A、同期整流昇圧コンバータ スタッカブル マルチフェーズ機能付き

1 特長

- 広い入出力電圧範囲
  - V_{IN}:2.0V～23V
  - スタートアップのための最低入力電圧:2.5V
  - V_{OUT}:4.5V～25V
- 高効率性と電力供給能力
  - スイッチ電流制限をプログラム可能:5A～20A
  - 8.5mΩ のハイサイド MOSFET を内蔵
  - スイッチング周波数:320kHz
  - V_{IN} = 3.6V、V_{OUT} = 18V、I_{OUT} = 2.0A で最大 92.3% の効率
  - V_{IN} = 7.2V、V_{OUT} = 18V、I_{OUT} = 4.0A で最大 95.48% の効率
- スタッカブル マルチフェーズ機能をサポート
- 自動 PFM モードと強制 PWM モードを選択可能
- 外部クロックへの同期機能
- 豊富な保護
  - 27V での出力過電圧保護
  - 高精度 EN/UVLO スレッショルド
  - サイクル単位の過電流保護
  - サーマル シャットダウン
- 外部ループ補償
- 2.5mm × 3.0mm VQFN HotRod™ Lite パッケージ

2 アプリケーション

- Bluetooth™ スピーカー
- LCD ディスプレイのソースドライバ
- USB Type-C® パワー デリバリ

3 概要

TPS61287 は、高電力密度の同期整流昇圧コンバータであり、ハイサイド同期整流 MOSFET を内蔵し、外付けローサイド MOSFET を使用して高効率で小型のソリューションを実現します。TPS61287 は、入力電圧範囲が 2.0V～23V と広く、出力電圧は最大 25V に対応し、20A のスイッチング バレー電流能力を備えています。

TPS61287 は、適応型一定オン時間バレー電流制御トポロジを使用して、出力電圧をレギュレートします。TPS61287 は、中負荷～重負荷時には、パルス幅変調 (PWM) モードで動作します。軽負荷時には、MODE ピンの設定により 2 つのモードを選択できます。1 つは、軽負荷時の効率向上のための自動 PFM モードです。もう 1 つは、低いスイッチング周波数によって生じる可聴ノイズなどの問題を回避する強制 PWM モードです。

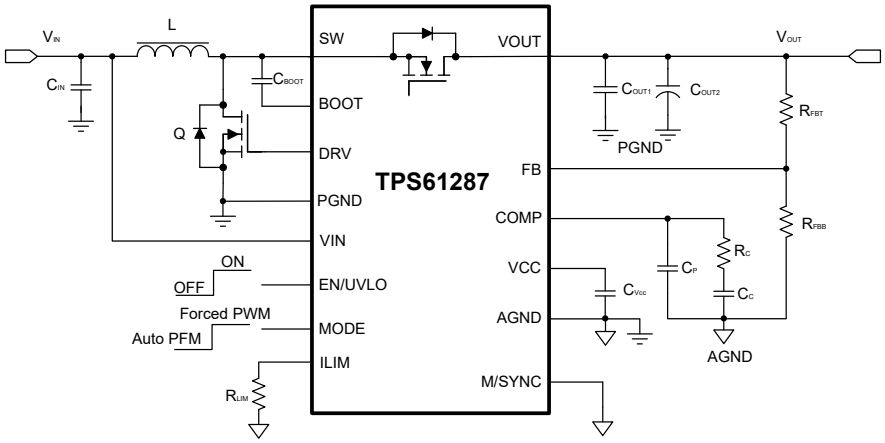
TPS61287 は、スタッカブル マルチフェーズ動作をサポートしています。最大 4 個の TPS61287 を同じスイッチング周波数でマルチフェーズ動作用に構成することで、より大きな電力と入力電流のバランシングをサポートできます。

TPS61287 は、最小限の外付けコンポーネントによる 2.5mm × 3.0mm VQFN HotRod™ Lite パッケージで、非常に小さなソリューション サイズを実現します。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ
TPS61287	VQFN (14)	2.5mm × 3.0mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



代表的なアプリケーション回路

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

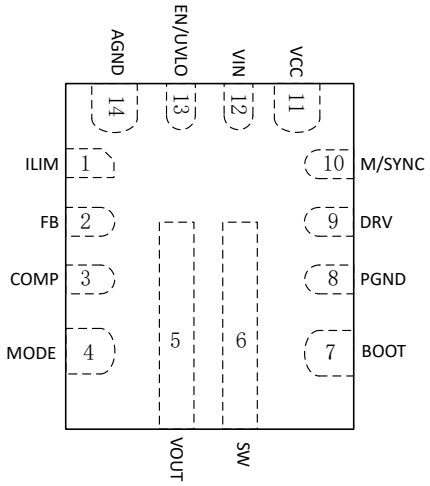

図 4-1. 14-Pin RZP VQFN Package (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NUMBER		
ILIM	1	I	Programmable switching valley current limit. An external resistor must be connected between this pin and the AGND pin.
FB	2	I	Output voltage feedback pin. Connect to the center tap of a resistor divider to program the output voltage.
COMP	3	O	Output of the internal error amplifier. Connect the loop compensation network between this pin and the AGND pin.
MODE	4	I	Operating mode selection pin at light load condition, this pin must not be floating. MODE = logic high, Forced PWM mode. MODE = logic low, Auto PFM mode.
VOUT	5	P	Boost converter output.
SW	6	P	The switching node pin. This pin is connected to the drain of the external low-side MOSFET and the source of the internal high-side MOSFET.
BOOT	7	O	Power supply for the high-side MOSFET gate driver. A ceramic capacitor of 0.1µF to 1.0µF must be connected between this pin and the SW pin.
PGND	8	G	Power ground of external low side MOSFET. Source of external low side MOSFET must be connected to this pin.
DRV	9	O	Gate driver output for external low-side MOSFET.
M/SYNC	10	I	When the M/SYNC pin is short to ground , the device works with internal configured switching frequency. When a valid clock signal is applied to this pin, the switching frequency of the device is forced to the external clock.
VCC	11	O	Output of the internal regulator. A ceramic capacitor of more than 2.2µF is required between this pin and AGND.
VIN	12	I	IC power supply input .
EN/UVLO	13	I	Enable logic input and programmable input voltage undervoltage lockout (UVLO) input. Logic high level enables the device. Logic low level disables the device and puts the device into shutdown mode. The converter start-up and shutdown levels can be programmed by connecting this pin to the supply voltage through a resistor divider. This pin must not be left floating and must be terminated.
AGND	14	G	Analog signal ground.

(1) I = Input, O = Output, G = Ground, P = Power.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	VIN, EN/UVLO	–0.3	30	V
Voltage	SW, VOUT	–0.3	32	V
Voltage	BOOT	SW–0.3	SW+6	V
Voltage	M/SYNC, MODE, VCC, COMP, FB, DRV, ILIM	–0.3	7	V
T_J	Operating Junction Temperature	–40	150	°C
T_{stg}	Storage Temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JS-002, all pins(2)	±500	

(1) HBM: JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
(2) CDM: JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process

5.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Input voltage range	2.5		23	V
VOUT	Out voltage range	4.5		25	V
L	Effective inductance range		3.3		µH
C_I	Effective input capacitance range		22		µF
C_O	Effective output capacitance range		22		µF
T_J	Operating junction temperature	-40		125	°C

5.4 Thermal Information

THERMAL METRIC		TPS61287 RZP (VQFN) - 14 PINS EVM(2)	TPS61287 RZP (VQFN) - 14 PINS Standard(1)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.6	64.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	N/A	41.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	N/A	18.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.4	1.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	18.7	18.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) Measured on TPS61287EVM, 4-layer, 2oz copper PCB.

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5.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{IN} = 3.6V and V_{OUT} = 18V. Typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
VIN	Input voltage range		2.0		23	V
VOUT	Output voltage range		4.5		25	V
V_{IN_UVLO}	Under voltage lockout threshold at VIN	V_{IN_UVLO} rising		2.2	2.3	V
V_{IN_UVLO}	Under voltage lockout threshold at VIN	V_{IN_UVLO} falling		1.9	2.0	V
V_{CC}	Internal regulator output	I_{VCC} = 15 mA		5.1		V
V_{CC_UVLO}	VCC UVLO threshold	VCC rising		2.3		V
V_{CC_UVLO}	VCC UVLO threshold	VCC falling		2.15		V
I_{Q_VIN}	Quiescent current into VIN pin	EN = High, No switching, 2.5V<VIN<5.5V, V_{FB} = V_{REF} + 0.1V, T_J up to 85°C		3	13	µA
I_{Q_VIN}	Quiescent current into VIN pin	EN = High, No switching, 6.5V<VIN<23V, V_{FB} = V_{REF} + 0.1V, T_J up to 85°C		200	250	uA
I_{Q_VOUT}	Quiescent current into VOUT pin	EN = High, No switching, 2.5V<VIN<5.5V, V_{FB} = V_{REF} + 0.1V, T_J up to 85°C		210	260	µA
I_{Q_VOUT}	Quiescent current into VOUT pin	EN = High, No switching, 6.5V<VIN<23V, V_{FB} = V_{REF} + 0.1V, T_J up to 85°C		30	60	uA
I_{Q_SW}	Quiescent current into SW pin	EN = High, No switching, 2.5V<VIN<23V, VOUT > VIN, V_{FB} = V_{REF} + 0.1V, T_J up to 85°C		2.5	5.0	µA
I_{SD_VIN}	Shutdown current into VIN pin	IC disabled, VIN = SW = 2.5V to 23V, T_J up to 85°C		1.5	7	µA
I_{SD_SW}	Shutdown current into SW pin	IC disabled, VIN = SW = 2.5V to 23V, T_J up to 85°C		0.25	2	µA
I_{SD_VOUT}	Shutdown current into VOUT pin	IC disabled, VOUT = 2.5V to 25V, VIN=0V, T_J up to 85°C		2.5	6	µA
I_{FB_LKG}	Leakage current into FB pin				50	nA
LOGIC INTERFACE						
V_{EN_H}	EN high-level voltage threshold	VCC = 5.0V			1.18	V
V_{EN_L}	EN low-level voltage threshold	VCC = 5.0V	0.4			V
$V_{EN/UVLO\_RISE}$	UVLO rising threshold at the EN/UVLO	VCC = 5.0V	1.20	1.23	1.27	V
$I_{EN/UVLO}$	Sourcing current at the EN/UVLO pin	$V_{EN/UVLO}$=1.3V		5.3		µA
V_{MODE_H}	MODE high-level voltage threshold	VCC = 5.0V			1.2	V
V_{MODE_L}	MODE low-level voltage threshold	VCC = 5.0V	0.4			V
OUTPUT						
V_{REF}	Reference voltage at the FB pin	PWM mode	0.985	1	1.015	V
V_{REF}	Reference voltage at the FB pin	PFM mode		1.01		V
V_{OUT_OVP}	Output OVP protection threshold	V_{OUT} OVP rising	25.7	27	28	V
$V_{OUT\_OVP\_HYS}$	Output OVP protection hysteresis			1		V
POWER SWITCH						
$R_{DS(on)}$	High-side MOSFET on resistance	VCC = 5.0V		8.5		mΩ
F_{SW}	Switching frequency	VIN = 3.6V, VOUT= 18V, PWM mode	285	320	355	kHz
t_{OFF_min}	Minimum off time			90	130	ns
t_{DLH}	LS-GATE off to HS-GATE on deadtime			30		ns
t_{DHL}	HS-GATE off to LS-GATE on deadtime			25		ns
I_{LIM}	High clamp valley current limit	R_{ILIM} = 20kΩ , Forced PWM mode	17	20	23	A

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T_J = –40°C to 125°C, V_{IN} = 3.6V and V_{OUT} = 18V. Typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LIM}	High clamp valley current limit	R_{ILIM} = 20kΩ , Auto PFM mode	17	20	23	A
I_{LIM}	Low clamp valley current limit			0.25		A
SOFT START						
t_{SS}	Soft start time of internal reference			7		ms
GATE DRIVER						
V_{DRV_L}	Low-state voltage drop	100-mA sinking		0.045		V
V_{DRV_H}	High-state voltage drop	100-mA sourcing		0.12		V
ERROR AMPLIFIER						
I_{SINK}	COMP pin sink current	V_{FB} = V_{REF} + 400mV, V_{COMP} = 1.5V		20		µA
I_{SOURCE}	COMP pin source current	V_{FB} = V_{REF} - 400mV, V_{COMP} = 1.5V		20		µA
V_{COMPH}	High clamp voltage at the COMP pin	R_{ILIM} = 20kΩ , PWM mode		1.6		V
V_{COMPH}	High clamp voltage at the COMP pin	R_{ILIM} = 20kΩ , PFM mode		1.45		V
V_{COMPL}	Low clamp voltage at the COMP pin			0.6		V
K_{COMP}	Power stage trans-conductance (inductor peak current / comp voltage)			20		A/V
G_{EA}	Error amplifier transconductance	VCC = 5.0V		180		µA/V
SYNCHRONOUS CLOCK						
R_{SYNC}	Internal pull down resistor from SYNC pin			800		kΩ
$V_{M/SYNC\_H}$	M/SYNC high-level voltage threshold				1.2	V
$V_{M/SYNC\_L}$	M/SYNC low-level voltage threshold		0.4			V
T_{SYNC_MIN}	Minimum sync clock pulse width		50			ns
PROTECTION						
T_{SD}	Thermal shutdown	Junction temperature rising		160		°C
T_{SD_HYS}	Thermal shutdown hysteresis			20		°C

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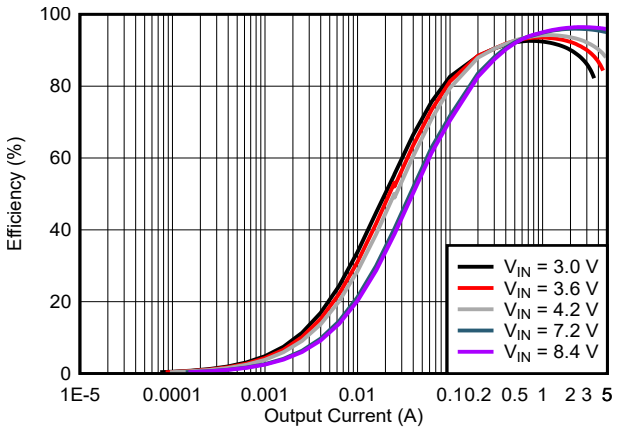
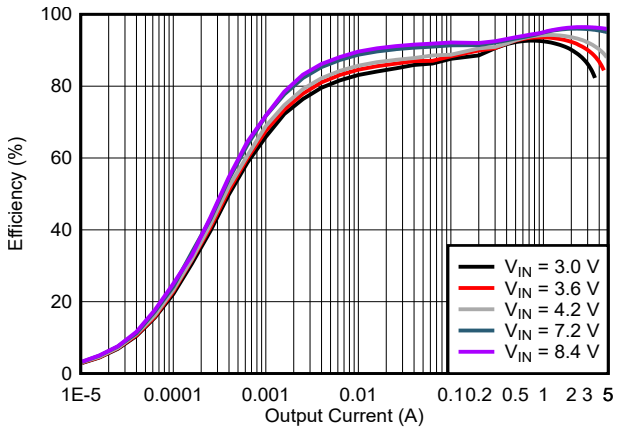
5.6 Typical Characteristics

T_A = 25°C, f_{SW} = 320 kHz, unless otherwise noted.



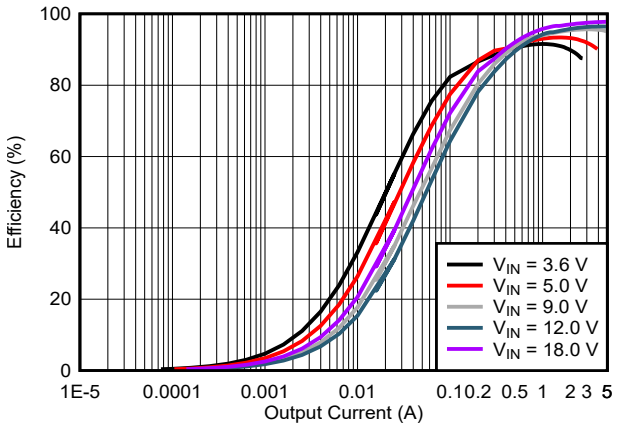
V_{IN} = 3.0V; 3.6V; 4.2V; 7.2V; 8.4V FPWM Mode

図 5-1. Efficiency vs Output Current, V_{OUT} = 18V



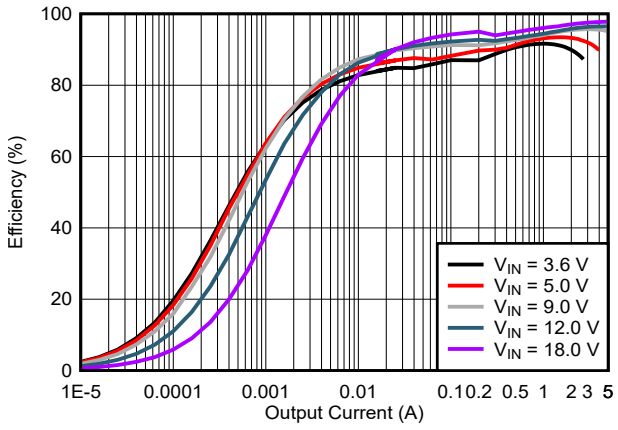
V_{IN} = 3.0V; 3.6V; 4.2V; 7.2V; 8.4V Auto PFM Mode

図 5-2. Efficiency vs Output Current, V_{OUT} = 18V



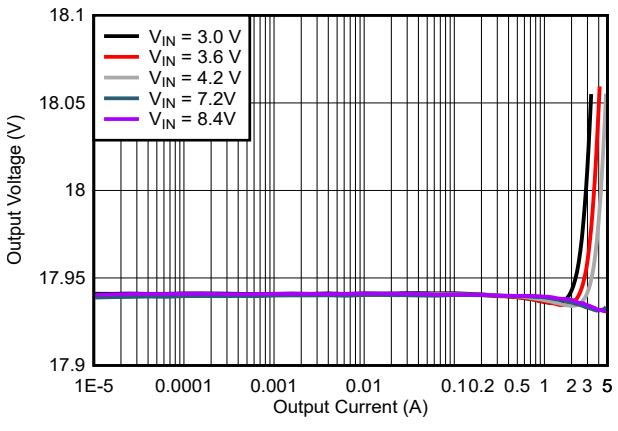
V_{IN} = 3.6V; 5.0V; 9.0V; 12.0V;18.0V FPWM Mode

図 5-3. Efficiency vs Output Current, V_{OUT} = 24V



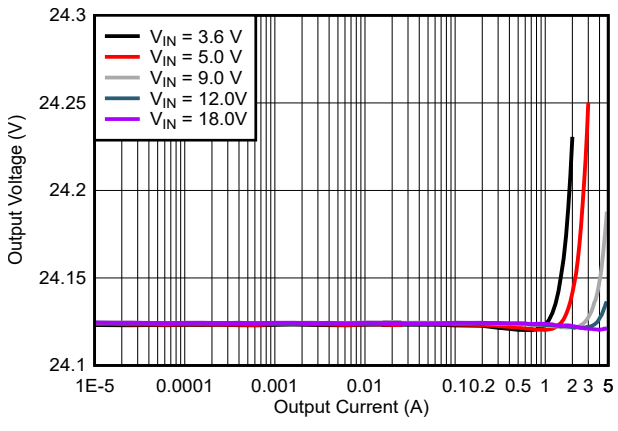
V_{IN} = 3.6V; 5.0V; 9.0V; 12.0V; 18.0V Auto PFM Mode

図 5-4. Efficiency vs Output Current, V_{OUT} = 24V



V_{IN} = 3.0V; 3.6V; 4.2V; 7.2V; 8.4V FPWM Mode

図 5-5. Output Voltage vs Output Current, V_{OUT} = 18V



V_{IN} = 3.6V; 5.0V; 9.0V; 12.0V; 18.0V FPWM Mode

図 5-6. Output Voltage vs Output Current, V_{OUT} = 24V

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5.6 Typical Characteristics (continued)

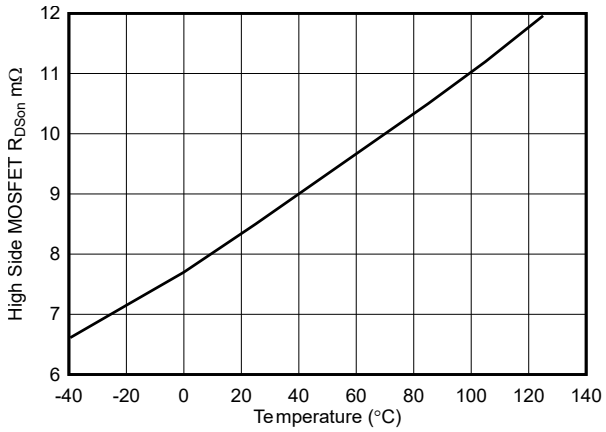


図 5-7. R_{DSON} vs Temperature

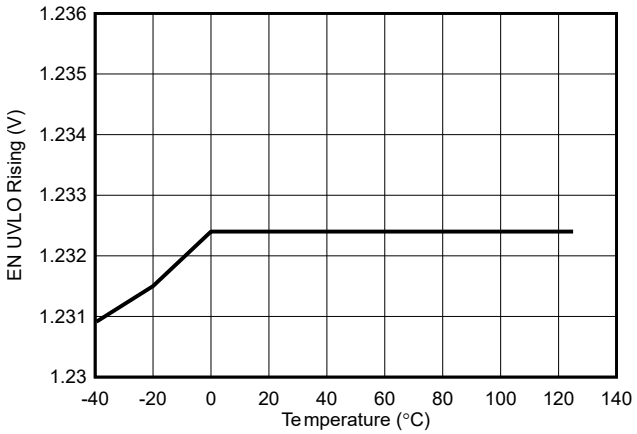


図 5-8. EN/UVLO Rising Voltage vs Temperature

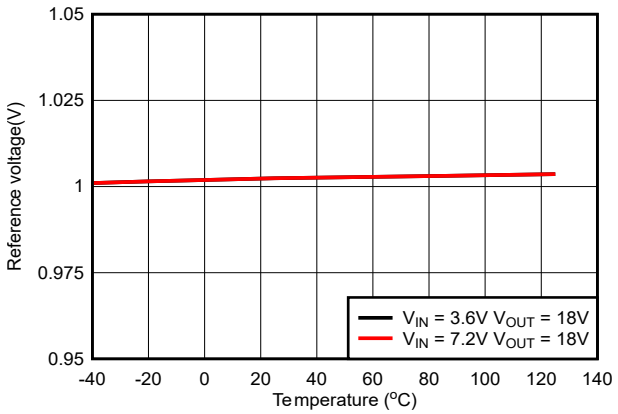


図 5-9. Reference Voltage vs Temperature

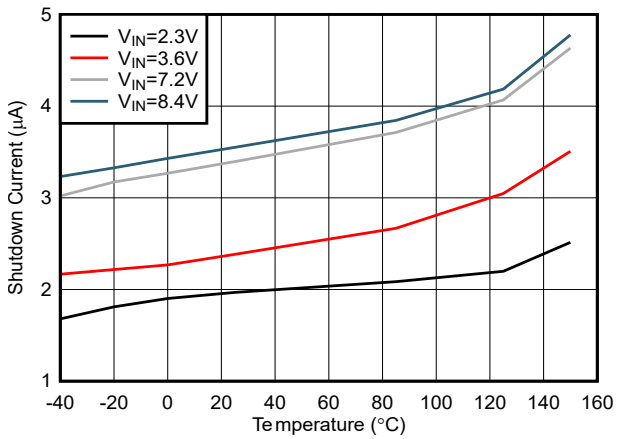
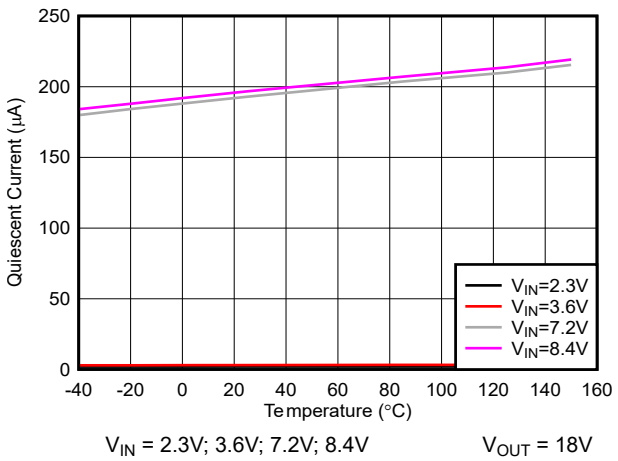
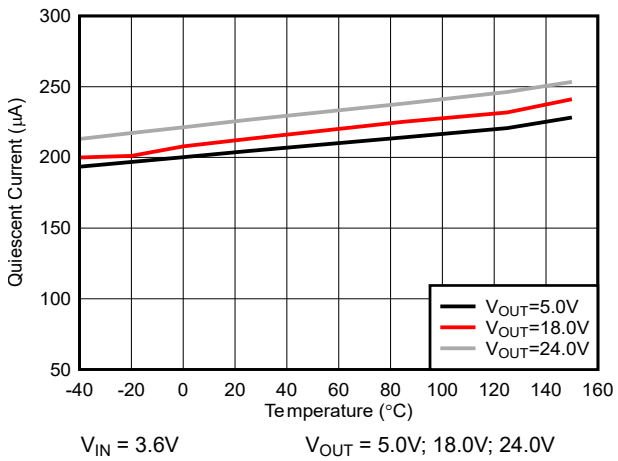


図 5-10. Shutdown Current vs Temperature



V_{IN} = 2.3V; 3.6V; 7.2V; 8.4V V_{OUT} = 18V

図 5-11. Quiescent Current into VIN vs Temperature



V_{IN} = 3.6V V_{OUT} = 5.0V; 18.0V; 24.0V

図 5-12. Quiescent Current into VOUT vs Temperature

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6 Detailed Description

6.1 Overview

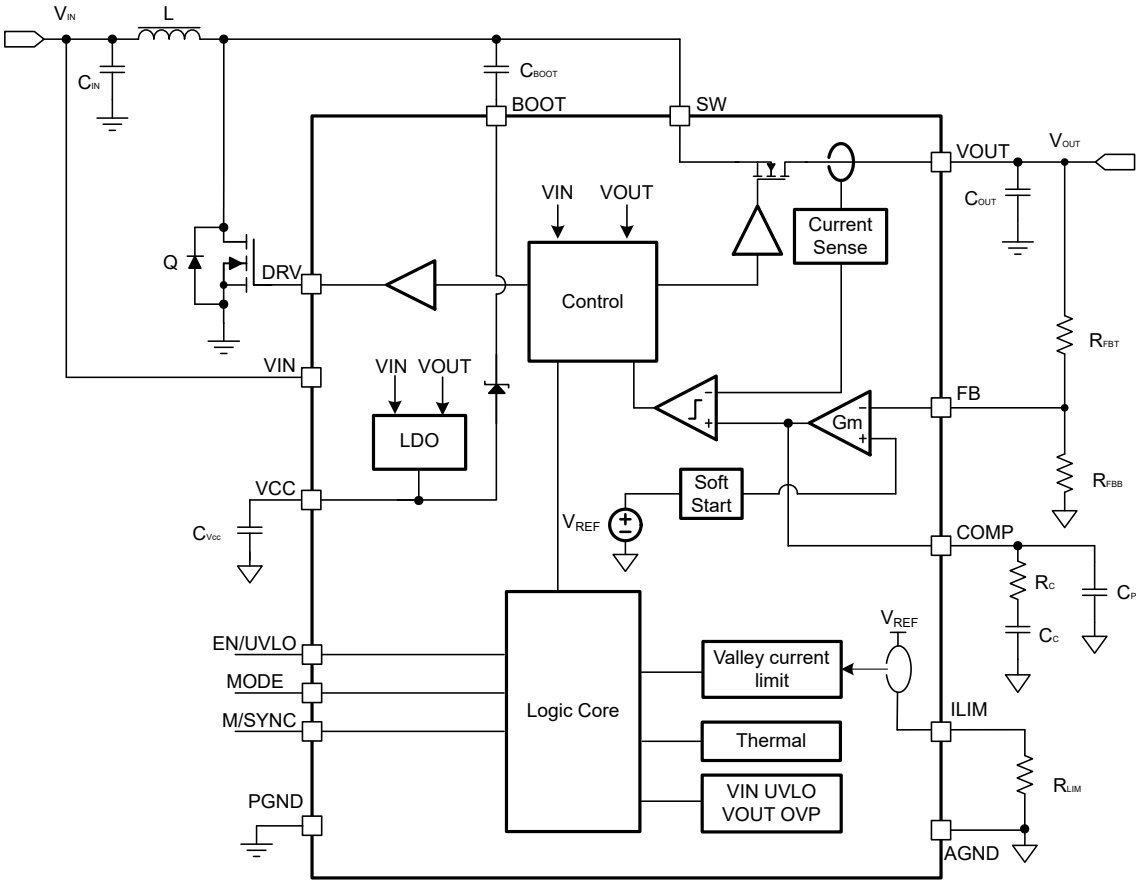
The TPS61287 is a high-power density, synchronous boost converter that integrates the high side synchronous rectifier MOSFET and uses an external low side MOSFET to provide a high efficiency and small size solution. The TPS61287 has a wide input voltage range from 2.0V to 23V and the output voltage covers up to 25V with 20A switching valley current capability.

The TPS61287 uses an adaptive constant on-time valley current control topology to regulate the output voltage. Under moderate to heavy load condition, the TPS61287 operates in pulse width modulation (PWM) mode. There are two optional modes in light load by configuring the MODE pin: Auto PFM mode to improve light-load efficiency and Forced PWM to avoid audible noise and other problems caused by low switching frequency. The switching frequency in the PWM mode is 320kHz. The TPS61287 provides 27V output overvoltage protection, cycle-by-cycle overcurrent protection, and thermal shutdown protection.

The TPS61287 supports stackable multi-phase operation. Two TPS61287 can build a stackable dual-phase converter. Furthermore, up to 4 pcs TPS61287 can be configured for multi-phase operation at same switching frequency to support higher power and inductor current balancing. Multi-phase operation greatly reduces peak inductor current, and capacitor ripple current, and increases effective switching frequency, minimizing inductor and capacitor sizes.

The TPS61287 offers a very small solution size with 2.5mm x 3.0mm VQFN HotRod™ Lite package with minimal external components.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Enable and Start-up

The TPS61287 has a soft start function to prevent high inrush current during start-up. When the EN/UVLO pin is pulled high, the internal soft-start capacitor is charged with a constant current. During this time, the soft-start capacitor voltage is compared with the internal reference (1.0V). The lower one is fed into the internal positive input of the error amplifier. The output of the error amplifier (which determines the inductor valley current value) ramps up slowly as the soft-start capacitor voltage goes up. The soft-start phase is completed after the soft-start capacitor voltage exceeds the internal reference (1.0V), which takes 7ms from 0V to 1.0V. When the EN pin is pulled low, the voltage of the soft-start capacitor is discharged to ground.

6.3.2 Undervoltage Lockout (UVLO)

The UVLO circuit prevents the device from malfunctioning at low input voltage and the battery from excessive discharge. The TPS61287 has both V_{IN_UVLO} and V_{CC_UVLO} function. This lockout functions disables the device from switching when the falling voltage at the VIN pin trips the falling UVLO threshold V_{IN_UVLO}, which is typically 1.9V. The device starts operating when the rising voltage at the VIN pin trips the rising UVLO threshold typically 2.2V. It also disables the device when the falling voltage at the VCC pin trips the UVLO threshold V_{CC_UVLO}, which is typically 2.15V.

6.3.3 Programmable EN/UVLO

The TPS61287 has a dual function enable and undervoltage lockout (UVLO) circuit at EN/UVLO pin. When the voltage at the VIN and VCC pin is above the rising threshold of UVLO and the EN/UVLO pin is pulled above 1.18V but below the enable EN/UVLO threshold of 1.23V, the TPS61287 is enabled but still in standby mode.

The EN/UVLO pin has an accurate UVLO voltage threshold to support programmable input undervoltage lockout with hysteresis. When the EN/UVLO pin voltage is greater than the UVLO threshold of 1.23V, the TPS61287 is enabled for switching operation. A hysteresis current, I_{UVLO_HYS}, is sourced out of the EN/UVLO pin to provide a hysteresis that prevents on/off chatter in the presence of noise with a slowly changing input voltage.

By using resistor divider as shown in 図 6-1, the turn-on threshold is calculated using 式 1.

$$V_{IN\,(UVLO\_ON)} = V_{UVLO} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

where

- V_{UVLO} is the UVLO threshold of 1.23V at the EN/UVLO pin.

The hysteresis between the UVLO turn-on threshold and turn-off threshold is set by the upper resistor in the EN/UVLO resistor divider and is given by 式 2.

$$\Delta V_{IN\,(UVLO)} = I_{UVLO\_HYS} \times R1 \quad (2)$$

where

- I_{UVLO_HYS} is the sourcing current from the EN/UVLO pin when the voltage at the EN/UVLO pin is above V_{UVLO}.

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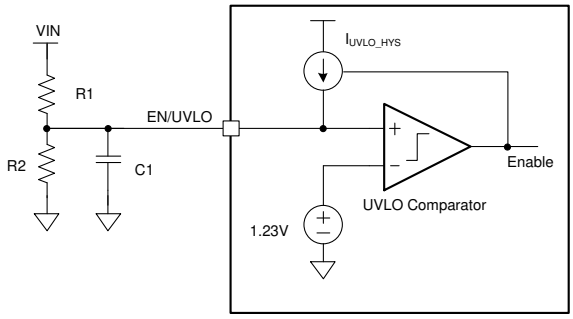

図 6-1. Programmable UVLO With Resistor Divider at the EN/UVLO Pin

By using an NMOSFET together with a resistor divider the user can implement both logic enable and programmable UVLO as shown in 図 6-2. The EN logic high level must be greater than the enable threshold plus the V_{th} of the NMOSFET Q1. The Q1 also eliminates the leakage current from VIN to ground through the UVLO resistor divider during shutdown mode.

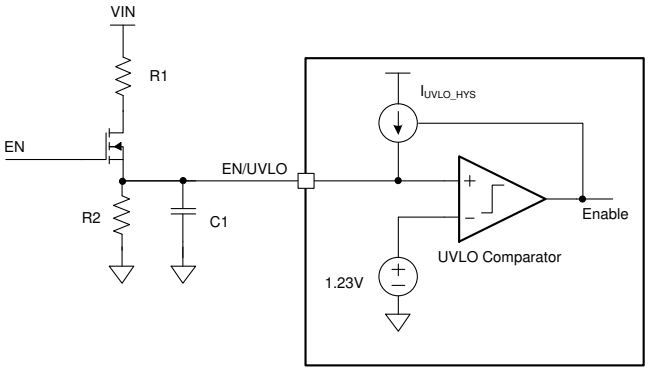

図 6-2. Logic Enable and Programmable UVLO

6.3.4 Switching Valley Current Limit

The TPS61287 has an internal cycle-by-cycle current limit to prevent the inadvertent application of a large switching current. Current limit detection occurs during the off-time by sensing of the voltage drop across the integrated high-side MOSFET. The high-side MOSFET is turned off immediately as soon as the switch valley current triggers the limit threshold. The switch valley current limit can be set by a resistor from the ILIM pin to ground. The relationship between the valley current limit and the resistor is shown in 式 3.

$$I_{valley}\left(A\right) = \frac{400k}{R_{LIM}(k)} \tag{3}$$

where

- R_{LIM} is the resistance between the ILIM pin and the AGND pin.
- I_{valley} is the switch valley current limit.

For instance, the valley current limit is 20A if the R_{LIM} is 20kΩ . ILIM pin can not be left floating or connected to VCC.

6.3.5 External Clock Synchronization

The TPS61287 can synchronize to an external clock signal applied to the M/SYNC pin for noise-sensitive or multiphase applications. When an external clock signal is applied to the M/SYNC pin, the device switching frequency is forced to the external clock. The external clock frequency must be within ±20% of default switching frequency 320kHz. The external clock on the M/SYNC pin must have a low-level voltage less than 0.4V and a

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high-level voltage greater than 1.2V. A valid synchronous clock signal must be greater than 50ns wide and have a minimum of 4 consecutive clocks prior to synchronization.

The TPS61287 can fail to synchronize to external clock when reaches switching limitations, such as reaching minimum on time, minimum off time, current limit and so on.

Connect M/SYNC pin to GND to avoid noise when external synchronization function is not used.

6.3.6 Stackable Multi-phase Operation

The TPS61287 supports stackable multi-phase operation. Two TPS61287 can build a stackable dual-phase converter. The M/SYNC of the host device is connected to ground. The M/SYNC of the subordinate device is connected to the attenuated signal of the driver pin of the host device. 図 6-3 shows the 2 pcs TPS61287 stackable configuration. Forced PWM mode is recommeded for a better current balance and reliable phase shifting.

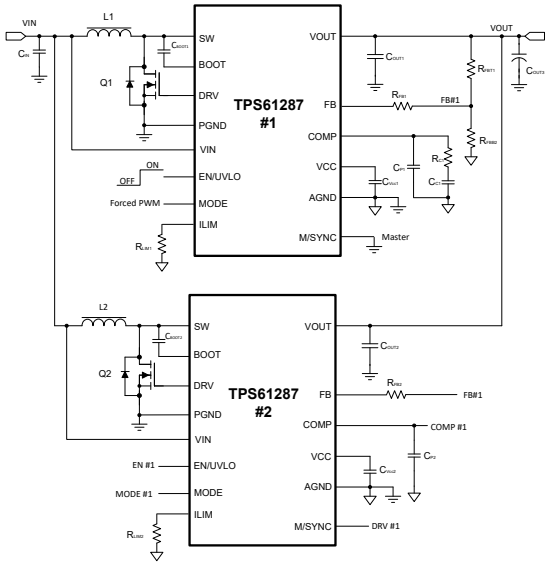

図 6-3. TPS61287 dual phase operation for high power application

Furthermore, up to 4 pcs TPS61287 can be configured for multi-phase operation at same switching frequency to support higher power and inductor current balancing. Multi-phase operation greatly reduces peak inductor current, and capacitor ripple current, and increases effective switching frequency, minimizing inductor and capacitor sizes. 図 6-4 shows the 4 pcs TPS61287 stackable configuration.

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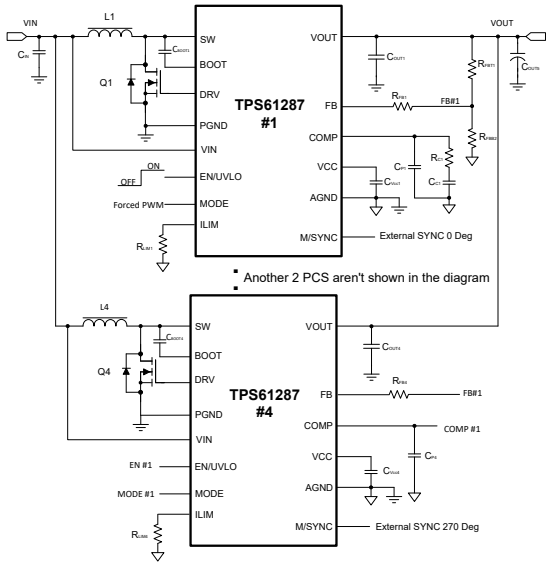

図 6-4. TPS61287 multi phase operation for high power application

6.3.7 Device Functional Modes

The TPS61287 operates at 320kHz frequency pulse width modulation (PWM) in moderate-to-heavy load condition. At light load, the TPS61287 implements two operating modes, Auto PFM mode and Forced PWM mode, to meet different application requirements. The operating mode is set by the status of the MODE pin. When the MODE pin is logic high, the device operates in Forced PWM mode. When the MODE pin is logic low, the device operates in Auto PFM mode.

6.3.7.1 Forced PWM Mode

In Forced PWM mode, the TPS61287 keeps the switching frequency unchanged at light load. When the load current decreases, the output of the internal error amplifier decreases as well to keep the inductor valley current down, delivering less power from input to output. When the output current further reduces, the current through the inductor decreases to zero during the off-time. The high-side N-MOSFET is not turned off even if the current through the MOSFET is zero. Thus, the inductor current changes its direction after it runs to zero. The power flow is from output side to input side. The efficiency is low in this mode. But with the fixed switching frequency, there is no audible noise and other problems which might be caused by low switching frequency at light load.

6.3.7.2 Auto PFM Mode

In Auto PFM mode , the TPS61287 provides a seamless transition from PWM to PFM operation and enables automatic pulse-skipping mode that provides excellent efficiency over a wide load range. As load current decreasing or VIN rising, the output of the internal error amplifier decreases to lower the inductor valley current, delivering less power to the load. When the output of the error amplifier goes down and reaches a threshold of about 250mA valley current, the output of the error amplifier is clamped at this value and does not decrease any more, the TPS61287 extends its off-time of the switching period to deliver less energy to the output and regulate the output voltage at 1.01 times of the normal value.

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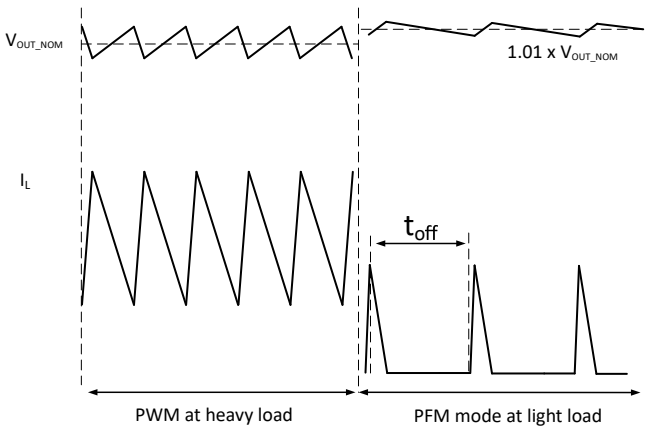

図 6-5. Auto PFM Mode Diagram

6.3.8 Overvoltage Protection

If the output voltage at the VOUT pin is detected above 27V (typical value), the TPS61287 stops switching immediately until the voltage at the VOUT pin drops the hysteresis value lower than the output overvoltage protection threshold. This function prevents overvoltage on the output and secures the circuits connected to the output from excessive overvoltage.

6.3.9 Thermal Shutdown

The thermal shutdown is implemented to prevent damage from excessive heat and power dissipation. Typically, the thermal shutdown occurs when junction temperatures exceeding 160°C (typical). If the thermal shutdown is triggered, the device stops switching and recovers when the junction temperature drops below 140°C (typical).

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7 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS61287 is designed for output voltage up to 25V with the 20A switch current capability. The TPS61287 operates at a quasi-constant frequency pulse-width modulation (PWM) in moderate to heavy load condition. At light load, the converter can operate in either Auto PFM mode or Forced PWM mode, depending on the mode selected. The Auto PFM mode provides high efficiency over the entire load range, while the Forced PWM mode can avoid the acoustic noise as the switching frequency is fixed. The converter uses the adaptive constant on-time valley current control scheme, which provides excellent transient line and load response with minimal output capacitance. The TPS61287 can work with different inductor and output capacitor combinations by external loop compensation.

7.2 Typical Application

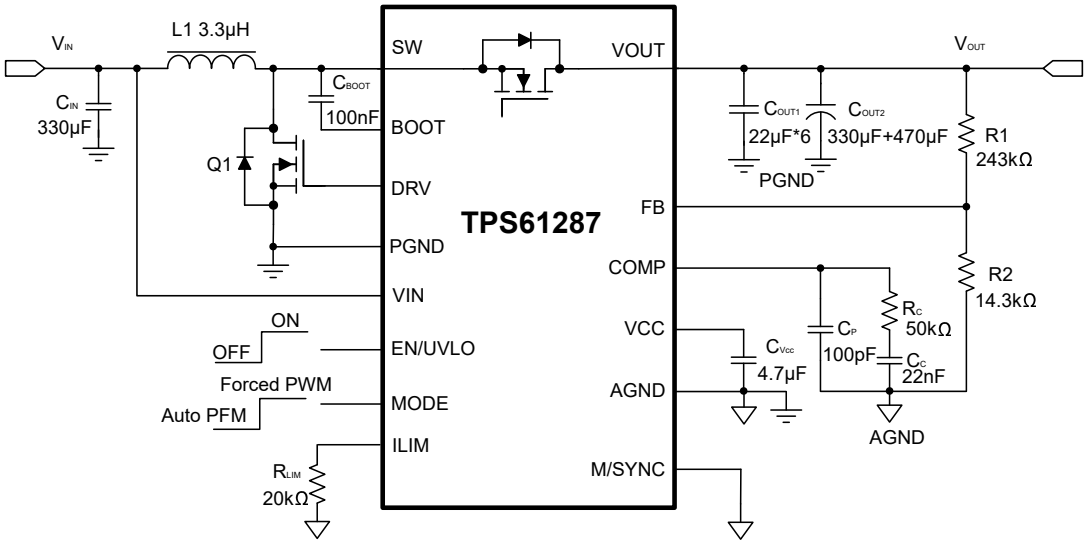

図 7-1. TPS61287 3.6V Vin to 18V Vout 3A Output Converter

7.2.1 Design Requirements

表 7-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	3.3V to 4.2V
Output voltage	18V
Output voltage ripple	180mV peak-to-peak
Output current rating	3A

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7.2.2 Detailed Design Procedure

7.2.2.1 Setting Output Voltage

The output voltage is set by an external resistor divider (R1, R2 in the 図 7-1 circuit diagram). For the best accuracy, R2 should be smaller than 300 kΩ to ensure the current flowing through R2 is at least 100 times larger than the FB pin leakage current. Changing R2 towards a lower value increases the immunity against noise injection. Changing R2 to higher values reduces the quiescent current to achieve higher efficiency at light load.

The value of R1 is then calculated as:

$$R_1 = \frac{(V_{OUT} - V_{REF}) \times R_2}{V_{REF}} \tag{4}$$

7.2.2.2 Inductor Selection

Since the selection of the inductor affects the steady state of the power supply operation, transient behavior, loop stability, and boost converter efficiency, the inductor is the most important component in switching power regulator design. The three most important specifications to the performance of the inductor are the inductor value, DC resistance, and saturation current.

The TPS61287 is recommended to work with inductor values between 2.2µH and 4.7µH. A 2.2µH inductor is typically available in a smaller or lower-profile package, while a 4.7µH inductor produces lower inductor current ripple.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, the inductance can decrease 20% to 35% from the value at 0A current, depending on how the inductor vendor defines saturation. When selecting an inductor, verify that the rated current of the inductor, especially the saturation current, is larger than the peak current during the operation.

Follow 式 5 to 式 7 to calculate the peak current of the inductor. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, and maximum load current of the application. To leave enough design margin, TI recommends using the minimum switching frequency, the inductor value with –30% tolerance, and a low-power conversion efficiency for the calculation.

In a boost regulator, calculate the inductor DC current as in 式 5.

$$I_{DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \tag{5}$$

where

- V_{OUT} is the output voltage of the boost regulator.
- I_{OUT} is the output current of the boost regulator.
- V_{IN} is the input voltage of the boost regulator.
- η is the power conversion efficiency.

Calculate the inductor current peak-to-peak ripple as in 式 6.

$$I_{PP} = \frac{1}{L \times \left(\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}}\right) \times f_{SW}} \tag{6}$$

where

- I_{PP} is the inductor peak-to-peak ripple.
- L is the inductor value.
- f_{SW} is the switching frequency.
- V_{OUT} is the output voltage.

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- V_{IN} is the input voltage.

Therefore, the peak current, I_{Lpeak}, seen by the inductor is calculated with 式 7.

$$I_{Lpeak} = I_{DC} + \frac{I_{PP}}{2} \quad (7)$$

The selected the inductor shall be with saturation current higher than the peak current calculated.

The valley current, $I_{Lvalley}$, seen by the inductor is calculated with 式 8.

Set the current limit of the TPS61287 higher than the calculated valley current .

$$I_{Lvalley} = I_{DC} - \frac{I_{PP}}{2} \quad (8)$$

Boost converter efficiency is dependent on the resistance of its current path, the switching loss associated with the switching MOSFETs, and the core loss of the inductor. The TPS61287 has optimized the internal switch resistance.

However, the overall efficiency is affected significantly by the DC resistance (DCR) of the inductor, equivalent series resistance (ESR) at the switching frequency, and the core loss. Core loss is related to the core material and different inductors have different core loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss. Usually, a data sheet of an inductor does not provide the ESR and core loss information. If needed, consult the inductor vendor for detailed information. Generally, TI recommend an inductor with lower DCR and ESR. However, there is a tradeoff among the inductance of the inductor, DCR and ESR resistance, and its footprint. Furthermore, shielded inductors typically have higher DCR than unshielded inductors.

表 7-2 lists recommended inductors for the TPS61287. Verify whether the recommended inductor can support the user target application with the previous calculations and bench evaluation. In this application, Coilcraft's inductor, XGL1060-332MEC is selected for its small size.

表 7-2. Recommended Inductors

PART NUMBER	L (µH)	DCR MAX (mΩ)	SATURATION CURRENT/HEAT RATING CURRENT (A)	SIZE MAX (L × W × H mm)	VENDOR(1)
CMLE105T-2R2MS	2.2	4.5	26.0 / 19.5	10.3 x 11.5 x 5.0	Cyntec
CMME105T-3R3MS	3.3	7.5	22.0 / 15.0	10.3 x 11.5 x 5.0	Cyntec
XAL1060-222MEC	2.2	4.3	31.0 / 25.3	10.0 x 11.3 x 6.0	Coilcraft
XGL1060-332MEC	3.3	5.7	26.0 / 22.0	10.0 × 11.3 × 6.0	Coilcraft

(1) See the Third-party Products Disclaimer

7.2.2.3 Bootstrap And VCC Capacitors Selection

The bootstrap capacitor between the BOOT and SW pin supplies the gate current to charge the high-side FET device gate during the turn on of each cycle. The gate current also supplies charge for the bootstrap capacitor. The recommended value of the bootstrap capacitor is 0.1µF to 1.0µF. C_{BOOT} must be a good quality, low-ESR ceramic capacitor located at the pins of the device to minimize potentially damaging voltage transients caused by trace inductance.

The VCC pin is the output of the internal LDO. A ceramic capacitor of more than 2.2µF is required at the VCC pin to get a stable operation of the LDO.

7.2.2.4 MOSFET Selection

The external power MOSFET must be selected with V_{DS} rating that can withstand the maximum output voltage plus transient spikes (ringing). 40V rated MOSFET is selected in this application.

Once the voltage rating is determined, select the MOSFETs by making tradeoffs between MOSFET $R_{DS(ON)}$ and total gate charge (Qg) to balance conduction and switching losses.

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Be aware of the deadtime limitation, verify that the low-side and high-side MOSFET are not turned on simultaneously. A leadless package is preferred for this high switching-frequency design to minimumize the driving parasitic inductance. Be careful when adding series gate resistors, as this can decrease the effective deadtime.

The MOSFET gate driver current of the device is supplied from VCC. Before start-up, the VCC voltage is powered from VIN from an internal LDO. Verify that the gate threshold voltage(Vth) of MOSFET is lower than minimum VIN voltage for the target design to guarntee a fully turn on of the MOSFET.

The maximum gate charge power is limited by the 15mA VCC sourcing current limit. Driving loss must be considered to meet the sourcing current limit of VCC.

7.2.2.5 Input Capacitor Selection

Multilayer ceramic capacitors are an excellent choice for the input decoupling of the step-up converter since they have extremely low ESR and are available in small footprints. Input capacitors must be located as close as possible to the device. While a 22µF input capacitor or equivalent is sufficient for the most applications, larger values can be used to reduce input current ripple.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or can even damage the device. Additional "bulk" capacitor (electrolytic or tantalum) in this circumstance, must be placed between C_{IN} and the power source lead to reduce ringing that can occur between the inductance of the power source leads and C_{IN}.

7.2.2.6 Output Capacitor Selection

Typically, a combination of ceramic capacitors and bulk electrolytic capacitors is needed to provide low ESR, high ripple current capacity, and small output voltage ripple.

When input voltage reaches the minimum value , there is the largest output voltage ripple caused by the capacitance. From the required output voltage ripple, use the following equations to calculate the minimum required effective capacitance C_{OUT}:

$$V_{ripple\_dis} = \frac{(V_{OUT} - V_{IN\_MIN}) \times I_{OUT}}{V_{OUT} \times f_{SW} \times C_{OUT}} \quad (9)$$

$$V_{ripple\_ESR} = I_{Lpeak} \times R_{C\_ESR} \quad (10)$$

where

- V_{ripple_dis} is output voltage ripple caused by charging and discharging of the output capacitor.
- V_{ripple_ESR} is output voltage ripple caused by ESR of the output capacitor.
- V_{IN_MIN} is the minimum input voltage of boost converter.
- V_{OUT} is the output voltage.
- I_{OUT} is the output current.
- I_{Lpeak} is the peak current of the inductor.
- f_{SW} is the converter switching frequency.
- R_{C_ESR} is the ESR of the output capacitors.

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DC bias effect: High-capacitance ceramic capacitors have a DC bias effect, which has a strong influence on the final effective capacitance. Therefore, the right capacitor value must be chosen carefully. The differences between the rated capacitor value and the effective capacitance result from package size and voltage rating in combination with material. A 10-V rated 0805 capacitor with 10 µF can have an effective capacitance of less than 5 µF at an output voltage of 5 V.

7.2.2.7 Loop Stability

The TPS61287 requires external compensation, which allows the loop response to be optimized for each application. The COMP pin is the output of the internal error amplifier. An external compensation network, comprised of resistor R_C, and ceramic capacitors C_C and C_P, is connected to the COMP pin.

The power stage small signal loop response of constant on-time (COT) with peak current control can be modeled by 式 11.

$$G_{PS}(S)=K_{COMP}\times\frac{R_O\times(1\text{-}D)}{2}\times\frac{\left(1+\frac{S}{2\pi f_{ESRZ}}\right)\times\left(1-\frac{S}{2\pi f_{RHPZ}}\right)}{1+\frac{S}{2\pi f_P}} \tag{11}$$

where

- D is the switching duty cycle.
- R_O is the output load resistance.
- K_{COMP} is power stage trans-conductance (inductor peak current / comp voltage), which is 20A/V.

$$f_P=\frac{2}{2\pi\times R_O\times C_O} \tag{12}$$

where

- C_O is output capacitor.

$$f_{ESRZ}=\frac{1}{2\pi\times R_{ESR}\times C_O} \tag{13}$$

where

- R_{ESR} is the equivalent series resistance of the output capacitor.

$$f_{RHPZ}=\frac{R_O\times(1-D)^2}{2\pi\times L} \tag{14}$$

The COMP pin is the output of the internal transconductance amplifier. 式 15 shows the small signal transfer function of compensation network.

$$Gc(S)=\frac{G_{EA}\times R_{EA}\times V_{REF}}{V_{OUT}}\times\frac{\left(1+\frac{S}{2\times\pi\times f_{COMZ}}\right)}{\left(1+\frac{S}{2\times\pi\times f_{COMP1}}\right)\left(1+\frac{S}{2\times\pi\times f_{COMP2}}\right)} \tag{15}$$

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where

- G_{EA} is the transconductance of the amplifier.
- R_{EA} is the output resistance of the amplifier.
- V_{REF} is the reference voltage at the FB pin.
- V_{OUT} is the output voltage.
- f_{COMP1}, f_{COMP2} are the frequency of the poles of the compensation network.
- f_{COMZ} is the zero's frequency of the compensation network.

The next step is to choose the loop crossover frequency, f_C. The higher frequency that the loop gain stays above zero before crossing over, the faster the loop response is. It is generally accepted that the loop gain cross over no higher than the lower of either 1/10 of the switching frequency, f_{SW}, or 1/5 of the RHPZ frequency, f_{RHPZ}.

Then set the value of R_C, C_C, and C_P (in) by following these equations.

$$R_C = \frac{2\pi \times V_{OUT} \times C_O \times f_C}{(1-D) \times V_{REF} \times G_{EA} \times K_{COMP}} \quad (16)$$

where

- f_C is the selected crossover frequency.

The value of C_C can be set by 式 17.

$$C_C = \frac{R_O \times C_O}{2R_C} \quad (17)$$

The value of C_P can be set by 式 18.

$$C_P = \frac{R_{ESR} \times C_O}{R_C} \quad (18)$$

If the calculated value of C_P is less than 10pF, it can be left open.

Designing the loop for greater than 45° of phase margin and greater than 10dB gain margin eliminates output voltage ringing during the line and load transient.

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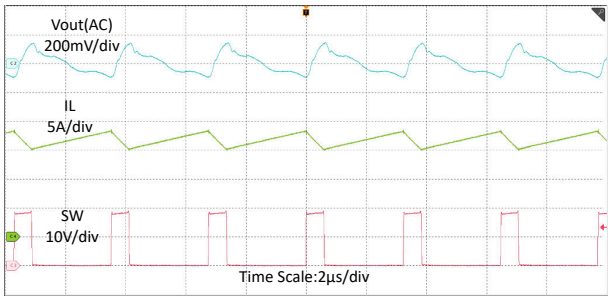
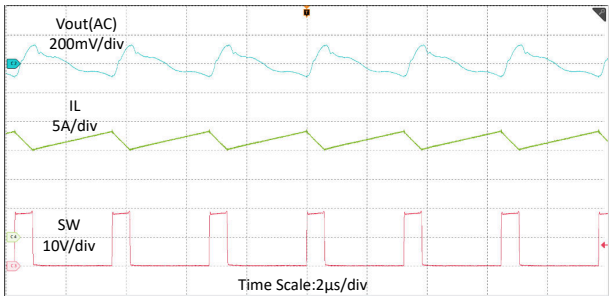
7.2.3 Application Curves



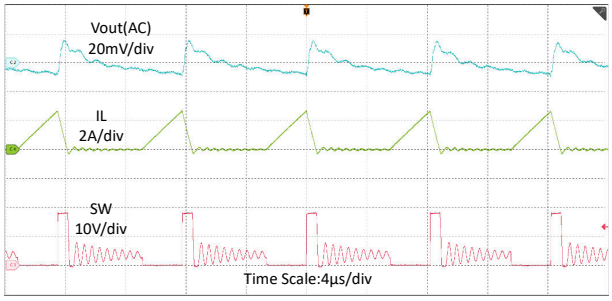
V_{IN} = 3.6V V_{OUT} = 18V I_{OUT} = 3A

図 7-2. Switching Waveforms in 3A load PFM Mode



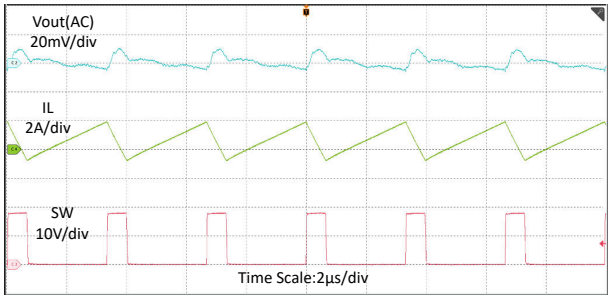
V_{IN} = 3.6V V_{OUT} = 18V I_{OUT} = 3A

図 7-3. Switching Waveforms in 3A load FPWM Mode



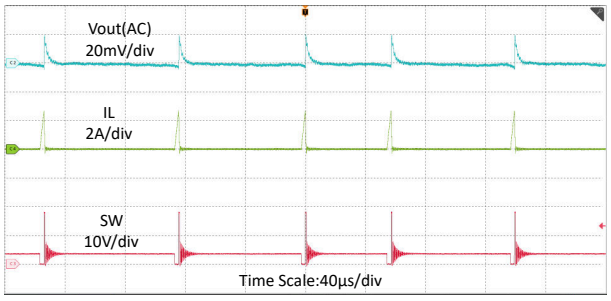
V_{IN} = 3.6V V_{OUT} = 18V I_{OUT} = 100mA

図 7-4. Switching Waveforms in 100mA load PFM Mode



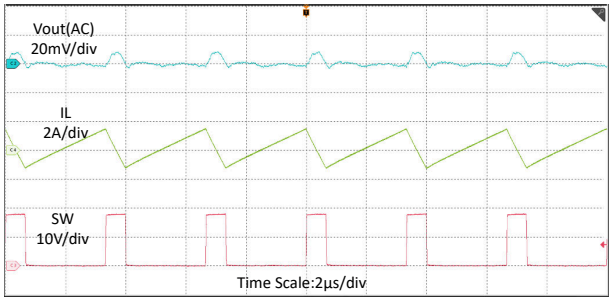
V_{IN} = 3.6V V_{OUT} = 18V I_{OUT} = 100mA

図 7-5. Switching Waveforms in 100mA load FPWM Mode



V_{IN} = 3.6V V_{OUT} = 18V I_{OUT} = 10mA

図 7-6. Switching Waveforms in 10mA load PFM Mode



V_{IN} = 3.6V V_{OUT} = 18V I_{OUT} = 10mA

図 7-7. Switching Waveforms in 10mA load FPWM Mode

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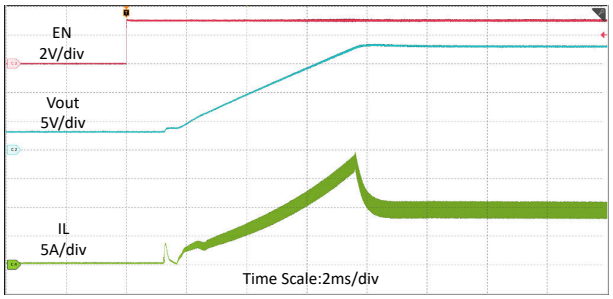
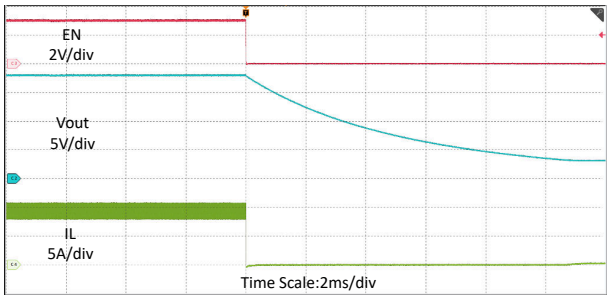


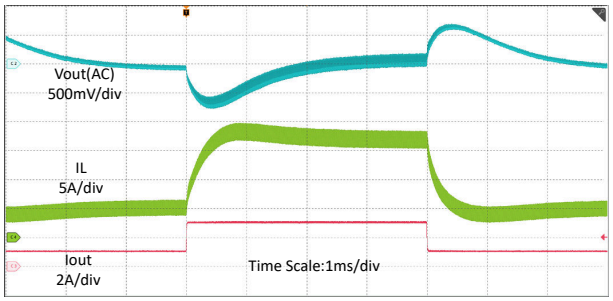
V_{IN} = 3.6V V_{OUT} = 18V R_{LOAD} = 10Ω

図 7-8. Start-up Waveforms



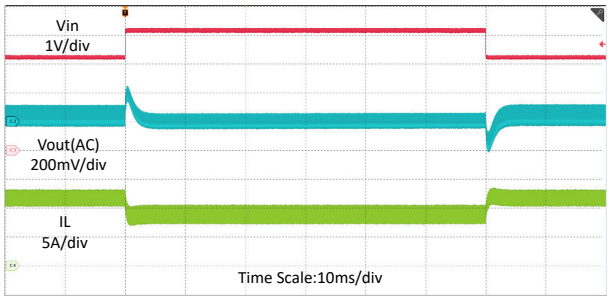
V_{IN} = 3.6V V_{OUT} = 18V R_{LOAD} = 10Ω

図 7-9. Shutdown Waveforms



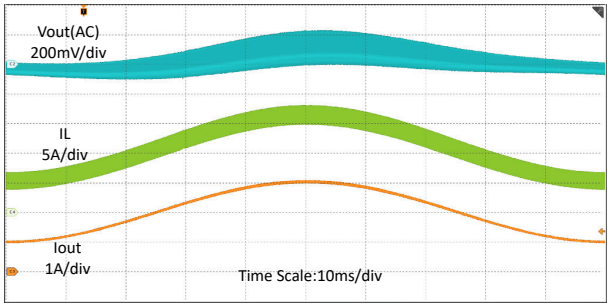
V_{IN} = 3.6V V_{OUT} = 18V

図 7-10. Load Transient (I_{OUT} = 1A to 3A)



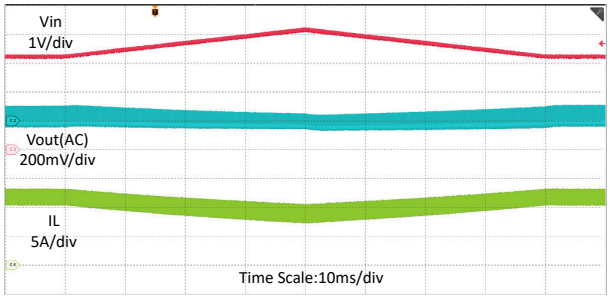
V_{OUT} = 18V I_{OUT} = 2A

図 7-11. Line Transient (V_{IN} = 3.3V to 4.2V)



V_{IN} = 3.6V V_{OUT} = 18V

図 7-12. Load Sweep (I_{OUT} = 1A to 3A)



V_{OUT} = 18V I_{OUT} = 2A

図 7-13. Line Sweep (V_{IN} = 3.3V to 4.2V)

7.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.0V to 23V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. A typical choice is an electrolytic or tantalum capacitor with a value of 47µF.

7.4 Layout

7.4.1 Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high current, layout is an important design step. If layout is not carefully done, the regulator can suffer from instability and noise problems. To maximize efficiency, switch rise and fall times are very fast. To prevent radiation of high-frequency noise (for example, EMI), proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize interplane coupling.

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The most critical current path for this converter is from the external low side MOSFET to the integrated high side MOSFET, then to the VOUT side capacitors, and back to the source of the external low side MOSFET. This current path contains nanosecond rise and fall times and must be kept as short as possible to reduce the parasitic inductance. Therefore, the VOUT side output capacitors must be close not only to the VOUT pin, but also to the source pin of the external low side MOSFET to reduce the spike at the SW pin and the VOUT pin.

The PGND plane and the AGND plane are connected at the terminal of the VCC capacitor. Thus the noise caused by the MOSFET driver and parasitic inductance does not interfere with the AGND and internal control circuit.

The layout should also be done with well consideration of the thermal as this is a high power density device. The SW, VOUT, and PGND pins that improves the thermal capabilities of the package should be soldered with the large polygon, using thermal vias underneath the SW pin could improve thermal performance.

7.4.2 Layout Example

The bottom layer is a large ground plane connected to the PGND plane and AGND plane on top layer by vias.

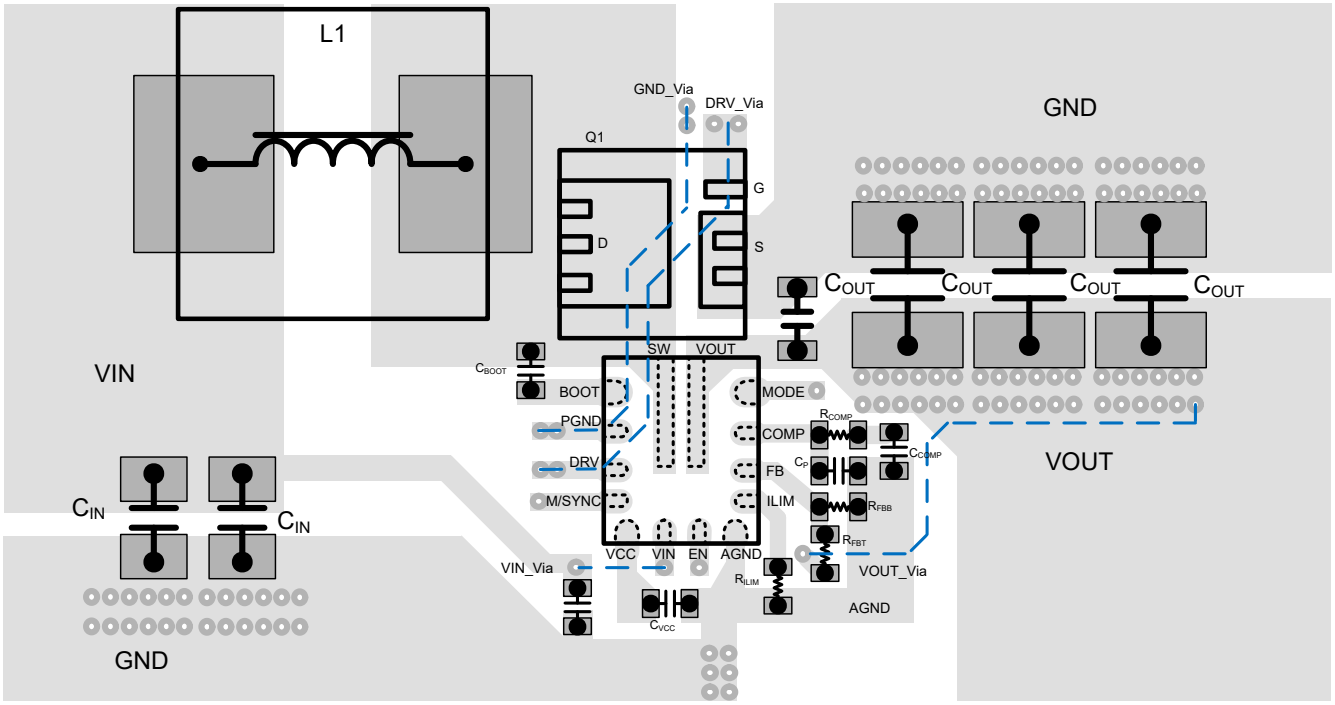

図 7-14. Layout Example

7.4.2.1 Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using:

$$P_{D(max)} = \frac{125 - T_A}{R_{\theta JA}} \tag{19}$$

where

- T_A is the maximum ambient temperature for the application.
- $R_{\theta JA}$ is the junction-to-ambient thermal resistance given in the セクション 5.4 table.

The TPS61287 comes in a thermally-enhanced VQFN package. The real junction-to-ambient thermal resistance of the package greatly depends on the PCB type, layout, and thermal pad connection. Using thick PCB copper and soldering the thermal pad to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

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8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 サポート・リソース

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8.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (October 2024) to Revision A (November 2024)	Page
• ステータスを「事前情報」から「量産データ」に変更	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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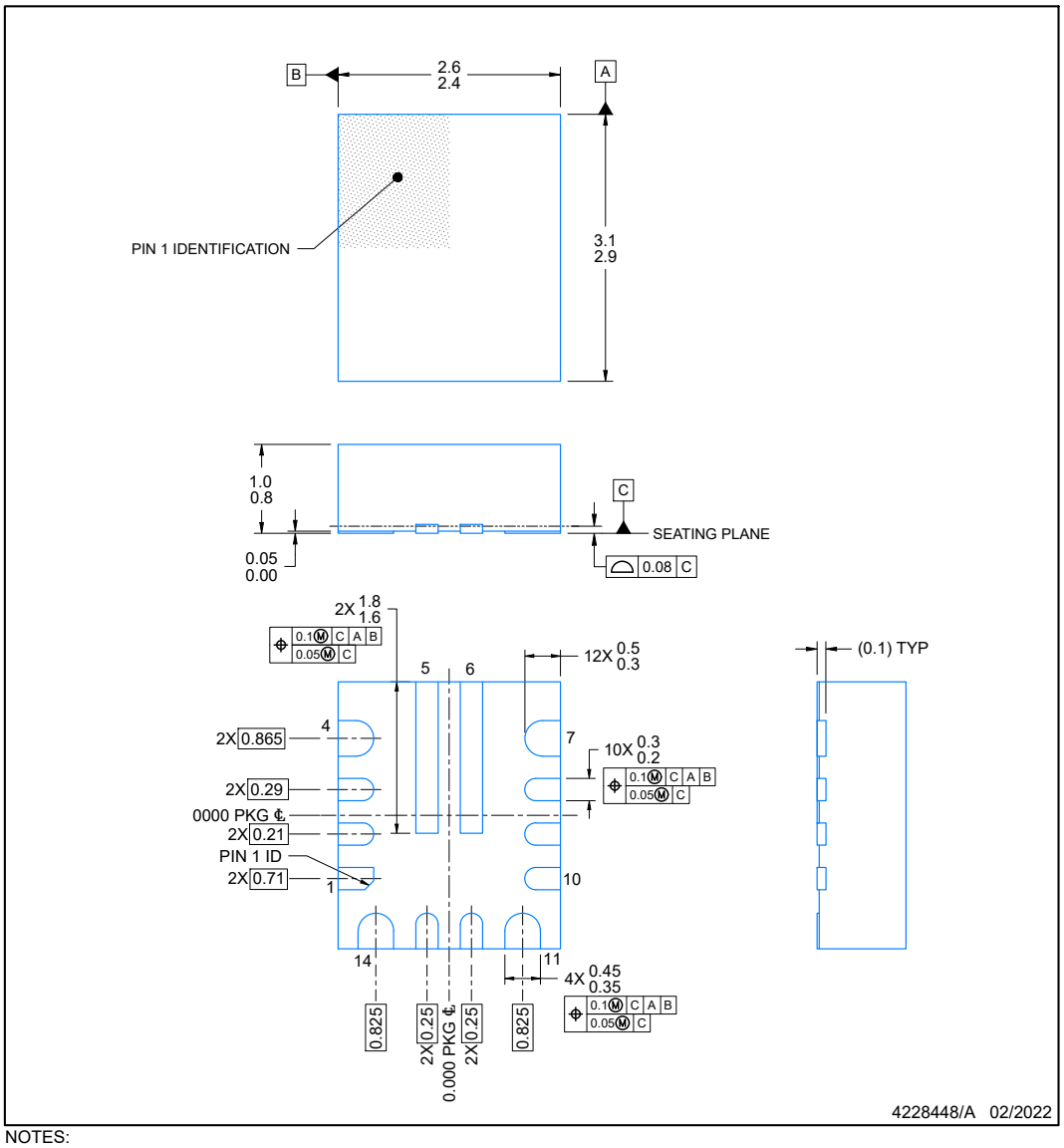
PACKAGE OUTLINE

RZP0014A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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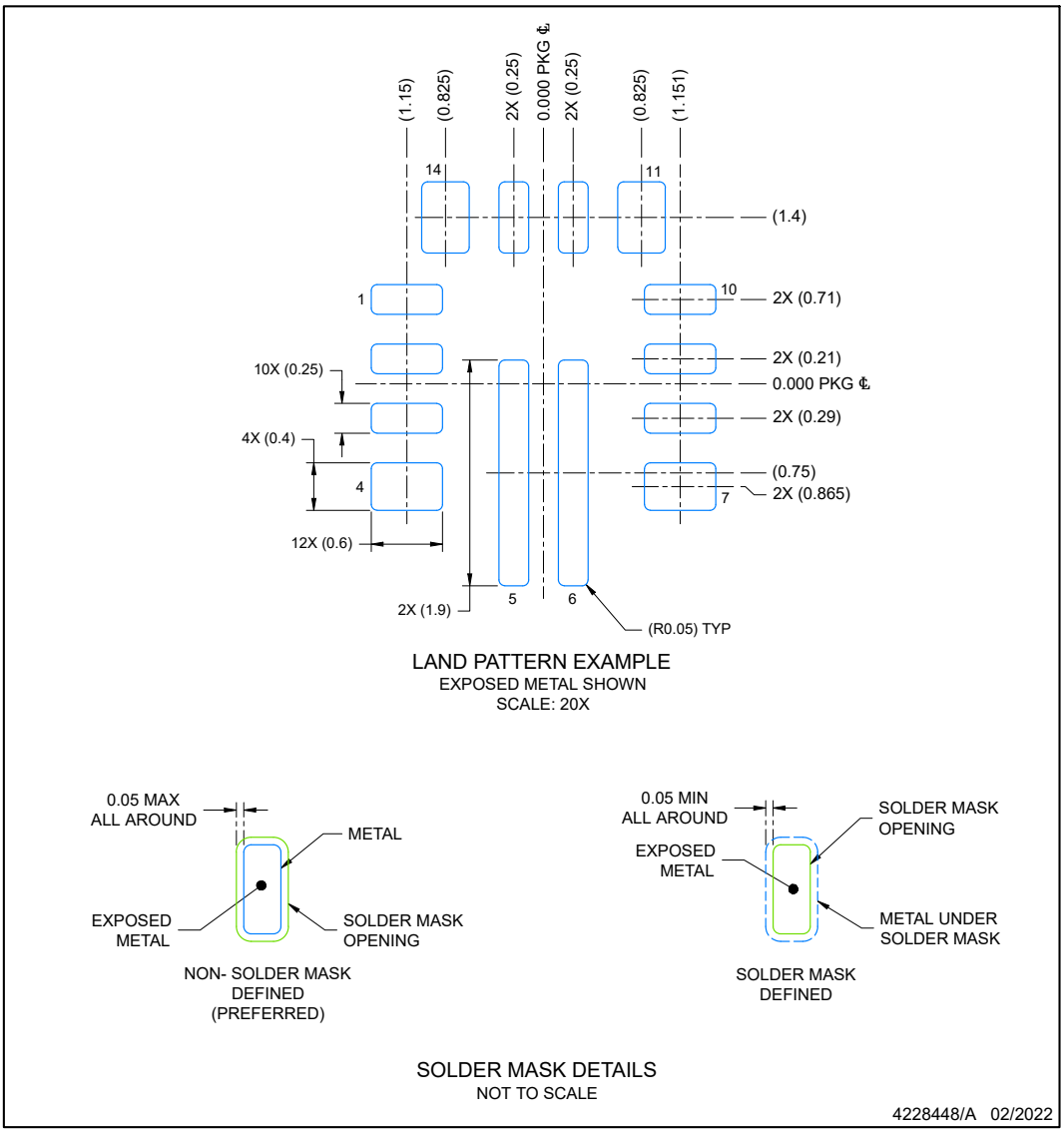
EXAMPLE BOARD LAYOUT

RZP0014A — **VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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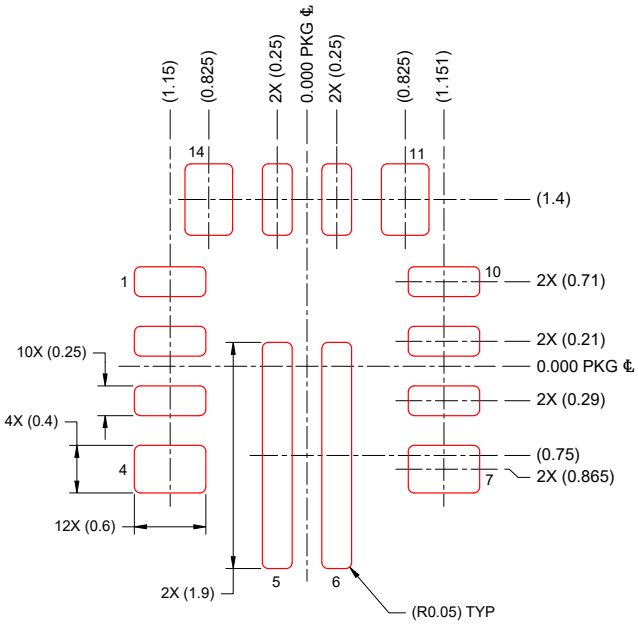
EXAMPLE STENCIL DESIGN

RZP0014A — **VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 20X

4228448/A 02/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61287RZPR	ACTIVE	VQFN-HR	RZP	14	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	61287	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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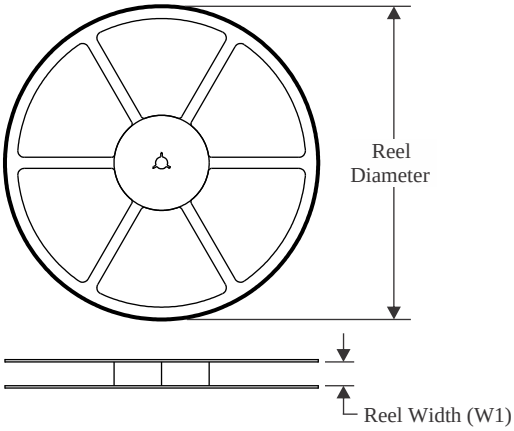
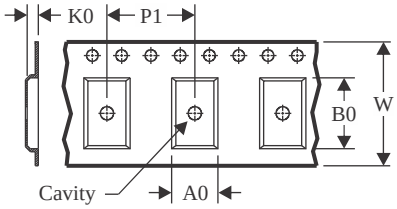
TAPE AND REEL INFORMATION

REEL DIMENSIONS

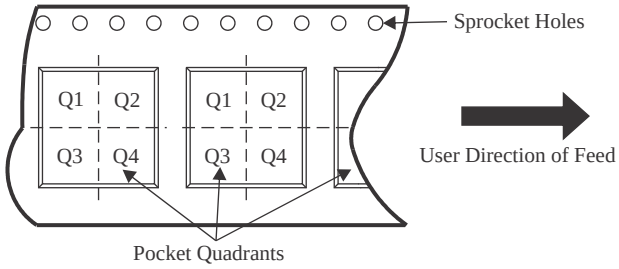


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

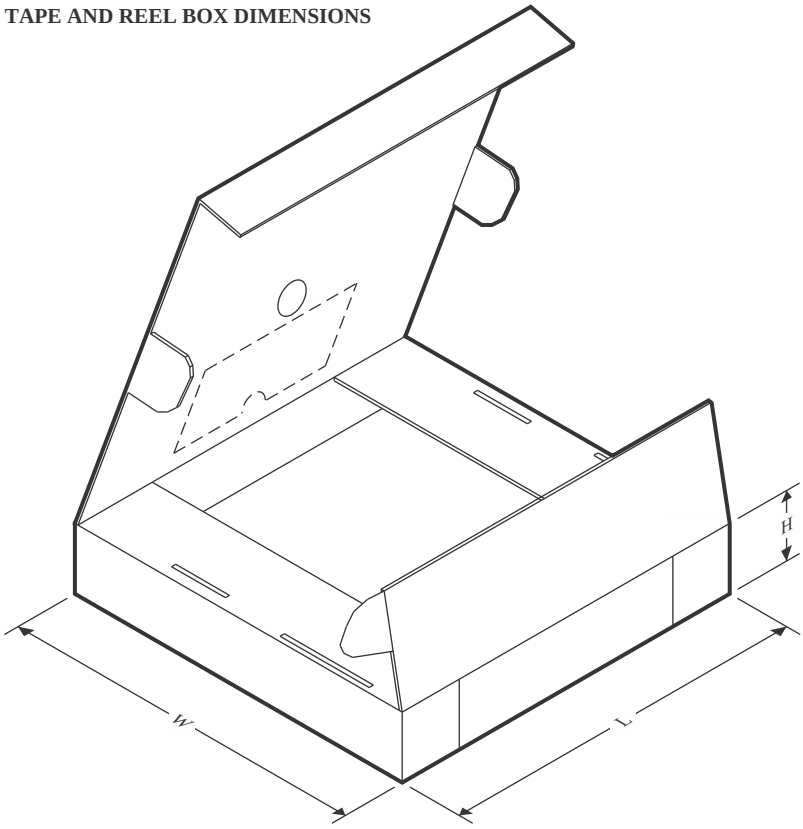
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61287RZPR	VQFN-HR	RZP	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

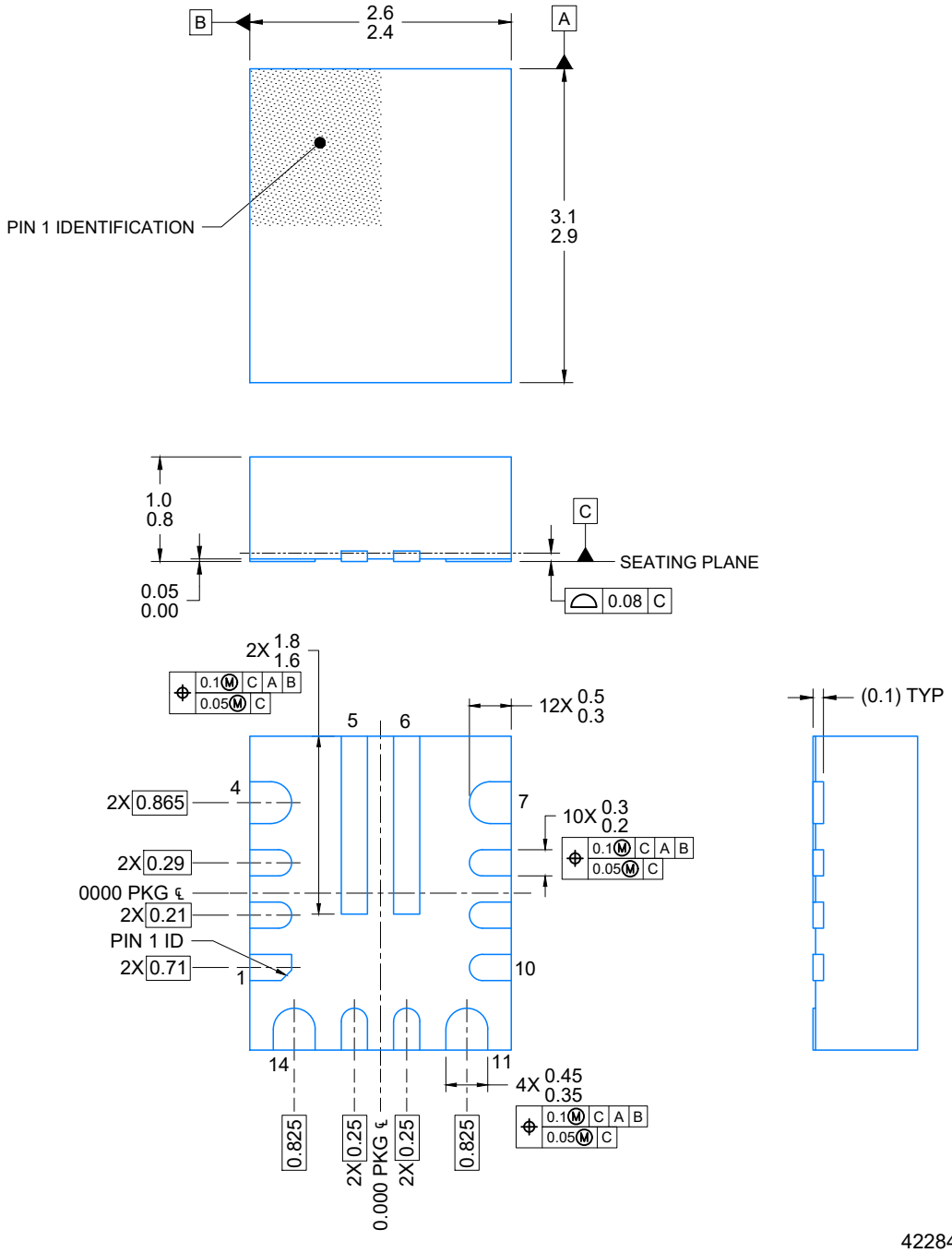
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61287RZPR	VQFN-HR	RZP	14	3000	210.0	185.0	35.0

PACKAGE OUTLINE

RZP0014A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES:

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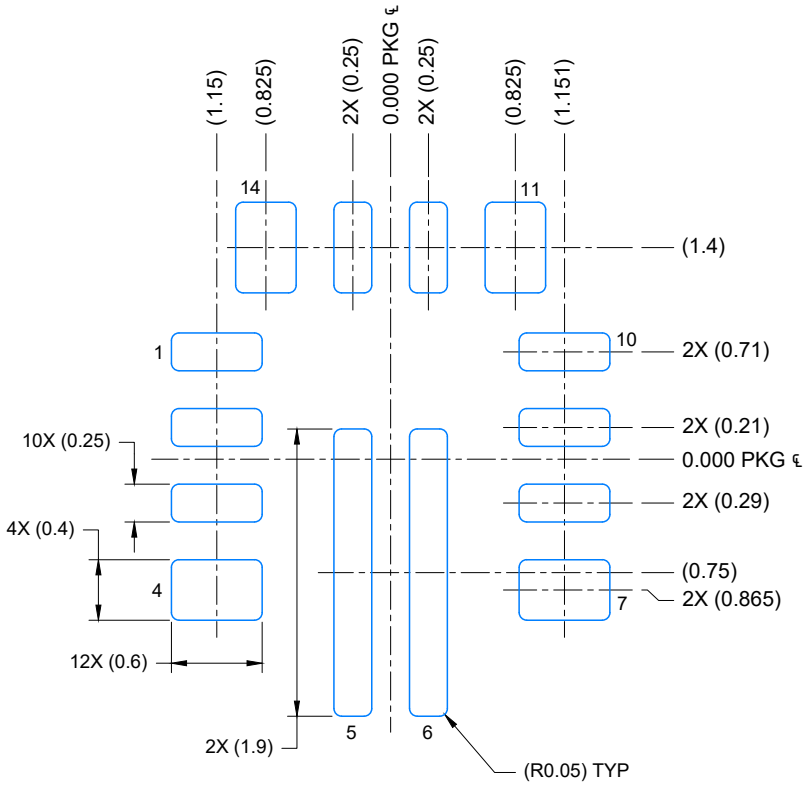
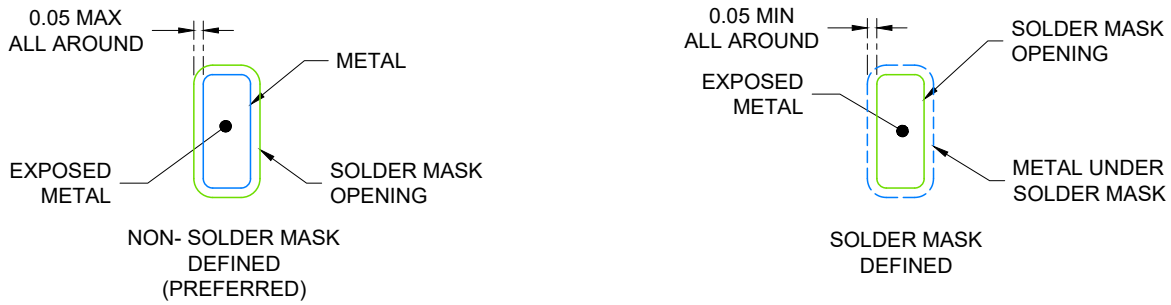


LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 20X



SOLDER MASK DETAILS

NOT TO SCALE

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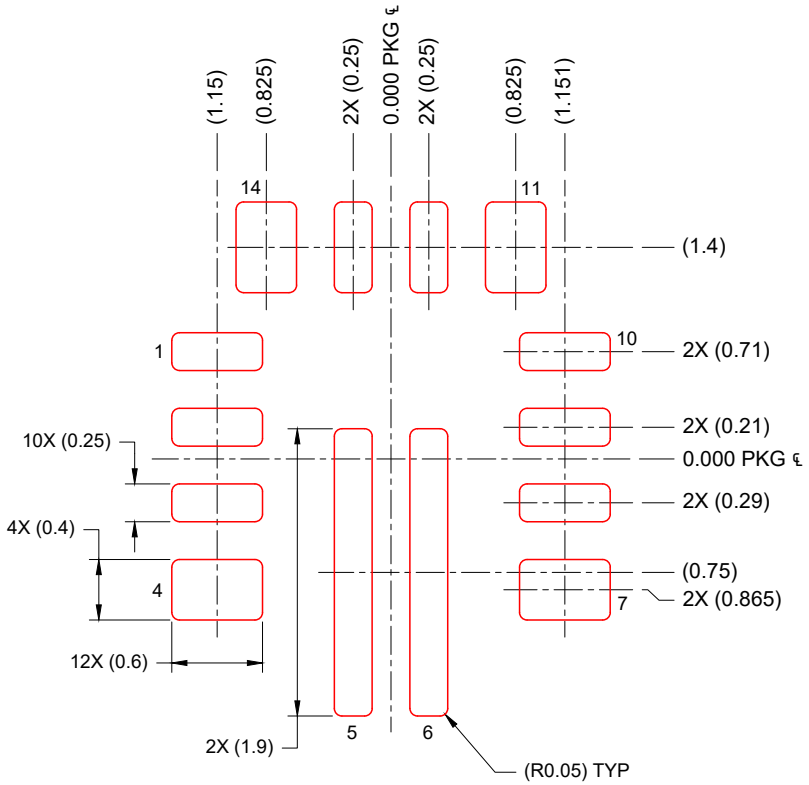
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 20X

4228448/A 02/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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