TPS61377 プログラム可能なピーク電流制限機能搭載、23V_{IN}、25V_{OUT}、6A、同期整流式昇圧コンバータ

1 特長

- 広い入出力電圧範囲
  - 入力電圧範囲：2.9V～23V
  - 出力電圧範囲：4.5V～25V
- 1.5A～6A の範囲でプログラム可能なピーク電流制限
- スイッチング周波数
  - TPS61377: 650kHz
  - TPS613771: 1.2MHz
- 高効率性と電力供給能力
  - 6A のピーク・スイッチング電流制限
  - ローサイド FET：50mΩ、ハイサイド FET：40mΩ
  - V_{IN} = 9V、V_{OUT} = 16V、I_{OUT} = 2.0A で最大 95.3% の効率
  - V_{IN} = 12V、V_{OUT} = 24V、I_{OUT} = 1.5A で最大 96.0% の効率
- システム動作時間を延長
  - 静止電流：70μA (標準値)
  - シャットダウン電流：1.25μA (最大値)
  - 自動 PFM モードと強制 PWM モードから選択可能
- 安全で堅牢な動作を実現する機能
  - 出力過電圧保護
  - サイクル単位の過電流保護
  - サーマル・シャットダウン
- 高精度 EN/UVLO スレッショルド
- 外部ループ補償
- 2.5mm × 2.0mm の HotRod™ Lite VQFN パッケージ

2 アプリケーション

- 3.3V_{IN}、5V_{IN}～12V_{OUT}、24V_{OUT} の電力変換
- 産業用電源システム
- 電化製品

3 概要

TPS61377 は、ローサイドの 50mΩ のパワー・スイッチとハイサイドの 40mΩ の整流器スイッチが搭載された、高効率で小型のソリューションを実現する、高電圧の同期整流式昇圧コンバータです。TPS61377 は、入力電圧範囲が 2.9V～23V と広く、出力電圧は最大 25V に対応し、6A のスイッチング電流能力を備えています。

TPS61377 は、適応型の定オフ時間ピーク電流の制御トポロジを使用して、出力電圧をレギュレートします。TPS61377 は、中負荷～重負荷時には、パルス幅変調 (PWM) モードで動作します。一方、軽負荷時に対しては、MODE ピンにより選択できる 2 つの動作モードを備えています。1 つは、軽負荷時の効率向上のためのパルス周波数変調 (PFM) モードです。もう 1 つは、低いスイッチング周波数によって生じる、可聴ノイズなどのアプリケーションの問題を回避する強制 PWM モードです。

TPS61377 は、ソフトスタート機能、およびプログラム可能なピーク・スイッチング電流制限機能を実装しています。また、TPS61377 は、出力過電圧保護、サイクルごとの過電流保護、およびサーマル・シャットダウン保護も備えています。

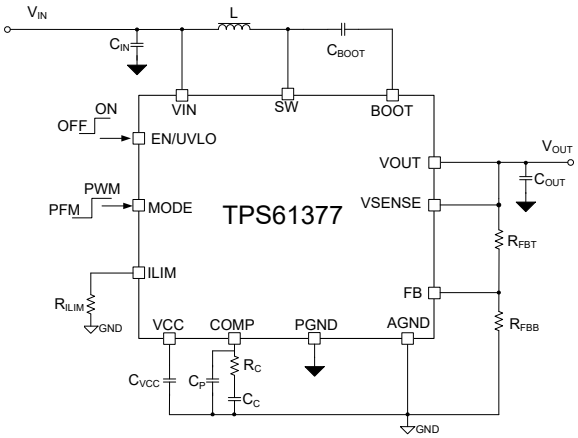
TPS61377 は、2.5mm × 2.0mm の HotRod™ Lite VQFN パッケージで供給され、超小型のソリューション・サイズを実現します。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TPS61377	VQFN (13)	2.5mm × 2.0mm
TPS613771	VQFN (13)	2.5mm × 2.0mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

このリソースの元の言語は英語です。 翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。 実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。



代表的なアプリケーション回路

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4 Device Comparison Table

PART NUMBER	FREQUENCY
TPS61377	650 kHz
TPS613771	1.2 MHz

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5 Pin Configuration and Functions

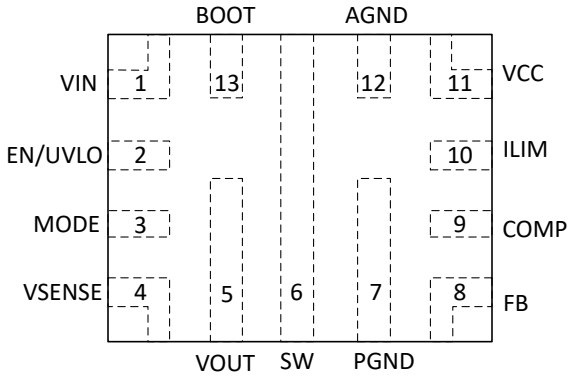

図 5-1. 13-Pin RYH VQFN Package (Top View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
VIN	1	I	IC power supply input
EN/UVLO	2	I	Enable logic input and programmable input voltage undervoltage lockout (UVLO) input. Logic high level enables the device. Logic low level disables the device and turns it into shutdown mode. The converter start-up and shutdown levels can be programmed by connecting this pin to the supply voltage through a resistor divider. This pin must not be left floating and must be terminated.
MODE	3	I	Operating mode selection pin for the device in light load condition. When this pin is logic low, the device operates in auto PFM mode. When this pin is logic high, the device operates in forced PWM mode.
VSENSE	4	I	Output voltage sense
VOUT	5	PWR	Boost converter output
SW	6	PWR	The switching node pin of the converter. It is connected to the drain of the internal low-side power MOSFET and the source of the internal high-side power MOSFET.
PGND	7	PWR	Power ground of the IC
FB	8	I	Output voltage feedback pin. Connect to the center tap of a resistor divider to program the output voltage.
COMP	9	O	Output of the internal error amplifier. Connect the loop compensation network between this pin and the AGND pin.
ILIM	10	I	Programmable switch peak current limit. An external resistor must be connected between this pin and the AGND pin.
VCC	11	O	Output of the internal regulator. A ceramic capacitor of more than 1 µF is required between this pin and AGND.
AGND	12	PWR	Analog ground of the IC
BOOT	13	O	Power supply for high side MOSFET gate driver. A ceramic capacitor of 0.47 µF to 1 µF must be connected between this pin and the SW pin.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range at terminals (2)	VIN, EN/UVLO	–0.3	25	V
	SW, VOUT, VSENSE	–0.3	30	V
	BOOT	–0.3	SW + 6	V
	MODE, FB, ILIM, VCC, COMP	–0.3	6	V
T_J (3)	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal.
(3) High junction temperatures degrade operating lifetime. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ (1)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	±750	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.9		23	V
V_{OUT}	Output voltage	4.5		25	V
L	Inductance, effective value	2.2	4.7	10	µH
C_I	Input capacitance, effective value		10		µF
C_O	Output capacitance, effective value	10		2000	µF
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS61377 VQFN 13 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W

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THERMAL METRIC(1)		TPS61377 VQFN 13 PINS	UNIT
ψ_{JB}	Junction-to-board characterization parameter	15.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_J = –40 to 125°C, L = 4.7 µH, V_{IN} = 5 V and V_{OUT} = 12 V. Typical values are at T_J = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		2.9		23	V
V_{IN_UVLO}	VIN under voltage lockout threshold	V_{IN} rising		2.8	2.9	V
V_{IN_UVLO}		V_{IN} falling		2.6	2.7	V
V_{IN_HYS}	VIN UVLO hysteresis			200		mV
I_Q	Quiescent current into V_{OUT} pin	IC enabled, no load, no switching V_{IN} =2.9V to 5.25V, V_{OUT} = 25 V, V_{FB} = V_{REF} + 0.1 V		70	100	µA
I_Q	Quiescent current into V_{OUT} pin	IC enabled, no load, no switching V_{IN} = 5.5 V to 23 V, V_{OUT} = 25 V, V_{FB} = V_{REF} + 0.1 V		2	8	µA
I_Q	Quiescent current into V_{IN} pin	IC enabled, no load, no switching V_{IN} =2.9V to 5.25V, V_{FB} = V_{REF} + 0.1 V		1.5	2	µA
I_Q	Quiescent current into V_{IN} pin	IC enabled, no load, no switching V_{IN} = 5.5 V to 23 V, V_{FB} = V_{REF} + 0.1 V		70	100	µA
V_{CC_UVLO}	VCC UVLO threshold	V_{CC} rising		2.75		V
V_{CC_HYS}	VCC UVLO hysteresis	V_{CC} hysteresis		160		mV
V_{CC}	VCC regulation	I_{VCC} = 4 mA, V_{OUT} = 12 V		4.80		V
I_{SD}	Shutdown current into V_{IN} pin	IC disabled, V_{IN} = 2.9 V to 23 V, EN = GND			1.25	µA
I_{SW_LKG}	Leakage current into SW	IC disabled, VOUT = 0 V, SW = 25 V,T_J up to 85°C			2	uA
I_{VOUT_LKG}	Leakage current into VOUT	IC disabled, VOUT = 25 V, SW = 0 V,T_J up to 85°C			2	µA
I_{FB_LKG}	Leakage current into FB	IC disabled, T_J up to 85°C			16	nA
OUTPUT VOLTAGE						
V_{OVP}	Output over-voltage protection threshold	V_{IN} = 3.3 V, V_{OUT} rising	26.5	27.5	28.6	V
V_{OVP_HYS}	Output over-voltage protection hysteresis	V_{IN} = 3.3 V, OVP threshold		0.9		V
VOLTAGE REFERENCE						
V_{REF}	Reference Voltage at FB pin	T_J = –40 to 125°C	0.985	1	1.015	V
POWER SWITCH						
$R_{DS(on)}$	Low-side MOSFET on resistance	V_{CC} = 4.85 V		50		mΩ
$R_{DS(on)}$	High-side MOSFET on resistance	V_{CC} = 4.85 V		40		mΩ
CURRENT LIMIT						
I_{LIM_SW}	Peak switching current limit FPWM	R_{LIM} = 14.4 kΩ	5.0	6.0	7.0	A
I_{LIM_SW}	Peak switching current limit Auto PFM	R_{LIM} = 14.4 kΩ	5.0	6.0	7.0	A
I_{LIM_SW}	Peak switching current limit FPWM	R_{LIM} = 57.6 kΩ	1.3	1.5	1.7	A
I_{LIM_SW}	Peak switching current limit Auto PFM	R_{LIM} = 57.6 kΩ	1.3	1.5	1.7	A
SWITCHING FREQUENCY						
Fsw	TPS61377 Switching frequency	V_{IN}=2.9V to 23V, V_{OUT} = 4.5V to 25V	500	650	800	kHz
Fsw	TPS613771 Switching frequency	V_{IN}=2.9V to 23V, V_{OUT} = 4.5V to 25V	1000	1200	1400	kHz
T_{SS}	Soft-start time			4		ms
t_{OFF_min}	Minimum off time			120		ns
t_{ON_min}	Minimum on time			75		ns

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T_J = –40 to 125°C, L = 4.7 µH, V_{IN} = 5 V and V_{OUT} = 12 V. Typical values are at T_J = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ERROR AMPLIFIER						
I_{SINK}	COMP pin sink current			20		uA
I_{SOURCE}	COMP pin source current			20		uA
V_{CCLPH}	COMP pin high clamp voltage			1.78		V
V_{CCLPL}	COMP pin low clamp voltage			0.55		V
G_{mEA}	Error amplifier trans conductance			240		uS
LOGIC INTERFACE						
V_{EN_H}	EN Logic high threshold				0.812	V
V_{EN_L}	EN Logic low threshold		0.36			V
V_{EN_L}	EN threshold hysteresis			120		mV
V_{UVLO}	UVLO rising threshold		0.788	0.813	0.835	V
I_{UVLO_HYS}	Sourcing current at the EN/UVLO pin		1.75	2	2.25	µA
V_{MODE_H}	MODE pins Logic high threshold				0.84	V
V_{MODE_L}	MODE pins Logic Low threshold		0.36			V
R_{DOWN}	MODE pins internal pull down resistor			800		kΩ
THERMAL SHUTDOWN						
t_{SD_R}	Thermal shutdown rising threshold	T_J rising		150		°C
t_{SD_F}	Thermal shutdown falling threshold	T_J falling		130		°C

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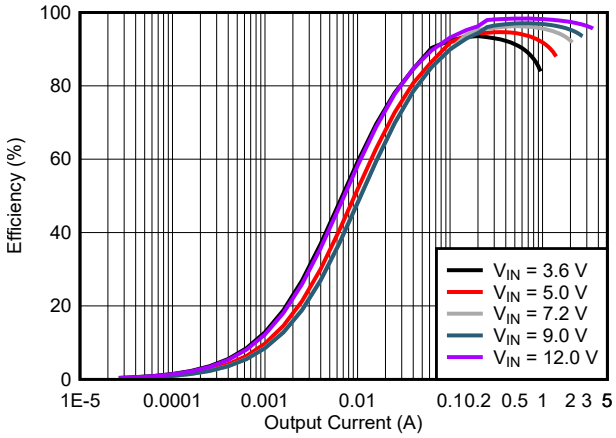
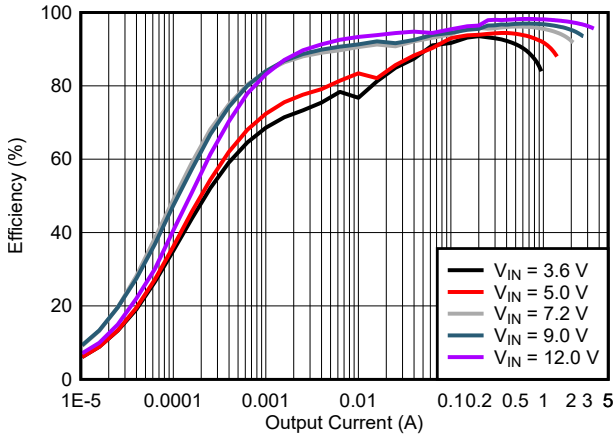
6.6 Typical Characteristics

TPS61377 Fsw= 650 kHz, T_A = 25°C, unless otherwise noted.



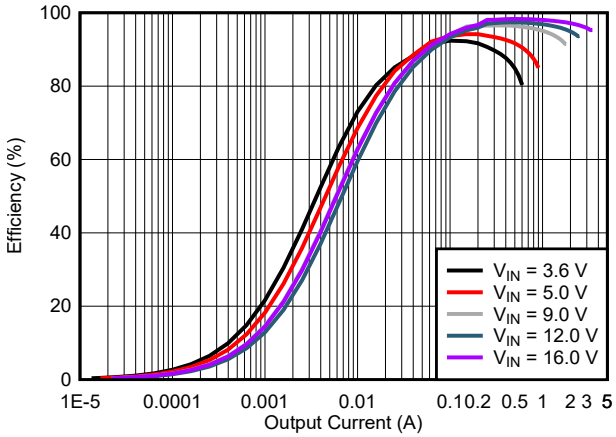
L = 4.7 µH V_{OUT} = 16 V FPWM Mode

図 6-1. Efficiency vs Output Current, V_{OUT} = 16 V



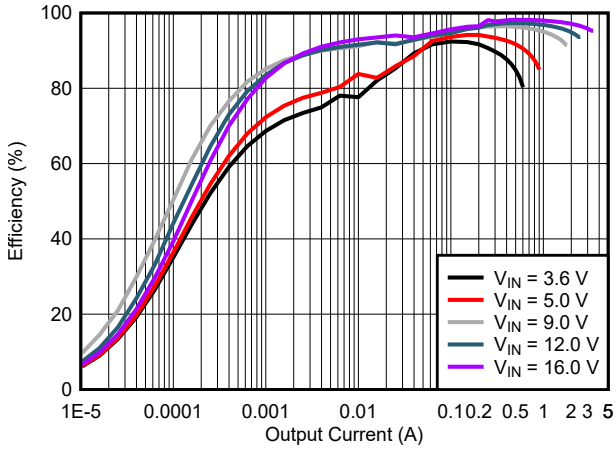
L = 4.7 µH V_{OUT} = 16 V PFM Mode

図 6-2. Efficiency vs Output Current, V_{OUT} = 16 V



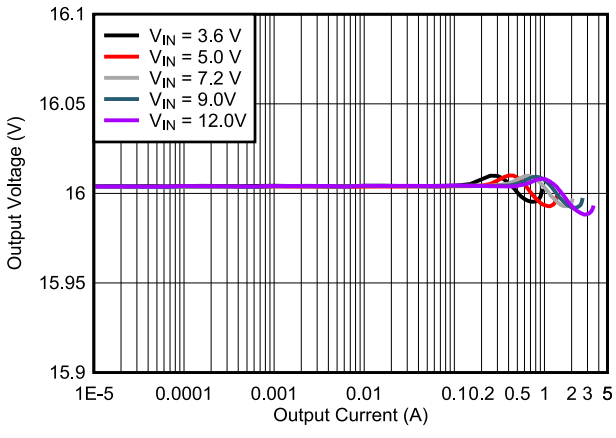
L = 10 µH V_{OUT} = 24 V FPWM Mode

図 6-3. Efficiency vs Output Current, V_{OUT} = 24 V



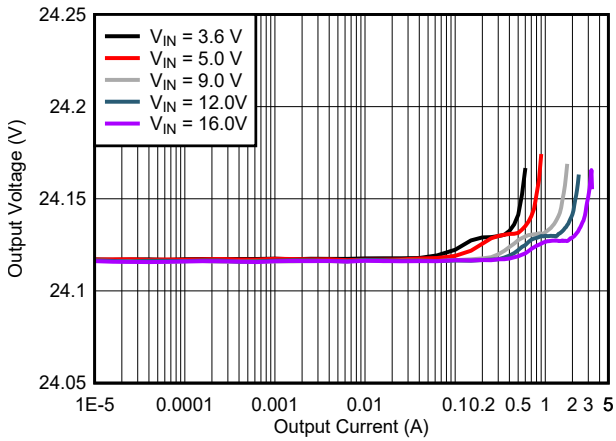
L = 10 µH V_{OUT} = 24 V PFM Mode

図 6-4. Efficiency vs Output Current, V_{OUT} = 24 V



L = 4.7 µH V_{OUT} = 16 V FPWM Mode

図 6-5. Load regulation, V_{OUT} = 16 V



L = 10 µH V_{OUT} = 24 V FPWM Mode

図 6-6. Load regulation, V_{OUT} = 24 V

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6.6 Typical Characteristics (continued)

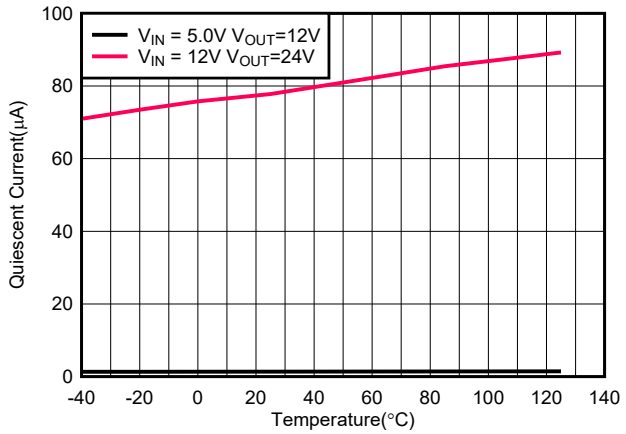

図 6-7. Quiescent Current into VIN vs Temperature

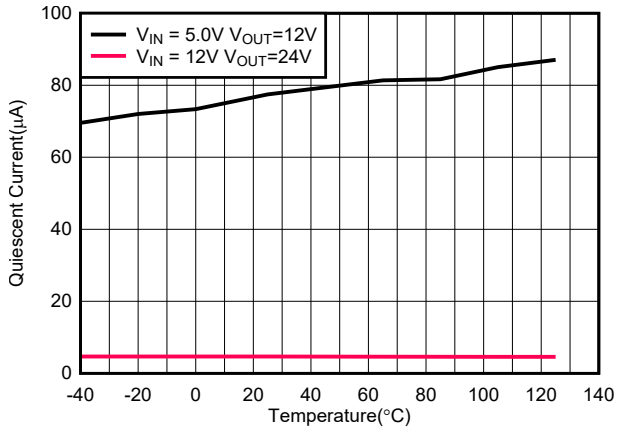

図 6-8. Quiescent Current into VOUT vs Temperature

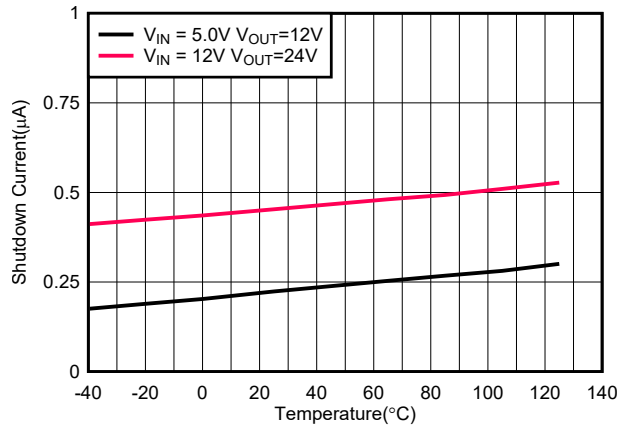

図 6-9. Shutdown Current vs Temperature

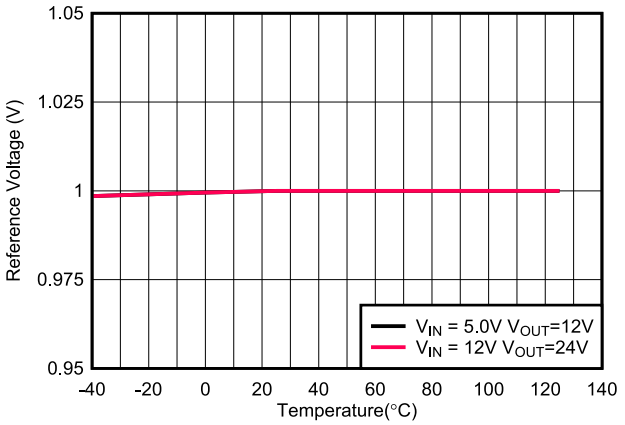

図 6-10. Reference Voltage vs Temperature

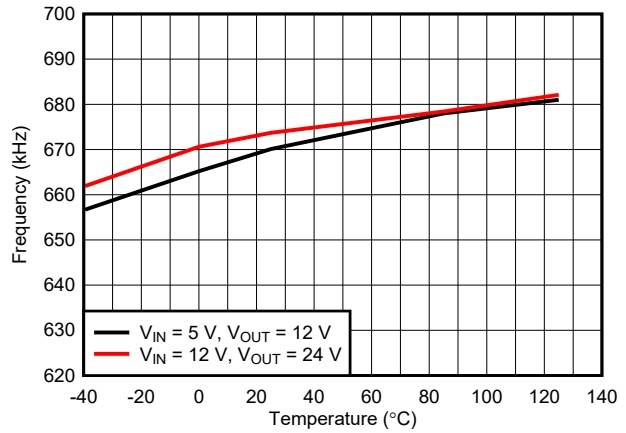

図 6-11. TPS61377 Switching Frequency vs Temperature

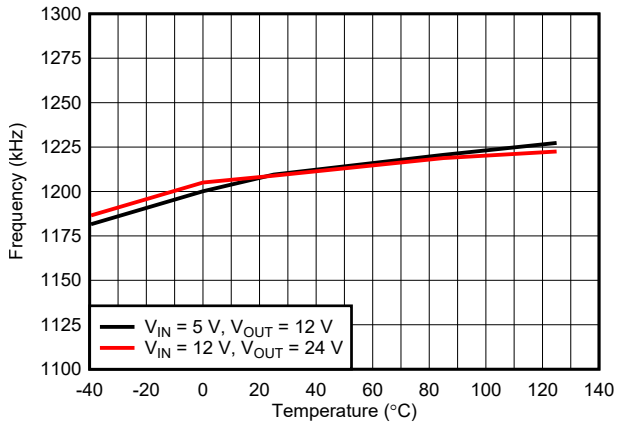

図 6-12. TPS613771 Switching Frequency vs Temperature

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7 Detailed Description

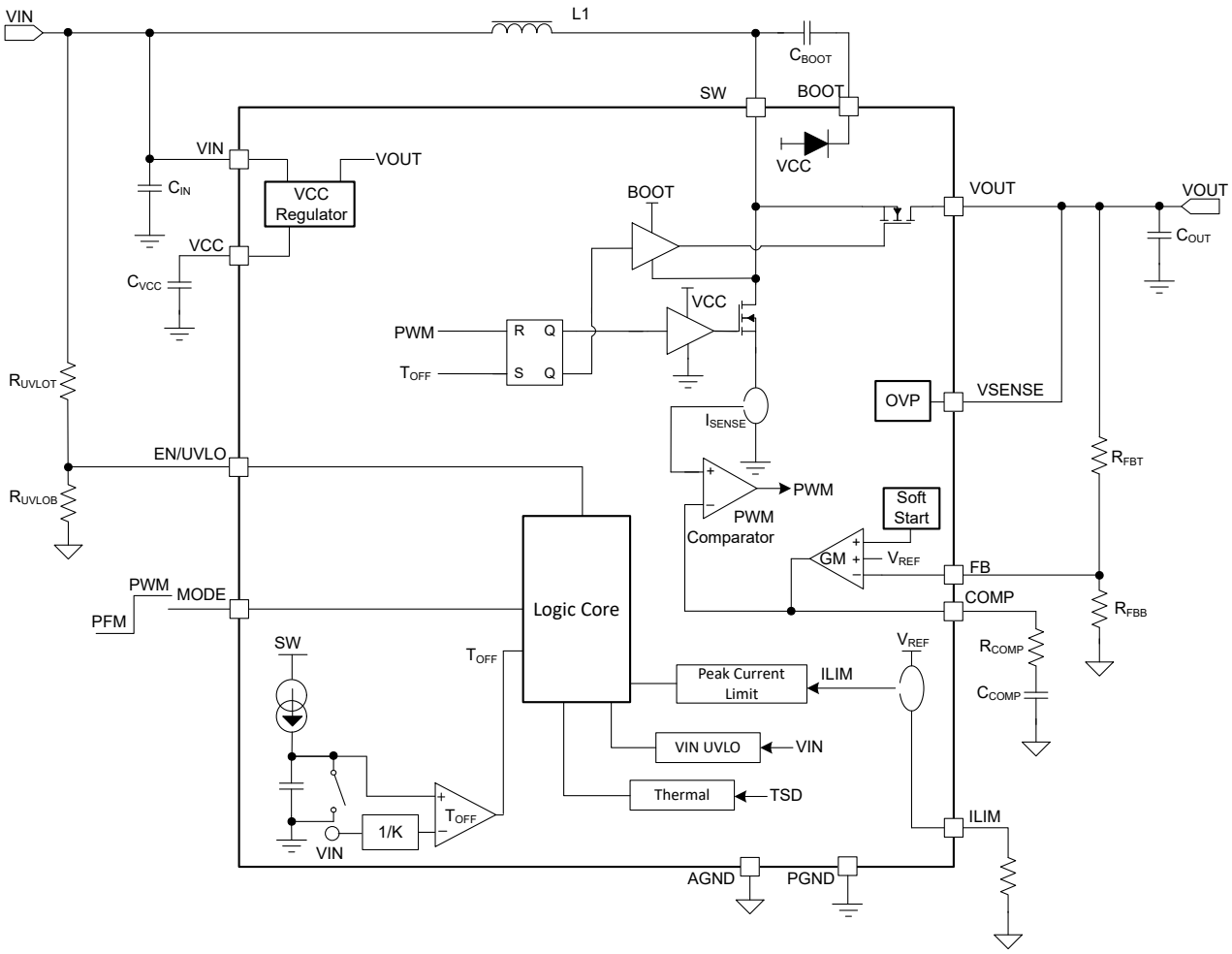
7.1 Overview

The TPS61377 is a fully-integrated high voltage synchronous boost converter with a low side 50 mΩ power switch and a 40 mΩ high side rectifier switch to provide a high efficiency and small size solution. The TPS61377 has a wide input voltage range of 2.9 V to 23 V, and can delivery up to 25 V output voltage with a peak switching current of typical 6 A. The peak switching current is programmable by a resistor connected between the ILIM pin and GND.

The TPS61377 uses the adaptive constant off-time peak current control topology to regulate the output voltage. Under moderate to heavy load condition, the TPS61377 operates in pulse width modulation (PWM) mode. As with conventional adaptive off-time converters, the device varies the off-time as a function of input and output voltage to maintain a near constant frequency. At light load, the device has two operating modes that can be selected via the MODE pin. When the MODE pin is low, the device operates in pulse frequency modulation (PFM) mode to improve light load efficiency. The off-time is modulated by the feedback loop and is extended as the load becoms lighter. When the MODE pin is high, the device operates in forced PWM mode to avoid audible noise and other application problems caused by low switching frequency. The TPS61377 uses external loop compensation, giving the flexibility to use different inductors and output capacitors.

The TPS61377 implements a soft-start function and provides output overvoltage protection, cycle-by-cycle overcurrent protection, and thermal shutdown protection.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 VCC Power Supply

The internal LDO of TPS61377 outputs a regulated voltage of 4.8 V with 10-mA output current capability. When the input voltage at the VIN pin is below 5.25 V, the internal LDO is powered by the VOUT pin, when the input voltage at the VIN pin is above 5.5 V, the internal LDO is powered by the VIN pin. A ceramic capacitor is connected between the VCC pin and AGND pin to stabilize the VCC voltage and also decouples the noise on the VCC pin. The value of this ceramic capacitor should be above 1 µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating higher than 10 V is recommended.

7.3.2 Enable and Programmable UVLO

The TPS61377 has a dual function enable and UVLO circuit. When the input voltage at the VIN pin is above the input UVLO rising threshold of 2.8 V typical and the EN/UVLO pin is pulled above the rising threshold, the TPS61377 is enabled and starts switching. The EN/UVLO pin has an accurate UVLO voltage threshold to support programmable input under-voltage lockout with hysteresis. A hysteresis current I_{UVLO_HYS} is sourced out of the EN/UVLO pin to provide hysteresis that prevents on/off chattering in the presence of input voltage noise. By using resistor divider as shown in 図 7-1 , the turn on threshold can be calculated by using 式 1.

$$V_{IN(UVLO\_ON)} = V_{UVLO} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

where

- V_{UVLO} is the UVLO threshold of 0.813 V at the EN/UVLO pin

The hysteresis between the UVLO turn on threshold and turn off threshold is set by the upper resistor in the EN/UVLO resistor divider and is given by 式 2

$$\Delta V_{IN(UVLO)} = I_{UVLO\_HYS} \times R1 \quad (2)$$

where

- I_{UVLO} is the sourcing current from the EN/UVLO pin when the voltage at the EN/UVLO pin is above V_{UVLO}

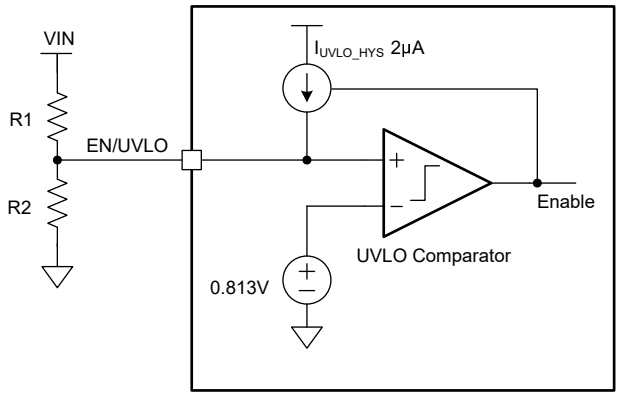


図 7-1. Programmable UVLO with Resistor Divider at EN/UVLO Pin

7.3.3 Soft Start

The TPS61377 has a 4 ms soft start function to prevent high inrush current during start-up. When the EN/UVLO pin is pulled high, the internal soft-start capacitor is charged with a constant current. During this time, the soft-start capacitor voltage is compared with the internal reference (1.0 V). The lower one is fed into the internal positive input of the error amplifier. The output of the error amplifier (which determines the inductor peak current value) ramps up slowly as the soft-start capacitor voltage goes up. The soft-start phase is completed after the soft-start capacitor voltage exceeds the internal reference , which takes 4 ms from 0 V to 1.0 V. When the EN/UVLO pin is pulled low, the voltage of the soft-start capacitor is discharged to ground.

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7.3.4 Switching Frequency

The TPS61377 uses adaptive constant off-time peak current control topology to regulate the output voltage. Under moderate to heavy load conditions, the TPS61377 operates in pulse width modulation (PWM) mode. The switching frequency in PWM mode is 650 kHz (1.2 MHz for TPS613771). At light load, the converter can either operate in PFM mode or in forced PWM mode according to the mode selected.

7.3.5 Programmable Inductor Peak Current Limit

The TPS61377 adopts a cycle-by-cycle peak switching current limit function internally. The low-side switch is turned off as soon as the switch peak current triggers the limit threshold. The peak switching current limit can be set by a resistor from the ILIM pin to ground. The relationship between the peak current limit and the resistor is shown in 式 3.

$$I_{PEAK} = 0.54V \times \frac{160k}{R_{LIM}} \quad (3)$$

where

- R_{LIM} is the resistance between the ILIM pin and the AGND pin.
- I_{PEAK} is the typical peak switching current limit.

For instance, the peak switching current is 5.4 A typical if the R_{LIM} is 16 kΩ. ILIM pin cannot be left floating or connected to VCC.

7.3.6 Shut Down

When the input voltage is below the UVLO threshold or the EN/UVLO pin is pulled low, the TPS61377 is in shutdown mode and all the functions are disabled.

7.3.7 Overvoltage Protection

If the output voltage at the VSENSE pin is detected above 27.5 V (typ), the TPS61377 stops switching immediately until the voltage at the VSENSE pin drops the hysteresis value lower than the output overvoltage protection threshold. This function prevents overvoltage on the output and secures the circuits connected to the output from excessive overvoltage.

7.3.8 Thermal Shutdown

A thermal shutdown is implemented to prevent damages due to excessive heat and power dissipation. Typically, the thermal shutdown happens at a junction temperature of 150°C. When the thermal shutdown is triggered, the device stops switching until the junction temperature falls below typically 130°C, then the device starts switching again.

7.4 Device Functional Modes

7.4.1 Operation

The TPS61377 operates at a quasi-constant frequency pulse width modulation (PWM) in moderate-to-heavy load condition. Based on the VIN to VOUT ratio, a circuit predicts the required off-time of the switching cycle. At the beginning of each switching cycle, the low-side N-MOSFET switch is turned on, and the inductor current ramps up to a peak current that is determined by the output of the internal error amplifier. After the peak current is reached, the current comparator trips. It turns off the low-side N-MOSFET switch and the inductor current goes through the body diode of the high-side N-MOSFET in a dead-time duration. After the dead-time duration, the high-side N-MOSFET switch is turned on. Since the output voltage is higher than the input voltage, the inductor current decreases. The high-side switch is not turned off until the off-time is reached. After a short dead-time duration, the low-side switch turns on again and the switching cycle is repeated. At light load, the TPS61377 implements two operating modes, PFM mode and forced PWM mode, to meet different application requirements. The operating mode is set by the status of the MODE pin. When the MODE pin is logic high, the device operates in forced PWM mode. When the MODE pin is logic low, the device operates in PFM mode.

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7.4.2 Forced PWM Mode

In forced PWM mode, the TPS61377 keeps the switching frequency unchanged at light load. When the load current decreases, the output of the internal error amplifier decreases as well to keep the inductor peak current down, delivering less power from input to output. When the output current further reduces, the current through the inductor decreases to zero during the off-time. The high-side N-MOSFET is not turned off even if the current through the MOSFET is zero. Thus, the inductor current changes its direction after it runs to zero. The power flow is from output side to input side. The efficiency is low in this mode. But with the fixed switching frequency, there is no audible noise and other problems which might be caused by low switching frequency at light load.

7.4.3 Auto PFM Mode

In auto PFM mode , the TPS61377 provides a seamless transition from PWM to PFM operation with smooth on-time/off-time (SOO) mode and enables automatic pulse-skipping mode that provides excellent efficiency over a wide load range. As load current decreasing or VIN rising, the output of the internal error amplifier decreases to lower the inductor peak current, delivering less power to the load. When the output of the error amplifier goes down and reaches a threshold of about 500-mA peak current, the output of the error amplifier is clamped at this value and does not decrease any more, the TPS61377 extends its off-time of the switching period to deliver less energy to the output and regulate the output voltage to the target.

With SOO mode, the TPS61377 keeps the output voltage equal to the setting voltage in PFM mode. In addition, the output voltage ripple is much smaller at light load due to low peak current. Refer to 図 7-2.

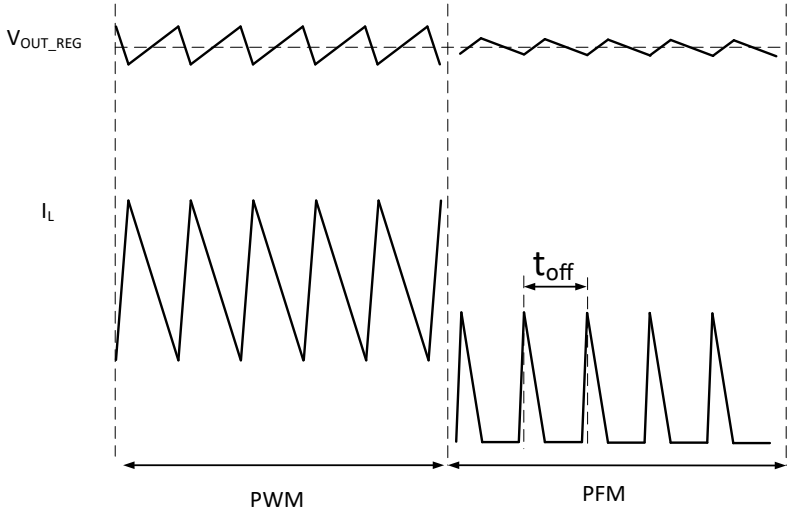

図 7-2. Auto PFM Mode Diagram

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8 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS61377 is designed for output voltages up to 25 V with a peak switching current limit of 6 A typical. The TPS61377 operates at a quasi-constant frequency pulse width modulation (PWM) under moderate to heavy load conditions. At light load, the converter can operate in either PFM mode or forced PWM mode, depending on the mode selected. The PFM mode provides high efficiency over the entire load range, while the PWM mode can avoid the acoustic noise as the switching frequency is fixed. The converter uses the adaptive constant off-time peak current control scheme, which provides excellent transient line and load response with minimal output capacitance. The TPS61377 can operate with different inductor and output capacitor combinations by adjusting the external loop compensation.

8.2 Typical Application

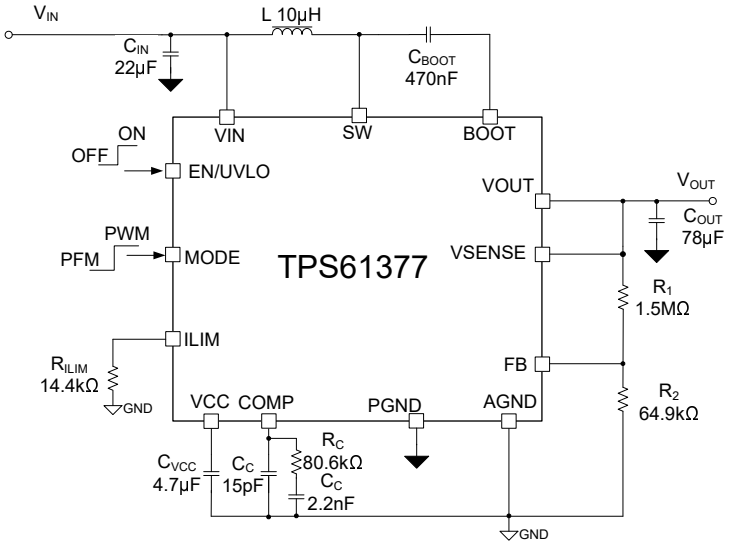

図 8-1. TPS61377 9-V to 16-V V_{IN} ;24V V_{OUT} 1.5-A Output Converter

8.2.1 Design Requirements

表 8-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	9 V to 16 V
Output voltage	24 V
Output voltage ripple	100 mV peak to peak
Output current rating	1.5 A
Operating frequency	650 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Setting Output Voltage

The output voltage is set by an external resistor divider (R1, R2 in the 図 8-1 circuit diagram). For the best accuracy, R2 should be smaller than 500 kΩ to ensure the current flowing through R2 is at least 100 times larger than the FB pin leakage current. Changing R2 to lower value increases the immunity against noise injection. Changing R2 to higher values reduces the quiescent current to achieve higher efficiency at light load.

The value of R1 is then calculated as:

$$R_1 = \frac{(V_{OUT} - V_{REF}) \times R_2}{V_{REF}} \tag{4}$$

8.2.2.2 Inductor Selection

The selection of the inductor affects the steady state of the power supply operation, transient behavior, loop stability, and boost converter efficiency, the inductor is the most important component in switching power regulator design. The three most important specifications to the performance of the inductor are the inductance value, DC resistance, and saturation current.

The TPS61377 is designed to work with inductor values between 2.2 µH and 10 µH. A 2.2 µH inductor is typically available in a smaller or lower-profile package, while a 10-µH inductor produces lower inductor current ripple. If the boost output current is limited by the peak current protection of the IC, using a inductor with bigger inductance can maximize the output current capability of the converter.

Inductance values can be ±20% or even ±30% of the value at 0 A bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A bias current, depending on how the inductor vendor defines saturation current. When selecting an inductor, make sure its rated current, especially the saturation current, is larger than boost converter peak current under all operating conditions.

Normally, it is advisable that the inductor peak-to-peak current is less than 40% of the average inductor current at maximum output current. Follow 式 5 to 式 7 to calculate the average, peak and ripple current of the inductor. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, and maximum load current of the application. To leave enough design margin, TI recommends using the minimum switching frequency, the inductance with -30% tolerance, and a low power conversion efficiency for the calculation.

In a boost regulator, calculate the inductor DC current as in 式 5.

$$I_{DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \tag{5}$$

where

- V_{OUT} is the output voltage of the boost regulator.
- I_{OUT} is the output current of the boost regulator.
- V_{IN} is the input voltage of the boost regulator.
- η is the power conversion efficiency.

Calculate the inductor current peak-to-peak ripple as in 式 6.

$$I_{PP} = \frac{1}{L \times \left(\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}}\right) \times f_{SW}} \tag{6}$$

where

- I_{PP} is the inductor peak-to-peak ripple.

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- L is the inductor value.
- f_{SW} is the switching frequency.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

Therefore, the peak current, I_{Lpeak}, seen by the inductor is calculated with 式 7.

$$I_{Lpeak} = I_{DC} + \frac{I_{PP}}{2} \tag{7}$$

It is important that the peak current does not exceed the inductor saturation current.

For a given physical inductor size, increasing inductance usually results in an inductor with lower saturation current. The total losses of the coil consists of the DC resistance (DCR) loss and the following frequency-dependent loss:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)

For a certain inductor, the larger current ripple (smaller inductor) generates the higher DC and also the frequency-dependent loss. Usually, a data sheet of an inductor does not provide the core loss information. If needed, consult the inductor vendor for detailed information. An inductor with lower DCR is basically recommended for higher efficiency. However, it is usually a tradeoff between the loss and foot print. The table below lists some recommended inductors.

表 8-2. Recommended Inductors

PART NUMBER	L (µH)	DCR TYP (mΩ)	SATURATION CURRENT (A)	SIZE (L × W × H mm)	VENDOR(1)
XGL5050-222ME	2.2	6.8	10.7	5.28 x 5.48 x 5.1	Coilcraft
XGL5050-472ME	4.7	13.9	7.0	5.28 x 5.48 x 5.1	Coilcraft
XGL6060-103ME	10	18.5	7.3	6.51 x 6.71 x 6.1	Coilcraft
XGL4020-222ME	2.2	19.5	6.2	4.0 x 4.0 x 2.1	Coilcraft
XGL4020-472ME	4.7	43	4.1	4.0 x 4.0 x 2.1	Coilcraft
XGL4020-822ME	8.2	71	3.2	4.0 x 4.0 x 2.1	Coilcraft

(1) See the *Third-party Products Disclaimer*.

8.2.2.3 Bootstrap Capacitor Selection

The bootstrap capacitor between the BOOT and SW pin supplies the gate current to charge the high-side FET device gate during the turn on of each cycle. The gate current also supplies charge for the bootstrap capacitor. The recommended value of the bootstrap capacitor is 0.47 µF to 1 µF. C_{BOOT} must be a good quality, low-ESR ceramic capacitor located at the pins of the device to minimize potentially damaging voltage transients caused by trace inductance. A value of 0.47 µF was selected for this design example.

8.2.2.4 Input Capacitor Selection

Multilayer ceramic capacitors are an excellent choice for the input decoupling of the step-up converter since they have extremely low ESR and are available in small footprints. Input capacitors must be located as close as possible to the device. While a 22-µF input capacitor or equivalent is sufficient for the most applications, larger values can be used to reduce input current ripple.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or can even damage the device. Additional "bulk" capacitor (electrolytic or tantalum) in this circumstance, must be placed

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between C_{IN} and the power source lead to reduce ringing that can occur between the inductance of the power source leads and C_{IN}.

8.2.2.5 Output Capacitor Selection

The output capacitor is mainly selected to meet the requirements at load transient or steady state. The loop is compensated for the output capacitor selected. The output ripple voltage is related to the equivalent series resistance (ESR) of the capacitor and its capacitance. Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by 式 8:

$$C_{OUT} = \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f_{SW} \times \Delta V \times V_{OUT}} \quad (8)$$

where

- C_{OUT} is the output capacitor
- I_{OUT} is the output current
- V_{OUT} is the output voltage
- V_{IN} is the input voltage
- Δ_V is the output voltage ripple required
- f_{SW} is the switching frequency

The additional output ripple component caused by ESR is calculated by 式 9:

$$\Delta V_{ESR} = I_{Lpeak} \times R_{ESR} \quad (9)$$

where

- ΔV_{ESR} is the output voltage ripple caused by ESR
- R_{ESR} is the resistor in series with the output capacitor

For the ceramic capacitor, the ESR ripple can be neglected. However, for the tantalum or electrolytic capacitors, it must be considered if used.

The minimum ceramic output capacitance needed to meet a load transient requirement can be estimated using 式 10:

$$C_{OUT} = \frac{\Delta I_{STEP}}{2\pi \times f_{BW} \times \Delta V_{TRAN}} \quad (10)$$

where

- ΔI_{STEP} is the transient load current step
- ΔV_{TRAN} is the allowed voltage dip for the load current step
- f_{BW} is the control loop bandwidth (that is, the frequency where the control loop gain crosses zero)

Take care when evaluating the derating of a ceramic capacitor under the DC bias. Ceramic capacitors can derate by as much as 70% of the capacitance at the respective rated voltage. Therefore, enough margins on the voltage rating must be considered to ensure adequate capacitance at the required output voltage.

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8.2.2.6 Loop Stability

The TPS61377 requires external compensation, which allows the loop response to be optimized for each application. The COMP pin is the output of the internal error amplifier. An external compensation network, comprised of resistor R_C, and ceramic capacitors C_C and C_P, is connected to the COMP pin.

The power stage small signal loop response of constant off-time (COT) with peak current control can be modeled by 式 11.

$$G_{PS}(S)=K_{COMP}\times\frac{R_O\times(1\text{-}D)}{2}\times\frac{\left(1+\frac{S}{2\pi f_{ESRZ}}\right)\times\left(1-\frac{S}{2\pi f_{RHPZ}}\right)}{1+\frac{S}{2\pi f_P}} \tag{11}$$

where

- D is the switching duty cycle.
- R_O is the output load resistance.
- K_{COMP} is power stage trans-conductance (inductor peak current / comp voltage), which is 6.5 A/V.

$$f_P=\frac{2}{2\pi\times R_O\times C_O} \tag{12}$$

where

- C_O is effective output capacitance.

$$f_{ESRZ}=\frac{1}{2\pi\times R_{ESR}\times C_O} \tag{13}$$

where

- R_{ESR} is the equivalent series resistance of the output capacitor.

$$f_{RHPZ}=\frac{R_O\times(1-D)^2}{2\pi\times L} \tag{14}$$

The COMP pin is the output of the internal transconductance amplifier. 式 15 shows the small signal transfer function of compensation network.

$$Gc(S)=\frac{G_{EA}\times R_{EA}\times V_{REF}}{V_{OUT}}\times\frac{\left(1+\frac{S}{2\times\pi\times f_{COMZ}}\right)}{\left(1+\frac{S}{2\times\pi\times f_{COMP1}}\right)\left(1+\frac{S}{2\times\pi\times f_{COMP2}}\right)} \tag{15}$$

where

- G_{EA} is the transconductance of the amplifier, which is 240 uS.
- R_{EA} is the output resistance of the amplifier, which is 100 MΩ.
- V_{REF} is the reference voltage at the FB pin.
- V_{OUT} is the output voltage.
- f_{COMP1}, f_{COMP2} are the frequency of the poles of the compensation network.
- f_{COMZ} is the zero's frequency of the compensation network.

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The next step is to choose the loop crossover frequency, f_C. The higher frequency that the loop gain stays above zero before crossing over, the faster the loop response is. It is generally accepted that the loop gain cross over no higher than the lower of either 1/10 of the switching frequency, f_{SW}, or 1/5 of the RHPZ frequency, f_{RHPZ}.

Then set the value of R_C, C_C, and C_P (in 図 8-1) by following these equations.

$$R_C = \frac{2\pi \times V_{OUT} \times C_O \times f_C}{(1\text{-}D) \times V_{REF} \times G_{EA} \times K_{COMP}} \quad (16)$$

where

- f_C is the selected crossover frequency.

The value of C_C can be set by 式 17.

$$C_C = \frac{R_O \times C_O}{2R_C} \quad (17)$$

The value of C_P can be set by 式 18.

$$C_P = \frac{R_{ESR} \times C_O}{R_C} \quad (18)$$

If the calculated value of C_P is less than 10 pF, it can be left open.

Designing the loop for greater than 45° of phase margin and greater than 10-dB gain margin eliminates output voltage ringing during the line and load transient.

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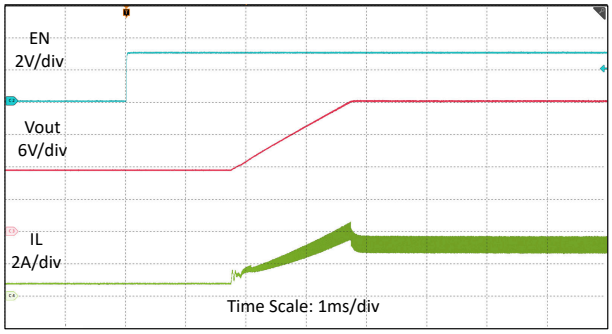
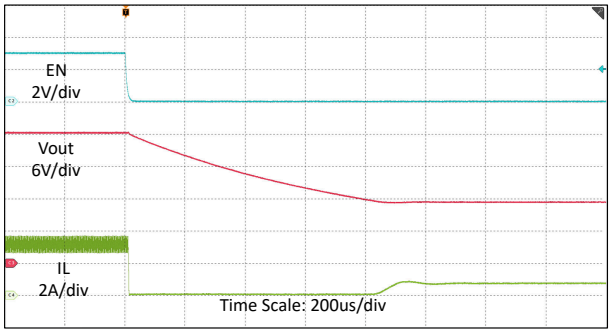
8.2.3 Application Curves

T_A = 25°C, Total C_{OUT} = 78 µF, L = 10 µH, EVM-based , unless otherwise noted.



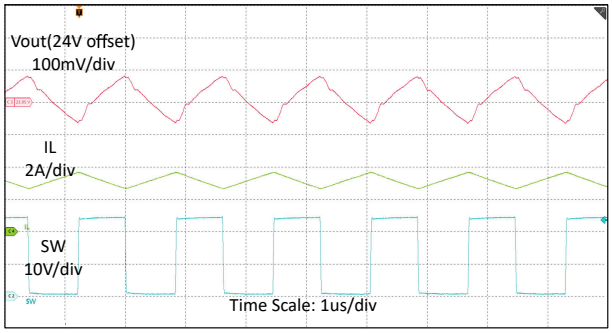
V_{IN} = 12 V V_{OUT} = 24 V R_{LOAD} = 16 Ω

図 8-2. Start-Up By EN Waveforms



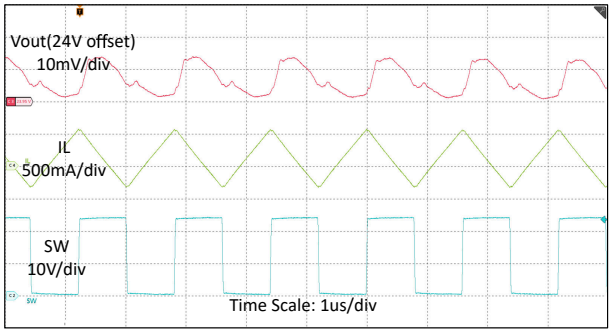
V_{IN} = 12 V V_{OUT} = 24 V R_{LOAD} = 16 Ω

図 8-3. Shutdown By EN Waveforms



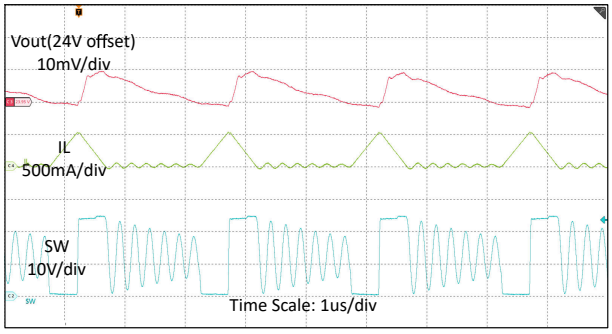
V_{IN} = 12 V V_{OUT} = 24 V I_{OUT} = 1.5 A

図 8-4. Switching Waveforms in CCM



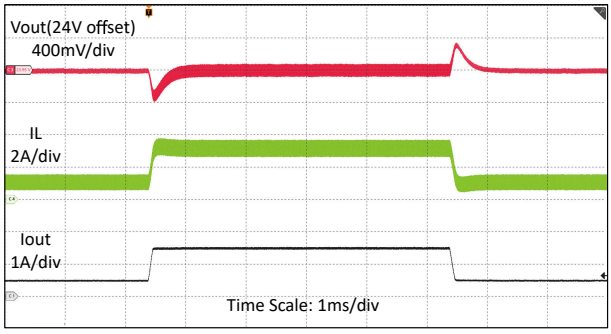
V_{IN} = 12 V V_{OUT} = 24 V I_{OUT} = 50 mA

図 8-5. Switching Waveforms in 50-mA Load FPWM Mode



V_{IN} = 12 V V_{OUT} = 24 V I_{OUT} = 50 mA

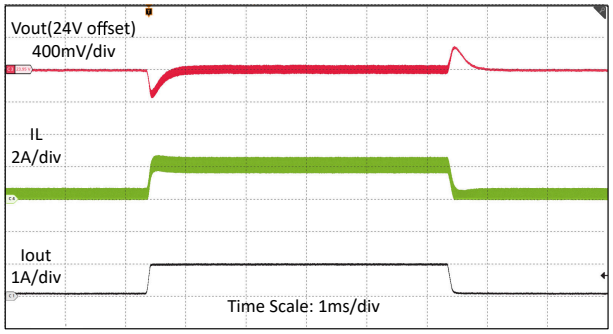
図 8-6. Switching Waveforms in 50-mA Load PFM Mode



V_{IN} = 12 V V_{OUT} = 24 V

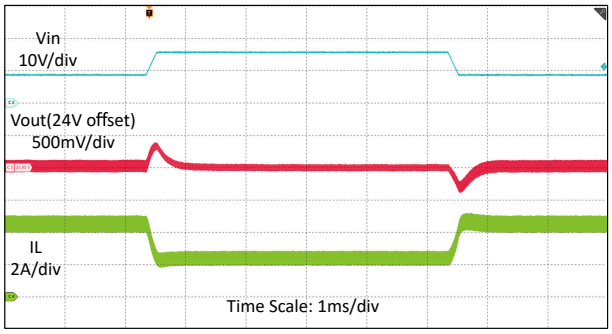
図 8-7. Load Transient (I_{OUT} = 0.5 A to 1.5 A)

8.2.3 Application Curves (continued)



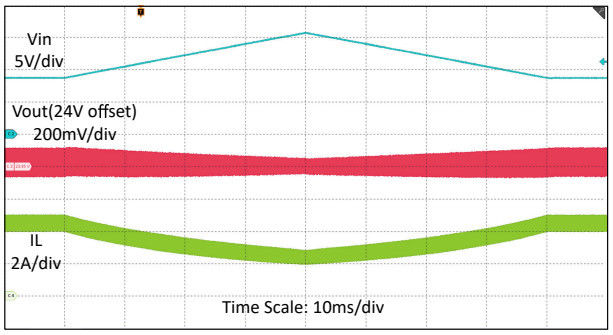
V_{IN} = 12 V V_{OUT} = 24 V

図 8-8. Load Transient (I_{OUT} = 0.1 to 1.0 A)



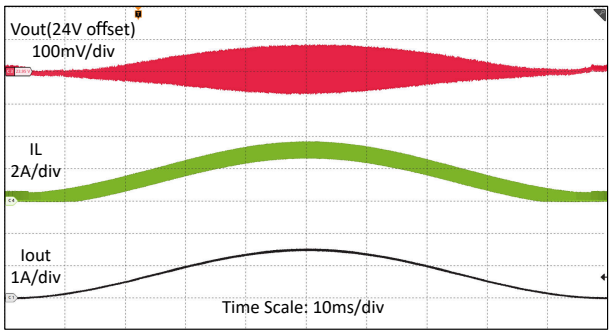
V_{OUT} = 24 V I_{OUT} = 1.5 A

図 8-9. Line Transient (V_{IN} = 9 V to 16 V)



V_{OUT} = 24 V I_{OUT} = 1.5 A

図 8-10. Line Sweep (V_{IN} = 9 V to 16 V)



V_{IN} = 12 V V_{OUT} = 24 V

図 8-11. Load Sweep (I_{OUT} = 0 A to 1.5 A)

8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.9 V to 23 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitor can be required in addition to the ceramic bypass capacitors. A typical choice is an electrolytic or tantalum capacitor with a value of 47 µF.

8.4 Layout

8.4.1 Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high current, layout is an important design step. If the layout is not carefully done, the regulator can suffer from instability and noise problems. To maximize efficiency, switching rise and fall times are very fast. To prevent radiation of high-frequency noise (for example, EMI), proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize interplane coupling.

The input capacitor needs to be close to the VIN pin and PGND pin in order to reduce the I_{input} supply ripple.

The power paths of VOUT, output capacitor and PGND should be as small as possible, in order to reduce parasitic inductance.

The layout should also be done with well consideration of the thermal as this is a high power density device. The SW, VOUT and PGND pins that improves the thermal capabilities of the package should be soldered with the large polygon, using thermal vias underneath the SW pin could improve thermal performance.

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8.4.2 Layout Example

The bottom layer is a large ground plane connected to the PGND plane and AGND plane on top layer by vias.

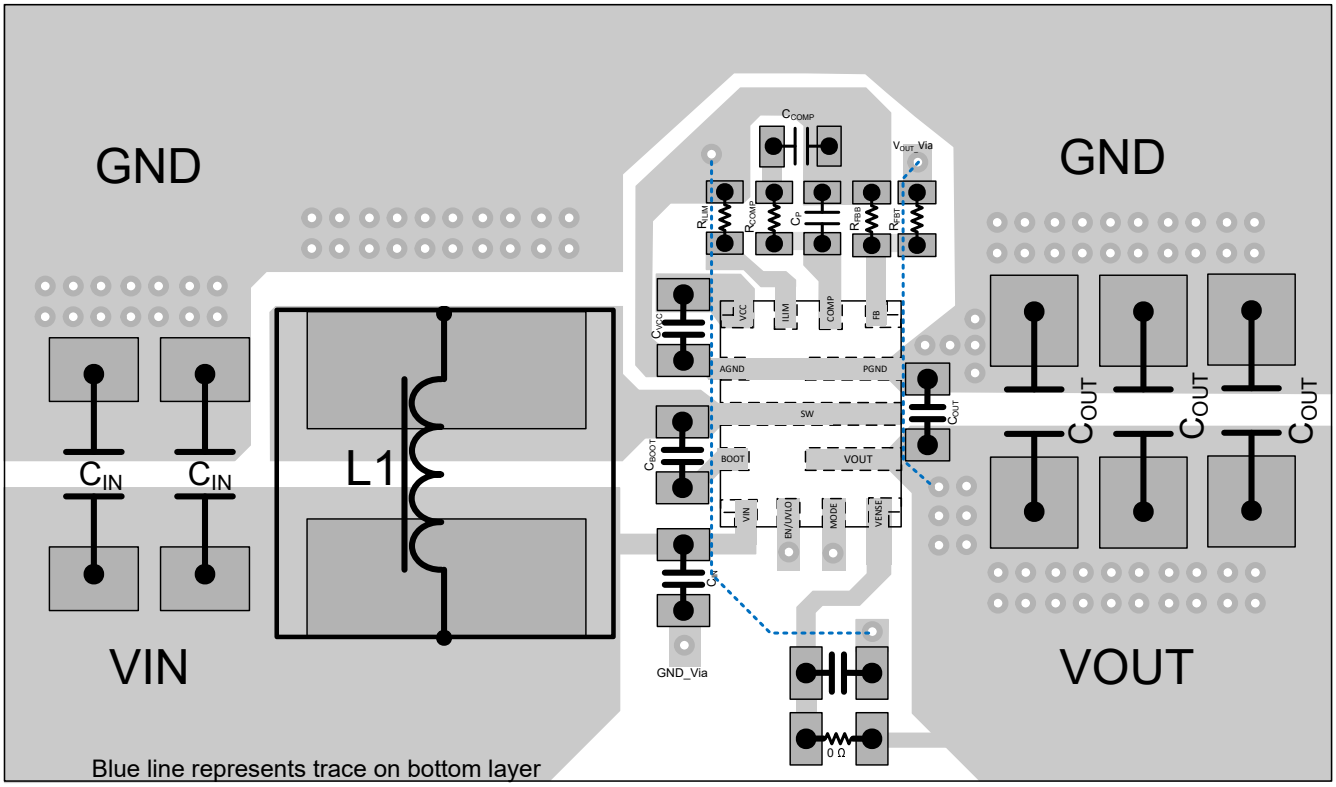

図 8-12. Layout Example

8.4.2.1 Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using 式 19.

$$P_{D(max)} = \frac{125 - T_A}{R_{\theta JA}} \tag{19}$$

where

- T_A is the maximum ambient temperature for the application.
- $R_{\theta JA}$ is the junction-to-ambient thermal resistance given in the *Thermal Information* table.

The TPS61377 comes in a thermally-enhanced VQFN package. The real junction-to-ambient thermal resistance of the package greatly depends on the PCB type, layout, and thermal pad connection. Using thick PCB copper enhances the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

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9 Device and Documentation Support

9.1 Device Support

9.1.1 サード・パーティ製品に関する免責事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
November 2023	*	Initial release.

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS613771RYHR	ACTIVE	VQFN-HR	RYH	13	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	3771	Samples
TPS61377RYHR	ACTIVE	VQFN-HR	RYH	13	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1377	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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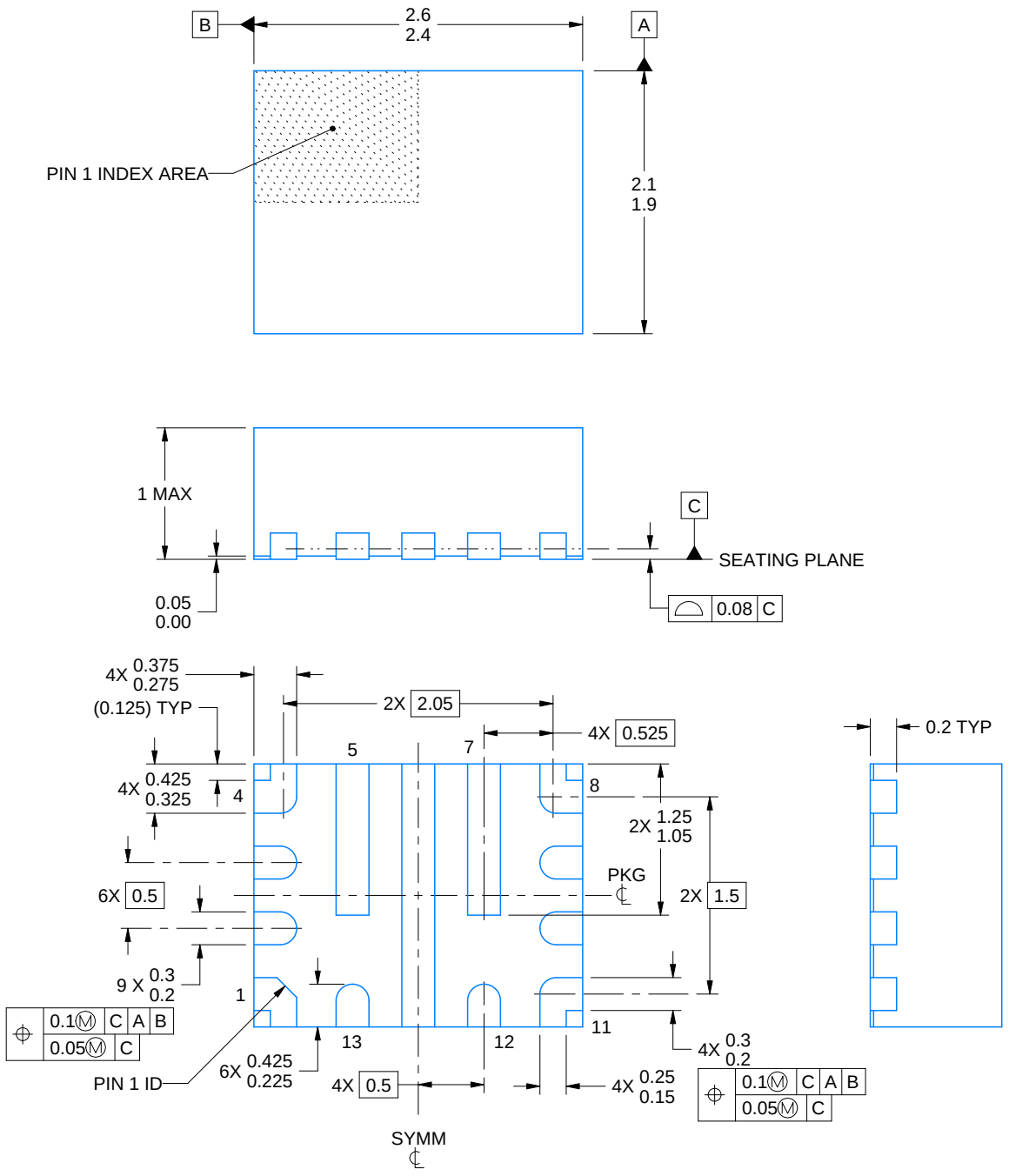
PACKAGE OUTLINE

RYH0013A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

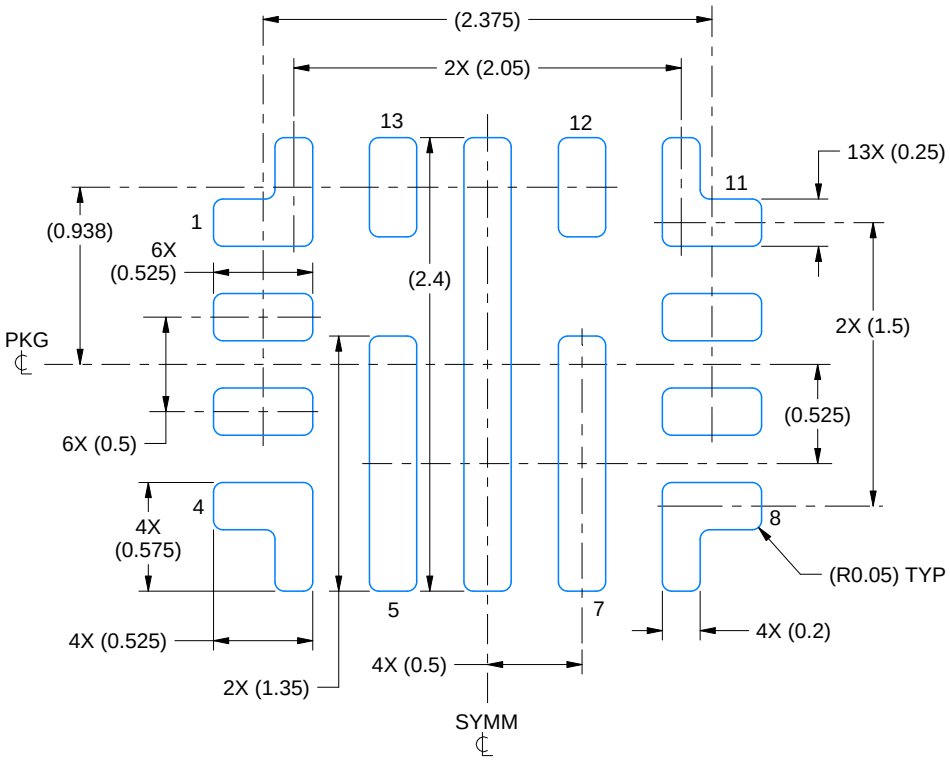
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

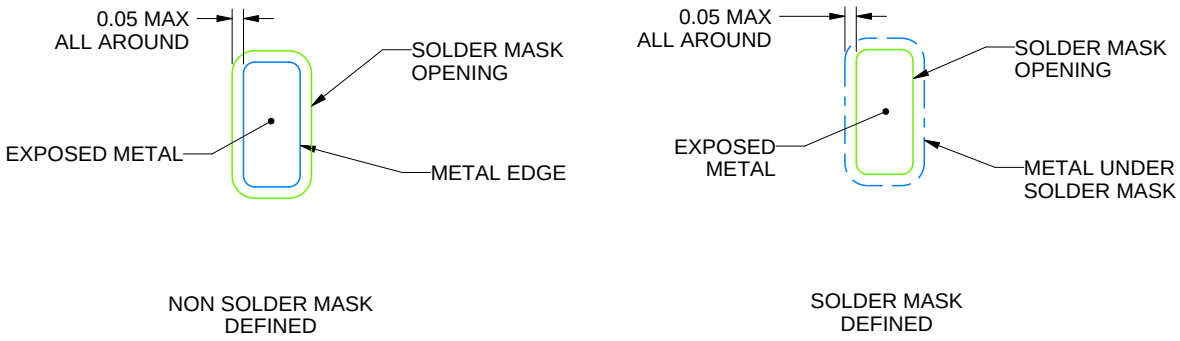
RYH0013A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



NON SOLDER MASK DEFINED

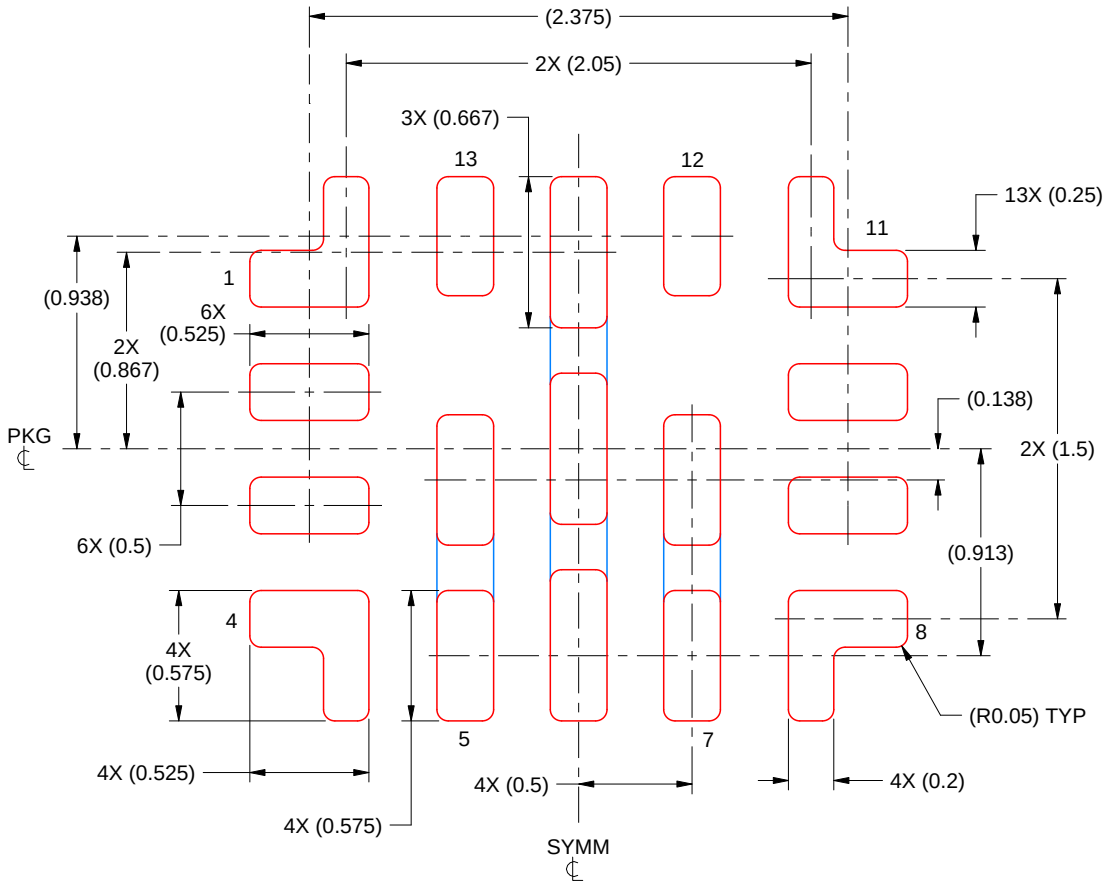
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4226722/A 04/2021

NOTES: (continued)

3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PIN 5 & 7 SOLDER COVERAGE = 85%
PIN 6 SOLDER COVERAGE = 83%
SCALE : 25X

4226722/A 04/2021

NOTES: (continued)

5. For alternate stencil design recommendations, see IPC-7525 or board assembly site preference.

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