TEXAS INSTRUMENTS
TPS62860, TPS62861
JAJSJ23F – SEPTEMBER 2019 – REVISED OCTOBER 2023

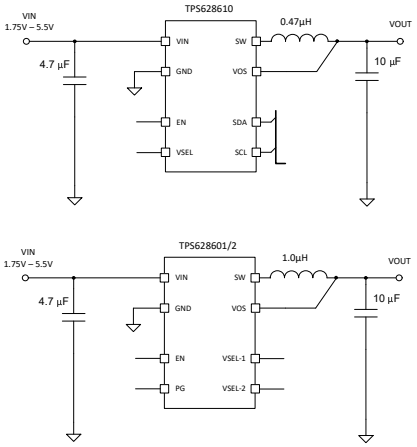
# TPS6286x I²C/VSEL インターフェイス搭載、1.75V～5.5V 入力、0.6/1A 同期整流降圧コンバータ

## 1 特長

- 動作時静止電流:2.3μA
- スイッチング周波数:最高 4MHz
- ±1% の出力電圧精度
- DVS 出力
  - 0.4V～1.9875V (12.5mV 刻み)
- 調整のための I²C ユーザー・インターフェイス
  - 出力電圧プリセット
  - ランプ速度
- 動作中に出力電圧を切り替えるための VSEL ピン
- パワー・グッド表示
- 6mm² 未満の設計サイズをサポート
- 0.6mm 未満の設計高さをサポート
- 小型、8 ピン、0.35mm ピッチ WCSP パッケージ
- 0201 コンポーネントのサポートに最適化されたピン配置

## 2 アプリケーション

- ウェアラブル電子機器
- ポータブル・エレクトロニクス
- 携帯電話
- 医療用センサ・パッチおよび患者モニタ




代表的なアプリケーション

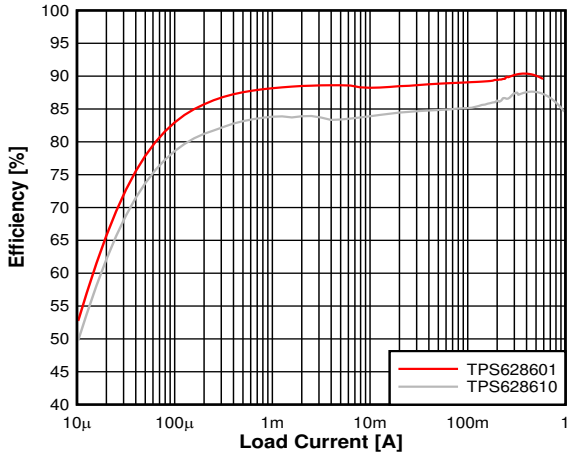
## 3 概要

TPS6286x デバイスは、I2C および VSEL インターフェイスを備えた高周波同期整流降圧コンバータです。これらの製品は、高効率かつ柔軟で電力密度が高いポイントオブロード DC/DC 設計を提供します。中負荷から高負荷では PWM モードで動作し、軽負荷時には自動的にパワーセーブ・モードへ移行するので、負荷電流の全範囲にわたって高効率が維持されます。このデバイスは、出力電圧リップルを最小化するために、強制的に PWM モードで動作させることもできます。DCS-Control アーキテクチャと相まって、優れた負荷過渡性能と厳格な出力電圧精度を実現します。I²C インターフェイスと専用 VSEL ピンにより出力電圧を迅速に変更できるので、常に変化するアプリケーションの性能要件に合わせて負荷の消費電力を調整できます。このデバイスは、2 本の VSEL ピンで 4 種類の工場出荷時プリセット電圧を選択できるため、I²C インターフェイスがなくても使用できます。

**製品情報**

| 部品番号 | 電流 | パッケージ (1) | パッケージ・サイズ (2) |
|---|---|---|---|
| TPS628610 | 1A | YCH (DSBGA、8) | 1.40mm × 0.70mm |
| TPS628601 | 0.6A | | |
| TPS628600 | 0.6A | | |
| TPS628603 | 0.6A | | |
| TPS628604 | 0.6A | | |

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。




効率と $I_{OUT}$ の関係 ($V_{OUT}$ = 1.1V、$V_{IN}$ = 3.8V)

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## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

**Changes from Revision E (April 2023) to Revision F (October 2023)** — **Page**

- データシートに TPS628604 を追加し、TPS628602 を削除 ... 1

**Changes from Revision D (May 2022) to Revision E (April 2023)** — **Page**

- TPS628603 をデータシートに追加 ... 1
- 商標の情報を更新 ... 1
- Updated the *ESD Ratings* CDM row to show testing was per JS-002 ... 5
- Added table note to the *Thermal Information* table ... 5

**Changes from Revision C (March 2022) to Revision D (May 2022)** — **Page**

- Corrected the internal fixed soft-start time test condition ... 5

**Changes from Revision B (September 2020) to Revision C (March 2022)** — **Page**

- TPS628602 をデータシートに追加 ... 1

## 5 Device Comparison Table

| ORDERABLE NUMBER | OUTPUT CURRENT (A) | DEFAULT $V_{OUT}$ SETTING (V) | SWITCHING FREQUENCY $f_{SW}$(MHz) | USER INTERFACE |
|---|---|---|---|---|
| TPS628600YCH | 0.6 | 0.6, 1.1 | 1.5 | EN, I2C, VSEL |
| TPS628601YCH | 0.6 | 0.6, 0.7, 0.8, 1.0 | 1.5 | 2× VSEL, EN, PG |
| TPS628603YCH | 0.6 | 1.05, 0.65 | 1.5 | EN, I2C, VSEL |
| TPS628604YCH | 0.6 | 0.85, 1.1 | 1.5 | EN, I2C, VSEL |
| TPS628610YCH | 1 | 0.6 , 1.1 | 4 | EN, I2C, VSEL |

## 6 Pin Configuration and Functions

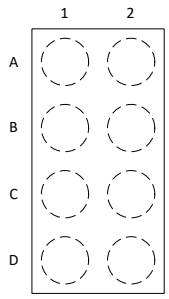



**図 6-1. 8-Pin DSBGA YCH Package (Top View)**

**表 6-1. Pin Functions, TPS628610, TPS628600, TPS6286003, and TPS6286004**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| GND | D2 | PWR | GND supply pin. Connect this pin close to the GND terminal of the input and output capacitor. |
| VOS | D1 | IN | Output voltage sense pin for the internal feedback divider network and regulation loop. This pin also discharges $V_{OUT}$ by an internal MOSFET when the converter is disabled. Connect this pin directly to the output capacitor with a short trace. |
| VIN | C2 | PWR | $V_{IN}$ power supply pin. Connect the input capacitor close to this pin for best noise and voltage spike suppression. A ceramic capacitor is required. |
| SW | C1 | PWR | The switch pin is connected to the internal MOSFET switches. Connect the inductor to this terminal. |
| VSEL | B2 | IN | Voltage Selection Pin. Can be toggled during operation. LOW = 0.6 V(TPS628600/10), 1.05 V(TPS628603), HIGH = 1.1 V(TPS628600/10), 0.65 V(TPS628603) |
| EN | B1 | IN | A high level enables the devices and a low level turns the device off. The pin features an internal pulldown resistor, which is disabled after the device has started up. |
| SDA | A2 | IN | $I^2C$ serial data pin. Do not leave floating. |
| SCL | A1 | IN | $I^2C$ serial clock pin. Do not leave floating. |

**表 6-2. Pin Functions, TPS628601**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| GND | D2 | PWR | GND supply pin. Connect this pin close to the GND terminal of the input and output capacitor. |
| VOS | D1 | IN | Output voltage sense pin for the internal feedback divider network and regulation loop. This pin also discharges VOUT by an internal MOSFET when the converter is disabled. Connect this pin directly to the output capacitor with a short trace. |
| VIN | C2 | PWR | VIN power supply pin. Connect the input capacitor close to this pin for best noise and voltage spike suppression. A ceramic capacitor is required. |
| SW | C1 | PWR | The switch pin is connected to the internal MOSFET switches. Connect the inductor to this terminal. |
| PG | B2 | OUT | Open-drain power-good output |
| EN | B1 | IN | A high level enables the devices and a low level turns the device off. The pin features an internal pulldown resistor, which is disabled after the device has started up. |
| VSEL-1 | A2 | IN | Voltage Selection Pin. Can be toggled during operation. |
| VSEL-2 | A1 | IN | Voltage Selection Pin. Can be toggled during operation. |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Pin voltage | VIN | –0.3 | 6 | V |
| Pin voltage | SW, DC | –0.3 | $V_{IN}$ +0.3V | V |
| Pin voltage | SW, transient < 10 ns, while switching | –2.5 | 9 | V |
| Pin voltage | EN, VSEL, SDA, SCL, PG | –0.3 | 6 | V |
| Pin voltage | VOS | –0.3 | 5 | V |
| $T_J$ | Operating junction temperature | –40 | 150 | °C |
| $T_{stg}$ | Storage temperature | –55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) | ±2000 | V |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input supply voltage range | | 1.75 | | 5.5 | V |
| $V_{OUT}$ | Output voltage range | | 0.4 | | 1.9875 | V |
| | Pin voltage | SW | 0 | | 5.5 | V |
| | Pin voltage | EN, SDA, SCL, VSEL, PG | 0 | | 5.5 | V |
| $I_{OUT}$ | Output current range | TPS628610, $V_{IN}$ > 2.3V | | | 1 | A |
| $I_{OUT}$ | Output current range | TPS628610, $V_{IN}$ <= 2.3V | | | 0.7 | A |
| $I_{OUT}$ | Output current range | TPS628601 | | | 0.6 | A |
| $I_{PG}$ | Power Good input current capability | | | | 1 | mA |
| $T_J$ | Operating junction temperature | | -40 | | 125 | °C |
| $C_{IN}$ | Effective Input Capacitance | | 2 | 4.7 | | µF |
| L | Effective Inductance | TPS628610 | 0.33 | 0.47 | 0.82 | µH |
| COUT | Effective Output Capacitance | | 2 | | 26 | µF |
| L | Effective Inductance | TPS628601 | 0.7 | 1.0 | 1.2 | µH |
| COUT | Effective Output Capacitance | | 3 | | 26 | µF |

## 7.4 Thermal Information

| THERMAL METRIC(1) | | DEVICE YCH (DSBGA) 8 PINs | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 121.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 1.1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 33.7 | °C/W |

| THERMAL METRIC(1) | | DEVICE | UNIT |
|---|---|---|---|
| | | YCH (DSBGA) | |
| | | 8 PINs | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.7 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 33.5 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 7.5 Electrical Characteristics

$T_J$ = –40°C to +125°C, $V_{IN}$ = 3.6 V. Typical values are at $T_J$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY** | | | | | | |
| $I_{Q(VIN)}$ | VIN quiescent current | EN = VIN, IOUT = 0µA, VOUT = 1.2 V device not switching, TJ = -40°C to +85°C | | 2.3 | 4 | µA |
| | | EN = VIN, IOUT = 0µA, VOUT = 1.2 V, device switching | | 2.5 | | µA |
| $I_{SD(VIN)}$ | VIN shutdown supply current | EN = GND, shutdown current into VIN VSEL/MODE = GND, TJ = -40°C to +85°C | | 120 | 250 | nA |
| **UVLO** | | | | | | |
| $V_{UVLO(R)}$ | VIN UVLO rising threshold | $V_{IN}$ rising | | 1.65 | 1.75 | V |
| $V_{UVLO(F)}$ | VIN UVLO falling threshold | $V_{IN}$ falling | | 1.56 | 1.7 | V |
| $V_{UVLO(H)}$ | VIN UVLO hysteresis | | | 100 | | mV |
| **LOGIC PINs** | | | | | | |
| $V_{IH}$ | High-level input voltage threshold | | 0.8 | | | V |
| $V_{IL}$ | Low-level input voltage threshold | | | | 0.4 | V |
| $I_{LKG}$ | Input leakage current into SDA, SCL, VSEL | Pin connected to VIN | | 10 | 25 | nA |
| | EN internal pull-down resistance | EN pin to GND | | 0.5 | | MΩ |
| $I_{LKG}$ | Input Leakage into EN | Pin connected to VIN | | 10 | 25 | nA |
| **VOUT VOLTAGE** | | | | | | |
| $V_{OUT}$ | Output Voltage Accuracy | PWM Mode, no load, $T_J$ = 25°C to 85°C | -1 | | +1 | % |
| $V_{OUT}$ | Output Voltage Accuracy | PWM Mode, no load, $T_J$ = -40°C to 125°C | -2 | | +1.7 | % |
| $I_{VOS(LKG)}$ | VOS input leakage current | EN = VIN, VOUT = 1.2 V (internal 12MΩ resistor divider), TJ = -40°C to +85°C | | 100 | 400 | nA |
| **SWITCHING FREQUENCY** | | | | | | |
| $f_{SW(FCCM)}$ | Switching frequency, TPS62861x | VIN = 3.6V, VOUT =1.2V, PWM operation | | 4 | | MHz |
| $f_{SW(FCCM)}$ | Switching frequency, TPS62860x | VIN = 3.6V, VOUT =1.2V, PWM operation | | 1.5 | | MHz |
| **STARTUP** | | | | | | |
| | Internal fixed soft-start time | from VOUT = 0V to 95% of VOUT nominal | | 0.125 | 0.2 | ms |
| | EN HIGH to start of switching delay | | | 500 | 1000 | µs |
| **POWER STAGE** | | | | | | |
| $R_{DSON(HS)}$ | High-side MOSFET on-resistance | IOUT = 500 mA | | 120 | 170 | mΩ |
| $R_{DSON(LS)}$ | Low-side MOSFET on-resistance | IOUT = 500 mA | | 80 | 115 | mΩ |
| **OVERCURRENT PROTECTION** | | | | | | |
| $I_{HS(OC)}$ | High-side peak current limit | TPS628610 | 1.3 | 1.45 | 1.55 | A |
| $I_{LS(OC)}$ | Low-side valley current limit | TPS628610 | 1.2 | 1.35 | 1.45 | A |
| $I_{HS(OC)}$ | High-side peak current limit | TPS628601 | 0.95 | 1.1 | 1.2 | A |
| $I_{LS(OC)}$ | Low-side valley current limit | TPS628601 | 0.85 | 1.0 | 1.1 | A |
| $I_{LS(NOC)}$ | Low-side negative current limit | Sinking current limit on LS FET | | 0.8 | | A |
| **POWER GOOD** | | | | | | |
| $V_{PGTH}$ | Power Good threshold | PGOOD low, VOS falling | | 93% | | |
| $V_{PGTH}$ | Power Good threshold | PGOOD high, VOS rising | | 96% | | |
| $t_{PG:DLY}$ | Power good deglitch delay | PG rising edge | | 16 | | µs |
| $I_{PG;LKG}$ | Input leakage current into PG-pin | $V_{PG}$ = 5.0V | | 10 | 100 | nA |
| | PG-pin output low-level voltage | $I_{PG}$ = 1mA | | | 400 | mV |
| **OUTPUT DISCHARGE** | | | | | | |
| | Output discharge resistor on VOS pin | EN = GND, IVOS = –10 mA into VOS pin TJ = -40°C to +85°C | | 7 | 11 | Ω |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{J(SD)}$ | Thermal shutdown threshold (1) | Temperature rising, PWM Mode | | 160 | | °C |

$T_J$ = –40°C to +125°C, $V_{IN}$ = 3.6 V. Typical values are at $T_J$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $T_{J(HYS)}$ | Thermal shutdown hysteresis (1) | | | 20 | | °C |

(1) Specified by design. Not production tested.

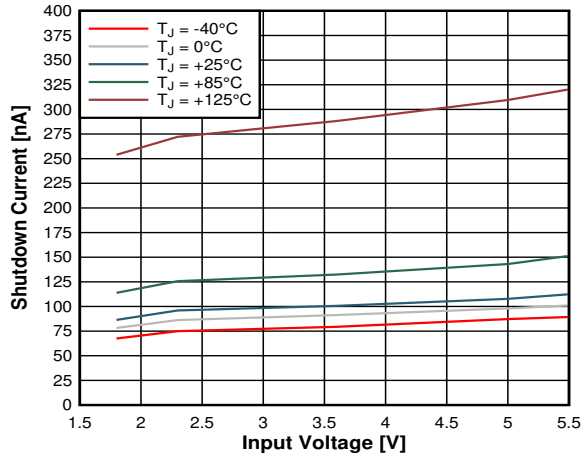
## 7.6 I²C Interface Timing Characteristics

| PARAMETER(1) | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | SCL Clock Frequency | Standard mode | | | 100 | kHz |
| | | Fast mode | | | 400 | kHz |
| | | Fast mode plus | | | 1 | MHz |
| $t_{BUF}$ | Bus Free Time Between a STOP and START Condition | Standard mode | 4.7 | | | µs |
| | | Fast mode | 1.3 | | | µs |
| | | Fast mode plus | 0.5 | | | µs |
| $t_{HD}$, $t_{STA}$ | Hold Time (Repeated) START condition | Standard mode | 4 | | | µs |
| | | Fast mode | 600 | | | ns |
| | | Fast mode plus | 260 | | | ns |
| $t_{LOW}$ | LOW Period of the SCL Clock | Standard mode | 4.7 | | | µs |
| | | Fast mode | 1.3 | | | µs |
| | | Fast mode plus | 0.5 | | | µs |
| $t_{HIGH}$ | HIGH Period of the SCL Clock | Standard mode | 4 | | | µs |
| | | Fast mode | 600 | | | ns |
| | | Fast mode plus | 260 | | | ns |
| $t_{SU}$, $t_{STA}$ | Setup Time for a Repeated START Condition | Standard mode | 4.7 | | | µs |
| | | Fast mode | 600 | | | ns |
| | | Fast mode plus | 260 | | | ns |
| $t_{SU}$, $t_{DAT}$ | Data Setup Time | Standard mode | 250 | | | ns |
| | | Fast mode | 100 | | | ns |
| | | Fast mode plus | 50 | | | ns |
| $t_{HD}$, $t_{DAT}$ | Data Hold Time | Standard mode | 0 | | 3.45 | µs |
| | | Fast mode | 0 | | 0.9 | µs |
| | | Fast mode plus | 0 | | | µs |
| $t_{RCL}$ | Rise Time of SCL Signal | Standard mode | | | 1000 | ns |
| | | Fast mode | 20+0.1CB | | 300 | ns |
| | | Fast mode plus | | | 120 | ns |
| $t_{RCL1}$ | Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge BIT | Standard mode | 20+0.1CB | | 1000 | ns |
| | | Fast mode | 20+0.1CB | | 300 | ns |
| | | Fast mode plus | | | 120 | ns |
| $t_{FCL}$ | Fall Time of SCL Signal | Standard mode | 20+0.1CB | | 300 | ns |
| | | Fast mode | | | 300 | ns |
| | | Fast mode plus | | | 120 | ns |
| $t_{RDA}$ | Rise Time of SDA Signal | Standard mode | | | 1000 | ns |
| | | Fast mode | 20+0.1CB | | 300 | ns |
| | | Fast mode plus | | | 120 | ns |

| PARAMETER[1] | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{FDA}$ | Fall Time of SDA Signal | Standard mode | | | 300 | ns |
| | | Fast mode | 20+0.1CB | | 300 | ns |
| | | Fast mode plus | | | 120 | ns |
| $t_{SU}$, $t_{STO}$ | Setup Time of STOP Condition | Standard mode | 4 | | | µs |
| | | Fast mode | 600 | | | ns |
| | | Fast mode plus | 260 | | | ns |
| CB | Capacitive Load for SDA and SCL | Standard mode | | | 400 | pF |
| | | Fast mode | | | 400 | pF |
| | | Fast mode plus | | | 550 | pF |

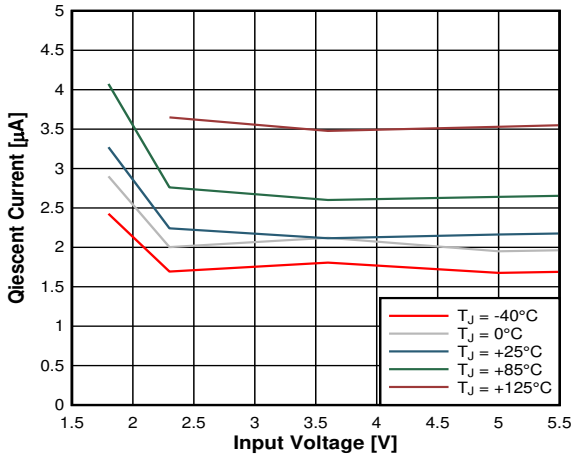
(1) All values referred to $V_{IL}$ MAX and $V_{IH}$ MIN levels in ELECTRICAL CHARACTERISTICS table.

## 7.7 Typical Characteristics




EN = GND

**図 7-1. Shutdown Current $I_{SD}$**




EN = VIN　　Device not switching

**図 7-2. Quiescent Current $I_Q$**

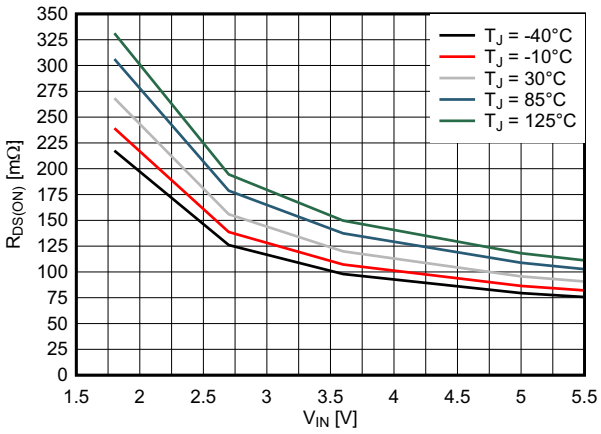



**図 7-3. High-side Switch Drain Source Resistance $R_{DS(ON)}$**

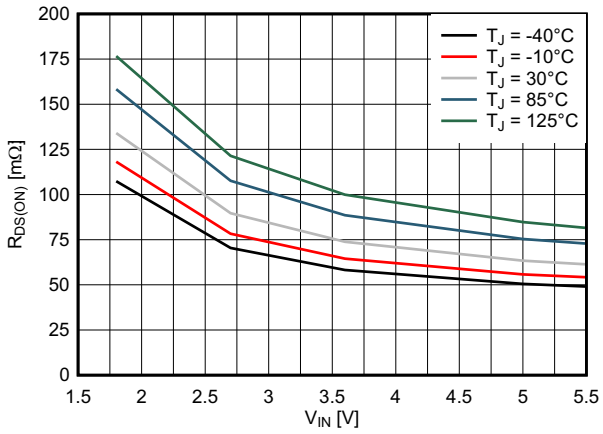


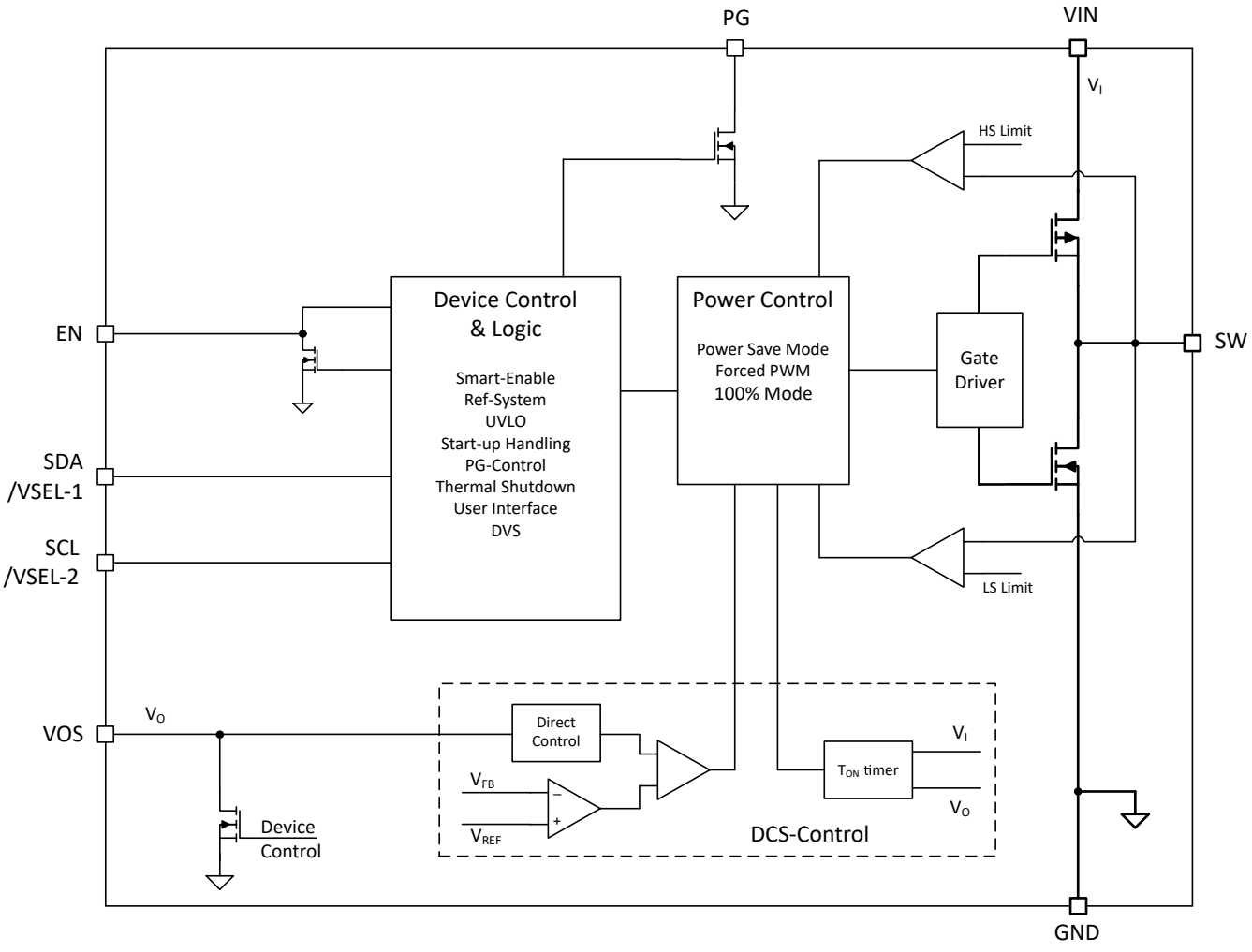

**図 7-4. Low-side Switch Drain Source Resistance $R_{DS(ON)}$**

# 8 Detailed Description

## 8.1 Overview

The TPS6286x is a high-frequency synchronous step-down converter with ultra-low quiescent current consumption and flexible output voltage by I²C or VSEL interface. Using TI's DCS-Control topology, the device extends the high efficiency operation area down to microamperes of load current during Power Save Mode Operation. TI's DCS-Control (direct control with seamless transition into power save mode) is an advanced regulation topology, which combines the advantages of hysteretic and voltage mode control. Characteristics of DCS-Control are excellent AC load regulation and transient response, low output ripple voltage, and a seamless transition between PFM and PWM mode operation. DCS-Control includes an AC loop which senses the output voltage (VOS pin) and directly feeds the information to a fast comparator stage. This comparator sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To achieve accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

### 8.3.1 Power Save Mode

As the load current decreases, the device enters Power Save Mode (PSM) operation. PSM occurs when the inductor current becomes discontinuous, which is when it reaches 0 A during a switching cycle. In Power Save

Mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor or inductor value.

### 8.3.2 Forced PWM Operation

Through $I^2C$, set the device in forced PWM (FPWM) mode by the CONTROL register. The device switches continuously, even with a light load. This reduces the output voltage ripple and allows simple filtering of the switching frequency for noise-sensitive applications. Efficiency at light load is lower in FPWM mode.

### 8.3.3 Smart Enable and Shutdown (EN)

An internal 500-kΩ resistor pulls the EN pin to GND and avoids the pin to be floating. This prevents an uncontrolled start-up of the device in case the EN pin cannot be driven to low level safely. With EN low, the device is in shutdown mode. The device is turned on with EN set to a high level. The pulldown control circuit disconnects the pulldown resistor on the EN pin after the internal control logic and the reference have been powered up. With EN set to a low level, the device enters shutdown mode and the pulldown resistor is activated again.

### 8.3.4 Soft Start

After the device has been enabled with EN high, it initializes and powers up its internal circuits. This occurs during the regulator start-up delay time, $t_{Delay}$. After $t_{Delay}$ expires, the internal soft-start circuitry ramps up the output voltage within the soft-start time, $t_{Ramp}$. See 図 8-1.

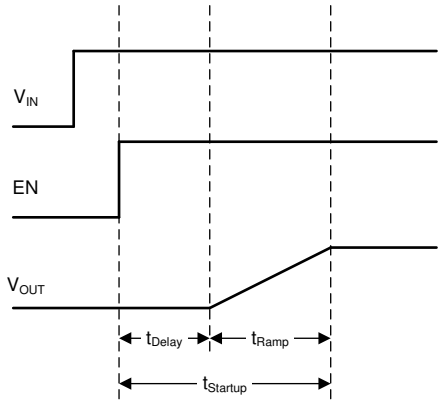



**図 8-1. Start-up Sequence**

### 8.3.5 Output Voltage Selection (VSEL) for TPS62860x

The optional VSEL Interface allows setting the output voltage by a 2-pin HIGH/LOW setting. Using and applying a digital pattern to the "VSEL-1" and "VSEL-2" pins sets the output voltage according to 表 8-1.

**表 8-1. Target Output Voltage Setting by VSEL Interface**

| VSEL-2 | VSEL-1 | TPS628601 | TPS628602 | OPERATION MODE |
|---|---|---|---|---|
| 0 | 0 | 0.6 V | 1.05 V | PFM Mode |
| 0 | 1 | 0.7 V | 0.9 V | PFM Mode |
| 1 | 0 | 0.8 V | 0.875 V | PFM Mode |
| 1 | 1 | 1.0 V | 0.625 V | PFM Mode |

### 8.3.6 Output Voltage Selection (VSEL and $I^2C$)

The TPS6286x has two options to select the output voltage.

The voltage on the VSEL pin can changes the output voltage. Putting this pin HIGH selects the output voltage according to $V_{OUT}$ register 2. Putting this pin LOW selects the voltage according to $V_{OUT}$ Register 1. The pin can be toggled during operation.

It can also be selected by the value in the $V_{OUT}$ register that is chosen by VSEL at the moment. The voltage changes right after the $I^2C$ command is received.

### 8.3.7 Forced PWM Mode During Output Voltage Change

In normal operation, the device does not force PWM operation during VOUT change after VSEL toggle or $I^2C$ command. For ramping down, this mode provides the remaining energy, stored in the output capacitor to the load of the DC/DC and save battery charge. See 図 9-14.

Through $I^2C$, the device can be set to forced PWM (FPWM) switching during output voltage change. This allows a controlled ramp of $V_{OUT}$ up and especially down, regardless of the load condition. See 図 9-15.

This feature follows the internal $I^2C$ ramp and is only recommended for the setting 1 mV/µs and 0.1 mV/µs. During the faster slopes (10 mV/µs and 5 mV/µs), the mode is likely to be left before the voltage reached the new target value.

### 8.3.8 Undervoltage Lockout (UVLO)

To avoid misoperation of the device at low input voltages, an undervoltage lockout (UVLO) comparator monitors the supply voltage. The UVLO comparator shuts down the device at an input voltage of 1.7 V (max) with falling VIN. The device starts at an input voltage of 1.8 V (max) rising VIN. After the device re-enters operation out of an undervoltage lockout condition, it behaves like being enabled.

### 8.3.9 Power Good (PG)

The built-in power-good (PG) signal indicates that the output voltage has reached its target and the device is ready. The PG signal can be used for start-up sequencing of multiple rails or to indicate any overload behavior on the output. The PG pin is an open-drain output that requires a pullup resistor to any voltage up to the recommended input voltage level. PG is low when the device is turned off due to EN or thermal shutdown. VIN must remain present for the PG pin to stay LOW. When applying VIN the first time, PG stays HIGH until the first enabling of the device.

If the power-good output is not used, TI recommends to tie to GND or leave open.

**表 8-2. Power Good Indicator Functional Table**

| LOGIC SIGNALS | | | | | PG STATUS |
|---|---|---|---|---|---|
| $V_I$ | EN-PIN | THERMAL SHUTDOWN | $V_{OUT}$ | DVS TRANSITION ACTIVE | |
| $V_I$ > UVLO | HIGH | NO | $V_{OUT}$ on target | NO | **High Impedance** |
| | | | | YES | **LOW** |
| | | | $V_{OUT}$ < target | x | **LOW** |
| | | YES | x | x | **LOW** |
| | LOW | x | x | x | **LOW** |
| $V_I$ < UVLO | x | x | x | x | **Undefined** |

The PG indicator triggers immediately (after internal comparator delay) when $V_O$ crosses the lower $V_{PGTH}$ to indicate that the voltage has left the target setting. It features a delay after crossing the upper $V_{PGTH}$ when going high to make sure $V_O$ has reached the target again. 図 8-2 sketches the behavior.

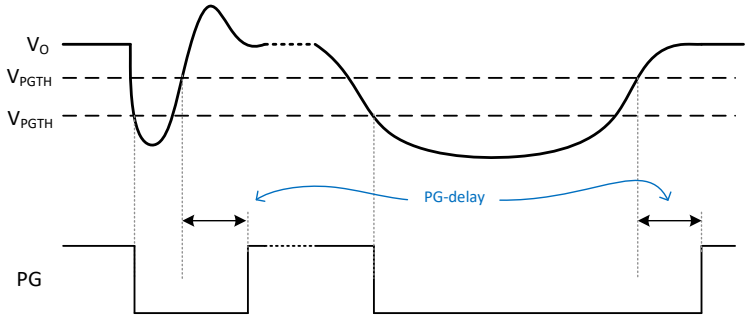



**図 8-2. Power Good Transient and De-glitch Behavior**

The PG Indicator is by default pulled low during DVS transition of the output voltage without any blanking or delay time. 図 8-2 shows an example of this behavior. After $V_O$ has reached the new target, the PG is again active as shown in 図 8-2.

### 8.3.10 Switch Current Limit and Short Circuit Protection

The TPS6286x integrates a current limit on the high-side and low-side MOSFETs to protect the converter against overload or short-circuit conditions. The current in the switches is monitored cycle by cycle. If the high-side MOSFET current limit, $I_{LIMF}$, trips, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. After the inductor current through the low-side switch decreases below the low-side MOSFET current limit, $I_{LIMF}$, the low-side MOSFET is turned off and the high-side MOSFET turns on again.

### 8.3.11 Thermal Shutdown

The junction temperature ($T_J$) of the device is monitored by an internal temperature sensor. If $T_J$ exceeds the thermal shutdown temperature TSD of 160°C (typ), the device enters thermal shutdown. Both the high-side and low-side power FETs are turned off. When $T_J$ decreases below the hysteresis amount of typically 20°C, the converter resumes operation, beginning with a soft start to the originally set VOUT. The thermal shutdown is not active in Power Save Mode.

### 8.3.12 Output Voltage Discharge

The purpose of the output discharge function is to ensure a defined down-ramp of the output voltage when the device is disabled and to keep the output voltage close to 0 V. The output discharge feature is only active after the device has been enabled at least once since the supply voltage was applied. The output discharge function is not active if the device is disabled and the supply voltage is applied the first time. The internal discharge resistor is connected to the VOS pin. The discharge function is enabled as soon as the device is disabled. The minimum supply voltage required to keep the discharge function active is $V_I > V_{TH\_UVLO-}$.

## 8.4 Programming

### 8.4.1 Serial Interface Description

I2C™ is a 2-wire serial interface developed by Philips Semiconductor, now NXP Semiconductors (see I²C-Bus Specification, Version .6, 2014). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All the I²C-compatible devices connect to the I²C bus through open-drain I/O pins, SDA and SCL. A *master* device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A *slave* device receives, transmits data, or both on the bus under control of the master device.

The device works as a *slave* and supports the following data transfer *modes*, as defined in the I²C-Bus Specification: standard mode (100 kbps), fast mode (400 kbps), and fast mode plus (1 Mbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as the input voltage remains above 1.8 V.

The data transfer protocol for standard and fast modes is exactly the same, therefore, they are referred to as F/S-mode in this document. The protocol for high-speed mode is different and must not be used.

It is recommended that the I²C master initiates a STOP condition on the I²C bus after the initial power up of SDA and SCL pullup voltages to ensure reset of the I²C engine.

### 8.4.2 Standard- and Fast-Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in 図 8-3. All I²C-compatible devices recognize a start condition.

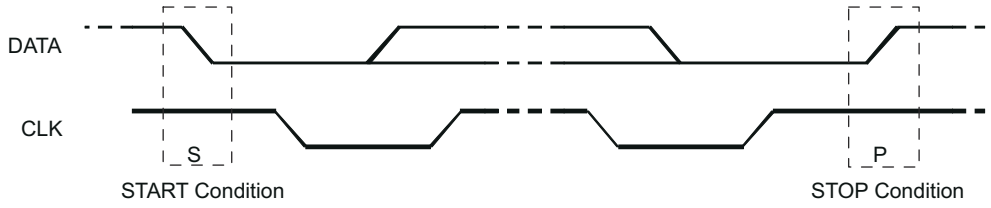



**図 8-3. START and STOP Conditions**

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see 図 8-4). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see 図 8-5) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

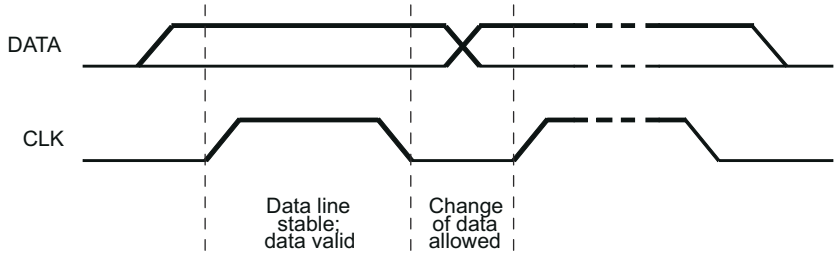



**図 8-4. Bit Transfer on the Serial Interface**

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver must acknowledge the data sent by the transmitter. An acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see 図 8-3). This action releases the bus and stops the communication link with the addressed slave. All $I^2C$-compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and the devices wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section results in 00h being read out.

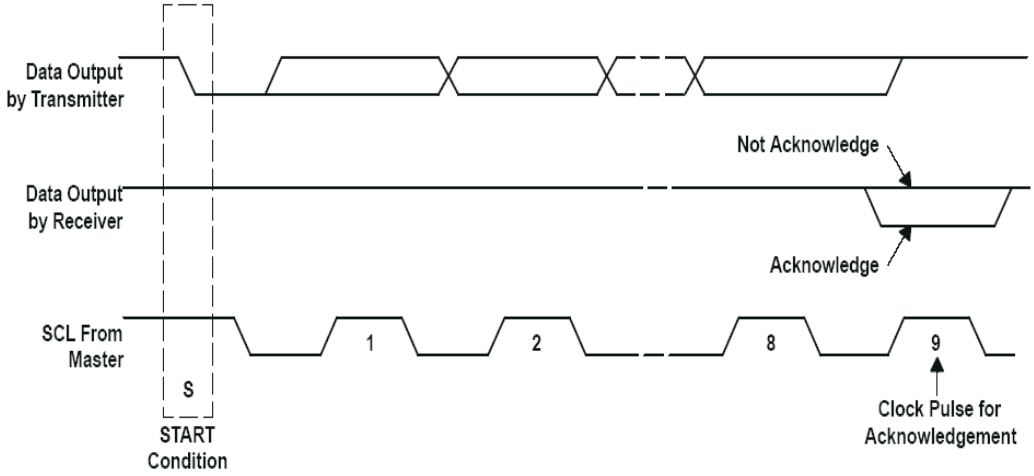



**図 8-5. Acknowledge on the $I^2C$ Bus**

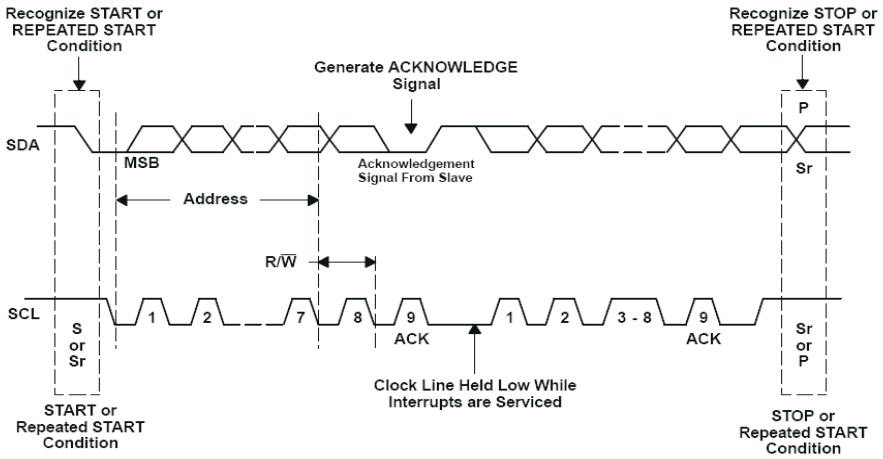



**図 8-6. Bus Protocol**

### 8.4.3 $I^2C$ Update Sequence

The requires the following:

- A start condition
- A valid $I^2C$ address
- A register address byte
- A data byte for a single update

After the receipt of each byte, the device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the device. The device performs an update on the falling edge of the acknowledge signal that follows the LSB byte.


**図 8-7. "Write" Data Transfer Format in Standard-, Fast, and Fast-Plus Modes**

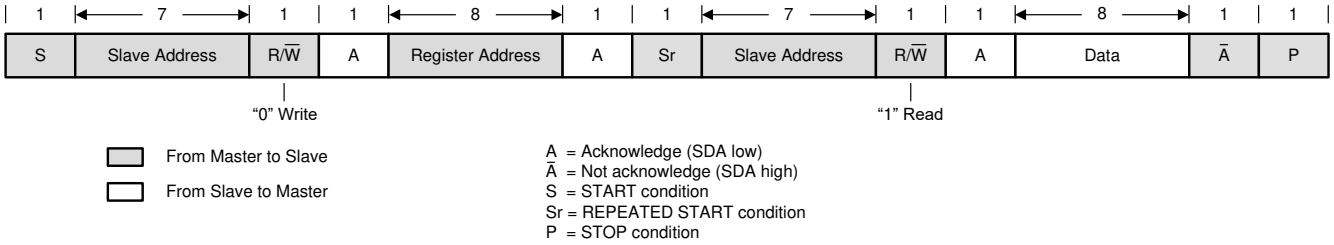



**図 8-8. "Read" Data Transfer Format in Standard-, Fast, and Fast-Plus Modes**

### 8.4.4 I²C Register Reset

The I²C registers can be reset by the following:

- Pull the input voltage below 1.8 V (typ).
- A high to low transition on EN. The previous value of the "Enable Output Discharge" bit is latched until the next EN rising edge or pulling the input voltage below 1.0 V (typ).
- Set the Reset bit in the CONTROL register. When Reset is set to 1, all registers are reset to the default values and a new start-up begins immediately. After $t_{Delay}$, the I²C registers can be programmed again.

## 8.5 Register Map

表 8-3. Register Map

| REGISTER ADDRESS (HEX) | REGISTER NAME | FACTORY DEFAULT (HEX) | DESCRIPTION |
|---|---|---|---|
| 0x01 | $V_{OUT}$ Register 1 | 0x10 | Sets the target output voltage |
| 0x02 | $V_{OUT}$ Register 2 | 0x38 | Sets the target output voltage |
| 0x03 | CONTROL Register | | Sets miscellaneous configuration bits |
| 0x05 | STATUS Register | 0x00 | Returns status flags, cleared on read-out |

### 8.5.1 Slave Address Byte

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | R/W |

The slave address byte is the first byte received following the START condition from the master device. The 7-bit slave address is 0x40 and internally set.

### 8.5.2 Register Address Byte

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | D2 | D1 | D0 |

Following the successful acknowledgment of the slave address, the bus master sends a byte to the device, which contains the address of the register to be accessed.

### 8.5.3 $V_{OUT}$ Register 1

表 8-4. $V_{OUT}$ Register 1 Description (Output Voltage Range 0.4 V to 1.9875 V)

| REGISTER ADDRESS 0X01 READ/WRITE | | | |
|---|---|---|---|
| BIT | FIELD | VALUE (HEX) | OUTPUT VOLTAGE (TYP) |
| 6:0 | VO1_SET | 0x00 | 0.400 V |
| | | 0x01 | 0.4125 V |
| | | ... | |
| | | 0x10 | **0.600 V** (default value for TPS628600/ TPS628610) |
| | | 0x24 | **0.85 V** (default value for TPS628604) |
| | | ... | |
| | | 0x34 | **1.05 V** (default value for TPS628603) |
| | | ... | |
| | | 0x7E | 1.975 V |
| | | 0x7F | 1.9875 V |

### 8.5.4 $V_{OUT}$ Register 2

**表 8-5. $V_{OUT}$ Register 2 Description (Output Voltage Range 0.4 V to 1.9875 V)**

| REGISTER ADDRESS 0X02 READ/WRITE | | | |
|---|---|---|---|
| **BIT** | **FIELD** | **VALUE (HEX)** | **OUTPUT VOLTAGE (TYP)** |
| 7 | Operation Mode | 0x00 | 0 - Keep PFM/PWM selection as in CONTROL-Register<br>1 - sets the device in PWM operation for this Voltage selection |
| 6:0 | VO2_SET | 0x00 | 0.400 V |
| | | 0x01 | 0.4125 V |
| | | ... | |
| | | 0x14 | **0.65 V** (default value for TPS628603) |
| | | ... | |
| | | 0x38 | **1.10 V** (default value for TPS628600/04 and TPS628610) |
| | | ... | |
| | | 0x7E | 1.975 V |
| | | 0x7F | 1.9875 V |

### 8.5.5 CONTROL Register

**表 8-6. CONTROL Register Description**

| REGISTER ADDRESS 0X03 READ/WRITE | | | | |
|---|---|---|---|---|
| **BIT** | **FIELD** | **TYPE** | **DEFAULT** | **DESCRIPTION** |
| 7 | Reset | W | 0 | 1 - Reset all registers to default.<br>This bit triggers a shutdown followed by a re-reading of the internal OTP settings and a new soft start. |
| 6 | Enable FPWM Mode during Output Voltage Change | R/W | 1 | 0 - Keep the current mode status during output voltage change.<br>1 - Force the device in FPWM during output voltage change. |
| 5 | Software Enable Device | R/W | 1 | 0 - Disable the device. All registers values are still kept.<br>1 - Re-enable the device with a new start-up without the $t_{Delay}$ period. |
| 4 | Enable FPWM Mode | R/W | 0 | 0 - Set the device in power save mode at light loads.<br>1 - Set the device in forced PWM mode at light loads. |
| 3 | Enable Output Discharge | R/W | 1 | 0 - Disable output discharge.<br>1 - Enable output discharge.<br>This setting is used for the next disable cycle (Software or Hardware). |
| 2 | Reserved | | | |
| 0:1 | Voltage Ramp Speed | R/W | 11(1) | 00 - 10mV/µs<br>01 - 5 mV/µs<br>10 - 1 mV/µs<br>11 - 0.1 mV/µs |

(1) The default value is programmed with 00 for TPS628603

### 8.5.6 STATUS Register

**表 8-7. STATUS Register Description**

| REGISTER ADDRESS 0X05 READ ONLY(1) | | | | |
|---|---|---|---|---|
| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
| 7:5 | Reserved | | | |
| 4 | Thermal Shutdown Tripped | R | 0 | 1: Thermal Shutdown has tripped since the last reading.<br>0: No Thermal Shutdown event occurred during the last reading. |
| 3 | Reserved | | | |
| 2 | Power Bad | R | 0 | 1: Output voltage is or was below 0.95xVO<br>0: No Power Bad event occurred since last reading |
| 1:0 | Reserved | | | |

(1) All bit values are latched until the device is reset, or the STATUS register is read. Then, the STATUS register is reset to its default values.

# 9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

## 9.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

## 9.2 Typical Application, TPS628610

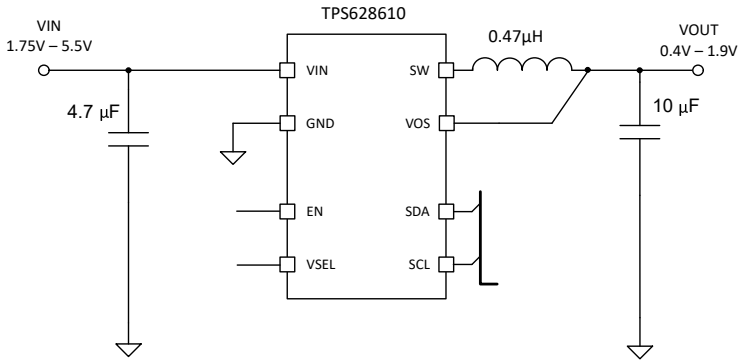



**図 9-1. TPS628610, Typical Application**

### 9.2.1 Design Requirements

表 9-1 shows the list of components for the application circuit and the characteristic application curves.

**表 9-1. Components for Application Characteristic Curves**

| REFERENCE | DESCRIPTION | VALUE | SIZE [L x W X T] | MANUFACTURER(1) |
|---|---|---|---|---|
| TPS628610 | Step down converter, 1 A | | 1.4 mm × 0.70 mm × 0.4 mm maximum | Texas Instruments |
| $C_{IN}$ | Ceramic capacitor, GRM155R60J475ME47D | 4.7 µF | 0402 (1 mm × 0.5 mm × 0.6 mm maximum) | Murata |
| $C_{OUT}$ | Ceramic capacitor, GRM155R60J106ME15D | 10 µF | 0402 (1 mm × 0.5 mm × 0.65 mm maximum) | Murata |
| L | Inductor DFE18SANR47MG0L | 0.47 µH | 0603 (1.6 mm × 0.8 mm × 1.0 mm maximum) | Murata |

(1) See *Third-party Products Disclaimer*.

### 9.2.2 Detailed Design Procedure

#### *9.2.2.1 Inductor Selection*

The inductor value affects the peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple, and the efficiency. The selected inductor has to be rated for its DC resistance and saturation current. The inductor ripple current ($\Delta I_L$) decreases with higher inductance and increases with higher $V_{IN}$ or $V_{OUT}$ and can be estimated according to 式 1.

式 2 calculates the maximum inductor current under static load conditions. The saturation current of the inductor must be rated higher than the maximum inductor current, as calculated with 式 2. This is recommended because during a heavy load transient the inductor current rises above the calculated value. A more conservative way is to select the inductor saturation current according to the high side MOSFET switch current limit, $I_{LIMF}$.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \quad (1)$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (2)$$

where

- f = Switching frequency
- L = Inductor value
- $\Delta I_L$= Peak-to-peak inductor ripple current
- $I_{Lmax}$ = Maximum inductor current

表 9-2 shows a list of possible inductors.

**表 9-2. List of Possible Inductors**

| INDUCTANCE [µH] | INDUCTOR SERIES | SIZE IMPERIAL (METRIC) | DIMENSIONS L × W × T | SUPPLIER(1) |
|---|---|---|---|---|
| 0.47 | DFE18SAN_G0 | 0603 (1608) | 1.6 mm × 0.8 mm × 1.0 mm maximum | Murata |
| 0.47 | HTEB16080F | 0603 (1608) | 1.6 mm × 0.8 mm × 0.6 mm maximum | Cyntec |
| 0.47 | HTET1005FE | 0402 (1005) | 1.0 mm × 0.5 mm × 0.65 mm maximum | Cyntec |
| 0.47 | TFM160808ALC | 0603 (1608) | 1.6 mm × 0.8 mm × 0.8 mm maximum | TDK |

(1) See *Third-party Products Disclaimer*

#### *9.2.2.2 Output Capacitor Selection*

The DCS-Control scheme of the TPS6286x allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. At light-load currents, the converter operates in power save mode and the output voltage ripple is dependent on the output capacitor value. A larger output capacitors can be used reducing the output voltage ripple.

The inductor and output capacitor together provide a low-pass filter. 表 9-3 outlines possible inductor and capacitor value combinations to simplify this process.

**表 9-3. Recommended LC Output Filter Combinations**

| DEVICE | NOMINAL INDUCTOR VALUE (µH) | NOMINAL OUTPUT CAPACITOR VALUE (µF) | | | |
|---|---|---|---|---|---|
| | | 4.7 µF | 10 µF | 2 × 10 µF | 22 µF |
| | 0.47(1) | √ | √(3) | √ | √ |
| TPS62860x | 1.0(2) | √ | √(3) | √ | √ |

(1) TI recommends an effective inductance range of 0.33 µH to 0.82 µH. TI recommends an effective capacitance range of 2 µF to 26 µF.
(2) TI recommends an effective inductance range of 0.7 µH to 1.2 µH. TI recommends an effective capacitance range of 3 µF to 26 µF.
(3) Typical application configuration. Other check marks indicate alternative filter combinations.

#### *9.2.2.3 Input Capacitor Selection*

Because the buck converter has a pulsating input current, a low ESR ceramic input capacitor is required for best input voltage filtering to minimize input voltage spikes. For most applications, a 4.7-µF input capacitor is sufficient. When operating from a high-impedance source (such as a coin cell), TI recommends a larger input buffer capacitor ≥10 µF to avoid voltage drops during start-up and load transients. The input capacitance can be increased without any limit for better input voltage filtering. The leakage current of the input capacitor adds to the overall current consumption.

表 9-4 shows a selection of input and output capacitors.

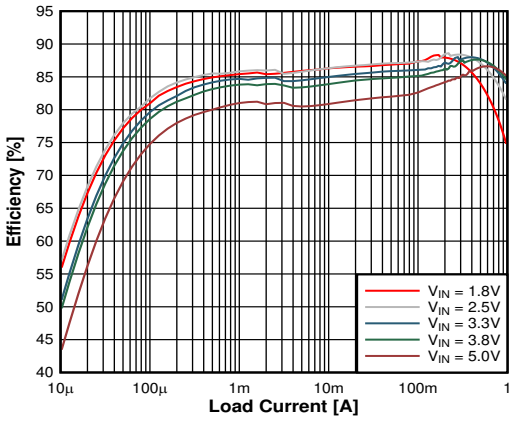
**表 9-4. Capacitor Options**

| CAPACITANCE [µF] | CAPACITOR PART NUMBER | SIZE IMPERIAL (METRIC) | DIMENSIONS L × W × T | SUPPLIER(1) |
|---|---|---|---|---|
| 4.7 | GRM155R60J475ME47D | 0402 (1005) | 1.0 mm × 0.5 mm × 0.6 mm maximum | Murata |
| 4.7 | GRM035R60J475ME15 | 0201 (0603) | 0.6 mm × 0.3 mm × 0.55 mm maximum | Murata |
| 10 | GRM155R60J106ME15D | 0402 (1005) | 1.0 mm × 0.5 mm × 0.65 mm maximum | Murata |

(1) See *Third-party Products Disclaimer*.

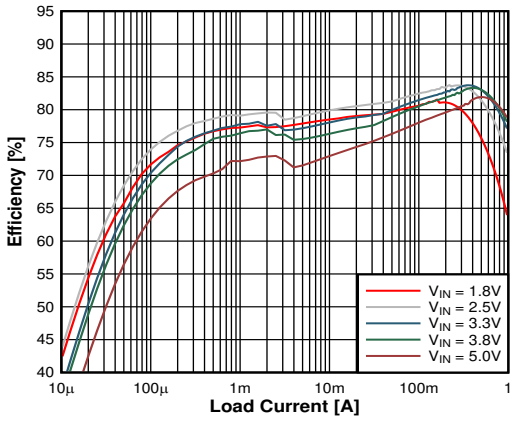
### 9.2.3 Application Curves

$V_{IN}$ = 3.8 V, $V_{OUT}$ = 1.1 V, $T_A$ = 25°C, unless otherwise noted



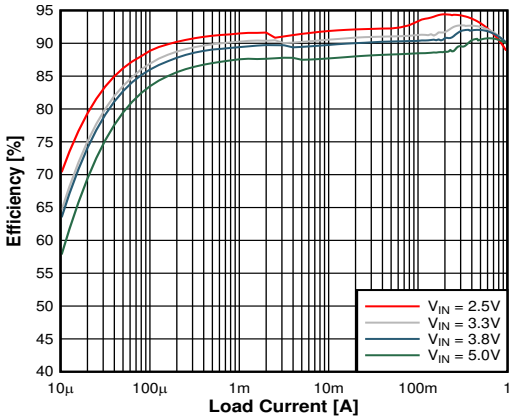

$V_{OUT}$ = 1.1 V Auto Power Save Mode

**図 9-2. Efficiency**



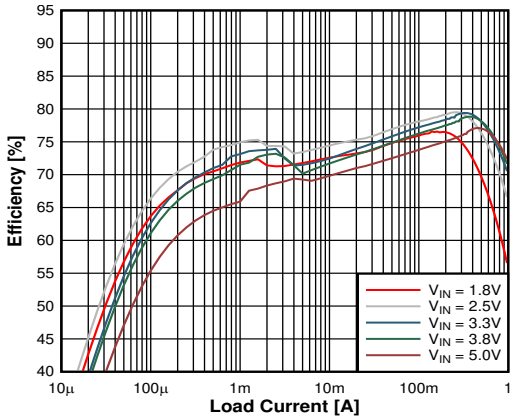

$V_{OUT}$ = 0.6 V Auto Power Save Mode

**図 9-3. Efficiency**



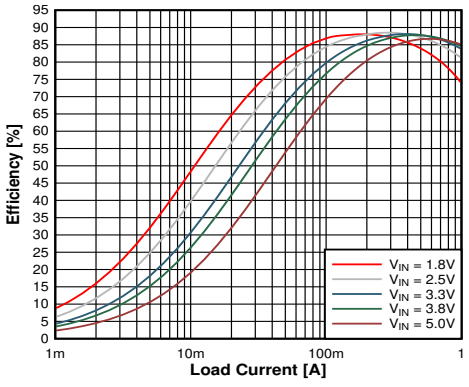

$V_{OUT}$ = 1.9875 V Auto Power Save Mode

**図 9-4. Efficiency**



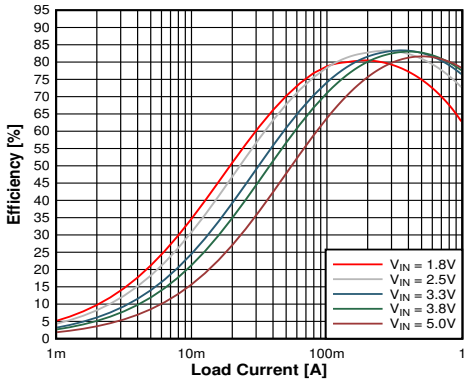

$V_{OUT}$ = 0.4 V Auto Power Save Mode

**図 9-5. Efficiency**



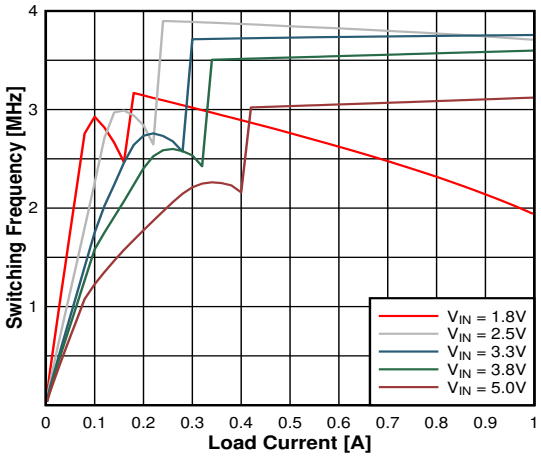

$V_{OUT}$ = 1.1 V Forced PWM Operation

**図 9-6. Efficiency, Inductor Comparison**



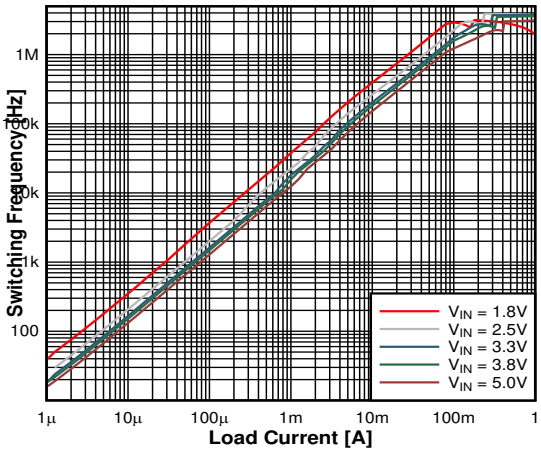

$V_{OUT}$ = 0.6 V Forced PWM operation

**図 9-7. Efficiency**



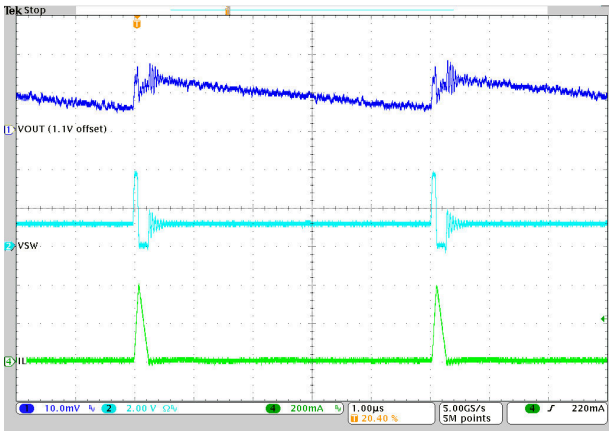

$V_{OUT}$ = 1.1 V Auto Power Save Mode

**図 9-8. Switching Frequency**



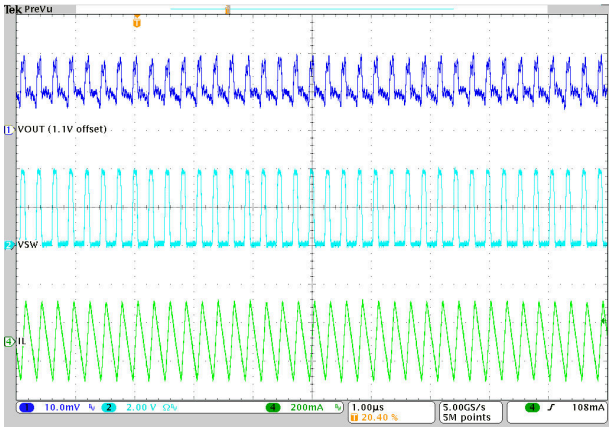

$V_{OUT}$ = 1.1 V

**図 9-9. Switching Frequency**



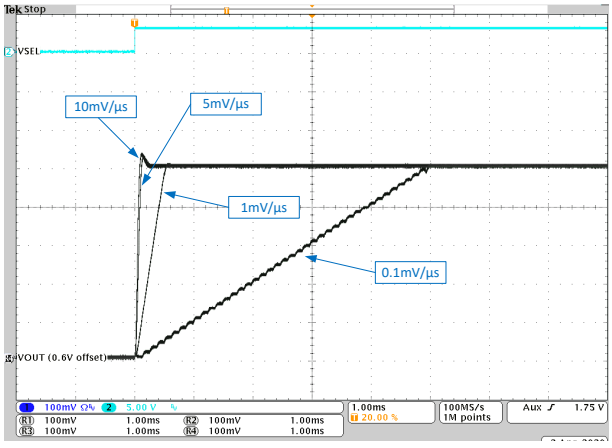

VSEL = HIGH

**図 9-10. PFM Mode Operation**



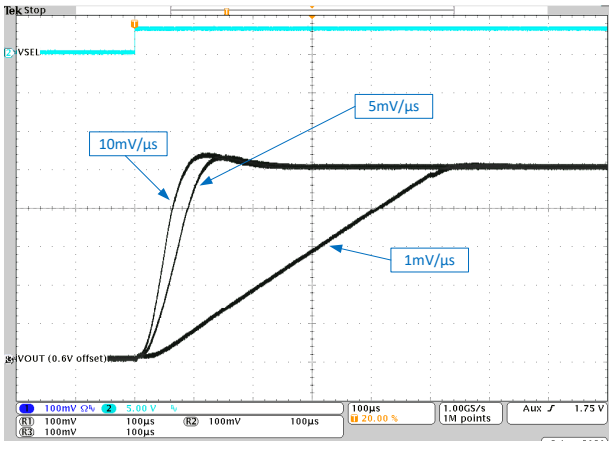

$I_{OUT}$ = 500 mA VSEL = HIGH

**図 9-11. PWM-Mode Operation**



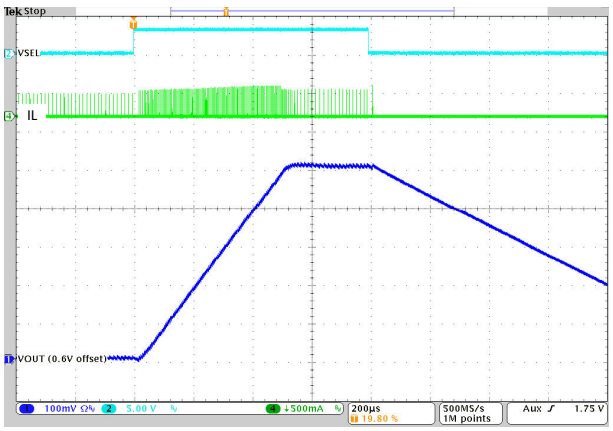

Default voltage setting

**図 9-12. DVS by VSEL, Different Ramp Speed Settings**



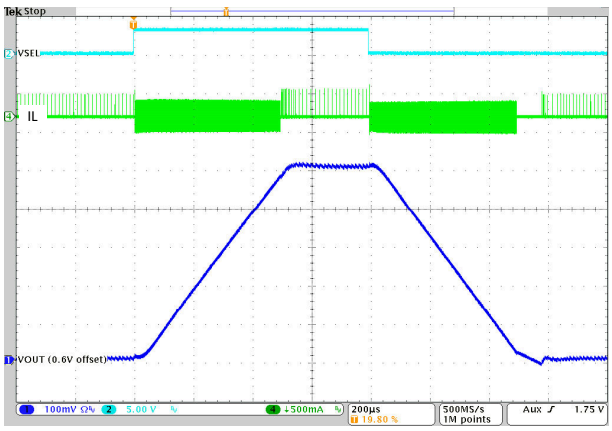

Default voltage setting

**図 9-13. DVS by VSEL, Different Ramp Speed Settings**




Power Save Mode is active

**図 9-14. Standard Operation: $V_{OUT}$ Change**




Power Save Mode is active

**図 9-15. FPWM-Mode During $V_{OUT}$ Change Enabled**

## 9.3 Typical Application, TPS628600, TPS62860x

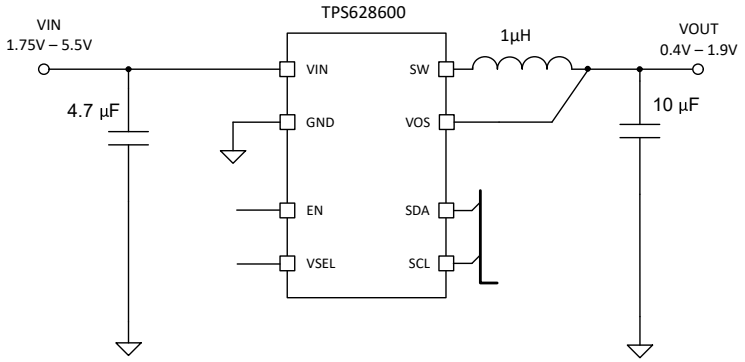



**図 9-16. TPS628600, Typical Application**

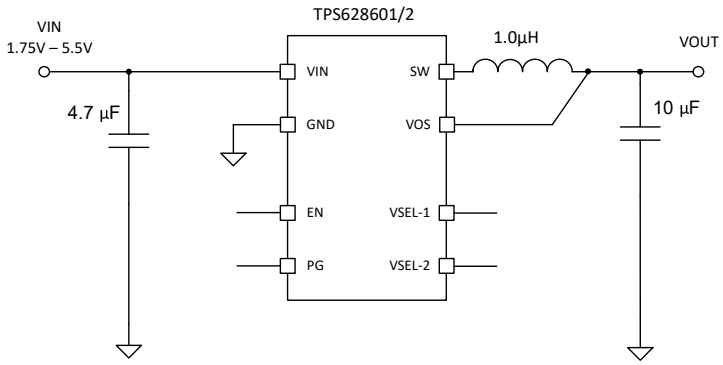



**図 9-17. TPS62860x, Typical Application**

### 9.3.1 Design Requirements

表 9-5 shows the list of components for the application circuit and the characteristic application curves.

**表 9-5. Components for Application Characteristic Curves**

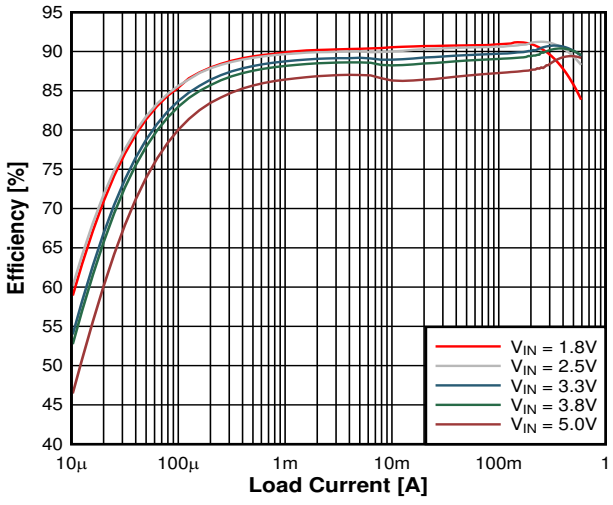
| REFERENCE | DESCRIPTION | VALUE | SIZE [L × W × T] | MANUFACTURER(1) |
|---|---|---|---|---|
| TPS628610 | Step down converter, 1 A | | 1.4 mm × 0.70 mm × 0.4 mm maximum | Texas Instruments |
| $C_{IN}$ | Ceramic capacitor, GRM155R60J475ME47D | 4.7 µF | 0402 (1 mm × 0.5 mm × 0.6 mm maximum) | Murata |
| $C_{OUT}$ | Ceramic capacitor, GRM155R60J106ME15D | 10 µF | 0402 (1 mm × 0.5 mm × 0.65 mm max.) | Murata |
| L | Inductor DFE201610E | 1 µH | 0805 (2.0 mm × 1.6 mm × 1.0 mm max.) | Murata |

(1) See *Third-party Products Disclaimer*.

### 9.3.2 Detailed Design Procedure

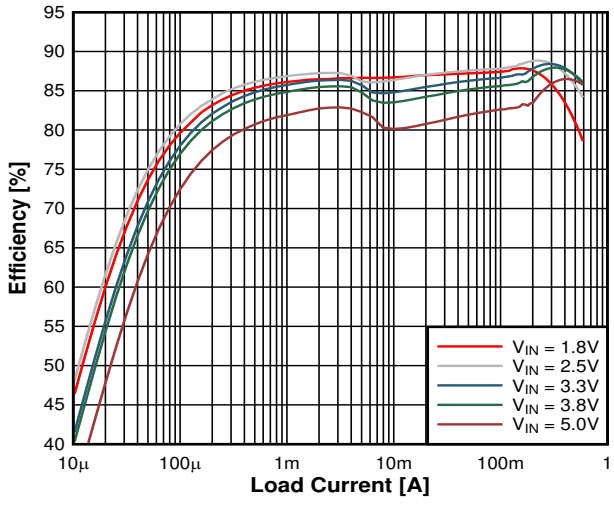
See *セクション 9.2.2*.

### 9.3.3 Application Curves




$V_{OUT}$ = 1.1 V Auto Power Save Mode

**図 9-18. Efficiency**




$V_{OUT}$ = 0.7 V Auto Power Save Mode

**図 9-19. Efficiency**

## 9.4 Power Supply Recommendations

The power supply must provide a current rating according to the supply voltage, output voltage, and output current of the TPS6286x.

## 9.5 Layout

### 9.5.1 Layout Guidelines

The pinout of the TPS6286x converter has been optimized to enable a single top layer PCB routing of the converter and its critical passive components such as CIN, COUT, and L. This pinout allows the connection of tiny components such as 0201 (0603) size capacitors and 0402 (1005) size inductor. A design size smaller than 5 $mm^2$ can be achieved with a fixed output voltage.

- As for all switching power supplies, the layout is an important step in the design. A specified performance requires the correct on board layout.
- Provide a low inductance, low impedance ground path. Therefore, use wide and short traces for the main current paths.
- Place the input capacitor as close as possible to the VIN and GND pins of the converter. This is the most critical component placement.
- The VOS line is a sensitive, high impedance line and must be connected to the output capacitor and routed away from noisy components and traces (for example, SW line) or other noise sources.

### 9.5.2 Layout Example

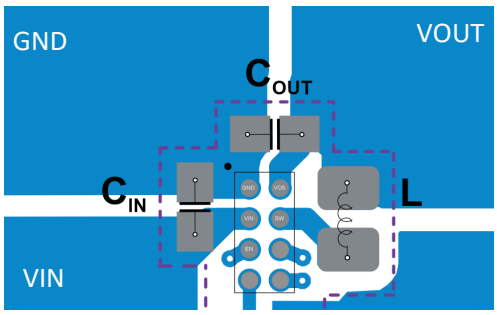



**図 9-20. PCB Layout Example**

# 10 Device and Documentation Support

## 10.1 Device Support

### 10.1.1 サード・パーティ製品に関する免責事項

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## 10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

## 10.3 サポート・リソース

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リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

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テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
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この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

## 10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS628600YCHR | ACTIVE | DSBGA | YCH | 8 | 12000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | S | Samples |
| TPS628601YCHR | ACTIVE | DSBGA | YCH | 8 | 12000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | T | Samples |
| TPS628603YCHR | ACTIVE | DSBGA | YCH | 8 | 12000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | Q | Samples |
| TPS628604YCHR | ACTIVE | DSBGA | YCH | 8 | 12000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | Q | Samples |
| TPS628610YCHR | ACTIVE | DSBGA | YCH | 8 | 12000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | U | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

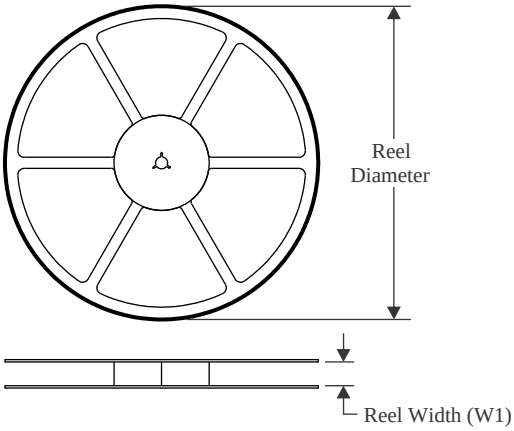
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

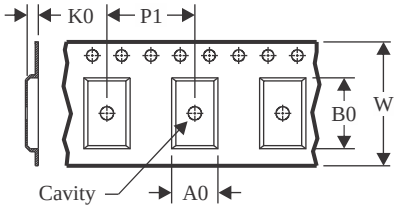
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

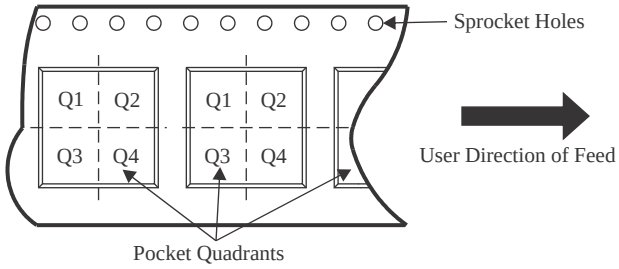



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

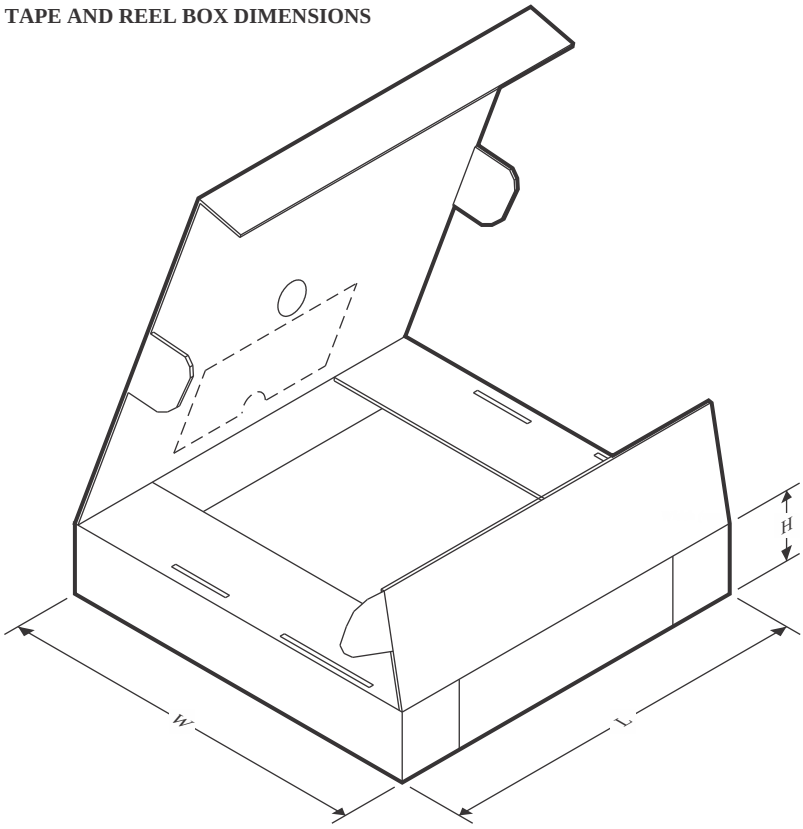
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS628600YCHR | DSBGA | YCH | 8 | 12000 | 180.0 | 8.4 | 0.81 | 1.53 | 0.43 | 2.0 | 8.0 | Q1 |
| TPS628601YCHR | DSBGA | YCH | 8 | 12000 | 180.0 | 8.4 | 0.81 | 1.53 | 0.43 | 2.0 | 8.0 | Q1 |
| TPS628603YCHR | DSBGA | YCH | 8 | 12000 | 180.0 | 8.4 | 0.81 | 1.53 | 0.43 | 2.0 | 8.0 | Q1 |
| TPS628604YCHR | DSBGA | YCH | 8 | 12000 | 180.0 | 8.4 | 0.81 | 1.53 | 0.43 | 2.0 | 8.0 | Q1 |
| TPS628610YCHR | DSBGA | YCH | 8 | 12000 | 180.0 | 8.4 | 0.81 | 1.53 | 0.43 | 2.0 | 8.0 | Q1 |

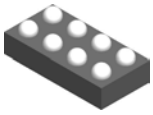
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS628600YCHR | DSBGA | YCH | 8 | 12000 | 182.0 | 182.0 | 20.0 |
| TPS628601YCHR | DSBGA | YCH | 8 | 12000 | 182.0 | 182.0 | 20.0 |
| TPS628603YCHR | DSBGA | YCH | 8 | 12000 | 182.0 | 182.0 | 20.0 |
| TPS628604YCHR | DSBGA | YCH | 8 | 12000 | 182.0 | 182.0 | 20.0 |
| TPS628610YCHR | DSBGA | YCH | 8 | 12000 | 182.0 | 182.0 | 20.0 |

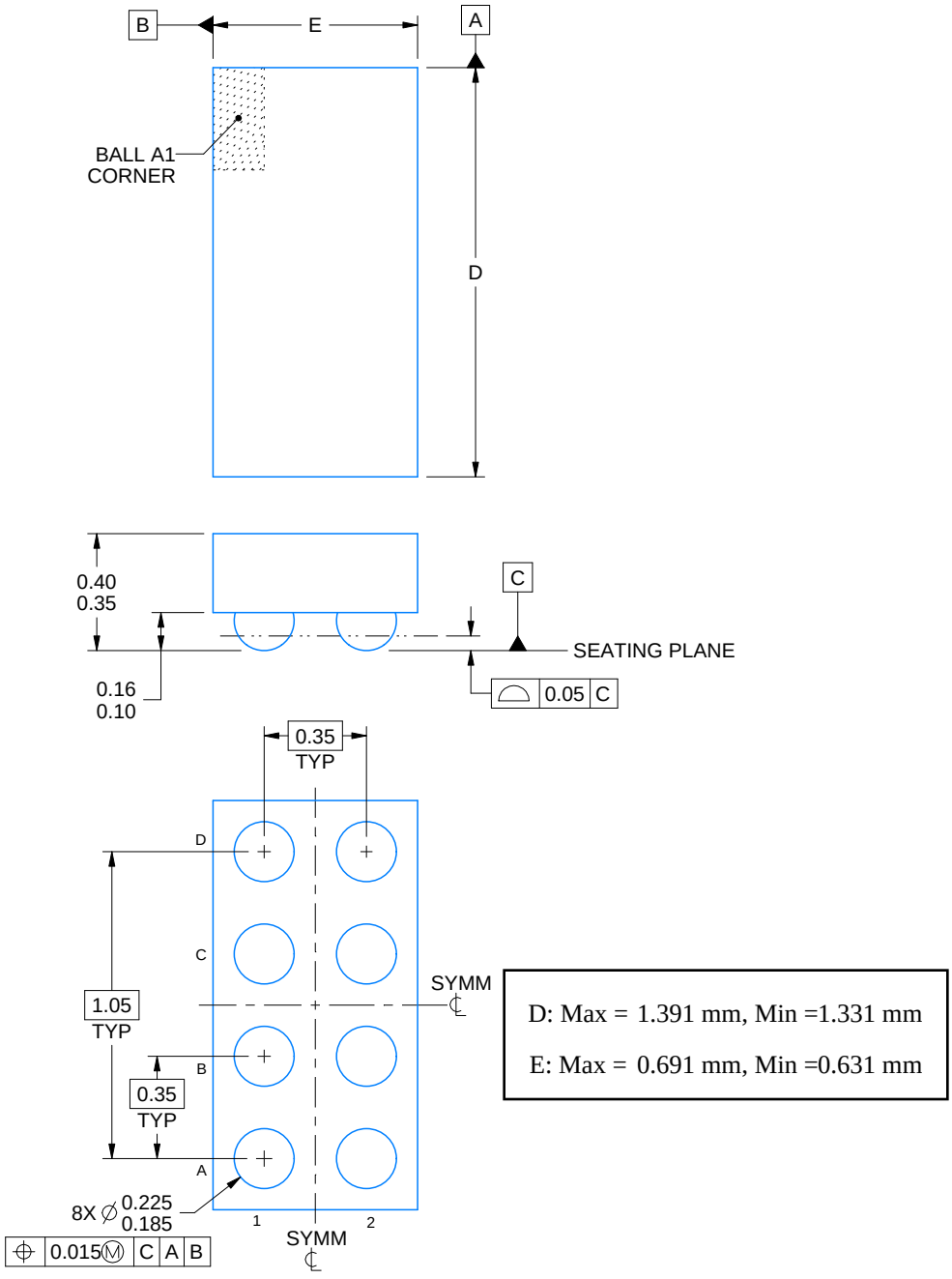
# YCH0008



# PACKAGE OUTLINE

## DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY

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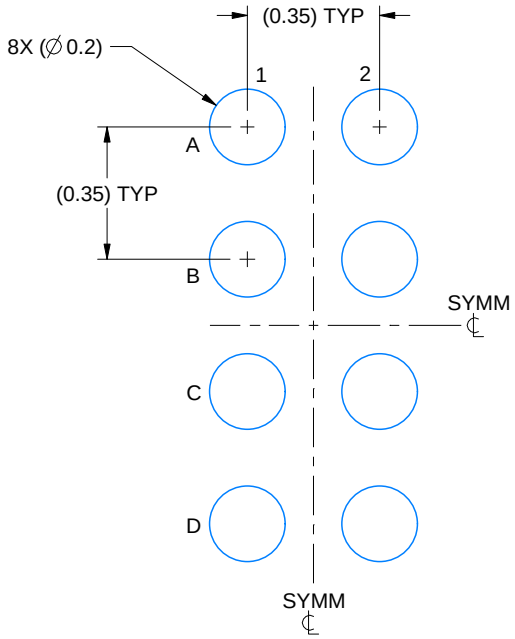
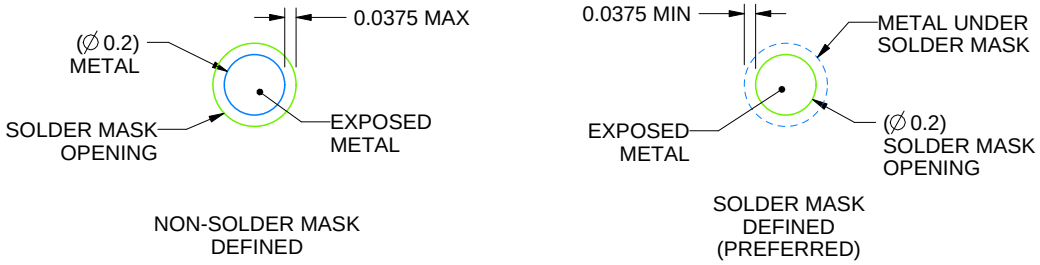
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X




SOLDER MASK DETAILS
NOT TO SCALE

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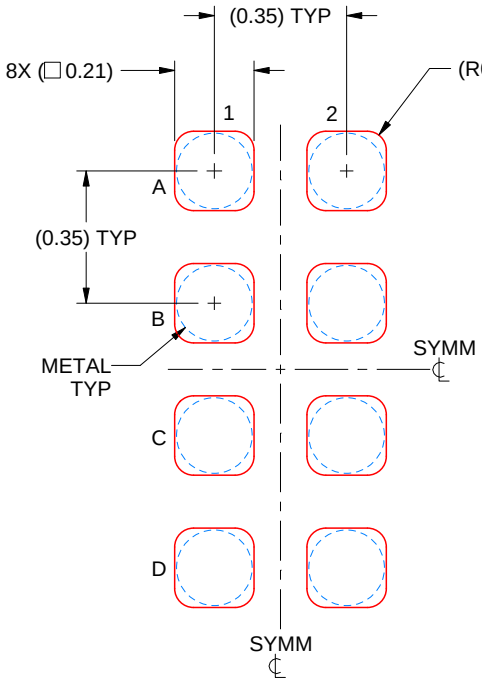
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).




SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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