TPS6287x-Q1 2.7V～6V 入力、15A、20A、25A、および 30A、車載用高速過渡同期整流式降圧コンバータ、I²C インターフェイス付き

1 特長

- 車載アプリケーション向けに AEC-Q100 認証済み
  - デバイス温度グレード 1:–40℃～125℃ T_A
  - 接合部温度範囲:-40℃～150℃
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 入力電圧範囲:2.7V～6V
- ピン互換性のあるデバイス ファミリ:15A、20A、25A、30A
- 3 つの選択可能な出力電圧範囲:0.4V～1.675V
  - 0.4V～0.71875V (1.25mV 刻み)
  - 0.4V～1.0375V (2.5mV 刻み)
  - 0.4V～1.675V (5mV 刻み)
- 出力電圧精度:±0.8%
- 内部電力 MOSFET:2.6mΩ、1.5mΩ
- 可変ソフト スタート
- 外部補償
- VSEL ピンを介してスタートアップ出力電圧を選択可能
- FSEL ピンを介して 1.5MHz、2.25MHz、2.5MHz、3MHz のスイッチング周波数を選択可能
- 強制 PWM またはパワー セーブ モード動作
- 外部抵抗または I²C によるスタートアップ出力電圧の選択
- I²C 互換インターフェイス:最高 3.4MHz
- オプションのスタック動作により、出力電流能力を向上
- 差動リモート センス
- サーマル事前警告およびサーマル シャットダウン
- 出力放電
- オプションのスペクトラム拡散クロック供給機能を内蔵
- ウィンドウ コンパレータによるパワー グッド出力

2 アプリケーション

- ADAS カメラ、ADAS センサ フュージョン
- サラウンド ビュー ECU
- ハイブリッドおよび再構成可能クラスタ
- ヘッド ユニット、テレマティクス制御ユニット

3 概要

TPS62874-Q1、TPS62875-Q1、TPS62876-Q1、および TPS62877-Q1 TPS6287B10-Q1 、TPS6287B15-Q1 、TPS6287B20、および TPS6287B30 は、I²C インターフェイスおよび差動リモート センスを搭載したピン互換、15A、20A、25A、30A 同期整流式降圧 DC/DC コンバータのファミリです。すべてのデバイスは、高い効率と使いやすさを特長としています。低抵抗の電源スイッチにより、高い周囲温度でも最大 30A の出力電流を供給できます。これらのデバイスをスタック モードで動作させることで、大きな出力電流を供給することや、消費電力を複数のデバイスに分散することが可能です。

TPS6287x-Q1 ファミリは、固定周波数動作での高速過渡応答を組み合わせた拡張 DCS 制御方式を実装しています。デバイスは、最大効率を達成するパワー セーブ モード、または最高の過渡性能と最小の出力電圧リップルを実現する強制 PWM モードで動作できます。

オプションのリモート センシング機能により、ポイント オブ ロードでの電圧レギュレーションが最大化され、デバイスは出力電圧範囲全体にわたって ±0.8% の DC 電圧精度を達成します。

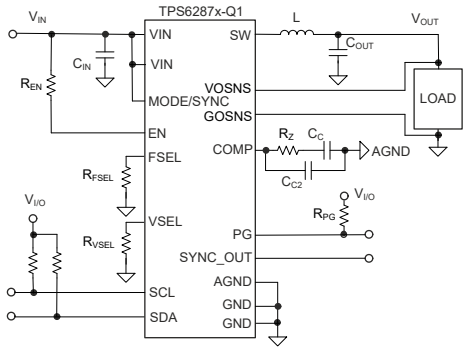
スイッチング周波数は FSEL ピンを介して選択可能であり、1.5MHz、2.25MHz、2.5MHz、3MHz のいずれかに設定する、または同じ周波数範囲の外部クロックに同期させることができます。

I²C 互換インターフェイスを使うと、各種の制御、監視、警告機能 (電圧の監視、温度に関連する警告など) を実現できます。出力電圧は、負荷の消費電力を性能ニーズに合わせて迅速に調整できます。デフォルトの起動電圧は、VSEL ピンを介して抵抗により選択できます。

製品情報

部品番号(2)	電流定格	パッケージ(1)
TPS62874-Q1	15A	RZV (WQFN、24) 4.05mm × 3.05mm
TPS62875-Q1	20A	
TPS62876-Q1	25A	
TPS62877-Q1	30A	

(1) 詳細については、セクション 13 を参照してください。
(2) デバイスのオプションの表を参照してください。



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4 Device Options

DEVICE NUMBER	OUTPUT CURRENT	VSEL SETTING FOR START-UP VOLTAGE AND I2C ADDRESS	SSC	DEFAULT DROOP	TRANS. NONSYNC MODE	SOFT-START TIME
TPS62874QWRZVRQ1	15A	VSEL with 6.2kΩ to GND: 0.80V, 0x44 VSEL shorted to GND: 0.75V, 0x45 VSEL shorted to VIN: 0.875V, 0x46 VSEL with 47kΩ to VIN: 0.58V, 0x47	Off	Off	Off	1ms
TPS62875QWRZVRQ1	20A		Off	Off	Off	
TPS62876QWRZVRQ1	25A		Off	Off	Off	
TPS62877QWRZVRQ1	30A		Off	Off	Off	
TPS62874B1QWRZVRQ1	15A	VSEL with 6.2kΩ to GND: 0.8V, 0x44 VSEL shorted to GND: 0.8V, 0x45 VSEL shorted to VIN: 0.875V, 0x46 VSEL with 47kΩ to VIN: 0.8V, 0x47	Off	On	On	
TPS62875B1QWRZVRQ1	20A		Off	On	On	
TPS62876B1QWRZVRQ1	25A		Off	On	On	
TPS62877B1QWRZVRQ1	30A		Off	On	On	
TPS62875B2QWRZVRQ1	20A	VSEL with 6.2kΩ to GND: 0.85V, 0x44 VSEL shorted to GND: 0.75V, 0x45 VSEL shorted to VIN: 0.875V, 0x46 VSEL with 47kΩ to VIN: 0.8V, 0x47	Off	On	On	
TPS62875B3QWRZVRQ1	20A	VSEL with 6.2kΩ to GND: 0.73V, 0x44 VSEL shorted to GND: 0.75V, 0x45 VSEL shorted to VIN: 0.8V, 0x46 VSEL with 47kΩ to VIN: 0.77V, 0x47	On	On	On	
TPS62876B3QWRZVRQ1	25A	VSEL with 6.2kΩ to GND: 0.845V, 0x44 VSEL shorted to GND: 0.75V, 0x45 VSEL shorted to VIN: 0.8V, 0x46 VSEL with 47kΩ to VIN: 0.9V, 0x47	On	On	On	
TPS62877B3QWRZVRQ1 (1)	30A		On	On	On	
TPS62874B4QWRZVRQ1	15A	VSEL with 6.2kΩ to GND: 0.7V, 0x44 VSEL shorted to GND: 0.75V, 0x45 VSEL shorted to VIN: 0.765V, 0x46 VSEL with 47kΩ to VIN: 0.85V, 0x47	Off	On	On	
TPS62875B4QWRZVRQ1	20A		Off	On	On	
TPS62875B5QWRZVRQ1	20A	VSEL with 6.2kΩ to GND: 0.725V, 0x44 VSEL shorted to GND: 0.75V, 0x45 VSEL shorted to VIN: 0.765V, 0x46 VSEL with 47kΩ to VIN: 0.85V, 0x47	Off	On	On	

(1) Preview information (not Production Data)

5 Pin Configuration and Functions

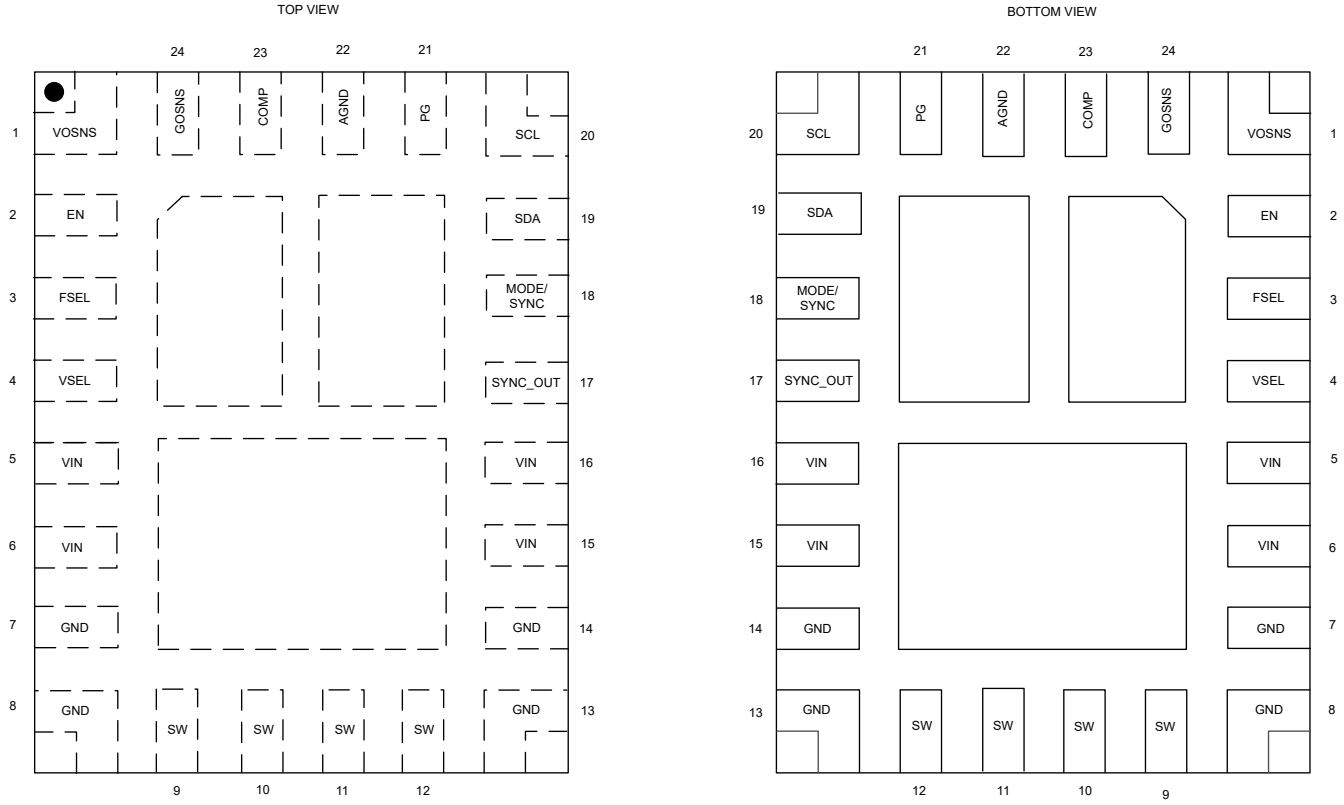


図 5-1. RZV Package 24 Pin WQFN

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	VOSNS	I	Output voltage sense (differential output voltage sensing).
2	EN	I	This pin is the enable pin of the device. Connect to this pin using a series resistor of at least 15kΩ. A logic low level on this pin disables the device, and a logic high level on the pin enables the device. Do not leave this pin unconnected. For stacked operation interconnect EN pins of all stacked devices with a resistor to the supply voltage or a GPIO of a processor. See *Stacked Operation* for a detailed description.
3	FSEL	I	Frequency select pin. A resistor or a short circuit to GND or V_{IN} determines the switching frequency if not externally synchronized. See セクション 8.3.6 for the frequency options.
4	VSEL	I	Start-up output voltage set pin. A resistor or short circuit to GND or V_{IN} defines the selected output voltage.
5, 6, 15, 16	VIN	P	Power supply input. Connect the input capacitor as close as possible between pin VIN and GND.
7, 8, 13, 14	GND	GND	Ground pin
9, 10, 11, 12	SW	O	This is the switch pin of the converter and is connected to the internal Power MOSFETs.

表 5-1. Pin Functions (続き)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
17	SYNCOUT	O	Internal clock output pin for synchronization in stacked mode. Leave this pin floating for single device operation. Connect this pin to the MODE/SYNC pin of the successing device in the daisy-chain in stacked operation. Do not use this pin to connect to a non-TPS6287x-Q1 device. During start-up, this pin is used to identify if a device must operate as a secondary converter in stacked operation. Connect a 47kΩ resistor from this pin to GND to define a secondary converter in stacked operation. See *Stacked Operation* for a detailed description.
18	MODE/SYNC	I	The device runs in Power-Save mode when this pin is pulled low. If the pin is pulled high, the device runs in Forced-PWM mode. Do not leave this pin unconnected. The mode pin can also be used to synchronize the device to an external clock.
19	SDA	I/O	I^2C serial data pin. Do not leave this pin floating. Connect a pullup to logic high level. Connect to GND for secondary devices in stacked operation.
20	SCL	I/O	I^2C serial clock pin. Do not leave this pin floating. Connect a pullup resistor to a logic high level. Connect to GND for secondary devices in stacked operation.
21	PG	I/O	Open drain power good output. Low impedance when not "power good", high impedance when "power good". This pin can be left open or be tied to GND when not used in single device operation. In stacked operation interconnect the PG pins of all stacked devices. Only the PG pin of the primary converter in stacked operation is an open drain output. For devices that are defined as secondary converters in stacked mode the pin is an input pin. See *Stacked Operation* for a detailed description.
22	AGND	GND	Analog Ground. Connect to GND.
23	COMP	—	Device compensation input. A resistor and capacitor from this pin to AGND define the compensation of the control loop. In stacked operation connect the COMP pins of all stacked devices together and connect a resistor and capacitor between the common COMP node and AGND.
24	GOSNS	I	Output ground sense (differential output voltage sensing)
Exposed Thermal Pads		—	The thermal pads must be soldered to GND to achieve an appropriate thermal resistance and for mechanical stability.

(1) I = input, O = output, P = power, GND = ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	VIN(4)	–0.3	6.5	V
	SW (DC)	–0.3	V_{IN} + 0.3	V
	COMP	–0.3	V_{IN}	V
	SW (AC, less than 10ns)(3)	–3	10	V
	VOSNS	–0.3	1.8	V
Voltage(2)	SCL, SDA	–0.3	5.5	V
Voltage(2)	SYNC_OUT	–0.3	2	V
Voltage(2)	PG	–0.3	6.5	V
Voltage(2)	FSEL, VSEL, EN, MODE/SYNC(4)	–0.3	6.5	V
Voltage(2)	GOSNS	–0.3	0.3	V
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the network ground terminal.
(3) While switching.
(4) The voltage at the pin can exceed the 6.5V absolute max condition for a short period of time, but must remain less than 8V. VIN at 8V for a 100ms duration is equivalent to approximately 8 hours of aging for the device at room temperature.

6.2 ESD Ratings - Q100

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1) HBM ESD classification level 2		±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM) per AEC Q100-011 CDM ESD classification level C5		±750	V

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.7		6	V
V_{OUT}	Output voltage range	0.4		1.675 V or (V_{IN} – 1.5 V)(1)	V
Voltage	Nominal pull-up voltage on pins SDA and SCL	1.2		5	V
L	Effective inductance for f_{SW} = 1.5MHz	100	150	200	nH
L	Effective inductance for f_{SW} = 2.25MHz, 2.5MHz and 3MHz	40	100	200	nH
C_{IN}	Effective input capacitance per power input pin	10	22		µF
C_{OUT}	Effective output capacitance	47		(3)	µF
C_{PAR}	Parasitic capacitance on FSEL, VSEL pin			100	pF
C_{PAR}	Parasitic capacitance on SYNC_OUT pin			20	pF
R_{EN}	Pull-up resistance on EN pin	15			kΩ
R_{VSEL}, R_{FSEL}	Resistance on VSEL, VSEL to GND if not directly tied to GND or VIN		6.2		kΩ

6.3 Recommended Operating Conditions (続き)

Over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
R_{VSEL}, R_{FSEL}	Resistance on VSEL, VSEL to VIN if not directly tied to GND or VIN		47		kΩ
R_{VSEL}, R_{FSEL}	Resistor tolerance on VSEL, FSEL			± 2%	
I_{SINK_PG}	Sink current at PG pin	0		1	mA
T_J	Operating junction temperature (2)	–40		150	°C

(1) Whatever V_{OUT} value is lower.
(2) Operating lifetime is derated at junction temperatures greater than 125°C.
(3) The maximum recommended output capacitance depends on the specific operating conditions of an application. Output capacitance values of up to a few millifarads are typically possible.

6.4 Thermal Information

THERMAL METRIC(1)		TPS6287x-Q1 RZV (JEDEC) 24 PINS	TPS6287x-Q1 RZV (EVM) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.7	28	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.9	-	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.5	-	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.5	-	°C/W
Y_{JB}	Junction-to-board characterization parameter	6.5	-	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.8	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics

over operating junction temperature (T_J = –40 °C to +150 °C) and V_{IN} = 2.7 V to 6 V. Typical values at V_{IN} = 5 V and T_J = 25 °C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current	EN = High, I_{OUT} = 0mA, device not switching; MODE = Low		2.1	3.8	mA
I_{SD}	Shutdown current	EN = Low, $V_{(SW)}$ = 0 V, max value at T_J = 125°C		18	450	µA
$V_{IT+(UVLO)}$	Positive-going UVLO threshold voltage (VIN)		2.5	2.6	2.7	V
$V_{IT-(UVLO)}$	Negative-going UVLO threshold voltage (VIN)		2.4	2.5	2.6	V
$V_{hys(UVLO)}$	UVLO hysteresis voltage (VIN)		80			mV
$V_{IT+(OVLO)}$	Positive-going OVLO threshold voltage (VIN)		6.1	6.3	6.5	V
$V_{IT-(OVLO)}$	Negative-going OVLO threshold voltage (VIN)		6.0	6.2	6.4	V
$V_{hys(OVLO)}$	OVLO hysteresis voltage (VIN)		80			mV
$V_{IT-(POR)}$	Negative-going power-on reset threshold voltage (VIN)		1.4			V
T_{SD}	Thermal shutdown threshold temperature	T_J rising		170		°C
	Thermal shutdown hysteresis			20		°C

6.5 Electrical Characteristics (続き)

over operating junction temperature (T_J = –40 °C to +150 °C) and V_{IN} = 2.7 V to 6 V. Typical values at V_{IN} = 5 V and T_J = 25 °C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_W	Thermal warning threshold temperature	T_J rising		150		°C
	Thermal warning hysteresis			20		°C
CONTROL and INTERFACE						
V_{IT+}	Positive-going input threshold voltage (EN)		0.97	1.0	1.03	V
V_{IT-}	Negative-going input threshold voltage (EN)		0.87	0.9	0.93	V
V_{hys}	Hysteresis voltage (EN)		95			mV
$R_{(EN)}$	Input resistance to GND (EN)	Only active during start-up in stacked operation.	1.4	1.8	3	kΩ
I_{IH}	High-level input current (EN)	V_{IH} = V_{IN}, internal pulldown resistor disabled			3	µA
I_{IL}	Low-level input current (EN)	V_{IL} = 0V, internal pulldown resistor disabled	–200			nA
V_{IH}	High-level input voltage (MODE/SYNC, VSEL, FSEL, SYNC_OUT, PG)		0.8			V
V_{IH}	High-level input voltage (SDA, SCL)		0.95			V
V_{IL}	Low-level input voltage (MODE/SYNC, VSEL, FSEL, SYNC_OUT, PG)				0.4	V
V_{IL}	Low-level input voltage (SDA, SCL)				0.5	V
R_{IN}	Input resistance to GND on pins MODE/SYNC, EN and PG		2	3	4	MΩ
V_{OL}	Low-level output voltage (SDA)	I_{OL} = 9mA			0.4	V
V_{OL}	Low-level output voltage (SDA)	I_{OL} = 5mA			0.2	V
I_{LKG}	Input leakage current into SDA, SCL	V_{OH} = 3.3V			200	nA
I_{IL}	Low-level input current (MODE/SYNC)	V_{IL} = 0V	–100		100	nA
I_{IH}	High-level input current (MODE/SYNC)	V_{IH} = V_{IN}			3	µA
I_{IL}	Low-level input current (SYNC_OUT)	V_{IL} = 0V	–230			nA
I_{IH}	High-level input current (SYNC_OUT)	V_{IH} = 2V			110	nA
V_{OL}	Low-level output voltage (SYNC_OUT)	I_{OL} = 1mA			0.3	V
V_{OH}	High-level output voltage (SYNC_OUT)	I_{OH} = 0.1mA	1.3		2.1	V
$t_{d(EN)1}$	Enable delay time when EN tied to V_{IN}	Measured from when EN goes high to when device starts switching, SR_{VIN} = 1V/µs		200	600	µs
$t_{d(EN)2}$	Enable delay time when V_{IN} already applied	Measured from when EN goes high to when device starts switching		40	100	µs
$td_{(Ramp)}$	Output voltage ramp time for CONTROL2[1:0] = 00	Measured from when device starts switching to rising edge of PG	0.35	0.5	0.65	ms
	Output voltage ramp time for CONTROL2[1:0] = 01		0.54	0.77	1.0	ms
	Output voltage ramp time for CONTROL2[1:0] = 10, default		0.7	1	1.3	ms
	Output voltage ramp time for CONTROL2[1:0] = 11		1.4	2	2.6	ms
$f_{(SYNC)}$	Synchronization clock frequency range (MODE/SYNC)	$f_{(SW)nom}$ = 1.5MHz, $D_{(MODE/SYNC)}$ = 45%...55%	1.2		1.8	MHz
	Synchronization clock frequency range (MODE/SYNC)	$f_{(SW)nom}$ = 2.25MHz, $D_{(MODE/SYNC)}$ = 45%...55%	1.8		2.7	MHz

6.5 Electrical Characteristics (続き)

over operating junction temperature (T_J = –40 °C to +150 °C) and V_{IN} = 2.7 V to 6 V. Typical values at V_{IN} = 5 V and T_J = 25 °C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Synchronization clock frequency range (MODE/SYNC)	$f_{(SW)nom}$ = 2.5MHz, $D_{(MODE/SYNC)}$ = 45%...55%	2		3.0	MHz
$f_{(SYNC)}$	Synchronization clock frequency range (MODE/SYNC)	$f_{(SW)nom}$ = 3MHz, $D_{(MODE/SYNC)}$ = 45%...55%	2.4		3.3	MHz
$D_{(MODE/SYNC)}$	Duty cycle of synchronization clock frequency (MODE/SYNC)		45		55	%
	Phase shift at SYNC_OUT with reference to internal CLK or external CLK	CONTROL2:SYNCH_OUT_PHASE = 0b0		120		°
	Phase shift at SYNC_OUT with reference to internal CLK or external CLK	CONTROL2:SYNCH_OUT_PHASE = 0b1		180		°
	Time to lock to external frequency			50		µs
	Resistance on FSEL, VSEL to GND if not tied to GND directly			6.2		kΩ
	Resistance on FSEL, VSEL to VIN if not tied to VIN directly			47		kΩ
$V_{T+(UVP)}$	Positive-going power good threshold voltage (output undervoltage)		94	96	98	%
$V_{T-(UVP)}$	Negative-going power good threshold voltage (output undervoltage)		92	94	96	%
$V_{T+(OVP)}$	Positive-going power good threshold voltage (output overvoltage)		104	106	108	%
$V_{T-(OVP)}$	Negative-going power good threshold voltage (output overvoltage)		102	104	106	%
V_{OL}	Low-level output voltage (PG)	I_{OL} = 1mA		0.012	0.3	V
I_{OH}	High-level output current (PG)	V_{OH} = 5V			3	µA
I_{IH}	High-level input current (PG)	Device configured as secondary device in stacked operation			3	µA
I_{IL}	Low-level input current (PG)	Device configured as secondary device in stacked operation	–1			µA
$t_{d(PG)}$	Deglitch time (PG)	High-to-low or low-to-high transition on the PG pin	34	40	46	µs
OUTPUT						
ΔV_{OUT}	Output voltage accuracy	$V_{IN} \geq V_{OUT}$ + 1.6V, droop compensation disabled	–0.8		0.8	%
ΔV_{OUT}	Output voltage change from no current to rated current	droop compensation enabled		±12		mV
	Accuracy of droop compensation voltage; TPS62874-Q1	device in forced PWM mode	–3.75		3.75	mV
	Accuracy of droop compensation voltage; TPS62875-Q1	device in forced PWM mode	–3.5		3.5	mV
	Accuracy of droop compensation voltage; TPS62876-Q1 and TPS62877-Q1	device in forced PWM mode	–3		3	mV
	Line regulation	I_{OUT} = 15A, $V_{IN} \geq V_{OUT}$ + 1.6V		0.02		%/V
I_{IB}	Input bias current (GOSNS)	EN = High; $V_{(GOSNS)}$ = –100mV to 100mV	–60		3	µA
I_{IB}	Input bias current (VOSNS)	$V_{(VOSNS)}$ = 1.675 V, V_{IN} = 6V, droop compensation disabled	–5.5		5.5	µA
I_{IB}	Input bias current (VOSNS)	$V_{(VOSNS)}$ = 1.675V, V_{IN} = 6V, droop compensation enabled	–13.2		13.2	µA
V_{ICR}	Input common-mode range (GOSNS)		–100		100	mV

6.5 Electrical Characteristics (続き)

over operating junction temperature (T_J = –40 °C to +150 °C) and V_{IN} = 2.7 V to 6 V. Typical values at V_{IN} = 5 V and T_J = 25 °C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{DIS}	Output discharge resistance	V_{OUT} ≤ 1V		2.7	9.2	Ω
f_{SW}	Switching frequency (SW)	f_{SW} = 1.5MHz, PWM operation	1.35	1.5	1.65	MHz
		f_{SW} = 2.25MHz, PWM operation	2.025	2.25	2.475	MHz
		f_{SW} = 2.5MHz, PWM operation	2.25	2.5	2.75	MHz
		f_{SW} = 3MHz, PWM operation	2.7	3	3.3	MHz
f_{SSC}	Modulation frequency			fsw/2048		kHz
Δf_{SW}	Switching frequency variation during spread spectrum operation		f_{SW}–10%		f_{SW}+10%	
gm	Transconductance of OTA on COMP pin			1.5		mS
τ	Emulated current time constant		11.87	12.5	13.2	µs
$R_{DS(ON)}$	High-side FET static on-resistance	V_{IN} = 3.3V		3.4	6.4	mΩ
$R_{DS(ON)}$	Low-side FET static on-resistance	V_{IN} = 3.3V		1.9	3.6	mΩ
$I_{(SW)(off)}$	SW pin current when HS-FET and LS-FET are off	V_{IN} = 6V; $V_{(SW)}$ = 0V, T_J = 25°C	–1.5		0.1	µA
	SW pin current when HS-FET and LS-FET are off	V_{IN} = 6V; $V_{(SW)}$ = 6V, T_J = 25°C	60		130	µA
	SW pin current when HS-FET and LS-FET are off	$V_{(SW)}$ = 0.4V, current into SW pin		11	3000	µA
ILIM	High-side FET forward switch current limit, DC	TPS62874-Q1	19	22.5	26	A
ILIM	High-side FET forward switch current limit, DC	TPS62875-Q1	24	28.5	32	A
ILIM	High-side FET forward switch current limit, DC	TPS62876-Q1	29	34	39	A
ILIM	High-side FET forward switch current limit, DC	TPS62877-Q1	34	39	44	A
ILIM	Low-side FET forward switch current limit, DC	TPS62874-Q1	15	20	24	A
ILIM	Low-side FET forward switch current limit, DC	TPS62875-Q1	20	24.5	29	A
ILIM	Low-side FET forward switch current limit, DC	TPS62876-Q1	24.5	29	33	A
ILIM	Low-side FET forward switch current limit, DC	TPS62877-Q1	29.5	33.5	38	A
ILIM	Low-side FET negative current limit, DC			–10		A
$t_{on, min}$	Minimum on-time of HS FET	V_{IN} = 3.3V		45	53	ns
$t_{on, min}$	Minimum on-time of HS FET	V_{IN} = 5V		35	44	ns
$t_{off, min}$	Minimum off-time of HS FET	V_{IN} = 5V		70	100	ns
	Maximum duty cycle of power stage	for TPS62877-Q1 only		45		%

6.6 I²C Interface Timing Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard mode			100	kHz
		Fast mode			400	kHz
		Fast mode plus			1	MHz
		High-speed mode (write operation), CB – 100pF max			3.4	MHz
		High-speed mode (read operation), CB – 100pF max			3.4	MHz
		High-speed mode (write operation), CB – 400pF max			1.7	MHz
		High-speed mode (read operation), CB – 400pF max			1.7	MHz
t_{HD}, t_{STA}	Hold time (repeated) START condition	Standard mode	4			µs
		Fast mode	0.6			µs
		Fast mode plus	0.26			µs
		High-speed mode	0.16			µs
t_{LOW}	LOW period of the SCL clock	Standard mode	4.7			µs
		Fast mode	1.3			µs
		Fast mode plus	0.5			µs
		High-speed mode, CB – 100pF max	0.16			µs
		High-speed mode, CB – 400pF max	0.32			µs
t_{HIGH}	HIGH period of the SCL clock	Standard mode	4			µs
		Fast mode	0.6			µs
		Fast mode plus	0.26			µs
		High-speed mode, CB – 100pF max	0.06			µs
		High-speed mode, CB – 400pF max	0.12			µs
t_{SU}, t_{STA}	Setup time for a repeated START condition	Standard mode	4.7			µs
		Fast mode	0.6			µs
		Fast mode plus	0.26			µs
		High-speed mode	0.16			µs
t_{SU}, t_{DAT}	Data setup time	Standard mode	250			ns
		Fast mode	100			ns
		Fast mode plus	50			ns
		High-speed mode, CB – 100pF max	10			ns
t_{HD}, t_{DAT}	Data hold time	Standard mode	0		3.45	µs
		Fast mode	0		0.9	µs
		Fast mode plus	0			µs
		High-speed mode, CB – 100pF max	0		70	ns
		High-speed mode, CB – 400pF max	0		150	ns
t_{RCL}	Rise time of both SDA and SCL signals	Standard mode			1000	ns
		Fast mode	20		300	ns
		Fast mode plus			120	ns
		High-speed mode, CB – 100pF max	10		40	ns
		High-speed mode, CB – 400pF max	20		80	ns

6.6 I²C Interface Timing Characteristics (続き)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{FCL}	Fall time of both SDA and SCL signals (1)	Standard mode			300	ns
		Fast mode	20 × V_{DD}/5.5 V		300	ns
		Fast mode plus	20 × V_{DD}/5.5 V		120	ns
		High-speed mode, CB – 100pF max	10		40	ns
		High-speed mode, CB – 400pF max	20		80	ns
t_{SU}, t_{STO}	Setup time of STOP Condition	Standard mode	4			µs
		Fast mode	0.6			µs
		Fast mode plus	0.26			µs
		High-Speed mode	0.16			µs
CB	Capacitive load for SDA and SCL	Standard mode			400	pF
		Fast mode			400	pF
		Fast mode plus			550	pF
		High-Speed mode			400	pF
t_{BUF}	Bus free time between a STOP and a START condition	Standard mode	4.7			µs
		Fast mode	1.3			µs
		Fast mode plus	0.5			µs

(1) V_{DD} is the pullup voltage of SDA and SCL.

6.7 Typical Characteristics

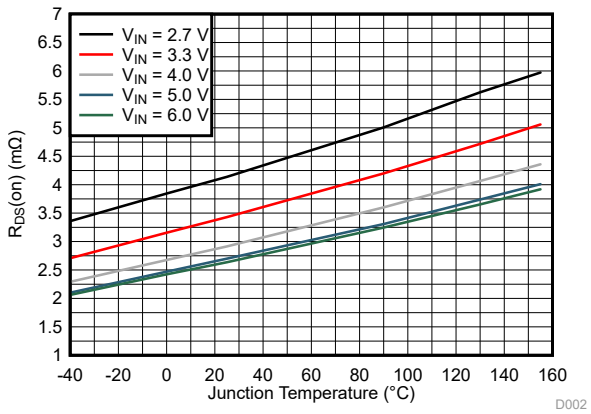


図 6-1. $R_{DS(ON)}$ of High Side Switch

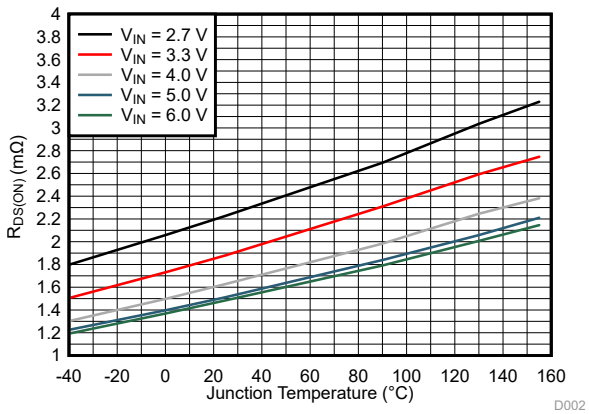


図 6-2. $R_{DS(ON)}$ of Low Side Switch

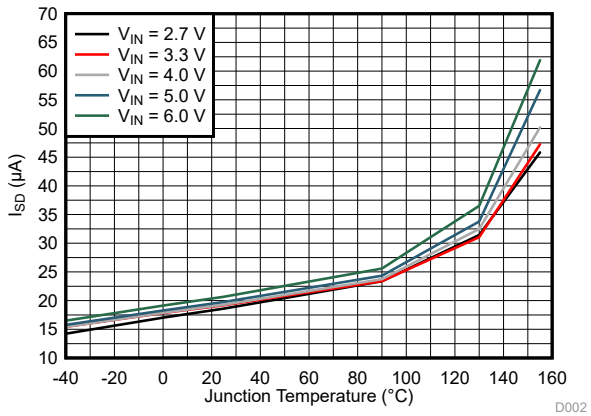


図 6-3. Shutdown Current vs Temperature

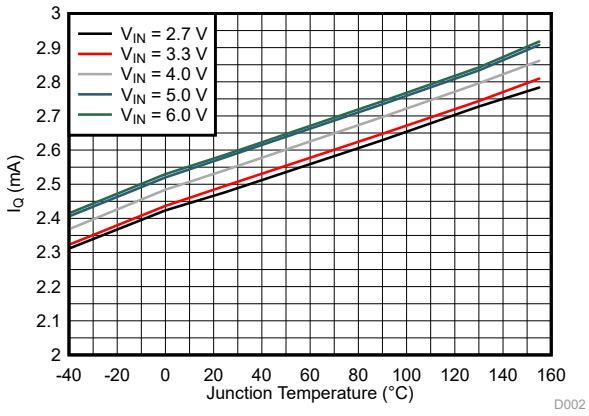


図 6-4. Quiescent Current vs Temperature

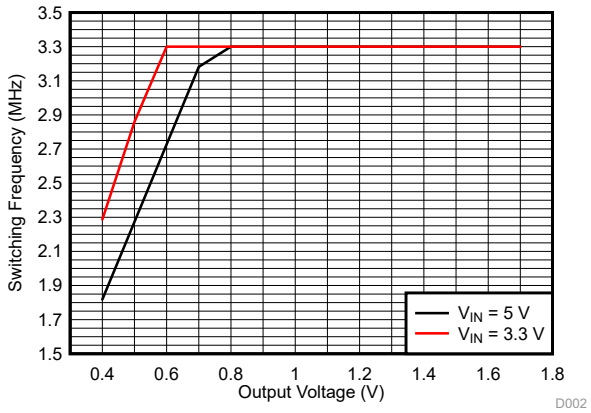


図 6-5. Maximum Switching Frequency vs Output Voltage

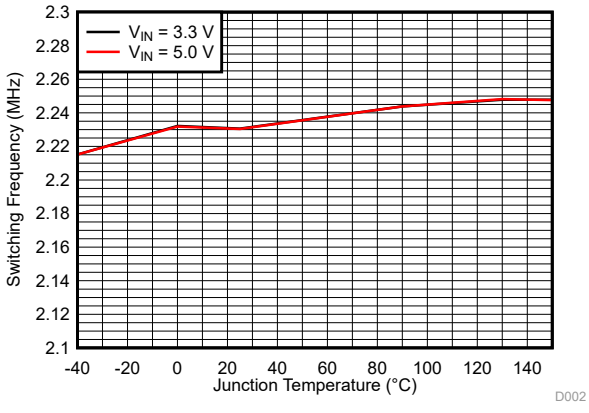


図 6-6. Switching Frequency vs Temperature

7 Parameter Measurement Information

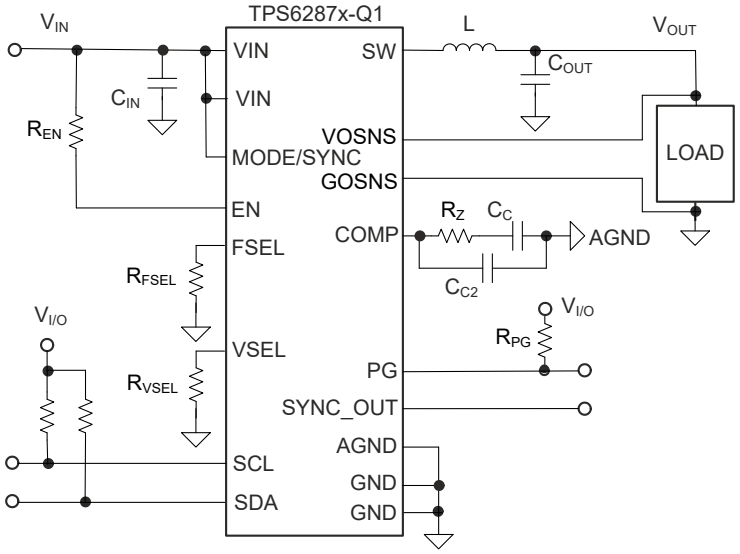


図 7-1. Measurement Setup for TPS6287x-Q1

表 7-1. List of Components

Reference	Description	Manufacturer
IC	TPS62877QWRZVRQ1	Texas Instruments
L	IHSR2525CZ-56nH	Vishay
C_{IN}	6 × 10µF / 10V; GCM21BR71A106KE22L + 2 × 4.7µF / 10V; LMK107BJ475MAHT	Murata, Taiyo Yuden
C_{OUT}	2 × 22µF / 10V; GCM31CR71A226KE02L + 8 × 47µF / 6.3V; GCM32ER70J476ME19L + 3 × 100µF / 6.3V; GRT32ER60J107NE13L	Murata
C_C	1nF	any
R_Z	3.6kΩ	any
C_{C2}	4.7pF	any
R_{EN}	22kΩ	any
R_{FSEL}	0kΩ to GND	any
R_{VSEL}	6.2kΩor 47kΩ or 0kΩ	any
R_{PG}	100kΩ	any

8 Detailed Description

8.1 Overview

The TPS6287x-Q1 devices are automotive-qualified, synchronous step-down (buck) DC/DC converters. These devices use an enhanced DCS-control scheme that combines fast transient response with fixed frequency operation, which, together with the low output voltage ripple, high DC accuracy, and differential remote sensing makes them designed for supplying the cores of modern high-performance processors.

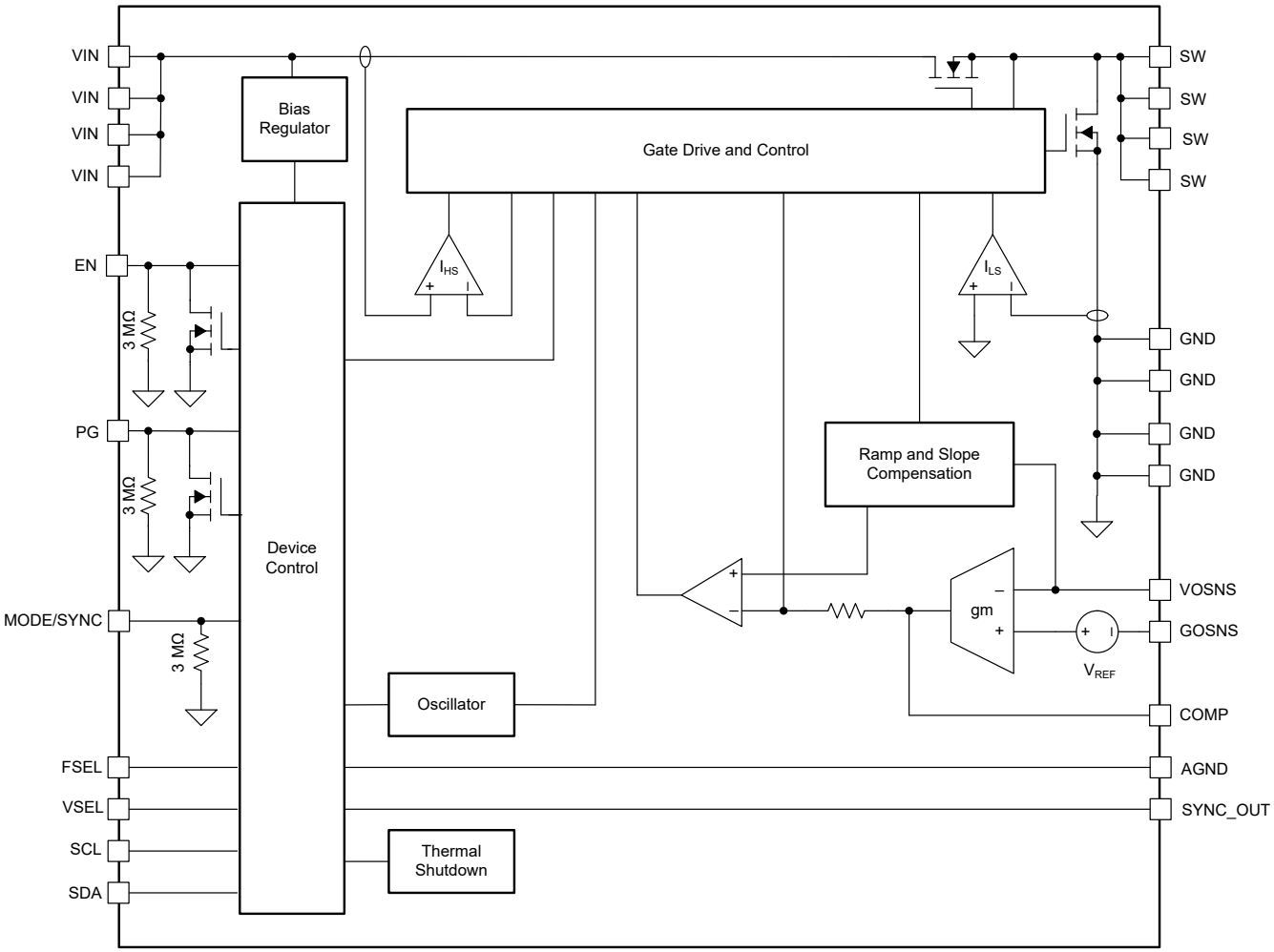
The four devices in this family are identical except for the current rating:

- The TPS62874-Q1 is a 15A rated device
- The TPS62875-Q1 is a 20A rated device
- The TPS62876-Q1 is a 25A rated device
- The TPS62877-Q1 is a 30A rated device

To further increase the output current capability, combine multiple devices in a *stack*. For example, a stack of two TPS62875-Q1 devices has a current capability of 40A.

The TPS6287x-Q1 devices have a built-in I^2C-compatible interface to control and monitor the operation. If the I^2C-compatible interface is not used, connect the SCL and SDA pins to GND.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fixed-Frequency DCS-Control Topology

図 8-1 shows a simplified block diagram of the fixed-frequency DCS-control topology used in the TPS6287x-Q1 devices. This topology comprises an inner emulated current loop and an outer voltage-regulating loop.

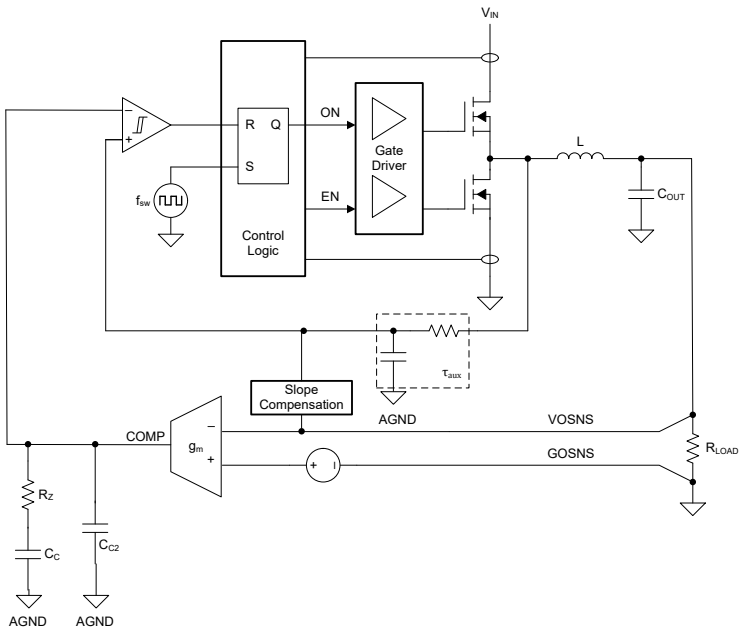


図 8-1. Fixed-Frequency DCS-Control Topology (Simplified)

8.3.2 Forced-PWM and Power-Save Modes

The device can control the inductor current in three different ways to regulate the output:

- Pulse-width modulation with continuous inductor current (PWM-CCM)
- Pulse-width modulation with discontinuous inductor current (PWM-DCM)
- Pulse-frequency modulation with discontinuous inductor current and pulse skipping (PFM-CCM)

During PWM-CCM operation, the device switches at a constant frequency and the inductor current is continuous (see 図 8-2). PWM operation achieves the lowest output voltage ripple and the best transient performance.

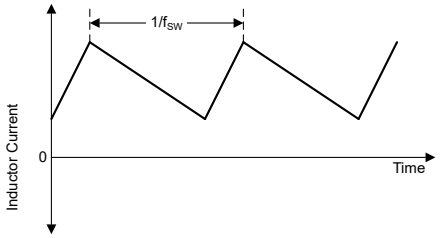


図 8-2. Continuous Conduction Mode (CCM) Current Waveform

During PWM-DCM operation the device switches at a constant frequency and the inductor current is discontinuous (see 図 8-3). In this mode the device controls the peak inductor current to maintain the selected switching frequency while still being able to regulate the output.

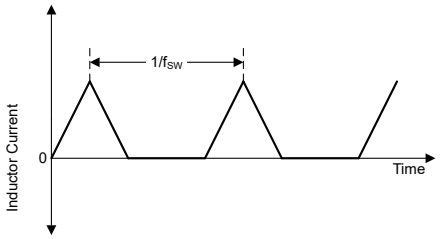


図 8-3. Discontinuous Conduction Mode (DCM) Waveform

During PFM-DCM operation the device keeps the peak inductor current constant (at a level corresponding to the minimum on-time of the converter) and skips pulses to regulate the output (see 図 8-4). The switching pulses that occur during PFM-DCM operation are synchronized to the internal clock.

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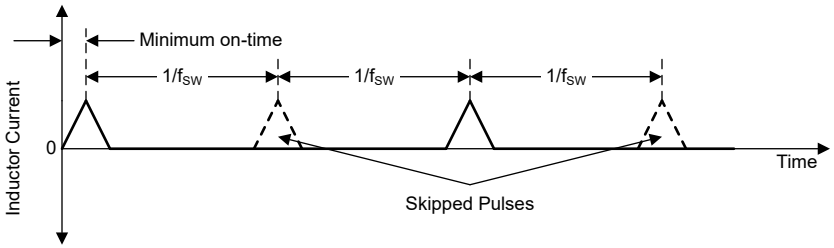


図 8-4. Discontinuous Conduction Mode (PFM-DCM) Current Waveform

Use 式 1 to calculate the output current threshold at which the device enters PFM-DCM:

$$I_{OUT(PFM)} = \frac{(V_{IN} - V_{OUT})}{2L} t_{ON}{}^2 \left(\frac{V_{IN}}{V_{OUT}} \right) f_{sw} \quad (1)$$

The following figure shows how this threshold typically varies with V_{IN} and V_{OUT} for a switching frequency of 2.25MHz

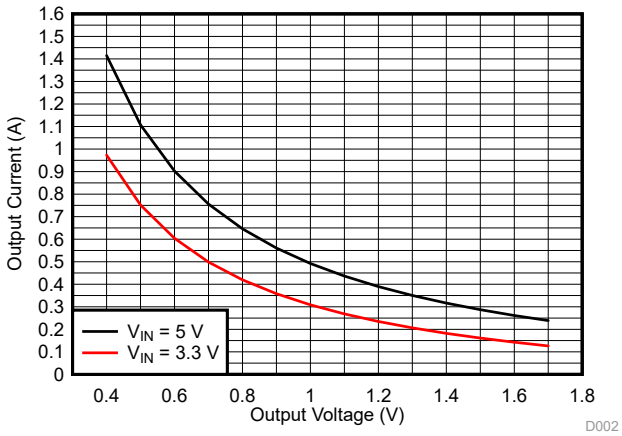


図 8-5. Output Current PFM-DCM Entry Threshold for f_{SW} = 2.25MHz

Configure the device to use either Forced-PWM (FPWM) mode or Power-Save Mode (PSM):

- In forced-PWM mode. the device uses PWM-CCM at all times.
- In power-save mode, the device uses PWM-CCM at medium and high loads, PWM-DCM at low loads, and PFM-DCM at very low loads. Transition between the different operating modes is seamless.

表 8-1 shows the function table of the MODE/SYNC pin and the FPWMEN bit in the CONTROL1 register, which control the operating mode of the device.

表 8-1. FPWM Mode and Power-Save Mode Selection

MODE/SYNC Pin	FPWMEN Bit	Operating Mode	Remark
Low	0	PSM	Do not use in a stacked configuration
	1	FPWM	
High	X	FPWM	
Sync Clock	X	FPWM	

8.3.3 Transient Non-Synchronous Mode (optional)

The TPS6287x-Q1 has a transient non-synchronous mode that helps to minimize the output voltage overshoot during a load release. When the high side FET is turned off, the decay in inductor current is mainly determined by the output voltage as there is little voltage drop over the low side FET. For very low output voltages the current decays slowly so the output voltage overshoot is typically larger than the undershoot during a load step. Non-synchronous mode turns off the low side FET for 6 switching cycles so the inductor current decays through the body diode. This adds extra voltage across the inductor so the current decays quicker and the output voltage overshoot is lower.

8.3.4 Precise Enable

The Enable (EN) pin is bidirectional, and has two functions:

- As an input, the pin enables and disables the DC/DC converter in the device.
- As an output, the pin provides a SYSTEM_READY signal to other devices in a stacked configuration.

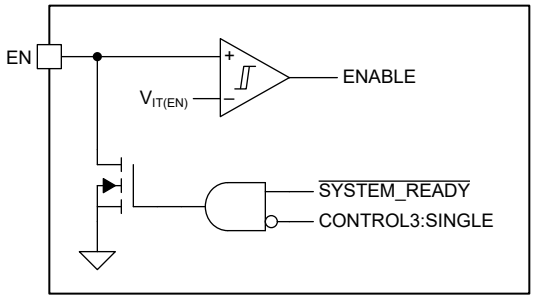


図 8-6. Enable Functional Block Diagram

Because there is an internal open-drain transistor connected to the EN pin, do not drive this pin directly from a low-impedance source. Instead, use a resistor to limit the current flowing into the EN pin (see セクション 10.1).

When power is first applied to the VIN pin, the device pulls the EN pin low until it has loaded the default register settings from nonvolatile memory and read the state of the VSEL, FSEL and SYNC_OUT pins. The device also pulls EN low if a fault such as thermal shutdown or overvoltage lockout occurs. In a stacked configuration all devices share a common enable signal, which means that the DC/DC converters in the stack cannot start to switch until *all* devices in the stack have completed the initialization. Similarly, a fault in one or more devices in the stack disables *all* converters in the stack (see セクション 8.3.18).

In stand-alone (non-stacked) applications, you can disable the active pulldown of the EN pin if you set SINGLE = 1 in the CONTROL3 register. Fault conditions have no effect on the EN pin when SINGLE = 1. (Note that the EN pin is *always* pulled down during device initialization.) In stacked applications, make sure that SINGLE = 0.

When the internal $\overline{\text{SYSTEM\_READY}}$ signal is low (that is, initialization is complete and there are no fault conditions), the internal open-drain transistor is high impedance and the EN pin functions like a standard input: A high level on the EN pin enables the DC/DC converter in the device and a low level disables the DC/DC

converter in the device. (The I^2C interface is enabled as soon as the device has completed the initialization and is not affected by the state of the internal ENABLE or $\overline{\text{SYSTEM\_READY}}$ signals.)

A low level on the EN pin forces the device into shutdown. During shutdown, the MOSFETs in the power stage are off, the internal control circuitry is disabled, and the device consumes only 20µA (typical).

The rising threshold voltage of the EN pin is 1.0V and the falling threshold voltage is 0.9V. The tolerance of the threshold voltages is ±30mV, which means that you can use the EN pin to implement precise turn-on and turn-off behavior.

8.3.5 Start-Up

When the voltage on the VIN pin exceeds the positive-going UVLO threshold, the device initializes as follows:

- The device pulls the EN pin low.
- The device enables the internal reference voltage.
- The device reads the state of the VSEL, FSEL and SYNC_OUT pins.
- The device loads the default values into the device registers.

When initialization is complete, the device enables I^2C communication and releases the EN pin. The external circuitry controlling the EN pin now determines the behavior of the device:

- If the EN pin is low, the device is disabled: write to and read from the device registers, but the DC/DC converter does not operate.
- If the EN pin is high, the device is enabled: write to and read from the device registers and, after a short delay from EN pin going high, the DC/DC converter starts to ramp up the output.

図 8-7 shows the start-up sequence when the EN pin is pulled up to V_{IN}.

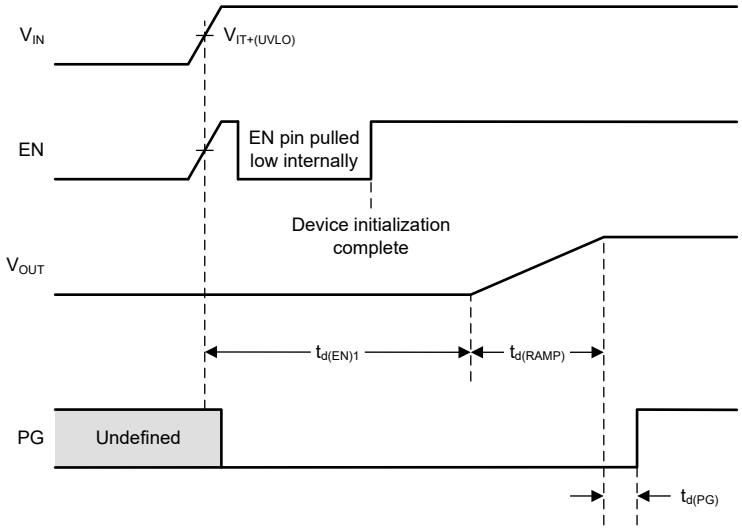


図 8-7. Start-Up Timing When EN is Pulled Up to V_{IN}

図 8-8 shows the start-up sequence when an external signal is connected to the EN pin.

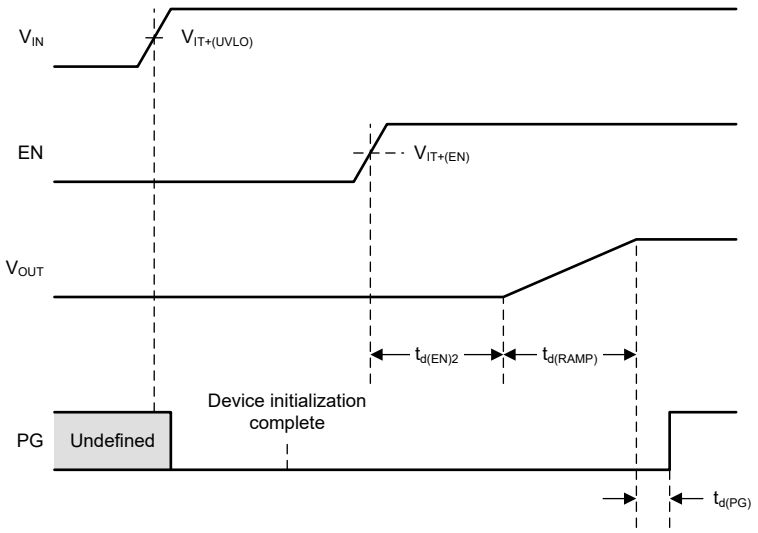


図 8-8. Start-Up Timing When an External Signal is Connected to the EN Pin

The SSTIME[1:0] bits in the CONTROL2 register select the duration of the soft-start ramp:

- $t_{d(RAMP)}$ = 500µs
- $t_{d(RAMP)}$ = 770µs
- $t_{d(RAMP)}$ = 1ms (default)
- $t_{d(RAMP)}$ = 2ms

If you program new output voltage setpoint (VOUT[7:0]), output voltage range (VRANGE[1:0]), or soft-start time (SSTIME[1:0]) settings when the device has already begun the soft-start sequence, the device ignores the new values until the soft-start sequence is complete. For example, if you change the value of VSET[7:0] during soft-start, the device first ramps to the value that VSET[7:0] had when the soft-start sequence began and then, when soft-start is complete, ramps up or down to the new value.

The device can start up into a prebiased output. In this case, only a portion of the internal voltage ramp is seen externally (see 図 8-9).

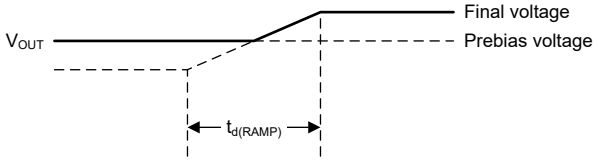


図 8-9. Start-Up into a Prebiased Output

Note that the device *always* operates in DCM/PFM allowed during the start-up ramp, regardless of other configuration settings or operating conditions.

8.3.6 Switching Frequency Selection

During device initialization, a resistor-to-digital converter in the device determines the state of the FSEL pin and sets the switching frequency of the DC/DC converter according to 表 8-2.

表 8-2. Switching Frequency Options

Resistor at FSEL (1%)	Switching Frequency
6.2 kΩ to GND	1.5 MHz
Short to GND	2.25 MHz
Short to V_{IN}	2.5 MHz

表 8-2. Switching Frequency Options (続き)

Resistor at FSEL (1%)	Switching Frequency
47 kΩ to V_{IN}	3 MHz

The following figure shows a simplified block diagram of the R2D converter used to detect the state of the FSEL pin (an identical circuit detects the state of the VSEL pin – see *Output Voltage Setpoint*).

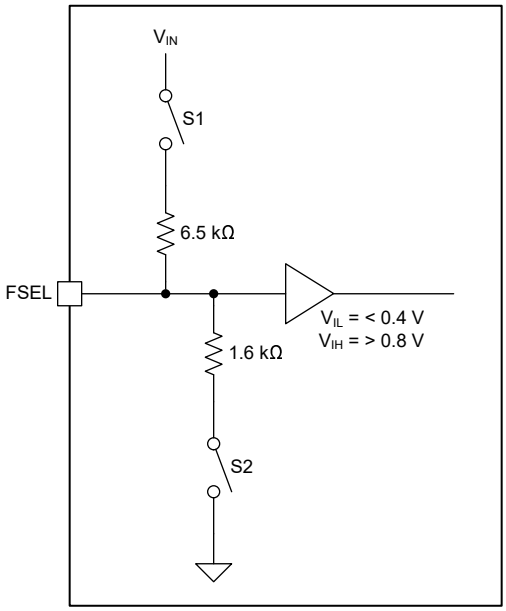


図 8-10. FSEL R2D Converter Functional Block Diagram

Detection of the state of the FSEL pin works as follows:

To detect the most significant bit (MSB), the circuit opens S1 and S2, and the input buffer detects if a high or a low level is connected to the FSEL pin.

To detect the least significant bit (LSB):

- If the MSB is 0, the circuit closes S1. If the input buffer detects a high level, the LSB = 1; if the circuit detects a low level, the LSB = 0.
- If the MSB is 1, the circuit closes S2. If the input buffer detects a low level, the LSB = 0; if the circuit detects a high level, the LSB = 1.

The propagation delay of the current-sensing comparator limits the minimum on-time of the device. In practice, this means that the maximum switching frequency the device can support decreases with small duty cycles. 図 6-5 shows the practical operating range of the device with 3.3-V and 5-V supplies.

8.3.7 Output Voltage Setting

8.3.7.1 Output Voltage Range

The device has three different voltage ranges. The VRANGE[1:0] bits in the CONTROL1 register control which range is active (see 表 8-3). The default output voltage range after device initialization is 0.4 V to 1.675 V in 5-mV steps.

表 8-3. Voltage Ranges

VRANGE[1:0]	Voltage Range
0b00	0.4 V to 0.71875V in 1.25mV steps
0b01	0.4 V to 1.0375V in 2.5mV steps

表 8-3. Voltage Ranges (続き)

VRANGE[1:0]	Voltage Range
0b10	0.4V to 1.675V in 5mV steps
0b11	0.4V to 1.675V in 5mV steps

Note that every change to the VRANGE[1:0] bits must be followed by a write to the VSET register – even if the value of the VSET[7:0] bits does not change. This sequence is necessary for the device to start to use the new voltage range.

8.3.7.2 Output Voltage Setpoint

Together with the selected range, the VSET[7:0] bits in the VSET register control the output voltage setpoint of the device (see 表 8-4).

表 8-4. Start-Up Voltage Settings

VRANGE[1:0]	Output Voltage Setpoint
0b00	0.4V + VSET[7:0] × 1.25mV
0b01	0.4V + VSET[7:0] × 2.5mV
0b10 (default)	0.4V + VSET[7:0] × 5mV
0b11	0.4V + VSET[7:0] × 5mV

During initialization, the device reads the state of the VSEL pin and selects the default output voltage according to 表 8-5. Note that the VSEL pin also selects the I^2C target address of the device (see below). Please see the DEVICE OPTIONS table for the complete list of device versions and their Output Voltage Setpoint.

表 8-5. Default Output Voltage Setpoints

VSEL Pin[1]	VSET[7:0]	I2C Device Address	Output Voltage Setpoint
6.2kΩ to GND	0x50	0x44	800mV
Short-Circuit to GND	0x46	0x45	750mV
Short-Circuit to V_{IN}	0x5F	0x46	875mV
47kΩ to V_{IN}	0x24	0x47	580mV

If you program new output voltage setpoint (VOUT[7:0]), output voltage range (VRANGE[1:0]), or soft-start time (SSTIME[1:0]) settings when the device has already begun the soft-start sequence, the device ignores the new values until the soft-start sequence is complete. For example, if you change the value of VSET[7:0] during soft-start, the device first ramps to the value that VSET[7:0] had when the soft-start sequence began and then, when soft-start is complete, ramps up or down to the new value.

If you change VOUT[7:0], VRAMP[1:0], or SSTIME[1:0] while EN is low, the device uses the new values the next time you enable it.

During start-up the output voltage ramps up to the target value set by the VSEL pin before ramping up or down to any new value programmed to the device over the I^2C interface.

8.3.7.3 Non-Default Output Voltage Setpoint

If none of the default voltage range / voltage setpoint combinations is suitable for your application, you can change these device settings via I^2C before you enable the device. Then, when you pull the EN pin high, the device starts up with the desired start-up voltage.

Note that if you change the device settings via I^2C *while the device is ramping*, the device ignores the changes until the ramp is complete.

[1] For reliable voltage setting, make sure that there is no stray current path connected to the VSEL pin and that the parasitic capacitance between the VSEL pin and GND is less than 30pF.

8.3.7.4 Dynamic Voltage Scaling

If you change the output voltage setpoint while the DC/DC converter is operating, the device ramps up or down to the new voltage setting in a controlled way.

The VRAMP[1:0] bits in the CONTROL1 register set the slew rate when the device ramps from one voltage to another during DVS (see 表 8-6).

表 8-6. Dynamic Voltage Scaling Slew Rate

VRAMP[1:0]	DVS Slew Rate
0b00	10mV/µs
0b01	5mV/µs
0b10 (default)	1.25mV/µs
0b11	0.5mV/µs

Note that ramping the output to a higher voltage requires additional output current, so that during DVS the converter must generate a total output current given by:

$$I_{OUT} = I_{OUT\,(DC)} + C_{OUT} \frac{dV_{OUT}}{dt} \quad (2)$$

where:

- I_{OUT} is the total current the converter must generate while ramping to a higher voltage
- $I_{OUT(DC)}$ is the DC load current
- C_{OUT} is the total output capacitance
- dV_{OUT}/dt is the slew rate of the output voltage (programmable in the range 0.5mV/µs to 10mV/µs)

For correct operation, make sure that the total output current during DVS does not exceed the current limit of the device.

8.3.7.5 Droop Compensation

Droop compensation scales the nominal output voltage based on the output current. This action is done such that the output voltage is set to a higher value with no output current and to a lower value than the nominal value with the maximum output current. Droop compensation therefore provides a higher margin during a load transient and helps to keep the output voltage within a certain tolerance band in case of a heavy load step or at load release or allows to use a lower output capacitance. The voltage scaling is absolute instead of relative. The voltage scaling vs output current depends on the output current version of TPS6287x-Q1 based on the rated output current of , 15A, 20A, 25A and 30A, respectively. The behavior is shown in the graph Voltage Scaling with Output Current. See the Device Options table for the specific version if droop compensation is disabled or enabled by default. Droop compensation can be enabled by bit CONTROL3:DROOPEN. Enabling droop compensation must be done while the device is disabled otherwise a transient output voltage deviation can occur.

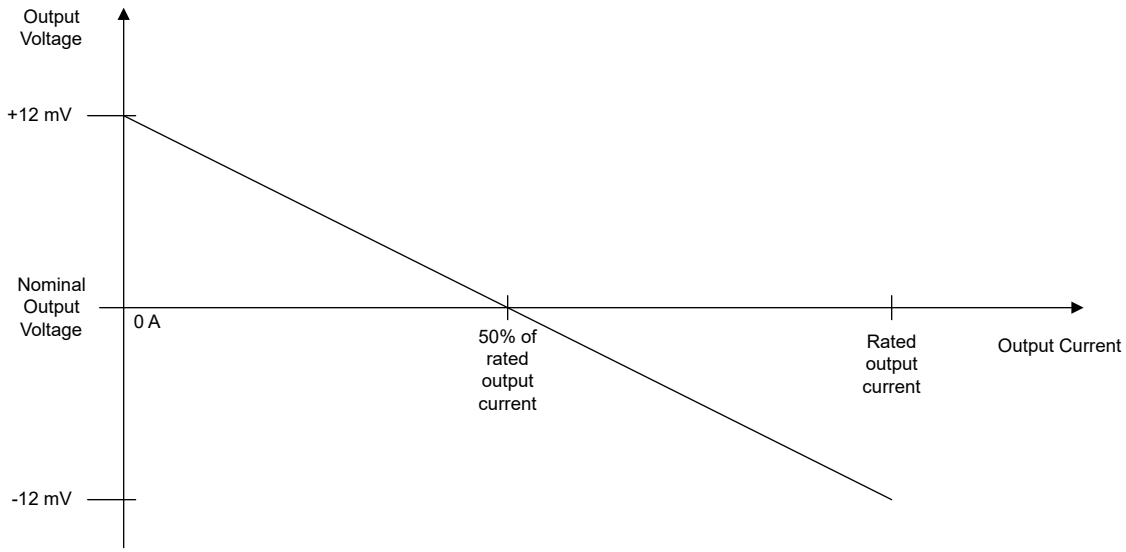


図 8-11. Voltage Scaling With Output Current

8.3.8 Compensation (COMP)

The COMP pin is the connection point for an external compensation network. A series-connected resistor and capacitor to GND is sufficient for typical applications and provides enough scope to optimize the loop response for a wide range of operating conditions.

When using multiple devices in a stacked configuration, all devices share a common compensation network, and the COMP pin makes sure of equal current sharing between them (see セクション 8.3.18).

8.3.9 Mode Selection / Clock Synchronization (MODE/SYNC)

A high level on the MODE/SYNC pin selects forced-PWM operation. A low level on the MODE/SYNC pin selects power-save operation, in which the device automatically transitions between PWM and PFM, according to the load conditions.

If you apply a valid clock signal to the MODE/SYNC pin, the device synchronizes the switching cycles to the external clock and automatically selects forced-PWM operation.

The MODE/SYNC pin is logically ORed with the FPWMEN bit in the CONTROL1 register (see 表 8-1).

When multiple devices are used together in a stacked configuration the MODE/SYNC pin of the secondary devices is the input for the clock signal (see セクション 8.3.18).

8.3.10 Spread Spectrum Clocking (SSC)

The device has a spread spectrum clocking function that can reduce electromagnetic interference (EMI). When the SSC function is active, the device modulates the switching frequency ±10% about the nominal value. The frequency modulation has a triangular characteristic (see 図 8-12).

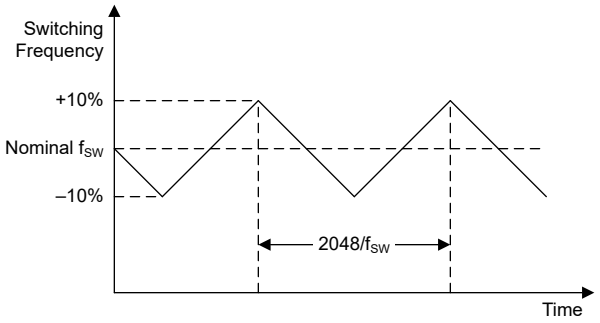


図 8-12. Spread Spectrum Clocking Behavior

To use the SSC function, make sure that:

- SSCEN = 1 in the CONTROL1 register
- Forced-PWM operation is selected (MODE pin is high or FPWMEN = 1 in the CONTROL1 register)
- The device is not synchronized to an external clock

To disable the SSC function, make sure that SCCEN = 0 in the CONTROL1 register.

To use the SSC function with multiple devices in a stacked configuration, make sure that the primary converter runs from the internal oscillator and synchronize all secondary converters to the primary clock (see 図 8-16).

8.3.11 Output Discharge

The device has an output discharge function which makes sure of a defined ramp down of the output voltage when the device is disabled and keeps the output voltage close to 0V while the device is off. The output discharge function is enabled when DISCHEN = 1 in the CONTROL1 register. The output discharge function is enabled by default.

If enabled, the device discharges the output under the following conditions:

- A low level is applied to the EN pin
- SWEN = 0 in the CONTROL1 register
- A thermal shutdown event occurs
- An UVLO event occurs
- An OVLO event occurs

The output discharge function is not available until you have enabled the device at least once after power up. During power-down, the device continues to discharge the output for as long as the supply voltage is greater than approximately 1.8V.

8.3.12 Undervoltage Lockout (UVLO)

The TPS6287x-Q1 has an undervoltage lockout function that disables the device if the supply voltage is too low for correct operation. The negative-going threshold of the UVLO function is 2.5V (typical). If the supply voltage decreases below this value, the device stops switching and, if DISCHEN = 1 in the CONTROL1 register, turns on the output discharge.

8.3.13 Overvoltage Lockout (OVLO)

The TPS6287x-Q1 has an overvoltage lockout function that disables the DC/DC converter if the supply voltage is too high for correct operation. The positive-going threshold of the OVLO function is 6.3V (typical). If the supply voltage increases above this value, the device stops switching and, if DISCHEN = 1 in the CONTROL1 register, turns on the output discharge.

The device automatically starts switching again – it begins a new soft-start sequence – when the supply voltage falls below 6.2V (typical).

8.3.14 Overcurrent Protection

8.3.14.1 Cycle-by-Cycle Current Limiting

If the peak inductor current increases above the high-side current limit threshold, the device turns off the high-side switch and turns on the low-side switch to ramp down the inductor current. The device only turns on the high-side switch again if the inductor current has decreased below the low-side current limit threshold.

Note that because of the propagation delay of the current limit comparator, the current limit threshold in practice can be greater than the DC value specified in the Electrical Characteristics. The current limit in practice is given by:

$$I_L = I_{LIMH} + \left(\frac{V_{IN} - V_{OUT}}{L}\right) t_{pd} \quad (3)$$

where:

- I_L is the peak inductor current
- I_{LIMH} is the high-side current limit threshold measured at DC
- V_{IN} is the input voltage
- V_{OUT} is the output voltage
- L is the effective inductance at the peak current level
- t_{pd} is the propagation delay of the current limit comparator (typically 50ns)

8.3.14.2 Hiccup Mode

To enable hiccup operation, make sure that HICCUPEN = 1 in the CONTROL1 register. The HICCUP function is disabled by default.

If hiccup operation is enabled and the high-side switch current exceeds the current limit threshold on 32 consecutive switching cycles, the device:

- Stops switching for 128µs, after which the device automatically starts switching again (starts a new soft-start sequence).
- Sets the HICCUP bit in the STATUS register.
- Pulls the PG pin low. The PG pin stays low until the overload condition goes away and the device can start up correctly and regulate the output voltage. Note that power-good function has a deglitch circuit, which delays the rising edge of the power-good signal by 40µs (typical).

Hiccup operation continues – in a repeating sequence of 32 cycles in current limit, followed by a pause of 128µs, followed by a soft-start attempt – for as long as the output overload condition exists.

The device clears the HICCUP bit if you read the STATUS register when the overload condition has been removed.

8.3.14.3 Current-Limit Mode

To enable current-limit mode, make sure that HICCUPEN = 0 in the CONTROL1 register.

When current limit operation is enabled the device limits the high-side switch current cycle-by-cycle for as long as the overload condition exists. If the device limits the high-side switch current for four or more consecutive switching cycles it sets ILIM = 1 in the STATUS register.

The device clears the ILIM bit if you read the STATUS register when the overload condition no longer exits.

8.3.15 Power Good (PG)

The Power-Good (PG) pin is bidirectional and has two functions:

- In a standalone configuration, and in the primary device of a stacked configuration, the PG pin is an open-drain output that indicates the status of the converter or stack.

- In a secondary device of a stacked configuration, the PG pin is an input that indicates when the soft-start sequence is complete and all converters in the stack can change from DCM switching to CCM switching.

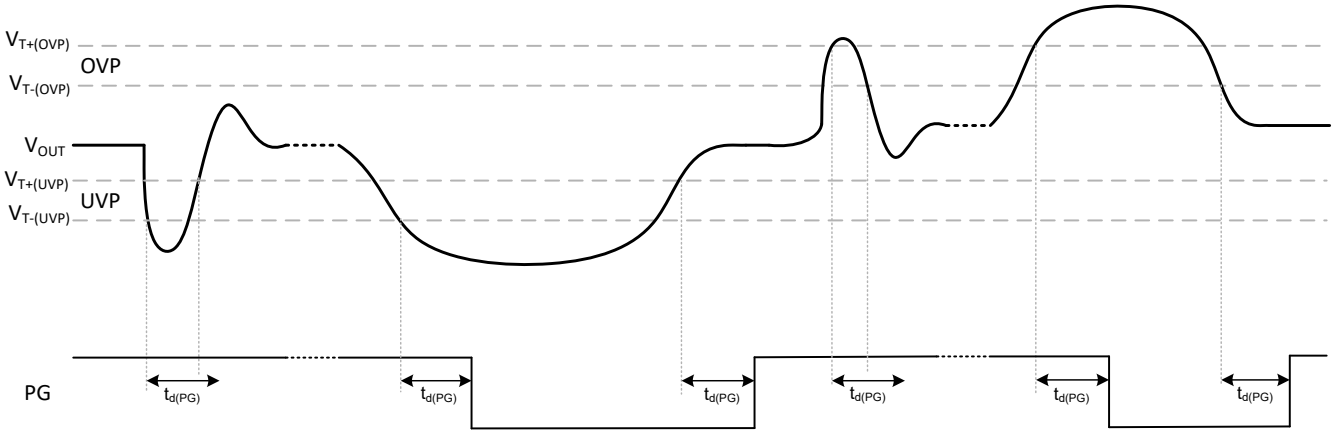


図 8-13. PG Timing

8.3.15.1 Standalone, Primary Device Behavior

The primary purpose of the PG pin is to indicate if the output voltage is in regulation, but the PG pin also indicates if the device is in thermal shutdown or disabled. 表 8-7 summarizes the behavior of the PG pin in a stand-alone or primary device.

表 8-7. Power-Good Function Table

V_{IN}	EN	V_{OUT}	Soft Start	PGBLNKDVS AND DVS_active	T_J	PG
$V_{IN} < 2V$	X	X	X	X	X	Undefined
$V_{IT-(UVLO)} \geq V_{IN} \geq 2V$	X	X	X	X	X	Low
$V_{IT-(UVLO)} < V_{IN} < V_{IT+(OVLO)}$	L	X	X	X	X	Low
	H	X	Active	X	X	Low
		$V_{OUT} > V_{T+(OVP)}$ or $V_{OUT} < V_{T-(UVP)}$	Inactive	0	X	low
				1	$T_J < T_{SD}$	Hi-Z
		$V_{T-(OVP)} > V_{OUT} > V_{T+(UVP)}$		X	$T_J < T_{SD}$	Hi-Z
		X	X	X	$T_J > T_{SD}$	Low
$V_{IN} > V_{IT+(OVLO)}$	X	X	X	X	X	Low

図 8-14 shows a functional block diagram of the power-good function in a stand-alone or primary device. A window comparator monitors the output voltage, and the output of the comparator goes high if the output voltage is either less than 95% (typical) or greater than 105% (typical) of the nominal output voltage. The output of the window comparator is deglitched – the typical deglitch time is 40µs – and then used to drive the open-drain PG pin.

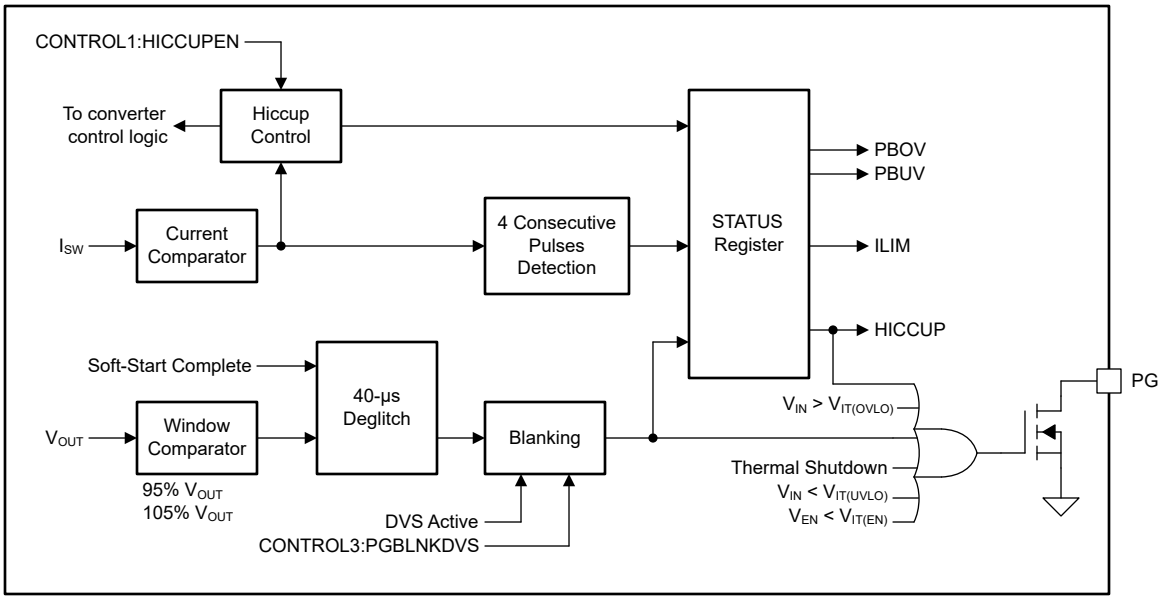


図 8-14. Power-Good Functional Block Diagram (Standalone / Primary Device)

During DVS activity, when the DC/DC converter transitions from one output voltage setting to another, the output voltage can temporarily exceed the limits of the window comparator and pull the PG pin low. The device has a feature to disable this behavior: if PGBLNKDVS = 1 in the CONTROL3 register, the device ignores the output of the power-good window comparator while DVS is active.

Note that the PG pin is always low – regardless of the output of the window comparator – when:

- The device is in thermal shutdown
- The device is disabled
- The device is in undervoltage lockout
- The device is in overvoltage lockout
- The device is in soft start
- The device is in HICCUP mode

8.3.15.2 Secondary Device Behavior

図 8-15 shows a functional block diagram of the power-good function in a secondary device. During initialization, the device presets FF2, which pulls down the PG pin and forces the devices in a stack to operate in DCM. When the device completes the internal start-up sequence, the device resets FF2, which turns off Q1. In a stacked configuration all devices share the same PG signal, and therefore the PG pin stays low until *all* devices in the stack have completed the start-up. When that happens, FF1 is set and the converters operate in CCM. FF1 and FF2 are preset such that DCM is allowed each time the converter is disabled, either by the EN pin, EN bit, thermal shutdown or UVLO.

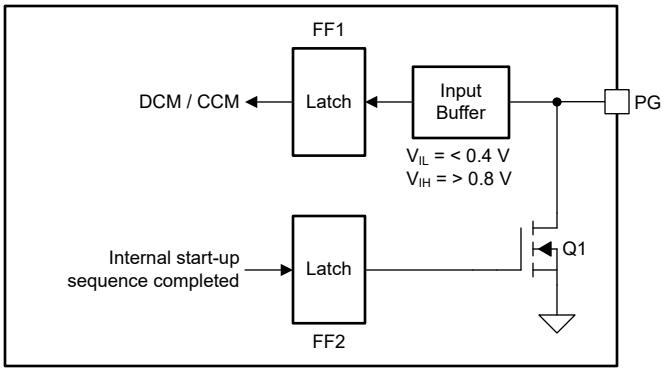


図 8-15. Power-Good Functional Block Diagram (Secondary Device)

8.3.16 Remote Sense

The device has two pins, VOSNS and GOSNS, to remotely sense the output voltage. Remote sensing lets the converter sense the output voltage directly at the point-of-load and increases the accuracy of the output voltage regulation.

In a stacked configuration, you must connect the VOSNS and GOSNS of the primary device directly at the point-of-load. For the secondary devices, you can connect the VOSNS and GOSNS pins to the local output capacitor or both pins to AGND (see セクション 8.3.18).

8.3.17 Thermal Warning and Shutdown

The device has a two-level overtemperature detection function.

If the junction temperature rises above the thermal warning threshold of 150 °C (typical), the device sets the TWARN bit in the STATUS register. The device clears the TWARN bit if you read the STATUS register when the junction temperature is below the TWARN threshold of 130°C (typical).

If the junction temperature rises above the thermal shutdown threshold of 170°C (typical), the device:

- Stops switching
- Pulls down the EN pin (if SINGLE = 0 in the CONTROL3 register)
- Enables the output discharge (if DISCHEN = 1 in the CONTROL1 register)
- Sets the TSHUT bit in the STATUS register
- Pulls the PG pin low

If the junction temperature falls below the thermal shutdown threshold of 150°C (typical), the device:

- Starts switching again, starting with a new soft-start sequence
- Sets the EN pin to high impedance
- Sets the PG pin to high-impedance

The device clears the TSHUT bit if you read the STATUS register when the junction temperature is below the TSHUT threshold of 150°C (typical).

In a stacked configuration, in which all devices share a common enable signal, a thermal shutdown condition in one device disables the entire stack. When the hot device cools down, the whole stack automatically starts switching again.

8.3.18 Stacked Operation

Connect multiple TPS6287x-Q1 devices in parallel in what is known as a "stack"; for example, to increase output current capability or reduce device junction temperature. A stack comprises one *primary* device and one or more *secondary* devices. During initialization, each device monitors the SYNCOUT pin to determine if it must operate as a primary device or a secondary device:

- If there is a 47kΩ resistor between the SYNCOUT pin and ground, the device operates as a secondary device
- If the SYNCOUT pin is high impedance, the device operates as a primary device

図 8-16 shows the recommended interconnections in a stack of two TPS6287x-Q1 devices.

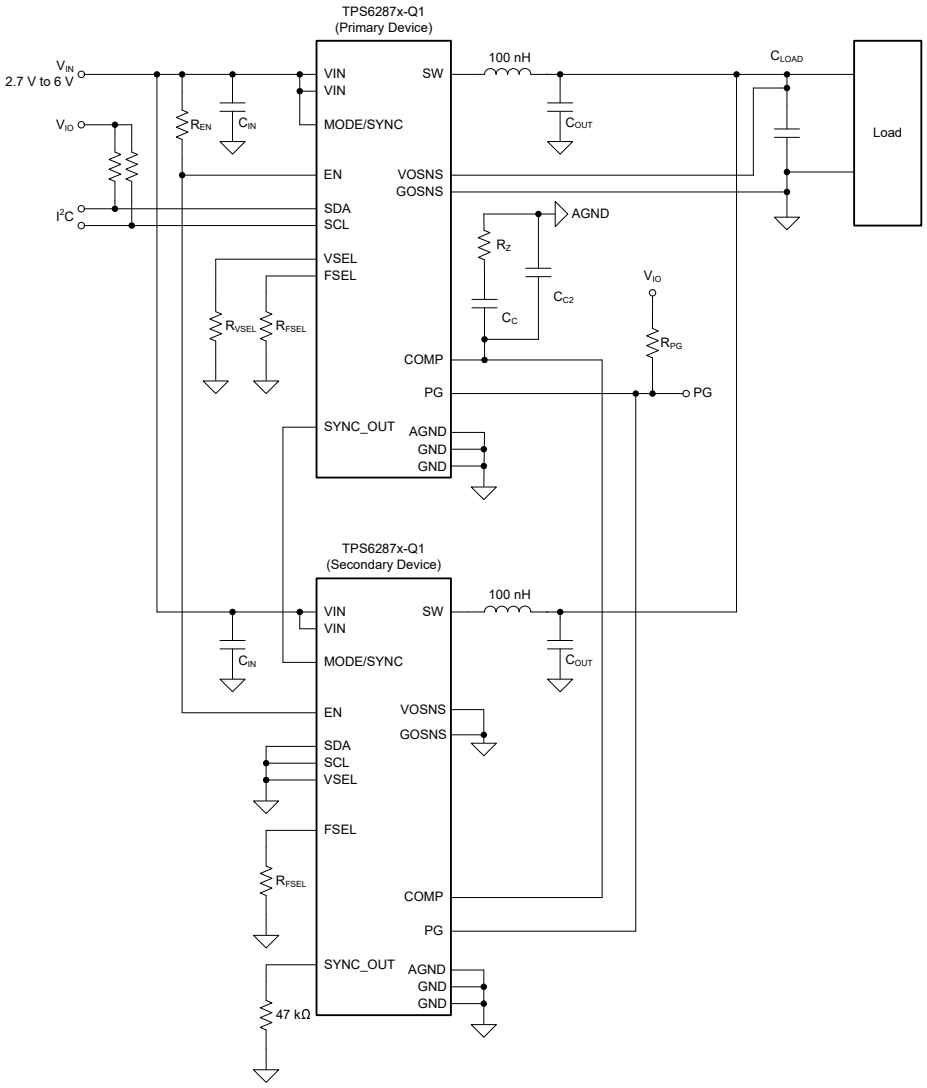


図 8-16. Two TPS6287x-Q1 Devices in a Stacked Configuration

The key points to note are:

- All the devices in the stack share a common enable signal, which must be pulled up with a resistance of at least 15kΩ.
- All the devices in the stack share a common power-good signal.
- All the devices in the stack share a common compensation signal.
- All secondary devices must connect a 47kΩ resistor between the SYNC_OUT pin and ground.
- The remote sense pins (VOSNS and GOSNS) *of each device* must be connected (do not leave these pins floating).
- VOSNS and GOSNS of the primary device must be connected to the capacitor at the load
- VOSNS and GOSNS of the secondary devices can either be connected to the output capacitor at the device or alternatively both pins can be tied to AGND.

- Each device must be configured for the same switching frequency.
- The primary device must be configured for forced-PWM operation (secondary devices are automatically configured for forced-PWM operation).
- A stacked configuration can support synchronization to an external clock or spread-spectrum clocking.
- Only the VSEL pin of the primary device is used to set the default output voltage. The VSEL pin of secondary devices is not used and must be connected to ground.
- The SDA and SCL pins of secondary devices are not used and must be connected to ground.
- A stacked configuration uses a daisy-chained clocking signal, in which each device switches with a phase offset of approximately 120° relative to the adjacent devices in the daisy-chain. To daisy-chain the clocking signal, connect the SYNCOUT pin of the primary device to the MODE/SYNC pin of the first secondary device. Connect the SYNCOUT pin of the first secondary device to the MODE/SYNC pin of the second secondary device. Continue this connection scheme for all devices in the stack, to daisy-chain them together.
- CONTROL2:SYNC_OUT_PHASE = 1 sets a phase shift of 180° from the primary to the first secondary device. Please see the DEVICE OPTIONS table for the complete list of available OTP spins.
- Hiccup overcurrent protection must not be used in a stacked configuration.

In a stacked configuration, the common enable signal also acts as a SYSTEM_READY signal (see セクション 8.3.4). Each device in the stack can pull the EN pin low during device start-up or when a fault occurs. Thus, the stack is only enabled when all devices have completed the start-up sequence and are fault-free. A fault in any one device disables the whole stack for as long as the fault condition exists.

During start-up, the primary device pulls the COMP pin low for as long as the enable signal (SYSTEM_READY) is low. When the enable signal goes high, the primary device actively controls the COMP pin and all devices in the stack follow the COMP voltage. During start-up, each device in the stack pulls the PG pin low while the pin initializes. When initialization is complete, each secondary device in the stack sets the PG pin to a high impedance and the primary device alone controls the state of the PG signal. The PG pin goes high when the stack has completed the start-up ramp and the output voltage is within specification. The secondary devices in the stack detect the rising edge of the power-good signal and switch from DCM operation to CCM operation. After the stack has successfully started up, the primary device controls the power-good signal in the normal way. In a stacked configuration, there are some faults that only affect individual devices, and other faults that affect all devices. For example, if one device enters current limit, only that device is affected. But a thermal shutdown or undervoltage lockout event in one device disables all devices through the shared enable (SYSTEM_READY) signal.

Functionality During Stacked Operation

Some device features are not available during stacked operation, or are only available in the primary converter. 表 8-8 summarizes the available functionality during stacked operation.

表 8-8. Functionality During Stacked Operation

Function	Primary Device	Secondary Device	Remark
UVLO	Yes	Yes	Common enable signal
OVLO	Yes	Yes	Common enable signal
OCP – Current Limit	Yes	Yes	Individual
OCP – Hiccup OCP	No	No	Do not use during stacked operation
Thermal Shutdown	Yes	Yes	Common enable signal
Power-Good (Window Comparator)	Yes	No	Primary device only
I^2C Interface	Yes	No	Primary device only
DVS	Via I^2C	No	Voltage loop controlled by primary device only
SSC	Via I^2C	No	Daisy-chained from primary device to secondary devices

表 8-8. Functionality During Stacked Operation (続き)

Function	Primary Device	Secondary Device	Remark
SYNC	Yes	Yes	Synchronization clock applied to primary device
Precise Enable	No	No	Only binary enable
Output Discharge	Yes	Yes	Always enabled in secondary devices

Fault Handling During Stacked Operation

In a stacked configuration, there are some faults that only affect individual devices, and other faults that affect all devices. For example, if one device enters current limit, only that device is affected. But a thermal shutdown or undervoltage lockout event in one device disables all devices via the shared enable (SYSTEM_READY) signal. 表 8-9 summarizes the fault handling of the TPS6287x-Q1 devices during stacked operation.

表 8-9. Fault Handling During Stacked Operation

Fault Condition	Device Response	System Response
UVLO	Enable signal pulled low	New soft start
OVLO		
Thermal Shutdown		
Current Limit	Enable signal remains high	Error amplifier clamped
External CLK applied to MODE/SYNC fails	SYNC_OUT and power-stage switch to internal oscillator	System active but switching frequency is not synchronized if clk to a secondary device fails

8.4 Device Functional Modes

8.4.1 Power-On Reset

The device operates in POR mode when the supply voltage is less than the POR threshold.

In POR mode no functions are available and the content of the device registers is not valid.

The device leaves POR mode and enters UVLO mode when the supply voltage increases above the POR threshold.

8.4.2 Undervoltage Lockout

The device operates in UVLO mode when the supply voltage is between the POR and UVLO thresholds.

If the device enters UVLO mode from POR mode, no functions are available. If the device enters UVLO mode from Standby mode, the output discharge function is available. The content of the device registers is valid in UVLO mode.

The device leaves UVLO mode and enters POR mode when the supply voltage decreases below the POR threshold. The device leaves UVLO mode and enters Standby mode when the supply voltage increases above the UVLO threshold.

8.4.3 Standby

The device operates in standby mode when the supply voltage is greater than the UVLO threshold and the device has completed the initialization[2]. Any of the following conditions is true:

- A low level is applied to the EN pin.
- SWEN = 0 in the CONTROL1 register.
- The device junction temperature is greater than the thermal shutdown threshold.
- The supply voltage is greater than the OVLO threshold.

The following functions are available in standby mode:

- I^2C interface
- Output discharge
- Power good

The device leaves standby mode and enters UVLO mode when the supply voltage decreases below the UVLO threshold. The device leaves standby mode and enters on mode when all of the following conditions are true:

- A high-level is applied to the EN pin.
- SWEN = 1 in the CONTROL1 register.
- The device junction temperature is below the thermal shutdown threshold.
- The supply voltage is below the OVLO threshold.

8.4.4 On

The device operates in On mode when the supply voltage is greater than the UVLO threshold and all of the following conditions are true:

- A high-level is applied to the EN pin
- SWEN = 1 in the CONTROL1 register
- The device junction temperature is below the thermal shutdown threshold
- The supply voltage is below the OVLO threshold

All functions are available in On mode.

The device leaves On mode and enters UVLO mode when the supply voltage decreases below the UVLO threshold. The device leaves On mode and enters the Standby mode when any of the following conditions is true:

- A low level is applied to the EN pin
- SWEN = 0 in the CONTROL1 register
- The device junction temperature is greater than the thermal shutdown threshold
- The supply voltage is greater than the OVLO threshold

8.5 Programming

8.5.1 Serial Interface Description

I2C™ is a 2-wire serial interface developed by Philips Semiconductor, now NXP Semiconductors (see I^2C-Bus Specification and User´s Manual, Revision 6, 4 April 2014). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All the I^2C compatible devices connect to the I^2C bus through open drain I/O pins, SDA and SCL. A controller, usually a microcontroller or a digital signal processor, controls the bus. The controller is responsible for generating the SCL signal and device addresses. The controller also generates specific conditions that indicate the START and STOP of data transfer. A target receives or transmits data on the bus under control of the controller.

[2] The device initializes for 400 µs (typical) after the supply voltage increases above the UVLO threshold voltage following a device power-on reset (if the supply voltage decreases below the UVLO threshold but not below the POR threshold, the device does not reinitialize when the supply voltage increases again). During initialization the device reads the state of the VSEL, FSEL, and SYNC_OUT pins.

The TPS6287x-Q1 device operates as a target and supports the following data transfer *modes*, as defined in the I²C-Bus Specification: standard mode (100kbps) and fast mode (400kbps) and fast mode plus (1Mbps). The interface adds flexibility to the power supply design, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as the input voltage remains above 1.4V.

The data transfer protocol for standard and fast modes is exactly the same, therefore the modes are referred to as F/S-mode in this document. The device supports 7-bit addressing; general call addresses are not supported. The device 7-bt address is selected by the status of pin VSEL (see 表 8-5).

The protocol for high-speed mode is different from F/S-mode and is referred to as HS-mode.

TI recommends that the I²C controller initiates a STOP condition on the I²C bus after the initial power up of SDA and SCL pullup voltages to make sure of reset of the I²C engine.

8.5.2 Standard-, Fast-, Fast-Mode Plus Protocol

The controller initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in 図 8-17. All I²C-compatible devices must recognize a start condition.

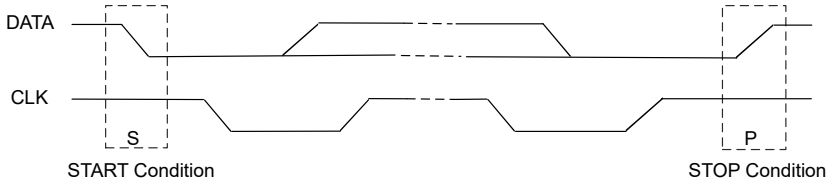


図 8-17. START and STOP Conditions

The controller then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the controller makes sure that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see 図 8-18). All devices recognize the address sent by the primary device and compare the address to the internal fixed addresses. Only the target with a matching address generates an acknowledge (see 図 8-19) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the controller knows that the communication link with a target has been established.

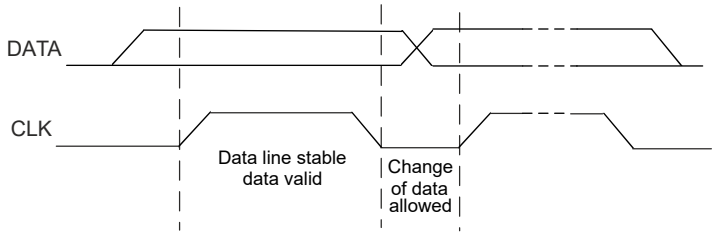


図 8-18. Bit Transfer on the Serial Interface

The controller generates further SCL cycles to either transmit data to the target (write command; R/$\overline{W}$ = 0) or receive data from the target (read command; R/$\overline{W}$ = 1). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the controller or by the target, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the controller generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see 図 8-17). This releases the bus and stops the communication link with the addressed target. All I²C compatible devices must recognize the stop condition. Upon the receipt of a stop

condition, all devices know that the bus is released, and the deviceswait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section results in 00h being read out.

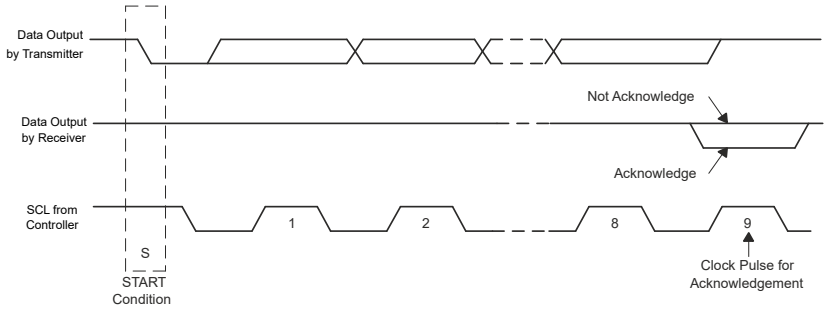


図 8-19. Acknowledge on the I²C Bus

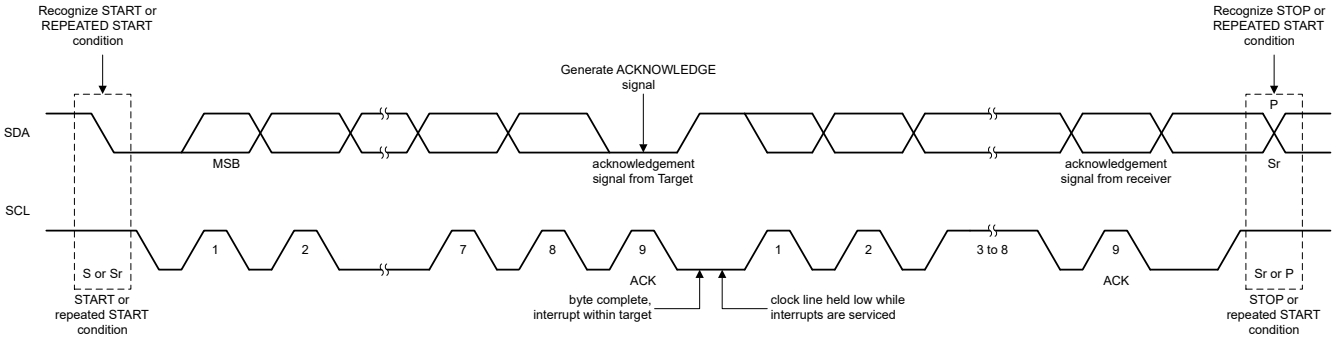


図 8-20. Bus Protocol

8.5.3 HS-Mode Protocol

The controller generates a start condition followed by a valid serial byte containing HS controller code 00001XXX. This transmission is made in F/S-mode at no more than 400Kbps. No device is allowed to acknowledge the HS controller code, but all devices must recognize the code and switch the internal setting to support 3.4Mbps operation.

The controller then generates a *repeated start condition* (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S-mode, except that transmission speeds up to 3.4Mbps are allowed. A stop condition ends the HS-mode and switches all the internal settings of the target devices to support the F/S-mode. Instead of using a stop condition, repeated start conditions must be used to secure the bus in HS-mode.

Attempting to read data from register addresses not listed in this section results in 00h being read out.

8.5.4 I²C Update Sequence

This requires a start condition, a valid I²C address, a register address byte, and a data byte for a single update. After the receipt of each byte, device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the device. The device performs an update on the falling edge of the acknowledge signal that follows the LSB byte.

図 8-21. : "Write" Data Transfer Format in Standard-, Fast, Fast-Plus Modes

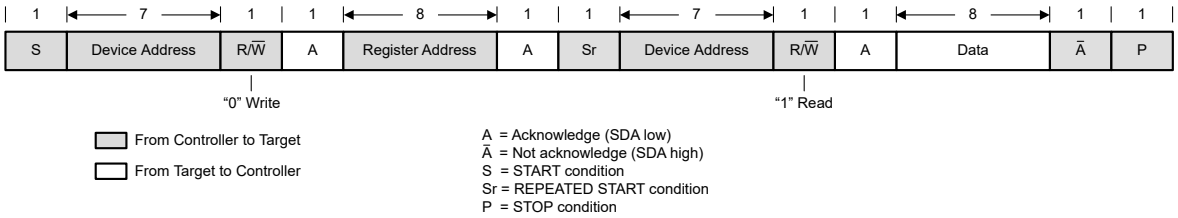


図 8-22. "Read" Data Transfer Format in Standard-, Fast, Fast-Plus Modes

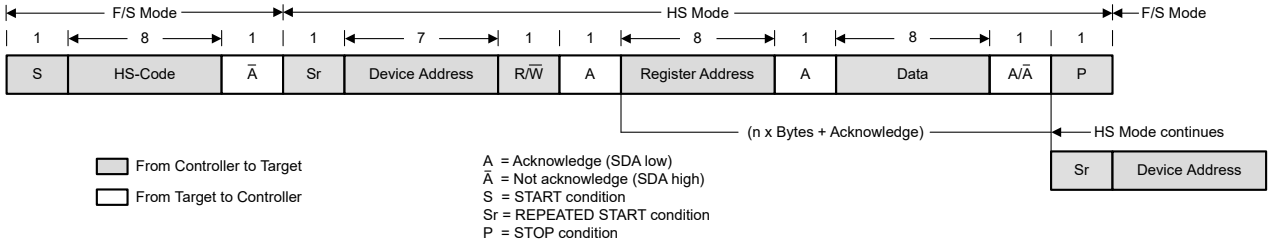


図 8-23. Data Transfer Format in HS-Mode

8.5.5 I²C Register Reset

The I²C registers can be reset by:

- pulling the input voltage below 1.4V (typ).
- or setting the Reset bit in the CONTROL register. When Reset is set to 1, all registers are reset to the default values and a new startup is begun immediately. After t_{Delay}, the I²C registers can be programmed again.

8.5.6 Dynamic Voltage Scaling (DVS)

To optimize the power consumption of the system, the output voltage of the TPS6287x-Q1 can be adapted during operation based on the actual power requirement of the load.

The device starts up into the default output voltage selected through the external VSEL pin or the settings in the VSET register. The output voltage can be dynamically adapted via the I²C interface by writing the new target output voltage to the VSET register. The output voltage then increases or decrease to the desired value with the voltage ramp speed defined in the CONTROL1 register.

Switching between different output voltage ranges

TPS6287x-Q1 devices offer three different output voltages ranges as defined in the CONTROL2 register. To change the output voltage range of TPS6287x-Q1, first step to the closest output voltage value within the currently used range, then change the VRANGE bit in the CONTROL2 register to the next VRANGE setting. After that set the target output voltage in the VSET register.

Note that a change in the output voltage range always must be followed by writing to the VSET Register, even though the output voltage does not change. The code in the VSET register must be updated to the correct value in the new range.

9 Device Registers

表 9-1 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in 表 9-1 should be considered as reserved locations and the register contents should not be modified.

表 9-1. DEVICE Registers

Address	Acronym	Register Name	Section
0h	VSET	Output Voltage Setpoint	セクション 9.1
1h	CONTROL1	Control 1	セクション 9.2
2h	CONTROL2	Control 2	セクション 9.3
3h	CONTROL3	Control 3	セクション 9.4
4h	STATUS	Status	セクション 9.5

Complex bit access types are encoded to fit into small table cells. 表 9-2 shows the codes that are used for access types in this section.

表 9-2. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

9.1 VSET Register (Address = 0h) [Reset = XXh]

VSET is shown in 表 9-3.

Return to the Summary Table.

This register controls the output voltage setpoint

表 9-3. VSET Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VSET	R/W	xxxxxxxxb	Output voltage setpoint (see also the range-setting bits in the CONTROL2 register). Range 1: Output voltage setpoint = 0.4 V + VSET[7:0] × 1.25 mV Range 2: Output voltage setpoint = 0.4 V + VSET[7:0] × 2.5 mV Range 3: Output voltage setpoint = 0.4 V + VSET[7:0] × 5 mV The state of the VSEL pin during power up determines the reset value.

9.2 CONTROL1 Register (Address = 1h) [Reset = X8h]

CONTROL1 is shown in 表 9-4.

Return to the Summary Table.

This register controls various device configuration options

表 9-4. CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESET	R/W	0b	Reset device. 0b = No effect 1b = The device is powered down, the pin status is read and all registers are reset to their default value. The device is then powered up again starting with a soft-start cycle. Reading this bit always returns 0.
6	SSCEN	R/W	xb	Spread spectrum clocking enable. Please see the DEVICE OPTIONS table if SSC is enabled by default. 0b = SSC operation disabled 1b = SSC operation enabled
5	SWEN	R/W	1b	Software enable. 0b = Switching disabled (register values retained) 1b = Switching enabled (without the enable delay)
4	FPWMEN	R/W	0b	Forced-PWM enable. 0b = Power-save operation enabled 1b = Forced-PWM operation enabled This bit is logically ORed with the MODE/SYNC pin: If a high level or a synchronization clock is applied to the the MODE/SYNC pin, the device operates in Forced-PWM, regardless of the state of this bit.
3	DISCHEN	R/W	1b	Output discharge enable. 0b = Output discharge disabled. 1b = Output discharge enabled.
2	HICCUPEN	R/W	0b	Hiccup operation enable. 0b = Hiccup operation disabled 1b = Hiccup operation enabled. Do not enable Hiccup operation during stacked operation
1-0	VRAMP	R/W	00b	Output voltage ramp speed when changing from one output voltage setting to another. 00b = 10 mV/µs 01b = 5 mV/µs 10b = 1.25 mV/µs 11b = 0.5 mV/µs

9.3 CONTROL2 Register (Address = 2h) [Reset = 0Ah]

CONTROL2 is shown in 表 9-5.

Return to the Summary Table.

This register controls various device configuration options

表 9-5. CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000b	Reserved for future use. To ensure compatibility with future device variants, program these bits to 0.
4	SYNC_OUT_PHASE	R/W	0b	Phase shift of SYNC_OUT with reference to internal clk or external clk applied at MODE/SYNC. 0b = SYNC_OUT is phase shifted by 120° 1b = SYNC_OUT is phase shifted by 180° The phase relation of 180° is only valid from the primary to the first secondary converter.
3-2	VRANGE	R/W	10b	Output voltage range. 00b = 0.4 V to 0.71875 V in 1.25-mV steps 01b = 0.4 V to 1.0375 V in 2.5-mV steps 10b = 0.4 V to 1.675 V in 5-mV steps 11b = 0.4 V to 1.675 V in 5-mV steps
1-0	SSTIME	R/W	10b	Soft-start ramp time. 00b = 0.5 ms 01b = 0.77 ms 10b = 1 ms 11b = 2 ms

9.4 CONTROL3 Register (Address = 3h) [Reset = 0Xh]

CONTROL3 is shown in 表 9-6.

Return to the Summary Table.

This register controls various device configuration options

表 9-6. CONTROL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	00000b	Reserved for future use. To ensure compatibility with future device variants, program these bits to 0.
2	DROOPEN	R/W	xb	Droop compensation enable. Please see the DEVICE OPTIONS table if droop compensation is enabled by default. 0b = droop compensation disabled 1b = droop compensation enabled
1	SINGLE	R/W	0b	Single operation. This bit controls the internal EN pulldown and SYNCOUT functions. 0b = EN pin pulldown and SYNCOUT enabled 1b = EN pin pulldown and SYNCOUT disabled. Do not set during stacked operation
0	PGBLNKDVS	R/W	0b	Power-good blanking during DVS. 0b = PG pin reflects the output of the window comparator 1b = PG pin is high impedance during DVS

9.5 STATUS Register (Address = 4h) [Reset = 00h]

STATUS is shown in 表 9-7.

Return to the Summary Table.

This register returns the device status flags

表 9-7. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved for future use. To ensure compatibility with future device variants, ignore these bits.
5	HICCUP	R	0b	Hiccup. This bit reports whether a hiccup event occurred since the last time the STATUS register was read. 0b = No hiccup event occured 1b = A hiccup event occurred
4	ILIM	R	0b	Current limit. This bit reports whether an current limit event occurred since the last time the STATUS register was read. 0b = No current limit event occured 1b = An current limit event occurred
3	TWARN	R	0b	Thermal warning. This bit reports whether a thermal warning event occurred since the last time the STATUS register was read. 0b = No thermal warning event occurred 1b = A thermal warning event occurred
2	TSHUT	R	0b	Thermal shutdown. This bit reports whether a thermal shutdown event occurred since the last time the STATUS register was read. 0b = No thermal shutdown event occurred 1b = A thermal shutdown event occurred
1	PBUV	R	0b	Power-bad undervoltage. This bit reports whether a power-bad event (output voltage too low) occurred since the last time the STATUS register was read. 0b = No power-bad undervoltage event occurred 1b = A power-bad undervoltage event occurred
0	PBOV	R	0b	Power-bad overvoltage. This bit reports whether a power-bad event (output voltage too high) occurred since the last time the STATUS register was read. 0b = No power-bad overvoltage event occurred 1b = A power-bad overvoltage event occurred

10 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

10.1 Application Information

The following section discusses selection of the external components to complete the power supply design for a typical application.

10.2 Typical Application

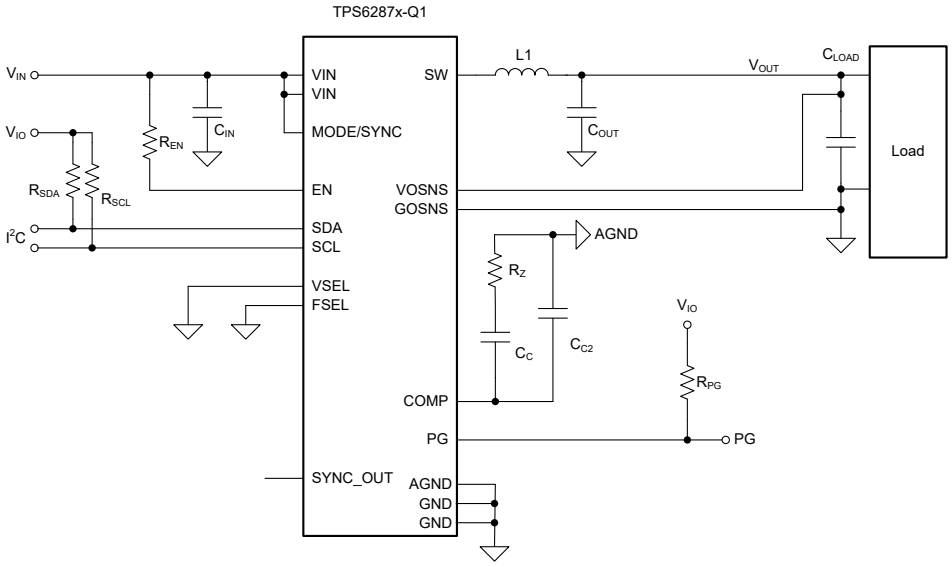


図 10-1. Typical Application Schematic

10.2.1 Design Requirements

表 10-1 lists the operating parameters for this application example.

表 10-1. Design Parameters

SYMBOL	PARAMETER	VALUE
V_{IN}	Input voltage	3.3V
V_{OUT}	Output voltage	0.75V
TOL_{VOUT}	Output voltage tolerance allowed by the application	±3.3%
TOL_{DC}	Output voltage tolerance of the TPS6287x-Q1 (DC accuracy)	±0.8%
ΔI_{OUT}	Output current load step	±7.5A
t_r	Load step rise time	1µs
t_f	Load step fall time	1µs
f_{SW}	Switching frequency	2.25MHz
L	Inductance	80nH
g_m	Error amplifier transconductance	1.5mS

表 10-1. Design Parameters (続き)

SYMBOL	PARAMETER	VALUE
τ	Emulated current time constant	12.5µs
k_{BW}	Ratio of switching frequency to converter bandwidth (must be ≥ 4)	4
k_{COUT}	Ratio of minimum to maximum output capacitance (typically 2)	2
R_{PG}	Pullup resistor on power-good output	10kΩ
R_{EN}	Pullup resistor on enable	22kΩ
R_{SCL}, R_{SDA}	Pullup resistors on SDA and SCL	680Ω

Preliminary Calculations

With a total allowable output voltage tolerance of ±3.3% and a maximum DC error of ±0.8%, the allowable output voltage tolerance during a load step is given by:

$$\Delta V_{OUT} = \pm V_{OUT} \times (TOL_{VOUT} - TOL_{DC}) \quad (4)$$

$$\Delta V_{OUT} = \pm 0.75 \times (0.033 - 0.008) = \pm 18.75\ mV \quad (5)$$

10.2.2 Detailed Design Procedure

The following subsections describe how to calculate the external components required to meet the specified transient requirements of a given application. The calculations include the worst-case variation of components and use the RMS method to combine the variation of uncorrelated parameters.

10.2.2.1 Inductor Selection

The TPS6287x-Q1 devices have been optimized for inductors in the the range 42nH to 200nH. If the transient response of the converter is limited by the slew rate of the current in the inductor, using a smaller inductor can improve performance. However, the output ripple current increases as the value of the inductor decreases, and higher output current ripple generates higher output voltage ripple, which adds to the transient over- or undershoot. The optimum configuration for a given application is a trade-off between a number of parameters. We recommend a starting value of 60nH to 80nH for typical applications.

The inductor ripple current is given by:

$$I_{L(PP)} = \frac{V_{OUT}}{V_{IN}}\left(\frac{V_{IN} - V_{OUT}}{L \times f_{sw}}\right) \quad (6)$$

$$I_{L(PP)} = \frac{0.75}{3.3}\left(\frac{3.3 - 0.75}{80 \times 10^{-9} \times 2.25 \times 10^{6}}\right) A = 3.22\ A \quad (7)$$

表 10-2 lists a number of inductors suitable for use with this application. This list is not exhaustive, however, and other inductors from other manufacturers may also be suitable.

表 10-2. Typical Inductors

PART NUMBER	INDUCTANCE [µH]	CURRENT [A]	DC RESISTANCE	Notes	DIMENSIONS [LxWxH] mm	MANUFACTURER
IHSR2525CZ-5A	0.056µH	45	0.38mΩ	For f ≥ 2.25MHz	6.65 × 6.65 × 3	Vishay
XEL4030-101ME	0.10µH	22	1.5mΩ	For f ≥ 1.5MHz	4 × 4 × 3.2	Coilcraft
744302010	0.105µH	30	0.235mΩ	For f ≥ 1.5MHz	7 × 7 × 4.8	Wurth
XGL5030-161ME	0.16µH	25	1.3mΩ	For f ≥ 1.5MHz	5.3 × 5.5 × 3	Coilcraft
744300006	0.06µH	37	0.22mΩ	For f ≥ 2.25MHz	8.64 × 6.35 × 4.5	Wurth
CLT32-55N	0.055µH	28	1mΩ	For f ≥ 2.25MHz	2.5 × 3.2 × 2.5	TDK

表 10-2. Typical Inductors (続き)

PART NUMBER	INDUCTANCE [µH]	CURRENT [A]	DC RESISTANCE	Notes	DIMENSIONS [LxWxH] mm	MANUFACTURER
CLT32-42N	0.042µH	28	1mΩ	For f ≥ 2.25MHz	2.5 × 3.2 × 2.5	TDK
HPL505032F1060MRD3P	0.06µH	34	0.7mΩ	For f ≥ 2.25MHz	5 × 5 × 3.2	TDK
HPL505028F080MRD3P	0.08 µH	34	0.8mΩ	For f ≥ 2.25MHz	5 × 5 × 3.2	TDK

10.2.2.2 Selecting the Input Capacitors

As with all buck converters, the input current of the TPS6287x-Q1 devices is discontinuous. The input capacitors provide a low-impedance energy source for the device, and the value, type, and location are critical for correct operation. TI recommends low-ESR multilayer ceramic capacitors for best performance. In practice, the total input capacitance typically comprises a combination of different capacitors, in which larger capacitors provide the decoupling at lower frequencies and smaller capacitors provide the decoupling at higher frequencies.

The TPS6287x-Q1 devices feature a *butterfly* layout with two VIN pin pairs on opposite sides of the package. This allows the input capacitors to be placed symmetrically on the PCB such that the electromagnetic fields generated cancel each other out, thereby reducing EMI.

The duty cycle of the converter is given by:

$$D = \frac{V_{OUT}}{\eta \times V_{IN}} \tag{8}$$

where:

- V_{IN} is the input voltage
- V_{OUT} is the output voltage
- η is the efficiency

$$D = \frac{0.75}{0.9 \times 3.3} = 0.253 \tag{9}$$

The value of input capacitance needed to meet the input voltage ripple requirements is given by:

$$C_{IN} = \frac{D \times (1 - D) \times I_{OUT}}{V_{IN(PP)} \times f_{sw}} \tag{10}$$

where:

- D is the duty cycle
- f_{sw} is the switching frequency
- $V_{IN(PP)}$ is the input voltage ripple
- I_{OUT} is the output current

$$C_{IN} = \frac{0.253 \times (1 - 0.253) \times 11.3}{0.1 \times 2.25 \times 10^{6}} F = 9.5\ \mu F \tag{11}$$

The value of C_{IN} calculated with 式 10 is the *effective* capacitance after all derating, tolerance, and ageing effects have been considered. We recommend multilayer ceramic capacitors with an X7R dielectric (or similar) for C_{IN}, and these capacitors must be placed as close to the VIN and GND pins as possible, so as to minimize the loop area.

表 10-3 lists a number of capacitors suitable for this application. This list is not exhaustive, however, and other capacitors from other manufacturers may also be suitable.

表 10-3. List of Recommended Input Capacitors

CAPACITANCE	DIMENSIONS mm (inch)	VOLTAGE RATING	MANUFACTURER, PART NUMBER
470nF ±10%	1005 (0402)	10V	Murata, GCM155C71A474KE36D
470nF ±10%	1005 (0402)	10V	TDK, CGA2B3X7S1A474K050BB
10µF ±10%	2012 (0805)	10V	Murata, GCM21BR71A106KE22L
10µF ±10%	2012 (0805)	10V	TDK, CGA4J3X7S1A106K125AB
22µF ±10%	3216 (1206)	10V	Murata, GCM31CR71A226KE02L
22µF ±20%	3216 (1206)	10V	TDK, CGA5L1X7S1A226M160AC

10.2.2.3 Selecting the Compensation Resistor

Use 式 12 to calculate the recommended value of compensation resistor R_Z:

$$R_Z = \frac{1}{g_m}\left(\frac{\pi \times \Delta I_{OUT} \times L}{4 \times \tau \times \Delta V_{OUT}}\right)(1 + TOL_{IND}) \tag{12}$$

$$\mathrm{R_Z} = \frac{1}{1.5 \times 10^{-3}}\left(\frac{\pi \times 7.5 \times 80 \times 10^{-9}}{4 \times 12.5 \times 10^{-6} \times 18.75 \times 10^{-3}}\right)(1 + 0.2\ )\Omega = 1.61\ \mathrm{k\Omega} \tag{13}$$

Rounding up, the closest standard value from the E24 series is 1.8kΩ.

10.2.2.4 Selecting the Output Capacitors

In practice, the total output capacitance typically comprises a combination of different capacitors, in which larger capacitors provide the load current at lower frequencies and smaller capacitors provide the load current at higher frequencies. The value, type, and location of the output capacitors are critical for correct operation. TI recommends low-ESR multilayer ceramic capacitors with an X7R dielectric (or similar) for best performance.

The TPS6287x-Q1 devices feature a butterfly layout with two GND pins on opposite sides of the package. This allows the output capacitors to be placed symmetrically on the PCB such that the electromagnetic fields generated cancel each other out, thereby reducing EMI.

The transient response of the converter is defined by one of two criteria:

- The loop bandwidth, which must be at least 4 times smaller than the switching frequency.
- The slew rate of the current through the inductor and the output capacitance.

  In typical low-output-voltage application, this is limited by the value of the output voltage and the inductors.

Which of the above criteria applies in any given application depends on the operating conditions and component values used. We therefore recommend calculating the output capacitance for both cases, and selecting the higher of the two values.

If the converter remains in regulation, the minimum output capacitance required is given by:

$$C_{OUT(min)(reg)} = \left(\frac{\tau \times g_m \times R_Z}{2 \times \pi \times L \times \frac{f_{SW}}{4}}\right)\left(1 + \sqrt{TOL_{IND}{}^2 + TOL_{fSW}{}^2}\right) \tag{14}$$

$$C_{OUT(min)(reg)} = \left(\frac{12.5 \times 10^{-6} \times 1.5 \times 10^{-3} \times 1.8 \times 10^{3}}{2 \times \pi \times 80 \times 10^{-9} \times \frac{2.25 \times 10^{6}}{4}}\right)\left(1 + \sqrt{20\%^2 + 10\%^2}\right)F = 146\ \mu F \tag{15}$$

If the converter loop saturates, the minimum output capacitance is given by:

$$C_{OUT(min)(sat)} = \frac{1}{\Delta V_{OUT}} \left(\frac{L \times \left(\Delta I_{OUT} + \frac{I_{L(PP)}}{2} \right)^2}{2 \times V_{OUT}} - \frac{\Delta I_{OUT} \times t_t}{2} \right) (1 + TOL_{IND}) \quad (16)$$

$$C_{OUT(min)(sat)} = \frac{1}{18.75 \times 10^{-3}} \left(\frac{80 \times 10^{-9} \times \left(7.5 + \frac{3.22}{2} \right)^2}{2 \times 0.75} - \frac{7.5 \times 1 \times 10^{-6}}{2} \right) (1 + 20\%)\ F = 43\ \mu F \quad (17)$$

In this case, choose $C_{OUT(min)}$ = 146µF, as the larger of the two values, for the output capacitance.

When calculating worst-case component values, use the value calculated above as the *minimum* output capacitance required. For ceramic capacitors, the *nominal* capacitance when considering tolerance, DC bias, temperature, and aging effects is typically two times the minimum capacitance. In this case the nominal capacitance is thus 292µF.

表 10-4. List of Recommended Output Capacitors

CAPACITANCE	DIMENSIONS mm (inch)	VOLTAGE RATING	MANUFACTURER, PART NUMBER
22µF ±20%	2012 (0805)	6.3V	TDK, CGA4J1X7T0J226M125AC
22µF ±10%	2012 (0805)	6.3V	Murata, GCM31CR71A226KE02
47µF ±20%	3216 (1206)	4V	TDK, CGA5L1X7T0G476M160AC
47µF ±20%	3225 (1210)	6.3V	Murata, GCM32ER70J476ME19
100µF ±20%	3225 (1210)	4V	TDK, CGA6P1X7T0G107M250AC
100µF ±20%	3216 (1210)	6.3V	Murata, GRT32EC70J107ME13

10.2.2.5 Selecting the Compensation Capacitor C_C

First, use 式 18 to calculate the bandwidth of the loop:

$$BW = \frac{\tau \times g_m \times R_Z}{2 \times \pi \times L \times C_{OUT,min} \times k_{COUT}} \quad (18)$$

$$BW = \frac{12.5 \times 10^{-6} \times 1.5 \times 10^{-3} \times 1.8 \times 10^{3}}{2 \times \pi \times 80 \times 10^{-9} \times 146 \times 10^{-6} \times 2} = 230kHz \quad (19)$$

Use 式 20 to calculate the recommended value of C_C.

$$C_C = \frac{k_{BW}}{2 \times \pi \times BW \times R_Z} \quad (20)$$

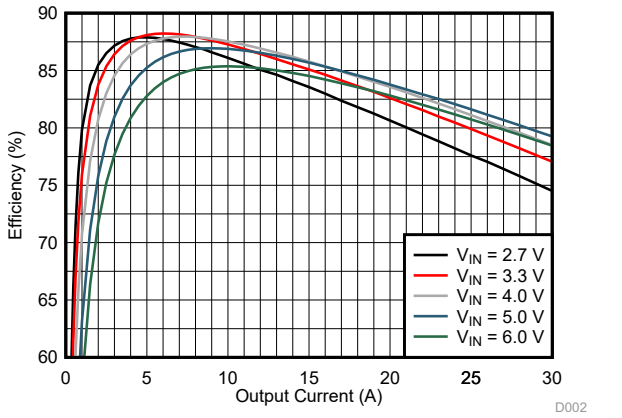
$$C_C = \frac{4}{2 \times \pi \times 230 \times 10^{3} \times 1.8 \times 10^{3}} = 1.54\ nF \quad (21)$$

The closest standard value from the E12 series is 1.5nF.

10.2.2.6 Selecting the Compensation Capacitor C_{C2}

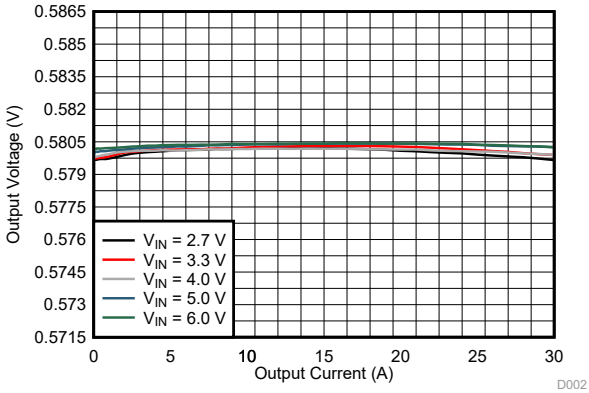
The compensation capacitor C_{C2} is an optional capacitor that we recommend you include to bypass high-frequency noise from the COMP pin. The value of this capacitor is not critical; 10pF or 22pF capacitors are suitable for typical applications.

10.2.3 Application Curves



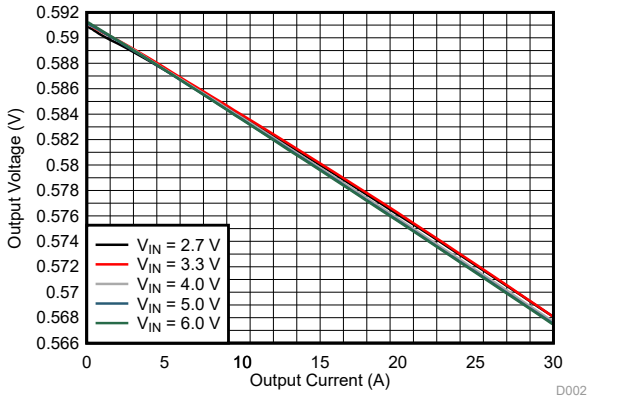
V_{OUT} = 0.58V PWM T_A = 25°C

図 10-2. Efficiency Versus Output Current



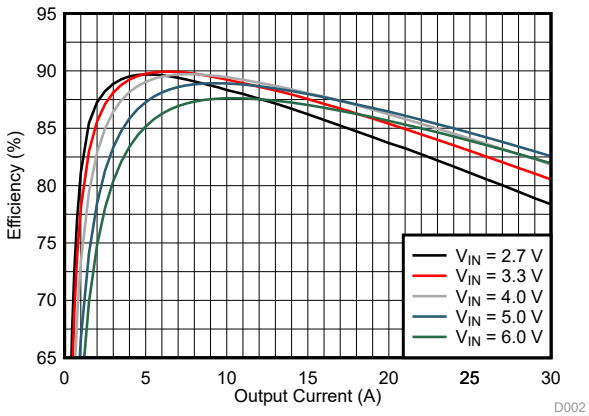
V_{OUT} = 0.58V PWM; droop disabled T_A = 25°C

図 10-3. Output Voltage Versus Output Current



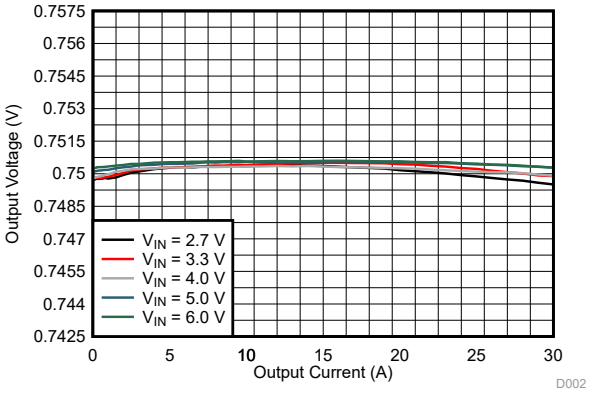
V_{OUT} = 0.58V PWM; TPS62877 droop enabled T_A = 25°C

図 10-4. Output Voltage Versus Output Current



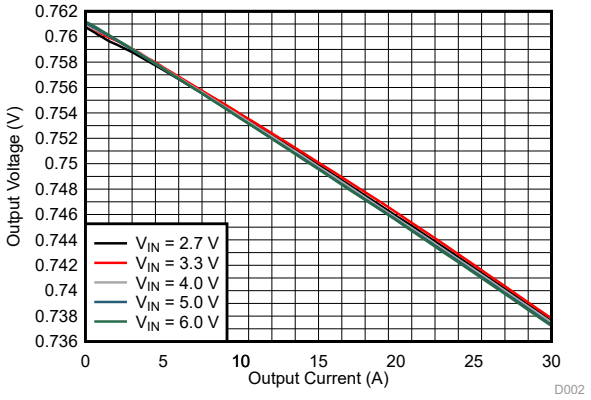
V_{OUT} = 0.75V PWM T_A = 25°C

図 10-5. Efficiency Versus Output Current



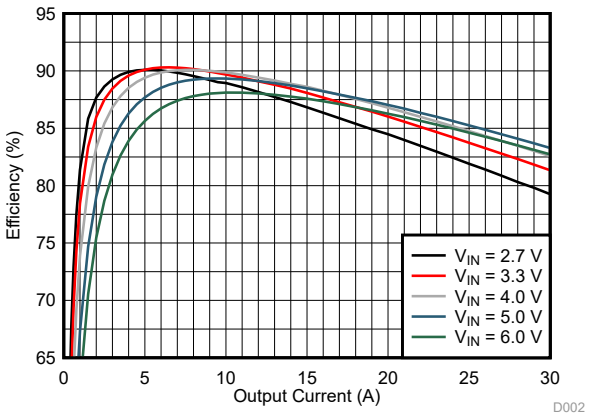
V_{OUT} = 0.75V PWM; droop disabled T_A = 25°C

図 10-6. Output Voltage Versus Output Current



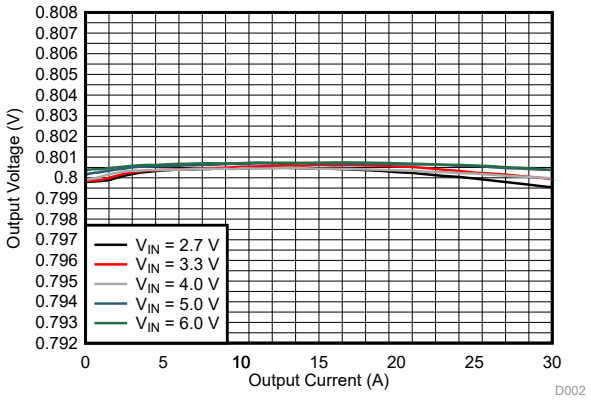
V_{OUT} = 0.75V PWM; TPS62877 droop enabled T_A = 25°C

図 10-7. Output Voltage Versus Output Current



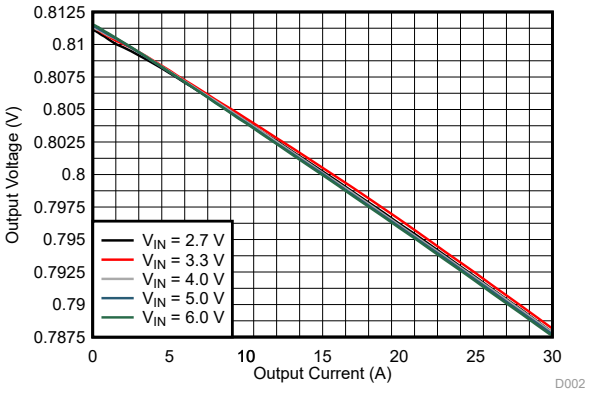
V_{OUT} = 0.8V PWM T_A = 25°C

図 10-8. Efficiency Versus Output Current



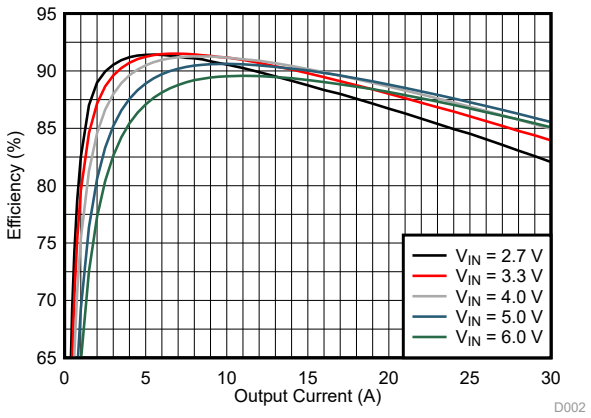
V_{OUT} = 0.8V PWM; droop disabled T_A = 25°C

図 10-9. Output Voltage Versus Output Current



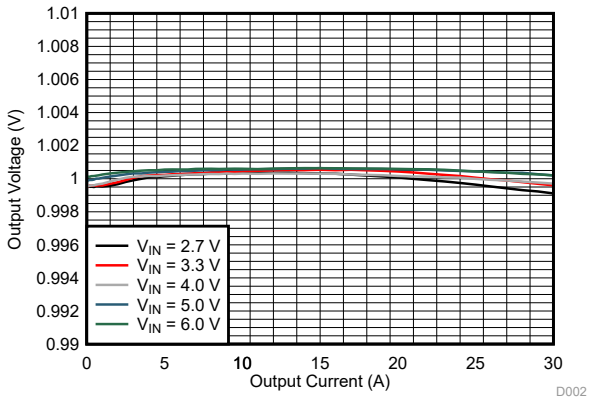
V_{OUT} = 0.8V PWM; TPS62877 droop enabled T_A = 25°C

図 10-10. Output Voltage Versus Output Current



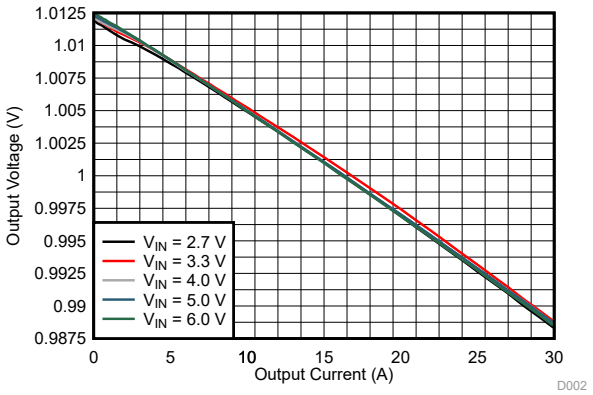
V_{OUT} = 1.0V PWM T_A = 25°C

図 10-11. Efficiency Versus Output Current



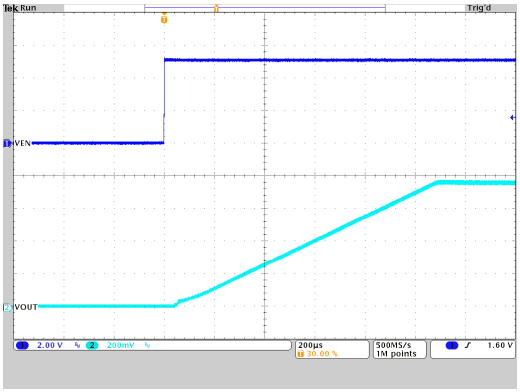
V_{OUT} = 1.0V PWM; droop disabled T_A = 25°C

図 10-12. Output Voltage Versus Output Current



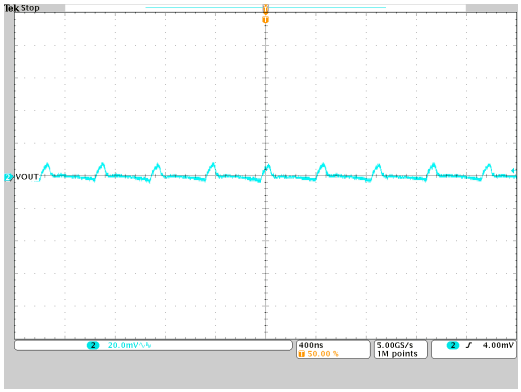
V_{OUT} = 1.0V PWM; TPS62877 droop enabled T_A = 25°C

図 10-13. Output Voltage Versus Output Current



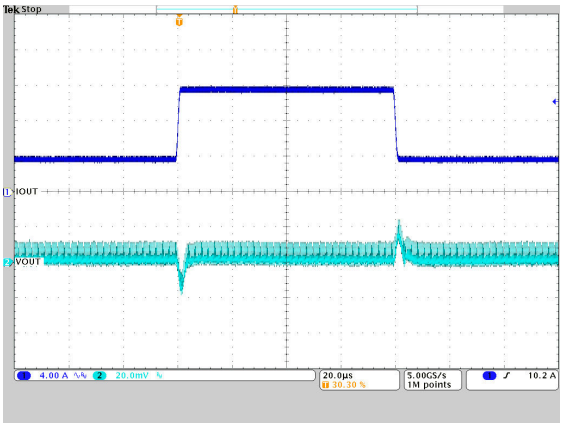
V_{OUT} = 0.75V PWM T_A = 25°C
V_{IN} = 5V R_{LOAD} = 66mΩ

図 10-14. Start-Up Timing



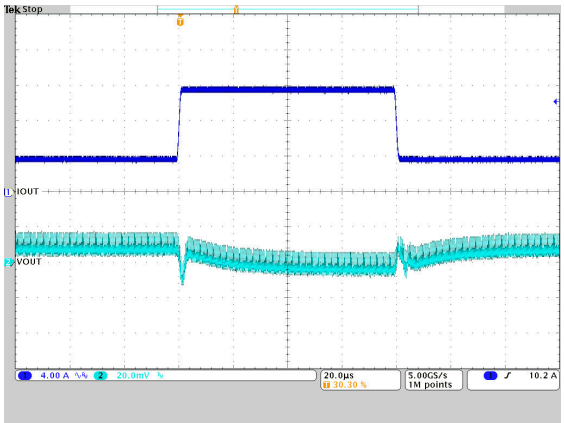
V_{OUT} = 0.75V PWM T_A = 25°C
V_{IN} = 5V R_{LOAD} = 66mΩ

図 10-15. Output Voltage Ripple



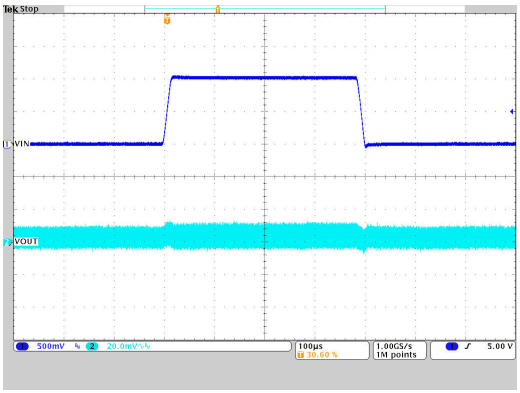
V_{OUT} = 0.75V PWM, TPS62874 droop disabled T_A = 25°C
V_{IN} = 5V Iout = 3.8A to 11.3A to 3.8A

図 10-16. Load Transient Response



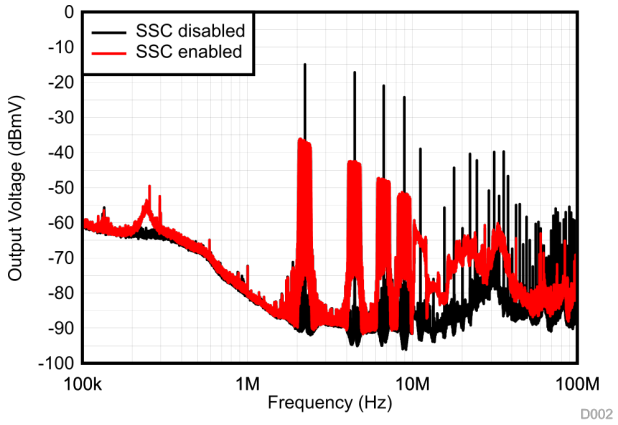
V_{OUT} = 0.75V PWM, TPS62874 droop enabled T_A = 25°C
V_{IN} = 5V Iout = 3.8A to 11.3A to 3.8A

図 10-17. Load Transient Response



V_{OUT} = 0.75V PWM T_A = 25°C
V_{IN} = 4.5V to 5.5V to 4.5V I_{OUT} = 11.3A

図 10-18. Line Transient Response



V_{OUT} = 0.75V PWM T_A = 25°C
V_{IN} = 5V I_{OUT} = 11.3A

図 10-19. Output Voltage Noise

10.3 Typical Application Using Two TPS62876-Q1 in a Stacked Configuration

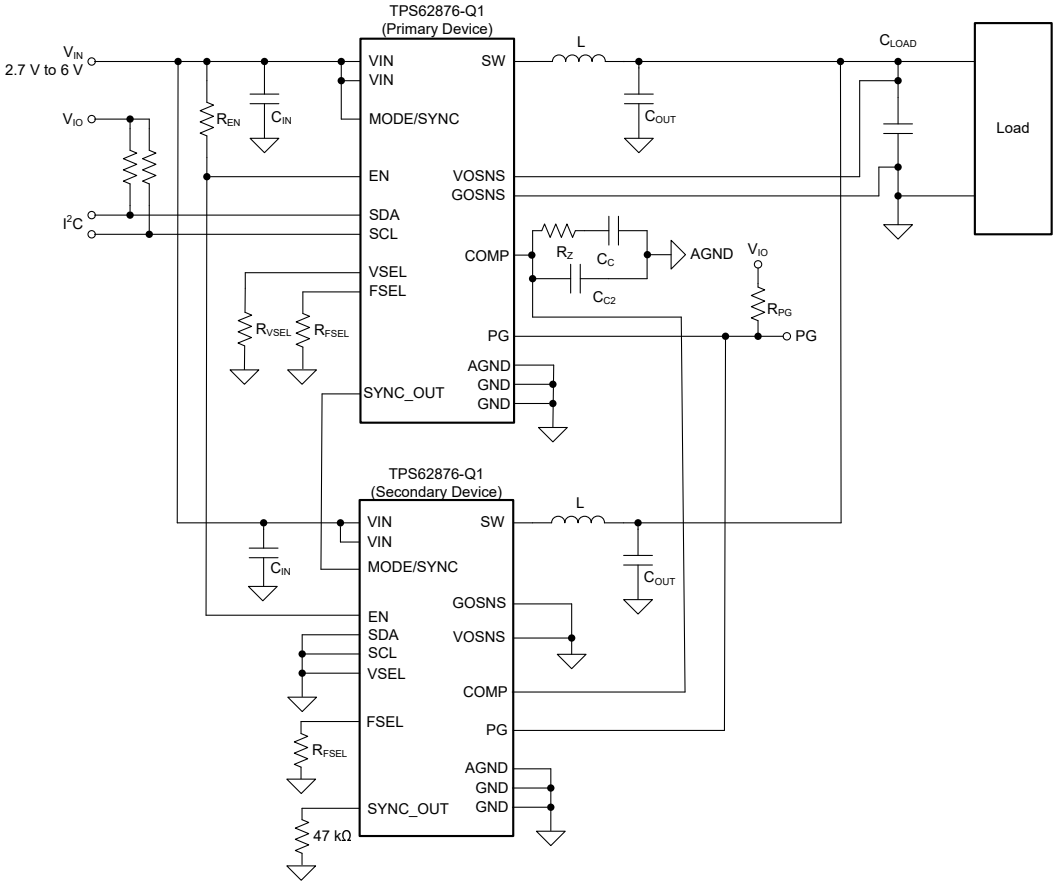


図 10-20. Stacking Two Devices

10.3.1 Design Requirements For Two Stacked Devices

表 10-5 lists the operating parameters for this application example.

表 10-5. Design Parameters

SYMBOL	PARAMETER	VALUE
V_{IN}	Input voltage	3.3V
V_{OUT}	Output voltage	0.8V
TOL_{VOUT}	Output voltage tolerance allowed by the application	±4%
TOL_{DC}	Output voltage tolerance of the TPS62876-Q1 (DC accuracy)	±0.8%
ΔI_{OUT}	Output current load step	±24A
t_r	Load step rise time	1µs
t_f	Load step fall time	1µs
f_{SW}	Switching frequency	2.25MHz
L	Inductance	56nH
g_m	Error amplifier transconductance	1.5mS
τ	Emulated current time constant	12.5µs
k_{BW}	Ratio of switching frequency to converter bandwidth (must be ≥4)	4

表 10-5. Design Parameters (続き)

SYMBOL	PARAMETER	VALUE
N_Φ	Number of phases (number of stacked devices)	2
k_{COUT}	Ratio of minimum to maximum output capacitance (typically 2)	2
R_{PG}	Pullup resistor on power-good output	10kΩ
R_{EN}	Pullup resistor on enable	22kΩ
R_{SCL}, R_{SDA}	Pullup resistors on SDA and SCL	680Ω

Preliminary Calculations

With a total allowable output voltage tolerance of ±4% and a maximum DC error of ±0.8%, the allowable output voltage tolerance during a load step is given by:

$$\Delta V_{OUT} = \pm V_{OUT} \times (TOL_{VOUT} - TOL_{DC}) \quad (22)$$

$$\Delta V_{OUT} = \pm 0.8 \times (0.04 - 0.008) = \pm 25.6\ mV \quad (23)$$

10.3.2 Detailed Design Procedure

10.3.2.1 Selecting the Compensation Resistor

The calculation for a stack of two converters is similar to the single device expect that the parameter "number of phases" N_Φ is added to the equations. Use 式 24 to calculate the recommended value of compensation resistor R_Z:

$$R_Z = \frac{1}{g_m}\left(\frac{\pi \times \Delta I_{OUT} \times L}{4 \times \tau \times N_\phi \times \Delta V_{OUT}}\right)(1 + TOL_{IND}) \quad (24)$$

$$R_Z = \frac{1}{1.5 \times 10^{-3}}\left(\frac{\pi \times 24 \times 56 \times 10^{-9}}{4 \times 12.5 \times 10^{-6} \times 2 \times 25.6 \times 10^{-3}}\right)(1 + 0.2)\Omega = 1.32\ k\Omega \quad (25)$$

Rounding up, the closest standard value from the E24 series is 1.5Ω.

10.3.2.2 Selecting the Output Capacitors

If the converter remains in regulation, the minimum output capacitance required is given by:

$$C_{OUT(min)(reg)} = \left(\frac{\tau \times g_m \times R_Z}{2 \times \pi \times \frac{L}{N_\phi} \times \frac{f_{SW}}{4}}\right)\left(1 + \sqrt{TOL_{IND}^2 + TOL_{fSW}^2}\right) \quad (26)$$

$$C_{OUT(min)(reg)} = \left(\frac{12.5 \times 10^{-6} \times 1.5 \times 10^{-3} \times 1.5 \times 10^{3}}{2 \times \pi \times \frac{56 \times 10^{-9}}{2} \times \frac{2.25 \times 10^{6}}{4}}\right)\left(1 + \sqrt{20\%^2 + 10\%^2}\right)F = 350\ \mu F \quad (27)$$

If the converter loop saturates, the minimum output capacitance is given by:

$$C_{OUT(min)(sat)} = \frac{1}{\Delta V_{OUT}}\left(\frac{L}{N_\Phi} \times \left(\Delta I_{OUT} + \frac{I_{L(PP)}}{2}\right)^2 \Big/ 2 \times V_{OUT} - \frac{\Delta I_{OUT} \times t_t}{2}\right)(1 + TOL_{IND}) \quad (28)$$

$$C_{OUT(min)(sat)} = \frac{1}{25.6 \times 10^{-3}} \left(\frac{\frac{56 \times 10^{-9}}{2} \times \left(24 + \frac{2.4}{2}\right)^2}{2 \times 0.8} - \frac{24 \times 1 \times 10^{-6}}{2} \right) (1 + 20\%)\ \text{F} = -41.5\ \mu\text{F} \quad (29)$$

In this case, choose $C_{OUT(min)}$ = 350µF, as the larger of the two values, for the output capacitance.

When calculating worst-case component values, use the value calculated above as the *minimum* output capacitance required. For ceramic capacitors, the *nominal* capacitance when considering tolerance, DC bias, temperature, and aging effects is typically two times the minimum capacitance. In this case the nominal capacitance is thus 700µF.

10.3.2.3 Selecting the Compensation Capacitor C_C

$$\text{BW} = \frac{\tau \times g_m \times R_Z}{2 \times \pi \times \frac{L}{N_\emptyset} \times C_{OUT,min} \times k_{COUT}} \quad (30)$$

$$\text{BW} = \frac{12.5 \times 10^{-6} \times 1.5 \times 10^{-3} \times 1.5 \times 10^{3}}{2 \times \pi \times \frac{56 \times 10^{-9}}{2} \times 350 \times 10^{-6} \times 2} = 230\ kHz \quad (31)$$

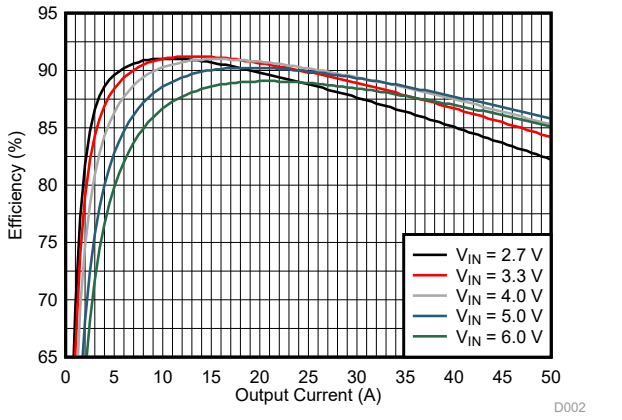
Next, calculate C_C:

$$C_C = \frac{k_{BW}}{2 \times \pi \times BW \times R_Z} \quad (32)$$

$$C_C = \frac{4}{2 \times \pi \times 230 \times 10^{3} \times 1.5 \times 10^{3}} = 1.85\ nF \quad (33)$$

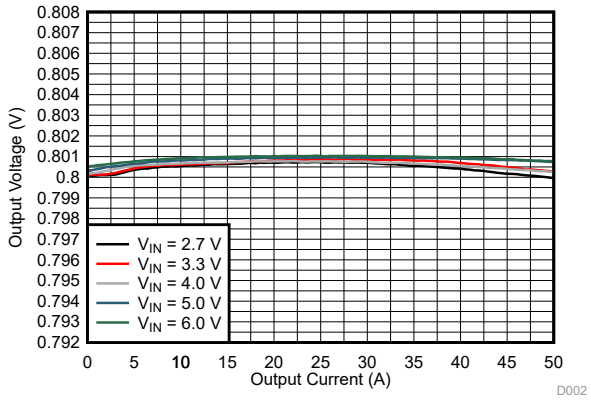
The closest standard value from the E12 series is 2.2nF.

10.3.3 Application Curves for Two Stacked Devices



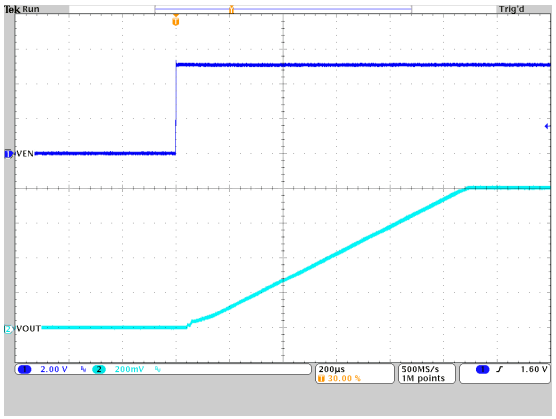
V_{OUT} = 0.8V PWM T_A = 25°C

図 10-21. Efficiency Versus Output Current



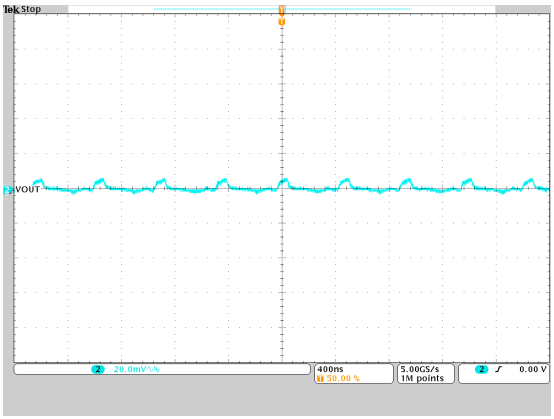
V_{OUT} = 0.8V PWM T_A = 25°C

図 10-22. Output Voltage Versus Output Current



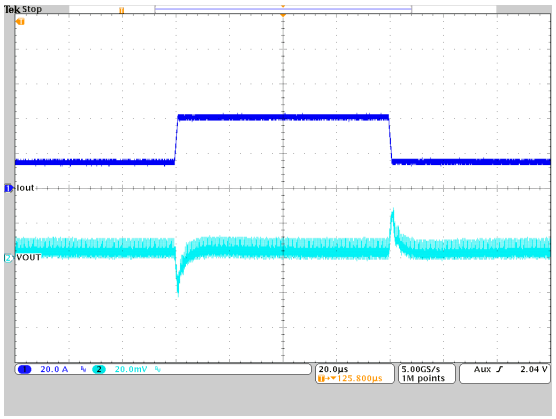
V_{OUT} = 0.8V PWM T_A = 25°C
V_{IN} = 5V R_{LOAD} = 20mΩ

図 10-23. Start-Up Timing



V_{OUT} = 0.8V PWM T_A = 25°C
V_{IN} = 5V R_{LOAD} = 20mΩ

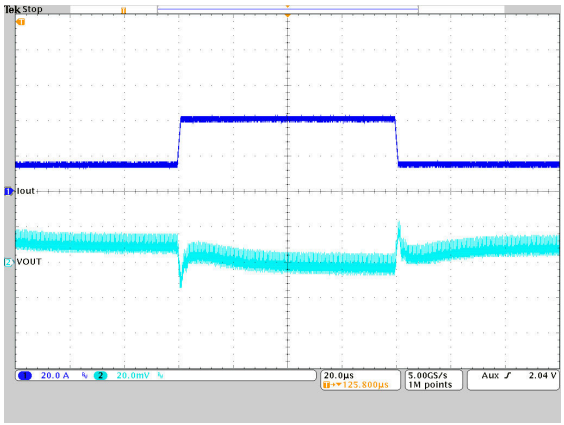
図 10-24. Output Voltage Ripple



V_{OUT} = 0.8V　　PWM; TPS62876 droop disabled　　T_A = 25°C

V_{IN} = 5V　　Iout = 15A to 40A to 15A

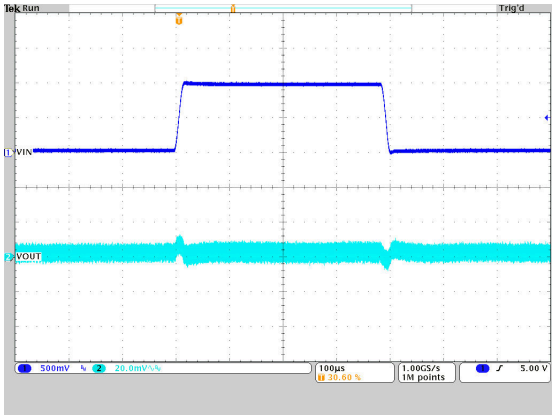
図 10-25. Load Transient Response



V_{OUT} = 0.8V　　PWM; TPS62876 droop enabled　　T_A = 25°C

V_{IN} = 5V　　Iout = 15A to 40A to 15A

図 10-26. Load Transient Response



V_{OUT} = 0.8V
V_{IN} = 4.5V to 5.5V to 4.5V

PWM

T_A = 25°C
I_{OUT} = 40A

図 10-27. Line Transient Response

10.4 Typical Application Using Three TPS62876-Q1 in a Stacked Configuration

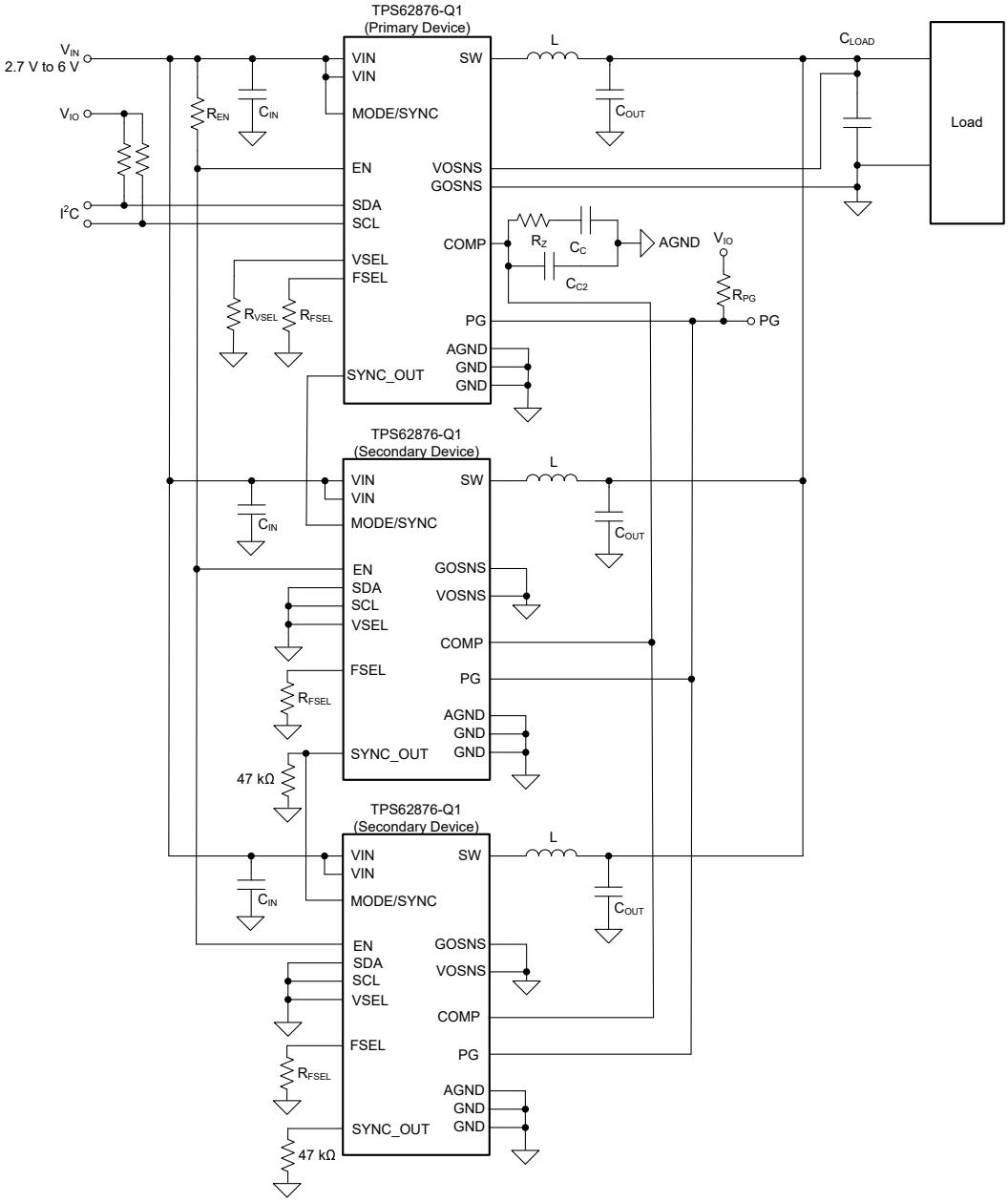


図 10-28. Stacking Three Devices

10.4.1 Design Requirements For Three Stacked Devices

表 10-6 lists the operating parameters for this application example.

表 10-6. Design Parameters

SYMBOL	PARAMETER	VALUE
V_{IN}	Input voltage	3.3V
V_{OUT}	Output voltage	0.875V
TOL_{VOUT}	Output voltage tolerance allowed by the application	±3%

表 10-6. Design Parameters (続き)

SYMBOL	PARAMETER	VALUE
TOL_{DC}	Output voltage tolerance of the TPS62876-Q1 (DC accuracy)	±0.8%
ΔI_{OUT}	Output current load step	±46A
t_r	Load step rise time	1µs
t_f	Load step fall time	1µs
f_{SW}	Switching frequency	2.25MHz
L	Inductance	56nH
g_m	Error amplifier transconductance	1.5mS
τ	Emulated current time constant	12.5µs
k_{BW}	Ratio of switching frequency to converter bandwidth (must be ≥ 4)	4
N_Φ	Number of phases (number of stacked devices)	3
k_{COUT}	Ratio of minimum to maximum output capacitance (typically 2)	2
R_{PG}	Pullup resistor on power good output	10kΩ
R_{EN}	Pullup resistor on enable	22kΩ
R_{SCL}, R_{SDA}	Pullup resistors on SDA and SCL	680Ω

Preliminary Calculations

With a total allowable output voltage tolerance of ±3% and a maximum DC error of ±0.8%, the allowable output voltage tolerance during a load step is given by:

$$\Delta V_{OUT} = \pm V_{OUT} \times (TOL_{VOUT} - TOL_{DC}) \tag{34}$$

$$\Delta V_{OUT} = \pm 0.875 \times (0.03 - 0.008) = \pm 19.25\ mV \tag{35}$$

10.4.2 Detailed Design Procedure

10.4.2.1 Selecting the Compensation Resistor

The calculation for a stack of two converters is similar to the single device expect that the parameter "number of phases" N_Φ is added to the equations. Use 式 36 to calculate the recommended value of compensation resistor R_Z:

$$R_Z = \frac{1}{g_m}\left(\frac{\pi \times \Delta I_{OUT} \times L}{4 \times \tau \times N_\phi \times \Delta V_{OUT}}\right)(1 + TOL_{IND}) \tag{36}$$

$$R_Z = \frac{1}{1.5 \times 10^{-3}}\left(\frac{\pi \times 46 \times 56 \times 10^{-9}}{4 \times 12.5 \times 10^{-6} \times 3 \times 19.25 \times 10^{-3}}\right)(1 + 0.2)\Omega = 2.24\ k\Omega \tag{37}$$

Rounding up, the closest standard value from the E24 series is 2.4kΩ.

10.4.2.2 Selecting the Output Capacitors

If the converter remains in regulation, the minimum output capacitance required is given by:

$$C_{OUT(min)(reg)} = \left(\frac{\tau \times g_m \times R_Z}{2 \times \pi \times \frac{L}{N_\phi} \times \frac{f_{SW}}{4}}\right)\left(1 + \sqrt{TOL_{IND}^2 + TOL_{fSW}^2}\right) \tag{38}$$

$$C_{OUT(min)(reg)} = \left(\frac{12.5 \times 10^{-6} \times 1.5 \times 10^{-3} \times 2.4 \times 10^{3}}{2 \times \pi \times \frac{56 \times 10^{-9}}{3} \times \frac{2.25 \times 10^{6}}{4}} \right) \left(1 + \sqrt{20\%^2 + 10\%^2}\right) F = 835\ \mu F \quad (39)$$

If the converter loop saturates, the minimum output capacitance is given by:

$$C_{OUT(min)(sat)} = \frac{1}{\Delta V_{OUT}} \left(\frac{\frac{L}{N_{\phi}} \times \left(\Delta I_{OUT} + \frac{I_{L(PP)}}{2} \right)^2}{2 \times V_{OUT}} - \frac{\Delta I_{OUT} \times t_t}{2} \right) (1 + TOL_{IND}) \quad (40)$$

$$C_{OUT(min)(sat)} = \frac{1}{19.25 \times 10^{-3}} \left(\frac{\frac{56 \times 10^{-9}}{3} \times \left(46 + \frac{2.4}{2}\right)^2}{2 \times 0.875} - \frac{46 \times 1 \times 10^{-6}}{2} \right) (1 + 20\%)\ F = 25.7\ \mu F \quad (41)$$

In this case, choose $C_{OUT(min)}$ = 835µF, as the larger of the two values, for the output capacitance.

When calculating worst-case component values, use the value calculated above as the *minimum* output capacitance required. For ceramic capacitors, the *nominal* capacitance when considering tolerance, DC bias, temperature, and aging effects is typically two times the minimum capacitance. In this case the nominal capacitance is thus 1670µF.

10.4.2.3 Selecting the Compensation Capacitor C_C

$$BW = \frac{\tau \times g_m \times R_Z}{2 \times \pi \times \frac{L}{N_{\emptyset}} \times C_{OUT,min} \times k_{COUT}} \quad (42)$$

$$BW = \frac{12.5 \times 10^{-6} \times 1.5 \times 10^{-3} \times 2.4 \times 10^{3}}{2 \times \pi \times \frac{56 \times 10^{-9}}{3} \times 835 \times 10^{-6} \times 2} = 230kHz \quad (43)$$

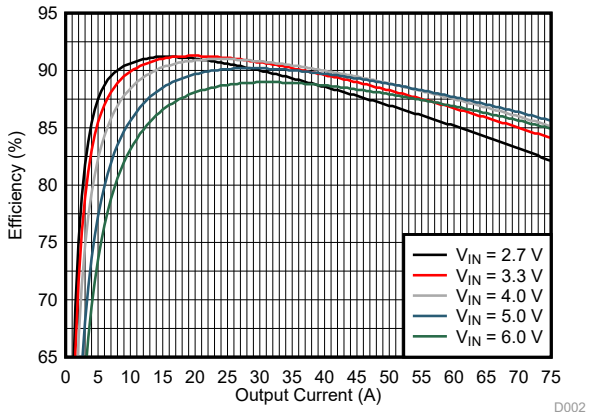
Next, calculate C_C:

$$C_C = \frac{k_{BW}}{2 \times \pi \times BW \times R_Z} \quad (44)$$

$$C_C = \frac{4}{2 \times \pi \times 230 \times 10^{3} \times 2.4 \times 10^{3}} = 1.15\ nF \quad (45)$$

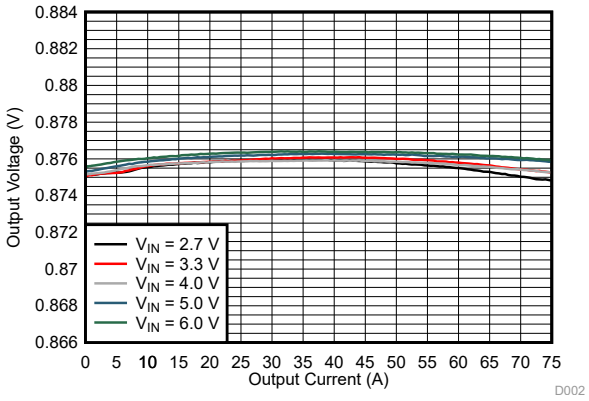
The closest standard value from the E12 series is 1.5nF.

10.4.3 Application Curves for Three Stacked Devices



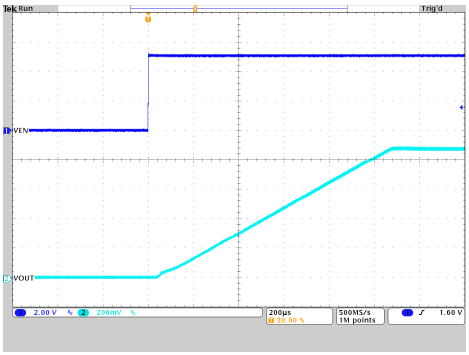
V_{OUT} = 0.875V PWM T_A = 25°C

図 10-29. Efficiency Versus Output Current



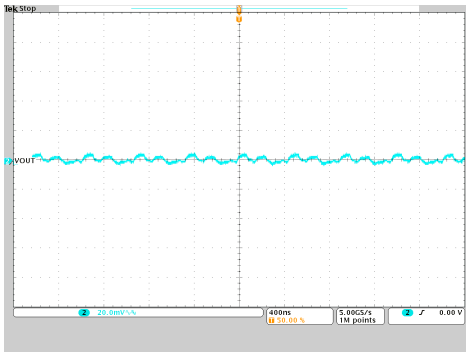
V_{OUT} = 0.875V PWM T_A = 25°C

図 10-30. Output Voltage Versus Output Current



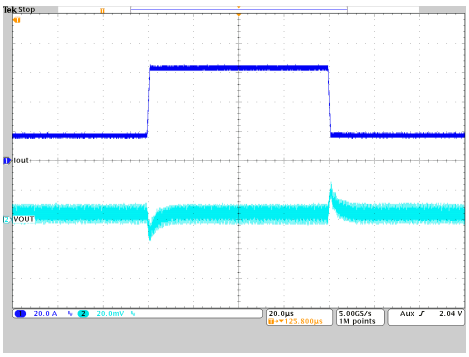
V_{OUT} = 0.875V PWM T_A = 25°C
V_{IN} = 5V R_{LOAD} = 14mΩ

図 10-31. Start-Up Timing



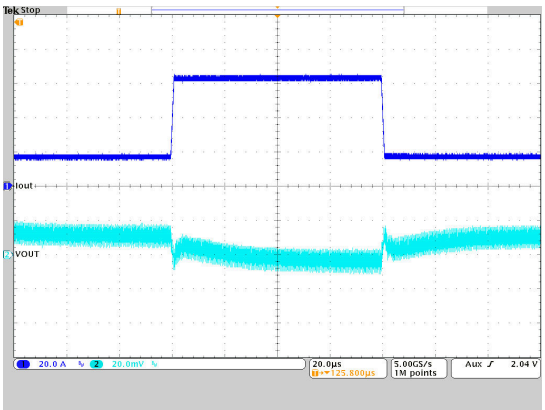
V_{OUT} = 0.875V PWM T_A = 25°C
V_{IN} = 5V R_{LOAD} = 14mΩ

図 10-32. Output Voltage Ripple



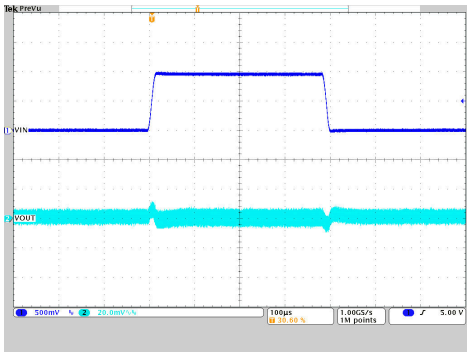
V_{OUT} = 0.875V PWM; TPS62876 droop disabled T_A = 25°C
V_{IN} = 5V Iout = 17A to 63A to 17A

図 10-33. Load Transient Response



V_{OUT} = 0.875V PWM; TPS62876 droop enabled T_A = 25°C
V_{IN} = 5V Iout = 17A to 63A to 17A

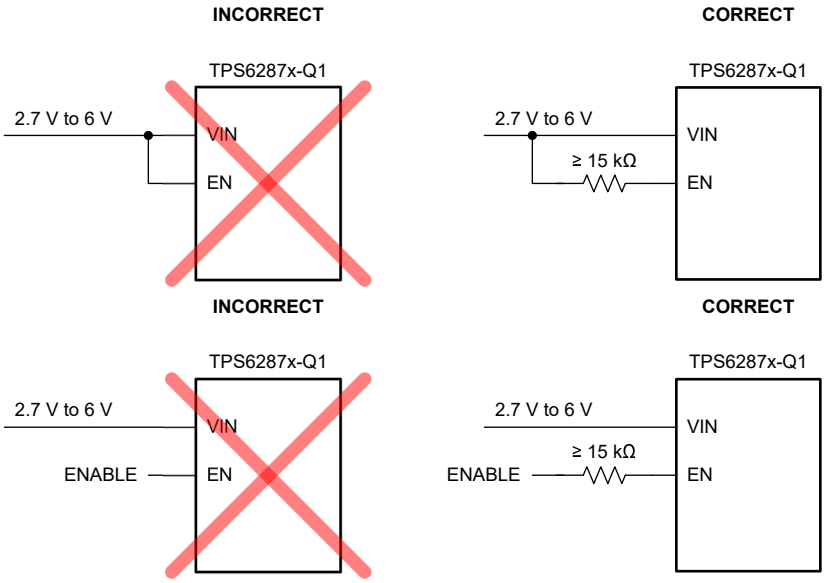
図 10-34. Load Transient Response



V_{OUT} = 0.875V
V_{IN} = 4.5V to 5.5V to 4.5V
PWM
T_A = 25°C
I_{OUT} = 63A

図 10-35. Line Transient Response

10.5 Best Design Practices



10.6 Power Supply Recommendations

The TPS6287x-Q1 device family has no special requirements for input power supply. The input power supply output current must be rated according to the supply voltage, output voltage, and output current of the TPS6287x-Q1.

10.7 Layout

Achieving the performance the TPS6287x-Q1 devices are capable of requires proper PDN and PCB design. TI therefore recommends the user perform a power integrity analysis on the design. There are a number of commercially available power integrity software tools, and the user can use these tools to model the effects on performance of the PCB layout and passive components.

In addition to the use of power integrity tools, TI recommends the following basic principles:

- Place the input capacitors close to the VIN and GND pins. Position the input capacitors in order of increasing size, starting with the smallest capacitors closest to the VIN and GND pins. Use an identical layout for both VIN-GND pin pairs of the package, to gain maximum benefit from the butterfly configuration.
- Place the inductor close to the device and keep the SW node small.

- Connect the exposed thermal pad and the GND pins of the device together. Use multiple thermal vias to connect the exposed thermal pad of the device to one or more ground planes (TI's EVM uses nine 150µm thermal vias).
- Use multiple power and ground planes.
- Route the VOSNS and GOSNS remote sense lines on the primary device as a differential pair and connect them to the lowest-impedance point of the PDN. If the desired connection point is not the lowest impedance point of the PDN, optimize the PDN until the desired connection point is the lowest impedance point of the PDN. Do not route the VOSNS and GOSNS close to any of the switch nodes.
- Connect the compensation components between COMP and AGND. Do not connect the compensation components directly to power ground.
- If possible, distribute the output capacitors evenly between the TPS6287x-Q1 device and the point-of-load, rather than placing them altogether in one place.
- Use multiple vias to connect each capacitor pad to the power and ground planes (TI's EVM typically uses four vias per pad).
- Use plenty of stitching vias to make sure of a low impedance connection between different power and ground planes.

10.7.1 Layout Guidelines

図 10-36 shows the top layer of one of the evaluation modules for this device. the figure demonstrates the practical implementation of the PCB layout principles previously listed. The user can find a complete set drawings of all the layers used in this PCB in the evaluation module user's guide *TPS62876 Buck Converter Evaluation Module* .

10.7.2 Layout Example

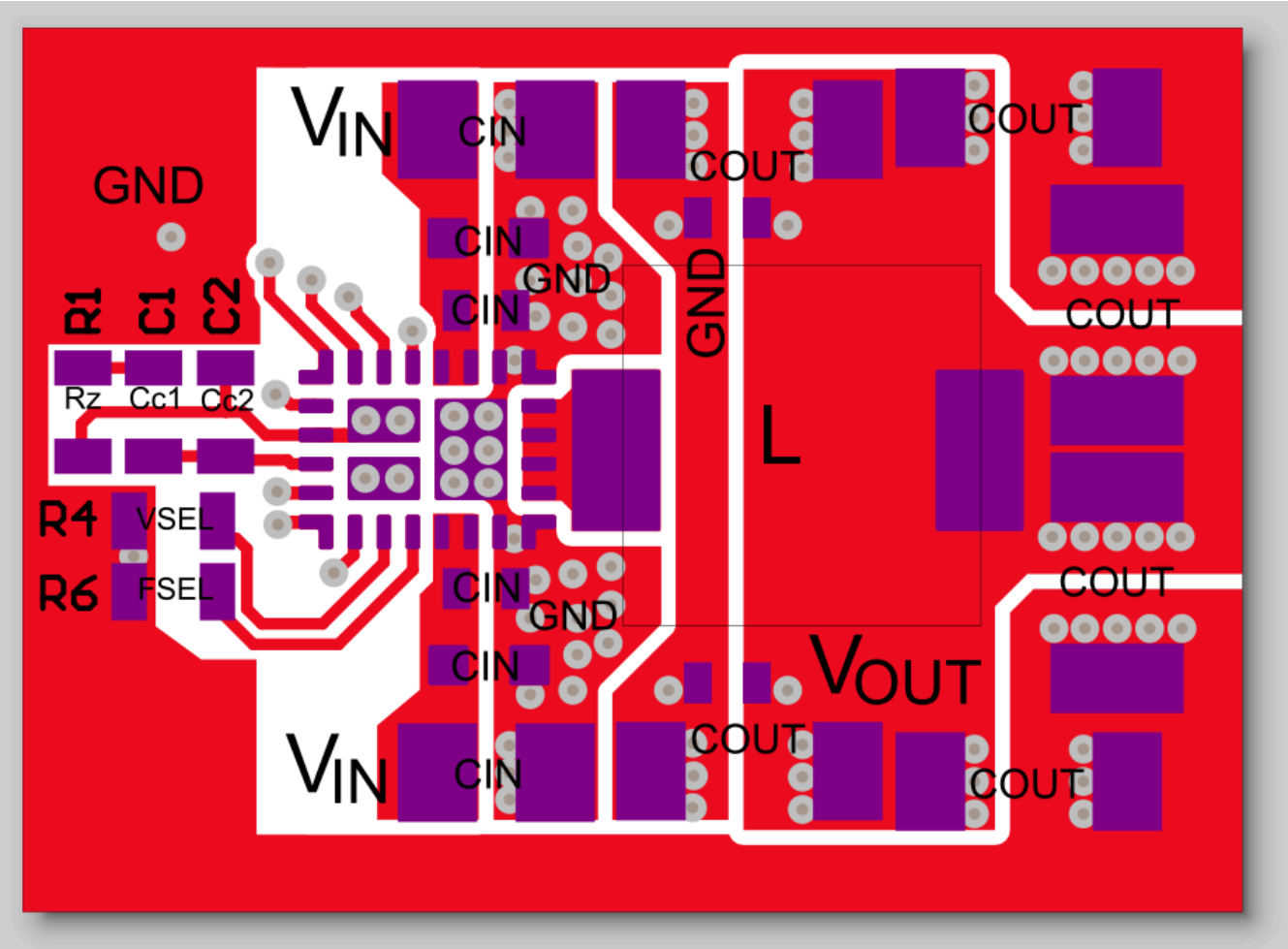


図 10-36. TPS62876-Q1 EVM Top Layer

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

Texas Instruments, *TPS62876 Buck Converter Evaluation Module*

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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11.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (October 2023) to Revision C (October 2024)	Page
• Added new device versions to the *Device Options* table	3

Changes from Revision A (July 2023) to Revision B (October 2023)	Page
• 「製品情報」表のプレビュー ラベルを削除	1
• Deleted preview labels in the *Device Options* table	3
• Deleted preview label for TPS62874-Q1	7
• Deleted preview label for TPS62875-Q1	7
• Deleted preview label for TPS62877-Q1	7

Changes from Revision * (April 2023) to Revision A (July 2023) **Page**

- ドキュメントのステータスを「事前情報」から「量産データ」に変更 1

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62874B1QWRZVRQ1	ACTIVE	WQFN-FCRLF	RZV	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6874B1Q	Samples
TPS62874B4QWRZVRQ1	ACTIVE	WQFN-FCRLF	RZV	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6874B4Q	Samples
TPS62874QWRZVRQ1	ACTIVE	WQFN-FCRLF	RZV	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	62874Q	Samples
TPS62875B1QWRZVRQ1	ACTIVE	WQFN-FCRLF	RZV	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6875B1Q	Samples
TPS62875B2QWRZVRQ1	ACTIVE	WQFN-FCRLF	RZV	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6875B2Q	Samples
TPS62875B3QWRZVRQ1	ACTIVE	WQFN-FCRLF	RZV	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6875B3Q	Samples
TPS62875B4QWRZVRQ1	ACTIVE	WQFN-FCRLF	RZV	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6875B4Q	Samples
TPS62875B5QWRZVRQ1	ACTIVE	WQFN-FCRLF	RZV	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6875B5Q	Samples
TPS62875QWRZVRQ1	ACTIVE	WQFN-FCRLF	RZV	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	62875Q	Samples
TPS62876B1QWRZVRQ1	ACTIVE	WQFN-FCRLF	RZV	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6876B1Q	Samples
TPS62876B3QWRZVRQ1	ACTIVE	WQFN-FCRLF	RZV	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6876B3Q	Samples
TPS62876QWRZVRQ1	ACTIVE	WQFN-FCRLF	RZV	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	62876Q	Samples
TPS62877B1QWRZVRQ1	ACTIVE	WQFN-FCRLF	RZV	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6877B1Q	Samples
TPS62877QWRZVRQ1	ACTIVE	WQFN-FCRLF	RZV	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	62877Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

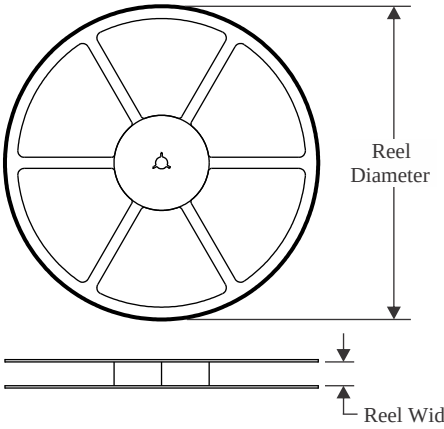
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

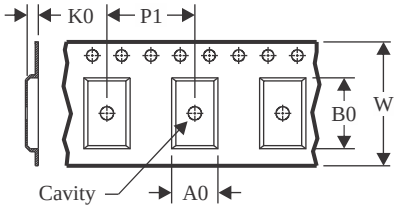
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

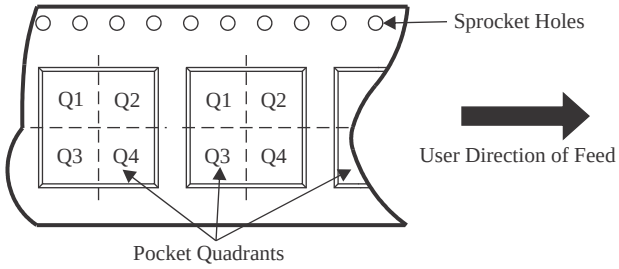


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

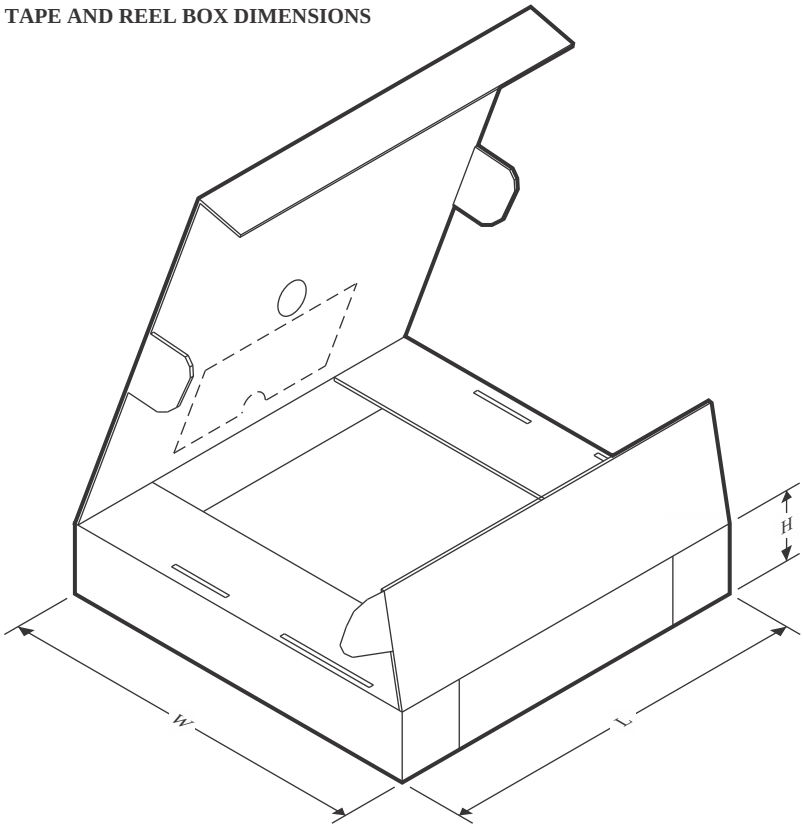


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62874B1QWRZVRQ1	WQFN-FCRLF	RZV	24	3000	330.0	12.4	3.3	4.4	0.8	8.0	12.0	Q1
TPS62874B4QWRZVRQ1	WQFN-FCRLF	RZV	24	3000	330.0	12.4	3.3	4.4	0.8	8.0	12.0	Q1
TPS62874QWRZVRQ1	WQFN-FCRLF	RZV	24	3000	330.0	12.4	3.3	4.4	0.8	8.0	12.0	Q1
TPS62875B1QWRZVRQ1	WQFN-FCRLF	RZV	24	3000	330.0	12.4	3.3	4.4	0.8	8.0	12.0	Q1
TPS62875B2QWRZVRQ1	WQFN-FCRLF	RZV	24	3000	330.0	12.4	3.3	4.4	0.8	8.0	12.0	Q1
TPS62875B4QWRZVRQ1	WQFN-FCRLF	RZV	24	3000	330.0	12.4	3.3	4.4	0.8	8.0	12.0	Q1
TPS62875B5QWRZVRQ1	WQFN-FCRLF	RZV	24	3000	330.0	12.4	3.3	4.4	0.8	8.0	12.0	Q1
TPS62875QWRZVRQ1	WQFN-FCRLF	RZV	24	3000	330.0	12.4	3.3	4.4	0.8	8.0	12.0	Q1
TPS62876B1QWRZVRQ1	WQFN-FCRLF	RZV	24	3000	330.0	12.4	3.3	4.4	0.8	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62876QWRZVRQ1	WQFN-FCRLF	RZV	24	3000	330.0	12.4	3.3	4.4	0.8	8.0	12.0	Q1
TPS62877B1QWRZVRQ1	WQFN-FCRLF	RZV	24	3000	330.0	12.4	3.3	4.4	0.8	8.0	12.0	Q1
TPS62877QWRZVRQ1	WQFN-FCRLF	RZV	24	3000	330.0	12.4	3.3	4.4	0.8	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

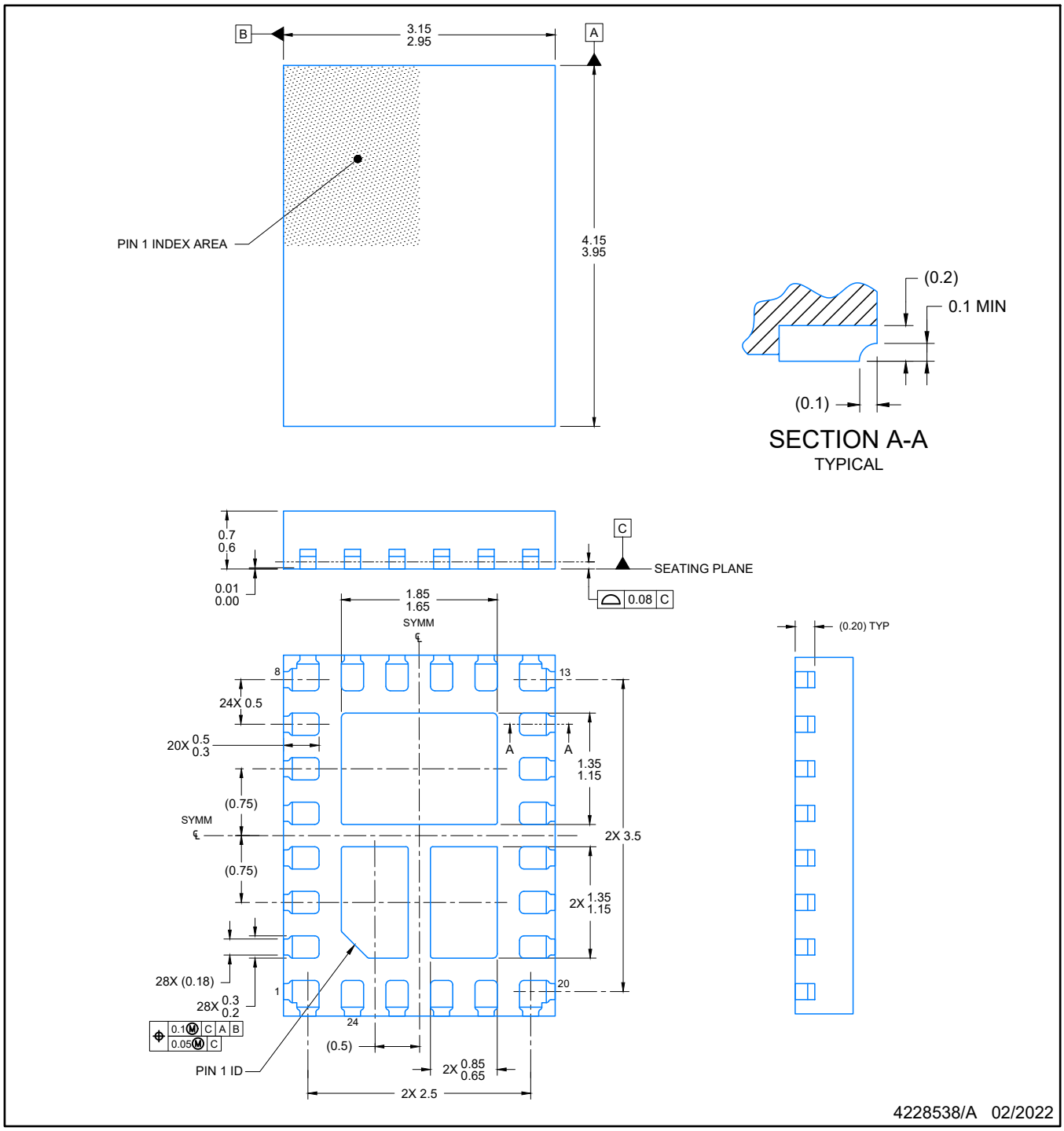
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62874B1QWRZVRQ1	WQFN-FCRLF	RZV	24	3000	338.0	355.0	50.0
TPS62874B4QWRZVRQ1	WQFN-FCRLF	RZV	24	3000	338.0	355.0	50.0
TPS62874QWRZVRQ1	WQFN-FCRLF	RZV	24	3000	338.0	355.0	50.0
TPS62875B1QWRZVRQ1	WQFN-FCRLF	RZV	24	3000	338.0	355.0	50.0
TPS62875B2QWRZVRQ1	WQFN-FCRLF	RZV	24	3000	338.0	355.0	50.0
TPS62875B4QWRZVRQ1	WQFN-FCRLF	RZV	24	3000	338.0	355.0	50.0
TPS62875B5QWRZVRQ1	WQFN-FCRLF	RZV	24	3000	338.0	355.0	50.0
TPS62875QWRZVRQ1	WQFN-FCRLF	RZV	24	3000	338.0	355.0	50.0
TPS62876B1QWRZVRQ1	WQFN-FCRLF	RZV	24	3000	338.0	355.0	50.0
TPS62876QWRZVRQ1	WQFN-FCRLF	RZV	24	3000	338.0	355.0	50.0
TPS62877B1QWRZVRQ1	WQFN-FCRLF	RZV	24	3000	338.0	355.0	50.0
TPS62877QWRZVRQ1	WQFN-FCRLF	RZV	24	3000	338.0	355.0	50.0

PACKAGE OUTLINE

RZV0024A

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



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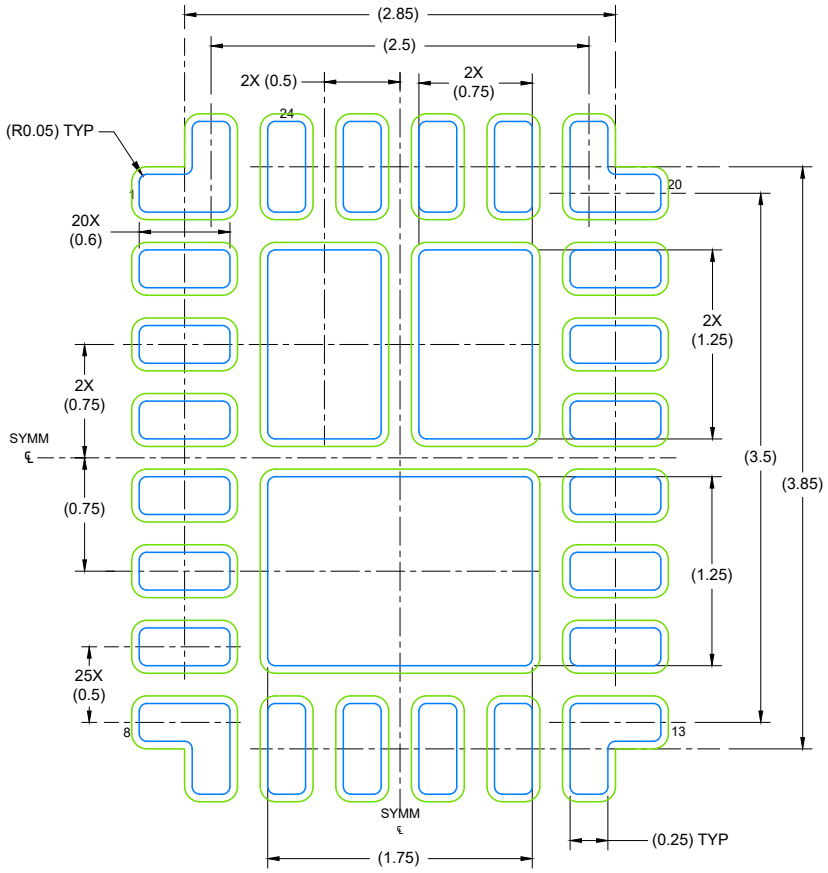
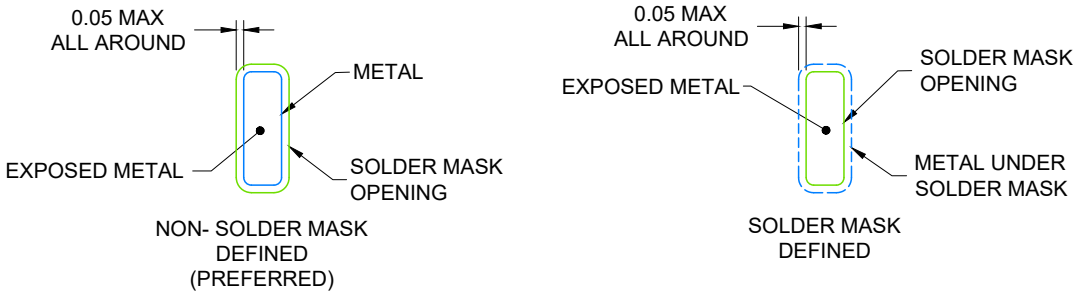
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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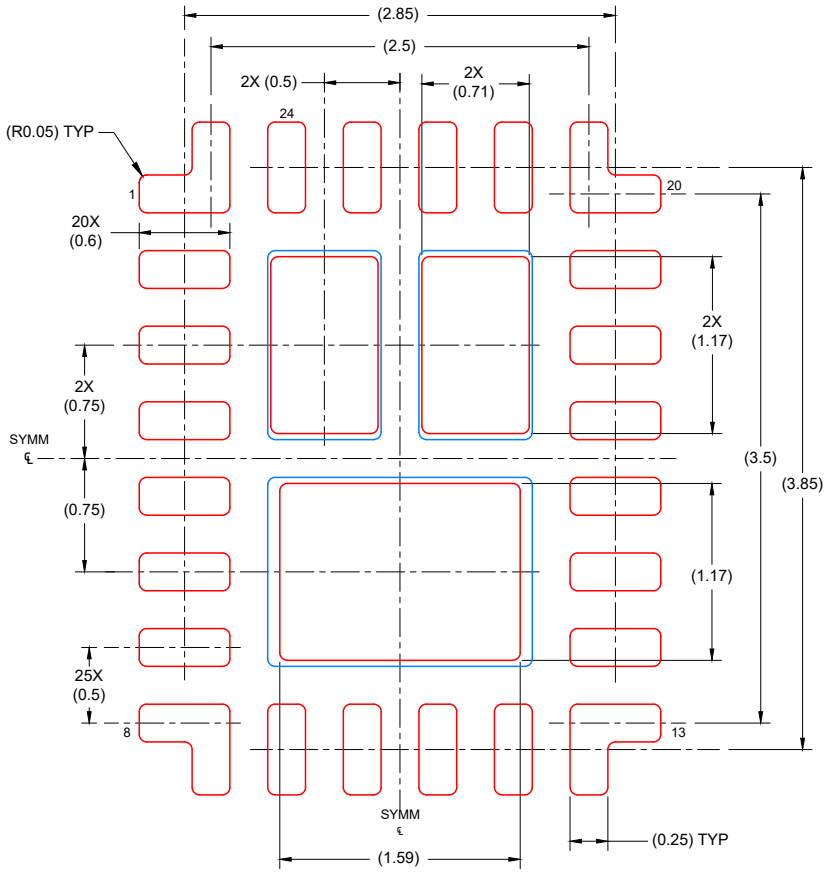
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

SCALE: 15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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