TEXAS INSTRUMENTS
TPS62912, TPS62913
JAJSJL4B – AUGUST 2020 – REVISED MARCH 2021

TPS6291x 3V～17V、2A/3A、低ノイズ、低リップル、降圧コンバータ、フェライト・ビーズ・フィルタ補償機能内蔵

1 特長

- 低い出力 1/f ノイズ：20μV_{RMS} 未満 (100Hz～100kHz)
- 低い出力電圧リップル：10μV_{RMS} 未満 (フェライト・ビーズの後)
- 優れた PSRR：65dB 超 (最大 100kHz)
- 2.2MHz または 1MHz の固定周波数ピーク電流モード制御
- 外部クロックと同期可能 (オプション)
- 2 段目 L-C フィルタとしてフェライト・ビーズ (オプション) を使用できる内蔵ループ補償機能 (30dB 減衰)
- スペクトラム拡散変調 (オプション)
- 入力電圧範囲：3.0V～17V
- 出力電圧範囲：0.8V～5.5V
- R_{DSon}：57mΩ/20mΩ
- ±1% の出力電圧精度
- 高精度のイネーブル入力により以下を実現
  - ユーザー定義の低電圧誤動作防止機能
  - 正確なシーケンシング
- 調整可能なソフト・スタート
- パワー・グッド出力
- 出力放電 (オプション)
- -40℃～150℃の接合部温度範囲
- 2.0mm x 2.0mm QFN (0.5mm ピッチ)
- WEBENCH® Power Designer により、TPS6291x を使用するカスタム設計を作成

2 アプリケーション

- 通信インフラ
- 試験および測定機器
- 航空宇宙および防衛 (レーダー / 航空電子機器)
- 医療用

3 概要

TPS6291x デバイスは、高効率、低ノイズ、低リップルの電流モード同期整流降圧コンバータのファミリです。これらのデバイスは、通常はポスト・レギュレーションに LDO を使用するような、ノイズの影響を受けやすいアプリケーション (たとえば、高速 ADC、クロックおよびジッタ・クリーナ、シリアライザ、デシリアライザ、レーダー) に理想的です。

本デバイスは、2.2MHz または 1MHz の固定スイッチング周波数で動作し、外部クロックにも同期できます。

出力電圧リップルをさらに低減するため、本デバイスは、オプションの 2 段目フェライト・ビーズ L-C フィルタを使用して動作するループ補償機能を内蔵しています。これにより、10μV_{RMS} 未満の出力電圧リップルを達成できます。

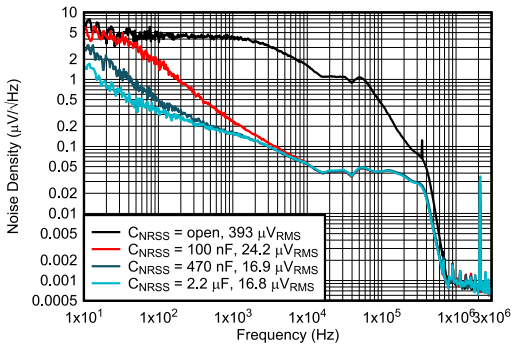
NR/SS ピンに接続されたコンデンサで内部基準電圧をフィルタ処理することで、低ノイズ LDO と同様の、低い周波数ノイズ・レベルを達成しています。

オプションのスペクトラム拡散変調方式を使用すると、DC/DC スイッチング周波数をより広い範囲にわたって拡散できるため、ミキシング・スプリアスを低減できます。

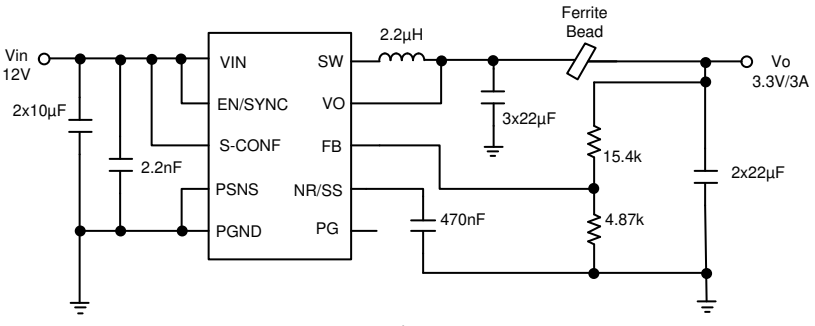
製品情報

型番	出力電流	パッケージ(1)	本体サイズ (公称)
TPS62912	2A	QFN (10)	2.0mm × 2.0mm
TPS62913	3A		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



出力ノイズと周波数との関係



代表的なアプリケーション

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4 Revision History

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• デバイス・ステータスを「事前情報」から「量産データ」に変更	1

5 Pin Configuration and Functions

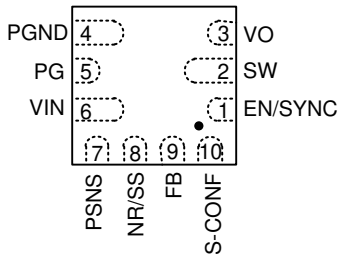


図 5-1. 10-Pin QFN RPU Package (Top View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	EN/SYNC	I	Enable/Disable pin including threshold-comparator. Connect to logic low to disable the device. Pull high to enable the device. This pin has an internal pulldown resistor of typically 500 kΩ when the device is disabled. Apply a clock to this pin to synchronize the device.
2	SW	I/O	Switch pin of the power stage
3	VO	I	Output voltage sense pin. This pin needs to be connected directly after the first inductor.
4	PGND		Power ground connection
5	PG	O	Open-drain power-good output. This pin is pulled to GND when V_{OUT} is below the power-good threshold. It requires a pullup resistor to output a logic high. It can be left open or tied to GND if not used.
6	VIN	I	Power supply input voltage pin
7	PSNS	I	Power sense ground. Connect directly to the ground plane.
8	NR/SS	O	A capacitor connected to this pin sets the soft-start time and low frequency noise level of the device.
9	FB	I	Feedback pin of the device
10	S-CONF	O	Smart Configuration pin. This pin configures the operation modes of the device. See 表 7-1.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	VIN, EN/SYNC, PG, S-CONF	– 0.3	18	V
	SW (DC)	– 0.3	V_{IN} + 0.3	V
	SW (AC, less than 10ns)(3)	– 2.5	21	V
	VO, FB, NR/SS	– 0.3	6	V
	PSNS	– 0.3	0.3	V
Sink Current	PG		10	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal
(3) While switching

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	3.0		17	V
V_{OUT}	Output voltage	0.8		5.5	V
C_{IN}	Effective input capacitance	5	10		µF
L_1	Effective output inductance	-30%	2.2 / 4.7	20%	µH
C_{OUT}	Effective output capacitance	40	47	80	µF
L_f	Effective filter inductance	0	10	50	nH
C_f	Effective filter capacitance	20	40	160	µF
C_{OUT} + C_f	Effective total output capacitance, including first and second L-C filter	40		200	µF
I_{OUT}	Output current for TPS62913	0		3	A
I_{OUT}	Output current for TPS62912	0		2	A
T_J (1)	Junction temperature	–40		150	°C

(1) Operating lifetime is derated at junction temperatures above 125°C.

6.4 Thermal Information

THERMAL METRIC[1]		TPS6291x		UNIT
		RPU 10-pin QFN		
		JEDEC 51-7 PCB	TPS6291xEVM-077	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87.7	56.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.9	n/a [2]	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.2	n/a [2]	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.9	1.3	°C/W
Y_{JB}	Junction-to-board characterization parameter	22.2	22.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Not applicable to an EVM

6.5 Electrical Characteristics

Over recommended input voltage range, T_J= -40℃ to 150℃. Typical values are at Vin=12V andT_J=25℃ (unless otherwise noted)

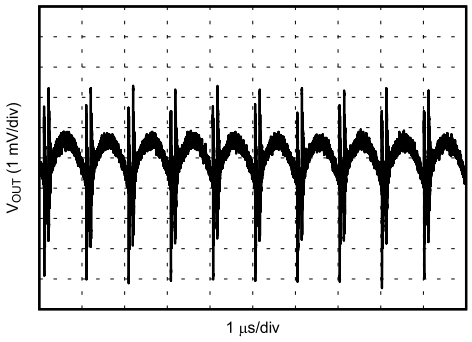
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current	EN = High, no load, device switching, fsw = 1 MHz		5		mA
I_{SD}	Shutdown current	EN = GND, T_J = -40°C to 125°C		0.3	70	µA
V_{UVLO}	Undervoltage lockout	V_{IN} rising, T_J = -40°C to 125°C	2.85	2.92	3.0	V
V_{UVLO}	Undervoltage lockout	V_{IN} rising			3.04	V
V_{HYS}	Undervoltage lockout hysteresis			200		mV
T_{JSD}	Thermal shutdown threshold	T_J rising		170		°C
	Thermal shutdown hysteresis	T_J falling		20		°C
CONTROL and INTERFACE						
V_{H_EN}	High-level input-threshold voltage at EN/SYNC		0.97	1.01	1.04	V
V_{L_EN}	Low-level input-threshold voltage at EN/SYNC		0.87	0.9	0.93	V
V_{H_SYNC}	High-level input-threshold clock signal on EN/SYNC	EN/SYNC = clock	1.1			V
V_{L_SYNC}	Low-level input-threshold clock signal on EN/SYNC	EN/SYNC = clock			0.4	V
$I_{EN,LKG}$	Input leakage current into EN/SYNC	EN/SYNC = GND or VIN, –40°C ≤ T_J ≤ 125°C		5	160	nA
R_{PD}	Pulldown resistor on EN/SYNC	EN/SYNC = Low	330	500		kΩ
t_{delay}	Enable delay time	Time from EN/SYNC high to device starts switching, R_{S-CONF} = 80.6 kΩ		1		ms
$I_{NR/SS}$	NR/SS source current		67.5	75	82.5	µA
R_{S-CONF}	S-CONF resistor step range accuracy	R_{S-CONF} tolerance for all settings according to S-CONF Table	–4%		+4%	
V_{PG}	Power good threshold	V_{FB} rising, referenced to V_{FB} nominal	93%	95%	98%	
V_{PG}	Power good threshold	V_{FB} falling, referenced to V_{FB} nominal	88%	90%	93%	
$V_{PG,OL}$	Low-level output voltage at PG pin	I_{SINK} = 1 mA			0.4	V
$I_{PG,LKG}$	Input leakage current into PG pin	V_{PG} = 5 V; –40°C ≤ T_J ≤ 125°C		5	500	nA
$t_{PG,DLY}$	Power good delay time	V_{FB} falling		8		µs
OUTPUT						
t_{on}	Minimum on-time	V_{IN} ≥ 5 V, I_{out} = 1 A		35	70	ns

Over recommended input voltage range, T_J= -40°C to 150°C. Typical values are at Vin=12V andT_J=25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{off}	Minimum off-time	V_{IN} ≥ 5 V, I_{out} = 1 A		50	60	ns
V_{FB}	Feedback regulation accuracy	–40°C ≤T_J ≤ 150°C	0.792	0.8	0.812	V
V_{FB}	Feedback regulation accuracy	–40°C ≤ T_J ≤ 125°C	0.792	0.8	0.808	V
$I_{FB,LKG}$	Input leakage current into FB	V_{FB} = 0.8 V, –40°C ≤ T_J ≤ 125°C		1	70	nA
$I_{VO,LKG}$	Input leakage current into VO	V_{VO} = 1.2 V, –40°C ≤ T_J ≤ 125°C		0.01	30	µA
PSRR	Power supply rejection ratio	V_{IN} = 12 V, 1.2 V_{OUT}, 1 A, $C_{NR/SS}$ = 470 nF, f_{sw} = 1 MHz, C_{FF} = open, L_1 = 2.2 µH, C_{OUT} = 3 × 22 µF, f ≤ 100 kHz		65		dB
PSRR	Power supply rejection ratio	V_{IN} = 5 V, 1.2 V_{OUT}, 1 A, $C_{NR/SS}$ = 470 nF, f_{sw} = 2.2 MHz, C_{FF} = open, L_1 = 2.2 µH, C_{OUT} = 3 × 22 µF, f ≤ 100 kHz		70		dB
V_{NRMS}	Output voltage RMS noise	V_{IN} = 12 V, BW = 100 Hz to 100 kHz, $C_{NR/SS}$ = 470 nF, f_{SW} = 1 MHz, V_{OUT} = 1.2 V, C_{FF} = open, L_1 = 2.2 µH, C_{OUT} = 3 × 22 µF		24.4		$µV_{RMS}$
V_{NRMS}	Output voltage RMS noise	V_{IN} = 5 V, BW = 100 Hz to 100 kHz, $C_{NR/SS}$ = 470 nF, f_{SW} = 2.2 Hz, V_{OUT} = 1.2 V, C_{FF} = open, L_1 = 2.2 µH, C_{OUT} = 3 × 22 µF		13.5		$µV_{RMS}$
V_{opp}	Output ripple voltage at f_{SW}	V_{IN} = 12 V, f_{SW} = 1 MHz, V_{OUT} = 1.2 V, L_1 = 4.7 µH, C_{OUT} = 3 × 22 µF, L_f = 10 nH, C_f = 2 × 22 µF		9		$µV_{RMS}$
V_{opp}	Output ripple voltage at f_{SW}	V_{IN} = 5 V, f_{SW} = 2.2 MHz, V_{OUT} = 1.2 V, L_1 = 2.2 µH, C_{OUT} = 3 × 22 µF, L_f = 10 nH, C_f = 2 × 22 µF		< 2.2		$µV_{RMS}$
R_{DIS}	Output discharge resistance	EN/SYNC = GND, V_{OUT} = 1.2 V, V_{IN} ≥ 5 V. See Typical Char for plot.		7		Ω
R_{DIS}	Output discharge resistance	EN/SYNC = GND, V_{OUT} = 5 V, V_{IN} ≥ 5 V. See Typical Char for plot.		32		Ω
f_{SW}	Switching frequency	2.2-MHz setting	1.98	2.2	2.42	MHz
f_{SW}	Synchronization range	2.2-MHz setting	1.9	2.2	2.42	MHz
f_{SW}	Switching frequency	1-MHz setting	0.9	1	1.18	MHz
f_{SW}	Synchronization range	1-MHz setting	0.86	1	1.2	MHz
D_{SYNC}	Synchronization duty cycle		45%		55%	
t_{sync_elay}	Synchronization phase delay	Phase delay from EN/SYNC rising edge to SW rising edge		90		ns
I_{SWpeak}	Peak switch current limit	TPS62912	2.9	3.5	4.0	A
I_{SWpeak}	Peak switch current limit	TPS62913	3.7	4.3	5.1	A
$I_{SWvalley}$	Valley switch current limit	TPS62912		3.4		A
$I_{SWvalley}$	Valley switch current limit	TPS62913		4.2		A
$Ineg_{valley}$	Negative valley current limit			–1.39	–0.96	A
$R_{DS(ON)}$	High-side FET on-resistance	V_{IN} ≥ 5 V		57	95	mΩ
	Low-side FET on-resistance	V_{IN} ≥ 5 V		20	39	mΩ

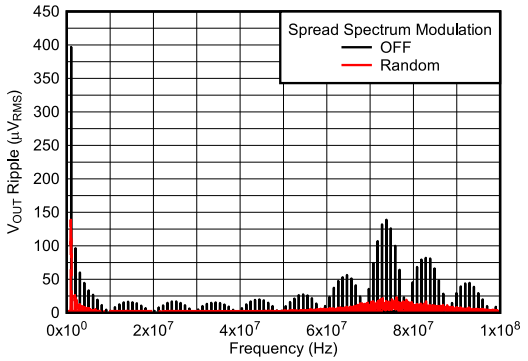
6.6 Typical Characteristics

V_{IN} = 12 V, V_{OUT} = 1.2 V, T_A = 25°C, BOM = 表 8-1, (unless otherwise noted)



12 V to 1.2 V, 1 A　2.2 µH, 1 MHz　First L-C Only

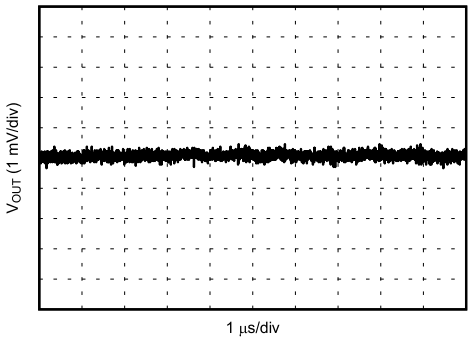
図 6-1. V_{OUT} Ripple After the First L-C Filter



BW = 10 kHz

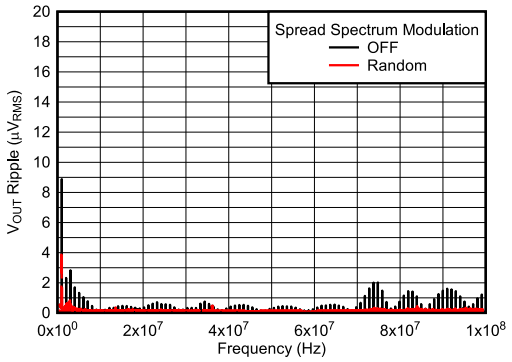
12 V to 1.2 V, 1 A　2.2 µH, 1 MHz　First L-C Only

図 6-2. V_{OUT} Ripple FFT After the First L-C Filter



12 V to 1.2 V, 1 A　2.2 µH, 1 MHz　First and second L-C

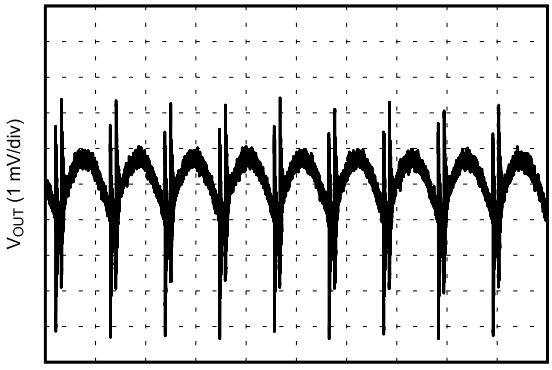
図 6-3. V_{OUT} Ripple After the Second L-C Filter



BW = 10 kHz

12 V to 1.2 V, 1 A　2.2 µH, 1 MHz　First and second L-C

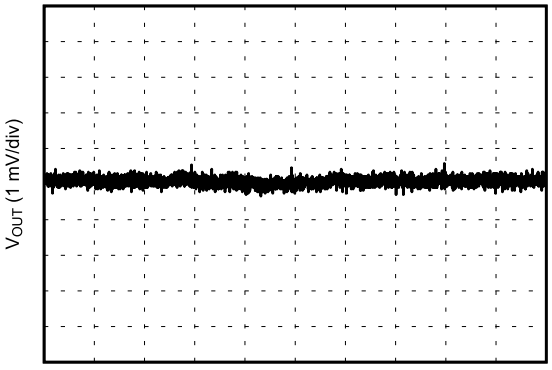
図 6-4. V_{OUT} Ripple FFT After the Second L-C Filter



12 V to 1.2 V, 1 A　2.2 µH, 1 MHz　First L-C Only

With Random Spread Spectrum Enabled

図 6-5. V_{OUT} Ripple After the First L-C Filter

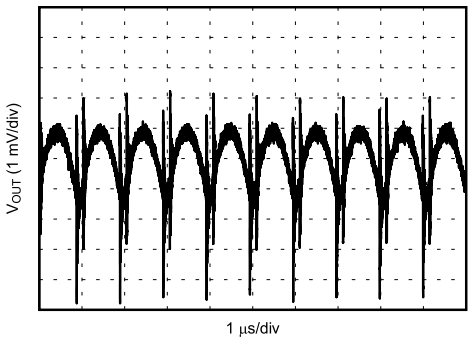


12 V to 1.2 V, 1 A　2.2 µH, 1 MHz　First and second L-C

With Random Spread Spectrum Enabled

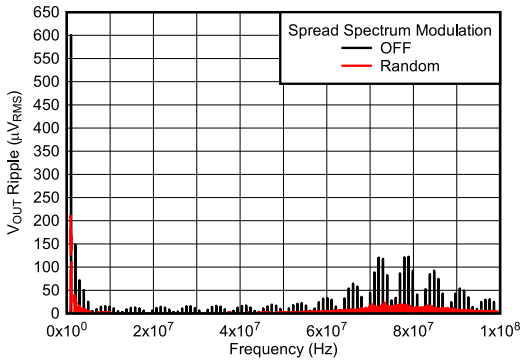
図 6-6. V_{OUT} Ripple After the Second L-C Filter

6.6 Typical Characteristics (continued)



12 V to 1.8 V, 1 A 2.2 µH, 1 MHz First L-C Only

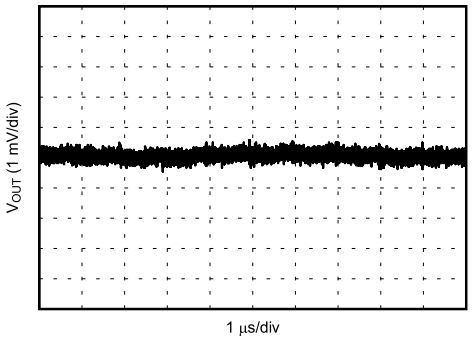
図 6-7. V_{OUT} Ripple After the First L-C Filter



BW = 10 kHz

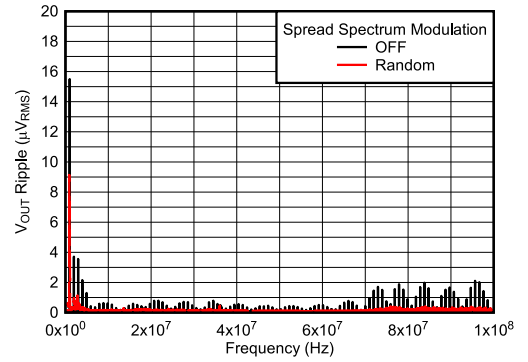
12 V to 1.8 V, 1 A 2.2 µH, 1 MHz First L-C Only

図 6-8. V_{OUT} Ripple FFT After the First L-C Filter



12 V to 1.8 V, 1 A 2.2 µH, 1 MHz First and second L-C

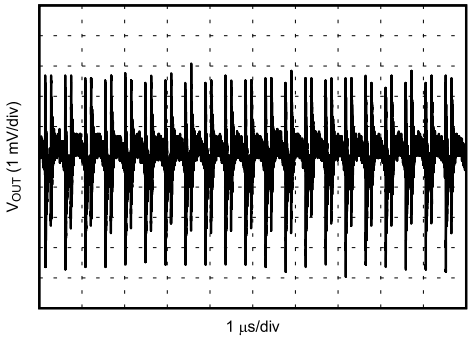
図 6-9. V_{OUT} Ripple After the Second L-C Filter



BW = 10 kHz

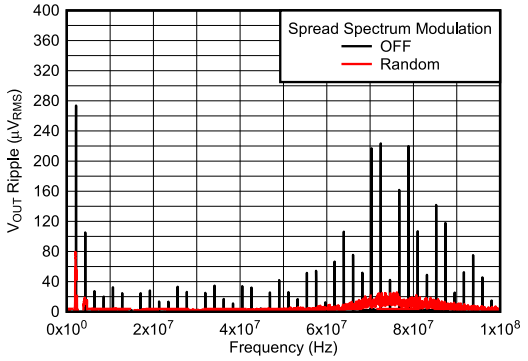
12 V to 1.8 V, 1 A 2.2 µH, 1 MHz First and second L-C

図 6-10. V_{OUT} Ripple FFT After the Second L-C Filter



12 V to 3.3 V, 1 A 2.2 µH, 2.2 MHz First L-C Only

図 6-11. V_{OUT} Ripple After the First L-C Filter

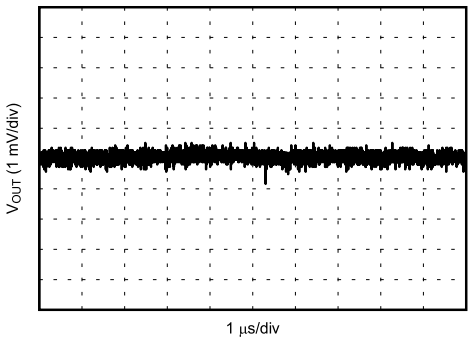


BW = 10 kHz

12 V to 3.3 V, 1 A 2.2 µH, 2.2 MHz First L-C Only

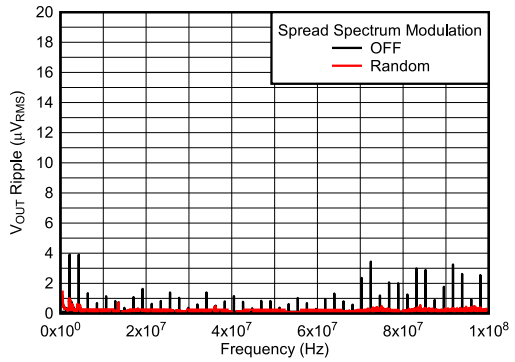
図 6-12. V_{OUT} Ripple FFT After the First L-C Filter

6.6 Typical Characteristics (continued)



12 V to 3.3 V, 1 A　2.2 µH, 2.2 MHz　First and second L-C

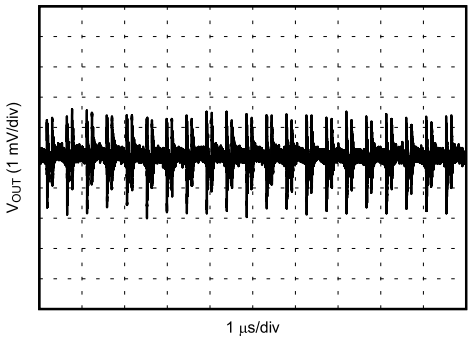
図 6-13. V_{OUT} Ripple After the Second L-C Filter



BW = 10 kHz

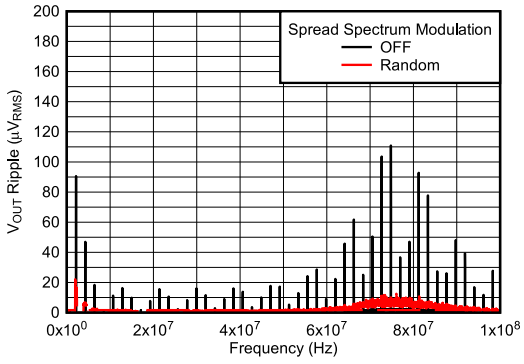
12 V to 3.3 V, 1 A　2.2 µH, 2.2 MHz　First and second L-C

図 6-14. V_{OUT} Ripple FFT After the Second L-C Filter



5 V to 1.2 V, 1 A　2.2 µH, 2.2 MHz　First L-C Only

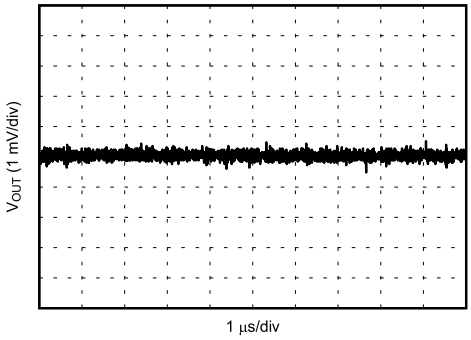
図 6-15. V_{OUT} Ripple After the First L-C Filter



BW = 10 kHz

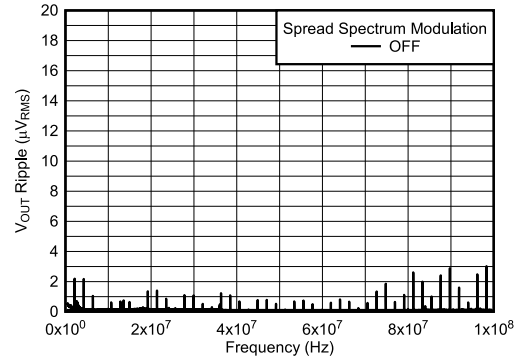
5 V to 1.2 V, 1 A　2.2 µH, 2.2 MHz　First L-C Only

図 6-16. V_{OUT} Ripple FFT After the First L-C Filter



5 V to 1.2 V, 1 A　2.2 µH, 2.2 MHz　First and second L-C

図 6-17. V_{OUT} Ripple after the Second L-C Filter

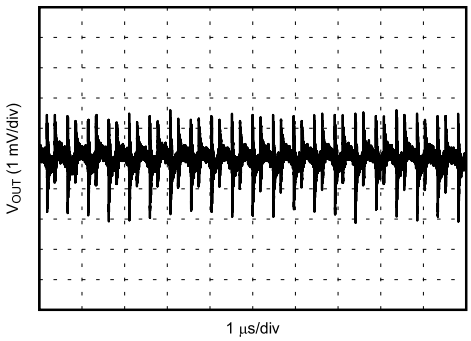


BW = 10 kHz

5 V to 1.2 V, 1 A　2.2 µH, 2.2 MHz　First and second L-C

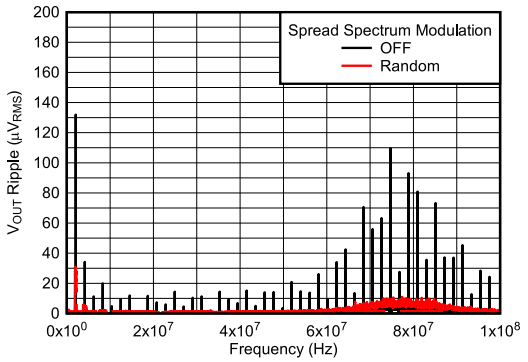
図 6-18. V_{OUT} Ripple FFT After the Second L-C Filter

6.6 Typical Characteristics (continued)



5 V to 1.8 V, 1 A 2.2 µH, 2.2 MHz First L-C Only

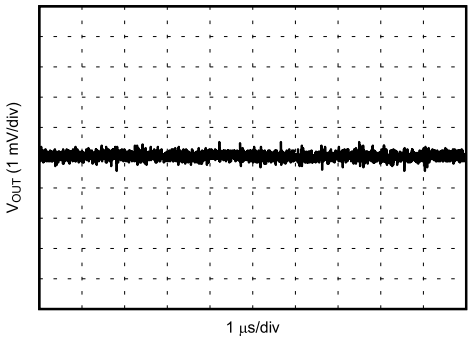
図 6-19. V_{OUT} Ripple After the First L-C Filter



BW = 10 kHz

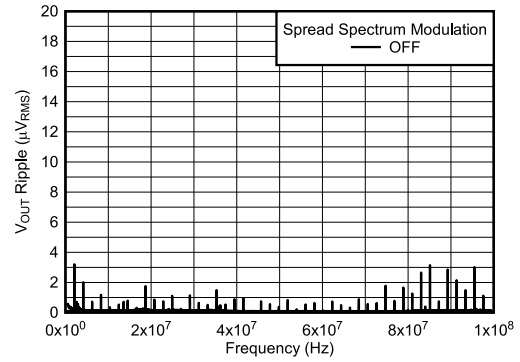
5 V to 1.8 V, 1 A 2.2 µH, 2.2 MHz First L-C Only

図 6-20. V_{OUT} Ripple FFT After the First L-C Filter



5 V to 1.8 V, 1 A 2.2 µH, 2.2 MHz First and second L-C

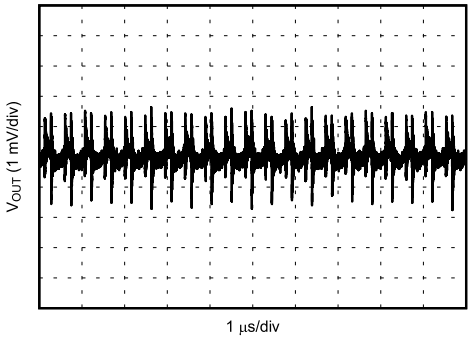
図 6-21. V_{OUT} Ripple After the Second L-C Filter



BW = 10 kHz

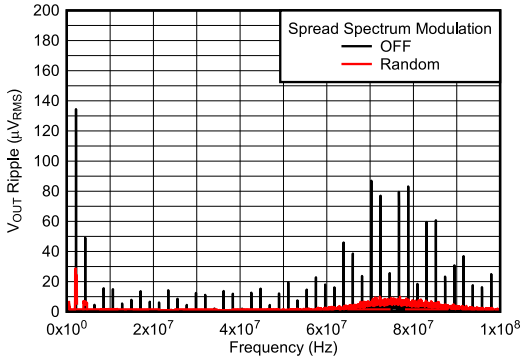
5 V to 1.8 V, 1 A 2.2 µH, 2.2 MHz First and second L-C

図 6-22. V_{OUT} Ripple FFT After the Second L-C Filter



5 V to 3.3 V, 1 A 2.2 µH, 2.2 MHz First L-C Only

図 6-23. V_{OUT} Ripple After the First L-C Filter

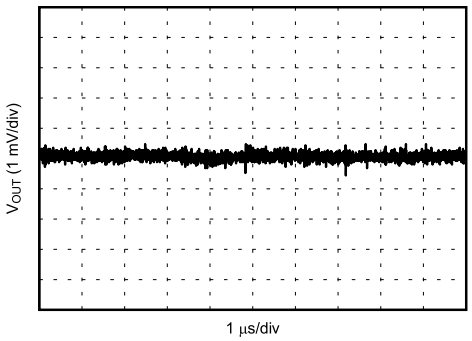


BW = 10 kHz

5 V to 3.3 V, 1 A 2.2 µH, 2.2 MHz First L-C Only

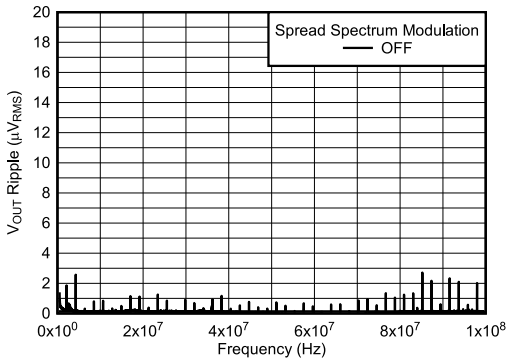
図 6-24. V_{OUT} Ripple FFT After the First L-C Filter

6.6 Typical Characteristics (continued)



5 V to 3.3 V, 1 A　　2.2 µH, 2.2 MHz　　First and second L-C

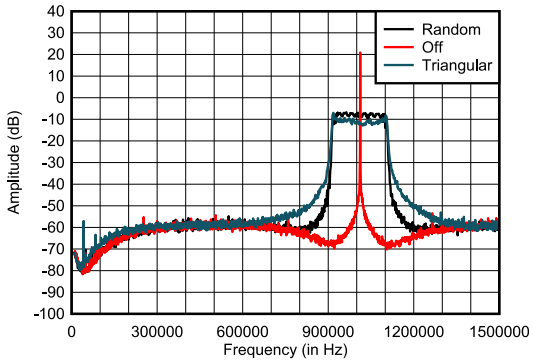
図 6-25. V_{OUT} Ripple After the Second L-C Filter



BW = 10 kHz

5 V to 3.3 V, 1 A　　2.2 µH, 2.2 MHz　　First and second L-C

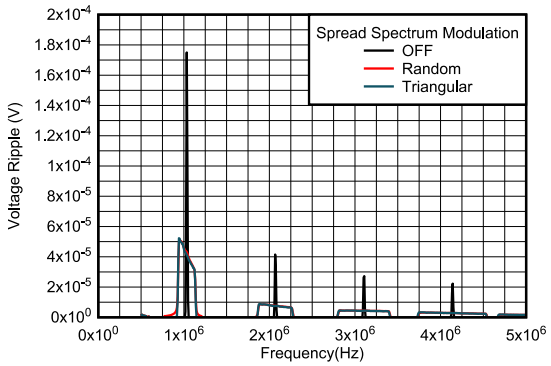
図 6-26. V_{OUT} Ripple FFT After the Second L-C Filter



6 V to 1.2 V, 1 A　　2.2 µH, 1 MHz　　BW = 50 Hz

S-CONF = OFF, Triangular, Random

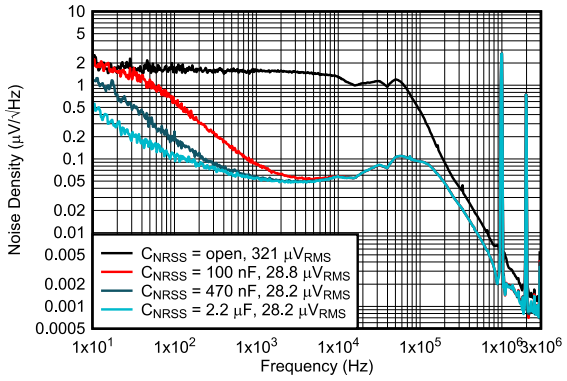
図 6-27. Spread Spectrum FFT - 50-Hz BW



12 V to 1.2 V, 2 A　　2.2 µH, 1 MHz　　BW = 10 kHz

S-CONF = OFF, Triangular, Random

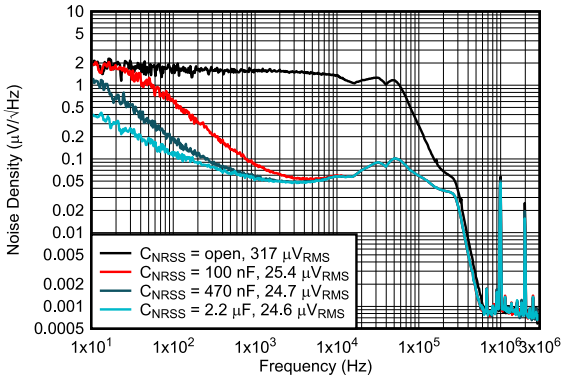
図 6-28. Spread Spectrum FFT - 10-kH BW



12 V to 1.2 V　　2.2 µH, 1 MHz　　First L-C Only

NR/SS = Open, 100 nF, 470 nF, 2.2 µF, BW = 100 Hz to 100 kHz

図 6-29. Output Noise Density vs Frequency

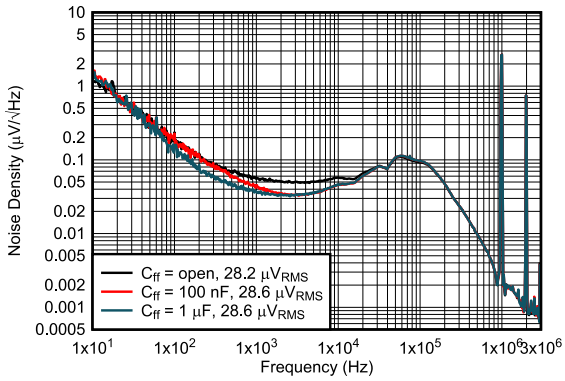


12 V to 1.2 V　　2.2 µH, 1 MHz　　After ferrite bead filter

NR/SS = Open, 100 nF, 470 nF, 2.2 µF, BW = 100 Hz to 100 kHz

図 6-30. Output Noise Density vs Frequency

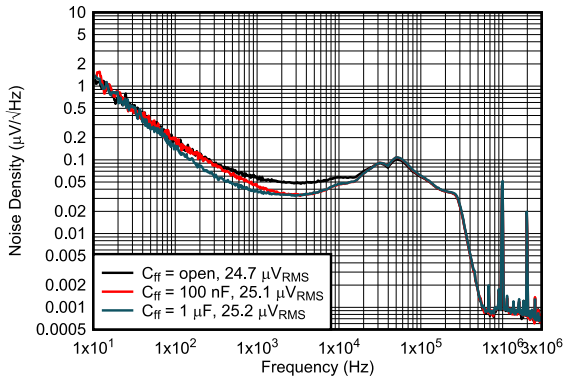
6.6 Typical Characteristics (continued)



12 V to 1.2 V　　2.2 µH, 1 MHz　　First L-C Only

NR/SS = 470 nF, C_{FF} = Open, 100 nF, 1 µF, BW = 100 Hz to 100 kHz

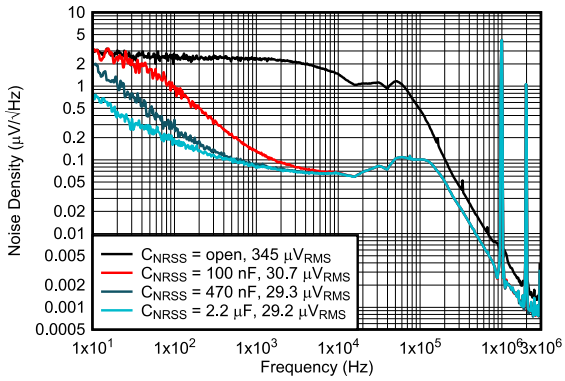
図 6-31. Output Noise Density vs Frequency



12 V to 1.2 V　　2.2 µH, 1 MHz　　After ferrite bead filter

NR/SS = 470 nF, C_{FF} = Open, 100 nF, 1 µF, BW = 100 Hz to 100 kHz

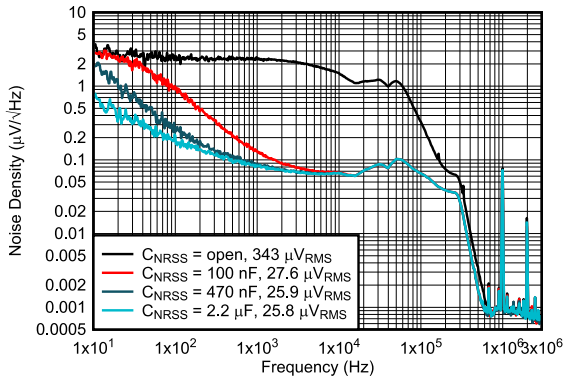
図 6-32. Output Noise Density vs Frequency



12 V to 1.8 V　　2.2 µH, 1 MHz　　First L-C Only

NR/SS = Open, 100 nF, 470 nF, 2.2 µF, BW = 100 Hz to 100 kHz

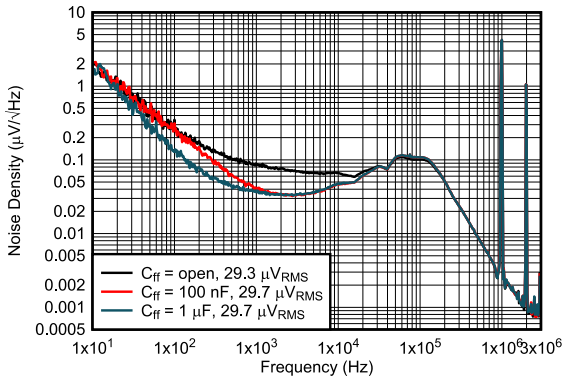
図 6-33. Output Noise Density vs Frequency



12 V to 1.8 V　　2.2 µH, 1 MHz　　After ferrite bead filter

NR/SS = Open, 100 nF, 470 nF, 2.2 µF, BW = 100 Hz to 100 kHz

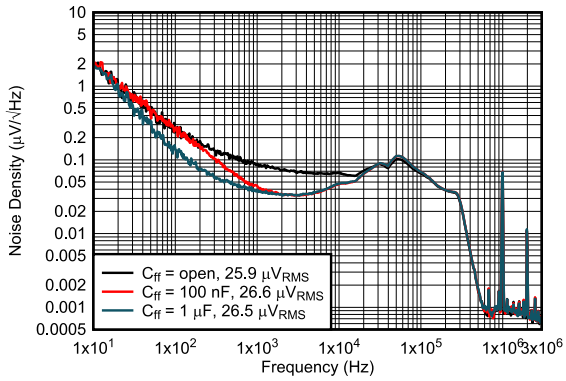
図 6-34. Output Noise Density vs Frequency



12 V to 1.8 V　　2.2 µH, 1 MHz　　First L-C Only

NR/SS = 470 nF, C_{FF} = Open, 100 nF, 1 µF, BW = 100 Hz to 100 kHz

図 6-35. Output Noise Density vs Frequency

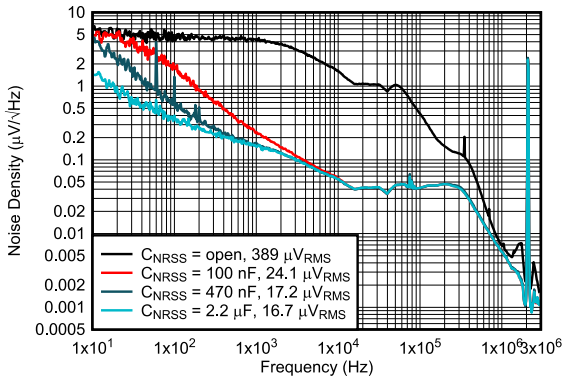


12 V to 1.8 V　　2.2 µH, 1 MHz　　After ferrite bead filter

NR/SS = 470 nF, C_{FF} = Open, 100 nF, 1 µF, BW = 100 Hz to 100 kHz

図 6-36. Output Noise Density vs Frequency

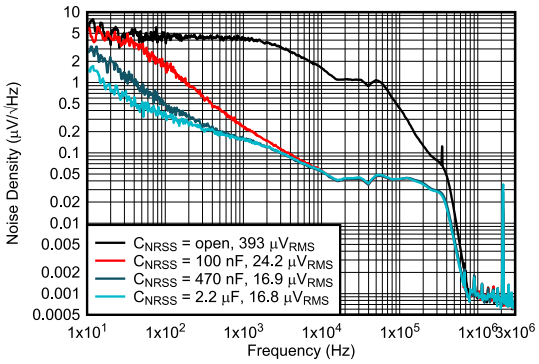
6.6 Typical Characteristics (continued)



12 V to 3.3 V 2.2 µH, 2.2 MHz First L-C Only

NR/SS = Open, 100 nF, 470 nF, 2.2 µF, BW = 100 Hz to 100 kHz

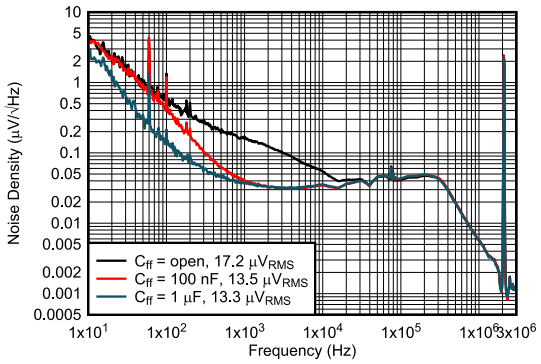
図 6-37. Output Noise Density vs Frequency



12 V to 3.3 V 2.2 µH, 2.2 MHz After ferrite bead filter

NR/SS = Open, 100 nF, 470 nF, 2.2 µF, BW = 100 Hz to 100 kHz

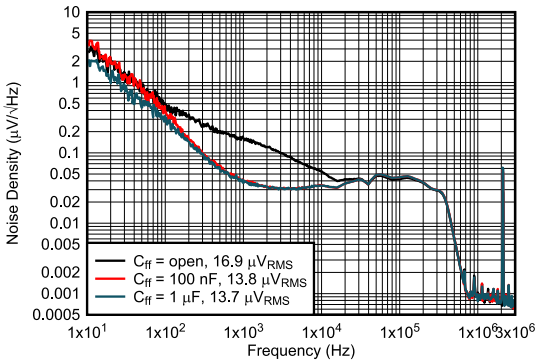
図 6-38. Output Noise Density vs Frequency



12 V to 3.3 V 2.2 µH, 2.2 MHz First L-C Only

NR/SS = 470 nF, C_{FF} = Open, 100 nF, 1 µF, BW = 100 Hz to 100 kHz

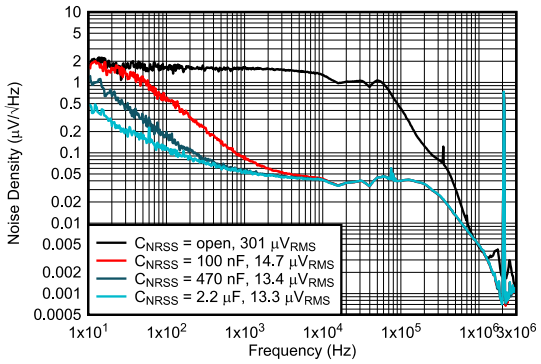
図 6-39. Output Noise Density vs Frequency



12 V to 3.3 V 2.2 µH, 2.2 MHz After ferrite bead filter

NR/SS = 470 nF, C_{FF} = Open, 100 nF, 1 µF, BW = 100 Hz to 100 kHz

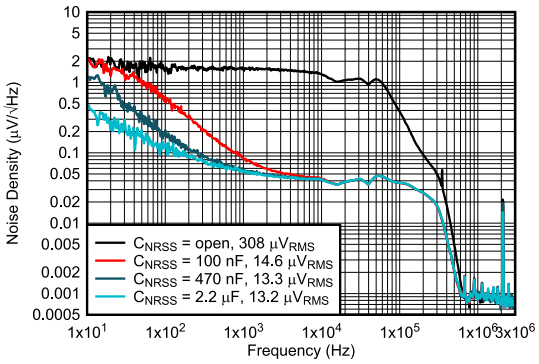
図 6-40. Output Noise Density vs Frequency



5 V to 1.2 V 2.2 µH, 2.2 MHz First L-C Only

NR/SS = Open, 100 nF, 470 nF, 2.2 µF, BW = 100 Hz to 100 kHz

図 6-41. Output Noise Density vs Frequency

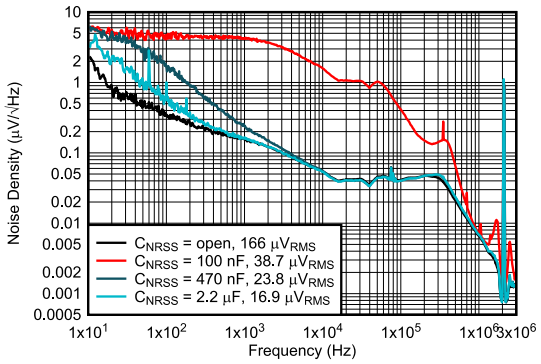


5 V to 1.2 V 2.2 µH, 2.2 MHz After ferrite bead filter

NR/SS = Open, 100 nF, 470 nF, 2.2 µF, BW = 100 Hz to 100 kHz

図 6-42. Output Noise Density vs Frequency

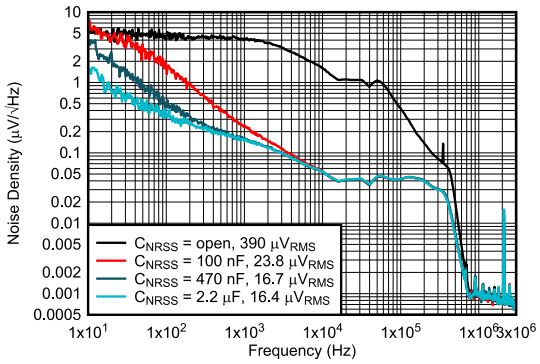
6.6 Typical Characteristics (continued)



5 V to 3.3 V 2.2 µH, 2.2 MHz First L-C Only

NR/SS = Open, 100 nF, 470 nF, 2.2 µF, BW = 100 Hz to 100 kHz

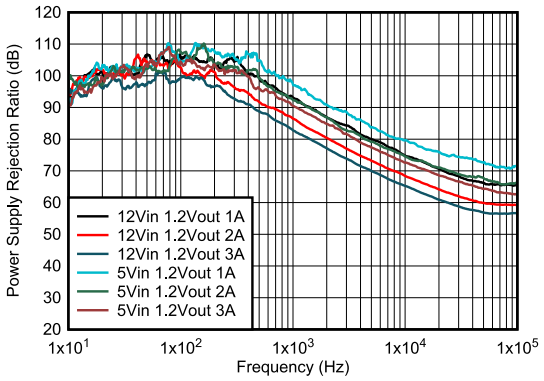
図 6-43. Output Noise Density vs Frequency



5 V to 3.3 V 2.2 µH, 2.2 MHz After ferrite bead filter

NR/SS = Open, 100 nF, 470 nF, 2.2 µF, BW = 100 Hz to 100 kHz

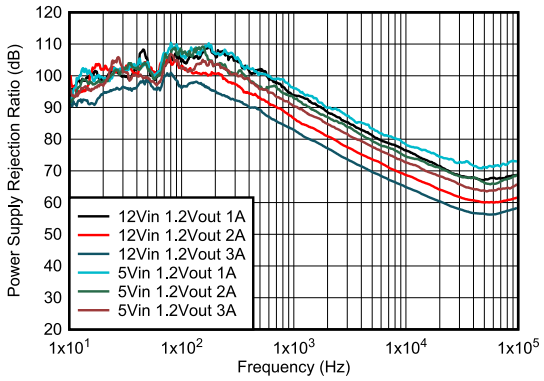
図 6-44. Output Noise Density vs Frequency



12 V to 1.2 V 2.2 µH, 1 MHz 1 A, 2 A, 3 A

First L-C Only, No Ferrite Bead

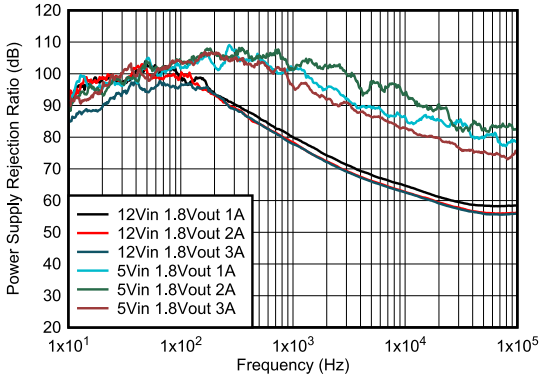
図 6-45. PSRR vs Frequency



12 V to 1.2 V 2.2 µH, 1 MHz 1 A, 2 A, 3 A

After Ferrite Bead Filter

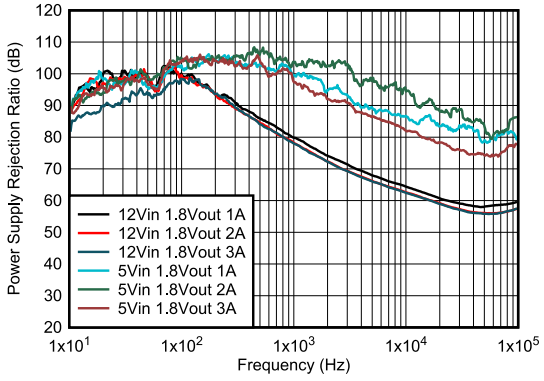
図 6-46. PSRR vs Frequency



12 V to 1.8 V 2.2 µH, 1 MHz 1 A, 2 A, 3 A

First L-C Only, No Ferrite Bead

図 6-47. PSRR vs Frequency

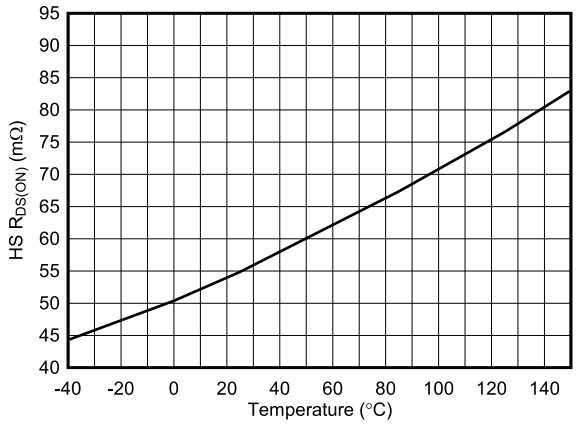


12 V to 1.8 V 2.2 µH, 1 MHz 1 A, 2 A, 3 A

After Ferrite Bead

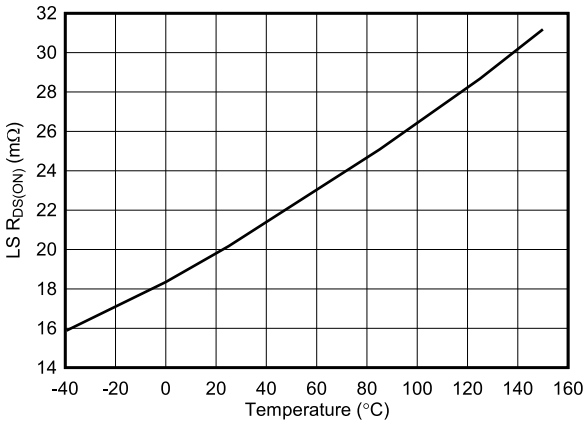
図 6-48. PSRR vs Frequency

6.6 Typical Characteristics (continued)



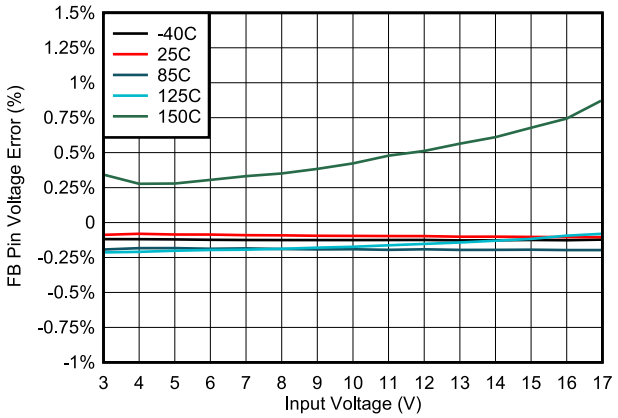
VIN = 5 V

図 6-49. High-Side $R_{DS(ON)}$ vs Junction Temperature



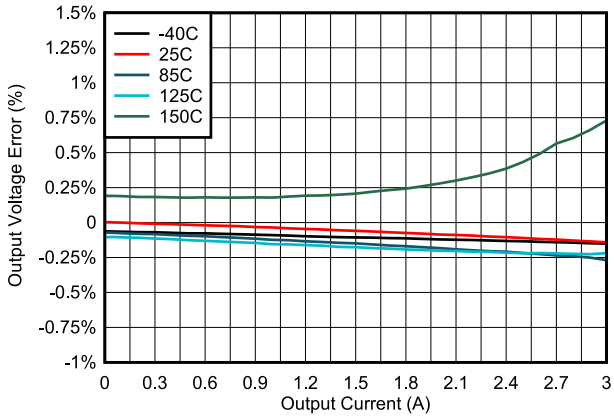
VIN = 5 V

図 6-50. Low-Side $R_{DS(ON)}$ vs Junction Temperature



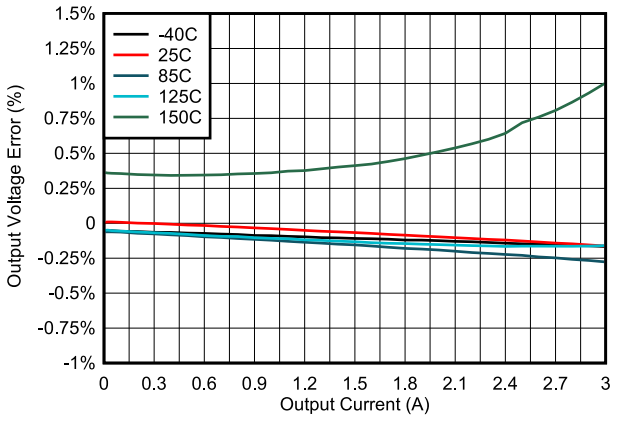
1 MHz, 2 A

図 6-51. FB Pin Voltage Error vs Input Voltage



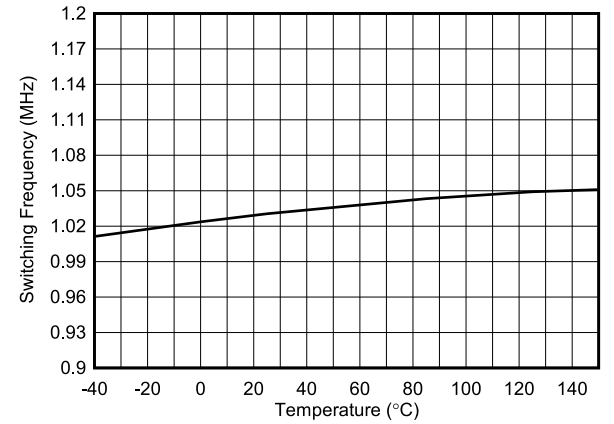
5 V_{IN} to 0.8 V_{OUT} 1 MHz

図 6-52. Output Voltage Error vs Load



12 V_{IN} to 0.8 V_{OUT} 1 MHz

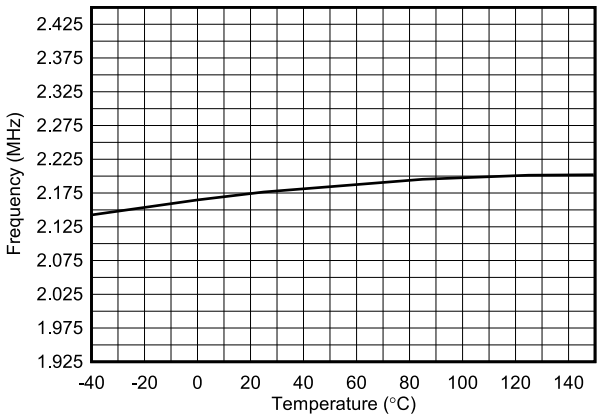
図 6-53. Output Voltage Error vs Load



12 V_{IN} 1 MHz

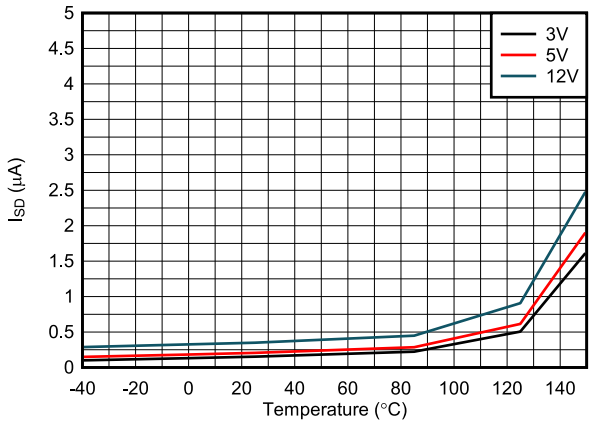
図 6-54. Oscillator Frequency vs Temperature

6.6 Typical Characteristics (continued)



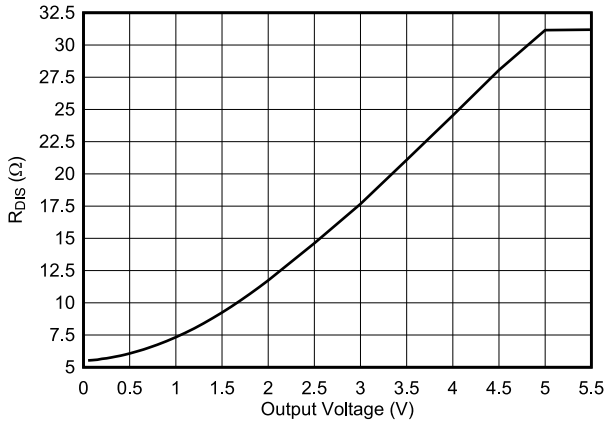
12 V_{IN} 2.2 MHz

図 6-55. Oscillator Frequency vs Temperature



V_{IN}: 3 V, 5 V, 12 V

図 6-56. Shutdown Current vs Temperature



V_{IN}: 12 V 25°C

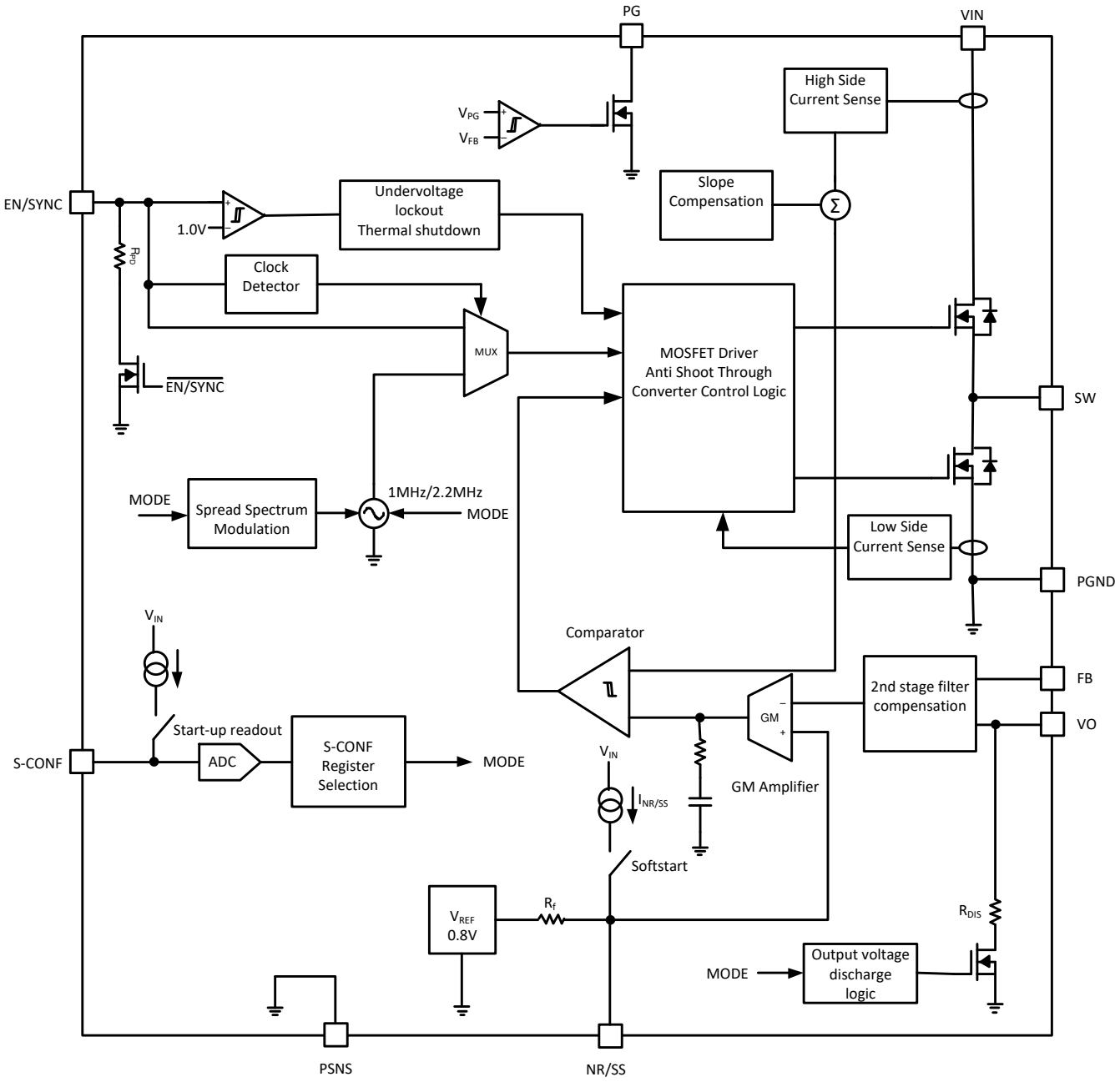
図 6-57. Output Discharge Resistance vs Output Voltage

7 Detailed Description

7.1 Overview

The TPS6291x low-noise, low-ripple synchronous buck converter is a fixed frequency current mode converter. The converter has a filtered internal reference to achieve a low-noise output similar to low-noise LDOs. The converter achieves lower output voltage ripple by using a switching frequency of either 2.2 MHz or 1 MHz and a larger inductance. The output voltage ripple can be further reduced by adding a small second stage L-C filter to the output. This can be a ferrite bead or a small inductor, followed by an output capacitor. Internal compensation maintains stability with an external filter inductor up to 50 nH. To avoid voltage drops across this second stage filter, the device regulates the output voltage after the filter. The TPS6291x family supports an optional spread spectrum modulation. For example, when powering ADCs, spread spectrum modulation reduces the mixing spurs. Switching frequency, spread spectrum modulation, and output discharge are set using the S-CONF pin.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Smart Config (S-CONF)

This S-CONF pin configures the device based on the resistor value. This pin is read after EN/SYNC goes high. The device configuration cannot be changed during operation. The S-CONF value is re-read if EN is pulled below 200 mV or if VIN falls below UVLO. 表 7-1 shows the configuration options of the following:

- Switching frequency
- Spread spectrum modulation
- Output discharge
- Synchronization

表 7-1. S-CONF Device Configuration Modes

S-CONF	SWITCHING FREQUENCY	SPREAD SPECTRUM	OUTPUT DISCHARGE	SYNCHRONIZATION
VIN	2.2 MHz	OFF	OFF	No
GND	1 MHz	OFF	OFF	No
4.87 kΩ	2.2 MHz	OFF	OFF	1.9 MHz to 2.42 MHz
6.04kΩ	2.2MHz	Triangle	OFF	No
7.5 kΩ	2.2 MHz	Random	OFF	No
9.31 kΩ	1 MHz	OFF	OFF	0.9 MHz to 1.2 MHz
11.5kΩ	1MHz	Triangle	OFF	No
14.3 kΩ	1 MHz	Random	OFF	No
			Discharge On	
18.2 kΩ	2.2 MHz	OFF	ON	No
22.1 kΩ	1 MHz	OFF	ON	No
27.4 kΩ	2.2 MHz	OFF	ON	1.9 MHz to 2.42 MHz
34kΩ	2.2MHz	Triangle	ON	No
42.2 kΩ	2.2 MHz	Random	ON	No
52.3 kΩ	1 MHz	OFF	ON	0.9 MHz to 1.2 MHz
64.9kΩ	1MHz	Triangle	ON	No
80.6 kΩ	1 MHz	Random	ON	No

7.3.2 Device Enable (EN/SYNC)

The device is enabled by pulling the EN/SYNC pin high, and has an accurate rising threshold voltage of typically 1.01 V. Once the device is enabled, the operation mode is set by the configuration of the S-CONF pin. This occurs during the device start-up delay time t_{delay}. Once t_{delay} expires, the internal soft-start circuitry ramps up the output voltage over the soft-start time set by the $C_{NR/SS}$ capacitor. The start-up delay time t_{delay} varies depending on the selected S-CONF value. It is shortest with smaller S-CONF resistors.

The EN/SYNC pin has an active pulldown resistor R_{PD}. This prevents an uncontrolled start-up of the device, in case the EN/SYNC pin cannot be driven to a low level. The pulldown resistor is disconnected after start-up. With EN set to a low level, the device enters shutdown and the pulldown resistor is activated again.

7.3.3 Device Synchronization (EN/SYNC)

The EN/SYNC pin is also used for device synchronization. Once a clock signal is applied to this pin, the device is enabled and reads the configuration of the S-CONF pin. The external clock frequency must be within the clock synchronization frequency range set by the S-CONF pin. When the clock signal changes from a clock to a static high, then the device switches from external clock to internal clock. To shutdown the device when using an external clock, EN/SYNC must go low for at least 10 µs.

The clock signal can be a logic signal with a logic level as specified in the electrical table, and can be applied directly to the EN/SYNC pin. External logic, such as an AND gate, can be used to combine separate enable and clock inputs, as shown in 図 7-1.

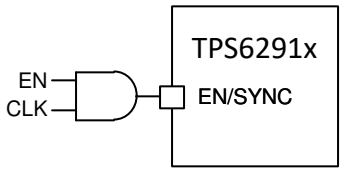


図 7-1. Synchronization with Separate Enable Signal (optional)

7.3.4 Spread Spectrum Modulation

Using the S-CONF pin enables or disables spread spectrum modulation. DC/DC converters generate an output voltage ripple at the switching frequency. When powering ADCs or an analog front end (AFE), the switching frequency generates high frequency mixing spurs as well as a low frequency spur in the output frequency spectrum. Using the optional second stage L-C filter reduces the ripple of the converter and spurs by up to 30 dB.

The device has integrated two different spread spectrum modulation (SSM) schemes that are selected by the resistor connected to the S-CONF pin acording to 表 7-1. It is possible to select random or triangle modulation to spread the switching frequency over a larger frequency range. The triangular SSM is modulated based on the switching frequency, and results in 1.9 kHz for 1 MHz switching frequency and 4.3 kHz for 2.2 MHz switching frequency. The modulation spread is ±10% of the device switching frequency. This SSM provides high attenuation when the receiver bandwidth is less than the modulation frequency, typically the case for systems using Fast Fourier Transforms (FFT) post processing as in high speed ADC applications. For applications sensitive to noise at the modulation frequency, random SSM is used. Using a random spread spectrum modulation also reduces the spurs in the output spectrum as shown in 図 6-2. The random SSM operates with the same frequency spread and modulation period as the triangular SSM. The randomized modulation uses a Fibonacci Linear-Feedback Shift Register (LFSR) so that every tone is generated once during the pseudo-random generation period. The frequency spreading is shown in 図 7-2.The attenuation using random or triangle SSM is shown in 図 6-28.

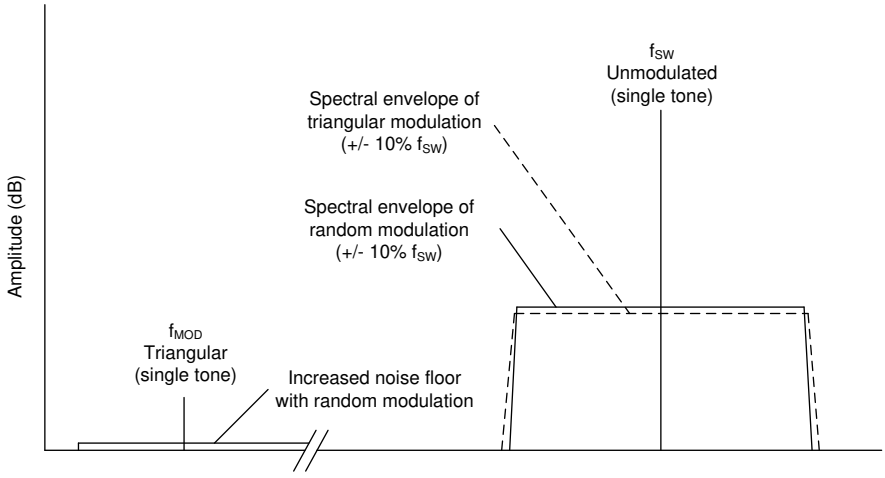


図 7-2. Spread Spectrum Modulation

7.3.5 Output Discharge

Output discharge is enabled or disabled, depending on the S-CONF setting. With output discharge enabled, the output voltage is pulled low by a discharge resistor R_{DIS} of typically 7 Ω. The output discharge function is enabled during thermal shutdown, UVLO, or when EN/SYNC is pulled low.

7.3.6 Undervoltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages, the device is enabled once the input voltage is above the undervoltage lockout threshold. The device is disabled once the input voltage falls below the undervoltage threshold.

7.3.7 Power-Good Output

The device has a power-good output. The PG pin goes high impedance once the FB pin voltage is above 95% of the nominal voltage, and is driven low once the voltage falls below typically 90% of the nominal voltage. 表 7-2 shows the typical PG pin logic. The PG pin is an open-drain output and is specified to sink up to 10 mA. The power-good output requires a pullup resistor connecting to any voltage rail less than 18 V. The PG signal can be used for sequencing of multiple rails by connecting to the EN pin of other converters. If not used, the PG pin can be left floating or connected to GND. PG has a deglitch time of typically 8 µs before going low.

表 7-2. Power Good Pin Logic

DEVICE STATE		PG LOGIC STATUS	
		HIGH IMPEDANCE	LOW
Enabled (EN/SYNC = High)	$V_{FB} \geq V_{PG}$	√	
	$V_{FB} < V_{PG}$ after t_{PG}		√
Shutdown (EN/SYNC = Low)			√
UVLO	$0.7\ V < V_{IN} < V_{UVLO}$		√
Thermal Shutdown	$T_J > T_{JSD}$		√
Power Supply Removal	$V_{IN} < 0.7\ V$	√	

7.3.8 Noise Reduction and Soft-Start Capacitor (NR/SS)

A capacitor connected to this pin reduces the low frequency noise of the converter and sets the soft-start time. The larger the capacitor, the lower the noise and the longer the start-up time of the converter. A 470-nF capacitor is typically connected to this pin for a start-up time of 5 ms, although longer and shorter start-up times can be used. During soft start with a light load, the device skips switching pulses as needed to not discharge the output voltage. The device can start into a pre-biased output voltage.

The device achieves low noise by adding an R-C filter to the reference voltage, as shown in *セクション 7.2*. During start-up, the NR/SS capacitor is charged with a constant current of 75 µA (typ) to 0.8 V. Larger NR/SS capacitors provide for lower low frequency noise, as shown in 図 6-29. The maximum NR/SS cap is 3.3 µF for a start-up time of 35 ms. The minimum start-up time is set internally to 0.7 ms, which occurs when there is a small NR/SS capacitor or no NR/SS capacitor.

7.3.9 Current Limit and Short Circuit Protection

The device is protected against short circuits and overcurrent. The switch current limit prevents the device from high inductor current and from drawing excessive current from the input voltage rail. Excessive current can occur with a shorted/saturated inductor or a heavy load/shorted output circuit condition. If the inductor current reaches the threshold I_{SWpeak}, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. The high-side MOSFET is turned on again only when the low-side current is below the low-side sourcing current limit $I_{SWvalley}$.

Due to internal propagation delay, the actual current can exceed the static current limit, especially if the input voltage is high and very small inductances are used. The dynamic current limit is calculated as follows:

$$I_{peak(typ)} = I_{SWpeak} + \left(\frac{V_L}{L}\right) \times t_{PD} \quad (1)$$

where

- I_{SWpeak} is the static current limit, specified in *セクション 6.5*

- L is the inductance
- V_L is the voltage across the inductor (VIN - VOUT)
- t_{PD} is the internal propagation delay, typically 50 ns

The low-side MOSFET also contains a negative current limit to prevent excessive current from flowing back through the inductor to the input. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off. In this scenario, both MOSFETs are off until the start of the next cycle.

7.3.10 Thermal Shutdown

The device goes into thermal shutdown once the junction temperature exceeds typically 170°C with a 20°C hysteresis.

7.4 Device Functional Modes

7.4.1 Fixed Frequency Pulse Width Modulation

To minimize output voltage ripple, the device operates in fixed frequency PWM operation down to no load. The switching frequency of 1 MHz or 2.2 MHz is selected using the S-CONF pin.

7.4.2 Low Duty Cycle Operation

For high input voltages or low output voltages, the 70-nsec minimum on-time limits the maximum input to output voltage difference and the switching frequency selected. When the minimum on-time is reached, the output voltage rises above the regulation point. Refer to 表 8-2 for detailed design recommendations.

7.4.3 High Duty Cycle Operation (100% Duty Cycle)

The device offers a low input-to-output voltage differential by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on. The minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, is calculated as:

$$V_{IN(\min)} = V_{OUT(\min)} + I_{OUT} \times (R_{DS(ON)} + R_L) \quad (2)$$

where

- $V_{OUT(min)}$ is the minimum output voltage the load can accept
- I_{OUT} is the output current
- $R_{DS(ON)}$ is the $R_{DS(ON)}$ of the high-side MOSFET
- R_L is the DC resistance of the inductor used

To maintain fixed frequency switching, the device requires a minimum off-time of 50 ns (typ), 60 ns (max). If this limit is reached during a switching pulse, the device skips switching pulses to maintain output voltage regulation. If the input voltage decreases further, the device enters 100% mode.

7.4.4 Second Stage L-C Filter Compensation (Optional)

Most low-noise and low-ripple applications use a ferrite bead and bypass capacitor before the load. Using a second L-C filter is especially useful for low-noise and low-ripple applications with constant load current such as ADCs, DACs, and Jitter Cleaner. The second stage L-C filter is optional, and the device can be used without this filter. Without the filter, the device has a low output voltage noise of typically 16.9 μV_{RMS} shown in 図 6-37 with an output voltage ripple of 280 μV_{RMS} shown in 図 6-12. The second stage L-C filter attenuates the output voltage ripple by another approximately 30 dB shown in 図 6-14. To improve load regulation, the device can remote sense the output voltage after the second stage L-C filter and is internally compensated for the additional double pole generated by the L-C filter.

To keep the second stage L-C filter as small as possible, the internal compensation is optimized for a 10-nH to 50-nH inductance. A small ferrite bead or even a PCB trace provides sufficient inductance for output voltage ripple filtering. See *セクション 8.2.2.2.4* for details.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TPS6291x family of devices are optimized for low noise and low output voltage ripple.

8.2 Typical Applications

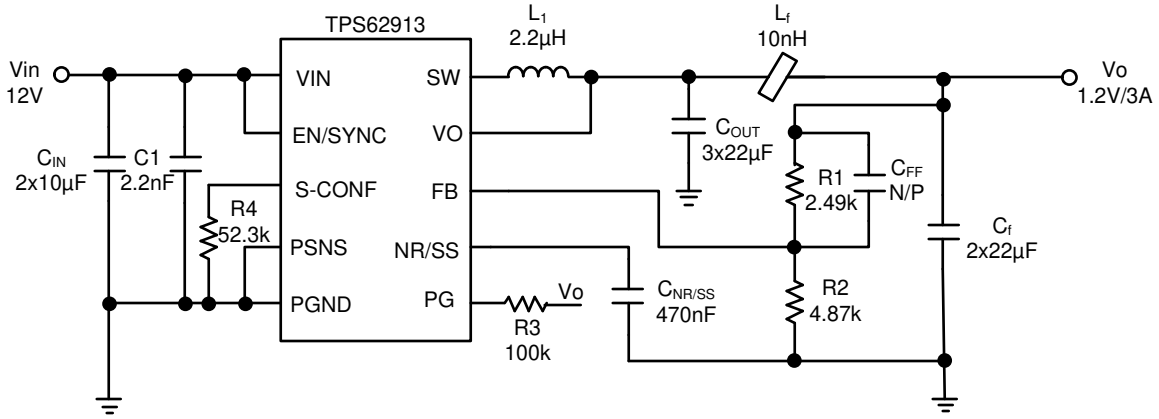


図 8-1. Typical Schematic

表 8-1 shows the list of components for the application curves in *セクション 8.2.3*, unless otherwise noted.

表 8-1. List of Components

REFERENCE	PART NUMBER	DESCRIPTION	MANUFACTURER(1)
TPS62913	TPS62913	Low Noise and low ripple buck converter	Texas Instruments
L_1	XGL4030-222MEC or XGL4030-472MEC	Inductor: 2.2 µH or 4.7 µH	Coilcraft
C_{IN}	C2012X7S1E106K125AC	Ceramic capacitors: 2 × 10 µF ±10% 25-V ceramic capacitor X7S 0805	TDK
C_{OUT}	C2012X7S1A226M125AC	Ceramic capacitors: 3 × 22 µF, 10 V, ±20%, X7S, 0805	TDK
L_f	BLE18PS080SN1	Ferrite Bead	MuRata
C_f	C2012X7S1A226M125AC	Ceramic capacitor: 2 × 22 µF, 10 V, ±20%, X7S, 0805	TDK
C_1	GRM155R71H222KA01D	Ceramic capacitor: 2200 pF, 50 V, ±10%, X7R, 0402	MuRata
$C_{NR/SS}$, C_{FF}		Ceramic capacitor	Standard
R1, R2, R3, R4		Resistor	Standard

(1) See the *Third-Party Porducts Disclaimer*

8.2.1 Design Requirements

The external components have to fulfill the needs of the application, but also meet the stability criteria of the control loop of the device. The device is optimized to work within a range of external components, and can be optimized for the following:

- Efficiency
- Output ripple
- Component count
- Lowest 1/f noise

Typical applications that have input voltages of ≤ 6 V use a 2.2-µH inductor with a 2.2-MHz switching frequency. Applications that have input voltages > 6 V can be optimized for efficiency using a 2.2-µH inductor with a 1-MHz switching frequency. In this case, the output voltage ripple doubles compared to the use of a 4.7-µH inductor, which is typically acceptable when powering high speed ADCs. Optimization for powering clock and PLL circuits that need a 3.3-V output use a 2.2-µH inductor with 2.2-MHz switching frequency, minimizing output voltage ripple and low frequency noise.

For the application cases that are not found in 表 8-2, there are two methods to design the TPS6291x circuit. *セクション 8.2.2.1* uses Webench to design the circuit automatically or the calculations in *セクション 8.2.2.2* can be used instead.

表 8-2. Typical Single L-C Filter Design Recommendations

DESIGN GOAL	V_{IN}	V_{OUT}	F_{SW}	INDUCTOR [2]	OUTPUT CAPACITORS [3]
Typical	12 V[1]	≤ 2.0 V[1]	1 MHz	2.2 µH	3 × 22 µF, 10 V, 0805
Typical	12 V	2.0 V < V_{OUT} ≤ 3.3 V	1 MHz	4.7 µH	3 × 22 µF, 10 V, 0805
Typical	12 V	> 3.3 V	2.2 MHz	2.2 µH	1 × 47 µF, 1210 and 2 × 22 µF, 10 V, 0805
Higher Efficiency (with higher ripple and noise)	12 V	2.0 V < V_{OUT} ≤ 3.3 V	1 MHz	2.2 µH[4]	3 × 22 µF, 10 V, 0805
Low ripple/noise PLL and Clock Supply	12 V	2.6 V ≤ V_{OUT} ≤ 3.3 V	2.2 MHz	2.2 µH	3 × 22 µF, 10V, 0805
Typical	5 V	≤ 3.3 V	2.2 MHz	2.2 µH	3 × 22 µF, 10 V, 0805
Typical	5 V	> 3.3V	2.2 MHz	2.2 µH	1 × 47 µF, 1210 and 2 × 22 µF, 10 V, 0805

(1) The maximum input to output voltage difference is limited by the device maximum minimum on-time of 70 ns. This is especially important for input voltages above 12 V or output voltages below 1 V. See *セクション 8.2.2.2.1*.
(2) For inductor part numbers, see 表 8-4.
(3) For output capacitor part numbers, see 表 8-5.
(4) The TPS62913 requires a 4.7-µH inductor when using the 1-MHz switching frequency to supply more than 2.5-A load current when the output voltage is greater than 2.0 V.

The second stage L-C filter is optional, as the device can be used without this filter to achieve below 20-μV_{RMS} noise typically. A second stage filter is added to provide additional attenuation of the output ripple voltage. The output voltage is sensed after the second L-C filter by connecting the FB resistors to the second stage L-C filter capacitor. This provides remote sense, minimizing output voltage drop due to the ferrite bead. Refer to 表 8-3 for second stage L-C filter recommendations based on the output voltage.

表 8-3. Second Stage L-C (Ferrite Bead) Filter Design Recommendations

V_{OUT} (V)	FERRITE BEAD IMPEDANCE (AT 100 MHZ)[2]	OUTPUT CAPACITORS [1]
≤ 3.3 V	8 to 20 Ω	2 × 22 µF, 10 V, 0805
> 3.3 V	8 to 20 Ω	3 × 22 µF, 10 V, 0805

(1) For output capacitor part numbers, see 表 8-5.
(2) For second stage L-C filter part numbers, see 表 8-6.

8.2.2 Detailed Design Procedure

If the specific design is not found in the *表 8-2* section, WEBENCH is recommended to generate the design. Alternatively, the manual design procedure in *External Component Selection* can be followed.

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS6291x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost.
3. Open the advanced tab to optimize for output voltage ripple.
4. Once in a TPS6291x design, you can enable the second stage L-C filter and change other settings from the drop-down on the left.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 External Component Selection

8.2.2.2.1 Switching Frequency Selection

The switching frequency can be chosen to optimize efficiency (1 MHz) or ripple/noise (2.2 MHz). Using the 2.2-MHz setting increases the gain of the feedback loop and can result in lower output noise. However, additional considerations for minimum on-time and duty cycle must also be considered. First, calculate the duty cycle using 式 3. Higher efficiency results in a shorter on-time, so a conservative approach is to use a higher efficiency than expected in the application.

$$D = \frac{V_{OUT}}{V_{IN} \times \eta} \tag{3}$$

where

- η is the estimated efficiency (use the value from the efficiency curves or 0.9 as an conservative assumption)

Then, calculate the on-time with both 1 MHz and 2.2 MHz using 式 4. The on-time must always remain above the minimum on-time of 70 nsec. Use the maximum input voltage and maximum efficiency to determine the minimum duty cycle, D_{min}. Use the maximum switching frequency for f_{SW}.

$$t_{ON\_min} = \frac{D_{min}}{f_{SW\_max}} \tag{4}$$

then

- If t_{ON_min} min < 70 ns with 2.2 MHz, use 1 MHz.
- If t_{ON_min} min < 70 ns with 1 MHz, reduce the maximum input voltage.
- If t_{ON_min} min ≥ 70 ns for both cases, use 1 MHz for highest efficiency, or 2.2 MHz for lowest noise and ripple.

8.2.2.2.2 Inductor Selection for the First L-C Filter

The inductor selection is dependent on the selected switching frequency and the duty cycle. When using the 2.2-MHz frequency, only use a 2.2-µH inductor. When using the 1-MHz frequency, calculate the maximum duty cycle using the minimum input voltage. If D_{max} is above 45%, only use a 4.7-µH inductor. If D_{max} is below 45% and the output voltage is 2 V or less, use only a 2.2-µH inductor. If D_{max} is below 45% and the output voltage is above 2 V, use a 4.7-µH inductor to achieve the full output current or a 2.2-µH inductor for higher efficiency with a reduced maximum output current.

The inductor also has to be rated for the appropriate saturation current. 式 5 and 式 6 calculate the maximum inductor current under static load conditions. The formula takes the converter efficiency into account. The calculation must be done for the maximum input voltage where the peak switch current is highest.

$$\Delta I_L = \frac{\frac{V_{OUT}}{\eta} \times \left(1 - \frac{V_{OUT}}{V_{IN} \times \eta}\right)}{f_{SW} \times L} \tag{5}$$

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \tag{6}$$

where

- f_{SW} is the switching frequency (typically 1 MHz or 2.2 MHz)
- L is inductance
- η is estimated efficiency (use the value from the efficiency curves or 0.9 as an conservative assumption)

注

The calculation must be done for the maximum input voltage of the application.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current. A margin of 20% is recommended to be added to cover for load transients during operation.

See 表 8-4 for typical inductors.

表 8-4. Inductor Selection

INDUCTOR VALUE	MANUFACTURER	PART NUMBER	SIZE (L X W X H IN mm)	ISAT/DCR (30% DROP)
2.2 µH	Coilcraft	XGL4020-222	4 × 4 × 2.1	6.2 A / 19.5 mΩ
2.2 µH	Coilcraft	XGL4030-222	4 × 4 × 3.1	7 A / 13.5 mΩ
2.2 µH	Wurth Elektronik	74438356022	4.1 × 4.1 × 2.1	5.2 A / 35 mΩ
2.2 µH	Wurth Elektronik	74438357022	4.1 × 4.1 × 3.1	7 A / 26 mΩ
2.2 µH	MuRata	DFE322520FD-2R2M=P2	3.2 × 2.5 × 2	5 A / 46 mΩ
4.7 µH	Coilcraft	XGL4020-472	4 × 4 × 2.1	4.1 A / 43.0 mΩ
4.7 µH	Coilcraft	XGL4030-472	4 × 4 × 3.1	4.4 A / 28.5 mΩ
4.7 µH for TPS62912 only	MuRata	DFE322520FD-4R7M=P2	3.2 × 2.5 × 2	3.4 A / 98 mΩ

8.2.2.2.3 Output Capacitor Selection

The effective output capacitance can range from 40 µF (minimum) up to 200 µF (maximum) for a single L-C system design. When using a second L-C filter, the first L-C filter must have output capacitance between 40 µF and 80 µF, the second stage L-C filter (if used) must have at least 20 µF of capacitance, and the total capacitance for both L-C filters must be less than 200 µF. Load transient testing and measuring the bode plot are good ways to verify stability.

Ceramic capacitors (X5R or X7R) are recommended. Ceramic capacitors have a DC-Bias effect, which has a strong influence on the final effective capacitance. Choose the right capacitor carefully in combination with considering its package size and voltage rating. The ESR and ESL of the output capacitor are also important considerations in selecting the output capacitors for low noise applications. Smaller package sizes typically have lower ESL and ESR. 0805 or smaller packages are recommended, as long as they provide the required capacitance and voltage rating for stable operation. 表 8-5 lists recommended output capacitors.

表 8-5. Recommended Output Capacitors

CAPACITOR TYPE	CAPACITOR VALUE	MANUFACTURER	VOLTAGE (V)	PACKAGE
Bulk Capacitor	22 µF, X7S	TDK C2012X7S1A226M125AC	10	0805

表 8-5. Recommended Output Capacitors (continued)

CAPACITOR TYPE	CAPACITOR VALUE	MANUFACTURER	VOLTAGE (V)	PACKAGE
Bulk Capacitor	47 µF, X7R	Murata GRM32ER71A476ME15L	10	1210

8.2.2.2.4 Ferrite Bead Selection for Second L-C Filter

Using a ferrite bead for the second stage L-C filter minimizes the external component count because most of the noise sensitive circuits use a RF bead for high frequency attenuation as a default component at their inputs.

It is important to select a ferrite bead with sufficiently high inductance at full load, and with low DC resistance (below 10 mΩ) to keep the converter efficiency as high as possible. The ferrite bead inductance decreases with increased load current. Therefore, the ferrite bead should have a current rating much higher than the desired load current.

The recommendation is to choose a ferrite bead with an impedance of 8 Ω to 20 Ω at 100 MHz. Refer to 表 8-6 for possible ferrite beads.

表 8-6. Recommended Ferrite Beads

PART NUMBER	MANUFACTURER	SIZE	IMPEDANCE AT 100 MHZ	INDUCTANCE AT 100 MHz (CALCULATED)	DC RESISTANCE	CURRENT RATING
BLE18PS080SN1	MuRata	0603	8.5 Ω	13.5 nH	4 mΩ	5 A
74279221100	Wurth Elektronik	1206	10 Ω	15.9 nH	3 mΩ	10.5 A
7427922808	Wurth Electronik	0603	8 Ω	12.7 nH	5 mΩ	9.5 A

The internal compensation has been designed to be stable with up to 50 nH of inductance in the second stage filter. To achieve low ripple, the second L-C filter requires only 5-nH to 10-nH inductance. The inductance can be estimated from the ferrite bead impedance specification at 100 MHz, with the assumption that the inductance is similar at the selected converter switching frequency of 1 MHz or 2.2 MHz, and can be verified through tools available on some manufacturer websites. The inductance of a ferrite bead is calculated using 式 7:

$$L = \frac{Z}{(2 \times \pi \times f)} \tag{7}$$

where

- Z is the impedance of the ferrite bead in ohms at the specified frequency (usually 100 MHz)
- f is the specified frequency (usually 100 MHz)

8.2.2.2.5 Input Capacitor Selection

For the best output and input voltage filtering, X5R or X7R ceramic capacitors are recommended. The input bulk capacitor minimizes input voltage ripple, suppresses input voltage spikes, and provides a stable system rail for the device. A 10-µF or larger input capacitor is recommended. Having two in parallel further improves the input voltage ripple filtering, minimizing noise coupling into adjacent circuits. The voltage rating of the cap must also be taken into consideration, and must provide the required 5-µF minimum effective capacitance after DC bias derating.

In addition to the bulk input cap, a smaller cap must be placed directly from the VIN pin to the PGND pin to minimize input loop parasitic inductance, thereby minimizing the high frequency noise of the device. The input cap placement affects the output noise, so care needs to be taken in placing both the bulk cap and bypass caps as shown in *セクション 10.2*. 表 8-7 lists recommended input capacitors.

表 8-7. Recommended Input Capacitors

INPUT CAP TYPE	CAPACITOR VALUE	MANUFACTURER	VOLTAGE RATING (V)	PACKAGE SIZE
Bulk Cap	10 µF, X7S	TDK C2012X7S1E106K125AC	25	0805

表 8-7. Recommended Input Capacitors (continued)

INPUT CAP TYPE	CAPACITOR VALUE	MANUFACTURER	VOLTAGE RATING (V)	PACKAGE SIZE
Bypass Cap	2.2 nF, X7R	Murata GRM155R71E222KA01D	25	0402

8.2.2.2.6 Setting the Output Voltage

Choose resistors R1 and R2 to set the output voltage within a range of 0.8 V to 5.5 V, according to 式 8. To keep the feedback network robust from noise, and to reduce the self-generated noise of resistors, set R2 equal to or lower than 5 kΩ. Lower values of FB resistors achieve better noise immunity, and lower light load efficiency, as explained in the *Design Considerations for a Resistive Feedback Divider in a DC/DC Converter Technical Brief*.

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) = R2 \times \left(\frac{V_{OUT}}{0.8V} - 1 \right) \quad (8)$$

A feedforward capacitor (C_{FF}) is not required for proper operation, but can further improve output noise. However, care must be taken in choosing the C_{FF}, since the power good (PG) function may not be valid with a large C_{FF} during start-up, and can cause spurious triggering of the PG pin during a large load transient. The noise performance with various C_{FF} is shown in 図 6-31. Refer to the *Pros and Cons Using a Feedforward Capacitor with a Low Dropout Regulator Application Report* for a discussion of the pros and cons of using a feedforward capacitor.

8.2.2.2.7 NR/SS Capacitor Selection

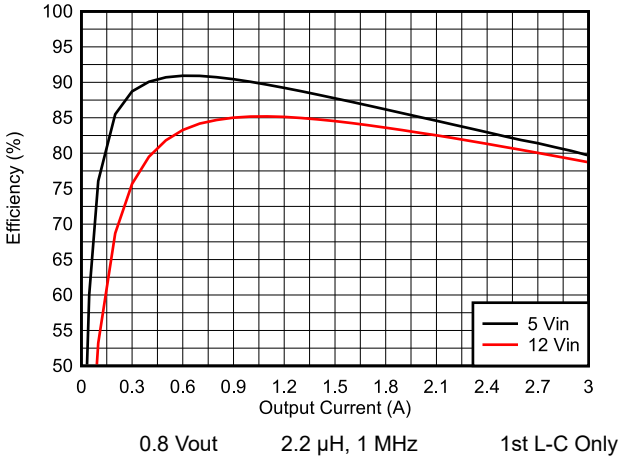
As described in *セクション 7.3.8*, the NR/SS cap affects both the total noise and the soft-start time. The recommended value for a 5-ms soft-start time and good noise performance is 470 nF. The maximum NR/SS cap is 3.3 µF for a start-up time of 35 ms. Values greater than 1 µF have minimal improvement in noise performance. Use 式 9 and 式 10 to calculate the soft-start time based on desired soft-start time or the chosen capacitor value.

$$t_{SS}(s) = \left(\frac{C_{NRSS} * 0.8}{I_{NRSS}} \right) \quad (9)$$

$$C_{NRSS}(F) = \frac{\left(I_{NRSS} \times t_{SS} \right)}{0.8} \quad (10)$$

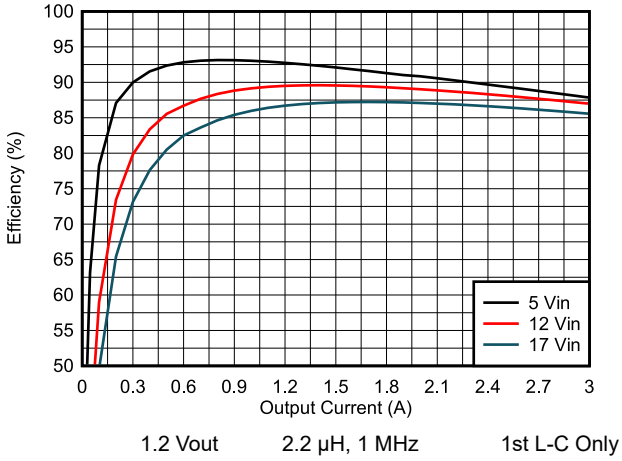
8.2.3 Application Curves

V_{IN}=12 V, V_{OUT}=1.2 V, T_A=25°C, BOM = 表 8-1, (unless otherwise noted)



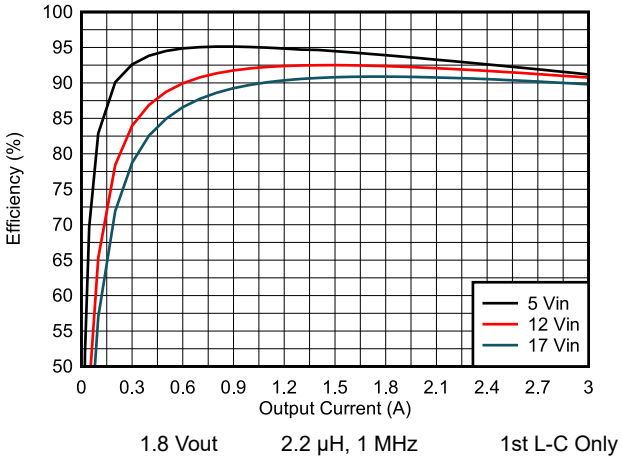
0.8 Vout 2.2 µH, 1 MHz 1st L-C Only

図 8-2. Efficiency vs Load Current



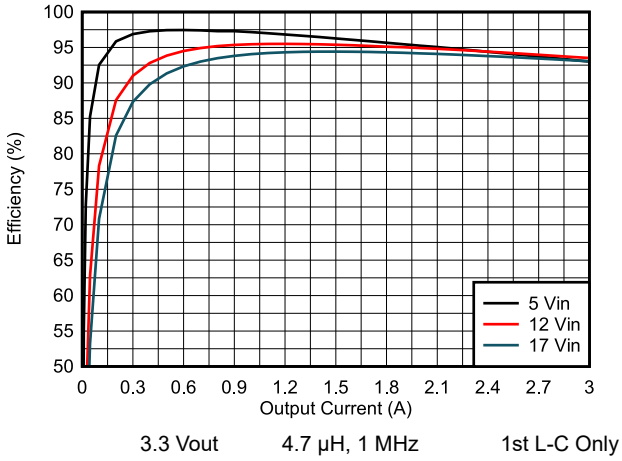
1.2 Vout 2.2 µH, 1 MHz 1st L-C Only

図 8-3. Efficiency vs Load Current



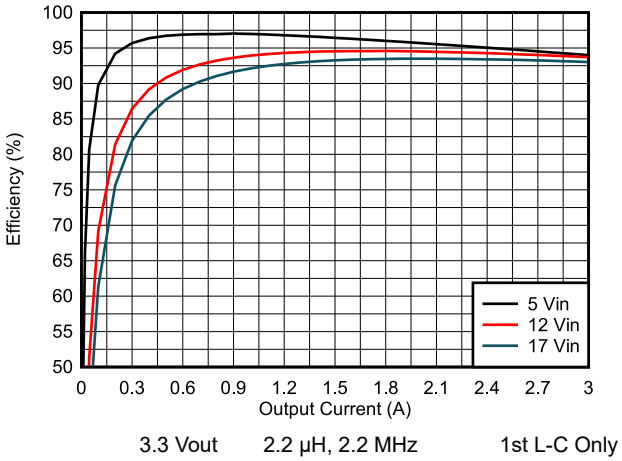
1.8 Vout 2.2 µH, 1 MHz 1st L-C Only

図 8-4. Efficiency vs Load Current



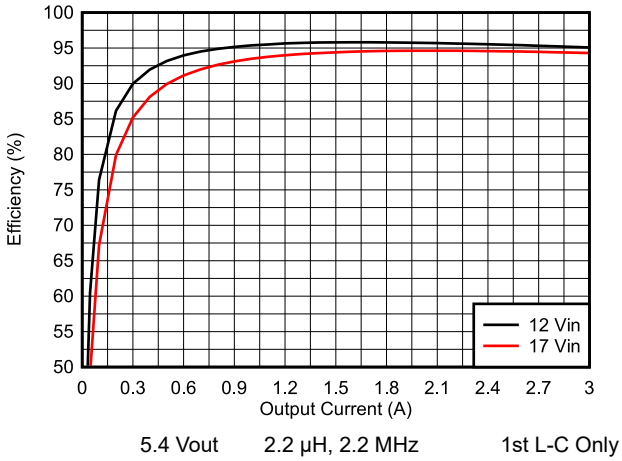
3.3 Vout 4.7 µH, 1 MHz 1st L-C Only

図 8-5. Efficiency vs Load Current



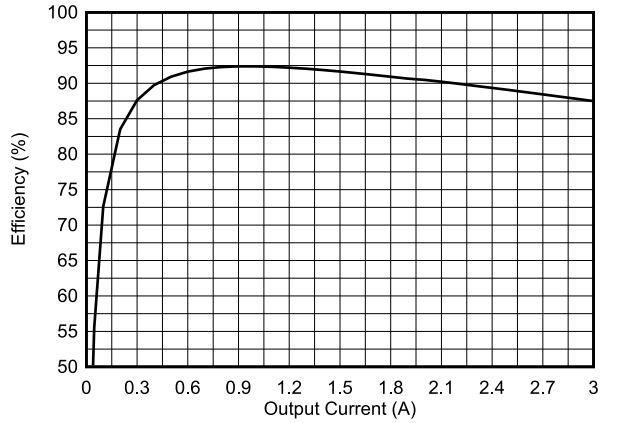
3.3 Vout 2.2 µH, 2.2 MHz 1st L-C Only

図 8-6. Efficiency vs Load Current



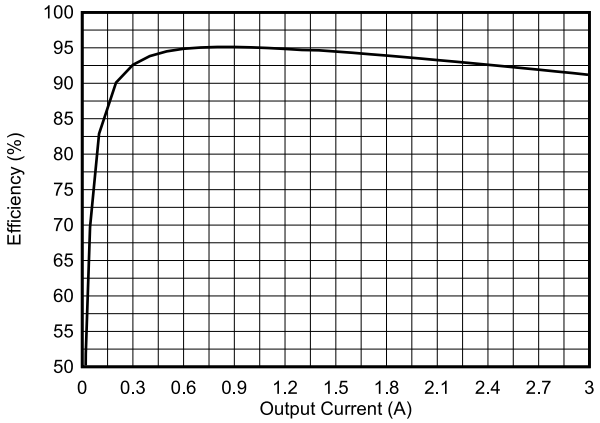
5.4 Vout 2.2 µH, 2.2 MHz 1st L-C Only

図 8-7. Efficiency vs Load Current



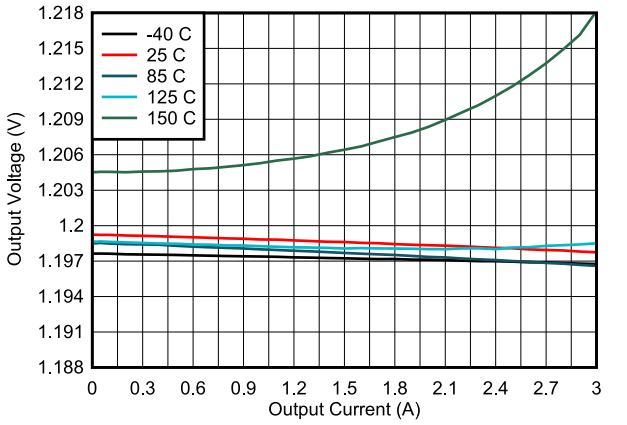
5 V to 1.2 V 2.2 µH, 2.2 MHz 1st L-C Only

図 8-8. Efficiency vs Load Current



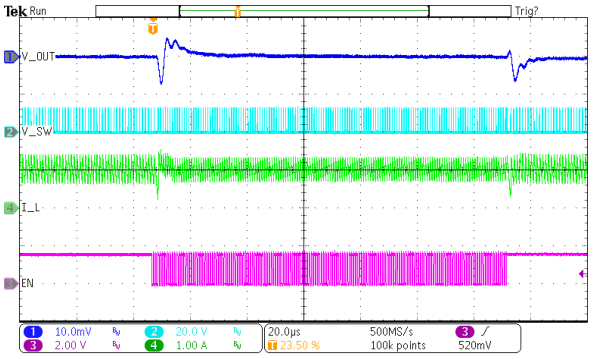
5 V to 1.8 V 2.2 µH, 2.2 MHz 1st L-C Only

図 8-9. Efficiency vs Load Current



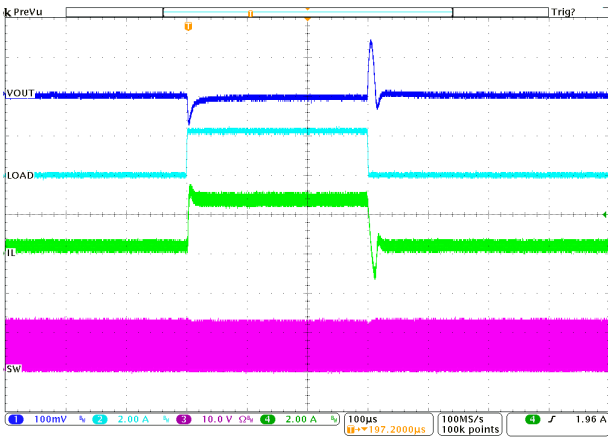
12 V to 1.2 V 2.2 µH, 1 MHz 1st L-C Only

図 8-10. Output Voltage vs Load Current



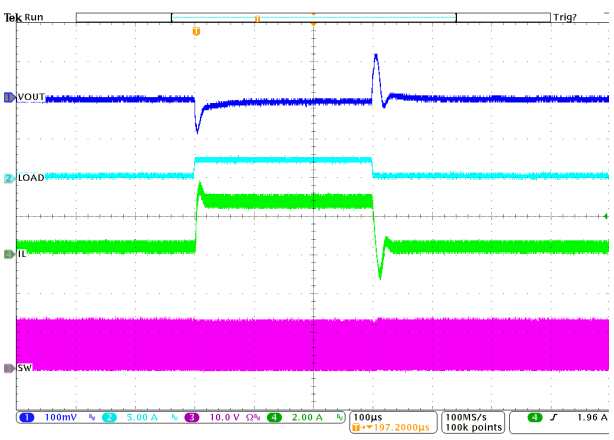
12 V to 1.2 V No load
2.2 µH, 1 MHz setting 1 MHz to 1.2 MHz to 1 MHz

図 8-11. Transition from Internal to External CLK



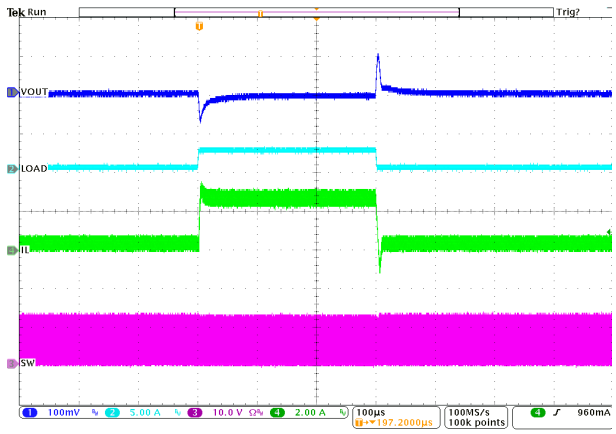
12 V to 1.2 V 2.2 µH, 1 MHz 1st L-C Only
300 mA to 2.7 A to 300 mA

図 8-12. Load Transient



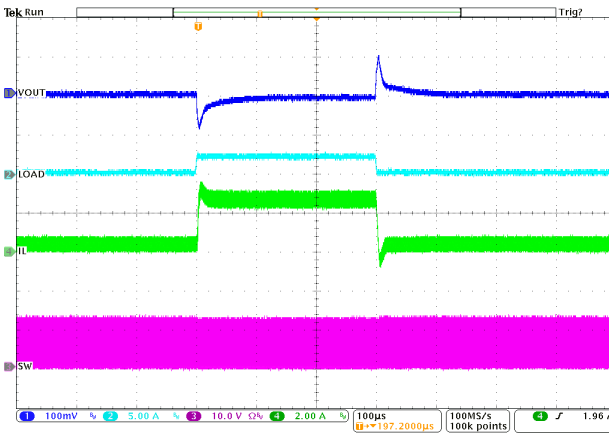
12 V to 1.2 V 2.2 µH, 1 MHz After 2nd L-C
300 mA to 2.7 A to 300 mA

図 8-13. Load Transient



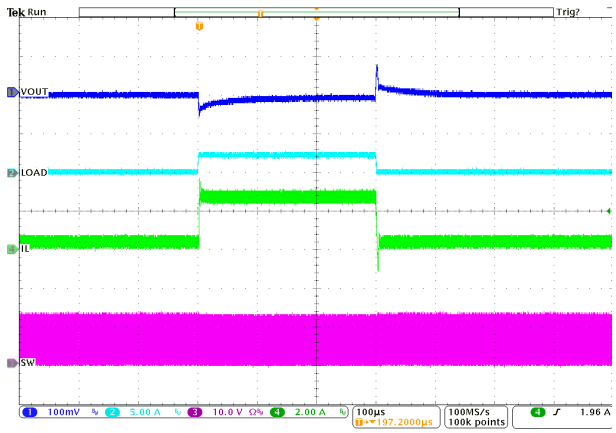
12 V to 1.8 V 2.2 µH, 1 MHz 1st L-C Only
300 mA to 2.7 A to 300 mA

図 8-14. Load Transient



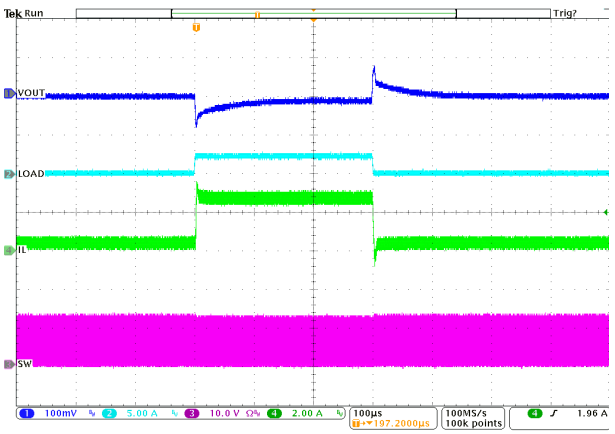
12 V to 1.8 V 2.2 µH, 1 MHz After 2nd L-C
300 mA to 2.7 A to 300 mA

図 8-15. Load Transient



12 V to 3.3 V 2.2 µH, 2.2 MHz 1st L-C Only
300 mA to 2.7 A to 300 mA

図 8-16. Load Transient



12 V to 3.3 V 2.2 µH, 2.2 MHz After 2nd L-C
300 mA to 2.7 A to 300 mA

図 8-17. Load Transient

9 Power Supply Recommendations

The power supply to the TPS6291x needs to have a current rating according to the supply voltage, output voltage, and output current of the TPS6291x.

10 Layout

10.1 Layout Guidelines

A proper layout is critical for the operation of any switched mode power supply, especially at high switching frequencies. Therefore, the PCB layout of the TPS6291x demands careful attention to ensure best performance. A poor layout can lead to issues like bad line and load regulation, instability, increased EMI radiation, and noise sensitivity. Refer to the *Five Steps to a Great PCB Layout for a Step-Down Converter Technical Brief* for a detailed discussion of general best practices. Specific recommendations for the device are listed below.

- The input capacitor or capacitors should be placed as close as possible to the VIN and PGND pins of the device. This is the most critical component placement. Route the input capacitors directly to the VIN and PGND pins avoiding vias.
- Place the inductor close to the SW pin. Minimize the copper area at the switch node.

- Place the output capacitor ground close to the PGND pin and route it directly avoiding vias. Minimize the length of the connection from the inductor to the output capacitor.
- Connect the VO pin directly to the first output capacitor, C_{OUT}.
- Sensitive traces, such as the connections to the NR/SS, VO, and FB pins need to be connected with short traces and be routed away from any noise source, such as the SW pin.
- Connect the PSNS pin directly to the system GND plane with a via.
- Place the second L-C filter, L_f and C_f, near the load to reduce any radiated coupling around the second L-C filter
- Avoid placing the ferrite bead in the keep out region as shown in 図 10-2
- Place the FB resistors, R1 and R2, close to the FB pin and route the VOUT connection from R1 to the load as a remote sense trace. If a second L-C filter is used, this connection should be made after L_f.
- The recommended layout is implemented on the EVM and shown in its User's Guide, *TPS6291xEVM-077 User's Guide*, as well as in 図 10-2.

10.2 Layout Example

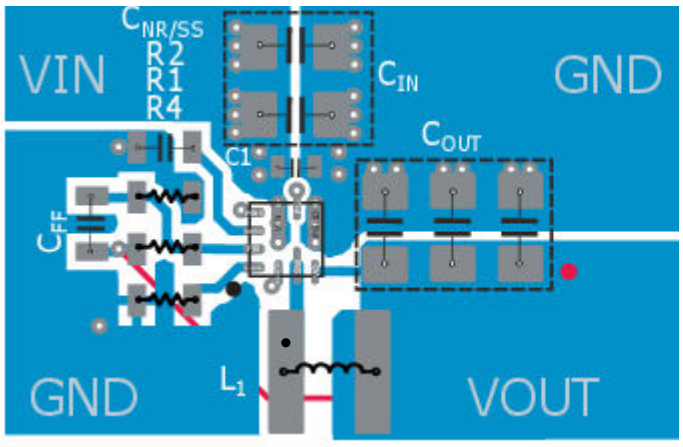


図 10-1. Recommended Layout for Single L-C Filter

注

The start winding of the inductor, as shown in the figures as a black dot, needs to be connected to the DC/DC converter switch pin, SW, to minimize capacitive coupling to the surrounding area.

注

The red dot indicates where the feedback sense should be placed for the best DC regulation. For a single L-C configuration, it is placed near the VOUT capacitors. For a second L-C filter design, the feedback sense is placed near the load after the VOUT_FILT capacitors.

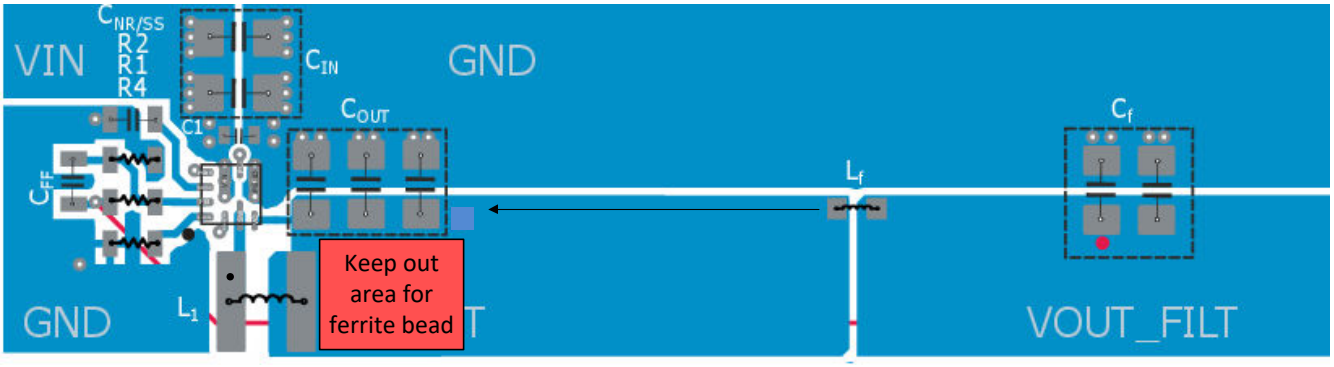


図 10-2. Recommended Layout for Design with Second L-C Filter

注

The ferrite bead can be placed closer to the device as long as it is outside the keep out area, as shown in the figure as a red rectangular area. This placement avoids capacitive and electromagnetic coupling to the output of the ferrite bead. If the ferrite bead is placed in the keep out area, the filtering effect of the ferrite bead is greatly reduced. If the ferrite bead is routed through a via to the back side of the board, ensure adequate ground plane between the layers if the ferrite bead will be in this area.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Development Support

11.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS6291x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost.
3. Open the advanced tab to optimize for output voltage ripple.
4. Once in a TPS6291x design, you can enable the second stage L-C filter and change other settings from the drop-down on the left.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 用語集

TI 用語集　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62912RPUR	ACTIVE	VQFN-HR	RPU	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	26PH	Samples
TPS62913RPUR	ACTIVE	VQFN-HR	RPU	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	26QH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

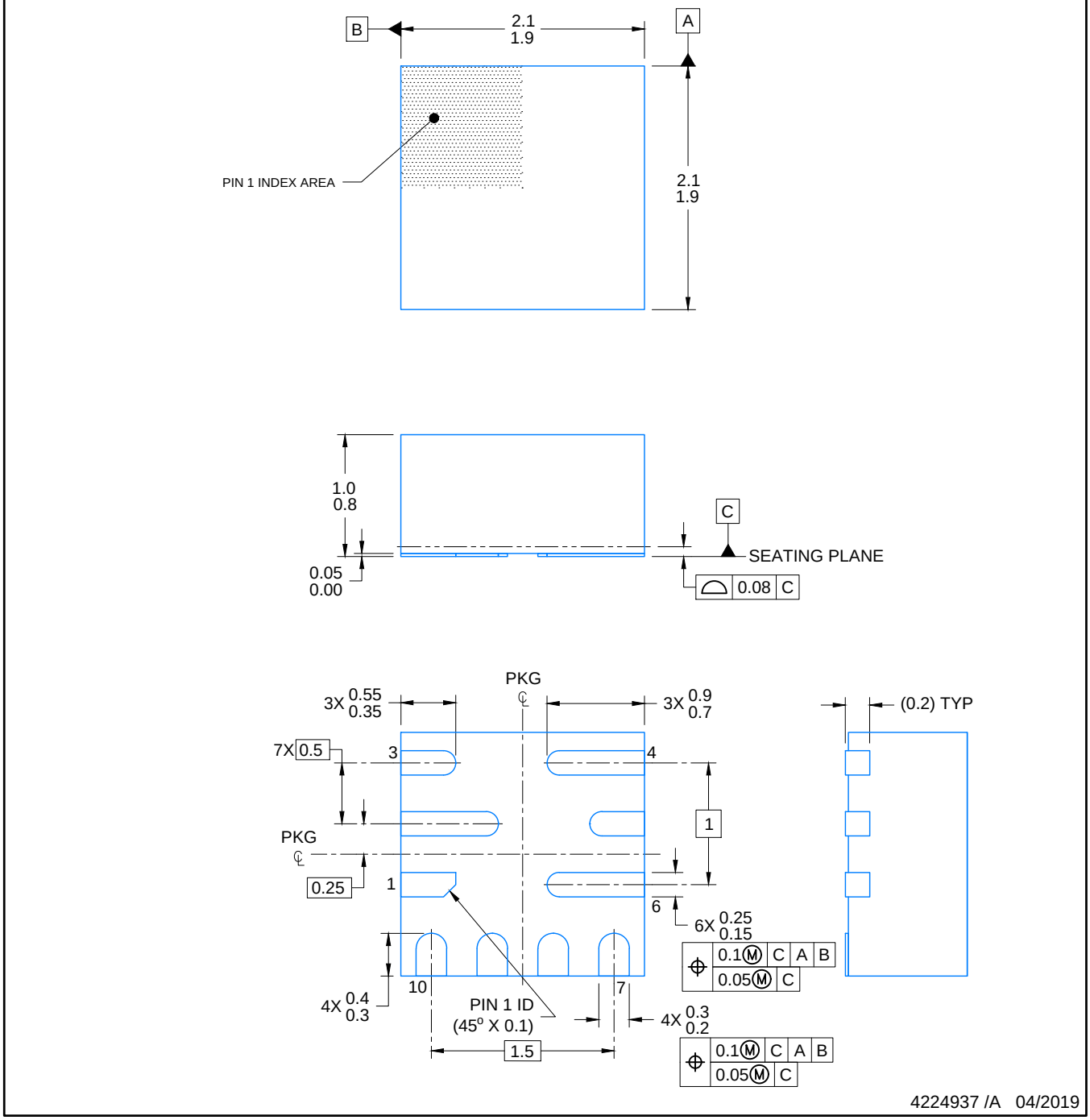
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

RPU0010A

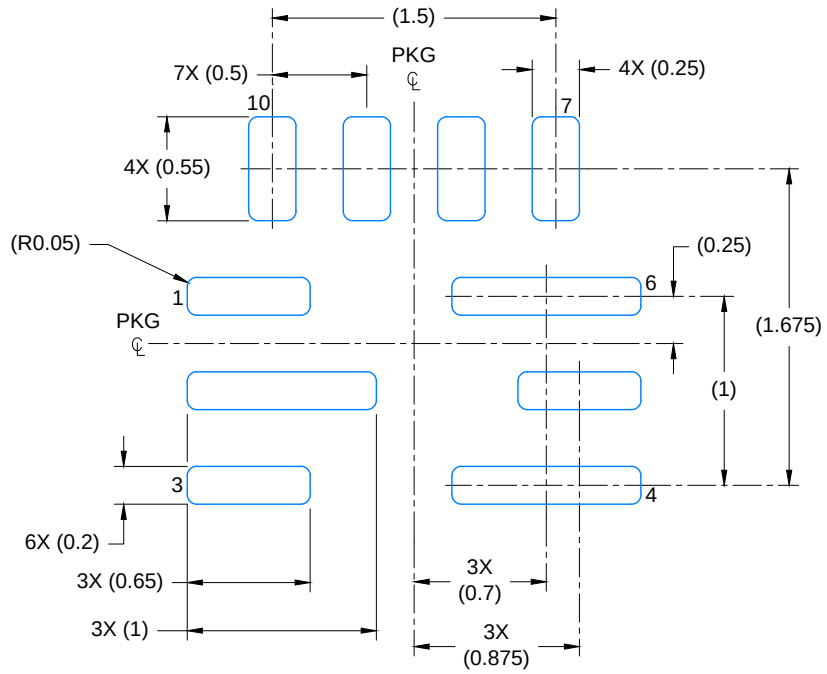
VQFN-HR - 1 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

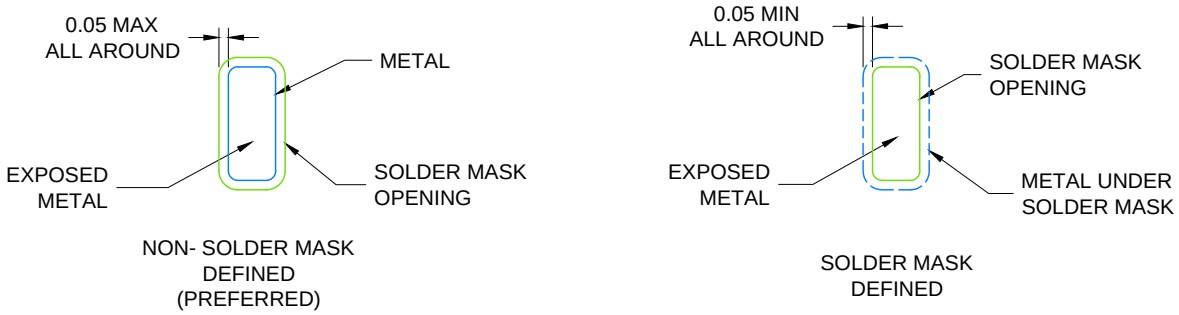


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

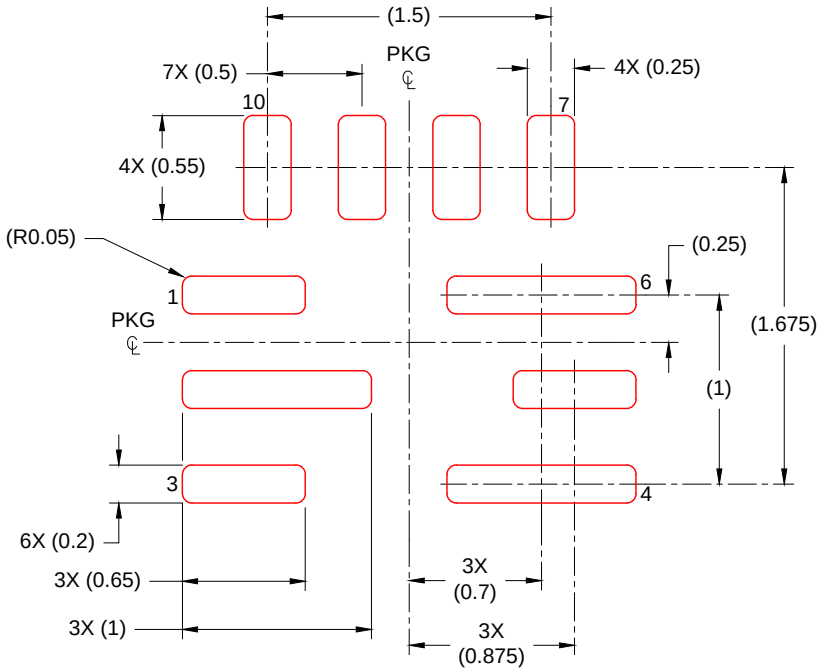


SOLDER MASK DETAILS
NOT TO SCALE

4224937 /A 04/2019

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL
SCALE: 25X

4224937 /A 04/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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