TEXAS INSTRUMENTS
TPS62A06, TPS62A06A
JAJSNR8A – APRIL 2023 – REVISED JUNE 2023

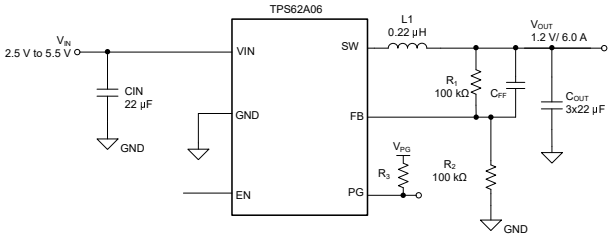
TPS62A06x SOT563 パッケージの 6A 高効率同期整流降圧コンバータ

1 特長

- 入力電圧範囲:2.5V～5.5V
- 可変出力電圧範囲:0.6V～V_{IN}
- 15mΩ/10mΩ 低 R_{DSON} スイッチ (6A)
- 静止電流:25μA
- タイミング精度:1% (0°C～125°C)
- 100% モード動作
- 2.2MHz のスイッチング周波数
- パワー・セーブ・モードまたは FPWM オプションが利用可能
- パワー・グッド出力ピン
- 短絡保護 (HICCUP)
- ソフト・スタートアップを内蔵
- 出力放電
- サーマル・シャットダウン保護機能
- 1.6mm × 1.6mm の SOT563 パッケージで供給
- TLV62585 とピン互換

2 アプリケーション

- 多機能プリンタ
- セットトップ・ボックス
- TV アプリケーション
- IP ネットワーク・カメラ
- ワイヤレス・ルータ、ソリッドステート・ドライブ
- バッテリ駆動アプリケーション
- 汎用 POL (ポイント・オブ・ロード) 電源



代表的なアプリケーション

3 概要

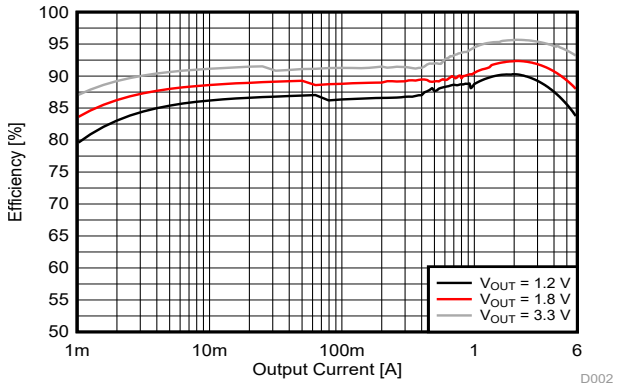
TPS62A06 デバイス・ファミリは同期整流降圧型 DC/DC コンバータで、高効率と小型のソリューション向けに最適化されています。このデバイスは最大 6A の出力電流を供給できるスイッチを内蔵しています。中～高負荷時には、スイッチング周波数 2.2MHz のパルス幅変調 (PWM) で動作します。軽負荷時には、デバイスは自動的にパワー・セーブ・モード (PSM) へ移行し、負荷電流範囲の全体にわたって高い効率を維持します。このデバイス・ファミリの TPS62A06A のバリアントでは、負荷電流範囲全体にわたって強制 PWM で動作します。

TPS62A06 は、外付けの分圧抵抗によって出力電圧を変更できます。内部のソフト・スタート回路により、スタートアップ時の突入電流が制限されます。過電流保護、サーマル・シャットダウン保護、パワー・グッドなど、その他の機能も備えています。本デバイスは SOT563 パッケージで供給されます。

製品情報

部品番号	モード	パッケージ (1)	本体サイズ (公称)
TPS62A06	PSM、PWM	DRL (SOT563、6)	1.60mm x 1.60mm
TPS62A06A	FPWM		

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



$5V_{IN}$ での出力電流と効率の関係

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (April 2023) to Revision A (June 2023)	Page
• ドキュメントのステータスを「事前情報」から「量産データ」に変更	1

5 Device Comparison Table

DEVICE NUMBER	OUTPUT CURRENT	OPERATION MODE
TPS62A06	6 A	PSM/ PWM
TPS62A06A	6 A	FPWM

6 Pin Configuration and Functions

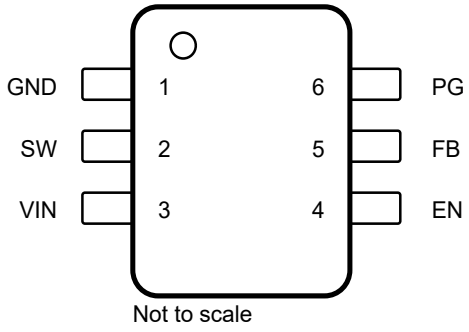


図 6-1. 6-Pin DRL SOT563 Package (Top View)

表 6-1. Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
EN	4	I	Device enable logic input. Logic high enables the device, logic low disables the device and turns the device into shutdown. Do not leave the pin floating.
FB	5	I	Feedback pin for the internal control loop. Connect this pin to an external feedback divider.
GND	1	G	Ground pin
PG	6	O	Power-good open-drain output pin. The pullup resistor cannot be connected to any voltage higher than 5.5 V. If unused, leave the pin open or connect to GND.
SW	2	O	Switch pin connected to the internal FET switches and inductor terminal. Connect the inductor of the output filter to this pin.
VIN	3	I	Power supply voltage pin

(1) I = Input, O = Output, G = Ground

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Pin voltage(2)	VIN, EN, PG	–0.3	6	V
	SW, DC	–0.3	V_{IN} + 0.3	V
	SW, transient < 10 ns	–3.0	10	V
	FB	–0.3	3	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range		2.5		5.5	V
V_{OUT}	Output voltage range		0.6		V_{IN}	V
L	Effective inductance			0.22		µH
C_{OUT}	Effective output capacitance	V_{OUT} < 1.2 V		120		µF
C_{OUT}	Effective output capacitance	1.2 V <= V_{OUT} < 1.8 V		45		µF
C_{OUT}	Effective output capacitance	V_{OUT} => 1.8 V		45		µF
I_{OUT}	Output current range	TPS62A06	0		6	A
I_{PG}	Power Good input current capability		0		1	mA
T_J	Operating junction temperature		–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS62A06x DRL 6 PINS	TPS62A06EVM-248 EVM 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	137.5	74.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.2	-	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.0	-	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.6	33.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

T_J = –40°C to +125°C, V_{IN} = 2.5 V to 5.5 V. Typical values are at T_J = 25°C and V_{IN} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$I_{Q(VIN)}$	VIN quiescent current	Non-switching, V_{EN} = High, V_{FB} = 610 mV		26		µA
$I_{SD(VIN)}$	VIN shutdown supply current	T_J = –40°C to 85°C, V_{EN} = Low		0.01	4	µA
UVLO						
$V_{UVLO(R)}$	VIN UVLO rising threshold	V_{IN} rising	2.3	2.4	2.5	V
$V_{UVLO(F)}$	VIN UVLO falling threshold	V_{IN} falling	2.2	2.3	2.4	V
ENABLE						
$V_{EN(R)}$	EN voltage rising threshold	EN rising, enable switching	1.2			V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching			0.4	V
$V_{EN(LKG)}$	EN Input leakage current	V_{EN} = 5 V			100	nA
REFERENCE VOLTAGE						
V_{FB}	FB voltage	T_J = 0°C to 125°C, PWM mode	594	600	606	mV
V_{FB}	FB voltage	PWM mode	591	600	609	mV
$I_{FB(LKG)}$	FB input leakage current	V_{FB} = 0.6 V			100	nA
SWITCHING FREQUENCY						
$f_{SW(FCCM)}$	Switching frequency, FPWM operation	V_{IN} = 5 V, V_{OUT} = 1.8 V		2200		kHz
STARTUP						
	Internal fixed soft-start time	From EN = High to V_{FB} = 0.56 V		0.5	1	ms
POWER STAGE						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	TPS62A06, V_{IN} = 5 V		15		mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	TPS62A06, V_{IN} = 5 V		10		mΩ
OVERCURRENT PROTECTION						
$I_{HS(OC)}$	High-side peak current limit	TPS62A06	8.2	10		A
$I_{LS(OC)}$	Low-side valley current limit	TPS62A06		9.1		A
POWER GOOD						
V_{PGTH}	Power Good threshold	PG low, FB falling		93.5		%
V_{PGTH}	Power Good threshold	PG high, FB rising		96		%
	PG delay falling			30		µs
	PG delay rising			10		µs
$I_{PG(LKG)}$	PG pin Leakage current when open drain output is high	V_{PG} = 5 V			100	nA
	PG pin output low-level voltage	I_{PG} = 1 mA			400	mV
OUTPUT DISCHARGE						
	Output discharge current on SW pin	V_{IN} = 3 V, V_{OUT} = 2.0 V		150		mA
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold	Temperature rising		170		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis			20		°C

7.6 Typical Characteristics

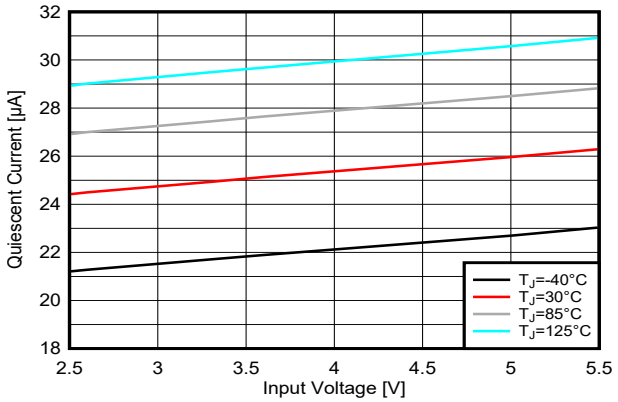


図 7-1. Quiescent Current vs Input Voltage

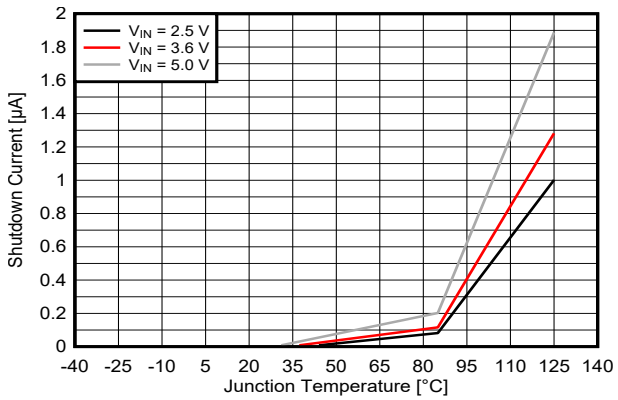


図 7-2. Shutdown Current vs Junction Temperature

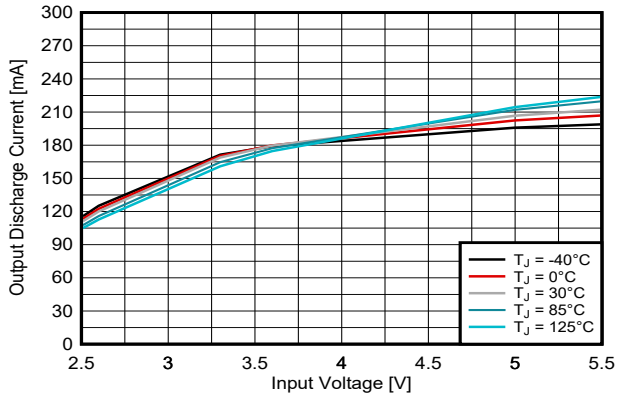


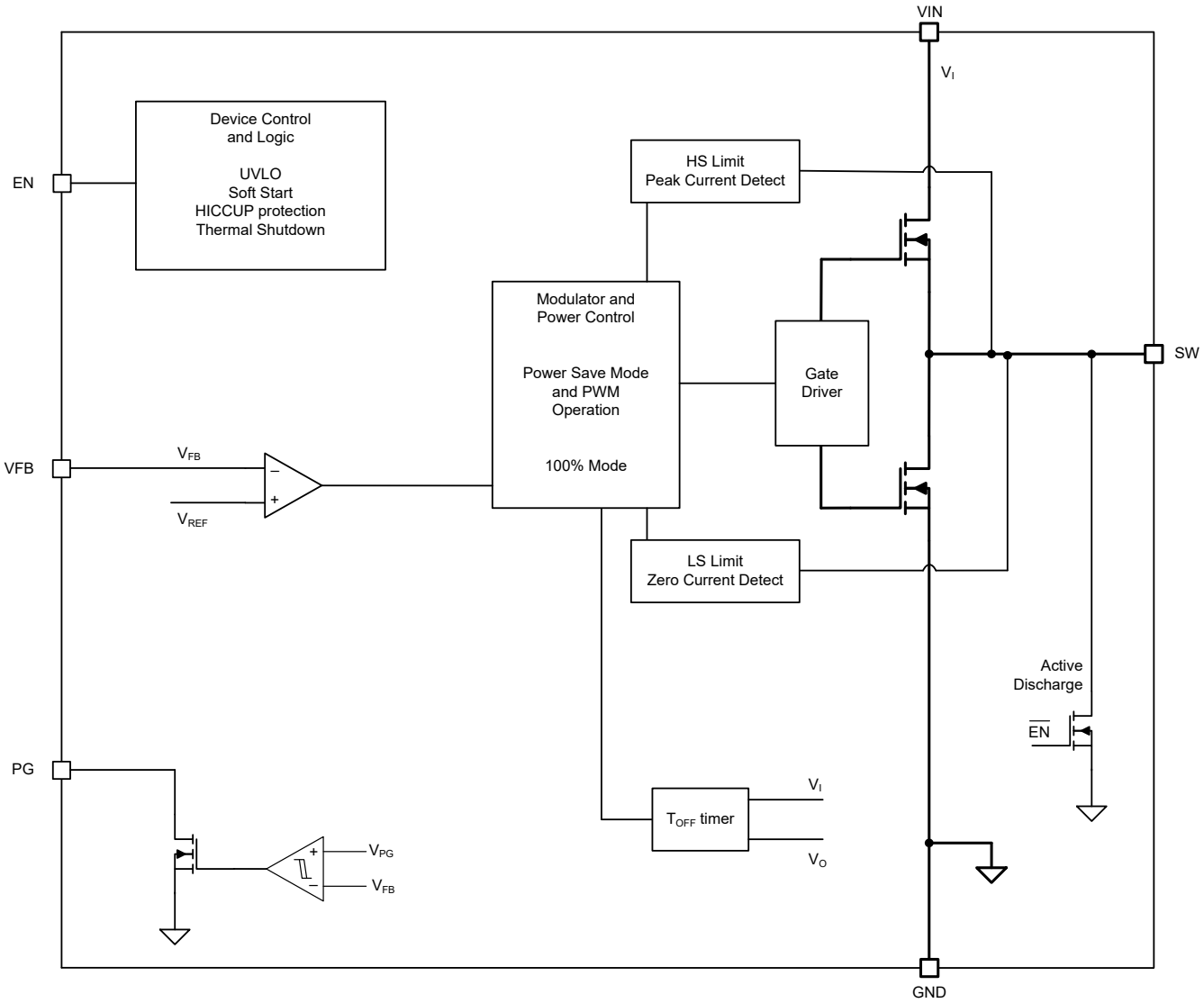
図 7-3. Output Discharge Current vs Input Voltage

8 Detailed Description

8.1 Overview

The TPS62A0x is a high-efficiency, synchronous step-down converter. The device operates with an adaptive off time with a peak current control scheme. The device operates typically at 2.2-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. Based on the V_{IN}/V_{OUT} ratio, a simple circuit sets the required off time for the low-side MOSFET. This action makes the switching frequency relatively constant regardless of the variation of the input voltage, output voltage, and load current.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power Save Mode

The device automatically enters power save mode to improve efficiency at light load when the inductor current becomes discontinuous. In power save mode, the converter reduces the switching frequency and minimizes current consumption. In power save mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor or adding a feedforward capacitor.

8.3.2 100% Duty Cycle Low Dropout Operation

The device offers low input-to-output voltage difference by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. The minimum input voltage to maintain output regulation, depending on the load current and output voltage, is calculated as:

$$V_{IN(MIN)} = V_{OUT} + I_{OUT} \times R_{DS(ON)} + R_L \quad (1)$$

where

- $R_{DS(ON)}$ = High-side FET on-resistance
- R_L = Inductor ohmic resistance (DCR)

8.3.3 Soft Start

After enabling the device, internal soft start-up circuitry ramps up the output voltage, which reaches the nominal output voltage during start-up time, avoiding excessive inrush current and creating a smooth output voltage rise slope. soft start-up circuitry also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

The TPS62A0x is able to start into a pre-biased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to its nominal value.

8.3.4 Switch Current Limit and Short-Circuit Protection (HICCUP)

The switch current limit prevents the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current can occur with a shorted or saturated inductor or an overload or shorted output circuit condition. If the inductor current reaches the threshold I_{LIM}, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current with an adaptive off time.

When this switch current limit is triggered 32 times, the device reduces the current limit for further 32 cycles and then stops switching to protect the output. The device then automatically starts a new start-up after a typical delay time of 500 µs has passed. This action is named HICCUP short-circuit protection. The device repeats this mode until the high load condition disappears. HICCUP protection is also enabled during the start-up.

8.3.5 Undervoltage Lockout

To avoid misoperation of the device at low input voltages, an undervoltage lockout (UVLO) is implemented, which shuts down the device at voltages lower than V_{UVLO} with a hysteresis of 130 mV.

8.3.6 Thermal Shutdown

The device goes into thermal shutdown and stops switching when the junction temperature exceeds T_{JSD}. When the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically.

8.4 Device Functional Modes

8.4.1 Enable and Disable

The device is enabled by setting the EN input to a logic High. Accordingly, a logic Low disables the device. If the device is enabled, the internal power stage starts switching and regulates the output voltage to the set point voltage. The EN input must be terminated and must not be left floating.

8.4.2 Power Good

The TPS62A06x has a built-in power-good (PG) feature to indicate whether the output voltage has reached its target and the device is ready. The PG signal can be used for start-up sequencing of multiple rails. The PG pin is an open-drain output that requires a pullup resistor to any voltage up to the recommended input voltage level. PG is low when the device is turned off due to EN, UVLO (undervoltage lockout), or thermal shutdown. VIN must remain present for the PG pin to stay low.

If the power-good output is not used, TI recommends to tie to GND or leave open.

表 8-1. Power-Good indicator Functional Table

LOGIC SIGNALS				PG STATUS
V_I	EN PIN	THERMAL SHUTDOWN	V_O	
V_I > UVLO	HIGH	NO	V_O on target	High Impedance
			V_O < target	LOW
			YES	LOW
		YES	x	LOW
	UVLO < V_I < 1.8 V	x	x	LOW
V_I < 1.8 V	x	x	x	Undefined

The PG indicator features a de-glitch to avoid the signal indicating glitches or transient responses from the loop sketch the behavior.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

9.2 Typical Application

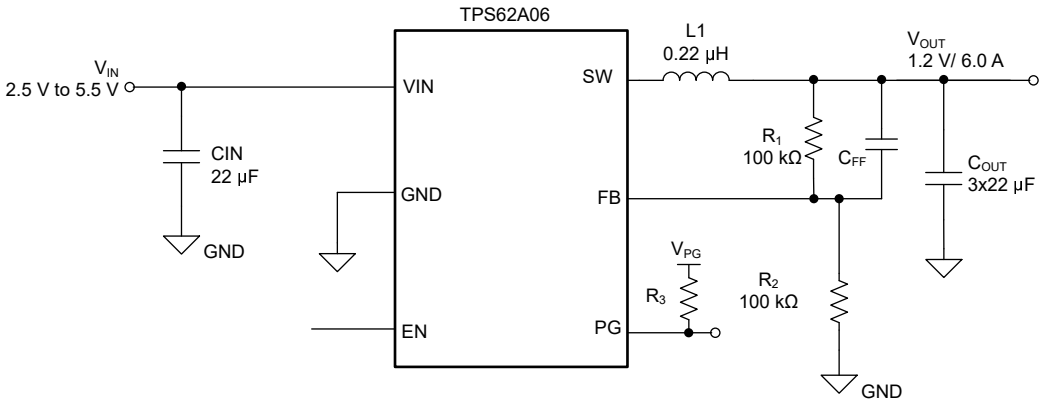


図 9-1. TPS62A06 Typical Application Circuit

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 9-1 as the input parameters

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.5 V to 5.5 V
Output voltage	1.2 V
Maximum output current	6.0 A

表 9-2 lists the components used for the example.

表 9-2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER(1)
C1	22 µF, Ceramic Capacitor, 10 V, X7R, size 0805, GRM21BZ71A226KE15L	Murata
C2, C3, C4	22 µF, Ceramic Capacitor, 10 V, X7R, size 0805, GRM21BZ71A226KE15L	Murata
L1	0.22 µH, Power Inductor, XGL4015-221MEC	Coilcraft
R1, R2	Chip resistor, 1%, size 0603	Std.
C5	Optional, 120 pF if needed	Std.

(1) See the *Third-Party Products Disclaimer*.

9.2.2 Detailed Design Procedure

9.2.2.1 Setting the Output Voltage

The output voltage is set by an external resistor divider according to 式 2. To keep the feedback (FB) net robust from noise, set R2 equal to or lower than 100 kΩ to have at least 6 µA of current in the voltage divider. Lower values of FB resistors achieve better noise immunity, and lower light load efficiency, as explained in the *Design Considerations for a Resistive Feedback Divider in a DC/DC Converter technical brief*.

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R2 \times \left(\frac{V_{OUT}}{0.6\,V} - 1\right) \quad (2)$$

9.2.2.2 Feedforward Capacitor

TI recommends a feedforward capacitor C_{FF} in parallel with R_1 to improve the load transient performance and reduce the output ripple voltage in PSM. The recommended value for C_{FF} is 120 pF.

9.2.2.3 Output Filter Design

The inductor and output capacitor together provide a low-pass filter. To simplify this process, 表 9-3 outlines possible inductor and capacitor value combinations. Checked cells represent combinations that are proven for stability by simulation and lab test. Check further combinations for each individual application.

表 9-3. Matrix of Output Capacitor and Inductor Combinations

V_{OUT} [V]	L [µH](1)	C_{OUT} [µF](2)		
		3 × 22	2 × 47	3 × 47
0.6 ≤ V_{OUT} < 1.2	0.22		++(3)	++
1.2 ≤ V_{OUT} < 1.8	0.22	++(3)	+	+
1.8 ≤ V_{OUT}	0.22	++(3)	+	+

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and –30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by +20% and –50%.
(3) This LC combination is the standard value and recommended for most applications.

9.2.2.4 Input and Output Capacitor Selection

The architecture of the TPS62A0x allows use of tiny ceramic-type output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are thus recommended. To keep resistance up to high frequencies and to achieve narrow capacitance variation with temperature, TI recommends to use X7R or X5R dielectric.

The input capacitor is the low impedance energy source for the converter that helps provide stable operation. TI recommends a low-ESR multilayer ceramic capacitor for best filtering. For most applications, a 10-µF input capacitor is sufficient; a larger value reduces input voltage ripple.

The recommended typical output capacitor value for 1.2-V output typical application is 45 µF of effective capacitance. This capacitance can vary over a wide range, as outlined in 表 9-3.

9.2.3 Application Curves

V_{IN} = 5.0 V, V_{OUT} = 1.2 V, T_A = 25°C, BOM = 表 9-2 unless otherwise noted.

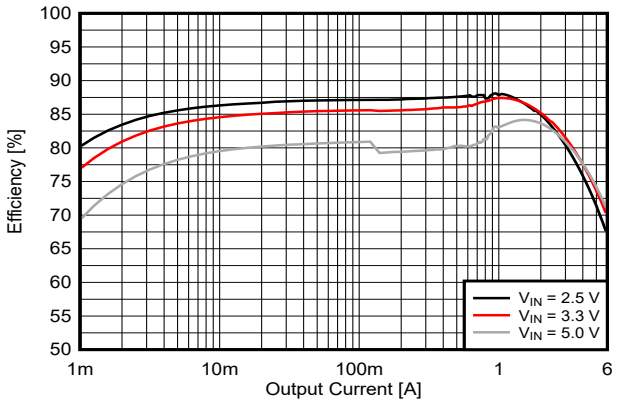


図 9-2. 0.6-V Output Efficiency (TPS62A06)

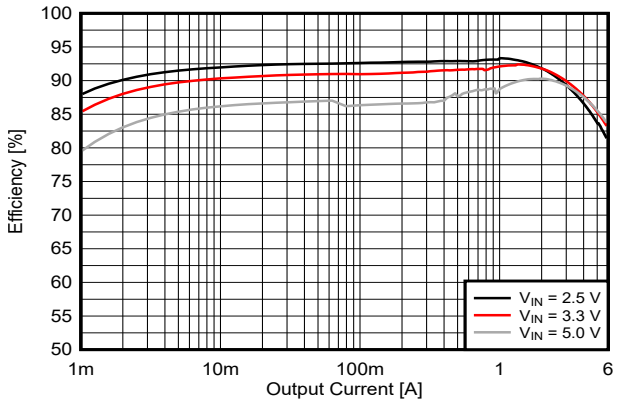


図 9-3. 1.2-V Output Efficiency (TPS62A06)

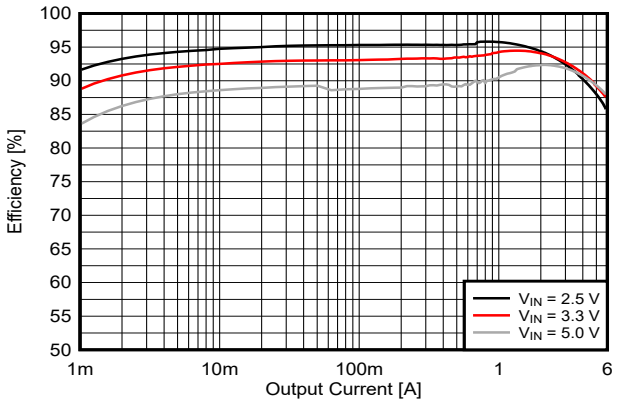


図 9-4. 1.8-V Output Efficiency (TPS62A06)

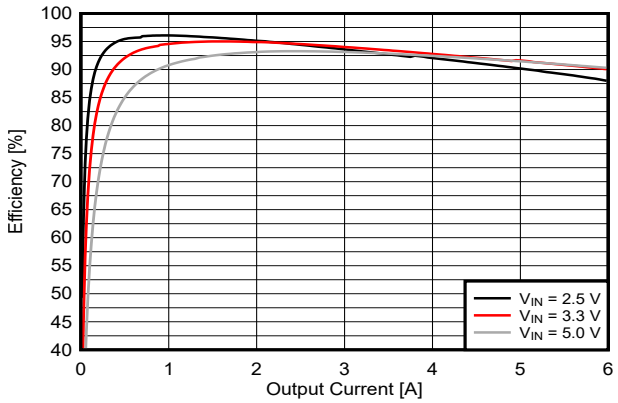
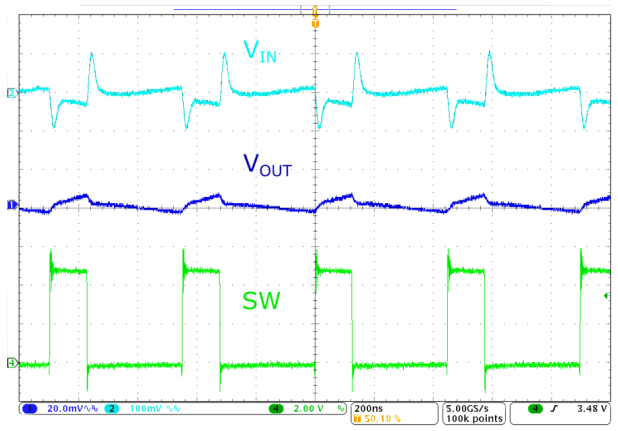
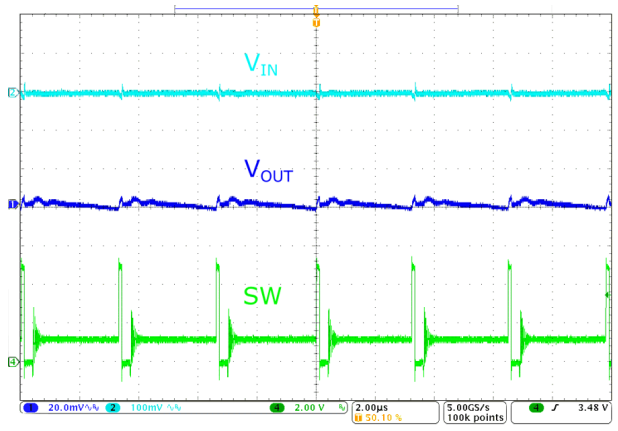


図 9-5. 1.8-V Output Efficiency (TPS62A06A)



Load Current = 6 A

図 9-6. PWM Operation (TPS62A06)



Load Current = 100 mA

図 9-7. PFM Operation (TPS62A06)

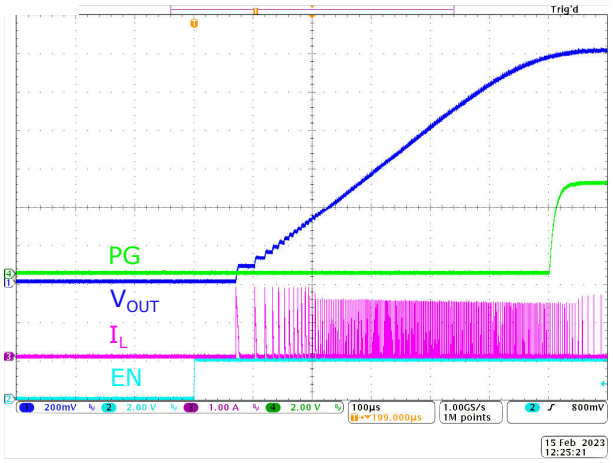


図 9-8. Start-Up With No Load (TPS62A06)

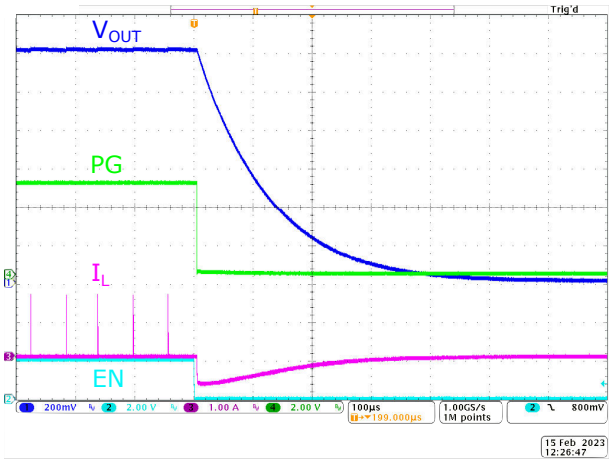
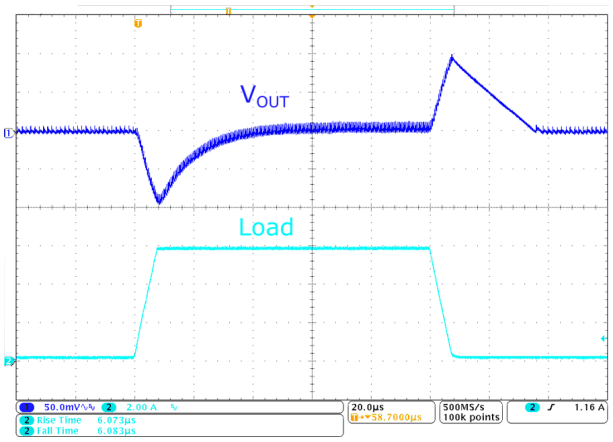
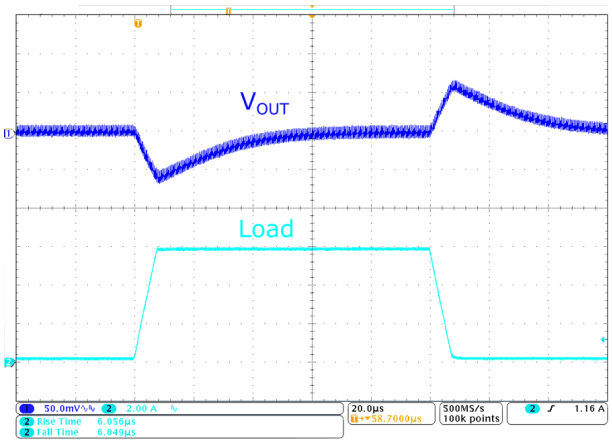


図 9-9. Shutdown With No Load (TPS62A06)



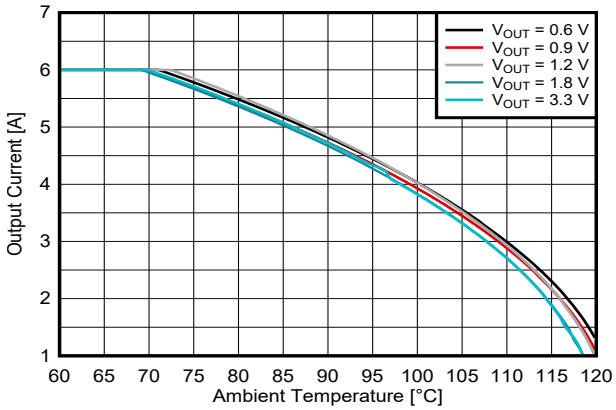
Load Step: 0.1 A to 6 A, 1 A/µs

図 9-10. Load Transient Response (TPS62A06)



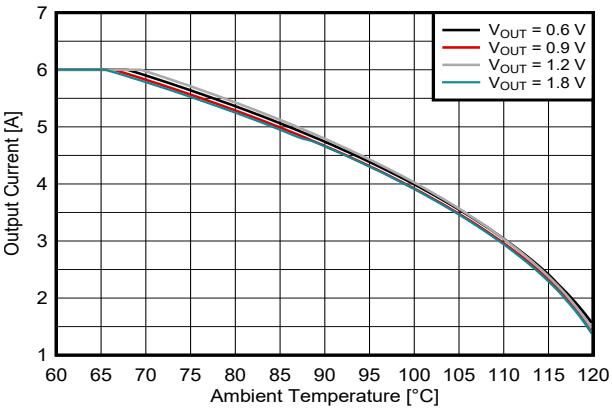
Load Step: 0.1 A to 6 A, 1 A/µs

図 9-11. Load Transient Response (TPS62A06A)



$R_{\theta JA}$ = 74.5°C/W T_{Jmax} = 125°C

図 9-12. Safe Operating Area Based On EVM, V_{IN} = 5.0 V, TPS62A06DRL



$R_{\theta JA}$ = 74.5°C/W T_{Jmax} = 125°C

図 9-13. Safe Operating Area Based On EVM, V_{IN} = 3.3 V, TPS62A06DRL

9.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.5 V to 5.5 V. Ensure that the input power supply has a sufficient current rating for the application.

9.4 Layout

9.4.1 Layout Guidelines

The printed-circuit-board (PCB) layout is an important step to maintain the high performance of the TPS62A0x device.

- Place the input and output capacitors and the inductor as close as possible to the IC. This action keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- Connect the low side of the input and output capacitors properly to the GND pin to avoid a ground potential shift.
- Take special care to avoid noise being induced. The sense traces connected to FB is a signal trace. Keep these traces away from SW nodes.
- Use common ground. GND layers can be used for shielding.

See 図 9-14 for the recommended PCB layout.

9.4.2 Layout Example

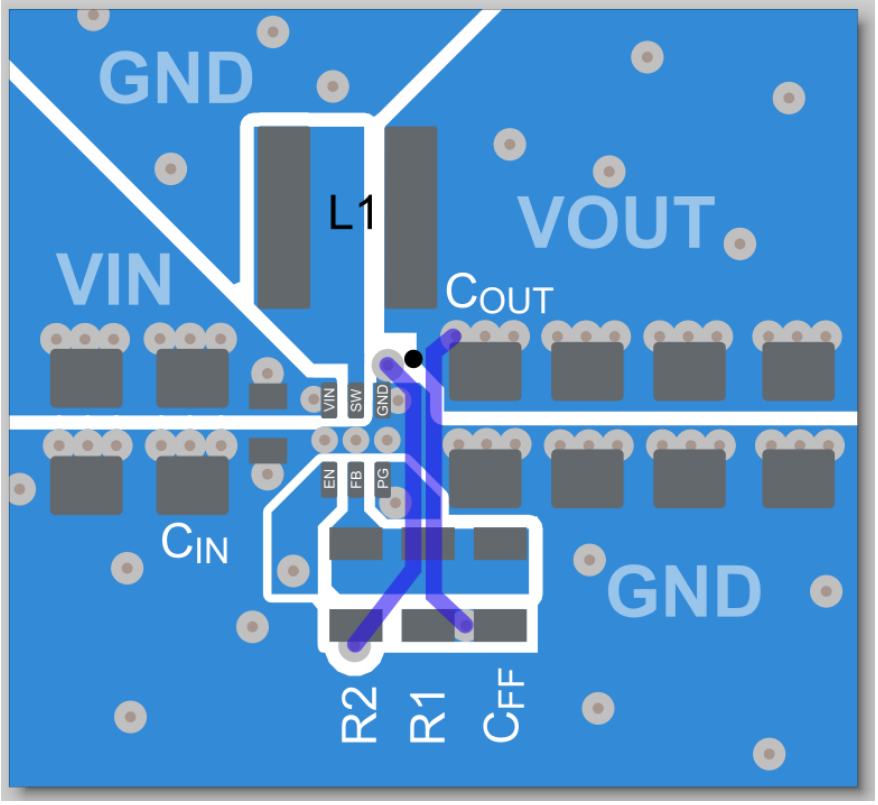


図 9-14. TPS62A06x PCB Layout Recommendation

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Device Support

10.1.1 サード・パーティ製品に関する免責事項

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10.2 Documentation Support

10.2.1 Related Documentation

Texas Instruments, *Design Considerations for a Resistive Feedback Divider in a DC/DC Converter* technical brief

10.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.4 サポート・リソース

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10.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

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10.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62A06ADRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	1MH	Samples
TPS62A06DRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	1MG	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

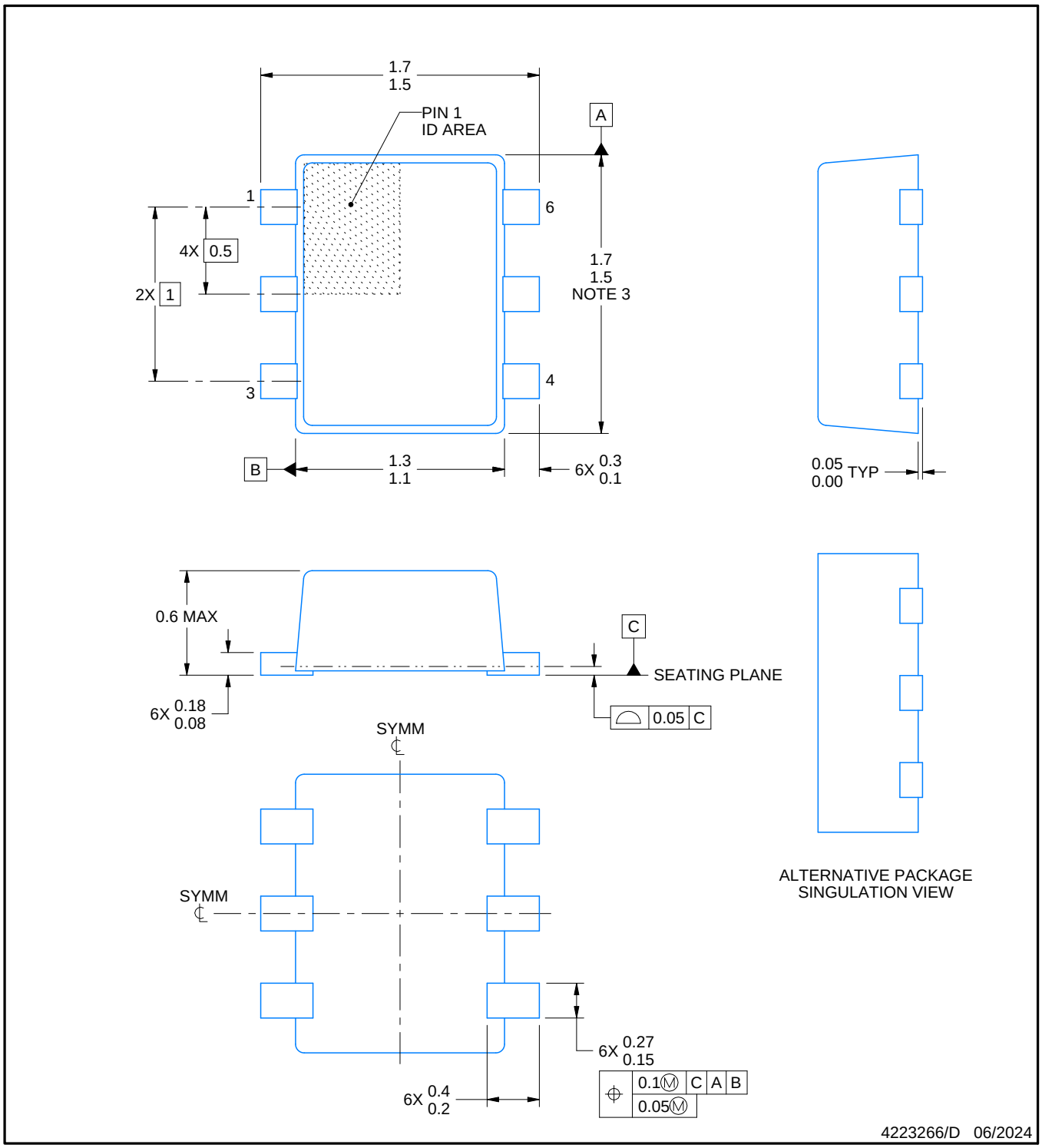
(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



NOTES:

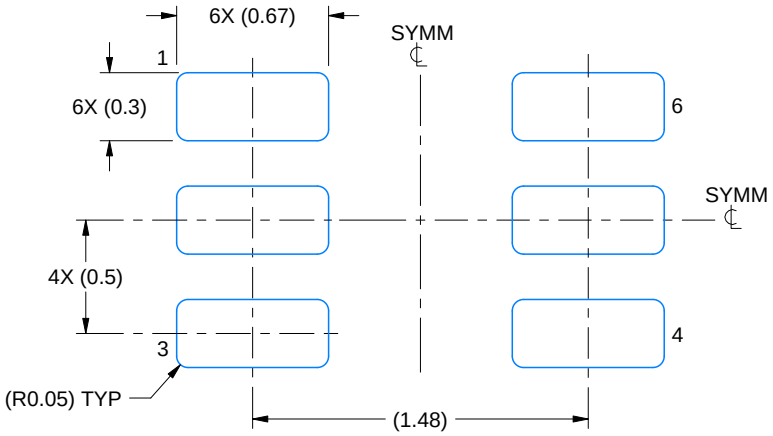
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

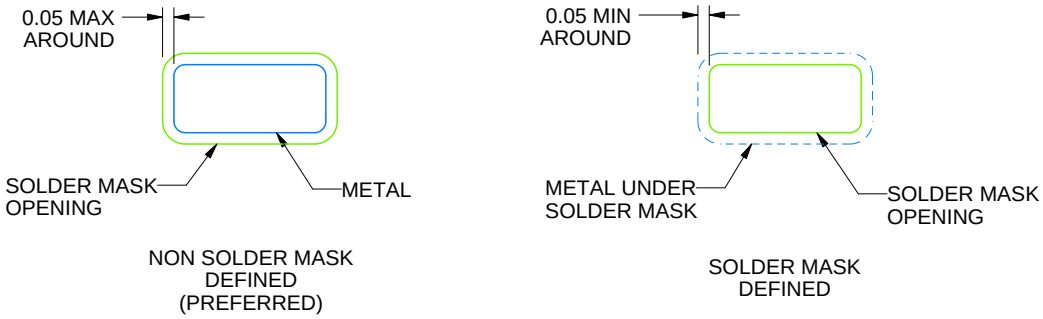
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

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NOTES: (continued)

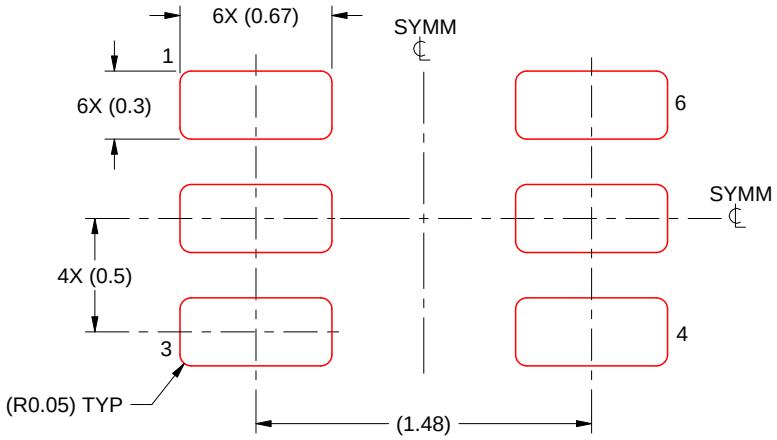
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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