TEXAS INSTRUMENTS
TPS63805, TPS63806, TPS63807
JAJSFP7E – JULY 2018 – REVISED AUGUST 2021

TPS6380x 小ソリューション・サイズの高効率、低 I_Q 昇降圧コンバータ

1 特長

- 3 つのピン互換デバイス・オプション：特定のアプリケーションに重点を置いた TPS63805、TPS63806、TPS63807
- 入力電圧範囲：1.3V～5.5V
  - デバイスのスタートアップ時入力電圧は 1.8V を超えること
- 出力電圧範囲：1.8V～5.2V (可変)
- 全負荷範囲にわたって高効率を実現
  - パワーセーブ・モードと強制 PWM モードのモード選択
- ピーク電流昇降圧モード・アーキテクチャ
  - 降圧、昇降圧、昇圧動作モード間の遷移点を定義済み
  - 順方向および逆方向電流動作
  - あらかじめ出力にバイアスを印加した状態で起動
- 安全で堅牢な動作を実現する機能
  - ソフトスタート内蔵
  - 過熱および過電圧保護
  - 負荷の切り離しを伴う真のシャットダウン機能
  - 順方向および逆方向の電流制限
- TPS63805
  - 18.5mm^2 の最小ソリューション・サイズに最適化 (22µF の最小限の出力コンデンサで動作)
  - 出力電流：2A (V_{IN} ≥ 2.3V、V_{OUT} = 3.3V)
  - 動作時の静止電流：11µA
- TPS63806
  - 最も優れた負荷ステップ応答性を示すように最適化済み (2A の電流ステップでの負荷ステップ応答 = 180mV)
  - 最大 2.5A の連続出力電流
  - 動作時の静止電流：13µA
- TPS63807
  - 18.5 mm^2 の最小ソリューション・サイズに最適化 (22µF の最小限の出力コンデンサで動作)
  - 出力電流：2A (V_{IN} ≥ 2.3V、V_{OUT} = 3.3V)
  - 動作時の静止電流：11µA
  - EN が LOW のときの出力放電機能
  - 480µs の T_{ramp} で起動時の突入電流を抑制

2 アプリケーション

- TPS63805
  - システム・プリレギュレータ (スマートフォン、タブレット、EFT 端末、テレマティクス)
  - ポイント・オブ・ロード・レギュレーション (有線センサ、ポート/ケーブル・アダプタ、ドングル)
- TPS63806
  - ToF (Time of Flight) カメラ・センサ (スマートフォン、電子スマート・ロック、IP ネットワーク・カメラ)
  - ブロードバンド・ネットワーク無線または SoC 電源 (IoT、トラッキング、ホーム・オートメーション、EPOS)
  - 熱電デバイスの電源 (TEC、光モジュール)
  - 汎用電圧スタビライザ
- TPS63807
  - 出力放電機能を必要とするアプリケーション

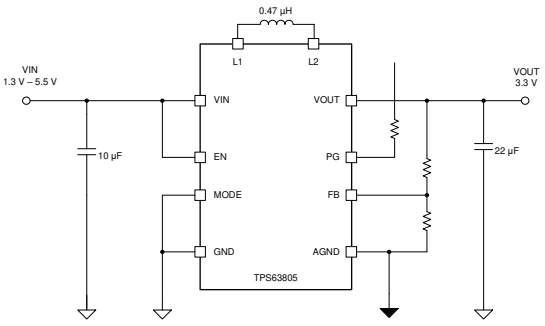
3 概要

TPS63805、TPS63806、TPS63807 は高効率、大出力電流の昇降圧コンバータです。入力電圧に応じて自動的に昇圧モード、降圧モード、革新的な 4 サイクル昇降圧モード (入力電圧が出力電圧とほぼ等しい場合) で動作します。

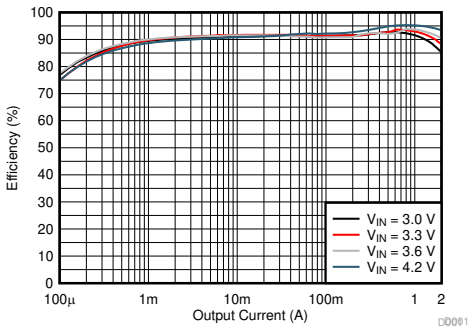
製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TPS63805	3 × 5 ボール WCSP (0.4mm ピッチ)	2.3mm × 1.4mm
TPS63806		
TPS63807		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション



効率と出力電流との関係 (V_O = 3.3V)

Table of Contents

4 Revision History

Changes from Revision D (January 2021) to Revision E (August 2021)	Page
• TPS63807 を追加	1

Changes from Revision C (September 2019) to Revision D (January 2021)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1

5 概要 (続き)

モード間の遷移は定義されたスレッショルドで行い、出力電圧リップルを減らすためモード内での不要な切り替えは行いません。本デバイスの出力電圧は、広い出力電圧範囲内で抵抗分圧器を使用して個別に設定されます。TPS63805 および TPS63807 は、非常に少ない部品数で最小のソリューション・サイズを実現しています。静止電流が 11µA であるため、無負荷または軽負荷条件で最高の効率が得られます。TPS63805、TPS63806、TPS63807 は 1.4mm × 2.3mm のパッケージで供給されます。小型の受動部品を使用できることから、ソリューション全体の小型化が可能になります。

TPS63806 は、重負荷プロファイルでの負荷ステップ応答を重視するアプリケーションに最適化されています。

6 Device Comparison Table

PART NUMBER	OUTPUT VOLTAGE (V_O)	$I_{(Q;VIN)}$ (TYP.)	$C_{(O,EFF)}$ (MIN.)	V_{PP} LOAD TRANSIENT RESPONDS (TYP.)
TPS63805/ TPS63807	Adjustable	11 µA	7 µF	320 mV
TPS63806	Adjustable	13 µA	21 µF	180 mV

7 Pin Configuration and Functions

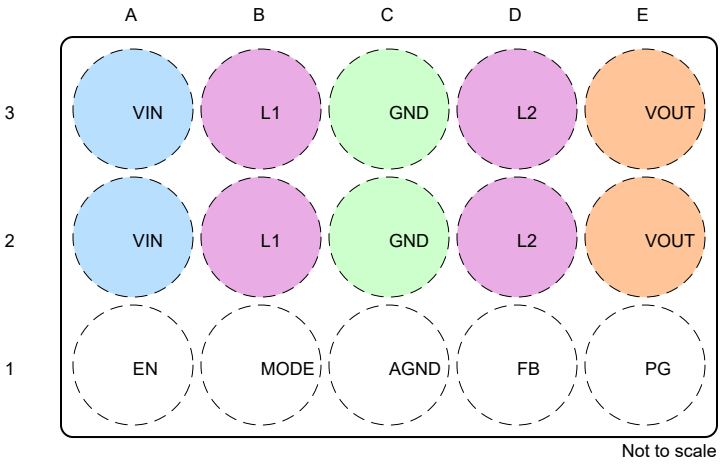


図 7-1. WCSP Package Top View

表 7-1. Pin Functions

PIN		DESCRIPTION
NO	NAME	
A2, A3	VIN	Supply voltage
B2, B3	L1	Connection for inductor
A1	EN	Device Enable input. Set HIGH to enable and LOW to disable. It must not be left floating.
C2, C3	GND	Power ground
B1	MODE	PFM/PWM mode selection. Set LOW for power save mode, set HIGH for forced PWM mode. It must not be left floating.
C1	AGND	Analog ground
D2, D3	L2	Connection for inductor
E2, E3	VOUT	Power stage output
D1	FB	Voltage feedback sensing pin
E1	PG	Power good indicator, open drain output. If not used can be left floating.

8 Specifications

8.1 Absolute Maximum Ratings

over junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	VIN, L1, L2, EN, MODE, VOUT, FB, PG	–0.3	6	V
	L1, L2 (AC, less than 10 ns)	–3	9	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_I	Input voltage		1.3 (1)		5.5	V
V_O	Output voltage		1.8		5.2 (2)	V
C_I	Effective capacitance connected to V_{IN}		4	5		µF
L	Effective inductance		0.37	0.47	0.57	µH
C_O	TPS63805/TPS63807 Effective capacitance connected to V_{OUT}	1.8 V ≤ V_O ≤ 2.3 V	10			µF
		V_O > 2.3 V	7	8.2		µF
C_O	TPS63806 Effective capacitance connected to V_{OUT}	1.8 V ≤ V_O < 2.3 V	30			µF
		V_O > 2.3 V	21	27		µF
T_J	Operating junction temperature	Operating junction temperature	–40		125	°C

(1) Minimum start-up voltage of V_I > 1.8 V until power good
(2) V_O margin for accuracy and load steps is considerd in absolut maximum ratings

8.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC(1)		TPS6380x 3x5 Ball WCSP 15 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	78.8	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	0.6	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	19.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	19.5	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

8.5 Electrical Characteristics

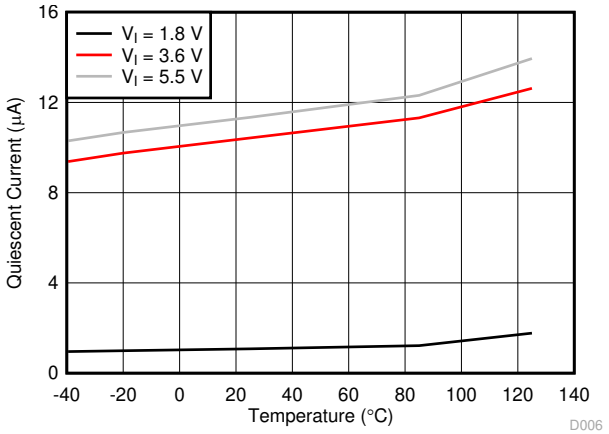
V_{IN}= 1.8 V to 5.5 V, V_{OUT} = 1.8 V to 5.2 V , T_J= –40°C to +125°C, typical values are at V_{IN}= 3.6 V, V_{OUT} = 3.3 V and T_J= 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$V_{IN;LOAD}$	Minimum input voltage for full load, once started	I_{OUT} = 2 A, VOUT = 3.3 V, T_J = 25°C		2.3		V
$I_{Q;VIN}$	Quiescent current into VIN	TPS63805/TPS63807; T_J = 25°C, EN = V_{IN} = 3.6 V, V_{OUT} = 3.3 V, not switching		11		µA
$I_{Q;VIN}$	Quiescent current into VIN	TPS63806; T_J = 25°C, EN = V_{IN} = 3.6 V, V_{OUT} = 3.3 V, not switching		13		µA
I_{SD}	Shutdown current into VIN	EN = low, -40°C ≤ T_J ≤ 85°C, V_{IN} = 3.6 V, V_{OUT} = 0 V		45	600	nA
UVLO	Undervoltage lockout threshold	V_{IN} falling, VOUT ≥ 1.8 V, once started	1.2	1.25	1.29	V
	Undervoltage lockout threshold	V_{IN} rising	1.6	1.7	1.79	V
T_{SD}	Thermal shutdown	Temperature rising		150		°C
$T_{SD;HYST}$	Thermal shutdown hysteresis			20		°C
SOFT-START, POWER GOOD						
T_{ramp}	Soft-start, Current limit ramp time	TPS63805/TPS63806 T_J = 25°C, V_{IN} = 3.6 V, V_{OUT} = 3.3 V, I_O = 3.5 A, time from first switching to power good		224		µs
		TPS63807 T_J = 25°C, V_{IN} = 3.6 V, V_{OUT} = 3.3 V, I_O = 3.5 A, time from first switching to power good		480		µs
T_{delay}	Delay from EN-edge until rising V_{OUT}	T_J = 25°C, V_{IN} = 3.6 V, V_{OUT} = 3.3 V, Delay from EN-edge until rising first switching		321		µs
LOGIC SIGNALS EN, MODE						
$V_{THR;EN}$	Threshold Voltage rising for EN-Pin		1.07	1.1	1.13	V
$V_{THF;EN}$	Threshold Voltage falling for EN-Pin		0.97	1	1.03	V
V_{IH}	High-level input voltage		1.2			V
V_{IL}	Low-level input voltage				0.4	V
$V_{PG;rising}$	Power Good threshold voltage	VOUT rising, referenced to VOUT nominal		95		%
$V_{PG;falling}$		VOUT falling, referenced to VOUT nominal		90		%
$V_{PG;Low}$	Power Good low-level output voltage	I_{SINK} = 1 mA			0.4	V
$t_{PG;delay}$	Power Good delay time	V_{FB} falling		14		µs
I_{lkg}	Input leakage current			0.01	0.2	µA
OUTPUT						
I_{SD}	Shutdown current into VOUT	TPS63805/TPS63806 EN = low, -40°C ≤ T_J ≤ 85°C, V_{IN} = 3.6 V, V_{OUT} = 3.3 V		±0.5	±600	nA
V_{FB}	Feedback Regulation Voltage			500		mV
V_{FB}	Feedback Voltage accuracy	PWM mode	–1		1	%
	Overvoltage Protection Threshold	V_{OUT} rising	5.5	5.7	5.9	V
		V_{IN} rising	5.5	5.7	5.9	V
$I_{PWM/PFM}$	Peak Inductor Current to enter PFM-Mode	V_{IN} = 3.6 V; V_{OUT} = 3.3 V		1.06		A
I_{FB}	Feedback Input Bias Current	V_{FB} = 500 mV		5	100	nA
I_{PK}	Peak Current Limit, Boost Mode	TPS63805/TPS63807; V_{IN} ≥ 2.5 V	4	5	5.75	A
	Peak Current Limit, Buck-Boost Mode			5		A
	Peak Current Limit, Buck Mode			3.8		A
I_{PK}	Peak Current Limit, Boost Mode	TPS63806; V_{IN} ≥ 2.5V	4.4	5.5	6.25	A
	Peak Current Limit, Buck-Boost Mode			5.5		A
	Peak Current Limit, Buck Mode			4		A
$I_{PK;Reverse}$	Peak Current Limit for Reverse Operation	V_I = 5 V, V_O = 3.3 V		–0.9		A

V_{IN}= 1.8 V to 5.5 V, V_{OUT} = 1.8 V to 5.2 V , T_J= –40°C to +125°C, typical values are at V_{IN}= 3.6 V, V_{OUT} = 3.3 V and T_J= 25°C (unless otherwise noted)

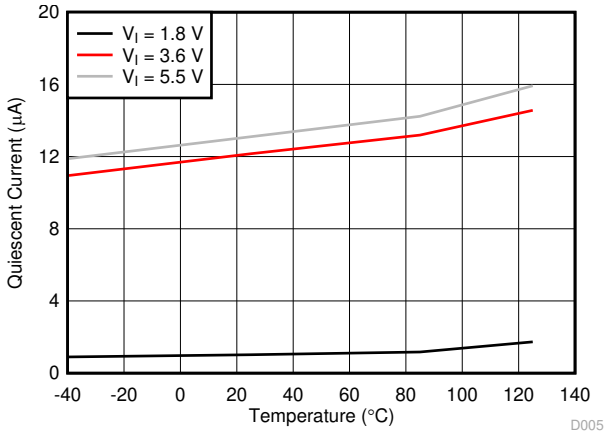
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Buck $R_{DS;ON}$	High-side FET on-resistance	V_{IN} = 3 V, V_{OUT} = 3.3 V; $I_{(L2)}$ = 0.19 A	V_{IN} = 3 V, V_{OUT} = 3.3 V; I_O = 0.5 A		47		mΩ
	Low-side FET on-resistance	V_{IN} = 3 V, V_{OUT} = 3.3 V; $I_{(L2)}$ = 0.19 A	V_{IN} = 3 V, V_{OUT} = 3.3 V; I_O = 0.5 A		30		mΩ
Boost $R_{DS;ON}$	High-side FET on-resistance	V_{IN} = 3 V, V_{OUT} = 3.3 V; $I_{(L1)}$ = 0.19 A	V_{IN} = 3 V, V_{OUT} = 3.3 V; I_O = 0.5 A		43		mΩ
	Low-side FET on-resistance	V_{IN} = 3 V, V_{OUT} = 3.3 V; $I_{(L1)}$ = 0.19 A	V_{IN} = 3 V, V_{OUT} = 3.3 V; I_O = 0.5 A		18		mΩ
f_{SW}	Inductor Switching Frequency, Boost Mode	V_{IN} = 2.3V, V_{OUT} = 3.3V, no Load, MODE = HIGH, T_J = 25°C			2.1		MHz
	Inductor Switching Frequency, Buck-Boost Mode	V_{IN} = 3.3V, V_{OUT} = 3.3V, no Load, MODE = HIGH, T_J = 25°C			1.4		MHz
	Inductor Switching Frequency, Buck Mode	V_{IN} = 4.3, V_{OUT} = 3.3V, no Load, MODE = HIGH, T_J = 25°C			1.6		MHz
	Line regulation	V_{IN} = 2.4 V to 5.5 V, V_{OUT} = 3.3V, I_{OUT} = 2 A			0.3		%
	Load regulation	V_{IN}= 3.6 V, V_{OUT} = 3.3V, I_{OUT} = 0 A to 2 A, forced-PWM mode			0.1		%

8.6 Typical Characteristics



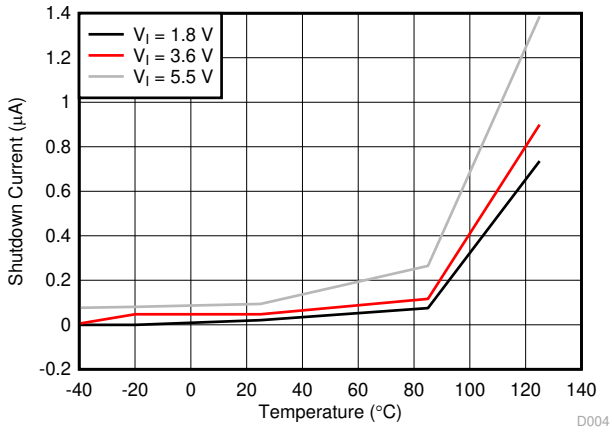
MODE = LOW V_O = 3.3 V I_O = 0 mA, not switching

図 8-1. TPS63805/TPS63807 Quiescent Current vs. Temperature



MODE = LOW V_O = 3.3 V I_O = 0 mA, not switching

図 8-2. Quiescent Current vs. Temperature



EN = LOW

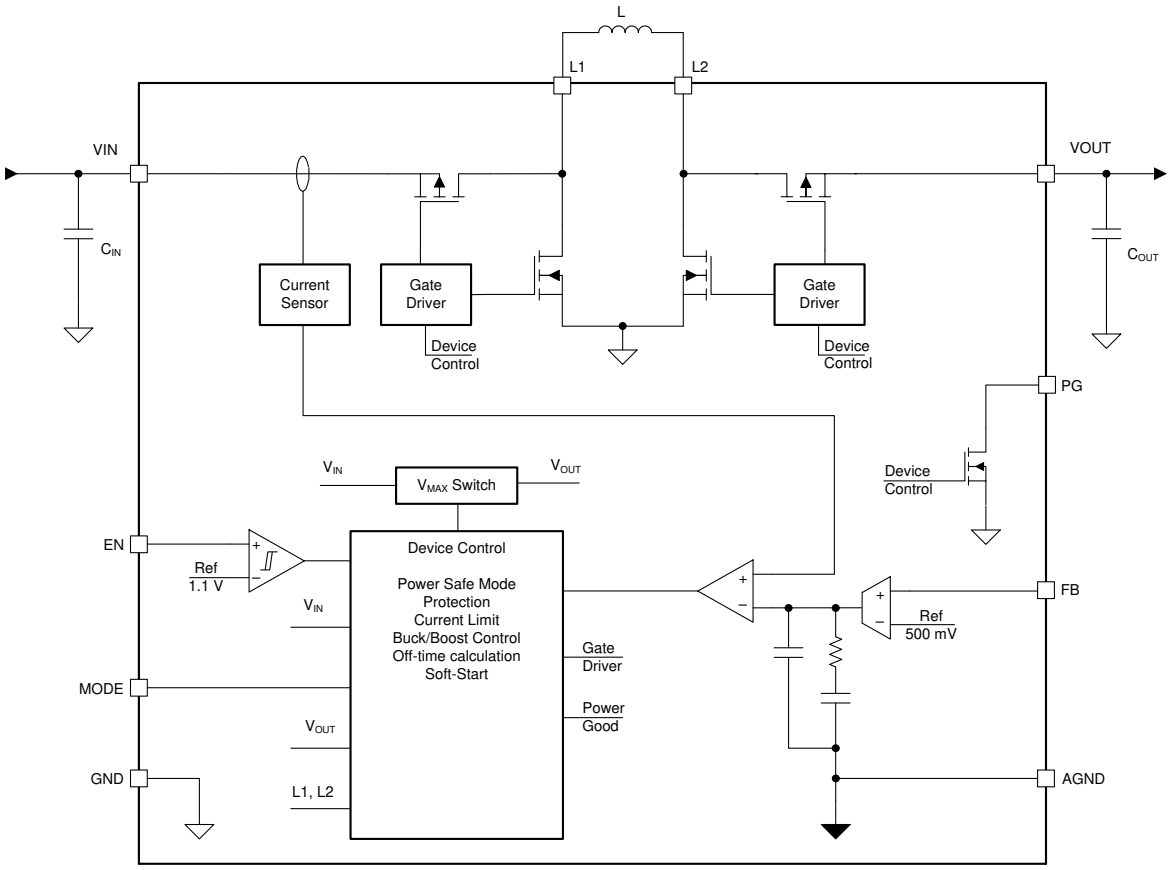
図 8-3. Shutdown Current vs. Temperature

9 Detailed Description

9.1 Overview

The TPS63805, TPS63806, and TPS63807 buck-boost converter use four internal switches to maintain synchronous power conversion at all possible operating conditions. This enables the device to keep high efficiency over a wide input voltage and output load range. To regulate the output voltage at all possible input voltage conditions, the device automatically transitions between buck, buck-boost, and boost operation as required by the operating conditions. Therefore, it operates as a buck converter when the input voltage is higher than the output voltage, and as a boost converter when the input voltage is lower than the output voltage. When the input voltage is close to the output voltage, it operates in a 3-cycle buck-boost operation. In this mode, all four switches are active (see *セクション 9.4.1.3*). The RMS current through the switches and the inductor is kept at a minimum to minimize switching and conduction losses. Controlling the switches this way allows the converter to always keep high efficiency over the complete input voltage range. The device provides a seamless transition between all modes.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Control Loop Description

The TPS63805, TPS63806, and TPS63807 use a peak current mode control architecture. It has an inner current loop where it measures the peak current of the boost high-side MOSFET and compares it to a reference current. This current is the output of the outer voltage loop. It measures the output voltage via the FB-pin and compares it with the internal voltage reference. That means, the outer voltage loop measures the voltage error (V_{REF}-V_{FB}), and transforms it into the system current demand (I_{REF}) for the inner current loop.

図 9-1 shows the simplified schematic of the control loop. The error amplifier and the type-2 compensation represent the voltage loop. The voltage output is converted into the reference current IREF and fed into the current comparator.

The scheme shows the skip-comparator handling the power-save mode (PFM) to achieve high efficiency at light loads. See *セクション 9.4.2* for further details.

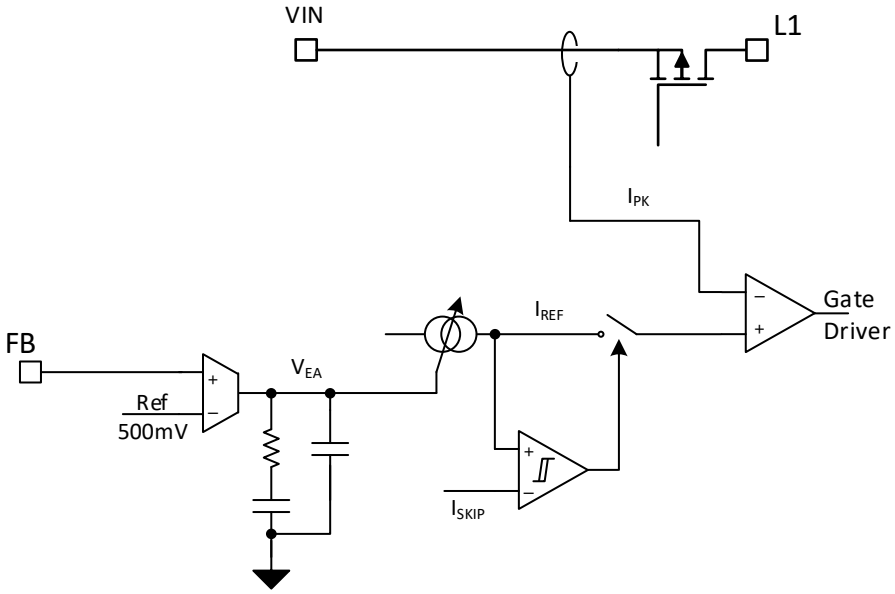


図 9-1. Control Loop Architecture Scheme

9.3.2 Precise Device Enable: Threshold- or Delayed Enable

The enable-pin is a digital input to enable or disable the device by applying a high or low level. The device enters shutdown when EN is set low. In addition, this input features a precise threshold and can be used as a comparator that enables and disables the part at a defined threshold. This allows you to drive the state by a slowly changing voltage and enables the use of an external RC network to achieve a precise power-up delay. The enable pin can also be used with an external voltage divider to set a user-defined minimum supply voltage. For proper operation, the EN pin must be terminated and must not be left floating.

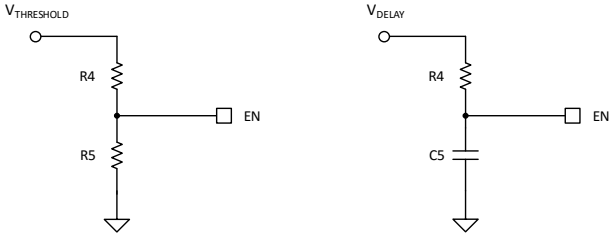


図 9-2. Circuit Example for How to Use the Precise Device Enable Feature

9.3.3 Mode Selection (PFM/PWM)

The mode-pin is a digital input to enable the automatic PWM/PFM mode that features the highest efficiency by allowing pulse-frequency-modulation for lower output currents. This mode is enabled by applying a low level. The device can be forced in PWM operation regardless of the output current to achieve minimum output ripple by applying a high level. This pin must not be left floating.

9.3.4 Undervoltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages, an undervoltage lockout is included. It activates the device once the input voltage (V_I) has increased the $UVLO_{rising}$ value. Once active, the device allows operation down to even smaller input voltages, which is determined by the $UVLO_{falling}$. This behavior requires V_O to be higher than the minimum value of 1.8 V.

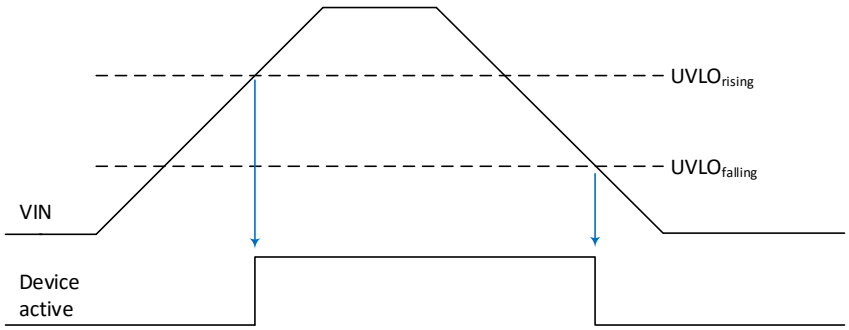


図 9-3. Rising and Falling Undervoltage Lockout Behavior

9.3.5 Soft Start

To minimize inrush current and output voltage overshoot during start-up, the device features a controlled soft start-up. After the device is enabled, the device starts all internal reference and control circuits within the enable delay time, T_{delay}. After that, the maximum switch current limit rises monotonically from 0 mA to the current limit. The loop stops switching once V_O is reached. This allows a quick output voltage ramp for small capacitors at the output. The bigger the output capacitor, the longer it takes to settle V_o. A potential load during start-up will lengthen the duration of the output voltage ramp as well. The gradual ramp of the current limit allows a small inrush current for no-load conditions, as well as the possibility to start into high loads at start-up.

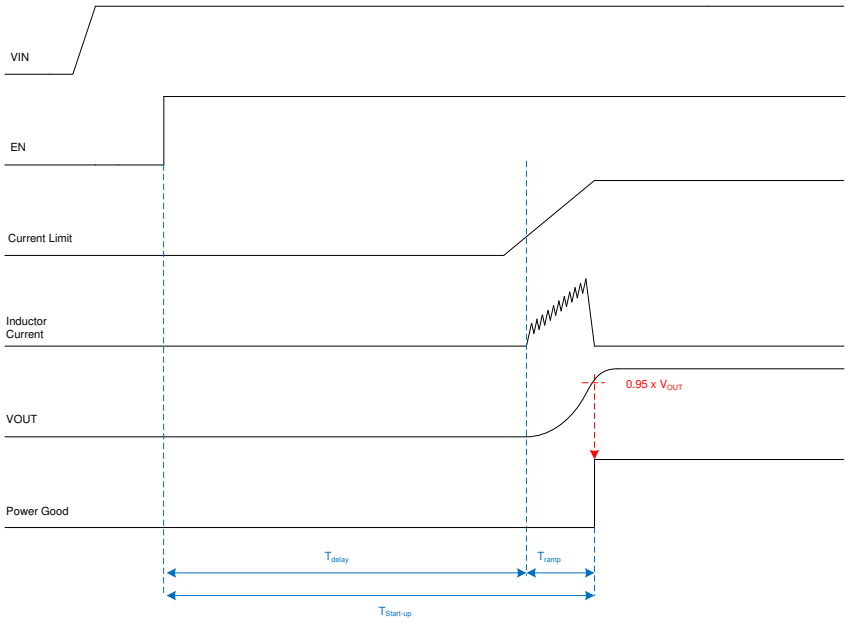


図 9-4. Device Start-up Scheme

9.3.6 Adjustable Output Voltage

The device's output voltage is adjusted by applying an external resistive divider between V_O, the FB-pin, and GND. This allows you to program the output voltage in the recommended range. The divider must provide a low-side resistor of less than 100 kΩ. The high-side resistor is chosen accordingly.

9.3.7 Overtemperature Protection - Thermal Shutdown

The device has a built-in temperature sensor which monitors the junction temperature. If the temperature exceeds the threshold, the device stops operating. As soon as the IC temperature has decreased below the programmed threshold, it starts operating again. There is a built-in hysteresis to avoid unstable operation at junction temperatures at the overtemperature threshold.

9.3.8 Input Overvoltage - Reverse-Boost Protection (IVP)

The TPS63805, TPS63806, and TPS63807 can operate in reverse mode where the device transfers energy from the output back to the input. If the source is not able to sink the revers current, the negative current builds up a charge to the input capacitance and V_{IN} rises. To protect the device and other components from that scenario, the device features an input voltage protection (IVP) for reverse boost operation. Once the input voltage is above the threshold, the converter forces PFM mode and the negative current operation is interrupted.

The PG signal goes low to indicate that behavior.

9.3.9 Output Overvoltage Protection (OVP)

In case of a broken feedback-path connection, the device can loose V_O information and is not able to regulate. To avoid an uncontrolled boosting of V_O, the TPS63805, TPS63806, and TPS63807 feature output overvoltage protection. It measures the voltage on the VOUT pin and stops switching when V_O is greater than the threshold to avoid harm to the converter and other components.

9.3.10 Power-Good Indicator

The power good goes high-impedance once the output is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. This feature also indicates overvoltage and device shutdown cases as shown in 表 9-1. The PG pin is an open-drain output and is specified to sink up to 1 mA. The power-good output requires a pullup resistor connecting to any voltage rail less than 5.5 V. The PG signal can be used to sequence multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used.

表 9-1. Power-Good Indicator Truth Table

LOGIC SIGNALS					PG LOGIC STATUS
EN	V_O	V_I	OVP	IVP	
X	< 1.8 V	< UVLO_R	X	X	Undefined
LOW	X	> UVLO_F	X	X	LOW
HIGH	V_O < 0.9 × target-V_O	> 1.3V	X	X	LOW
HIGH	X	> UVLO_F	HIGH	X	LOW
HIGH	X	> UVLO_F	X	HIGH	LOW
HIGH	V_O > 0.95 × target-V_O	> UVLO_F	LOW	LOW	HIGH Z

9.4 Device Functional Modes

9.4.1 Peak-Current Mode Architecture

The TPS63805, TPS63806, and TPS63807 are based on a peak-current mode architecture. The error amplifier provides a peak-current target (voltage that is translated into an equivalent current, see 図 9-1), based on the current demand from the voltage loop. This target is compared to the actual inductor current during the ON-time. The ON-time is ended once the inductor current is equal to the current target and OFF-time is initiated. The OFF-time is calculated by the control and a function of V_I and V_O.

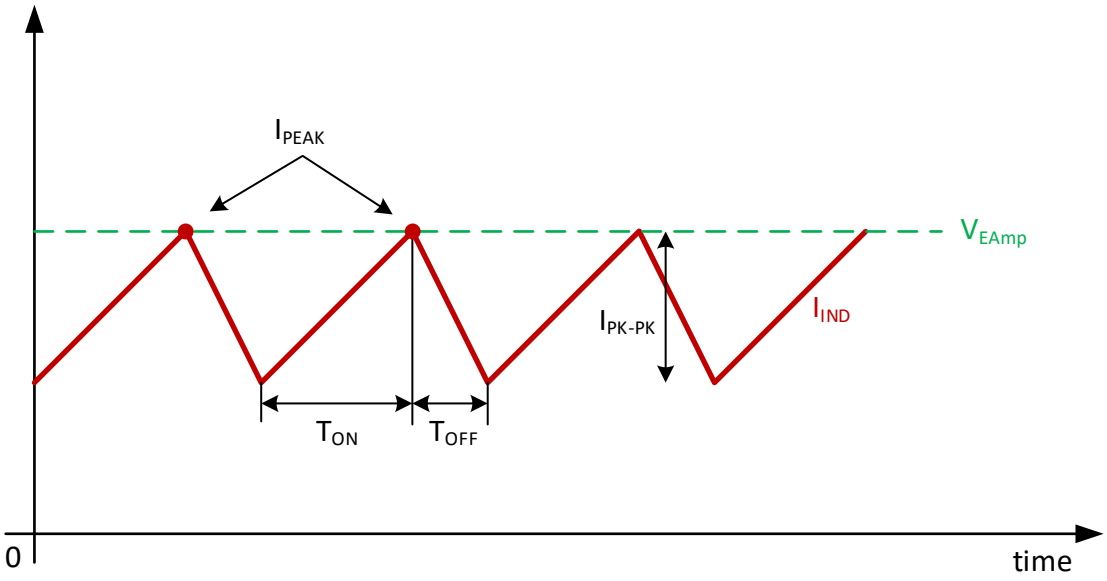


図 9-5. Peak-Current Architecture Operation

9.4.1.1 Reverse Current Operation, Negative Current

When the TPS63805, TPS63806, and TPS63807 are forced to PWM operation (MODE = HIGH), the device current can flow in reverse direction. This happens by the negative current capability of the TPS63805, TPS63806, and TPS63807. The error amplifier provides a peak-current target (voltage that is translated into an equivalent current, see 図 9-1), even if the target has a negative value. The maximum average current is even more negative than the peak current.

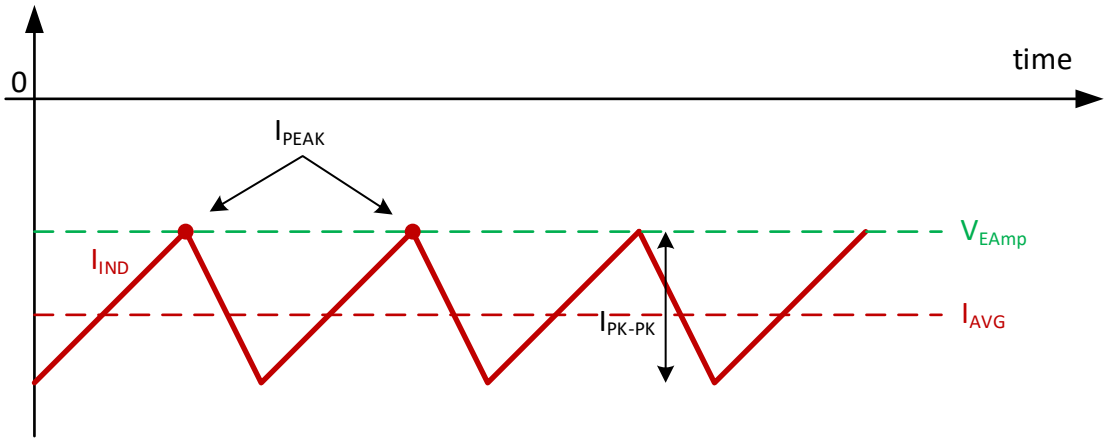


図 9-6. Peak-Current Operation, Reverse Current

9.4.1.2 Boost Operation

When V_I is smaller than V_O (and the voltages are not close enough to trigger buck-boost operation), the TPS63805, TPS63806, and TPS63807 operate in boost mode where the boost high-side and low-side switches are active. The buck high-side switch is always turned on and the buck low-side switch is always turned off. This lets the TPS63805, TPS63806, and TPS63807 operate as a classical boost converter.

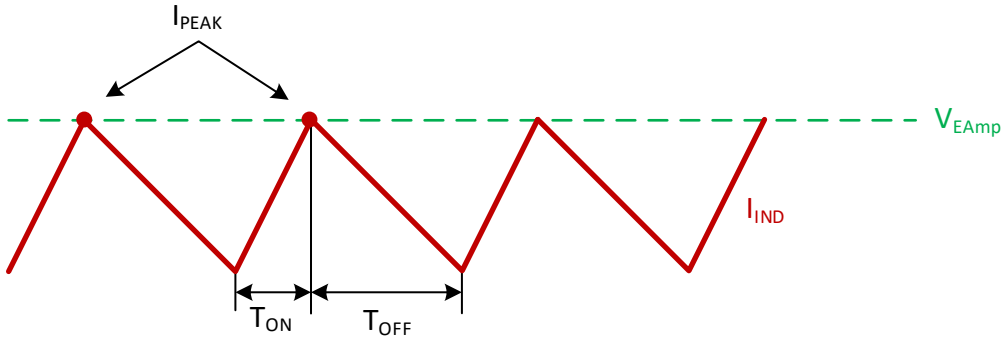


図 9-7. Peak-Current Boost Operation

9.4.1.3 Buck-Boost Operation

When V_I is close to V_O, the TPS63805, TPS63806, and TPS63807 operate in buck-boost mode where all switches are active and the device repeats 3-cycles:

- T_{ON}: Boost-charge phase where boost low-side and buck high-side are closed and the inductor current is built up
- T_{OFF}: Buck discharge phase where boost high-side and buck low-side are closed and the inductor is discharged
- T_{COM}: V_I connected to V_O where all high-side switches are closed and the input is connected to the output

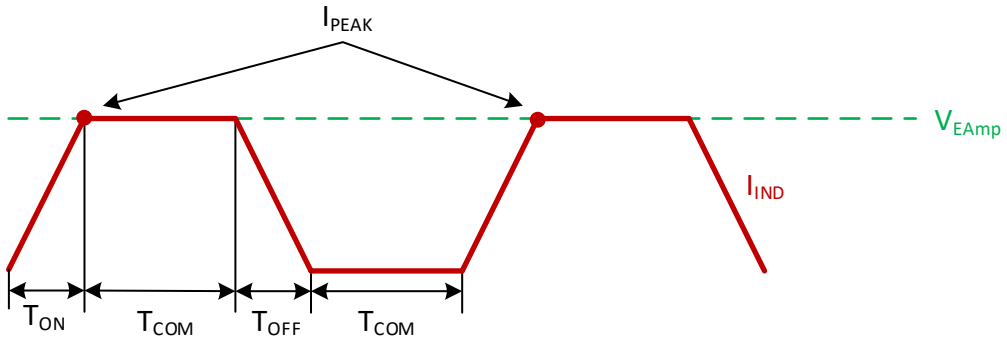


図 9-8. Peak-Current Buck-Boost Operation

9.4.1.4 Buck Operation

When V_I is greater than V_O (and the voltages are not close enough to trigger buck-boost operation), the TPS63805, TPS63806, and TPS63807 operate in buck mode where the buck high-side and low-side switches are active. The boost high-side switch is always turned on and the boost low-side switch is always turned off. This lets the TPS63805, TPS63806, and TPS63807 operate as a classical buck converter.

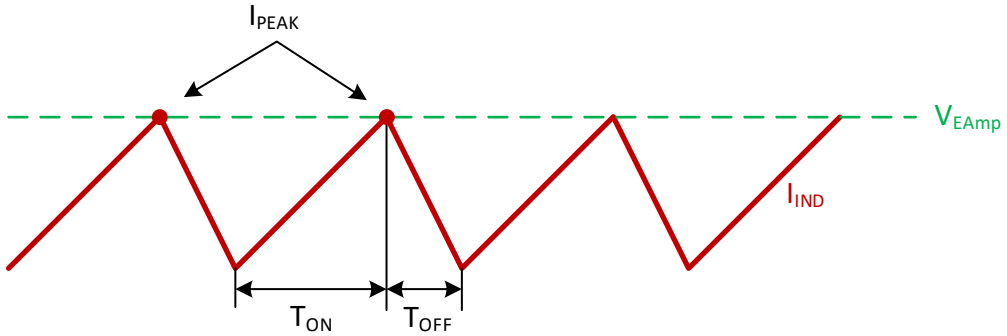


図 9-9. Peak-Current Buck Operation

9.4.2 Power Save Mode Operation

Besides continuos conduction mode (PWM), the TPS63805, TPS63806, and TPS63807 feature power safe mode (PFM) operation to achieve high efficiency at light load currents. This is implemented by pausing the switching operation, depending on the load current.

The skip comparator manages the switching or pause operation. It compares the current demand signal from the voltage loop, I_{REF}, with the skip threshold, I_{SKIP}, as shown in 図 9-1. If the current demand is lower than the skip value, the comparator pauses switching operation. If the current demand goes higher (due to falling V_O), the comparator activates the current loop and allows switching according to the loop behavior. Whenever the current loop has risen V_O by bringing charge to the output, the voltage loop output, I_{REF} (respectively V_{EA}), decreases. When I_{REF} falls below I_{SKIP}-hysteresis, it automatically pauses again.

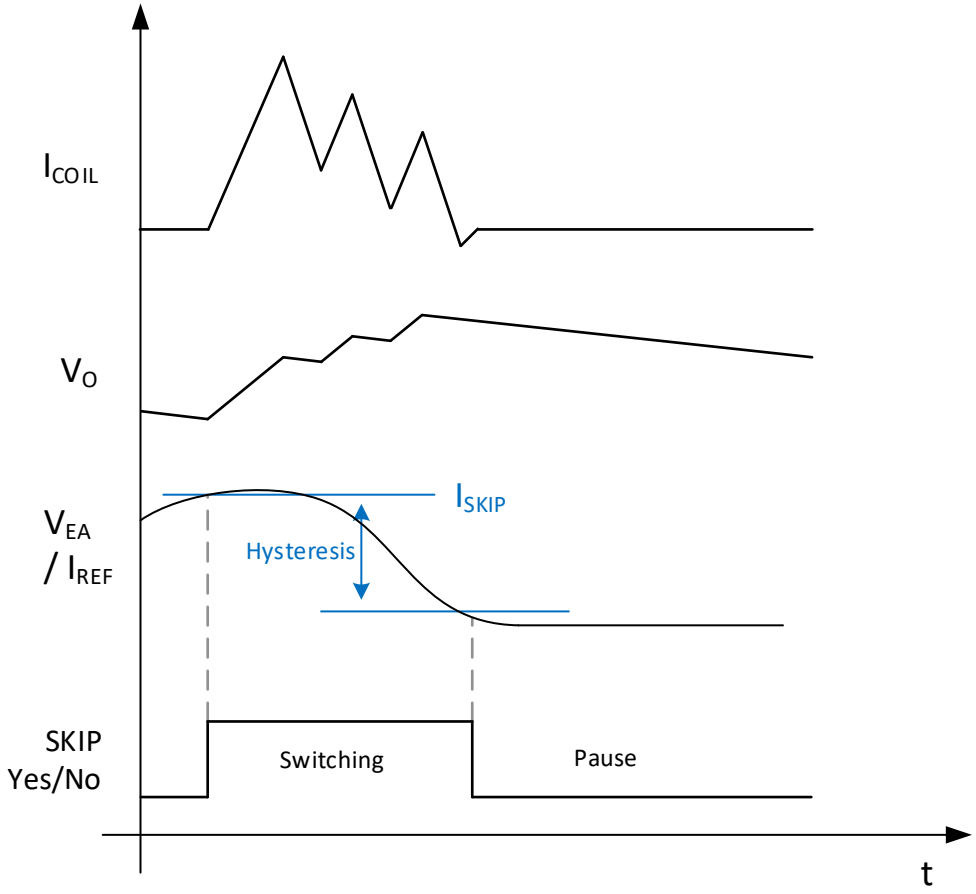


図 9-10. Power Safe Mode Operation Curves

9.4.2.1 Current Limit Operation

To limit current and protect the device and application, the maximum peak inductor current is limited internally on the IC. It is measured at the buck high-side switch which turns into an input current detection. To provide a certain load current across all operation modes, the boost and buck-boost peak current limit is higher than in buck mode. It limits the input current and allows no further increase of the delivered current. When using the device in this mode, it behaves similar to a current source.

The current limit depends on the operation mode (buck, buck-boost, or boost mode).

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The TPS63805, TPS63806, and TPS63807 are high efficiency, low quiescent current, non-inverting buck-boost converters, suitable for applications that need a regulated output voltage from an input supply that can be higher or lower than the output voltage.

10.2 Typical Application

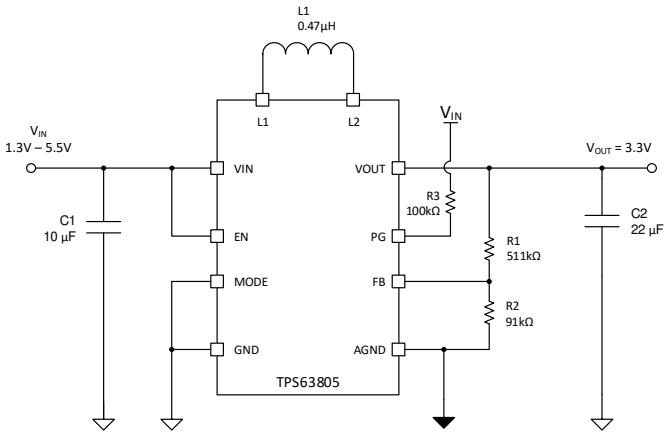


図 10-1. TPS63805/TPS63807 3.3 V_{OUT} Typical Application

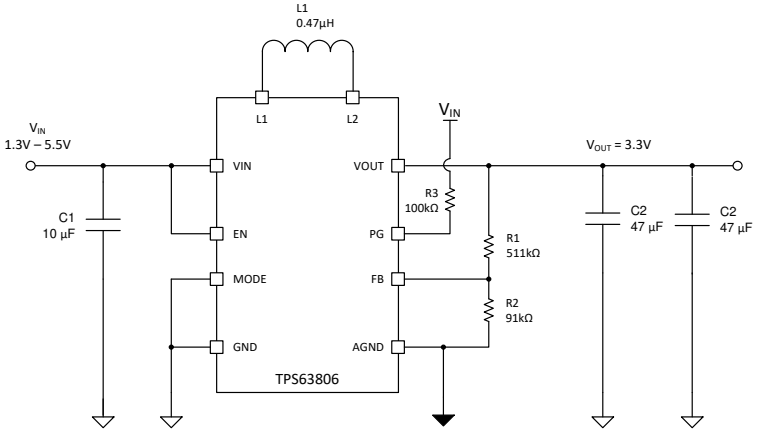


図 10-2. TPS63806 3.3 V_{OUT} Typical Application

10.2.1 Design Requirements

The design guideline provides a component selection to operate the device within 表 10-1.

表 10-1 shows the list of components for the application characteristic curves.

表 10-1. Matrix of Output Capacitor and Inductor Combinations for the TPS63805/TPS63807

NOMINAL INDUCTOR VALUE [µH](1)	NOMINAL OUTPUT CAPACITOR VALUE [µF](2)				
	10	22	47	66	100
0.47	-	+ (3)	+	+	+

(1) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and –30%.
(2) Capacitance tolerance and DC bias voltage derating is anticipated. The effective capacitance can vary by 20% and –50%.
(3) TPS63805/TPS63807 typical application. Other check marks indicate possible filter combinations.

表 10-2. Matrix of Output Capacitor and Inductor Combinations for TPS63806

NOMINAL INDUCTOR VALUE [µH](1)	NOMINAL OUTPUT CAPACITOR VALUE [µF](2)				
	10	22	47	66	100
0.47	-	-	+(1)	+	+

(1) TPS63806 typical application. Other check marks indicate possible filter combinations.

10.2.2 Detailed Design Procedure

The first step is the selection of the output filter components. To simplify this process, *セクション 8.1* outlines minimum and maximum values for inductance and capacitance. Take tolerance and derating into account when selecting nominal inductance and capacitance.

10.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS63805/TPS63807 device with the WEBENCH® Power Designer. Click here to create a custom design using the TPS63806 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

10.2.2.2 Inductor Selection

The inductor selection is affected by several parameters such as the following:

- Inductor ripple current
- Output voltage ripple
- Transition point into power save mode
- Efficiency

See 表 10-3 for typical inductors.

For high efficiencies, the inductor must have a low DC resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a high impact on efficiency. When using small chip inductors, the efficiency is reduced, mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. To avoid saturation of the inductor, the peak current for the inductor in steady-state operation is calculated using 式 2. Only the equation which defines the switch current

in boost mode is shown because this provides the highest value of current and represents the critical current value for selecting the right inductor.

$$\text{Duty Cycle Boost} \quad D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{1}$$

$$I_{PEAK} = \frac{Iout}{\eta \times (1 - D)} + \frac{Vin \times D}{2 \times f \times L} \tag{2}$$

where

- D = Duty Cycle in Boost mode
- *f* = Converter switching frequency
- L = Inductor value
- η = Estimated converter efficiency (use the number from the efficiency curves or 0.9 as an assumption)

Note

The calculation must be done for the minimum input voltage in boost mode.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. It is recommended to choose an inductor with a saturation current 20% higher than the value calculated using 式 2. 表 10-3 lists the possible inductors.

表 10-3. List of Recommended Inductors

INDUCTOR VALUE [µH]	SATURATION CURRENT [A]	DCR [mΩ]	PART NUMBER	MANUFACTURER(1)	SIZE (LxWxH mm)
0.47	5.4	7.6	XFL4015-471ME	Coilcraft	4 x 4 x 2
0.47	5.5	26	DFE201612E	Toko	2.0 x 1.6 x 1.2

(1) See *Third-party Products Disclaimer*.

10.2.2.3 Output Capacitor Selection

For the output capacitor, it is recommended to use small ceramic capacitors placed as close as possible to the VOUT and PGND pins of the IC. The recommended nominal output capacitor value is a single 22 µF for the TPS63805/TPS63807 and 2x47 µF for the TPS63806 for all programmed output voltages ≤ 3.6 V. Above that voltage, 2x22 µF for the TPS63805/TPS63807 and 3x47 µF for the TPS63806 capacitors are recommended.

It is important that the effective capacitance is given according to the recommended value in *セクション 8.3*. In general, consider DC bias effects resulting in less effective capacitance. The choice of the output capacitance is mainly a trade-off between size and transient behavior since higher capacitance reduces transient response overshoot and undershoot and increases transient response time. 表 10-4 lists possible output capacitors.

There is no upper limit for the output capacitance value.

表 10-4. List of Recommended Capacitors(1)

CAPACITOR [µF]	VOLTAGE RATING [V]	ESR [mΩ]	PART NUMBER	MANUFACTURER	SIZE (METRIC)
22	6.3	10	GRM188R60J226MEA0	Murata	0603 (1608)
22	6.3	10	GRM187R61A226ME15	Murata	0603 (1608)
22	10	40	GRM188R61A226ME15	Murata	0603 (1608)
22	10	10	GRM187R60J226ME15	Murata	0603 (1608)
47	6.3	43	GRM188R60J476ME15	Murata	0603 (1608)
47	6.3	43	GRM219R60J476ME44	Murata	0805 (2012)

(1) See *Third-party Products Disclaimer*.

10.2.2.4 Input Capacitor Selection

A 10 µF input capacitor is recommended to improve line transient behavior of the regulator and EMI behavior of the total power supply circuit. An X5R or X7R ceramic capacitor placed as close as possible to the VIN and PGND pins of the IC is recommended. This capacitance can be increased without limit. If the input supply is located more than a few inches from the TPS63805, TPS63806, and TPS63807 converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

表 10-5. List of Recommended Capacitors(1)

CAPACITOR [µF]	VOLTAGE RATING [V]	ESR [mΩ]	PART NUMBER	MANUFACTURER	SIZE (METRIC)
10	6.3	10	GRM188R60J106ME84	Murata	0603 (1608)
10	10	40	GRM188R61A106ME69	Murata	0603 (1608)
22	6.3	10	GRM188R60J226MEA0	Murata	0603 (1608)

10.2.2.5 Setting The Output Voltage

The output voltage is set by an external resistor divider. The resistor divider must be connected between VOUT, FB, and GND. The feedback voltage is 500 mV nominal. The low-side resistor R2 (between FB and GND) must not exceed 100 kΩ. The high-side resistor (between FB and VOUT) R1 is calculated by 式 3.

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \tag{3}$$

where

- V_{FB} = 500 mV

表 10-6. Resistor Selection for Typ. Voltages

V_O [V]	R1 [kΩ]	R2 [kΩ]
2.5	365	91
3.3	511	91
3.6	562	91
5	806	91

10.2.3 Application Curves

表 10-7. Components for Application Characteristic Curves (1)

REFERENCE	DESCRIPTION	PART NUMBER	MANUFACTURER	COMMENT
L1	0.47µH, 4 mm x 4 mm x 1.5 mm, 5.4 A, 7.6 mΩ	XFL4015-471ME	Coilcraft	
C1	10 µF, 0603, Ceramic Capacitor, ±20%, 6.3 V	GRM188R60J106ME84	Murata	
C2	TPS63805 1x 22 µF, 0603, Ceramic Capacitor, ±20%, 10 V	GRM188R61A226ME15	Murata	TPS63805/TPS63807, V_O ≤ 3.6 V
C2	TPS63806 2x 47 µF, 0603, Ceramic Capacitor, ±20%, 6.3 V	GRM188R60J476ME15	Murata	TPS63806, V_O ≤ 3.6 V
C2	TPS63805 2x 22 µF, 0603, Ceramic Capacitor, ±20%, 10 V	GRM188R61A226ME15	Murata	TPS63805/TPS63807, V_O > 3.6 V
C2	TPS63806 3x 47 µF, 0603, Ceramic Capacitor, ±20%, 6.3 V	GRM188R60J476ME15	Murata	TPS63806, V_O > 3.6 V
R1	511 kΩ, 0603 Resistor, 1%, 100 mW	Standard	Standard	V_O = 3.3 V
R1	562 kΩ, 0603 Resistor, 1%, 100 mW	Standard	Standard	V_O = 3.6 V
R1	806 kΩ, 0603 Resistor, 1%, 100 mW	Standard	Standard	V_O = 5 V
R2	91 kΩ, 0603 Resistor, 1%, 100 mW	Standard	Standard	

表 10-7. Components for Application Characteristic Curves (1) (continued)

REFERENCE	DESCRIPTION	PART NUMBER	MANUFACTURER	COMMENT
R3	100 kΩ, 0603 Resistor, 1%, 100 mW	Standard	Standard	

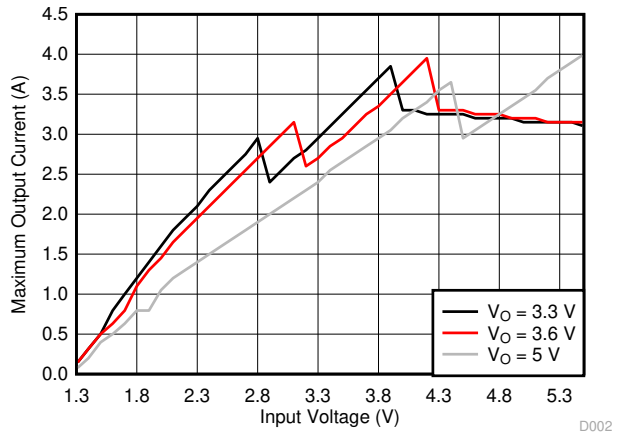
(1) See *Third-party Products Disclaimer*.

表 10-8. Typical Characteristics Curves

PARAMETER	CONDITIONS	FIGURE
Output Current Capability		
Typical Output Current Capability versus Input Voltage	V_O = 3.3 V, TPS63805/TPS63807	図 10-3
Typical Output Current Capability versus Input Voltage	V_O = 3.3 V, TPS63806	図 10-4
Switching Frequency (TPS63805, TPS63806,TPS63807)		
Typical Inductor Switching Frequency versus Input Voltage	I_O = 0 A, MODE = High	図 10-5
Typical Inductor Burst Frequency versus Output Current	V_O = 3.3 V	図 10-6
Efficiency (TPS63805/TPS63807)		
Efficiency versus Output Current (PFM/PWM)	V_I = 2.5 V to 4.2 V, V_O = 3.3 V, MODE = Low	図 10-7
Efficiency versus Output Current (PWM only)	V_I = 2.5 V to 4.2 V, V_O = 3.3 V, MODE = High	図 10-8
Efficiency versus Output Current (PFM/PWM)	V_I = 1.8 V to 5 V, V_O = 3.3 V, MODE = Low	図 10-9
Efficiency versus Output Current (PWM only)	V_I = 1.8 V to 5 V, V_O = 3.3 V, MODE = High	図 10-10
Efficiency versus. Input Voltage (PFM/PWM)	V_O = 3.3 V, MODE = Low	図 10-11
Efficiency versus Input Voltage (PWM only)	I_O = 1 A, MODE = High	図 10-12
Efficiency (TPS63806)		
Efficiency versus Output Current (PFM/PWM)	V_I = 2.5 V to 4.2, V_O = 3.3 V, MODE = Low	図 10-13
Efficiency versus Output Current (PWM only)	V_I = 2.5 V to 4.2 , V_O = 3.3 V, MODE = High	図 10-14
Efficiency versus Output Current (PFM/PWM)	V_I = 1.8 V to 5, V_O = 3.3 V, MODE = Low	図 10-15
Efficiency versus Output Current (PWM only)	V_I = 2.5 V to 5, V_O = 3.3 V, MODE = High	図 10-18
Efficiency versus Input Voltage (PFM/PWM)	V_O = 3.3 V, MODE = Low	図 10-17
Efficiency versus Input Voltage (PWM only)	I_O = 1 A, MODE = High	図 10-18
Regulation Accuracy (TPS63805/TPS63807)		
Load Regulation, PWM Operation	V_O = 3.3 V, MODE = High	図 10-19
Load Regulation, PFM/PWM Operation	V_O = 3.3 V, MODE = Low	図 10-20
Line Regulation, PWM Operation	I_O = 1 A, MODE = High	図 10-21
Line Regulation, PFM/PWM Operation	I_O = 1 A, MODE = Low	図 10-22
Regulation Accuracy (TPS63806)		
Load Regulation, PWM Operation	V_O = 3.3 V, MODE = High	図 10-23
Load Regulation, PFM/PWM Operation	V_O = 3.3 V, MODE = Low	図 10-24
Line Regulation, PWM Operation	I_O = 1 A, MODE = High	図 10-25
Line Regulation, PFM/PWM Operation	I_O = 1 A, MODE = Low	図 10-26
Switching Waveforms (TPS63805, TPS63806,TPS63807)		
Switching Waveforms, PFM Boost Operation	V_I = 2.3 V, V_O = 3.3 V, MODE = Low	図 10-27
Switching Waveforms, PFM Buck-Boost Operation	V_I = 3.3 V, V_O = 3.3 V, MODE = Low	図 10-28
Switching Waveforms, PFM Buck Operation	V_I = 4.3 V, V_O = 3.3 V, MODE = Low	図 10-29
Switching Waveforms, PWM Boost Operation	V_I = 2.3 V, V_O = 3.3 V, MODE = High	図 10-30
Switching Waveforms, PWM Buck-Boost Operation	V_I = 3.3 V, V_O = 3.3 V, MODE = High	図 10-31
Switching Waveforms, PWM Buck Operation	V_I = 4.3 V, V_O = 3.3 V, MODE = High	図 10-32
Transient Performance (TPS63805/TPS63807)		
Load Transient, PFM/PWM Boost Operation	V_I = 2.5 V, V_O = 3.3 V, Load = 100 mA to 1A, MODE = Low	図 10-33
Load Transient, PFM/PWM Buck-Boost Operation	V_I = 3.3 V, V_O = 3.3 V, Load = 100 mA to 1A, MODE = Low	図 10-34
Load Transient, PFM/PWM Buck Operation	V_I = 4.2 V, V_O = 3.3V, Load = 100 mA to 1A, MODE = Low	図 10-35

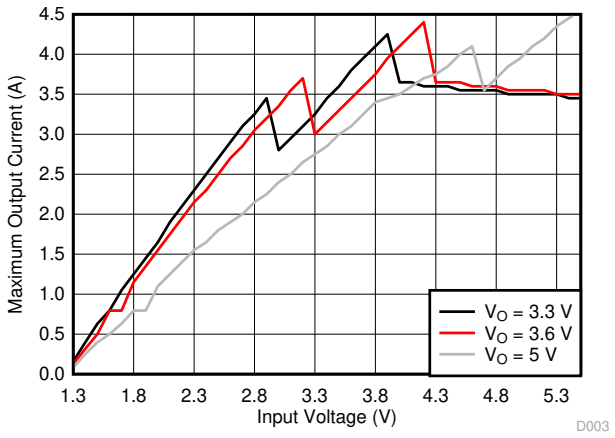
表 10-8. Typical Characteristics Curves (continued)

PARAMETER	CONDITIONS	FIGURE
Load Transient, PWM Boost Operation	V_I = 2.5 V, V_O = 3.3 V, Load = 100 mA to 1A, MODE = High	図 10-36
Load Transient, PWM Buck-Boost Operation	V_I = 3.3 V, V_O = 3.3 V, Load = 100 mA to 1A, MODE = High	図 10-37
Load Transient, PWM Buck Operation	V_I = 4.2 V, V_O = 3.3 V, Load = 100 mA to 1A, MODE = High	図 10-38
Line Transient, PWM Operation	V_I = 2.3 V to 4.3 V, V_O = 3.3 V, Load = 0.5 A , MODE = Low	図 10-39
Line Transient, PWM Operation	V_I = 2.3 V to 4.3 V, V_O = 3.3 V, Load = 1 A , MODE = Low	図 10-40
Line Transient, PWM Operation	V_I = 3 V to 3.6 V, V_O = 3.3 V, Load = 0.5 A , MODE = Low	図 10-41
Transient Performance (TPS63806)		
Load Transient, PFM/PWM Boost Operation	V_I = 2.3 V, V_O = 3.3 V, Load = 25% to 75%, MODE = Low	図 10-42
Load Transient, PFM/PWM Buck-Boost Operation	V_I = 3.3 V, V_O = 3.3 V, Load = 25% to 75%, MODE = Low	図 10-43
Load Transient, PFM/PWM Buck Operation	V_I = 4.3 V, V_O = 3.3 V, Load = 25% to 75%, MODE = Low	図 10-44
Load Transient, PWM Boost Operation	V_I = 2.3 V, V_O = 3.3 V, Load = 25% to 75%, MODE = High	図 10-45
Load Transient, PWM Buck-Boost Operation	V_I = 3.3 V, V_O = 3.3 V, Load = 25% to 75%, MODE = High	図 10-46
Load Transient, PWM Buck Operation	V_I = 4.3 V, V_O = 3.3 V, Load = 25% to 75%, MODE = High	図 10-47
Line Transient, PWM Operation	V_I = 2.3 V to 4.3 V, V_O = 3.3 V, Load = 0.5 A , MODE = Low	図 10-48
Line Transient, PWM Operation	V_I = 2.3 V to 4.3 V, V_O = 3.3 V, Load = 1 A , MODE = Low	図 10-49
Line Transient, PWM Operation	V_I = 3 V to 3.6 V, V_O = 3.3 V, Load = 0.5 A , MODE = Low	図 10-50
Pulsed load, PWM Operation	V_I = 2.8 V, V_O = 3.3 V, Load = 50 mA to 5 A, with 1 MHz and 50% duty cycle, t_r = 120 ns, t_f = 60 ns, MODE = High	図 10-51
Pulsed load, PWM Operation	V_I = 3.3 V, V_O = 3.3 V, Load = 50 mA to 5 A, with 1 MHz and 50% duty cycle, t_r = 120 ns, t_f = 60 ns, MODE = High	図 10-52
Pulsed load, PWM Operation	V_I = 4.2 V, V_O = 3.3 V, Load = 50 mA to 5 A, with 1 MHz and 50% duty cycle, t_r = 120 ns t_f = 60 ns, MODE = High	図 10-53
Start-up (TPS63805, TPS63806,TPS63807)		
Start-up Behavior from Rising Enable, PFM Operation	V_I = 2.2 V, V_O = 3.3 V, Load = 10 mA, MODE = Low	図 10-54
Start-up Behavior from Rising Enable, PWM Operation	V_I = 2.2 V, V_O = 3.3 V, Load = 10 mA, MODE = High	図 10-55



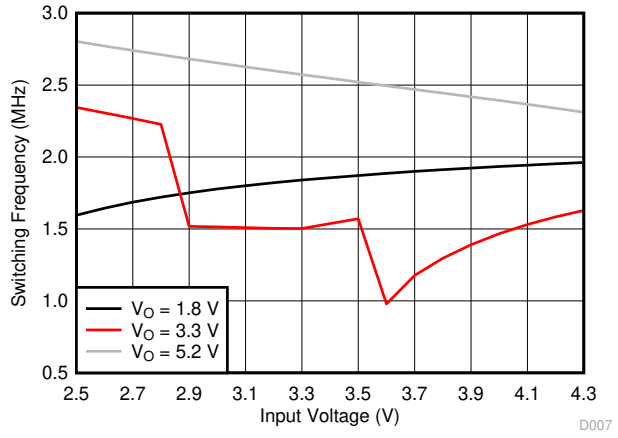
MODE = High TPS63805

図 10-3. Typical Output Current Capability versus Input Voltage



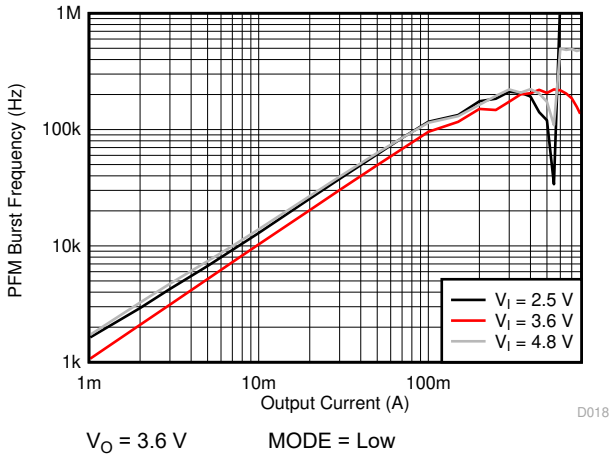
MODE = High TPS63806

図 10-4. Typical Output Current Capability versus Input Voltage



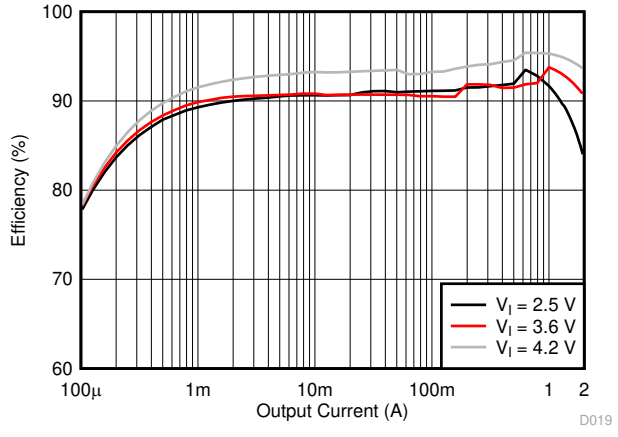
IO = 0 A MODE = High VI rising

図 10-5. Typical Inductor Switching Frequency versus Input Voltage



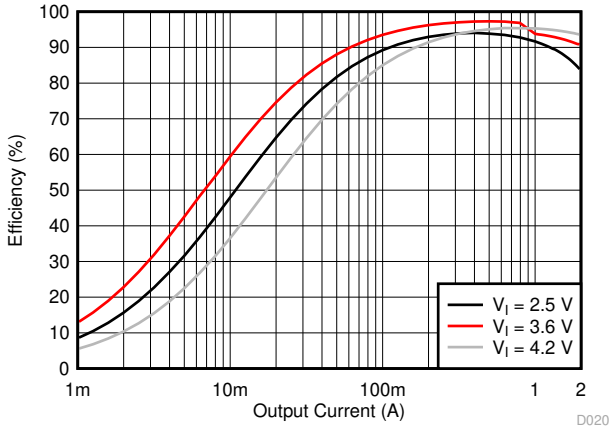
VO = 3.6 V MODE = Low

図 10-6. Typical Inductor Burst Frequency versus Output Current



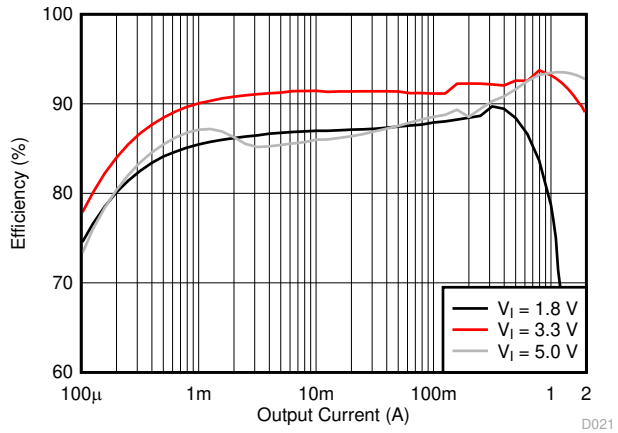
VO = 3.3 V MODE = Low TPS63805

図 10-7. Efficiency versus Output Current (PFM/PWM)



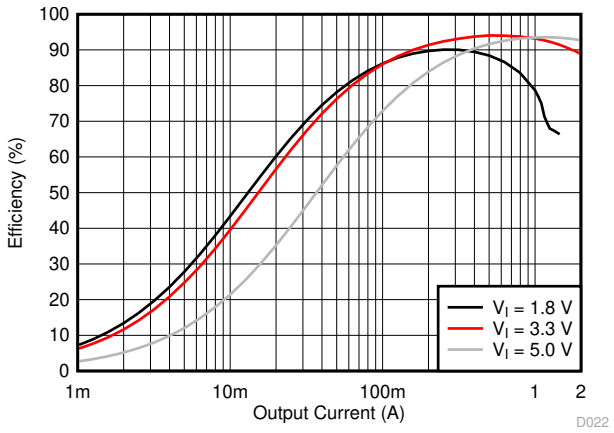
VO = 3.3 V MODE = High TPS63805

図 10-8. Efficiency versus Output Current (PWM Only)



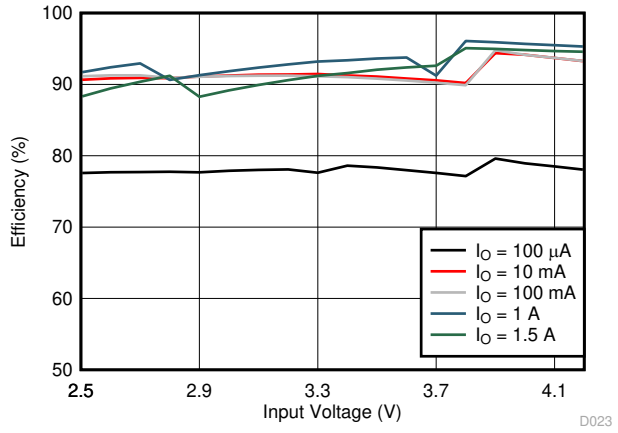
V_O = 3.3 V MODE = Low TPS63805

図 10-9. Efficiency versus Output Current (PFM/ PWM)



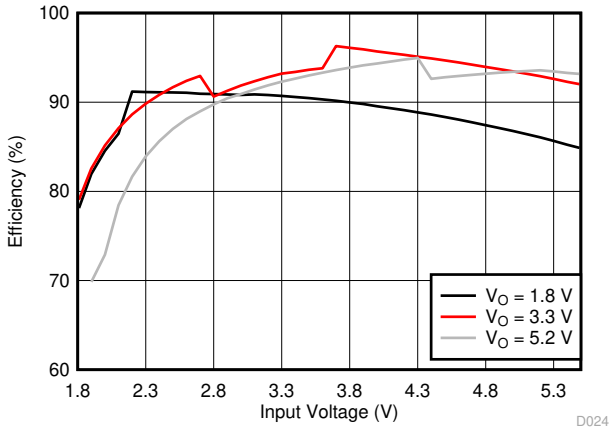
V_O = 3.3 V MODE = High TPS63805

図 10-10. Efficiency versus Input Voltage (PWM Only)



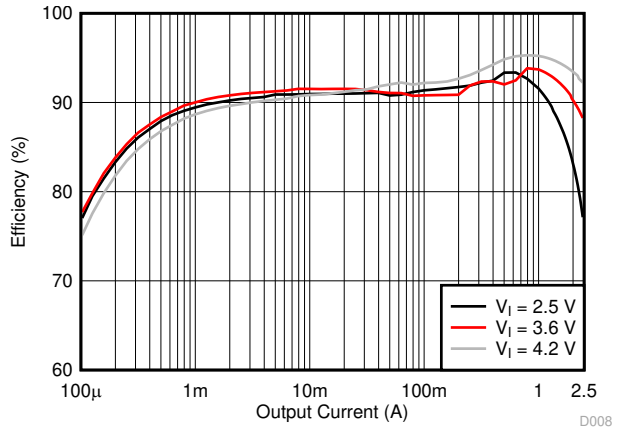
V_O = 3.3 V MODE = Low TPS63805

図 10-11. Efficiency versus Input Voltage (PFM/ PWM)



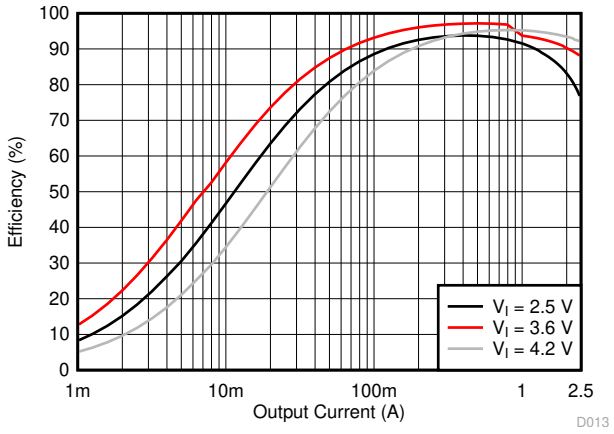
I_O = 1 A MODE = Low TPS63805

図 10-12. Efficiency versus Input Voltage (PWM Only)



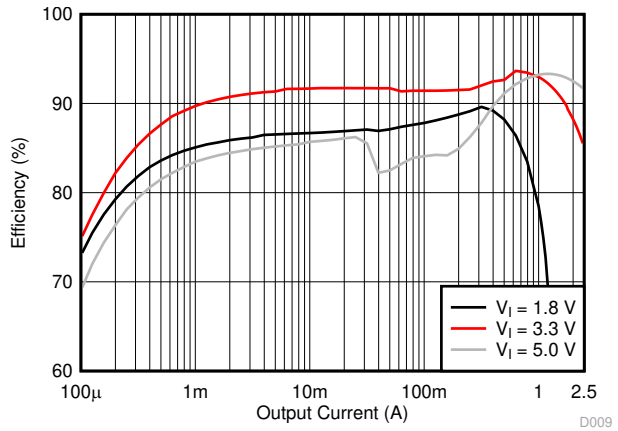
V_O = 3.3 V MODE = High TPS63806

図 10-13. Efficiency versus Output Current (PFM/ PWM)



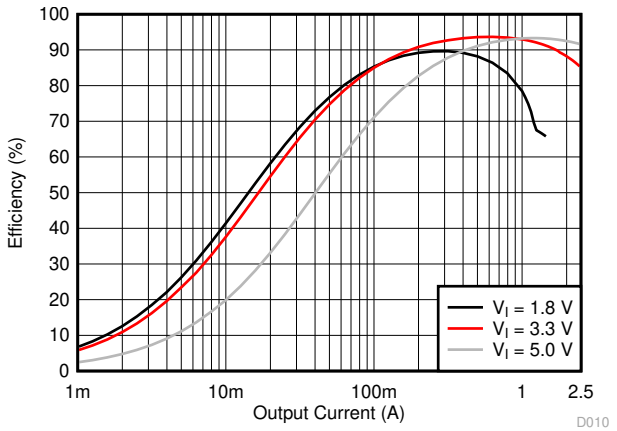
V_O = 3.3 V MODE = Low TPS63806

図 10-14. Efficiency versus Output Current (PWM Only)



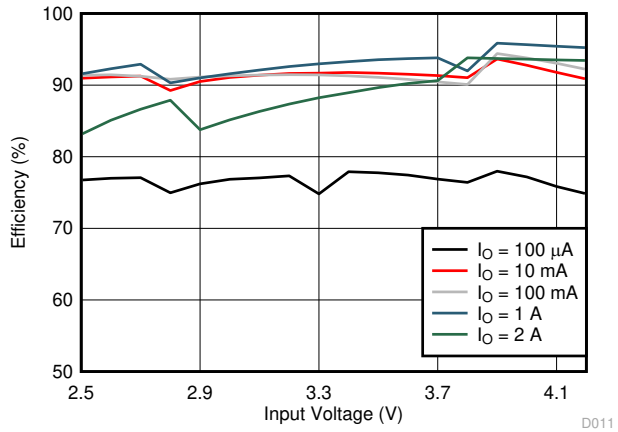
V_O = 3.3 V MODE = High TPS63806

図 10-15. Efficiency versus Output Current (PFM/PWM)



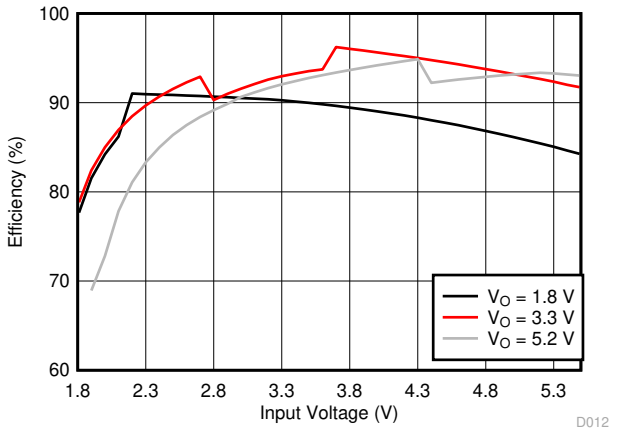
V_O = 3.3 V MODE = Low TPS63806

図 10-16. Efficiency versus Input Voltage (PWM Only)



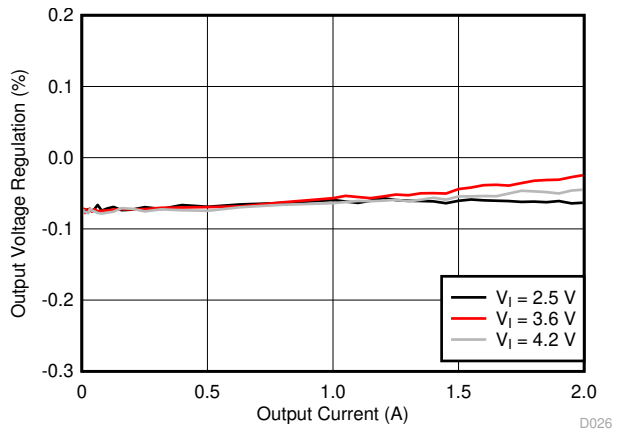
V_O = 3.3 V MODE = High TPS63806

図 10-17. Efficiency versus Input Voltage (PFM/PWM)



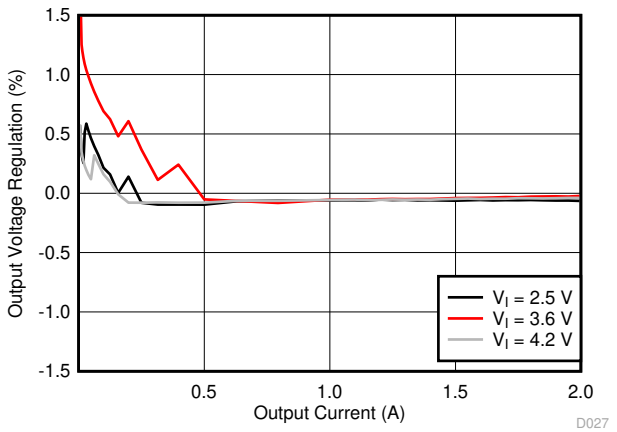
I_O = 1 A MODE = Low TPS63806

図 10-18. Efficiency versus Input Voltage (PWM Only)



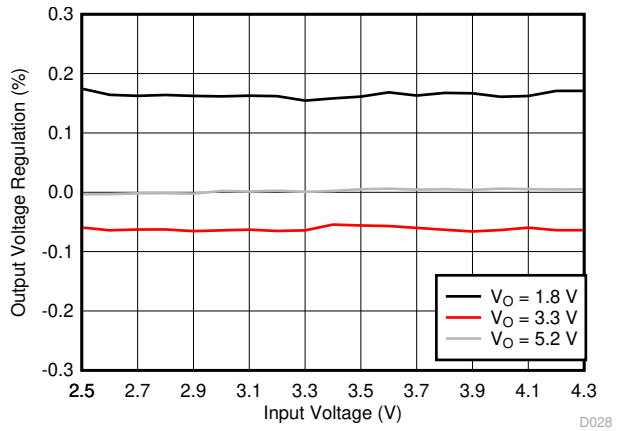
V_O = 3.3 V MODE = High TPS63805

図 10-19. Load Regulation (PWM Only)



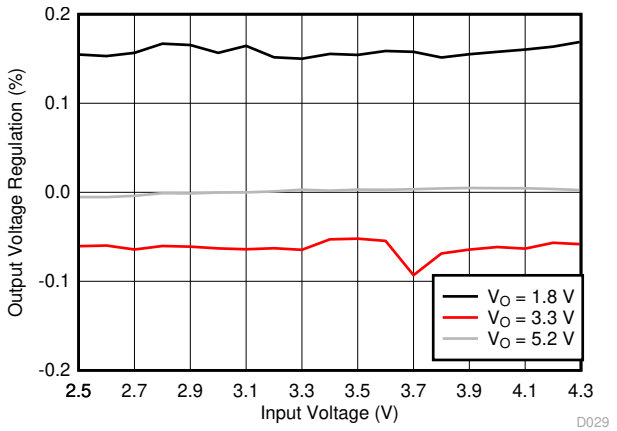
V_O = 3.3 V MODE = Low TPS63805

図 10-20. Load Regulation (PFM/PWM)



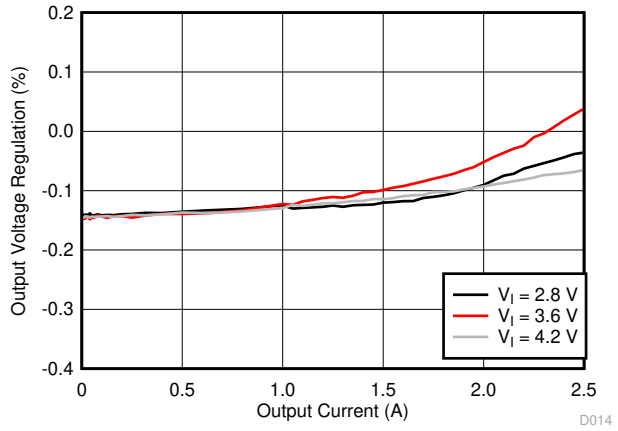
I_O = 1 A MODE = Low TPS63805

図 10-21. Line Regulation (PWM Only)



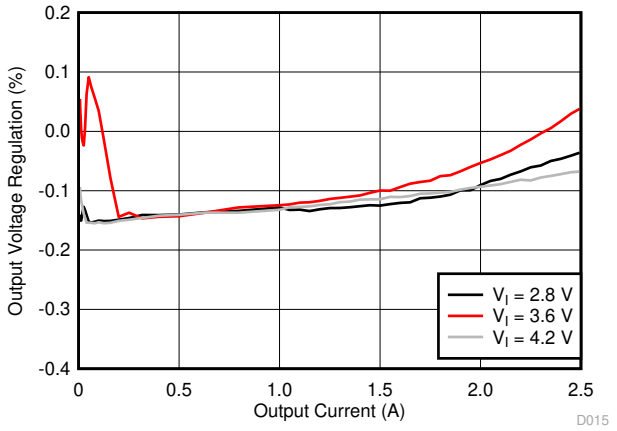
I_O = 1 A MODE = High TPS63805

図 10-22. Line Regulation (PFM/PWM)



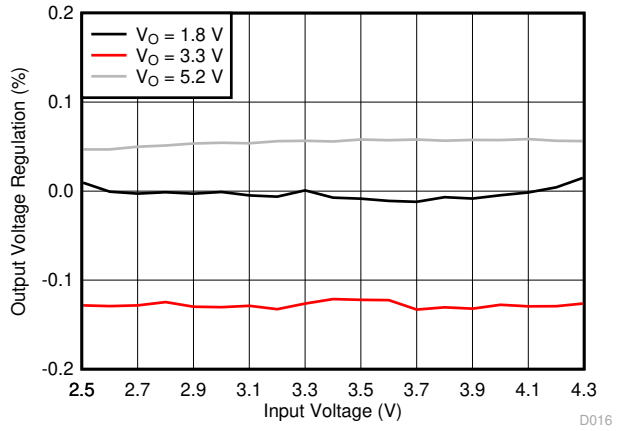
V_O = 3.3 V MODE = High TPS63806

図 10-23. Load Regulation (PWM Only)



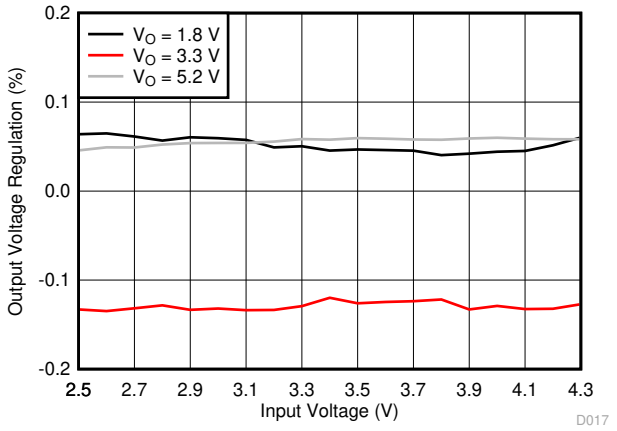
V_O = 3.3 V MODE = Low TPS63806

図 10-24. Load Regulation (PFM/PWM)



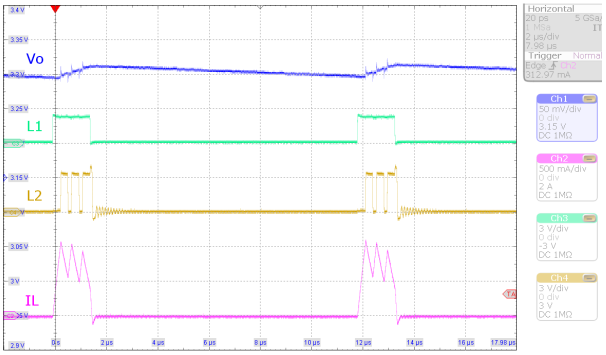
I_O = 1 A MODE = Low TPS63806

図 10-25. Line Regulation (PWM Only)



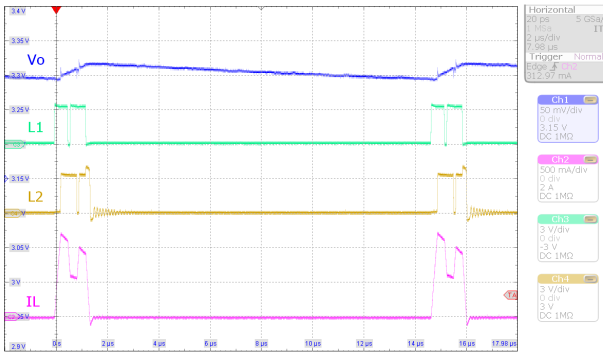
I_O = 1 A MODE = High TPS63806

図 10-26. Line Regulation (PFM/PWM)



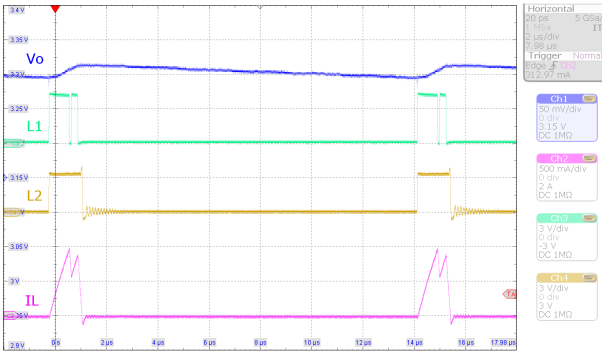
V_I = 2.3 V, V_O = 3.3 V MODE = Low I_O = 40 mA

図 10-27. Switching Waveforms, PFM Boost Operation



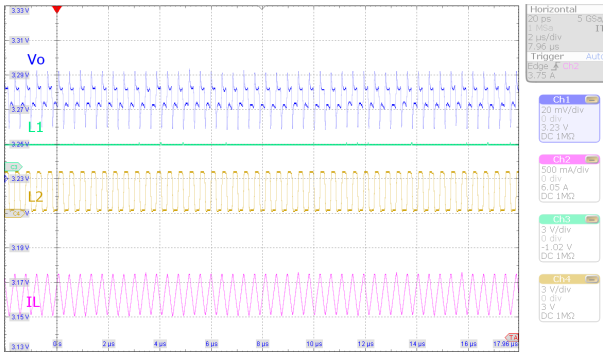
V_I = 3.3 V, V_O = 3.3 V MODE = Low I_O = 40 mA

図 10-28. Switching Waveforms, PFM Buck-Boost Operation



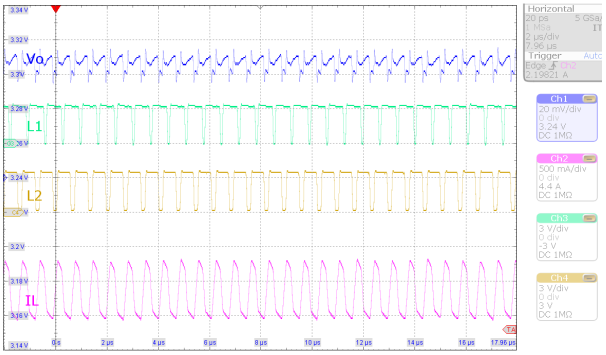
V_I = 4.2 V, V_O = 3.3 V MODE = Low I_O = 40 mA

図 10-29. Switching Waveforms, PFM Buck Operation



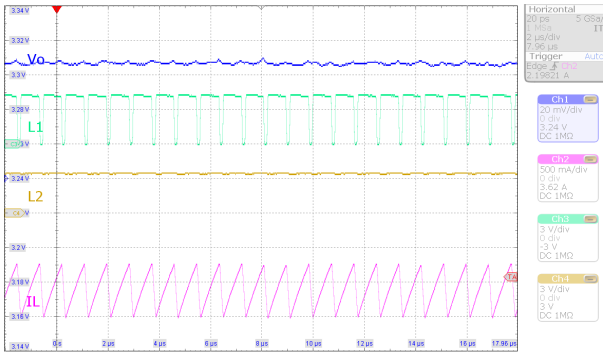
V_I = 2.3 V, V_O = 3.3 V MODE = Low I_O = 2 A

図 10-30. Switching Waveforms, PWM Boost Operation



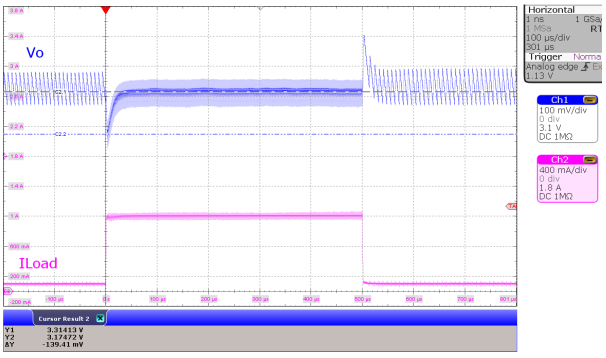
V_I = 3.3 V, V_O = 3.3 V MODE = Low I_O = 2 A

図 10-31. Switching Waveforms, PWM Buck-Boost Operation



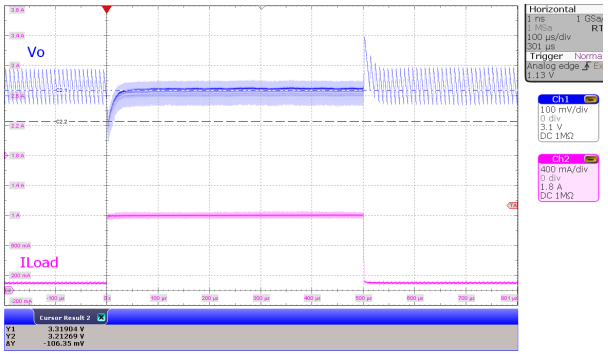
V_I = 4.2 V, V_O = 3.3 V MODE = Low I_O = 2 A

図 10-32. Switching Waveforms, PWM Buck Operation



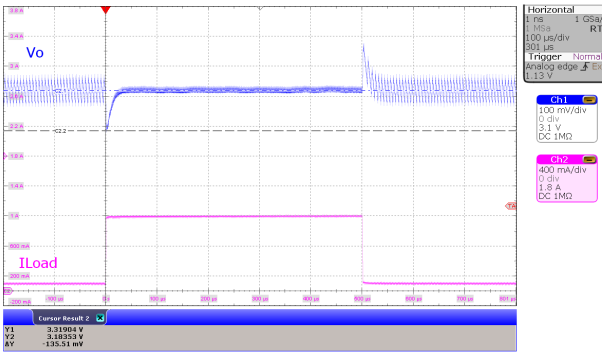
V_I = 2.5 V, V_O = 3.3 V | I_O from 100 mA to 1 A t_r = 1 µs, t_f = 1 µs | TPS63805 MODE = Low

図 10-33. Load Transient, PFM/PWM Boost Operation



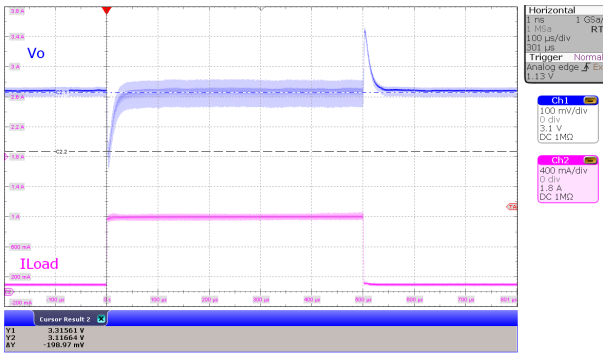
V_I = 3.3 V, V_O = 3.3 V | I_O from 100 mA to 1 A t_r = 1 µs, t_f = 1 µs | TPS63805 MODE = Low

図 10-34. Load Transient, PFM/PWM Buck-Boost Operation



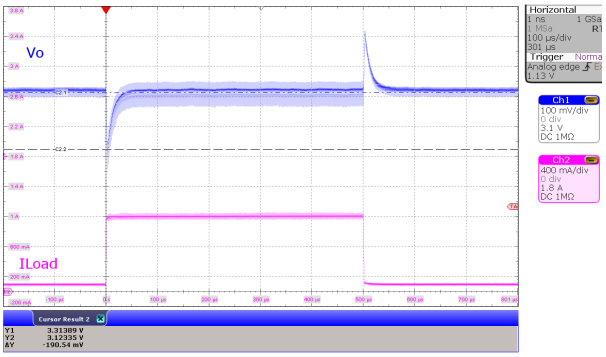
V_I = 5 V, V_O = 3.3 V | I_O from 100 mA to 1 A t_r = 1 µs, t_f = 1 µs | TPS63805 MODE = Low

図 10-35. Load Transient, PFM/PWM Buck Operation



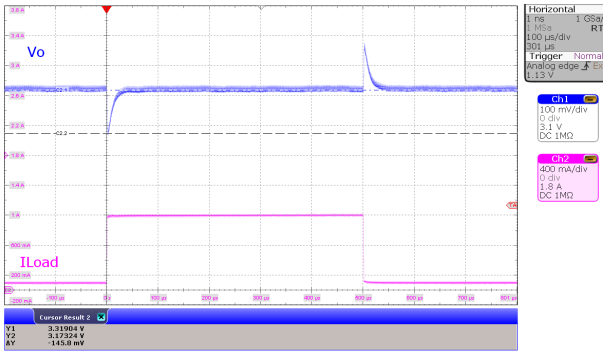
V_I = 2.5 V, V_O = 3.3 V | I_O from 100 mA to 1 A t_r = 1 µs, t_f = 1 µs | TPS63805 MODE = High

図 10-36. Load Transient, PWM Boost Operation



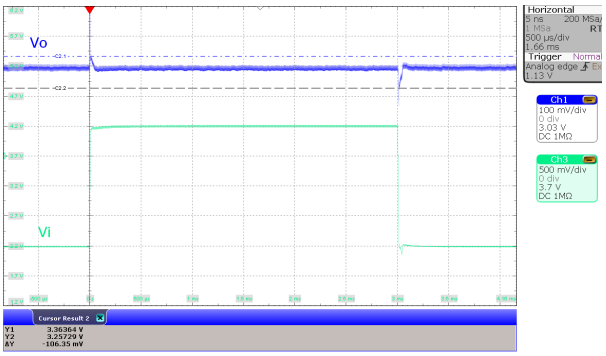
V_I = 3.3 V, V_O = 3.3 V | I_O from 100 mA to 1 A t_r = 1 µs, t_f = 1 µs | TPS63805 MODE = High

図 10-37. Load Transient, PWM Buck-Boost Operation



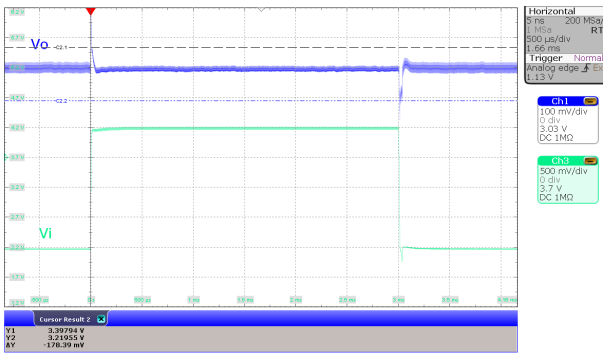
V_I = 5 V, V_O = 3.3 V | I_O from 100 mA to 1 A t_r = 1 µs, t_f = 1 µs | TPS63805 MODE = High

図 10-38. Load Transient, PWM Buck Operation



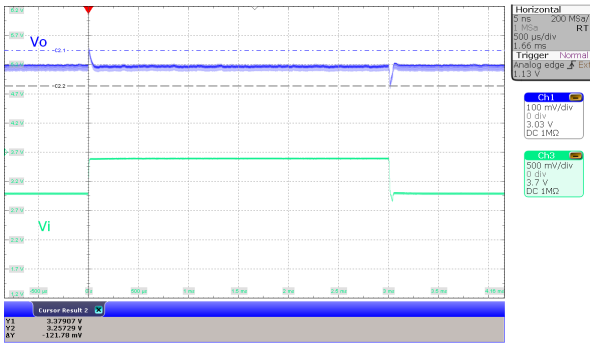
I_O = 0.5 A | V_I from 2.2 V to 4.2 V t_r =1 µs, t_f = 1 µs | TPS63805 MODE = High

図 10-39. Line Transient, PWM Operation



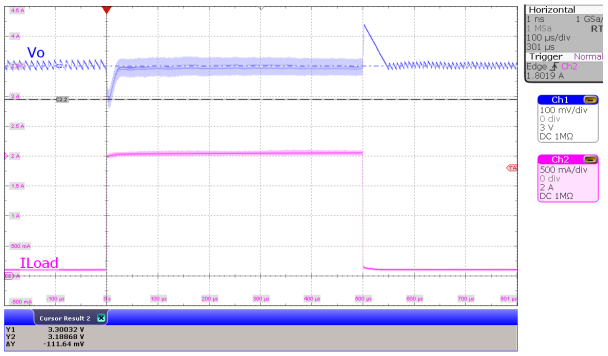
I_O = 1 A | V_I from 2.2 V to 4.2 V t_r = 1 µs, t_f = 1 µs | TPS63805 MODE = High

図 10-40. Line Transient, PWM Operation



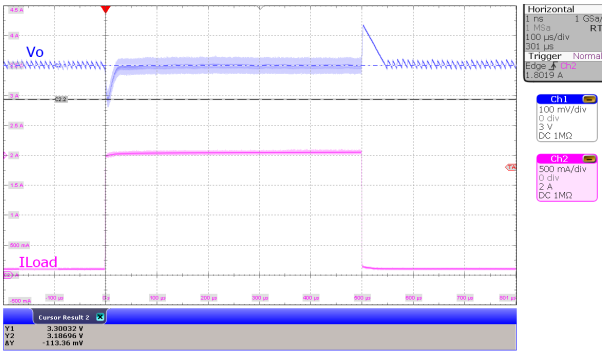
I_O = 0.5 A | V_I from 3 V to 3.6 V t_r = 1 µs, t_f = 1 µs | TPS63805 MODE = High

図 10-41. Line Transient, PWM Operation



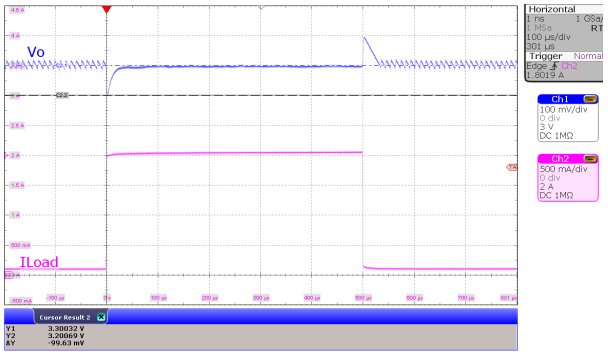
V_I = 2.8 V, V_O = 3.3 V | I_O from 100 mA to 2 A t_r = 1 µs, t_f = 1 µs | TPS63806 MODE = Low

図 10-42. Load Transient, PFM/PWM Boost Operation



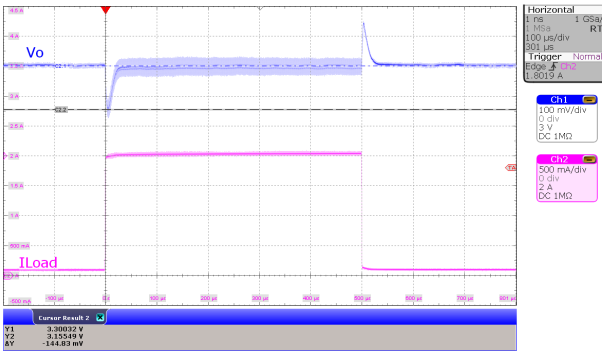
V_I = 3.3 V, V_O = 3.3 V | I_O from 100 mA to 2 A t_r = 1 µs, t_f = 1 µs | TPS63806 MODE = Low

図 10-43. Load Transient, PFM/PWM Buck-Boost Operation



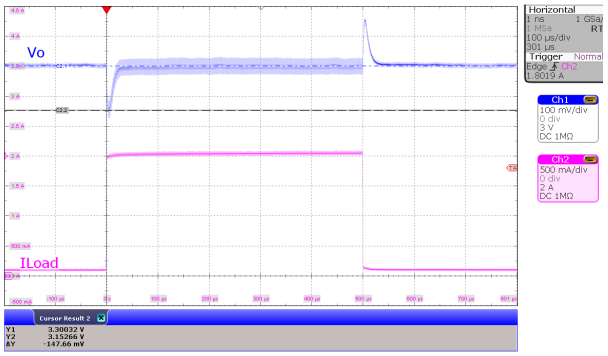
V_I = 4.2 V, V_O = 3.3 V | I_O from 100 mA to 2 A t_r = 1 µs, t_f = 1 µs | TPS63806 MODE = Low

図 10-44. Load Transient, PFM/PWM Buck Operation



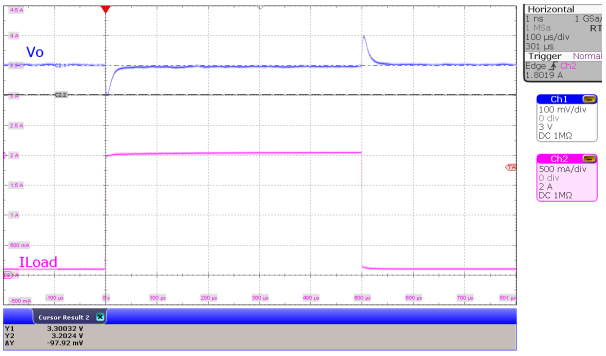
V_I = 2.8 V, V_O = 3.3 V | I_O from 100 mA to 2 A t_r = 1 µs, t_f = 1 µs | TPS63806 MODE = High

図 10-45. Load Transient, PWM Boost Operation



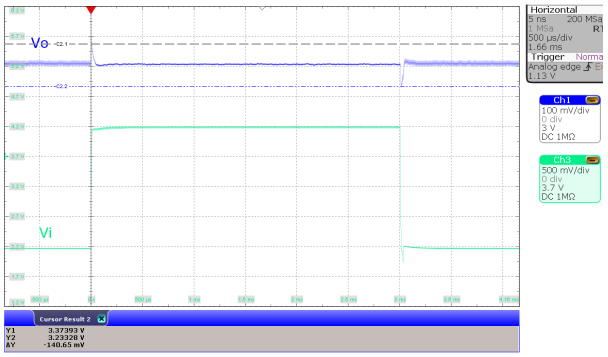
V_I = 3.3 V, V_O = 3.3 V | I_O 100 mA to 2 A t_r = t_f = 1 µs | TPS63806 MODE = High

図 10-46. Load Transient, PWM Buck-Boost Operation



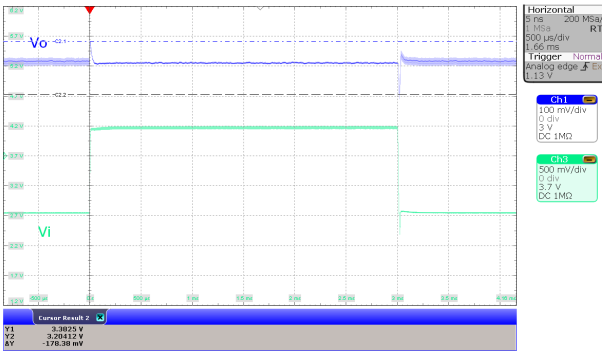
V_I = 4.2 V, V_O = 3.3 V | I_O 100 mA to 2 A t_r = t_f = 1 µs | TPS63806 MODE = High

図 10-47. Load Transient, PWM Buck Operation



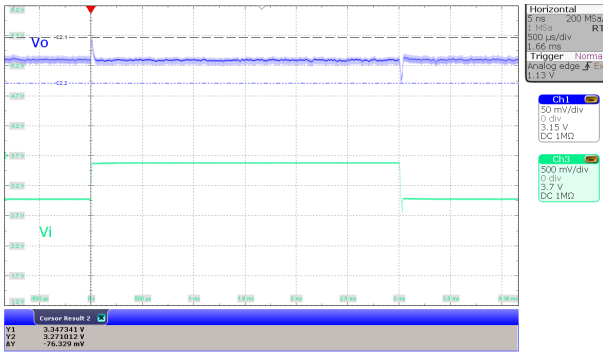
I_O = 1 A | V_I 2.2 V to 4.2 V t_r = t_f = 1 µs | TPS63806 MODE = High

図 10-48. Line Transient, PWM Operation



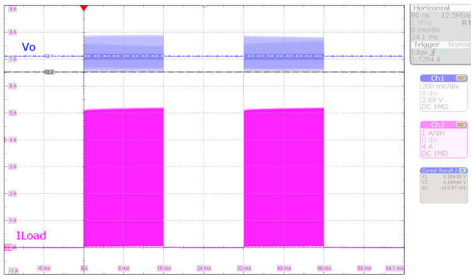
I_O = 2 A | V_I 2.2 V to 4.2 V t_r = t_f = 1 µs | TPS63806 MODE = High

図 10-49. Line Transient, PWM Operation



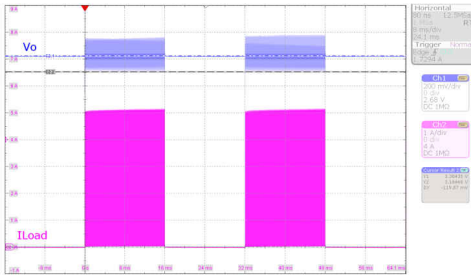
I_O = 1 A | V_I 3.0 V to 3.6 V t_r = t_f = 1 µs | TPS63806 MODE = High

図 10-50. Line Transient, PWM Operation



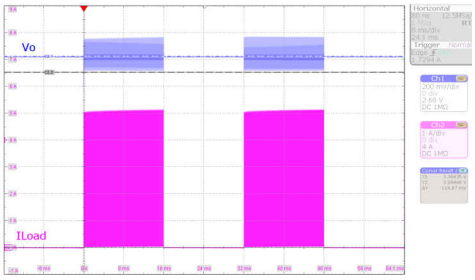
V_I = 2.8 V, V_O = 3.3 V	I_O 50 mA to 5 A with 1 MHz and 50% duty cycle t_r = 120 ns, t_f = 60 ns	TPS63806 MODE = High

図 10-51. Pulsed Load, PWM Operation



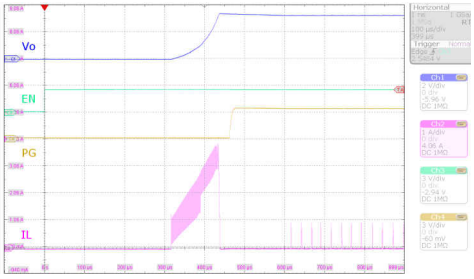
V_I = 3.3 V, V_O = 3.3 V	I_O 50 mA to 5 A with 1 MHz and 50% duty cycle t_r = 120 ns, t_f = 60 ns	TPS63806 MODE = High

図 10-52. Pulsed Load, PWM Operation



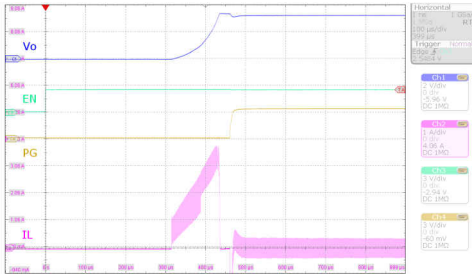
V_I = 4.2 V, V_O = 3.3 V	I_O 50 mA to 5 A with 1 MHz and 50% duty cycle t_r = 120 ns, t_f = 60 ns	TPS63806 MODE = High

図 10-53. Pulsed Load, PWM Operation



V_I = 4.2 V, V_O = 3.3 V	MODE = Low	100 mΩ resistive load

図 10-54. Start-up Behavior from Rising Enable, PFM Operation



V_I = 4.2 V, V_O = 3.3 V	MODE = High	100 mΩ resistive load

図 10-55. Start-up Behavior from Rising Enable, PWM Operation

11 Power Supply Recommendations

The TPS63805, TPS63806, and TPS63807 device families have no special requirements for its input power supply. The input power supply output current needs to be rated according to the supply voltage, output voltage, and output current of the TPS63805, TPS63806, and TPS63807.

12 Layout

12.1 Layout Guidelines

The PCB layout is an important step to maintain the high performance of the TPS63805, TPS63806, and TPS63807 device.

1. Place input and output capacitors as close as possible to the IC. Traces need to be kept short. Route wide and direct traces to the input and output capacitor results in low trace resistance and low parasitic inductance.
2. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.
3. Use separate traces for the supply voltage of the power stage and the supply voltage of the analog stage.
4. The sense trace connected to FB is signal trace. Keep these traces away from L1 and L2 nodes.

12.2 Layout Example

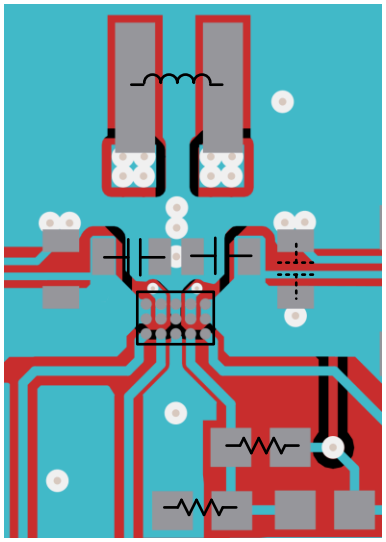


図 12-1. TPS63805, TPS63806, and TPS63807 Layout

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

13.1.2 Development Support

QFN/SON Package FAQs

13.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS63805/TPS63807 device with the WEBENCH® Power Designer. Click here to create a custom design using the TPS63806 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

13.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS63805YFFR	ACTIVE	DSBGA	YFF	15	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS63805	Samples
TPS63805YFFT	ACTIVE	DSBGA	YFF	15	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS63805	Samples
TPS63806YFFR	ACTIVE	DSBGA	YFF	15	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS63806	Samples
TPS63807YFFR	ACTIVE	DSBGA	YFF	15	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS63807	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

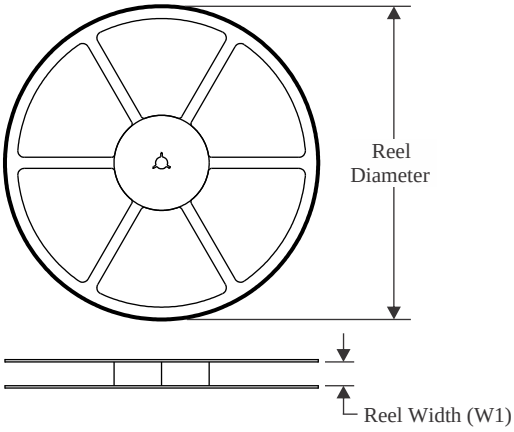
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

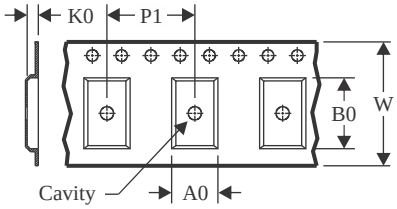
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

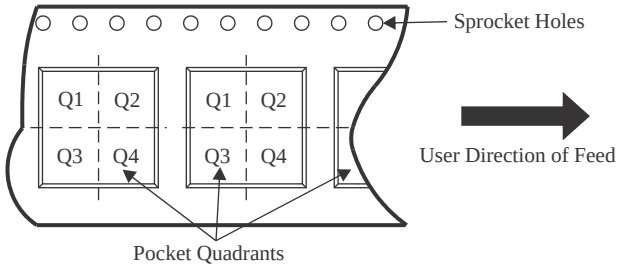


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

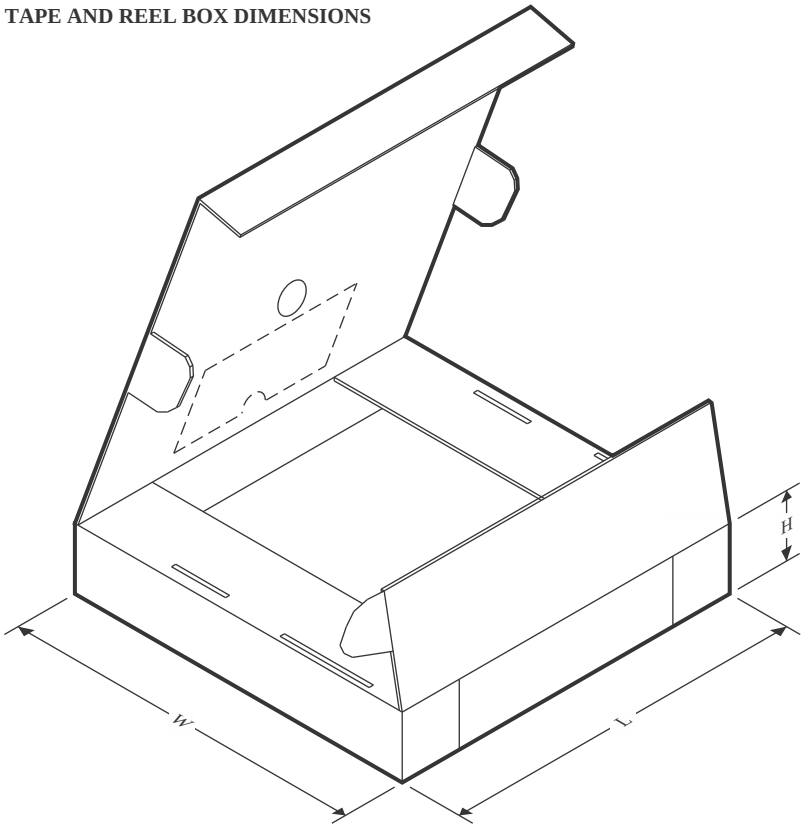
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS63805YFFR	DSBGA	YFF	15	3000	180.0	8.4	1.5	2.42	0.75	4.0	8.0	Q1
TPS63805YFFT	DSBGA	YFF	15	250	180.0	8.4	1.5	2.42	0.75	4.0	8.0	Q1
TPS63806YFFR	DSBGA	YFF	15	3000	180.0	8.4	1.5	2.42	0.75	4.0	8.0	Q1
TPS63807YFFR	DSBGA	YFF	15	3000	180.0	8.4	1.5	2.42	0.75	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

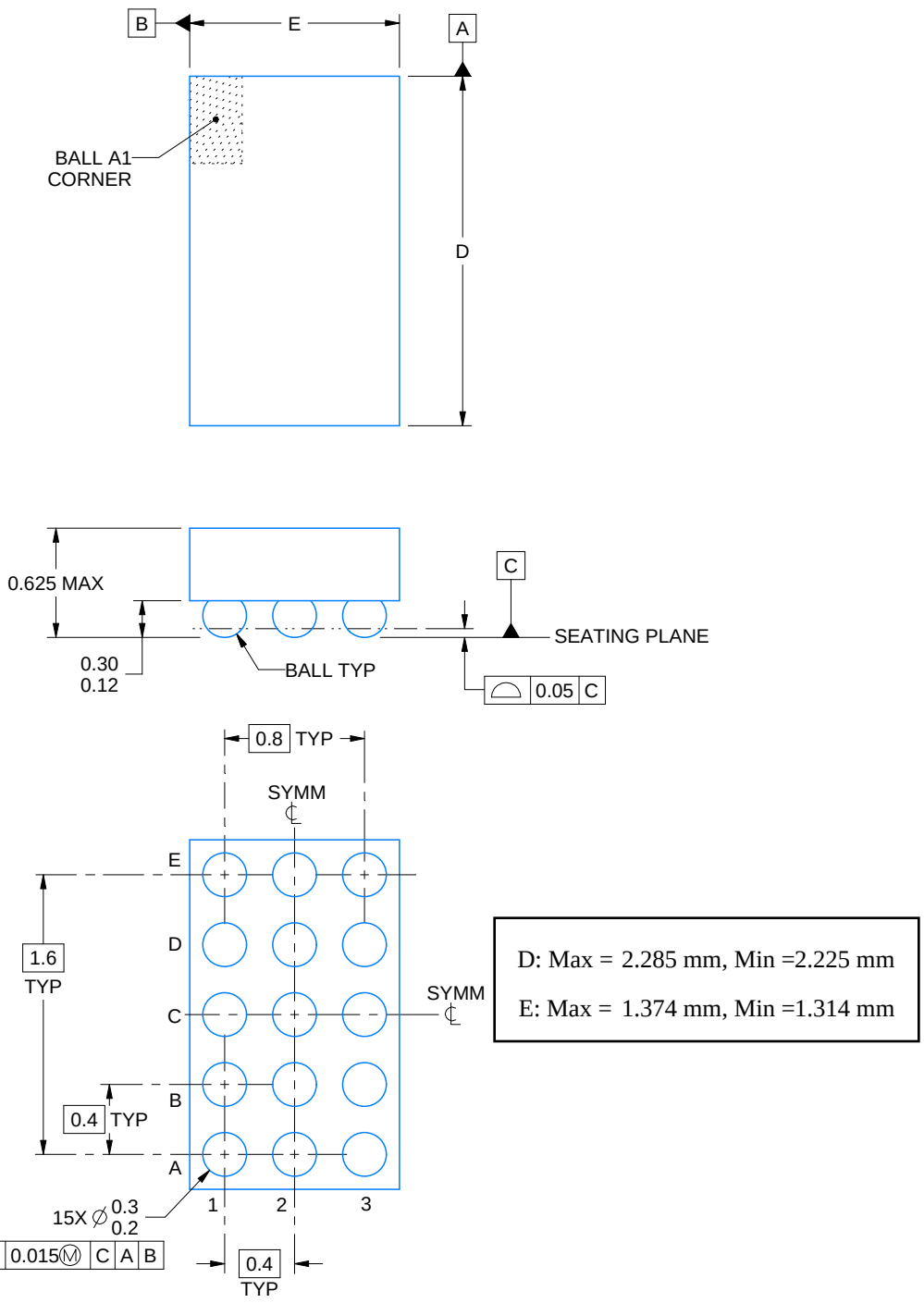
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS63805YFFR	DSBGA	YFF	15	3000	182.0	182.0	20.0
TPS63805YFFT	DSBGA	YFF	15	250	182.0	182.0	20.0
TPS63806YFFR	DSBGA	YFF	15	3000	182.0	182.0	20.0
TPS63807YFFR	DSBGA	YFF	15	3000	182.0	182.0	20.0

PACKAGE OUTLINE

YFF0015

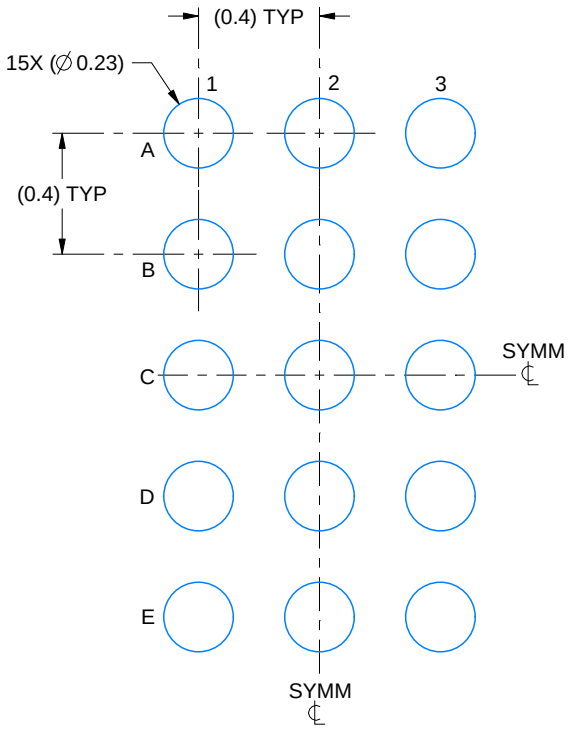
DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY

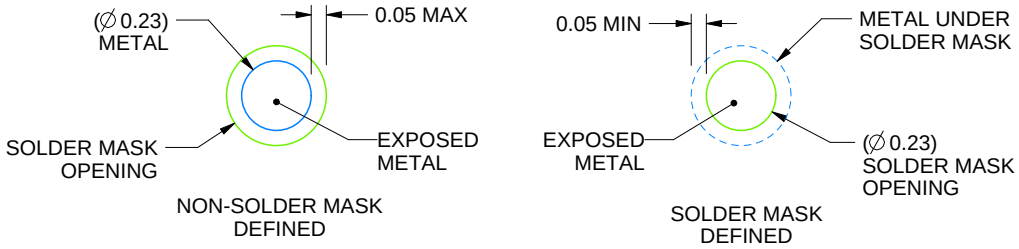


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219378/B 05/2020

NOTES: (continued)

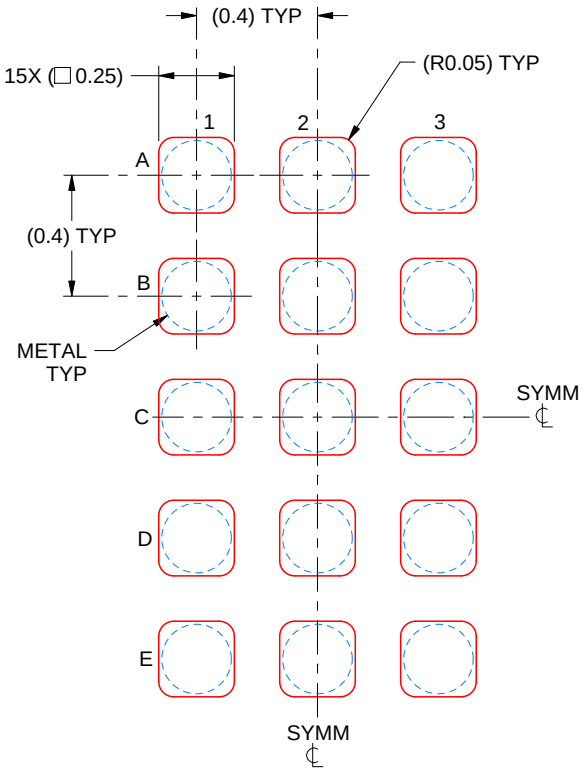
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFF0015

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219378/B 05/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265