TPS65197x: 電荷共有なし/2チャネル電荷共有/3チャネル電荷共有を選択可能でシャットダウン中のVGHへのパネル放電に対応した8チャネル・レベル・シフタ

1 特長

- 8チャネル・レベル・シフタ(STV、RESET、6×CLK)
- 16.5V～45Vの高出力電圧レベル(VGH)
- 最低–20Vの低出力電圧レベル(VGL)
- 電荷共有を選択可能
  - 電荷共有なし
  - 2チャネル電荷共有
  - 3チャネル電荷共有
- 2チャネル・パネル放電
- T-CON障害検出
  - TPS65197: STVパルスによるロジック・リセット
  - TPS65197B: ロジックのリセットなし
- ラッチ・シャットダウン検出(VGHへのクロック)
- 100kHzのクロック動作周波数に対応
- 28ピン4mm×4mmのQFNパッケージ

2 アプリケーション

- ゲート・イン・パネル(GIP) LCD
  - ノートPC
  - モニタ
  - テレビ

3 概要

TPS65197/Bは、ノートPC、モニタ、テレビなどのLCDディスプレイ・アプリケーションに適した、放電機能付きの8チャネル・レベル・シフタです。

タイミング・コントローラ(T-CON)の論理レベル信号を、ゲート・イン・パネル(GIP)ディスプレイが必要とする高レベル信号に変換します。

クロック出力CLKOUTxが通常レベルのシフト動作と2チャネルまたは3チャネルの電荷共有をサポートしているため、画質の向上と消費電力の削減が可能です。電源切断時には、すべての出力が可能な限り長く、それぞれの入力信号に追従しますが、放電機能を使用すると出力は High(V_{GH})にプルアップされます。

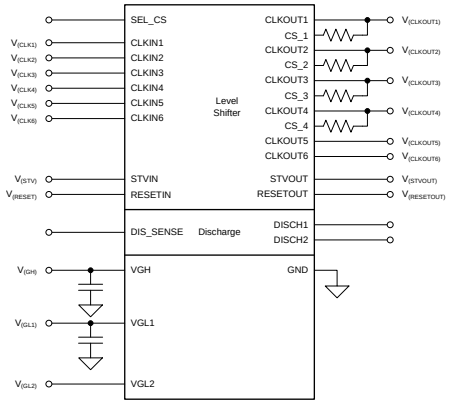
TPS65197はロジック・リセットを実装しているため、STVの立ち上がりエッジにより6つの出力クロックがすべて強制的にVGL1に設定された後、誤ったT-CON信号は無視されます。次のCLKIN1の立ち上がりエッジでロジックのロックが解除され、通常動作がイネーブルになります。TPS65197Bにはロジック・リセットがないため、常時入力信号に追従します。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS65197	WQFN (28)	4.00mm×4.00mm
TPS65197B	WQFN (28)	4.00mm×4.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

4 概略回路図



目次

5 改訂履歴

Revision C (May 2017) から **Revision D** に変更 **Page**

- データシートの最初の公開リリース ... 1

Revision B (July 2015) から **Revision C** に変更 **Page**

- Changed V_{IH} MIN value from 2 to 1.65 in the INPUT SIGNALS section of the Electrical Characteristics table ... 5

Revision A (June 2015) から **Revision B** に変更 **Page**

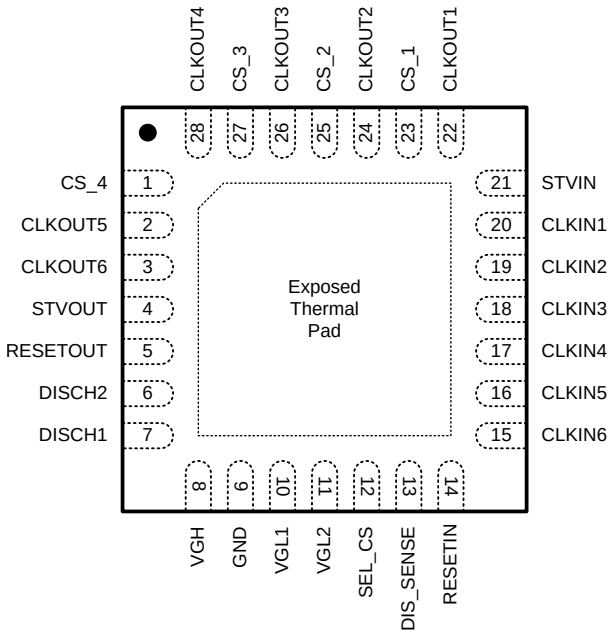
- 概略回路図を変更、TPS65197Bを 追加 ... 1

2012年4月 発行のものから更新 **Page**

- ESD定格の表、タイミング要件の表、「機能説明」セクション、「デバイスの機能モード」、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 ... 1
- TPS65197B 追加 ... 1
- Changed the text in the first paragraph of *Output Clock Behavior* ... 10
- 追加「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクション ... 20

6 Pin Configuration and Functions

RUY Package
28-Pin WQFN With Thermal Pad
Top View



Pin Functions

PIN		I/O/P	DESCRIPTION
NAME	NUMBER		
CLKIN1	20	I	Clock 1 input
CLKIN2	19	I	Clock 2 input
CLKIN3	18	I	Clock 3 input
CLKIN4	17	I	Clock 4 input
CLKIN5	16	I	Clock 5 input
CLKIN6	15	I	Clock 6 input
CLKOUT1	22	I/O	Clock 1 output
CLKOUT2	24	I/O	Clock 2 output
CLKOUT3	26	I/O	Clock 3 output
CLKOUT4	28	I/O	Clock 4 output
CLKOUT5	2	I/O	Clock 5 output
CLKOUT6	3	I/O	Clock 6 output
CS_1	23	I/O	Clock 1 charge-sharing input
CS_2	25	I/O	Clock 2 charge-sharing input
CS_3	27	I/O	Clock 3 charge-sharing input
CS_4	1	I/O	Clock 4 charge-sharing input
DISCH1	7	I/O	Discharge 1 output. Internally connected to VGL1 and VGH
DISCH2	6	I/O	Discharge 2 output. Internally connected to VGL2 and VGH
DIS_SENSE	13	I	Discharge sense terminal
GND	9	–	Ground
RESETIN	14	I	RESET input
RESETOUT	5	I/O	RESET output

Pin Functions (continued)

PIN		I/O/P	DESCRIPTION
NAME	NUMBER		
SEL_CS	12	I	Charge-sharing method-selection terminal. When left floating or pulled to GND, charge-sharing is disabled.
STVIN	21	I	STV input
STVOUT	4	I/O	STV output
VGH	8	P	Positive supply voltage. Place a buffer capacitor close to this terminal.
VGL1	10	P	Negative supply voltage for all outputs except discharge 2. Place a buffer capacitor close to this terminal.
VGL2	11	P	Negative supply voltage for discharge 2
Thermal pad	–	–	The thermal pad is connected to VGL1.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Terminal voltage(1)	SEL_CS, DIS_SENSE, CLKIN1, CLKIN2, CLKIN3, CLKIN4, CLKIN5, CLKIN6, STVIN, RESETIN	–0.3	7	V
	VGH	–0.3	50	
	VGL1, VGL2	–25	0.3	
	CLKOUT1, CLKOUT2, CLKOUT3, CLKOUT4, CLKOUT5, CLKOUT6, CS_1, CS_2, CS_3, CS_4, STVOUT, RESETOUT, DISCH1, DISCH2	–25	50	
	VGH – VGLx		62	
	$V_{GL1} – V_{GL2}$	–20	0	
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	

(1) With respect to the GND terminal

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±700	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{(GH)}$	Voltage range of positive supply	16.5		45	V
$V_{(GL\_x)}$	Voltage range of negative supply	–20		–3	
$V_{(GH)} – V_{(GL\_x)}$	Voltage difference between $V_{(GH)}$ and $V_{(GL\_x)}$	0		60	
$V_{GL1} – V_{GL2}$	Voltage difference between $V_{(GL1)}$ and $V_{(GL2)}$ ($V_{(GL1)}$ must be more negative than $V_{(GL2)}$)	–20		0	
T_A	Operating free-air temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	

7.4 Thermal Information

THERMAL METRIC(1)		TPS65197/B RUY 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.5	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	25.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	7.5	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	7.5	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	2.5	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

$V_{(GH)}$ = 30 V, $V_{(GL1)}$ = –10 V, $V_{(GL2)}$ = –8 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(GH)}$	Input voltage range $V_{(GH)}$		16.5		45	V
$V_{(GL1)}$	Input voltage range $V_{(GL1)}$		–20		–3	
$V_{(GL2)}$	Input voltage range $V_{(GL2)}$		–20		–3	
$I_{(GH)}$	Positive supply current	CLKINx = STVIN = RESETIN = SEL_CS = 0 V, DIS_SENSE = 5 V		0.3	1	mA
$I_{(GL1)}$	Negative supply current		–0.5	–0.05		
$I_{(GL2)}$	Negative supply current		–0.5	–0.05		
$V_{(UVLO)}$	Undervoltage lockout threshold	$V_{(GH)}$ rising, T_J = –40ºC to 85ºC	13.5	15	16.5	V
		$V_{(GH)}$ falling, T_J = –40ºC to 85ºC	2	3.5	5	
$T_{(SD)}$	Thermal shutdown temperature	T_J rising	130	150	170	°C
INPUT SIGNALS (CLKINx, STVIN, RESETIN, SEL_CS, DIS_SENSE)						
V_{IH}	High-level input voltage CLKINx, STVIN, RESETIN	Input rising	1.65			V
V_{IL}	Low-level input voltage CLKINx, STVIN, RESETIN	Input falling			0.8	
$V_{(SEL\_CS)}$	Charge-sharing-disabled voltage				0.5	
	3-Channel Charge-Sharing voltage		1		2	
	2-Channel Charge-Sharing voltage		2.8		6.5	
$V_{(DIS\_SENSE)}$	Discharge detection threshold	$V_{(DIS\_SENSE)}$ falling, T_J = 0ºC to 85ºC	1.17	1.26	1.36	
I_{IN}	Input current CLKINx, STVIN, RESETIN, DIS_SENSE	CLKINx = STVIN = RESETIN = DIS_SENSE = 5 V		2	100	nA
	Input current SEL_CS	SEL_CS = 5 V		50	100	µA
$R_{(SEL\_CS)}$	SEL_CS pin, internal pulldown resistance		50	100	150	kΩ
LEVEL SHIFTERS (CLKOUT1 to CLKOUT6)						
$r_{DS(on)}$	High-side on-resistance, CLKOUTx	$I_{(OUT)}$ = 10 mA, sourcing (high side)		11	25	Ω
	Low-side on-resistance, CLKOUTx	$I_{(OUT)}$ = 10 mA, sinking (low side)		7	15	
$R_{(CS)}$	Internal charge-sharing resistance	$I_{(CS)}$ = 10 mA, T_J = –40ºC to 85ºC	30	60	100	
LEVEL SHIFTERS (STVOUT, RESETOUT)						
$r_{DS(on)}$	High-side on-resistance STVOUT, RESETOUT	$I_{(OUT)}$ = 10 mA, sourcing (high side)		30	60	Ω
	Low-side on-resistance STVOUT, RESETOUT	$I_{(OUT)}$ = 10 mA, sinking (low side)		15	30	

Electrical Characteristics (continued)

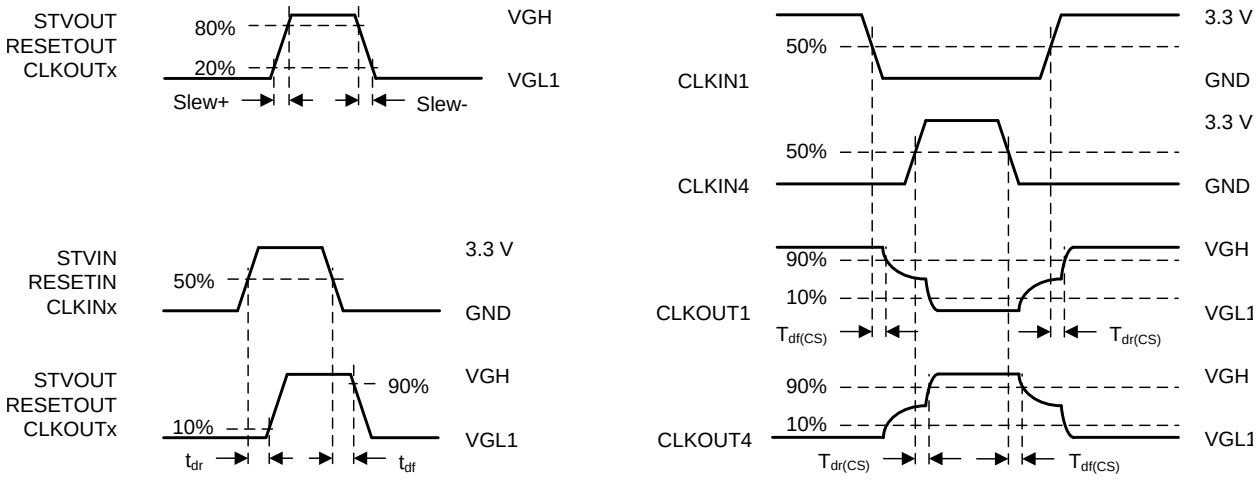
$V_{(GH)}$ = 30 V, $V_{(GL1)}$ = –10 V, $V_{(GL2)}$ = –8 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DISCHARGE OUTPUTS (DISCH1, DISCH2)						
$r_{DS(on)}$	High-side on-resistance, DISCH1	$I_{(OUT)}$ = 10 mA, sourcing (high side)		14	60	Ω
	Low-side on-resistance DISCH1	$I_{(OUT)}$ = 10 mA, sinking (low side)		3	10	
	High-side on-resistance, DISCH2	$I_{(OUT)}$ = 10 mA, sourcing (high side)		14	60	
	Low-side on-resistance DISCH2	$I_{(OUT)}$ = 10 mA, sinking (low side)		10	20	

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
LEVEL SHIFTERS (CLKOUT1 to CLKOUT6)						
Slew+	Slew rate, rising	$C_{(OUT)}$ = 4.7 nF, $V_{(OUT)}$ = 20% to 80%	50	140		V/µs
Slew–	Slew rate, falling		50	150		
t_{dr}	Propagation delay	$V_{(OUT)}$ rising, $C_{(OUT)}$ = 150 pF		40	100	ns
t_{df}		$V_{(OUT)}$ falling, $C_{(OUT)}$ = 150 pF		50	100	
$t_{dr(CS)}$		$V_{(OUT)}$ rising, $C_{(OUT)}$ = 150 pF, $R_{(CS)}$ = 50 Ω		50	150	
$t_{df(CS)}$		$V_{(OUT)}$ falling, $C_{(OUT)}$ = 150 pF, $R_{(CS)}$ = 50 Ω		70	150	
LEVEL SHIFTERS (STVOUT, RESETOUT)						
Slew+	Slew rate, rising	$C_{(OUT)}$ = 4.7 nF, $V_{(OUT)}$ = 20% to 80%	20	50		V/µs
Slew–	Slew rate, falling		30	60		
t_{dr}	Propagation delay	$V_{(OUT)}$ rising, $C_{(OUT)}$ = 150 pF		40	100	ns
t_{df}		$V_{(OUT)}$ falling, $C_{(OUT)}$ = 150 pF		50	100	



7.7 Typical Characteristics

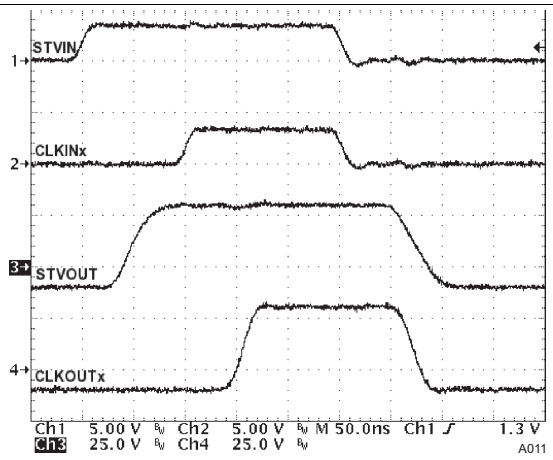


図 1. Propagation Delay, Charge Sharing Disabled

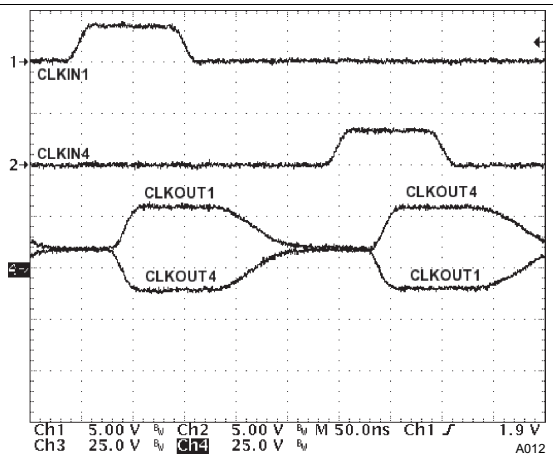


図 2. Propagation Delay, Charge Sharing Enabled

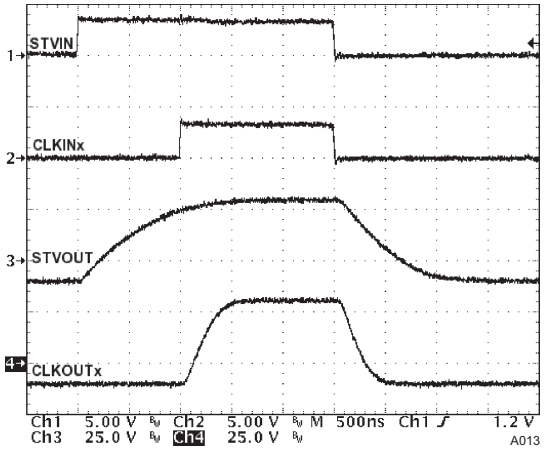


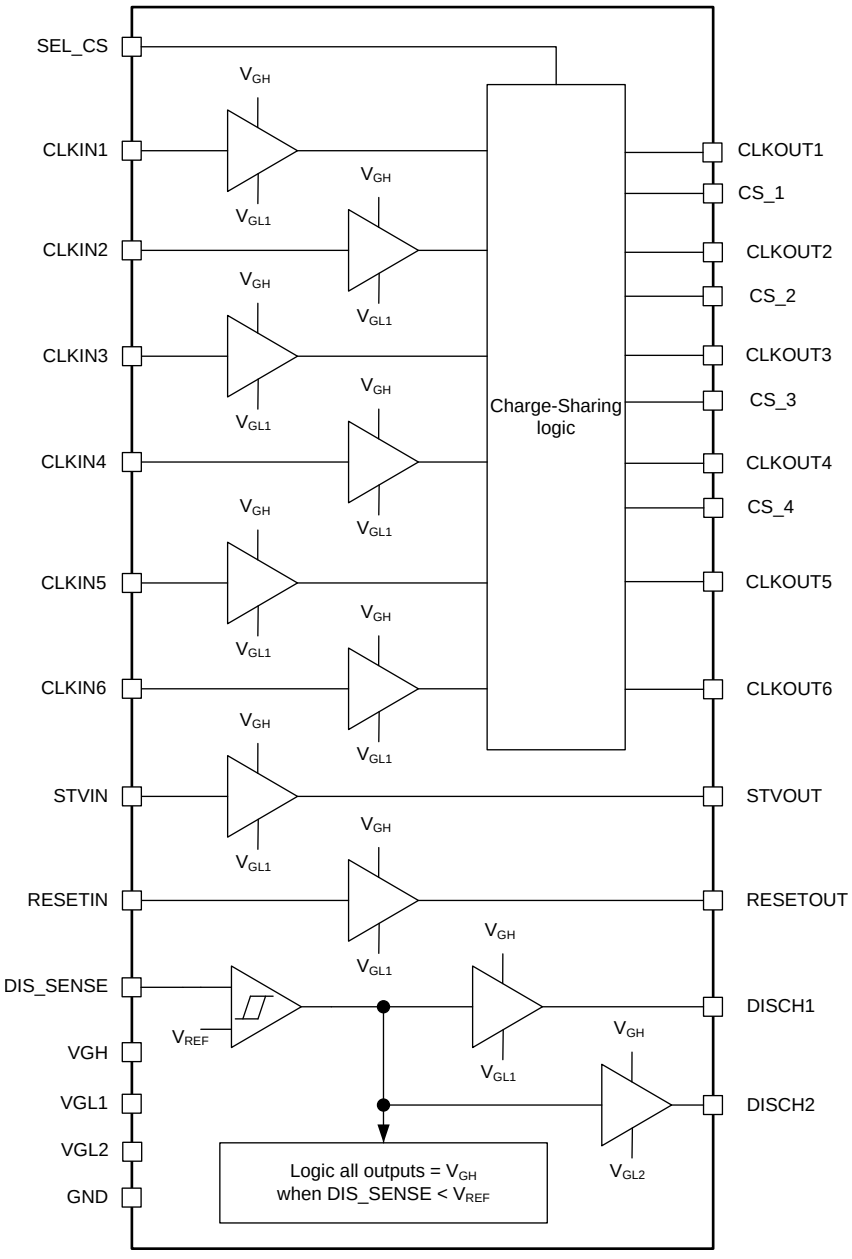
図 3. Slew Rate

8 Detailed Description

8.1 Overview

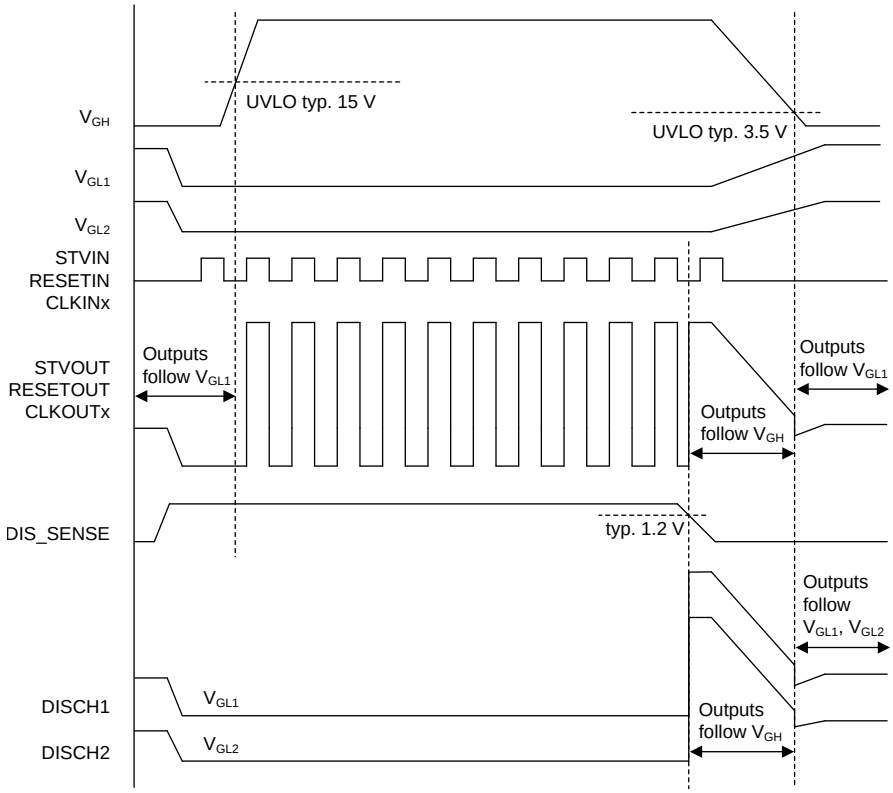
The TPS65197/B is a 8-channel level-shifter with optional discharge function during shut-down. It supports no charge-sharing as well as 2-channel and 3-channel charge-sharing. Two channels are used to generate the STV and RESET signal, the remaining 6 channels generate the clocks. The two discharge outputs (DISCH1 and DISCH2) are connected to VGL1 and VGL2 during operation, at shutdown both discharge outputs are connected to VGH.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Sequencing



8.3.2 Power Up

At power up V_{GL1} and V_{GL2} must be present before V_{GH} is rising. V_{GL1} must be always more negative or equal to V_{GL2}, V_{GH} should not rise faster than in 100 us. All clock output channels and DISCH1 follow V_{GL1}, DISCH2 follows V_{GL2} until V_{GH} rises above its rising UVLO threshold voltage of 15 V, then all clock output channels of the TPS65197B follow their input signals. The TPS65197 has a different startup behavior as CLKOUT1 to CLKOUT6 are forced to V_{GL1} until the 1st rising edge of CLKIN1 releases all clocks. The discharge-sense (DIS_SENSE) voltage must be higher than its maximum threshold voltage of 1.36 V before V_{GH} reaches the rising UVLO threshold of 15 V, otherwise all outputs are forced to V_{GH} and the state is latched. The selected Charge-Sharing method is latched when V_{GH} reaches the rising UVLO according to the SEL_CS voltage, it is reset with the falling UVLO.

8.3.3 Power Down

When the discharge-sense (DIS_SENSE) voltage falls below its typical threshold voltage of 1.26 V, all clock output channels follow V_{GH} until V_{GH} falls below its typical falling UVLO threshold voltage of 3.5 V; then all clock output channels and DISCH1 follow V_{GL1}, DISCH2 follows V_{GL2}. Once discharge-sense is triggered the state is latched, to reset and continue normal operation V_{GH} has to fall below the falling UVLO threshold of 3.5 V.

In case the discharge-sense (DIS_SENSE) voltage stays high during power down, all clock output channels follow their input signals until V_{GH} falls below its typical falling UVLO threshold voltage of 3.5 V; then all clock output channels follow V_{GL1}. The discharge channels follow V_{GL1} and V_{GL2} all the time.

8.3.4 Disabling the Discharge Function

When the discharge function is not used, the DIS_SENSE pin must be pulled above its maximum threshold voltage of 1.36 V all the time (for example to 3.3 V).

Feature Description (continued)

8.3.5 Undervoltage Lockout

To avoid improper operation of the device at low input voltages, an undervoltage lockout function is implemented. When V_{GH} is below the UVLO threshold each output channel is clamped to its respective negative supply, V_{GL1} or V_{GL2}.

8.3.6 Thermal Shutdown

A thermal shutdown is implemented to prevent damage because of excessive heat or power dissipation. Once the junction temperature exceeds a typical value of 150 ºC, all outputs are set to high-impedance. This state is latched. V_{GH} must fall below the falling UVLO (3.5 V) to reset the thermal shutdown.

8.4 Device Functional Modes

8.4.1 Output Clock Behavior

The STV and RESET channels always follow their inputs while the clocks 1 to 6 behave different for TPS65197 and TPS65197B.

TPS65197:

At startup the output signals CLKOUT1 to CLKOUT6 are forced low (V_{GL1}) until the first rising edge of CLKOUT1 releases all clocks. Every rising edge of STVIN stops the Charge-Sharing and resets the output signals CLKOUT1 to CLKOUT6 (that is, forced low) until the next rising edge of CLKIN1 after which the clock outputs follow their inputs again. The rising edge of CLKIN1 should occur not sooner than 50 ns after the rising edge of STVIN. This logic ensures a proper reset and a clean start every frame.

TPS65197B:

The TPS65197B does not have the reset logic as TPS65197 and all outputs always follow their input signals (also at startup). If Charge-Sharing is activated every rising edge of STVIN stops the Charge-Sharing and the output signals CLKOUT1 to CLKOUT6 follow their input signals. The next Charge-Sharing event should not occur sooner than 50 ns after the rising edge of STVIN.

Device Functional Modes (continued)

8.4.2 Charge-Sharing Methods TPS65197

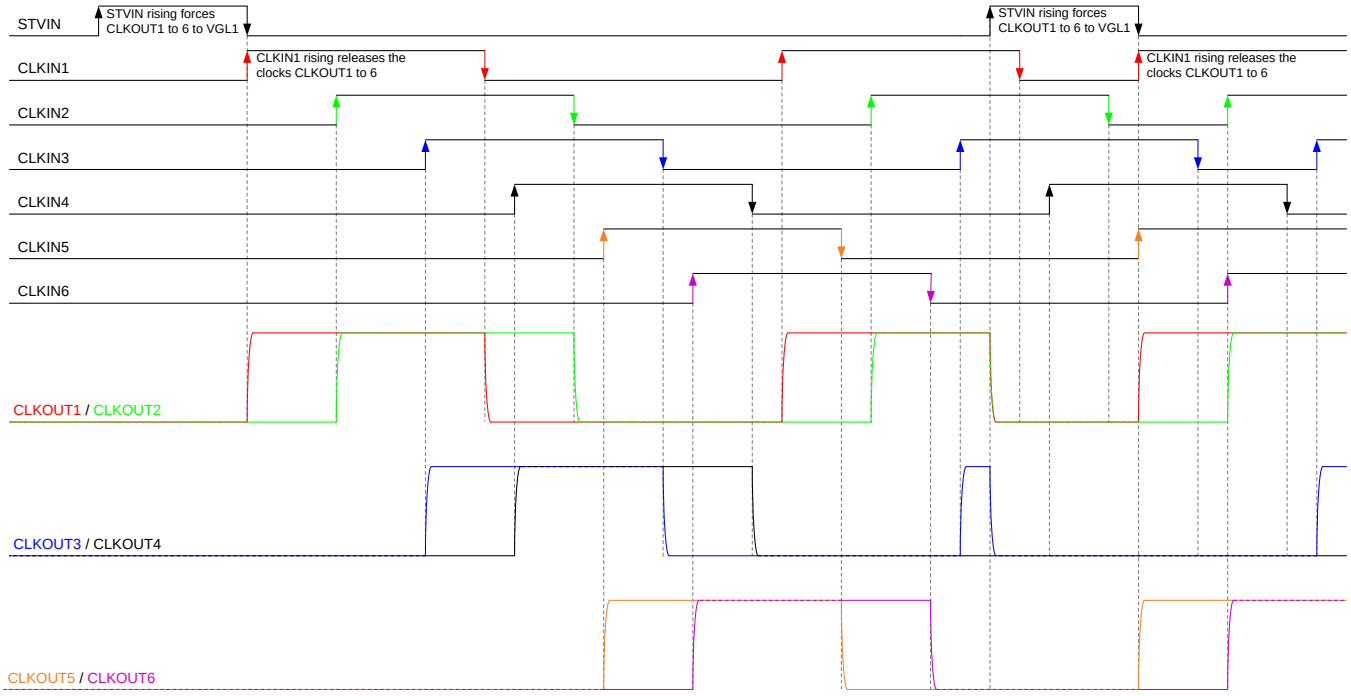
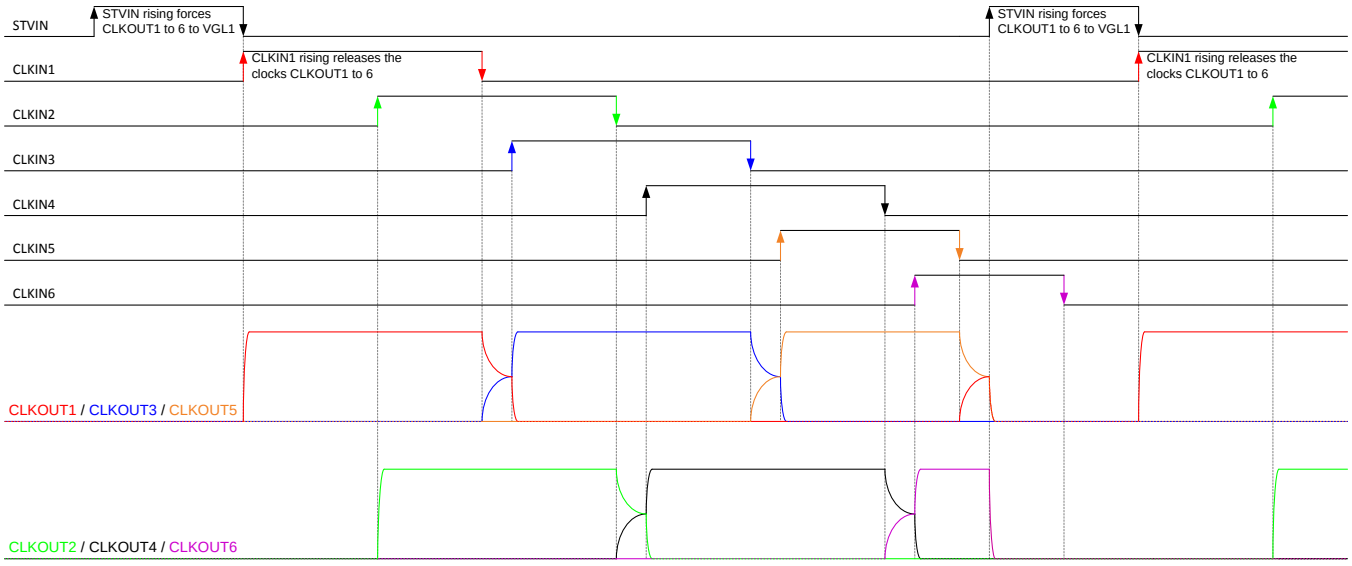


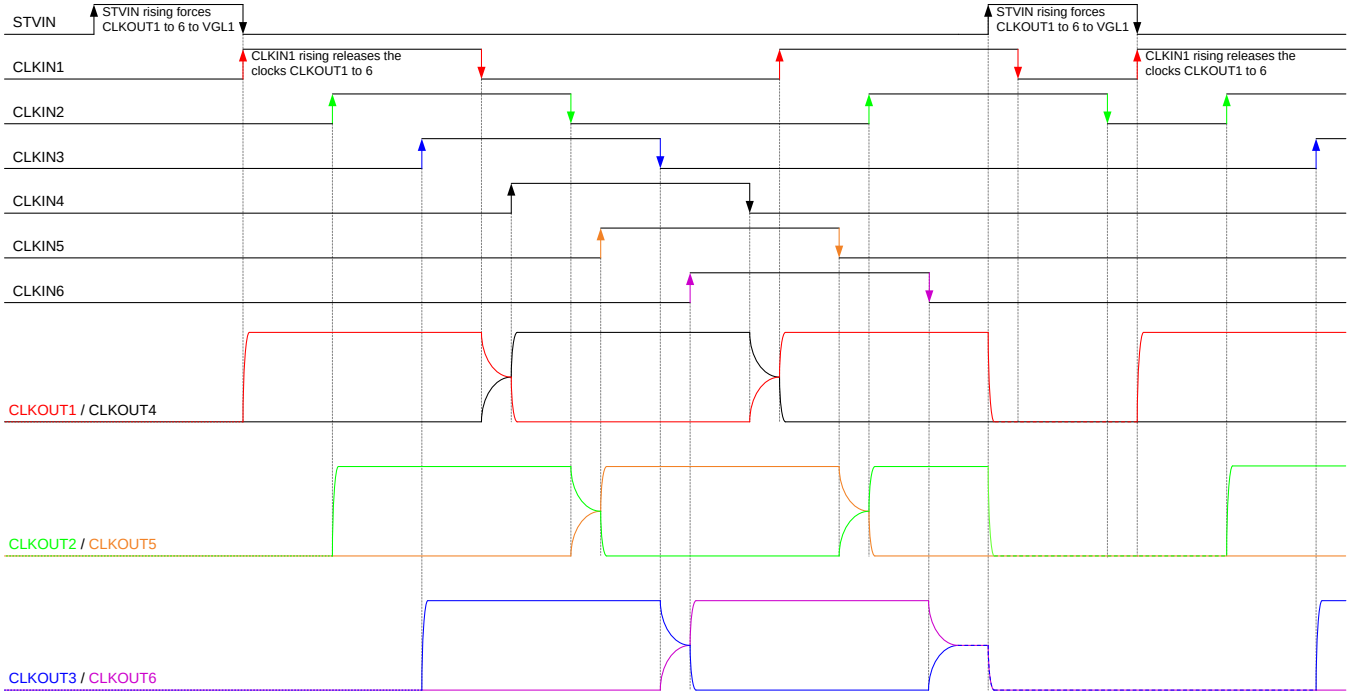
図 4. TPS65197: Charge-Sharing Disabled (CS_SEL < 0.5 V)



Charge-sharing of CLKOUT1 ↔ CLKOUT3 between CLKIN1↓ CLKIN3↑.
Charge-sharing of CLKOUT3 ↔ CLKOUT5 between CLKIN3↓ CLKIN5↑.
Charge-sharing of CLKOUT5 ↔ CLKOUT1 between CLKIN5↓ CLKIN1↑.
Charge-sharing of CLKOUT2 ↔ CLKOUT4 between CLKIN2↓ CLKIN4↑.
Charge-sharing of CLKOUT4 ↔ CLKOUT6 between CLKIN4↓ CLKIN6↑.
Charge-sharing of CLKOUT6 ↔ CLKOUT2 between CLKIN6↓ CLKIN2↑.

図 5. TPS65197: 3-Channel Charge-Sharing (CS_SEL = 1 V…2 V)

Device Functional Modes (continued)



Charge-sharing of CLKOUT1 ↔ CLKOUT4 between CLKIN1↓ CLKIN4↑ and CLKIN4↓ CLKIN1↑.
Charge-Sharing of CLKOUT2 ↔ CLKOUT5 between CLKIN2↓ CLKIN5↑ and CLKIN5↓ CLKIN2↑.
Charge-Sharing of CLKOUT3 ↔ CLKOUT6 between CLKIN3↓ CLKIN6↑ and CLKIN6↓ CLKIN3↑.

図 6. TPS65197: 2-Channel Charge-Sharing (CS_SEL = 2.8 V…6.5 V)

Device Functional Modes (continued)

8.4.3 Charge-Sharing Methods TPS65197B

TPS65197B:

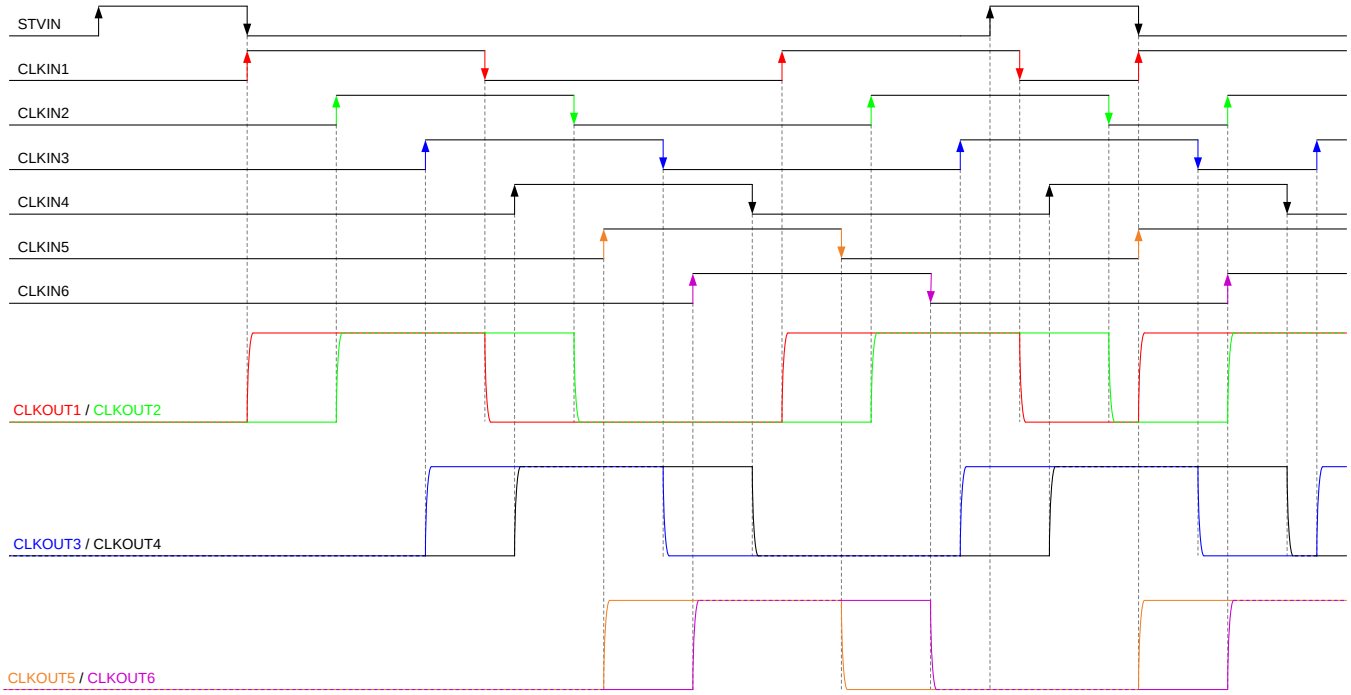
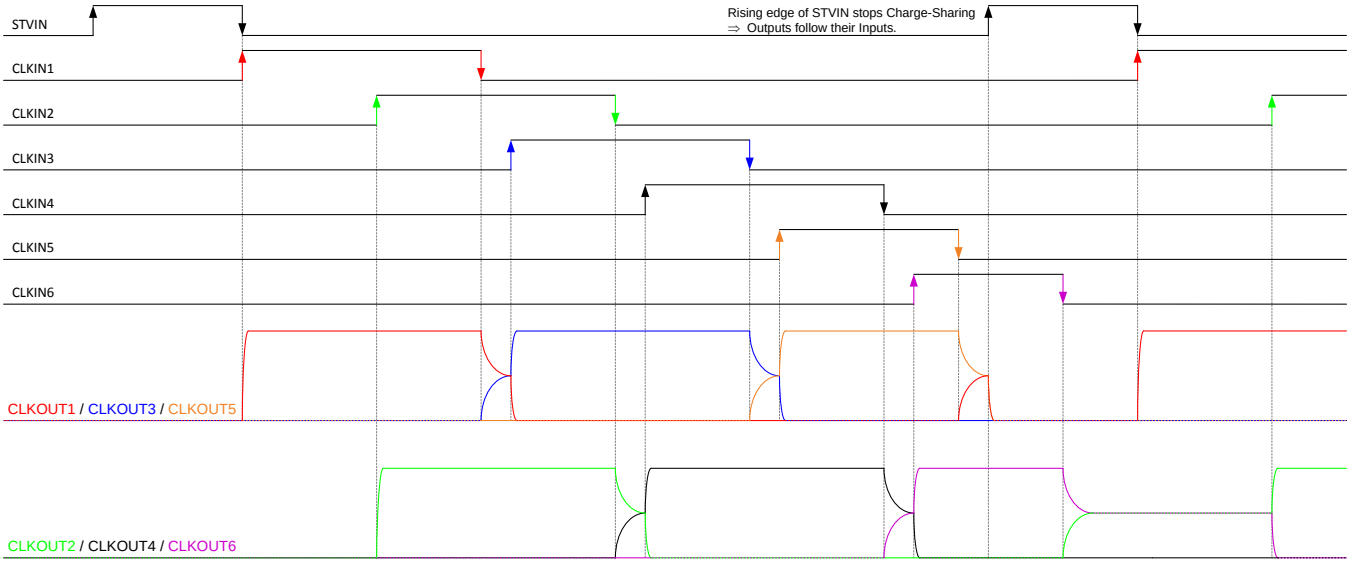


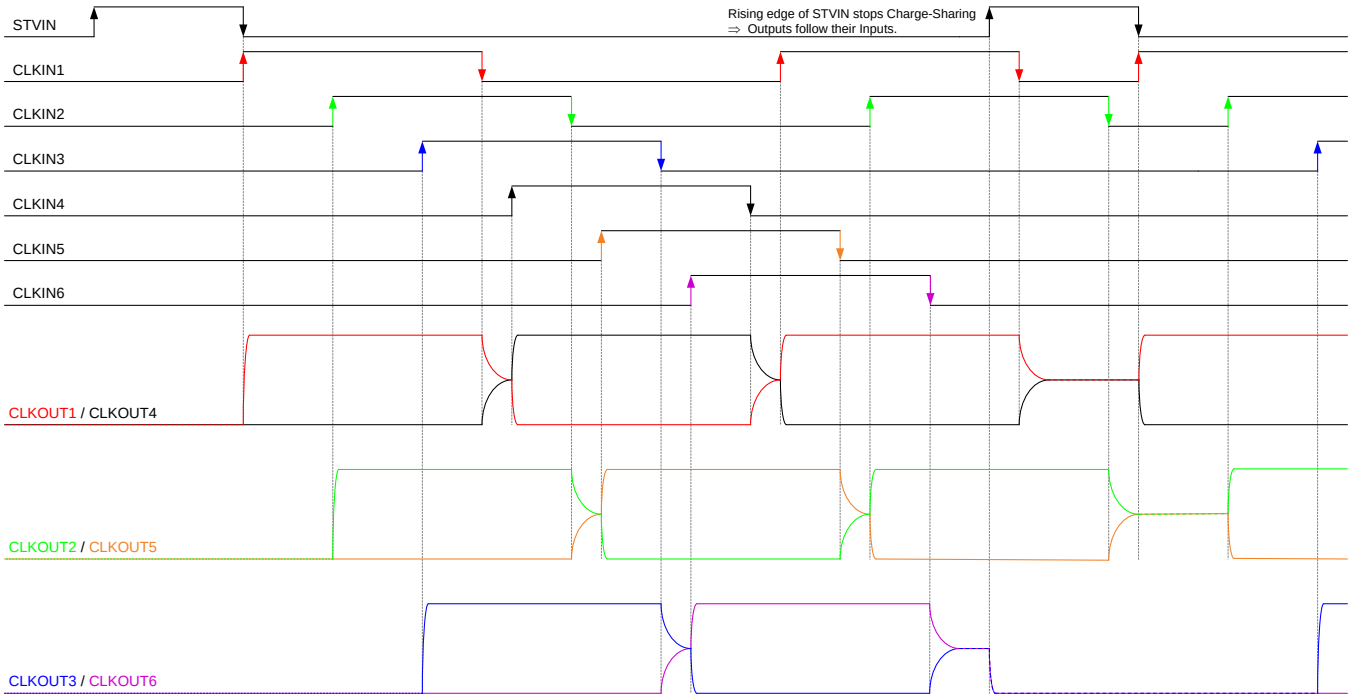
図 7. TPS65197B: Charge-Sharing Disabled (CS_SEL < 0.5 V)



Charge-sharing of CLKOUT1 ↔ CLKOUT3 between CLKIN1↓ CLKIN3↑.
Charge-sharing of CLKOUT3 ↔ CLKOUT5 between CLKIN3↓ CLKIN5↑.
Charge-sharing of CLKOUT5 ↔ CLKOUT1 between CLKIN5↓ CLKIN1↑.
Charge-sharing of CLKOUT2 ↔ CLKOUT4 between CLKIN2↓ CLKIN4↑.
Charge-sharing of CLKOUT4 ↔ CLKOUT6 between CLKIN4↓ CLKIN6↑.
Charge-sharing of CLKOUT6 ↔ CLKOUT2 between CLKIN6↓ CLKIN2↑.

図 8. TPS65197B: 3-Channel Charge-Sharing (CS_SEL = 1 V…2 V)

Device Functional Modes (continued)



Charge-sharing of CLKOUT1 ↔ CLKOUT4 between CLKIN1↓ CLKIN4↑ and CLKIN4↓ CLKIN1↑.
Charge-Sharing of CLKOUT2 ↔ CLKOUT5 between CLKIN2↓ CLKIN5↑ and CLKIN5↓ CLKIN2↑.
Charge-Sharing of CLKOUT3 ↔ CLKOUT6 between CLKIN3↓ CLKIN6↑ and CLKIN6↓ CLKIN3↑.

図 9. TPS65197B: 2-Channel Charge-Sharing (CS_SEL = 2.8 V…6.5 V)

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS65197/B is a 8-channel level-shifter with discharge function. It supports no charge-sharing as well as 2-channel and 3-channel charge-sharing.

9.2 Typical Application

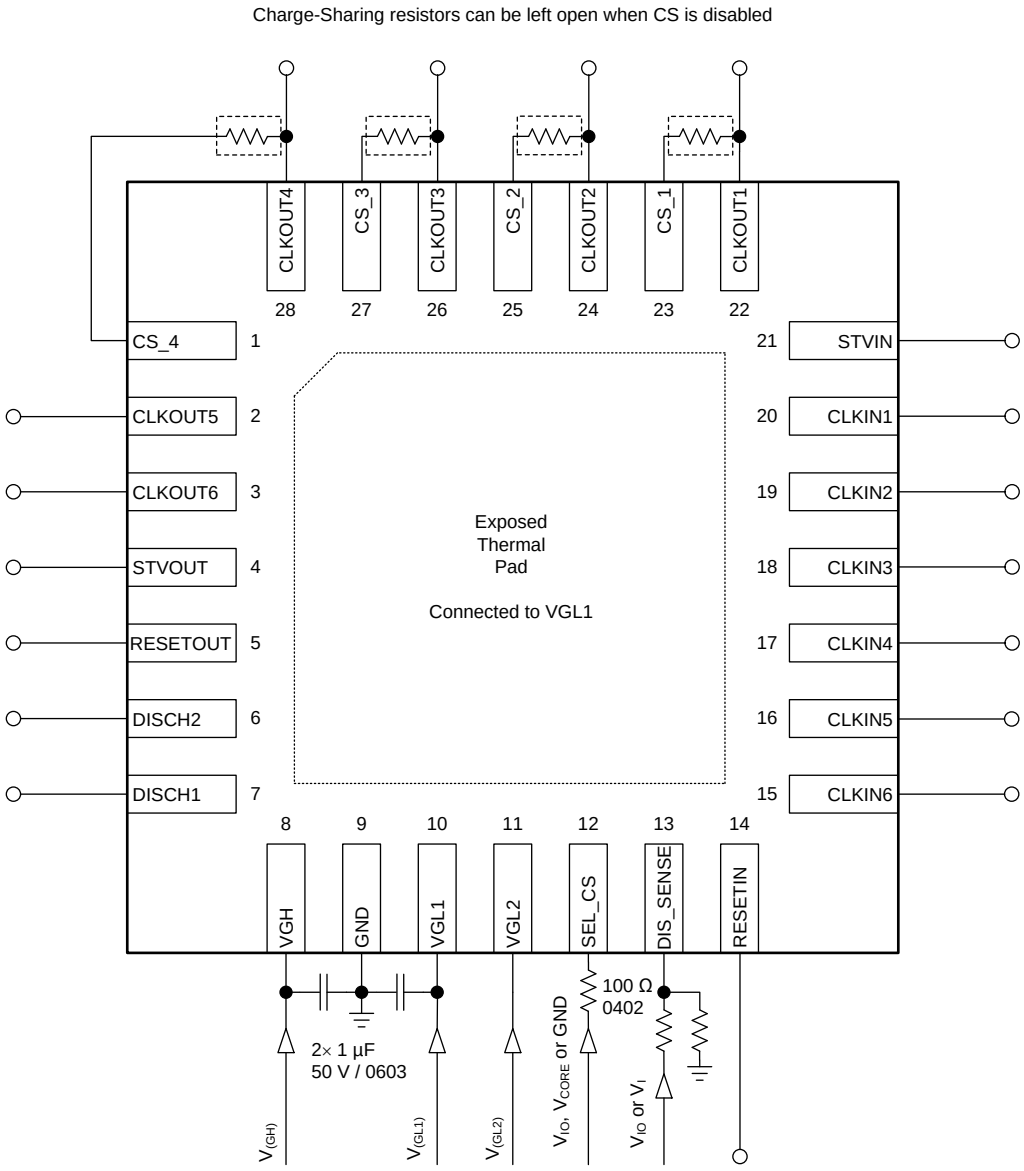


図 10. Typical Application Schematic

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the input parameters shown in 表 1.

表 1. Design Parameters

DESIGN PARAMETER	EXAMPLE
Input voltage range	16.5 V to 45 V
	–20 V to –3 V
Input signals	83 kHz
Logic levels	low level < 0.8 V
	high level > 2 V
Output load	150 pF and 50 Ω in series with 4.7 nF
Charge-sharing resistance	100 Ω

9.2.2 Detailed Design Procedure

Level Shifters for LCD panels generate fast signals, therefore special care must be taken to the input and output trace length and layout symmetry. Signal delays can be caused by unsymmetric trace length. Placing the components around the device is not critical, as mostly resistors are used. Care must be taken for the supply capacitors which should be close to the device and have a good connection to ensure clean output signals.

9.2.3 Application Curves

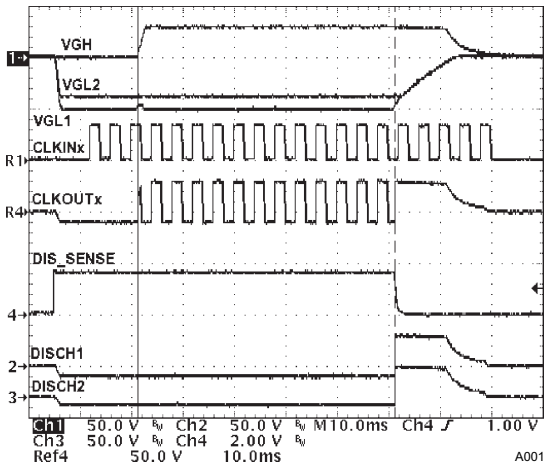


図 11. Power Up, Power Down

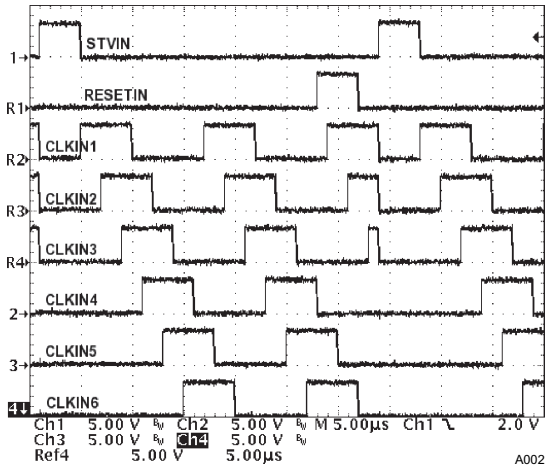
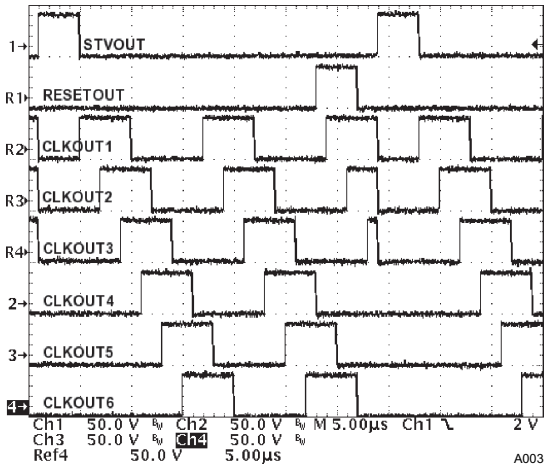
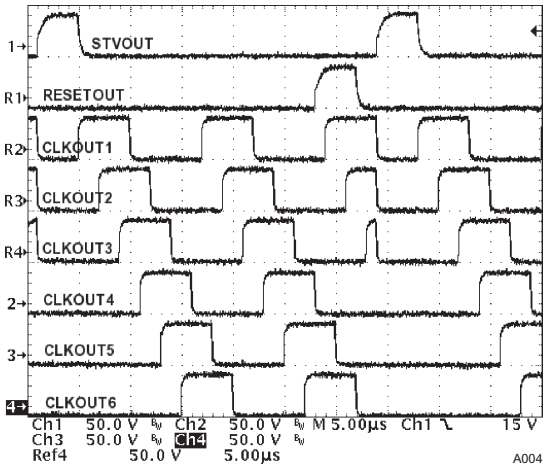


図 12. No Charge Sharing Input Signals



Load: 150 pF

図 13. No Charge Sharing Outputs



Load: 50 Ω, 4.7 nF

図 14. No Charge Sharing Outputs

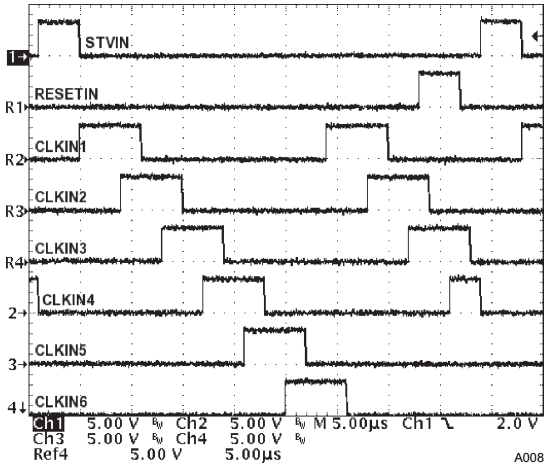
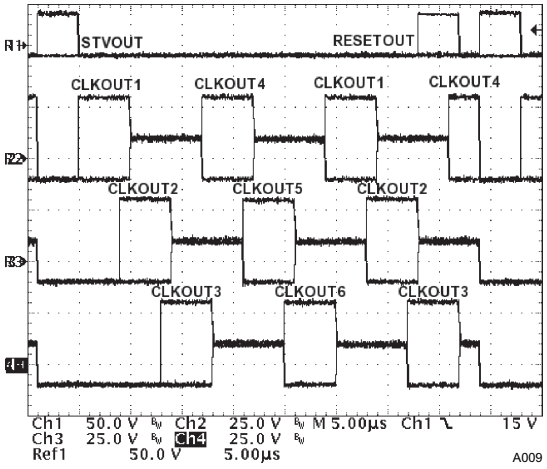
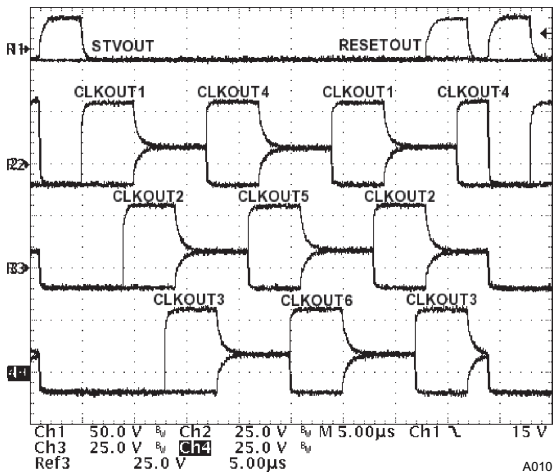


図 15. 2-Channel Charge Sharing Input Signals



Load: 150 pF R_{CS} = 100 Ω

図 16. 2-Channel Charge Sharing Outputs



Load: 50 Ω, 4.7 nF R_{CS} = 100 Ω

図 17. 2-Channel Charge Sharing Outputs

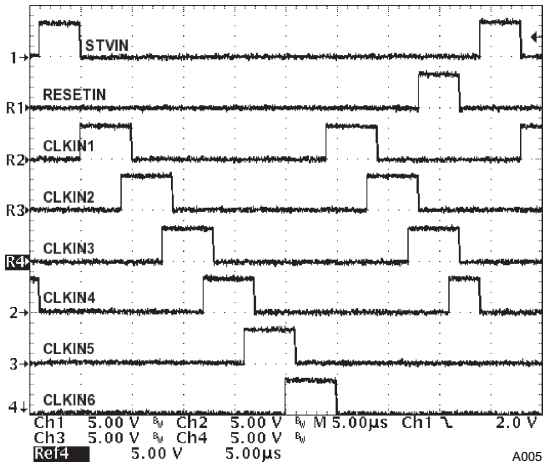
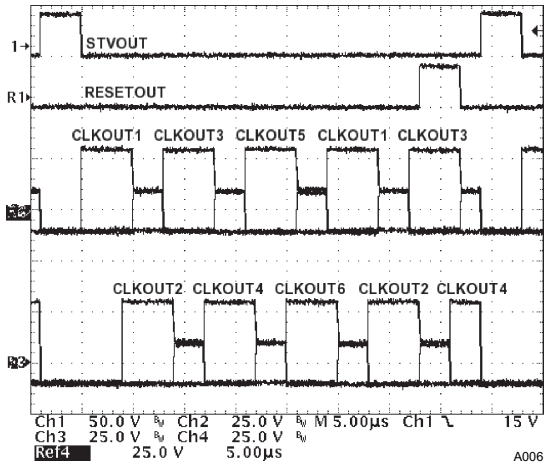
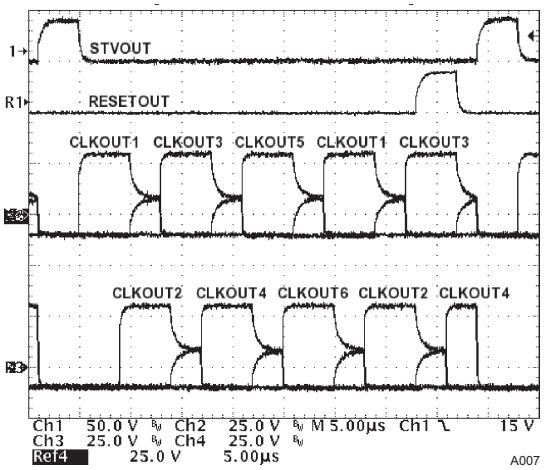


図 18. 3-Channel Charge Sharing Input Signals



Load: 150 pF R_{CS} = 100 Ω

図 19. 3-Channel Charge Sharing Outputs



Load: 50 Ω, 4.7 nF R_{CS} = 100 Ω

図 20. 3-Channel Charge Sharing Outputs

10 Power Supply Recommendations

The TPS65197/B is designed to operate from an input voltage supply range between 16.5 V and 45 V on the positive supply rail (VGH) and between –20 V and –3 V on the negative supply rails (VGL1, VGL2). A 1-µF capacitor on VGH and VGL1 should be used to ensure clean output signals.

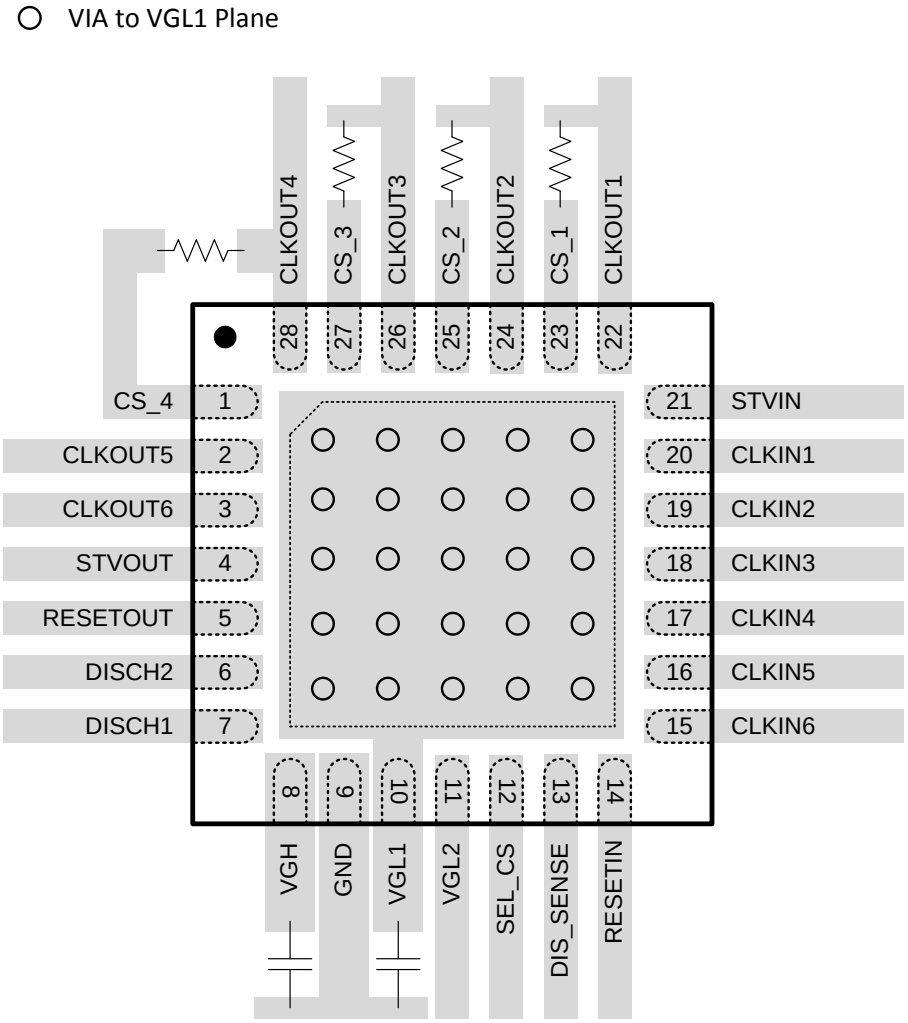
11 Layout

11.1 Layout Guidelines

Proper PCB layout is essential for achieving the expected performance and a low device temperature. The following points should be considered.

- Place the supply decoupling capacitors as close as possible to device terminals VGH and VGL1.
- Use wide traces to route power from the bias IC to the device to avoid voltage drops. The device is able to sink and source high peak currents up to 1 A. If wide traces are not possible, place additional 1-µF capacitors of at least 0805 size close to the supply decoupling capacitors.
- The output channel traces should be kept as short as possible to reduce EMI emissions, and not too thin to minimize stray inductances producing voltage overshoots at the panel, because high peak currents up to 1 A can flow.
- The thermal pad must be connected by many vias to a large copper area on a VGL1 potential, to be used as a heat sink. Use a copper area of at least 10 cm^2. The bigger the copper area, the cooler the device temperature. On a multilayer board, use the copper areas of as many layers as possible to maximize the heat sink.
- Output resistors for clock channels 1 to 6 can be used to reduce EMI emissions and device temperature if necessary. They generate heat and should therefore not be placed close to the device.

11.2 Layout Example



12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

『放熱特性の優れたPowerPAD™パッケージ』アプリケーション・レポート(SLMA002)
『PowerPAD™の簡単な使用法』アプリケーション・レポート(SLMA004)
『QFNレイアウト・ガイドライン』アプリケーション・レポート(SLOA122)
『QFN/SONのPCB実装』アプリケーション・レポート(SLUA271)

12.2 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 2. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
TPS65197	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS65197B	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

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12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65197BRUYR	ACTIVE	WQFN	RUY	28	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65197B	Samples
TPS65197BRUYT	ACTIVE	WQFN	RUY	28	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 65197B	Samples
TPS65197RUYR	ACTIVE	WQFN	RUY	28	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65197A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

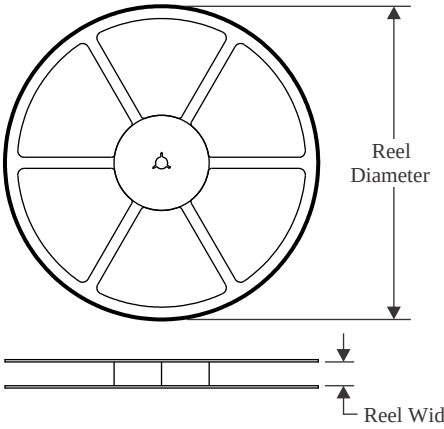
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

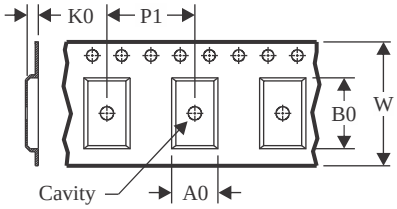
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

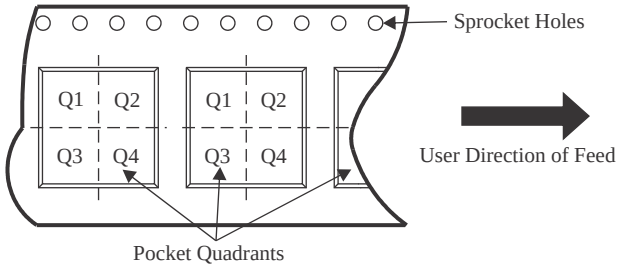


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

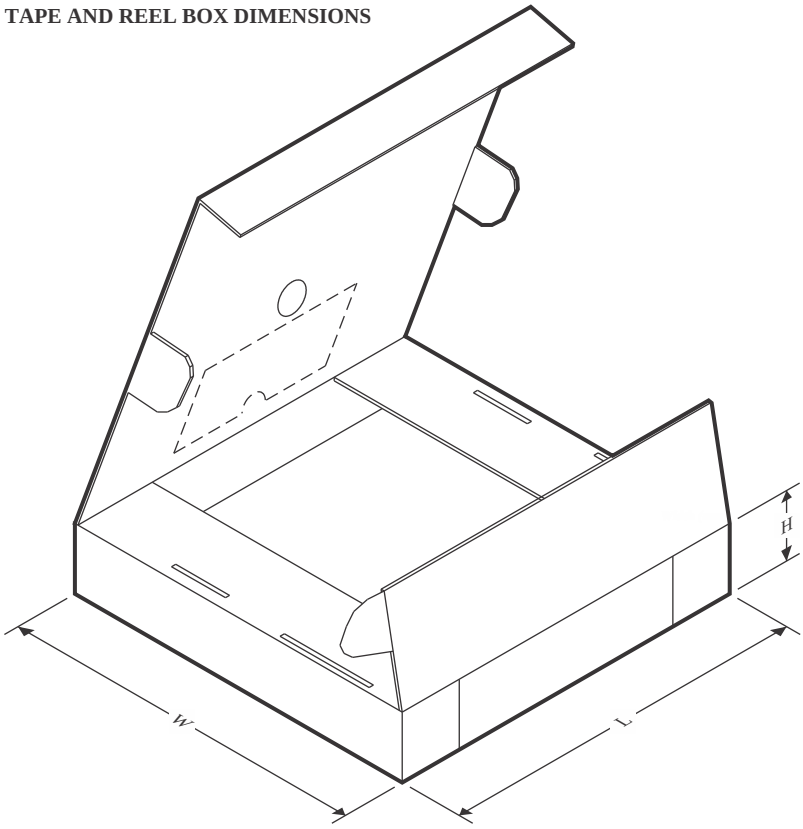
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65197BRUYR	WQFN	RUY	28	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65197BRUYT	WQFN	RUY	28	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65197RUYR	WQFN	RUY	28	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

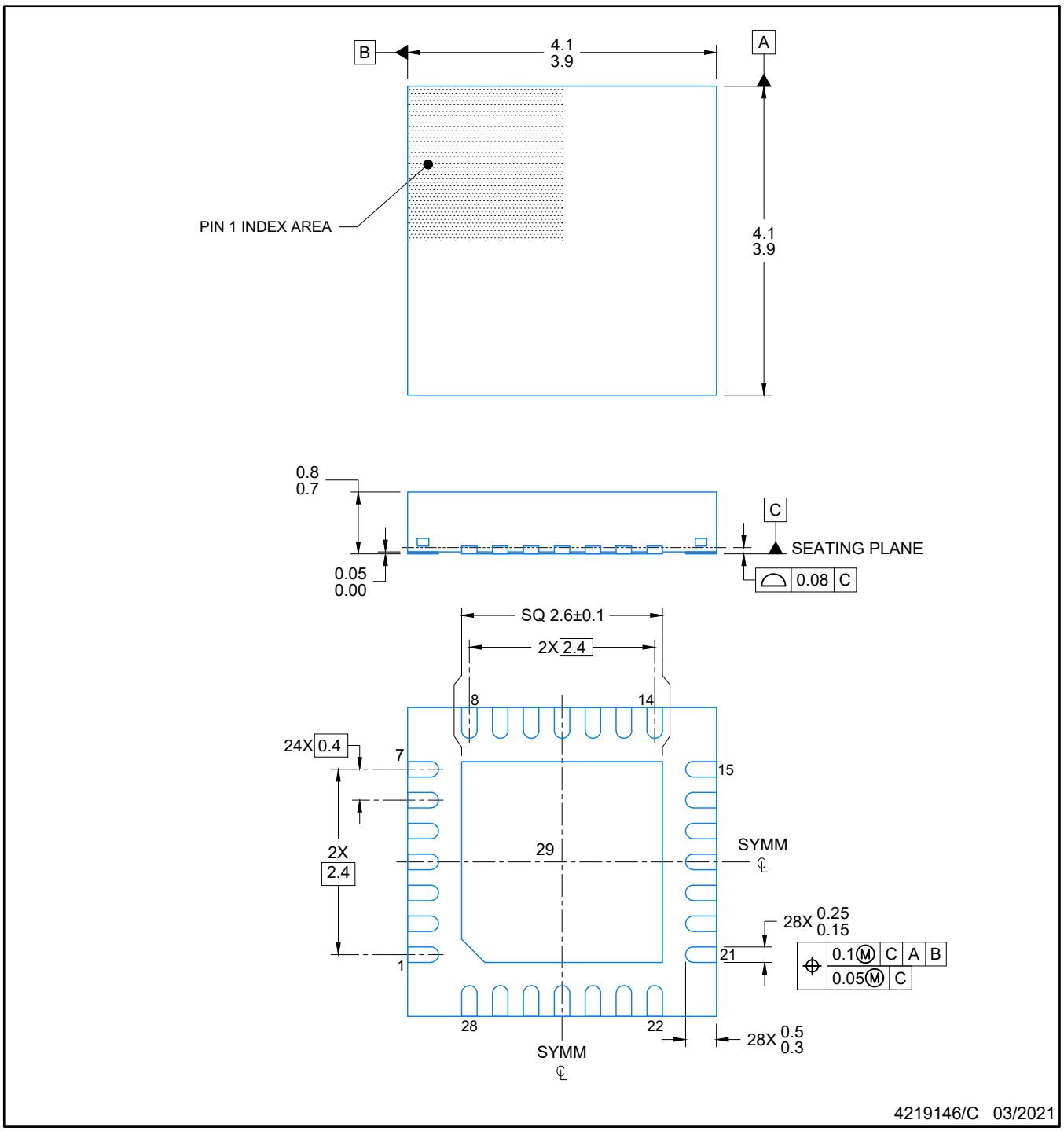
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65197BRUYR	WQFN	RUY	28	3000	346.0	346.0	33.0
TPS65197BRUYT	WQFN	RUY	28	250	182.0	182.0	20.0
TPS65197RUYR	WQFN	RUY	28	3000	346.0	346.0	33.0

PACKAGE OUTLINE

RUY0028A

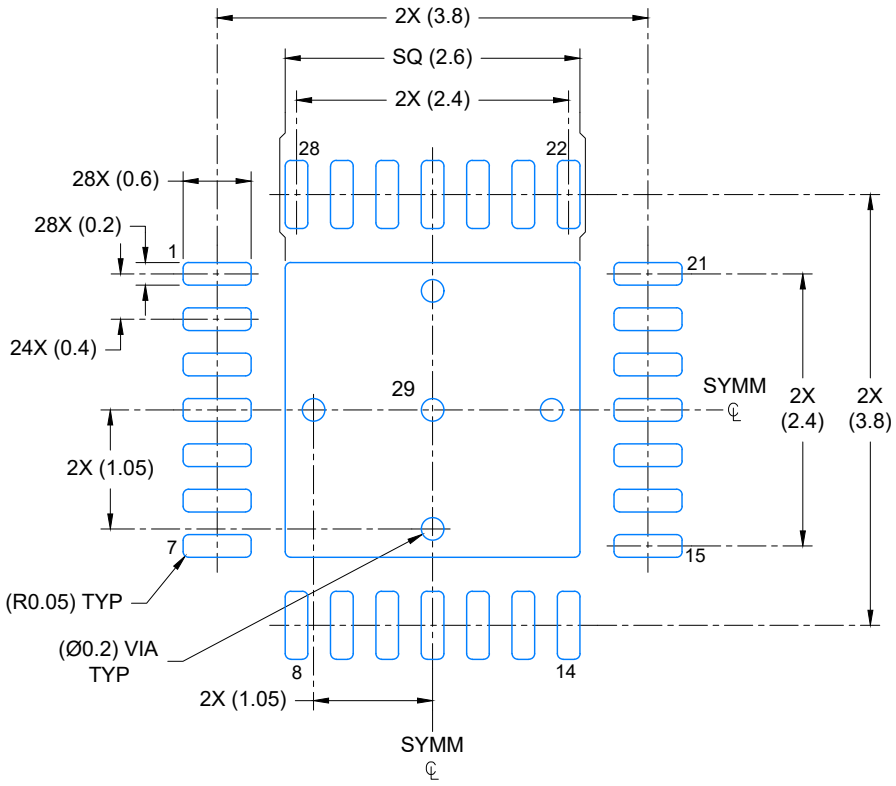
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK-NO LEAD

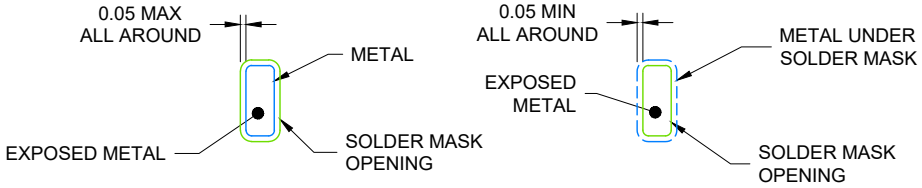


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON SOLDER MASK DEFINED (PREFERRED)

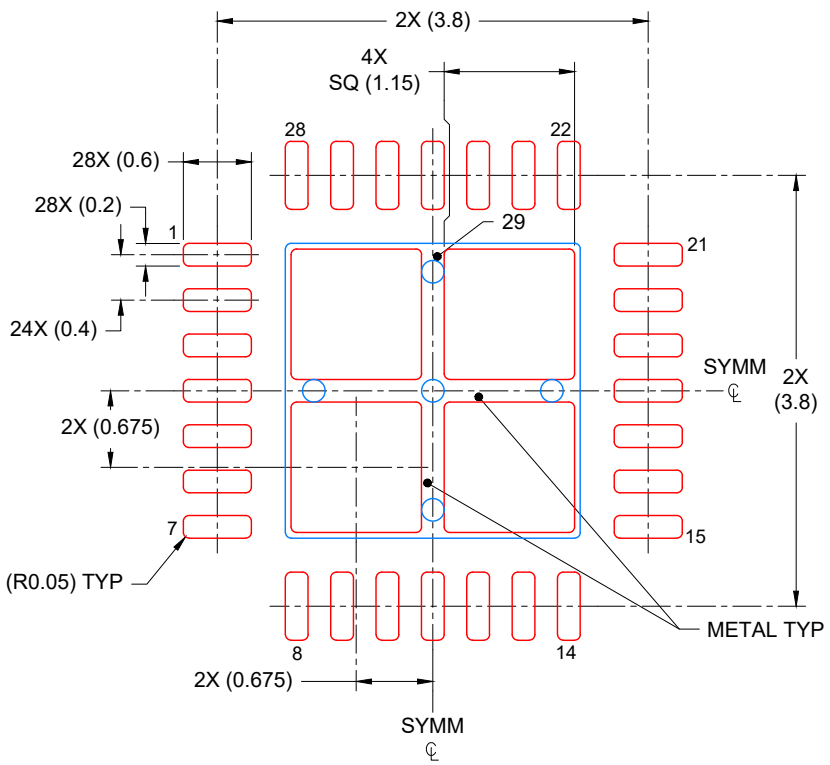
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4219146/C 03/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 15X

4219146/C 03/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

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