# TPS6526x 入力電圧 4.5V〜18V、出力電流 3A / 2A / 2A、トリプル同期整流降圧型コンバータ

## 1 特長

- 動作入力電源電圧範囲 (4.5V〜18V)
- 帰還基準電圧：0.6V±1%
- 最大連続出力電流：3A / 2A / 2A
- 可変クロック周波数：250kHz〜2MHz
- 各バックに専用のイネーブル・ピンとソフト・スタート・ピン
- 自動パワーアップ / パワーダウン・シーケンス
- 軽負荷時のパルス・スキップ・モード (PSM) (TPS65261 のみ)
- 出力電圧パワー・グッド・インジケータ
- 入力電圧パワー障害インジケータ
- 過熱保護

## 2 アプリケーション

- DTV
- セット・トップ・ボックス
- ホーム・ゲートウェイおよびアクセス・ポイント・ネットワーク
- ワイヤレス・ルータ
- 監視機器
- POS 機器

## 3 概要

TPS65261、TPS65261-1 は、出力電流 3A / 2A / 2A のモノリシック・トリプル同期降圧型 (バック) コンバータです。4.5V〜18V の幅広い入力電源電圧範囲をサポートしており、5V、9V、12V、または 15V のようなほとんどの中間バス電圧入力に対応できます。コンバータは定周波数ピーク電流モードを備え、アプリケーションを単純化しながら、目的のアプリケーションに合わせてシステムを最適化できるよう設計されています。コンバータのスイッチング周波数は、外付け抵抗を使用して 250kHz〜2MHz の範囲内で調整できます。Buck1 と Buck2、3 の間は位相差 180 度で動作し (Buck2 と 3 は同相動作)、入力フィルタ回路への要求を最小限に抑えることができるようになります。

TPS65261、TPS65261-1 は、MODE ピンを V7V に接続して EN1 / 2 / 3 ピンを設定することで、自動パワー・シーケンスを有効にできます。また、オープン・ドレインの RESET 信号を使用してパワーダウンを監視できます。
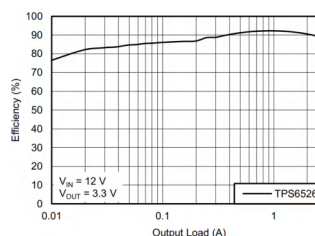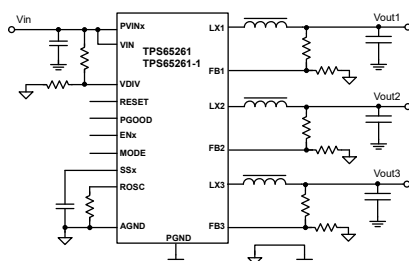
軽負荷時には、TPS65261 は自動的にパルス・スキップ・モード (PSM) で動作し、TPS65261-1 は強制連続電流モード (FCC) で動作します。PSM モードでは、軽負荷時にスイッチング損失を低減することで高い効率を実現します。FCC モードでは、ノイズ耐性が高まり、RF 干渉が低減されます。

また、これらの製品は、過電圧保護、過電流保護、短絡保護、および過熱保護機能を備えており、どちらかの出力電圧がレギュレーション範囲を外れると、パワー・グッド・ピンがアサートされます。

### デバイス情報 [(1)]

| 部品番号 | モード | パッケージ |
|---|---|---|
| TPS65261 | PSM | RHB (VQFN、32) |
| TPS65261-1 | FCCM | |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション

English Data Sheet: SLVSCD3

# Table of Contents

# 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision B (May 2014) to Revision C (May 2023) | Page |
|---|---|
| • ドキュメント全体にわたって表、図、相互参照の採番方法を更新.............................................................1 | |
| • ドキュメント全体にわたって画像の色を除去.........................................................................................1 | |
| • Changed the description of V7V pin in 表 5-1..................................................................................3 | |
| • Moved the storage temperature row in the *ESD Ratings* table to the *Absolute Maximum Ratings* table...........5 | |
| • Renamed *Handling Ratings* to *ESD Ratings* .................................................................................5 | |
| • Changed the recommended value of capacitor from V7V pin to power ground in *V7V Low Dropout Regulator and Bootstrap*........................................................................................................................20 | |
| • Changed the recommended value of C5 in 図 8-1 ..........................................................................25 | |

| Changes from Revision A (December 2013) to Revision B (May 2014) | Page |
|---|---|
| • 新しいデータシートのテンプレートに合わせてすべてのテキスト、表、およびグラフィックスを変更.............................1 | |
| • Changed 図 8-37 ...........................................................................................................................37 | |

# 5 Pin Configuration and Functions
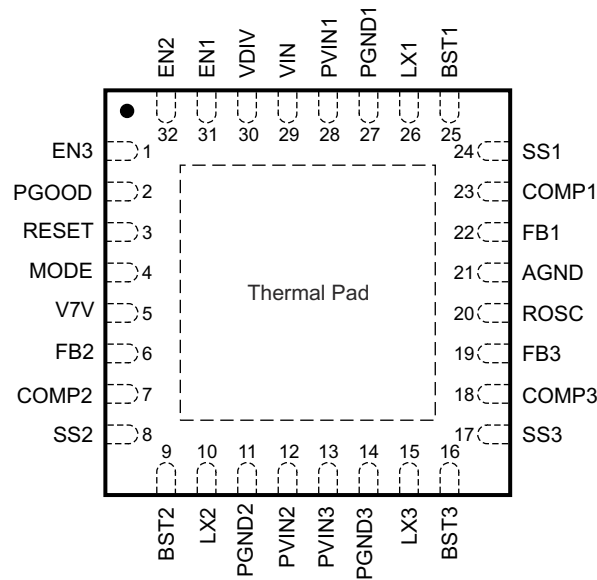


(There is no electric signal down bonded to thermal pad inside IC. Exposed thermal pad must be soldered to PCB for optimal thermal performance.)

図 5-1. RHB Package 8-Pin VQFN (Top View)

表 5-1. Pin Functions

| PIN | | DESCRIPTION |
|---|---|---|
| NO. | NAME | |
| 1 | EN3 | Enable for buck3. Float to enable. Can use this pin to adjust the input undervoltage lockout of buck3 with a resistor divider. |
| 2 | PGOOD | An open drain output, asserts low if output voltage of any buck beyond regulation range due to thermal shutdown, overcurrent, undervoltage or ENx shut down. |
| 3 | RESET | Open drain power failure output signal. |
| 4 | MODE | When high, an automatic power-up/power-down sequence is provided according to states of EN1, EN2 and EN3 pins. |
| 5 | V7V | Internal LDO for gate driver and internal controller. Connect a 10-µF capacitor from the pin to power ground |
| 6 | FB2 | Feedback Kelvin sensing pin for buck2 output voltage. Connect this pin to buck2 resistor divider. |
| 7 | COMP2 | Error amplifier output and Loop compensation pin for buck2. Connect a series resistor and capacitor to compensate the control loop of buck2 with peak current PWM mode. |
| 8 | SS2 | Soft-start and tracking input for buck2. An internal 5-µA pullup current source is connected to this pin. The soft-start time can be programmed by connecting a capacitor between this pin and ground. |
| 9 | BST2 | Boot strapped supply to the high side floating gate driver in buck2. Connect a capacitor (recommend 47nF) from BST2 pin to LX2 pin. |
| 10 | LX2 | Switching node connection to the inductor and bootstrap capacitor for buck2. The voltage swing at this pin is from a diode voltage below the ground up to PVIN2 voltage. |
| 11 | PGND2 | Power ground connection of buck2. Connect PGND2 pin as close as practical to the (–) terminal of VIN2 input ceramic capacitor. |
| 12 | PVIN2 | Input power supply for buck2. Connect PVIN2 pin as close as practical to the (+) terminal of an input ceramic capacitor (suggest 10µF). |
| 13 | PVIN3 | Input power supply for buck3. Connect PVIN3 pin as close as practical to the (+) terminal of an input ceramic capacitor (suggest 10µF). |
| 14 | PGND3 | Power ground connection of buck3. Connect PGND3 pin as close as practical to the (–) terminal of VIN3 input ceramic capacitor. |

表 5-1. Pin Functions (continued)

| PIN | | DESCRIPTION |
|---|---|---|
| NO. | NAME | |
| 15 | LX3 | Switching node connection to the inductor and bootstrap capacitor for buck3. The voltage swing at this pin is from a diode voltage below the ground up to PVIN3 voltage. |
| 16 | BST3 | Boot strapped supply to the high side floating gate driver in buck3. Connect a capacitor (recommend 47nF) from BST3 pin to LX3 pin. |
| 17 | SS3 | Soft-start and tracking input for buck3. An internal 5-μA pullup current source is connected to this pin. The soft-start time can be programmed by connecting a capacitor between this pin and ground. |
| 18 | COMP3 | Error amplifier output and Loop compensation pin for buck3. Connect a series resistor and capacitor to compensate the control loop of buck3 with peak current PWM mode. |
| 19 | FB3 | Feedback Kelvin sensing pin for buck3 output voltage. Connect this pin to buck3 resistor divider. |
| 20 | ROSC | Oscillator frequency programmable pin. Connect an external resistor to set the switching frequency. |
| 21 | AGND | Analog ground common to buck controllers and other analog circuits. It must be routed separately from high current power grounds to the (–) terminal of bypass capacitor of input voltage VIN. |
| 22 | FB1 | Feedback Kelvin sensing pin for buck1 output voltage. Connect this pin to buck1 resistor divider. |
| 23 | COMP1 | Error amplifier output and Loop compensation pin for buck1. Connect a series resistor and capacitor to compensate the control loop of buck1 with peak current PWM mode. |
| 24 | SS1 | Soft-start and tracking input for buck1. An internal 5-μA pullup current source is connected to this pin. The soft-start time can be programmed by connecting a capacitor between this pin and ground. |
| 25 | BST1 | Boot strapped supply to the high side floating gate driver in buck1. Connect a capacitor (recommend 47nF) from BST1 pin to LX1 pin. |
| 26 | LX1 | Switching node connection to the inductor and bootstrap capacitor for buck1. The voltage swing at this pin is from a diode voltage below the ground up to PVIN1 voltage. |
| 27 | PGND1 | Power ground connection of Buck1. Connect PGND1 pin as close as practical to the (–) terminal of VIN1 input ceramic capacitor. |
| 28 | PVIN1 | Input power supply for buck1. Connect PVIN1 pin as close as practical to the (+) terminal of an input ceramic capacitor (suggest 10μF). |
| 29 | VIN | Buck controller power supply. |
| 30 | VDIV | Input voltage threshold for power failure detection of input voltage. |
| 31 | EN1 | Enable for buck1. Float to enable. Can use this pin to adjust the input undervoltage lockout of buck1 with a resistor divider. |
| 32 | EN2 | Enable for buck2. Float to enable. Can use this pin to adjust the input undervoltage lockout of buck2 with a resistor divider. |
| | PAD | There is no electric signal down bonded to thermal pad inside IC. Exposed thermal pad must be soldered to PCB for optimal thermal performance. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

|  | MIN | MAX | UNIT |
|---|---|---|---|
| PVIN1, PVIN2, PVIN3,VIN | −0.3 | 20 | V |
| LX1, LX2, LX3 (Maximum withstand voltage transient < 20 ns) | −1.0 | 20 | V |
| BST1, BST2, BST3 referenced to LX1, LX2, LX3 pins respectively | −0.3 | 7 | V |
| EN1, EN2, EN3, PGOOD, V7V, MODE, RESET, VDIV | −0.3 | 7 | V |
| FB1, FB2, FB3, COMP1 , COMP2, COMP3, SS1, SS2, SS3, ROSC | −0.3 | 3.6 | V |
| AGND, PGND1, PGND2, PGND3 | −0.3 | 0.3 | V |
| Operating junction temperature, $T_J$ | −40 | 125 | °C |
| Storage temperature range, $T_{stg}$ | −55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

|  |  |  | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1] | −2000 | 2000 | V |
|  |  | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2] | −500 | 500 |  |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|  |  | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
|  | PVIN1, PVIN2, PVIN3,VIN | 4.5 |  | 18 | V |
|  | LX1, LX2, LX3 (Maximum withstand voltage transient < 20 ns) | −0.8 |  | 18 | V |
|  | BST1, BST2, BST3 referenced to LX1, LX2, LX3 pins respectively | −0.1 |  | 6.8 | V |
|  | EN1, EN2, EN3, PGOOD, V7V, MODE, RESET, VDIV | −0.1 |  | 6.3 | V |
|  | FB1, FB2, FB3, COMP1 , COMP2, COMP3, SS1, SS2, SS3, ROSC | −0.1 |  | 3 | V |
| $T_A$ | Operating junction temperature | −40 |  | 85 | °C |
| $T_J$ | Operating junction temperature | −40 |  | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC[1] | | TPS65261 RHB (32 PINS) | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 31.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 23.4 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 6.1 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.2 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 6.1 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 0.9 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics

$T_A$ = 25°C, $V_{IN}$ = 12 V, $f_{SW}$ = 600 kHz (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT SUPPLY VOLTAGE** | | | | | | |
| VIN | Input voltage range | | 4.5 | | 18 | V |
| UVLO | VIN undervoltage lockout | VIN rising | 4 | 4.25 | 4.5 | V |
| | | VIN falling | 3.5 | 3.75 | 4 | |
| | | Hysteresis | | 500 | | mV |
| $IDD_{SDN}$ | Shutdown supply current | EN1=EN2=EN3=MODE=0 V | | 9.2 | | µA |
| $IDD_{Q\_NSW}$ | Input quiescent current without buck1/2/3 switching | EN1=EN2=EN3=5 V, FB1=FB2=FB3=0.8 V | | 605 | | µA |
| $IDD_{Q\_NSW1}$ | | EN1=5V, EN2=EN3=0 V, FB1=0.8V | | 330 | | µA |
| $IDD_{Q\_NSW2}$ | | EN2=5 V, EN1=EN3=0V, FB2=0.8 V | | 330 | | µA |
| $IDD_{Q\_NSW3}$ | | EN3=5V, EN1=EN2=0V, FB3=0.8V | | 330 | | µA |
| $V_{7V}$ | V7V LDO output voltage | $V_{7V}$ load current = 0 A | 6 | 6.3 | 6.6 | V |
| $I_{OCP\_V7V}$ | V7V LDO current limit | | | 175 | | mA |
| **FEEDBACK VOLTAGE REFERENCE** | | | | | | |
| $V_{FB}$ | Feedback voltage | $V_{COMP}$ = 1.2 V, $T_J$ = 25°C | 0.596 | 0.6 | 0.605 | V |
| | | $V_{COMP}$ = 1.2 V, $T_J$ = -40°C to 125°C | 0.594 | 0.6 | 0.606 | V |
| $V_{LINEREG\_BUCK}$ | Line regulation-DC | $I_{OUT1}$ = 1.5 A, $I_{OUT2}$ = 1 A, $I_{OUT3}$ = 1 A<br>5 V < PVINx < 18 V | | 0.002 | | %/V |
| $V_{LOADREG\_BUCK}$ | Load regulation-DC | $I_{OUTx}$ = (10–100%) × $I_{OUTx\_max}$ | | 0.02 | | %/A |
| **Buck1, Buck2, Buck3** | | | | | | |
| $V_{ENXH}$ | EN1/2/3 high level input voltage | | | 1.2 | 1.26 | V |
| $V_{ENXL}$ | EN1/2/3 low level input voltage | | 1.1 | 1.15 | | V |
| $I_{ENX1}$ | EN1/2/3 pullup current | ENx = 1 V | | 3.6 | | µA |
| $I_{ENX2}$ | EN1/2/3 pullup current | ENx = 1.5 V | | 6.6 | | µA |
| $I_{ENhys}$ | Hysteresis current | | | 3 | | µA |
| $I_{SSX}$ | Soft start charging current | | 4.3 | 5 | 6 | µA |
| $T_{ON\_MIN}$ | Minimum on time | | | 80 | 100 | ns |
| $G_{m\_EA}$ | Error amplifier trans-conductance | −2 µA < $I_{COMPX}$ < 2 µA | | 300 | | µS |
| $G_{m\_PS1/2/3}$ | COMP1/2/3 voltage to inductor current Gm | $I_{LX}$ = 0.5 A | | 7.4 | | A/V |
| $I_{LIMIT1}$ | Buck1 peak inductor current limit | | 4.33 | 5.1 | 6.02 | A |
| $I_{LIMITSOURCE1}$ | Buck1 low side source current limit | | | 4.3 | | A |
| $I_{LIMITSINK1}$ | Buck1 low side sink current limit | | | 1.3 | | A |
| $I_{LIMIT2/3}$ | Buck2/3 peak inductor current limit | | 2.6 | 3.1 | 3.73 | A |
| $I_{LIMITSOURCE2/3}$ | Buck2/3 low side source current limit | | | 2.7 | | A |
| $I_{LIMITSINK2/3}$ | Buck2/3 low side sink current limit | | | 1 | | A |
| $T_{Hiccup\_wait}$ | Overcurrent wait time | | | 256 | | cycles |
| $T_{Hiccup\_re}$ | Hiccup time before re-start | | | 8192 | | cycles |
| Rdson_HS1 | Buck1 High-side switch resistance | VIN = 12 V | | 100 | | mΩ |
| Rdson_LS1 | Buck1 low-side switch resistance | VIN = 12 V | | 65 | | mΩ |
| Rdson_HS2 | Buck2 High-side switch resistance | VIN = 12 V | | 140 | | mΩ |
| Rdson_LS2 | Buck2 low-side switch resistance | VIN = 12 V | | 95 | | mΩ |
| Rdson_HS3 | Buck3 High-side switch resistance | VIN = 12 V | | 140 | | mΩ |
| Rdson_LS3 | Buck3 low-side switch resistance | VIN = 12 V | | 95 | | mΩ |

Product Folder Links: *TPS65261 TPS65261-1*

English Data Sheet: *SLVSCD3*

## 6.5 Electrical Characteristics (continued)

$T_A$ = 25°C, $V_{IN}$ = 12 V, $f_{SW}$ = 600 kHz (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER GOOD, MODE, POWER SEQUENCE** | | | | | | |
| $V_{th\_PG}$ | Feedback voltage threshold | FBx undervoltage Falling | | 92.5 | | %$V_{REF}$ |
| | | FBx undervoltage Rising | | 95 | | %$V_{REF}$ |
| | | FBx overvoltage Rising | | 107.5 | | %$V_{REF}$ |
| | | FBx overvoltage Falling | | 105 | | %$V_{REF}$ |
| $T_{DEGLITCH(PG)\_F}$ | PGOOD falling edge deglitch time | | | 128 | | cycles |
| $T_{RDEGLITCH(PG)\_R}$ | PGOOD rising edge deglitch time | | | 512 | | cycles |
| $I_{PG}$ | PGOOD pin leakage | | | | 0.05 | µA |
| $V_{LOW\_PG}$ | PGOOD pin low voltage | $I_{SINK}$ = 1 mA | | | 0.4 | V |
| $V_{MODEH}$ | MODE high level input voltage | | | 1.2 | 1.26 | V |
| $V_{MODEL}$ | MODE low level input voltage | | 1.1 | 1.15 | | V |
| $I_{MODE1}$ | MODE pullup current | MODE = 1 V | | 3.6 | | µA |
| $I_{MODE2}$ | MODE pullup current | MODE = 1.5 V | | 6.6 | | µA |
| $T_{psdelay}$ | Delay time between bucks at automatic power sequencing mode | MODE = 1.5 V | | 1024 | | cycles |
| **POWER FAILURE DETECTOR** | | | | | | |
| $VDIV_{th}$ | VDIV threshold | | 1.18 | 1.23 | 1.26 | V |
| $I_{VDIV}$ | VDIV pullup current | VDIV = 1 V | | 1 | | µA |
| | | VDIV = 1.5 V | | 2 | | µA |
| $I_{VDIVhys}$ | VDIV hysteresis current | | | 1 | | µA |
| $T_{deglitch\_R}$ | RESET deglitch on the rising edge | | | 534 | | cycles |
| $T_{deglitch\_F}$ | RESET deglitch on the falling edge | | 12 | 14 | 16 | cycles |
| **OSCILLATOR** | | | | | | |
| $F_{SW}$ | Switching frequency | ROSC = 73.2 kΩ | 560 | 600 | 640 | kHz |
| $F_{SW\_range}$ | | | 250 | | 2000 | kHz |
| **THERMAL PROTECTION** | | | | | | |
| $T_{TRIP\_OTP}$ | Thermal protection trip point | Temperature rising | | 160 | | °C |
| $T_{HYST\_OTP}$ | | Hysteresis | | 20 | | °C |

Product Folder Links: *TPS65261 TPS65261-1*

English Data Sheet: *SLVSCD3*

## 6.6 Typical Characteristics

$T_A$ = 25°C, $V_{IN}$ = 12 V, $V_{OUT1}$ = 1.2 V, $V_{OUT2}$ = 3.3 V, $V_{OUT3}$ = 1.8 V, $f_{SW}$ = 600 kHz (unless otherwise noted)
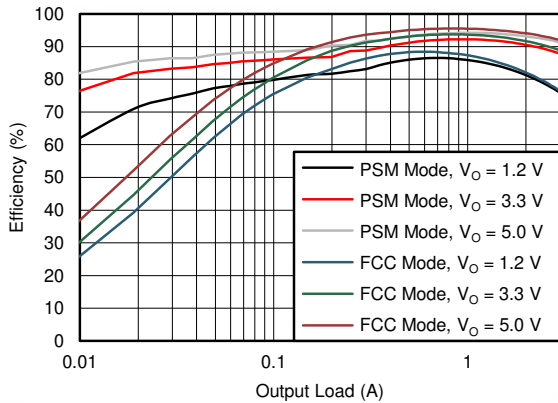


図 6-1. BUCK 1 Efficiency
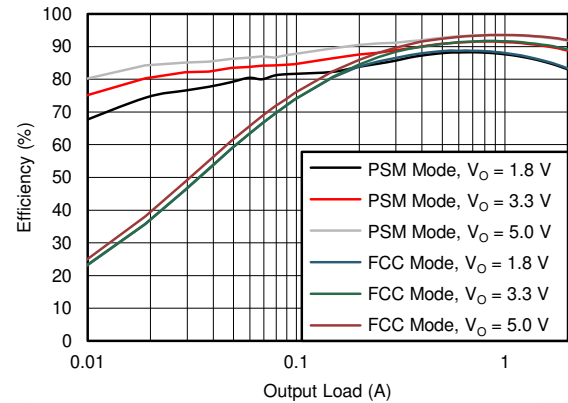


図 6-2. BUCK 2 Efficiency



$V_{OUT}$ = 1.2 V
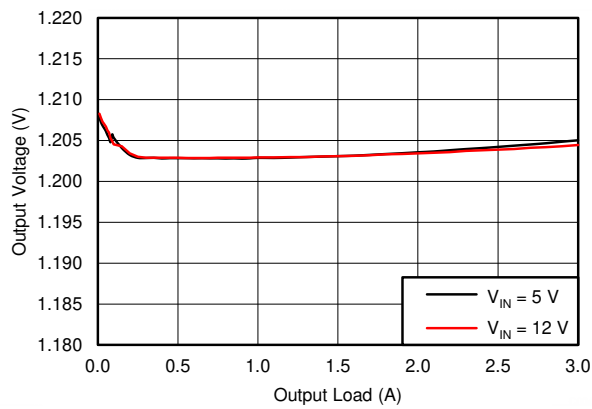
図 6-3. BUCK1, PSM Mode, Load Regulation



$V_{OUT}$ = 3.3 V
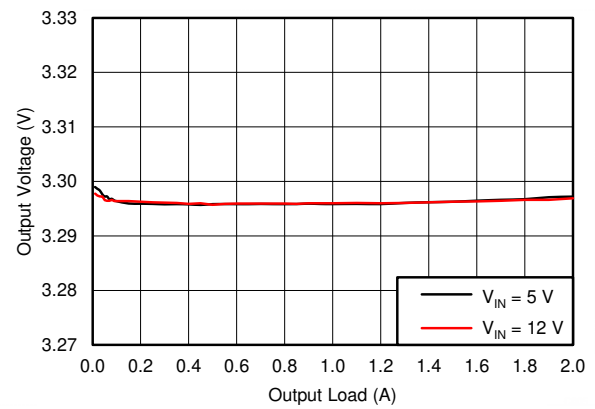
図 6-4. BUCK2, PSM Mode, Load Regulation



$V_{OUT}$ = 1.8 V
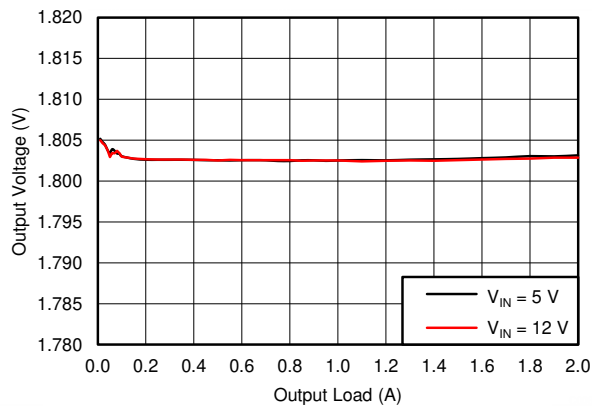
図 6-5. BUCK3, PSM Mode, Load Regulation



$V_{OUT}$ = 1.2 V
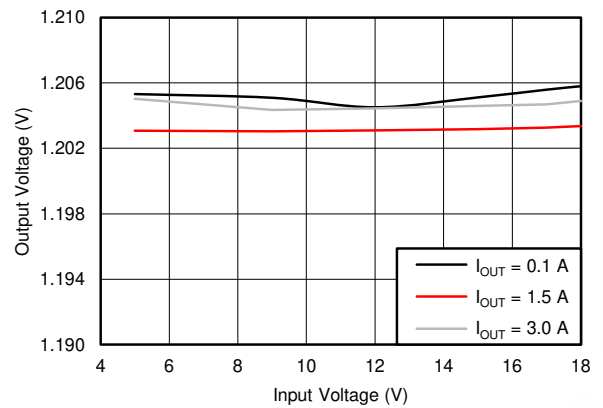
図 6-6. BUCK1, PSM Mode, Line Regulation

Product Folder Links: *TPS65261 TPS65261-1*

English Data Sheet: *SLVSCD3*

## 6.6 Typical Characteristics (continued)

$T_A$ = 25°C, $V_{IN}$ = 12 V, $V_{OUT1}$ = 1.2 V, $V_{OUT2}$ = 3.3 V, $V_{OUT3}$ = 1.8 V, $f_{SW}$ = 600 kHz (unless otherwise noted)
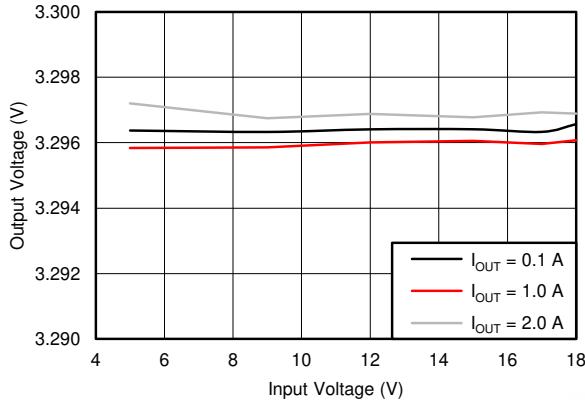
$V_{OUT}$ = 3.3 V

**図 6-7. BUCK2, PSM MODE, LINE REGULATION**
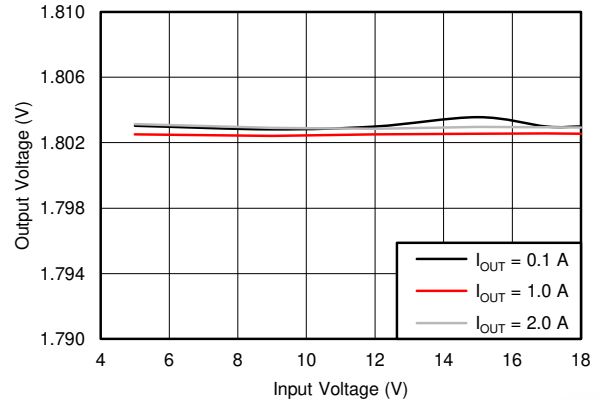
$V_{OUT}$ = 1.8 V

**図 6-8. BUCK3, PSM Mode, Line Regulation**
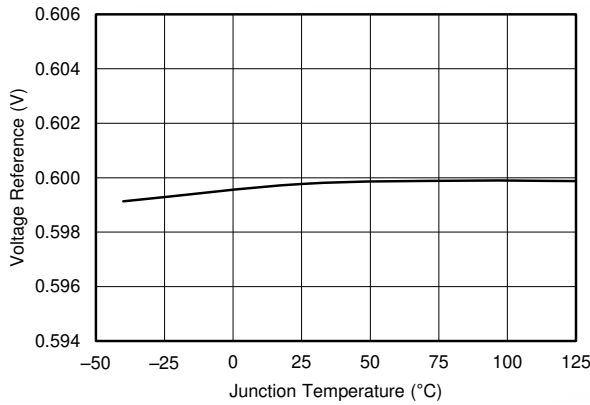
**図 6-9. Voltage Reference vs Temperature**
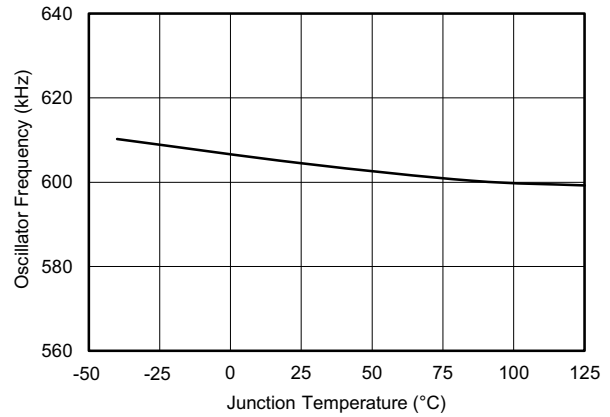
ROSC = 73.2 kΩ

**図 6-10. Oscillator Frequency vs Temperature**
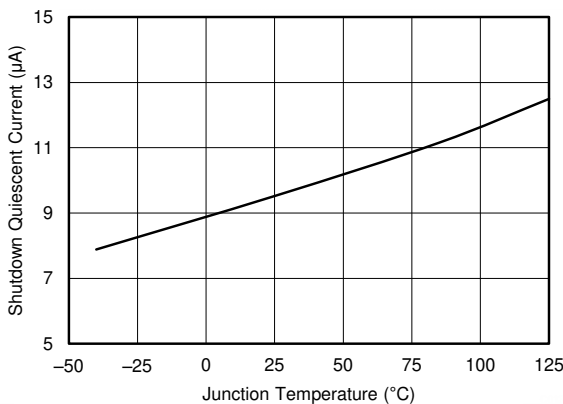
$V_{IN}$ = 12 V

**図 6-11. Shutdown Quiescent vs Temperature**
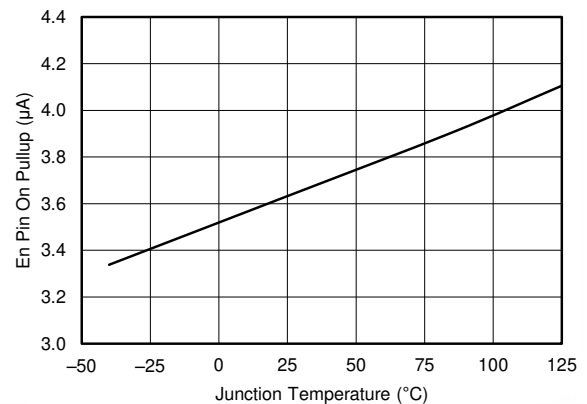
$V_{IN}$ = 12 V          EN = 1 V

**図 6-12. EN Pin Pull-Up Current vs Temperature, EN=1.0V**

Product Folder Links: *TPS65261 TPS65261-1*

English Data Sheet: SLVSCD3

## 6.6 Typical Characteristics (continued)

$T_A$ = 25°C, $V_{IN}$ = 12 V, $V_{OUT1}$ = 1.2 V, $V_{OUT2}$ = 3.3 V, $V_{OUT3}$ = 1.8 V, $f_{SW}$ = 600 kHz (unless otherwise noted)

$V_{IN}$ = 12 V          EN = 1.5 V
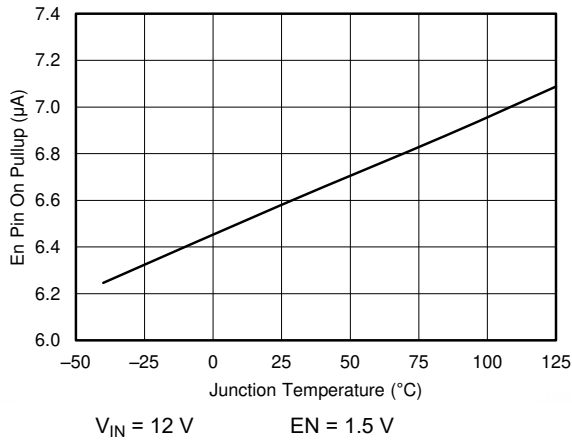
**図 6-13. EN Pin Pullup Current vs Temperature, EN = 1.5 V**

$V_{IN}$ = 12 V
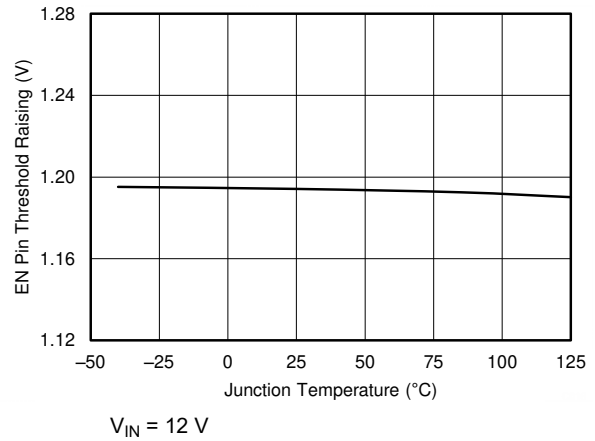
**図 6-14. EN Pin Threshold Raising vs Temperature**
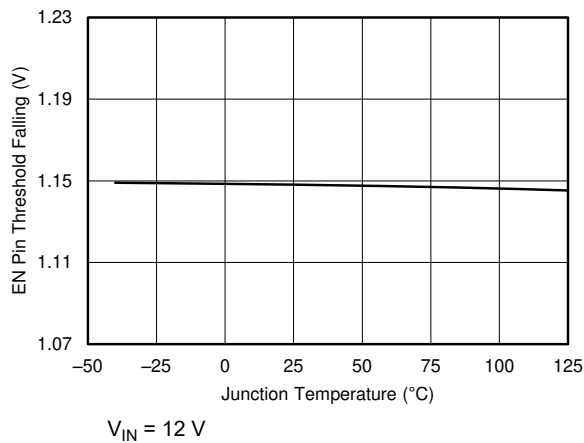
$V_{IN}$ = 12 V

**図 6-15. EN Pin Threshold Falling vs Temperature**
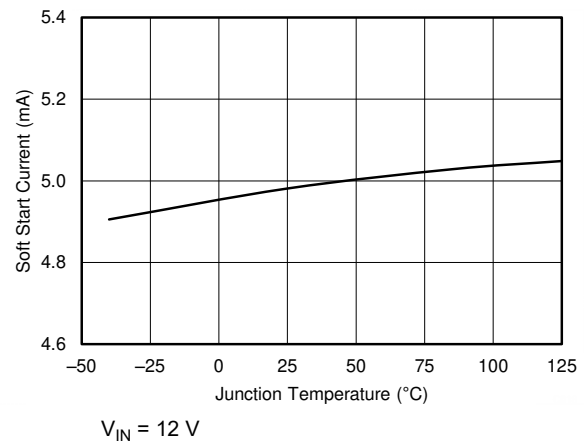
$V_{IN}$ = 12 V

**図 6-16. SS Pin Charge Current vs Temperature**
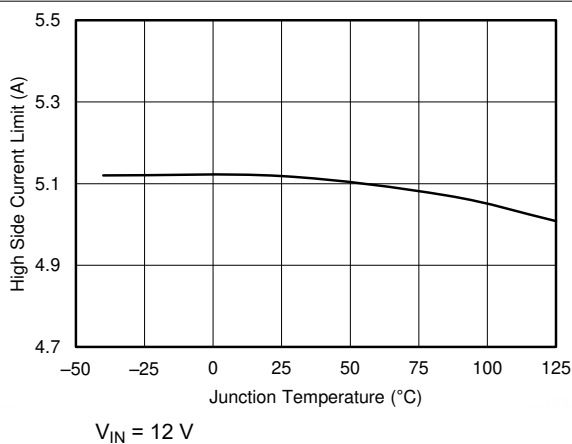
$V_{IN}$ = 12 V

**図 6-17. Buck1 High-Side Current Limit vs Temperature**
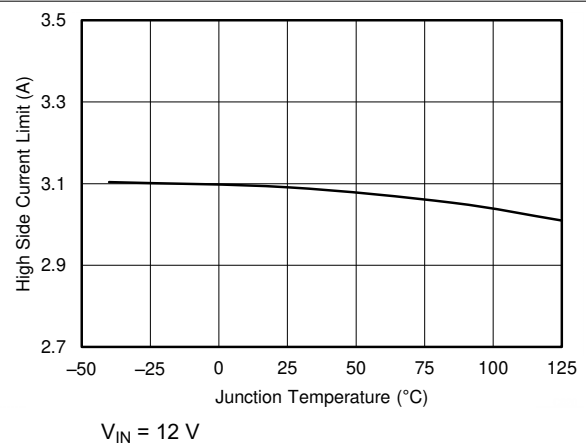
$V_{IN}$ = 12 V

**図 6-18. Buck2 High-Side Current Limit vs Temperature**

Product Folder Links: *TPS65261 TPS65261-1*

English Data Sheet: *SLVSCD3*

## 6.6 Typical Characteristics (continued)

$T_A$ = 25°C, $V_{IN}$ = 12 V, $V_{OUT1}$ = 1.2 V, $V_{OUT2}$ = 3.3 V, $V_{OUT3}$ = 1.8 V, $f_{SW}$ = 600 kHz (unless otherwise noted)
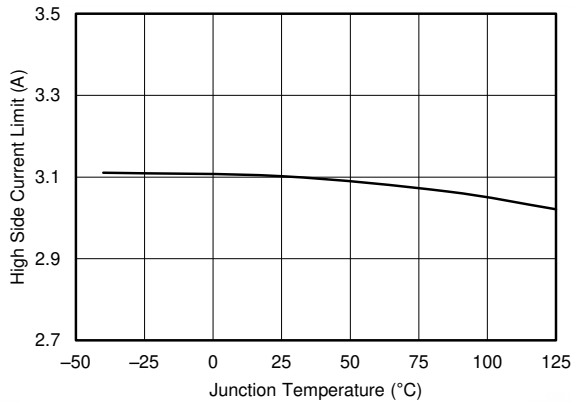


$V_{IN}$ = 12 V

図 6-19. Buck3 High-Side Current Limit vs Temperature
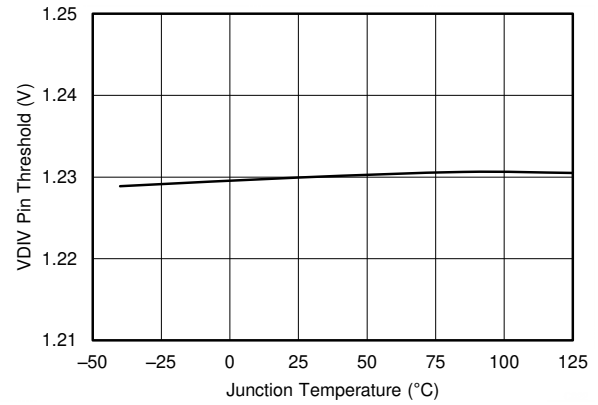
図 6-20. VDIV Pin Threshold vs Temperature

Product Folder Links: *TPS65261 TPS65261-1*

English Data Sheet: SLVSCD3

# 7 Detailed Description

## 7.1 Overview

The TPS65261, TPS65261-1 is a monolithic triple synchronous step-down (buck) converter with 3A/2A/2A output currents. A wide 4.5V to 18V input supply voltage range encompasses the most intermediate bus voltages operating off 5V, 9V, 12V or 15V power bus. The feedback voltage reference for each buck is 0.6V. Each buck is independent with dedicated enable, soft-start and loop compensation pins.

The TPS65261, TPS65261-1 implements a constant frequency, peak current mode control that simplifies external loop compensation. The wide switching frequency of 250kHz to 2MHz allows optimizing system efficiency, filtering size and bandwidth. The switching frequency can be adjusted with an external resistor connected between ROSC pin and ground. The switching clock of buck1 is 180° out-of-phase operation from the clocks of buck2 and buck3 channels to reduce input current ripple, input capacitor size and power supply induced noise.

The TPS65261, TPS65261-1 has been designed for safe monotonic startup into pre-biased loads. The default start up is when VIN is typically 4.5V. The ENx pin also can be used to adjust the input voltage under voltage lockout (UVLO) with an external resistor divider. In addition, the ENx pin has an internal 3.6uA current source, so the EN pin can be floating to automatically power up the converters.

The TPS65261, TPS65261-1 reduces the external component count by integrating a bootstrap circuit. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BST and LX pin. A UVLO circuit monitors the bootstrap capacitor voltage VBST-VLX in each buck. When $V_{BST-VLX}$ voltage drops to the threshold, LX pin is pulled low to recharge the bootstrap capacitor. The TPS65261, TPS65261-1 can operate at 100% duty cycle as long as the bootstrap capacitor voltage is higher than the BOOT-LX UVLO threshold which is typically 2.1V.

The TPS65261, TPS65261-1 features a PGOOD pin to supervise each output voltage of the buck converters. The TPS65261, TPS65261-1 has power good comparators with hysteresis, which monitor the output voltages through feedback voltages. When all bucks are in regulation range and power sequence is done, PGOOD is asserted to high.

The SS (soft start/tracking) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor or resistor divider is connected to the pin for soft start or voltage tracking.

At light loading, TPS65261 will automatically operate in pulse skipping mode (PSM) to save power.

The TPS65261, TPS65261-1 is protected from overload and over temperature fault conditions. The converter minimizes excessive output overvoltage transients by taking advantage of the power good comparator. When the output is overvoltage, the high-side MOSFET is turned off until the internal feedback voltage is lower than 105% of the 0.6V reference voltage. The TPS65261, TPS65261-1 implements both high-side MOSFET overload protection and bidirectional low-side MOSFET overload protection to avoid inductor current runaway. If the overcurrent condition has lasted for more than the OC wait time (256 clock cycles), the converter will shut down and re-start after the hiccup time (8192 clock cycles). The TPS65261, TPS65261-1 shuts down if the junction temperature is higher than the thermal shutdown trip point. When the junction temperature drops 20°C typically below the thermal shutdown trip point, the TPS65261, TPS65261-1 will be restarted under control of the soft start circuit automatically.
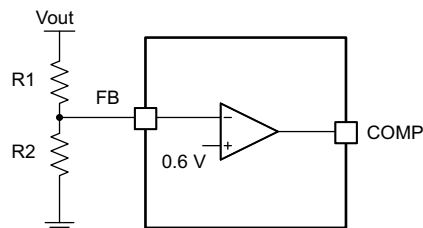
Product Folder Links: *TPS65261 TPS65261-1*

English Data Sheet: SLVSCD3

## 7.2 Functional Block Diagram
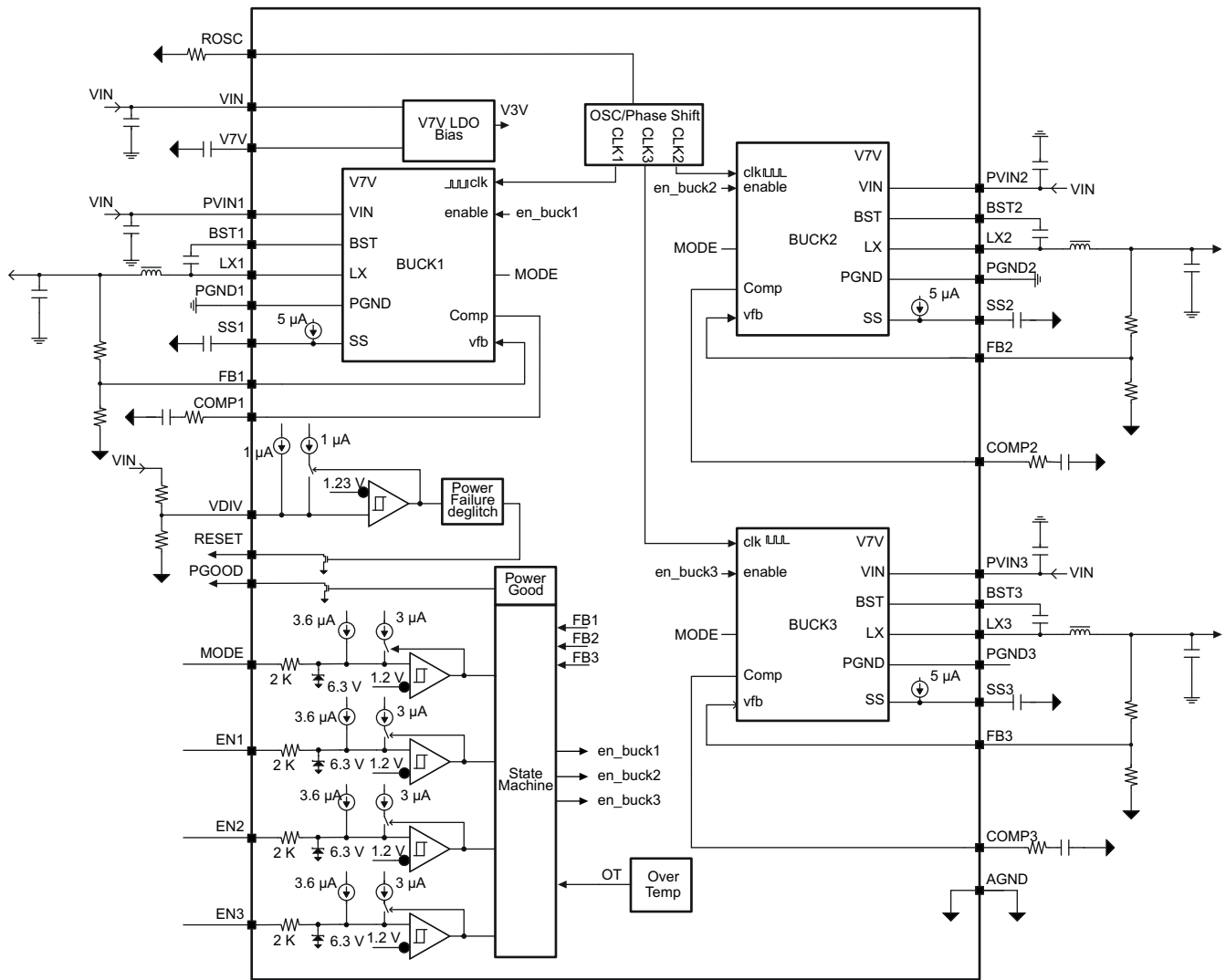


## 7.3 Feature Description

### 7.3.1 Adjusting the Output Voltage

The output voltage of each buck is set with a resistor divider from the output of buck to the FB pin. It is recommended to use 1% tolerance or better resistors.



**図 7-1. Voltage Divider Circuit**

$$R_2 = R_1 \times \frac{0.6}{V_{out} - 0.6}$$

(1)

To improve efficiency at light loads, consider using larger value resistors. If the values are too high, the regulator is more sensitive to noise. The recommended resistor values are shown in 表 7-1.

**表 7-1. Output Resistor Divider Selection**

| OUTPUT VOLTAGE (V) | R1 (kΩ) | R2 (kΩ) |
|---|---|---|
| 1 | 10 | 15 |
| 1.2 | 10 | 10 |
| 1.5 | 15 | 10 |
| 1.8 | 20 | 10 |
| 2.5 | 31.6 | 10 |
| 3.3 | 45.3 | 10 |
| 3.3 | 22.6 | 4.99 |
| 5 | 73.2 | 10 |
| 5 | 36.5 | 4.99 |

### 7.3.2 Power Failure Detector

The power failure detector monitors the voltage on VDIV, and sets open-drain output RESET low when VDIV is below 1.23V. There is deglitch on the rising edge, 534 frequency cycles. 図 7-2 shows the power failure detector timing diagram.



**図 7-2. Power Failure Detector Timing Diagram**

Product Folder Links: *TPS65261 TPS65261-1*

English Data Sheet: *SLVSCD3*
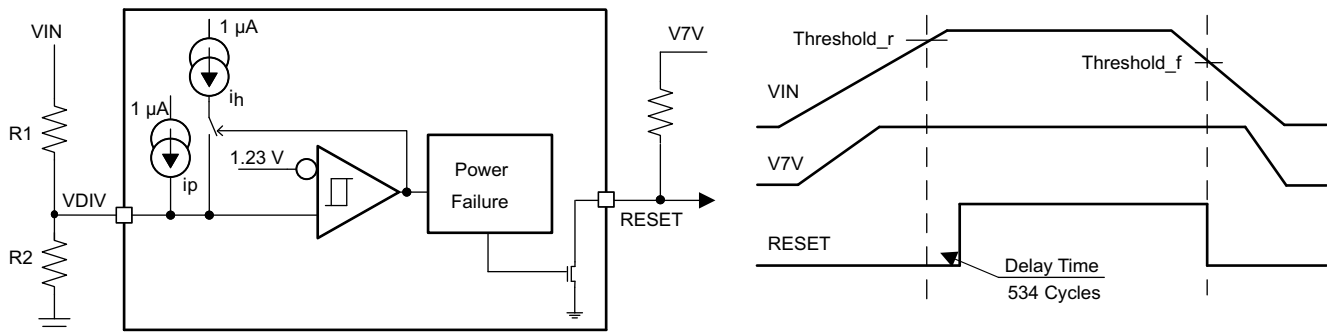
The thresholds can be calculated using 式 2 and 式 3.

$$Threshold_{\_r} = Vref\left(1 + \frac{R1}{R2}\right) - I_p \times R1 \tag{2}$$

$$Threshold_{\_f} = Vref\left(1 + \frac{R1}{R2}\right) - (I_P + I_h) \times R1 \tag{3}$$

The divider resisters can be calculated using 式 4 and 式 5.

$$R1 = \frac{Threshold_{\_r} - Threshold_{\_f}}{I_h} \tag{4}$$

$$R2 = \frac{Vref}{\dfrac{Threshold_{\_r} - Vref}{Threshold_{\_r} - Threshold_{\_f}} \times I_h + I_p} \tag{5}$$

Where $I_h = 1\mu A$, $I_p = 1\mu A$.

### 7.3.3 Enable and Adjusting Undervoltage Lockout

The EN1/2/3 pin provides electrical on/off control of the device. After the EN1/2/3 pin voltage exceeds the threshold voltage, the device starts operation. If each ENx pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low Iq state.

The EN pin has an internal pull-up current source, allowing the user to float the EN pin to enable the device. If an application requires controlling the EN pin, use open drain or open collector output logic to interface with the pin.

The device implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 500mV. If an application requires either a higher UVLO threshold on the VIN pin or a secondary UVLO on the PVINx in split rail applications, then the ENx pin can be configured as shown in 図 7-3, 図 7-4 and 図 7-5. When using the external UVLO function, it is recommended to set the hysteresis to be greater than 500mV.

The EN pin has a small pull-up current Ip which sets the default state of the pin to enable when no external components are connected. The pull-up current is also used to control the voltage hysteresis for the UVLO function because it increases by Ih after the EN pin crosses the enable threshold. The UVLO thresholds can be calculated using 式 6 and 式 7.
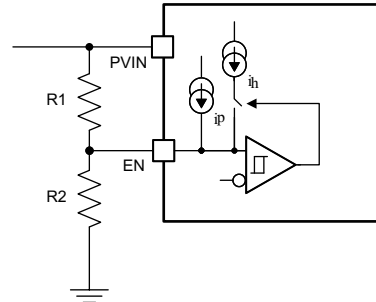
$$R_1 = \frac{V_{START}\left(\dfrac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_P\left(1 - \dfrac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \tag{6}$$

$$R_2 = \frac{R_1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLILNG} + R_1\left(I_h + I_p\right)} \tag{7}$$

Where $I_h = 3\mu A$, $I_P = 3.6uA$, $V_{ENSRISING} = 1.2V$, $V_{ENFALLING} = 1.15V$.
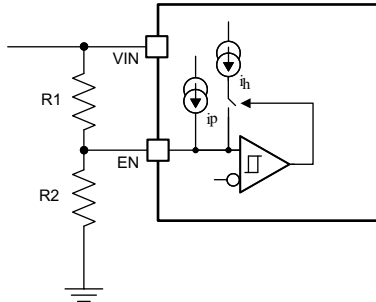
**図 7-3. Adjustable VIN Undervoltage Lockout**



**図 7-4. Adjustable PVIN Undervoltage Lockout, VIN>4.5V**
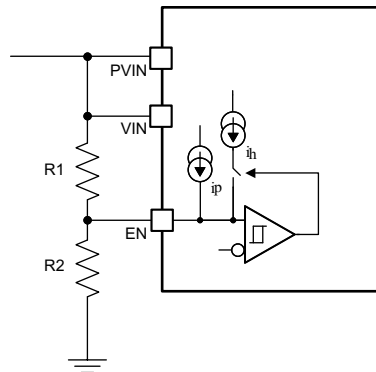


**図 7-5. Adjustable VIN and PVIN Undervoltage Lockout**

**7.3.4 Soft-Start Time**

The voltage on the respective SS pin controls the start-up of the buck output. When the voltage on the SS pin is less than the internal 0.6V reference, the TPS65261, TPS65261-1 regulates the internal feedback voltage to the voltage on the SS pin instead of 0.6V. The SS pin can be used to program an external soft-start function or to allow output of the buck to track another supply during start-up. The device has an internal pull-up current source of 5μA (typical) that charges an external soft-start capacitor to provide a linear ramping voltage at the SS pin. The TPS65261, TPS65261-1 regulates the internal feedback voltage to the voltage on the SS pin, allowing VOUT to rise smoothly from 0V to its regulated voltage without inrush current. The soft-start time can be calculated approximately by 式 8.

$$Tss(ms) = \frac{Css(nF) \times Vref(V)}{Iss(\mu A)}$$

(8)

Many of the common power supply sequencing methods can be implemented using the SSx and ENx pins. 図 7-6 shows the method implementing ratio-metric sequencing by connecting the SSx pins of three buck channels together. The regulator outputs ramp up and reach regulation at the same time. When calculating the soft-start time, the pull-up current source must be tripled in 式 8.
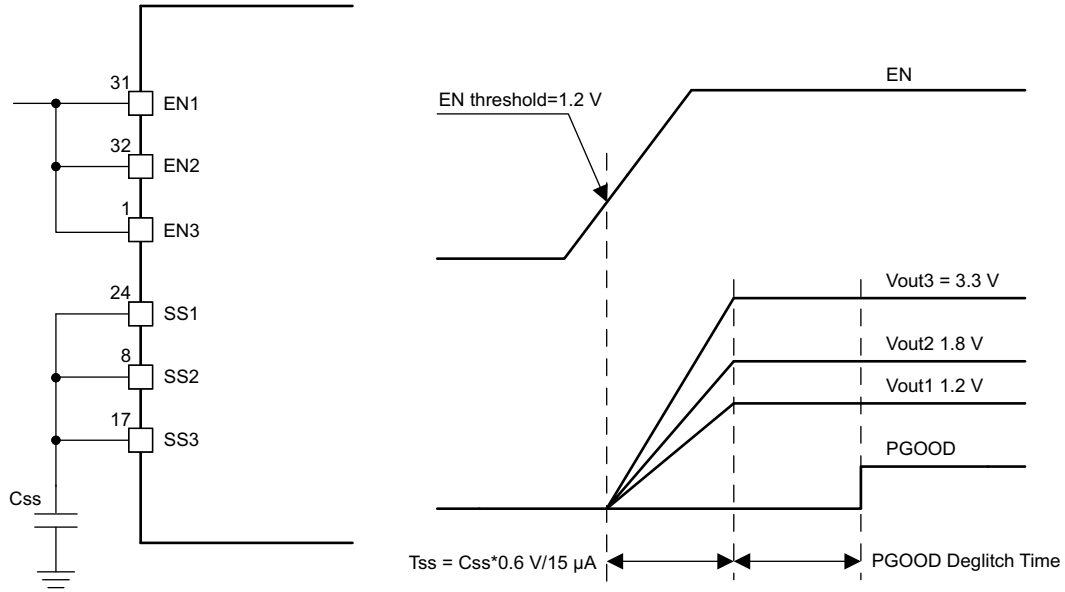
図 **7-6. Ratio Metric Power Up Using SSx Pins**

Product Folder Links: *TPS65261 TPS65261-1*

English Data Sheet: *SLVSCD3*

Simultaneous power supply sequencing can be implemented by connecting capacitor to SSx pin, shown in 図 7-7. The capacitors can be calculated using 式 8 and 式 9.

$$\frac{Css1}{Vout1} = \frac{Css2}{Vout2} = \frac{Css3}{Vout3}$$

(9)
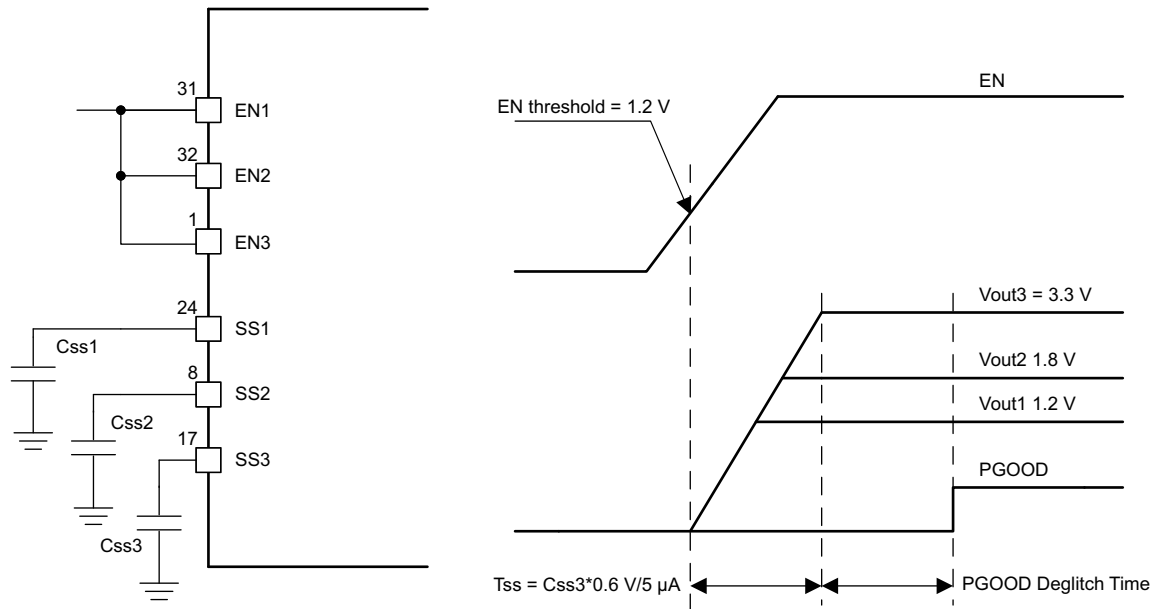


**図 7-7. Simultaneous Startup Sequence Using SSx Pins**

### 7.3.5 Power Up Sequencing

TPS65261, TPS65261-1 features a comprehensive sequencing circuit for the 3 bucks. If the MODE pin ties high to V7V, three buck start up and shutdown is in sequence according to different buck enable pin setup. If the MODE pin ties low to ground, three buck on/off is separately controlled by three enable pins.

#### 7.3.5.1 External Power Sequencing

The TPS65261, TPS65261-1 has a dedicated enable pin and soft-start pin for each converter. The converter enable pins are biased by a current source that allows for easy sequencing with the addition of an external capacitor. Disabling the converter with an active pull-down transistor on the ENs pin allows for a predictable power-down timing operation. 図 7-8 shows the timing diagram of a typical buck power-up sequence by connecting a capacitor at ENx pin.
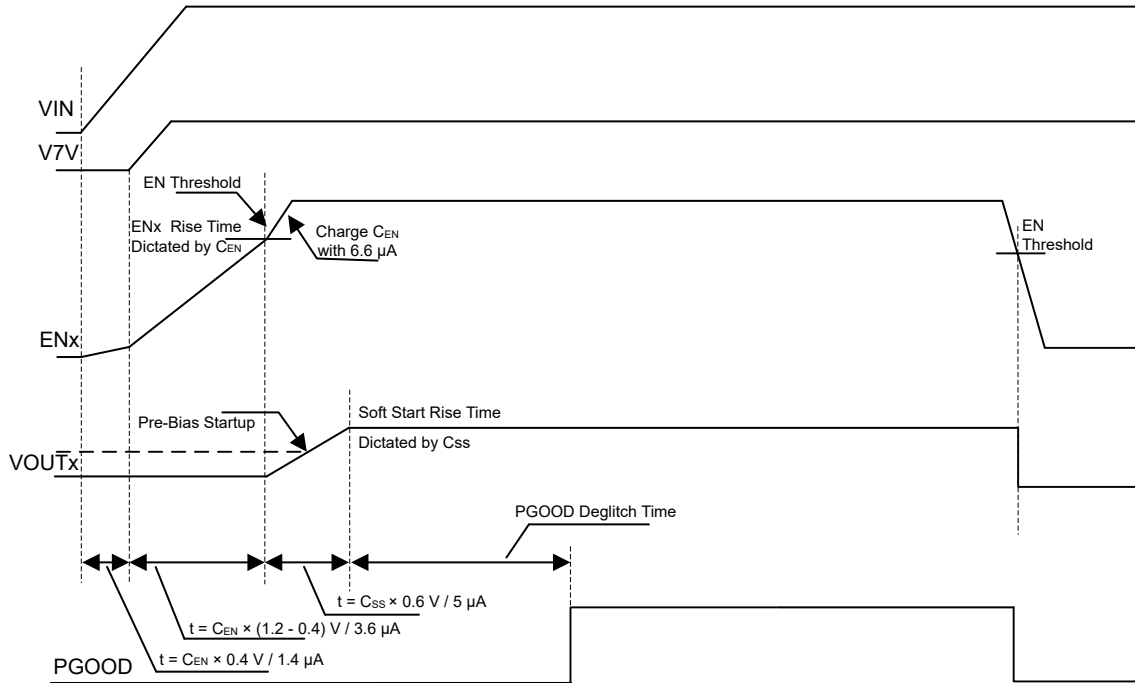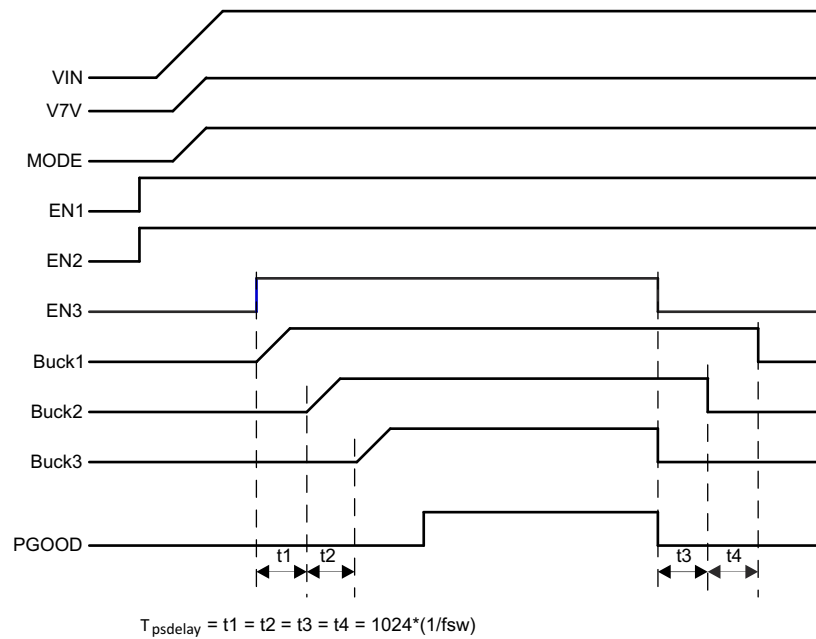
**図 7-8. Startup Power Sequence**

### 7.3.5.2 Automatic Power Sequencing

The TPS65261, TPS65261-1 starts with a pre-defined power-up and power-down sequence when the MODE pin ties high to V7V. As shown in 表 7-2, the sequence is dictated by the different combinations of EN1 and EN2 status. EN3 is used to start/stop the converters. Buck2 and buck3 are identical converters and can be swapped in the system operation to allow for additional sequencing stages. 図 7-9 shows the power sequencing when EN1 and EN2 are pulled up high.

**表 7-2. Power Sequencing**

|  | MODE | EN1 | EN2 | EN3 | Start Sequencing | Shutdown Sequencing |
|---|---|---|---|---|---|---|
| Automatic Power Sequencing | High | High | High | Used to start/stop bucks in sequence | Buck1→Buck2→Buck3 | Buck3→Buck2→Buck1 |
|  | High | Low | High |  | Buck2→Buck1→Buck3 | Buck3→Buck1→Buck2 |
|  | High | High | Low |  | Buck2→Buck3→Buck1 | Buck1→Buck3→Buck2 |
|  | High | Low | Low | Reserved | Reserved | Reserved |
| Externally controlled sequencing | Low | Used to start/stop buck1 | Used to start/stop buck2 | Used to start/stop buck3 | x | x |

Product Folder Links: *TPS65261 TPS65261-1*

English Data Sheet: *SLVSCD3*

$T_{psdelay} = t1 = t2 = t3 = t4 = 1024*(1/fsw)$

**図 7-9. Automatic Power Sequencing**

### 7.3.6 V7V Low Dropout Regulator and Bootstrap

Power for the high-side and low-side MOSFET drivers and most other internal circuitry is derived from the V7V pin. The internal built-in low dropout linear regulator (LDO) supplies 6.3V (typical) from VIN to V7V. A 10µF ceramic capacitor must be connected from V7V pin to power ground.

If the input voltage, VIN, decreases to UVLO threshold voltage, the UVLO comparator detects the V7V pin voltage and forces the converter off.

Each high-side MOSFET driver is biased from the floating bootstrap capacitor, CB, shown in 図 7-10, which is normally recharged during each cycle through an internal low-side MOSFET or the body diode of a low-side MOSFET when the high-side MOSFET turns off. The boot capacitor is charged when the BST pin voltage is less than VIN and BST-LX voltage is below regulation. The recommended value of this ceramic capacitor is 47nF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10V or higher is recommended because of the stable characteristics over temperature and voltage. Each low-side MOSFET driver is powered from the V7V pin directly.

To improve drop out, the device is designed to operate at 100% duty cycle as long as the BST to LX pin voltage is greater than the BST-LX UVLO threshold, which is typically 2.1V. When the voltage between BST and LX drops below the BST-LX UVLO threshold, the high-side MOSFET is turned off and the low-side MOSFET is turned on allowing the boot capacitor to be recharged.
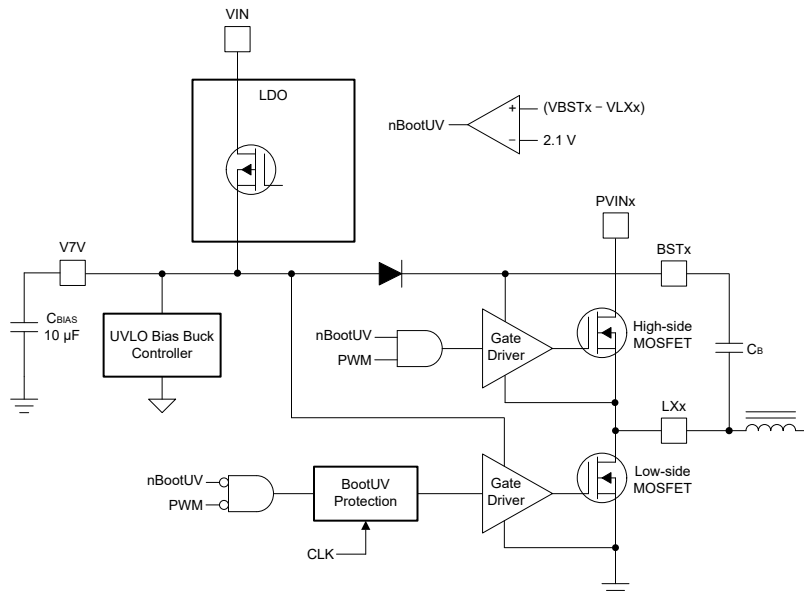
**図 7-10. V7V Linear Dropout Regulator and Bootstrap Voltage Diagram**

### 7.3.7 Out-of-Phase Operation

To reduce input ripple current, the switch clock of buck1 is 180° out-of-phase from the clock of buck2 and buck3. This enables the system, having less input current ripple, to reduce the input capacitors' size, cost and EMI.

### 7.3.8 Output Overvoltage Protection (OVP)

The device incorporates an output overvoltage protection (OVP) circuit to minimize output voltage overshoot. When the output is overloaded, the error amplifier compares the actual output voltage to the internal reference voltage. If the FB pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier demands maximum output current. After the condition is removed, the regulator output rises and the error amplifier output transitions to the steady state voltage. In some applications with small output capacitance, the load can respond faster than the error amplifier. This leads to the possibility of an output overshoot. Each buck compares the FB pin voltage to the OVP threshold. If the FB pin voltage is greater than the OVP threshold, the high-side MOSFET is turned off preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVP threshold, the high-side MOSFET turns on at the next clock cycle.

### 7.3.9 Slope Compensation

To prevent the sub-harmonic oscillations when the device operates at duty cycles greater than 50%, the device adds built-in slope compensation, which is a compensating ramp to the switch current signal.

### 7.3.10 Overcurrent Protection

The device is protected from overcurrent conditions with cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET.

#### 7.3.10.1 High-side MOSFET Overcurrent Protection

The device implements current mode control which uses the COMP pin voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle-by-cycle basis. During each cycle, the switch current and the current reference generated by the COMP pin voltage are compared, when the peak switch current intersects the current reference, the high-side switch is turned off.

### 7.3.10.2 Low-side MOSFET Overcurrent Protection

While the low-side MOSFET is turned on, its conduction current is monitored by the internal circuitry. During normal operation, the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current limit. If the low-side sourcing current is exceeded, the high-side MOSFET is not turned on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET is turned on again when the low-side current is below the low-side sourcing current limit at the start of a cycle.

The low-side MOSFET can also sink current from the load. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario both MOSFETs are off until the start of the next cycle.

Furthermore, if an output overload condition (as measured by the COMP pin voltage) has lasted for more than the hiccup wait time which is programmed for 256 switching cycles shown in 図 7-11, the device will shut down itself and restart after the hiccup time of 8192 cycles. The hiccup mode helps reduce the device power dissipation under severe overcurrent condition.
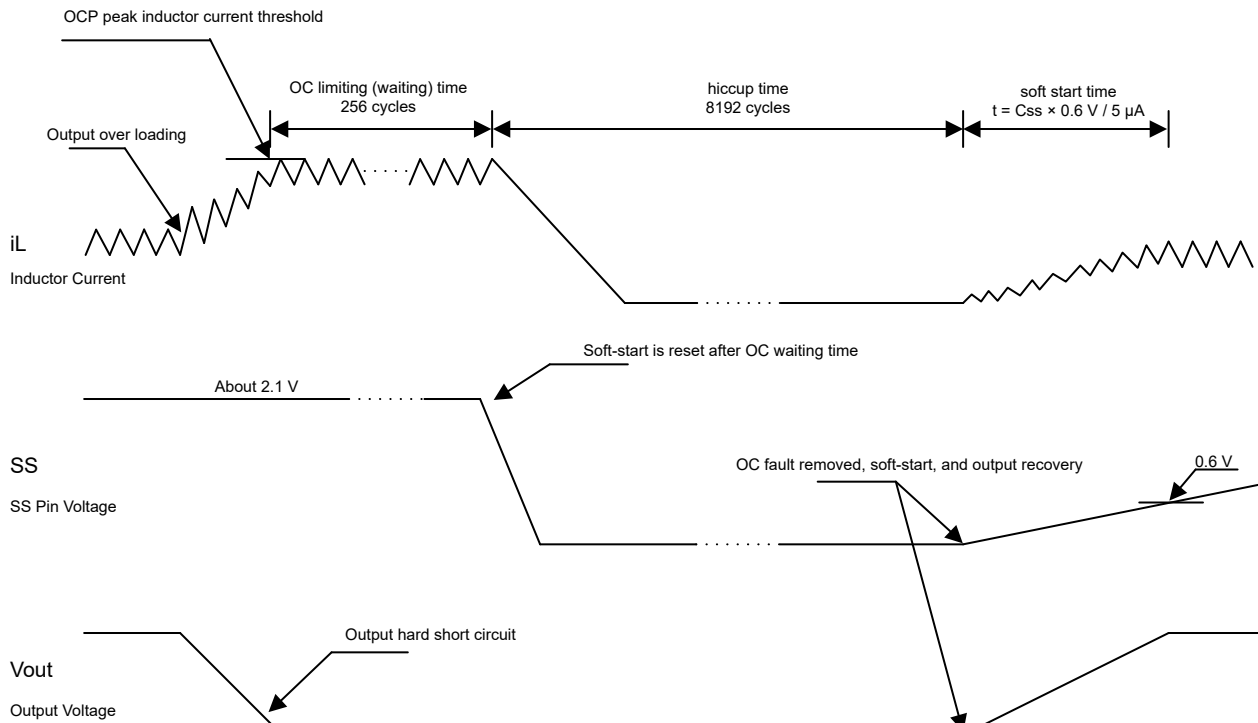


**図 7-11. Overcurrent Protection**

### 7.3.11 Power Good

The PGOOD pin is an open drain output. After feedback voltage of each buck is between 95% (rising) and 105% (falling) of the internal voltage reference, the PGOOD pin pull-down is de-asserted and the pin floats. It is recommended to use a pull-up resistor between the values of 10kΩ and 100kΩ to a voltage source that is 5.5V or less. The PGOOD is in a defined state after the VIN input voltage is greater than 1V, but with reduced current sinking capability. The PGOOD achieves full current sinking capability after the VIN input voltage is above UVLO threshold, which is 4.25V.

The PGOOD pin is pulled low when any feedback voltage of a buck is lower than 92.5% (falling) or greater than 107.5% (rising) of the nominal internal reference voltage. Also, the PGOOD is pulled low if the input voltage is

undervoltage locked up, thermal shutdown is asserted, the EN pin is pulled low or the converter is in a soft-start period.

### 7.3.12 Adjustable Switching Frequency

The ROSC pin can be used to set the switching frequency by connecting a resistor to GND. The switching frequency of the device is adjustable from 250KHz to 2MHz.

To determine the ROSC resistance for a given switching frequency, use 式 10 or the curve in 図 7-12. To reduce the solution size, set the switching frequency as high as possible, but tradeoffs of the supply efficiency and minimum controllable on time must be considered.

$$f_{osc}(kHz) = 39557 \times R(k\Omega)^{-0.975} \tag{10}$$
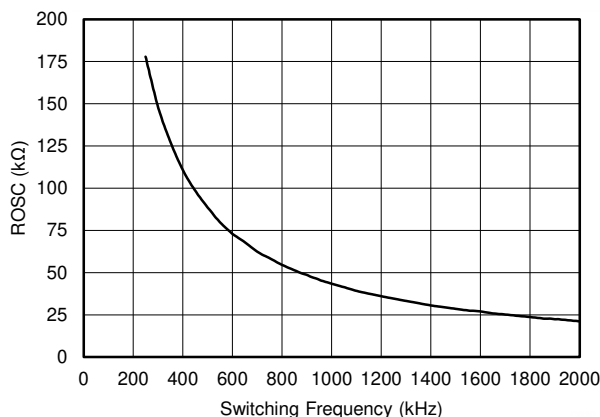
**図 7-12. ROSC versus Switching Frequency**

### 7.3.13 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160°C typically. The device reinitiates the power up sequence when the junction temperature drops below 140°C typically.

## 7.4 Device Functional Modes

### 7.4.1 Pulse Skipping MODE (PSM)

The TPS65261 can enter high efficiency pulse skipping mode (PSM) operation at light load current.

When a controller is enabled for PSM operation, the peak inductor current is sensed and compared with 230mA current typically. Because the integrated current comparator catches the peak inductor current only, the average load current entering PSM varies with applications and external output filters. In PSM, the sensed peak inductor current is clamped at 230mA.

When a controller operates in PSM, the inductor current is not allowed to reverse. The reverse current comparator turns off the low-side MOSFET when the inductor current reaches zero, preventing it from reversing and going negative.

Due to the delay in the circuit and current comparator tdly (typical 50ns at $V_{IN}$ = 12V), the real peak inductor current threshold to turn off high-side power MOSFET, can shift higher depending on inductor inductance and input/output voltages. The threshold of peak inductor current to turn off high-side power MOSFET can be calculated by 式 11.

$$IL_{PEAK} = 230 \text{ mA} + \frac{Vin - Vout}{L} \times tdly \tag{11}$$

After the charge accumulated on the Vout capacitor is more than loading need, COMP pin voltage drops to low voltage driven by the error amplifier. There is an internal comparator at the COMP pin. If COMP voltage is lower than 0.35V, the power stage stops switching to save power.
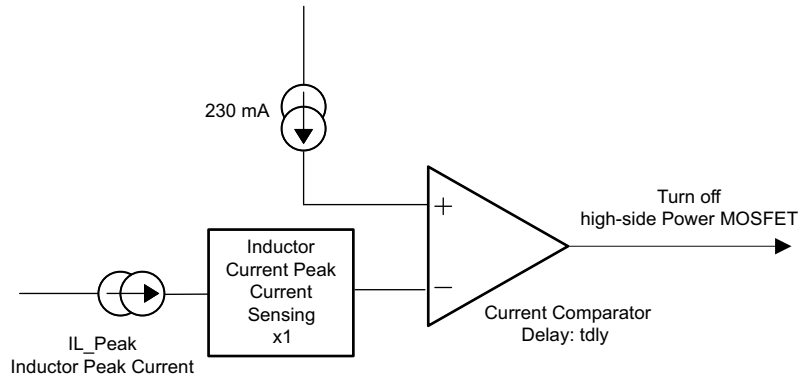
**図 7-13. PSM Current Comparator**

Product Folder Links: *TPS65261 TPS65261-1*

English Data Sheet: SLVSCD3

# 8 Application and Implementation

注

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## 8.1 Application Information

The devices are triple synchronous step down dc/dc converters. They are typically used to convert a higher dc voltage to lower dc voltages with continuous available output current of 3A/2A/2A. The following design procedure can be used to select component values for the TPS65261 and TPS65261-1. This section presents a simplified discussion of the design process.

## 8.2 Typical Application
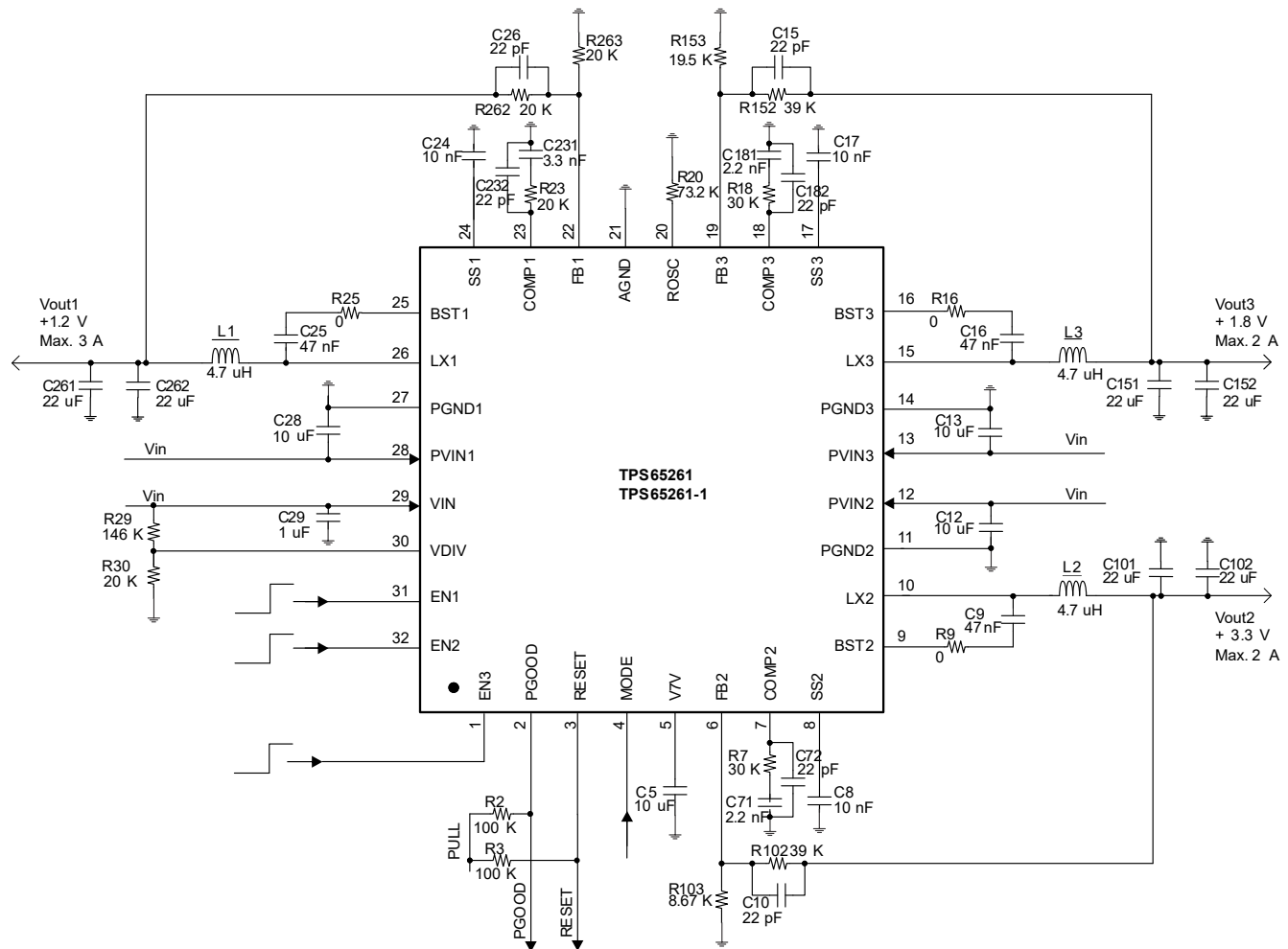


**図 8-1. Typical Application Schematic**

### 8.2.1 Design Requirements

This example details the design of triple synchronous step-down converter. A few parameters must be known in order to start the design process. These parameters are typically determined at the system level. For this example, we start with the following known parameters:

表 8-1. Design Parameters

| DESIGN PARAMETER | EXAMPLE VALUE |
| --- | --- |
| Vout1 | 1.2 V |
| Iout1 | 3 A |
| Vout2 | 3.3 V |
| Iout2 | 2 A |
| Vout3 | 1.8 V |
| Iout3 | 2 A |
| Transient Response 1A Load Step | ±5% |
| Input Voltage | 12 V normal, 4.5 V to 18 V |
| Output Voltage Ripple | ±1% |
| Switching Frequency | 600 kHz |

### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 Output Inductor Selection

To calculate the value of the output inductor, use 式 12. LIR is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impact the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, LIR is normally from 0.1 to 0.3 for the majority of applications.

$$L = \frac{V_{inmax} - V_{out}}{I_o \times LIR} \times \frac{V_{out}}{V_{in\,max} \times f_{sw}}$$

(12)

For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from 式 14 and 式 15.

$$I_{ripple} = \frac{V_{inmax} - V_{out}}{L} \times \frac{V_{out}}{V_{inmax} \times f_{sw}}$$

(13)

$$I_{Lrms} = \sqrt{I_O^2 + \frac{\left(\dfrac{V_{out} \times (V_{inmax} - V_{out})}{V_{inmax} \times L \times f_{sw}}\right)^2}{12}}$$

(14)

$$I_{Lpeak} = I_{out} + \frac{I_{ripple}}{2}$$

(15)

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

#### 8.2.2.2 Output Capacitor Selection

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current when the regulator cannot. This situation can occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as a transition from no load to full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of drop in the output voltage. 式 16 shows the minimum output capacitance necessary to accomplish this.

$$C_o = \frac{2 \times \Delta I_{out}}{f_{sw} \times \Delta V_{out}}$$
(16)

Where $\Delta I_{out}$ is the change in output current, $f_{sw}$ is the regulators switching frequency and $\Delta V_{out}$ is the allowable change in the output voltage.

式 17 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where $f_{sw}$ is the switching frequency, $V_{oripple}$ is the maximum allowable output voltage ripple, and $I_{oripple}$ is the inductor ripple current.

$$C_o > \frac{1}{8 \times f_{sw}} \times \frac{1}{\dfrac{V_{oripple}}{I_{oripple}}}$$
(17)

式 18 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification.

$$R_{esr} < \frac{V_{oripple}}{I_{oripple}}$$
(18)

Additional capacitance de-ratings for aging, temperature and DC bias must be factored in, which increases this minimum value. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the root mean square (RMS) value of the maximum ripple current. 式 19 can be used to calculate the RMS ripple current the output capacitor needs to support.

$$I_{corms} = \frac{V_{out} \times (V_{inmax} - V_{out})}{\sqrt{12} \times V_{inmax} \times L \times f_{sw}}$$
(19)

#### 8.2.2.3 Input Capacitor Selection

The TPS65261, TPS65261-1 requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 10 µF of effective capacitance on the PVIN input voltage pins. In some applications, additional bulk capacitance can also be required for the PVIN input. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of The TPS65261, TPS65261-1. The input ripple current can be calculated using 式 20.

English Data Sheet: SLVSCD3

$$I_{inrms} = I_{out} \times \sqrt{\frac{V_{out}}{V_{in\,min}} \times \frac{(V_{in\,min} - V_{out})}{V_{in\,min}}}$$

(20)

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using 式 21.

$$\Delta V_{in} = \frac{I_{out\,max} \times 0.25}{C_{in} \times f_{sw}}$$

(21)

### 8.2.2.4 Loop Compensation

The TPS65261, TPS65261-1 incorporates a peak current mode control scheme. The error amplifier is a trans-conductance amplifier with a gain of 300 µS. A typical type II compensation circuit adequately delivers a phase margin between 60° and 90°. $C_b$ adds a high frequency pole to attenuate high frequency noise when needed. To calculate the external compensation components, follow these steps.

1. Select switching frequency $f_{sw}$ that is appropriate for application depending on L and C sizes, output ripple, and EMI. Switching frequency between 500kHz to 1MHz gives best trade-off between performance and cost. To optimize efficiency, lower switching frequency is desired.
2. Set up cross over frequency, $fc$, which is typically between 1/5 and 1/20 of $f_{sw}$.
3. $R_C$ can be determined by

$$R_C = \frac{2\pi \times fc \times Vo \times Co}{G_{m-EA} \times Vref \times G_{m-PS}}$$

(22)

Where $G_{m\_EA}$ is the error amplifier gain (300µS), $G_{m\_PS}$ is the power stage voltage to current conversion gain (7.4A/V).

4. Calculate $C_C$ by placing a compensation zero at or before the dominant pole $\left( fp = \frac{1}{C_o \times R_L \times 2\pi} \right)$.

$$C_C = \frac{R_L \times Co}{R_C}$$

(23)

5. Optional $C_b$ can be used to cancel the zero from the ESR associated with $C_O$.

$$C_b = \frac{R_{ESR} \times Co}{R_C}$$

(24)
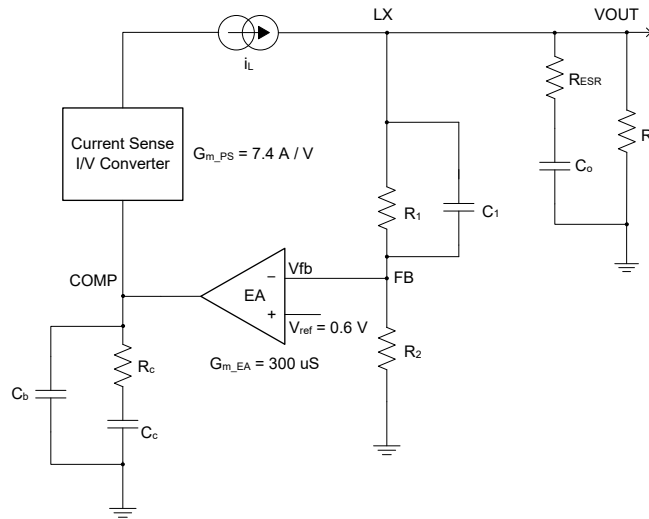
**図 8-2. DC/DC Loop Compensation**

Product Folder Links: *TPS65261 TPS65261-1*

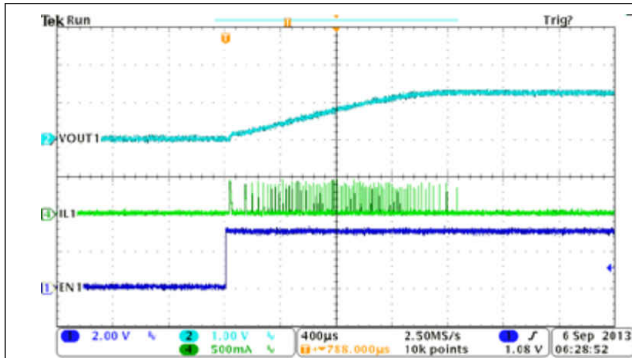English Data Sheet: *SLVSCD3*

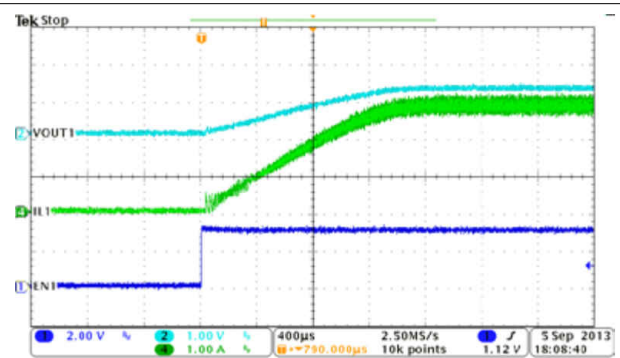### 8.2.3 Application Curves

図 8-3. BUCK1, Soft-Start with No Load
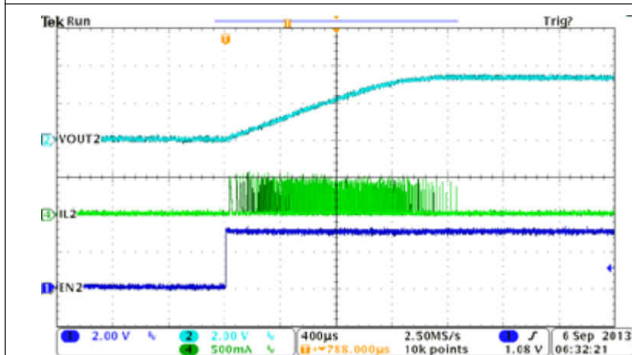
図 8-4. BUCK1, Soft-Start with Full Load
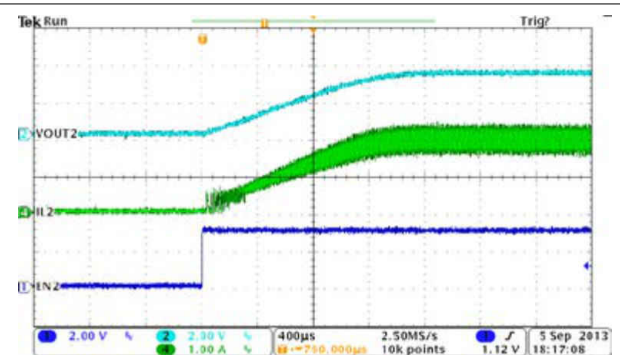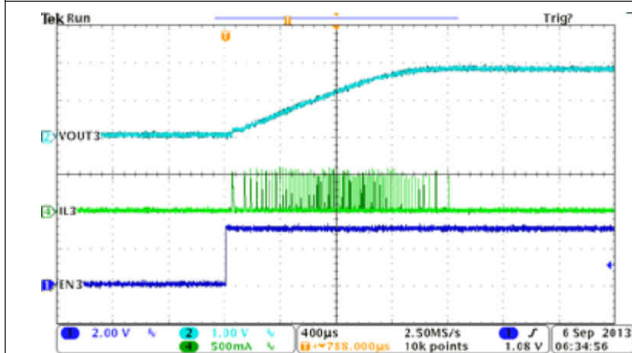
図 8-5. BUCK2, Soft-Start with No Load

図 8-6. BUCK2, Soft-Start with Full Load

図 8-7. BUCK3, Soft-Start with No Load

図 8-8. BUCK3, Soft-Start with Full Load
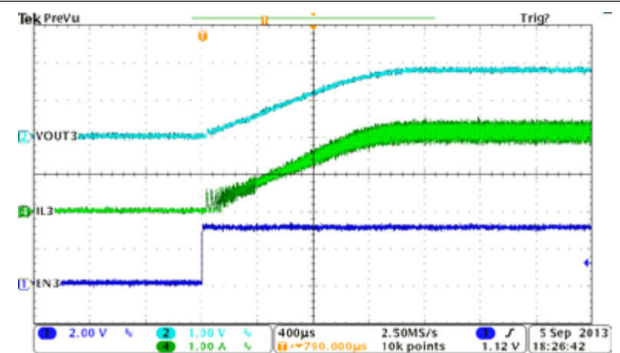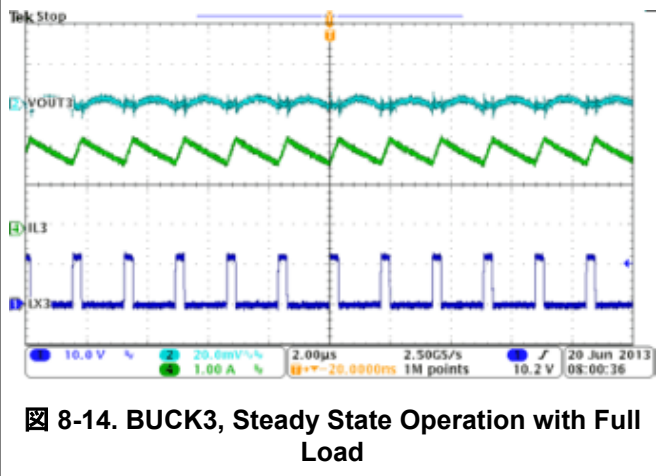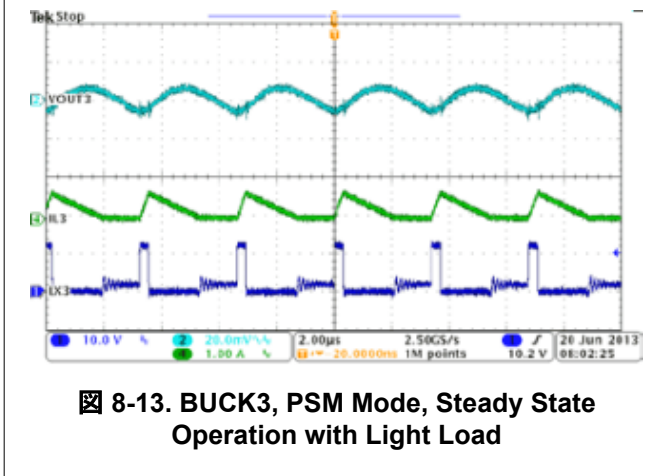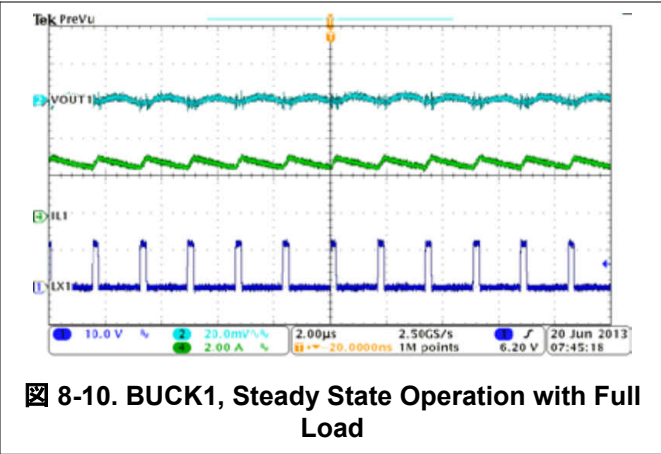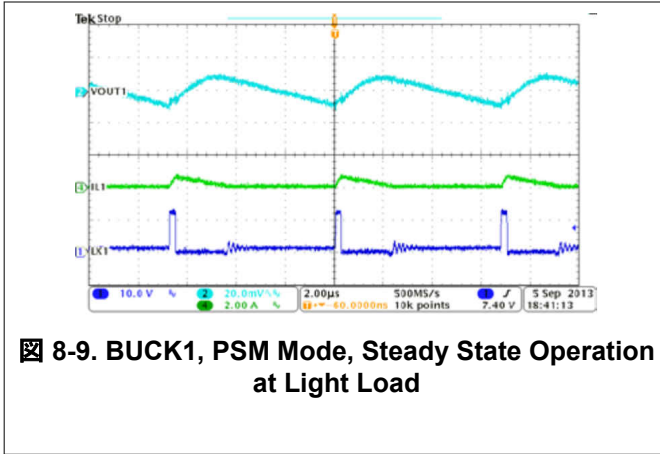
Product Folder Links: *TPS65261 TPS65261-1*

English Data Sheet: SLVSCD3

図 8-9. BUCK1, PSM Mode, Steady State Operation at Light Load



図 8-10. BUCK1, Steady State Operation with Full Load



図 8-11. BUCK2, PSM Mode, Steady State Operation at Light Load



図 8-12. BUCK2, Steady State Operation with Full Load



図 8-13. BUCK3, PSM Mode, Steady State Operation with Light Load



図 8-14. BUCK3, Steady State Operation with Full Load

Product Folder Links: *TPS65261 TPS65261-1*

English Data Sheet: SLVSCD3

**図 8-15. BUCK1, Load Transient, 0.75 A to 1.5 A SR = 0.25 A/μs**
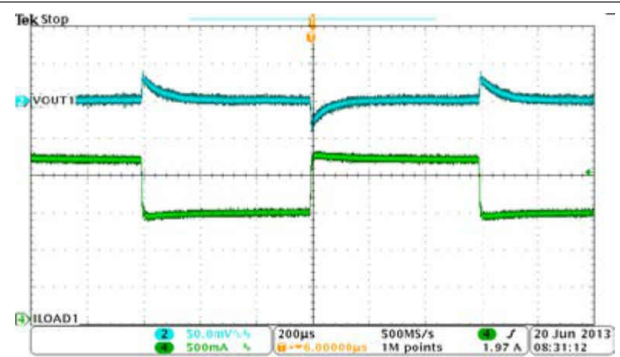
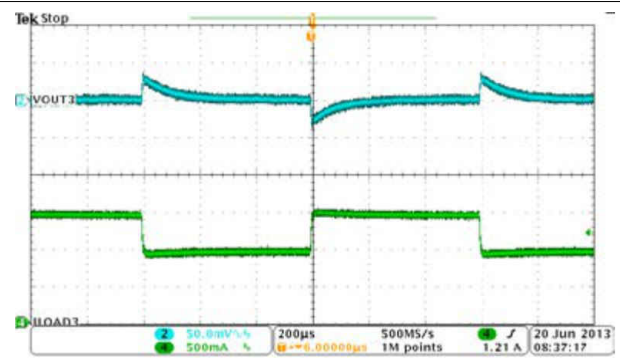**図 8-16. BUCK1, Load Transient, 1.5 A to 2.25 A SR = 0.25 A/μs**
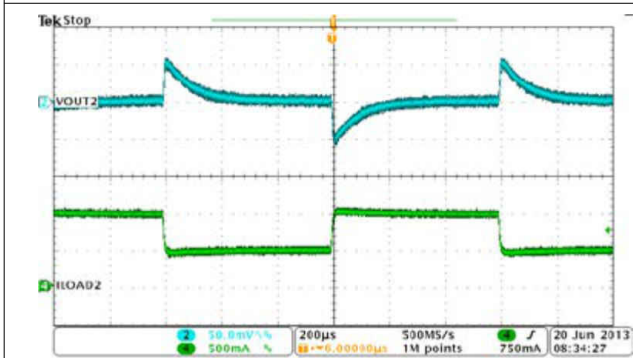
**図 8-17. BUCK2, Load Transient, 0.5 A to 1.0 A SR = 0.25 A/μs**
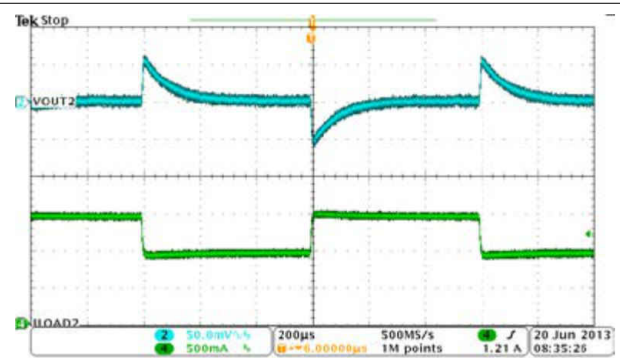
**図 8-18. BUCK2, Load Transient, 1.0 A to 1.5 A SR = 0.25 A/μs**
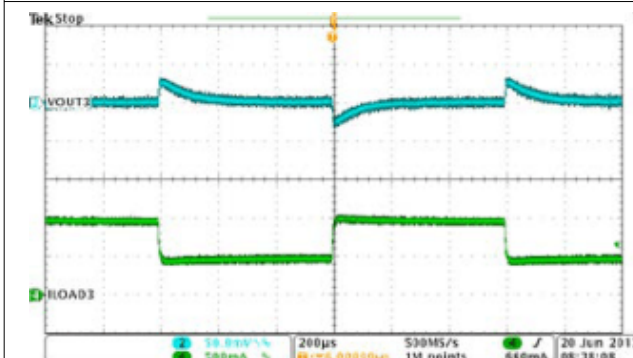
**図 8-19. BUCK3, Load Transient, 0.5 A to 1.0 A SR = 0.25 A/μs**

**図 8-20. BUCK3, Load Transient, 1.0 A to 1.5 A SR = 0.25 A/μs**

Product Folder Links: *TPS65261 TPS65261-1*
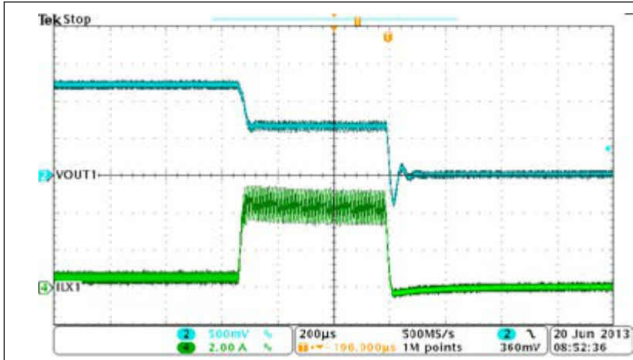
English Data Sheet: SLVSCD3
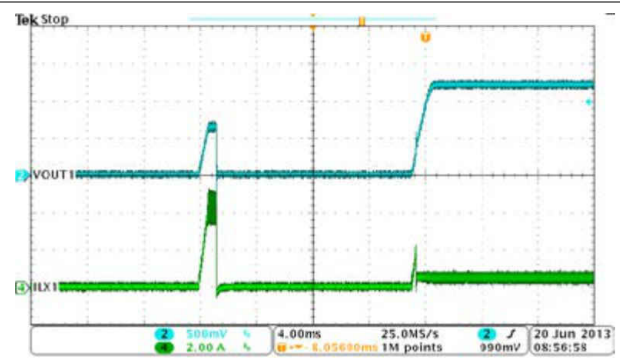
図 8-21. BUCK1, Overcurrent Protection


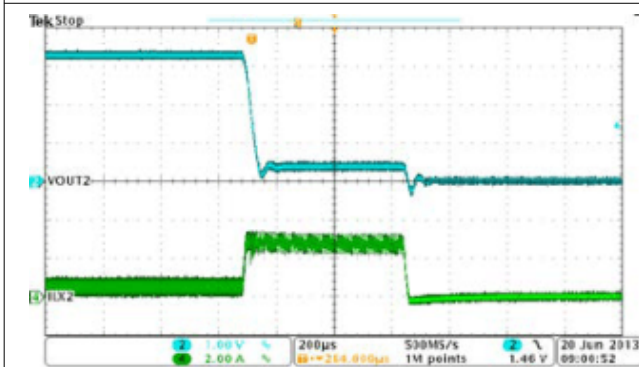図 8-22. BUCK1, Hiccup and Recovery


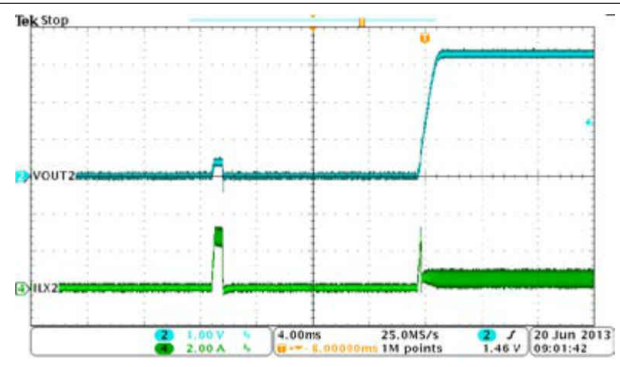図 8-23. BUCK2, Overcurrent Protection


図 8-24. BUCK2, Hiccup and Recovery
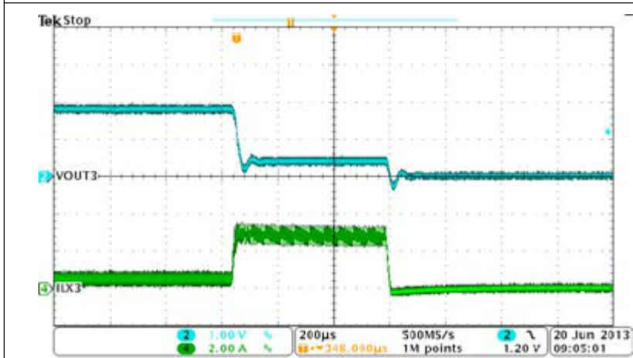

図 8-25. BUCK3, Overcurrent Protection


図 8-26. BUCK3, Hiccup and Recovery

Product Folder Links: *TPS65261 TPS65261-1*

English Data Sheet: SLVSCD3
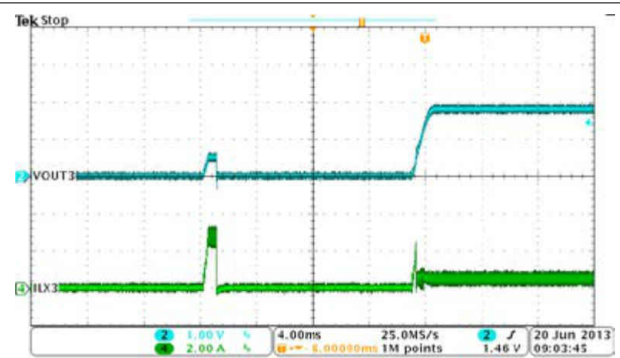
図 8-27. Automatic Power Sequencing,
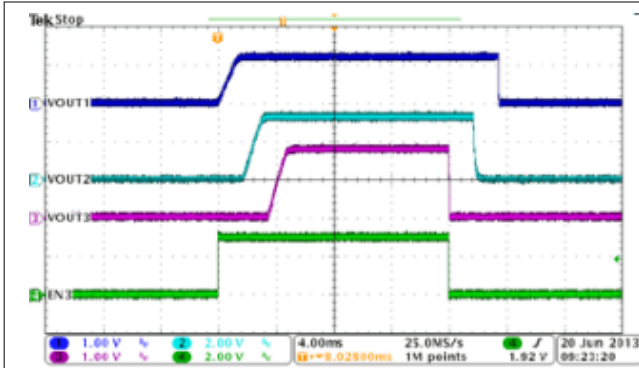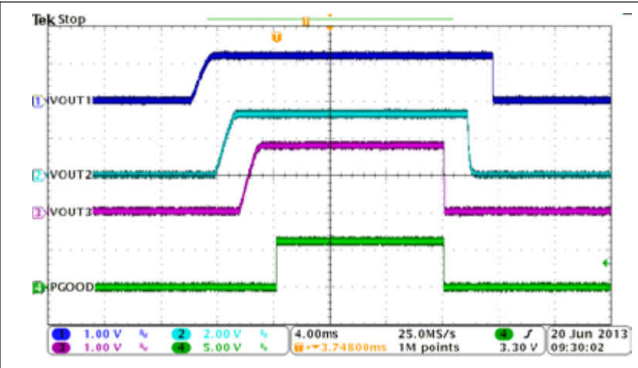MODE=EN1=EN2=HIGH
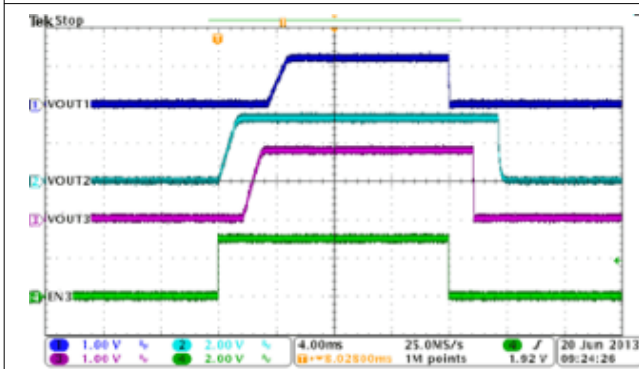
図 8-28. Automatic Power Sequencing,
MODE=EN1=EN2=HIGH

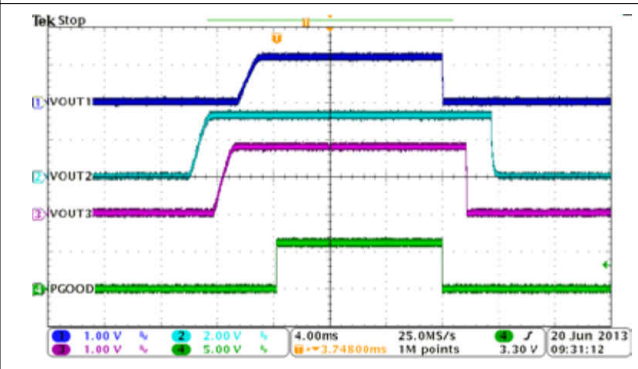図 8-29. Automatic Power Sequencing,
MODE=EN1= HIGH, EN2=LOW

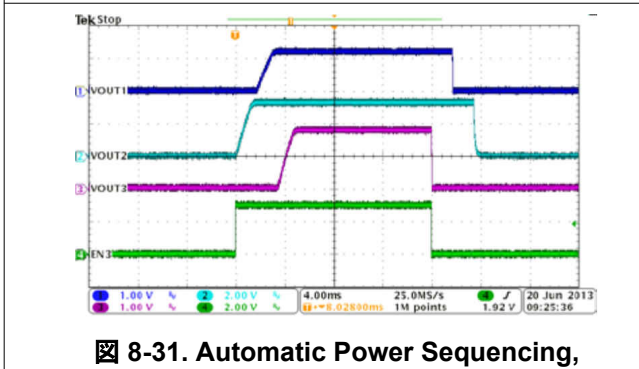図 8-30. Automatic Power Sequencing,
MODE=EN1=HIGH, EN2=LOW

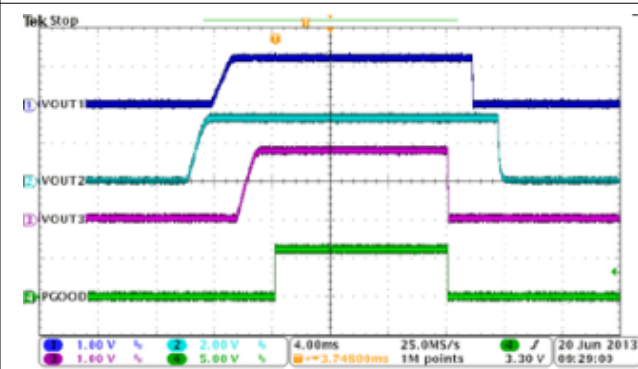図 8-31. Automatic Power Sequencing,
MODE=EN2=HIGH, EN1=LOW

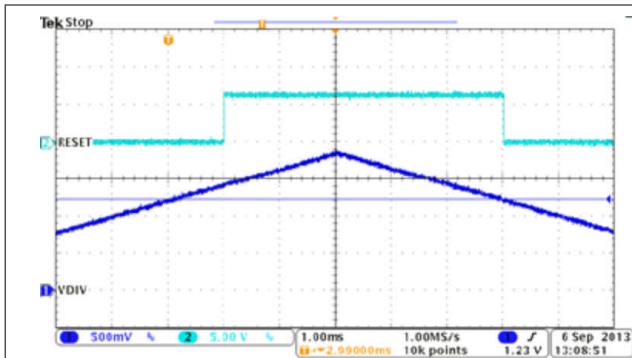図 8-32. Automatic Power Sequencing,
MODE=EN2=HIGH, EN1=LOW

Product Folder Links: TPS65261 TPS65261-1

English Data Sheet: SLVSCD3

図 8-33. Trigger Voltage 1.23V, Reset vs VDIV
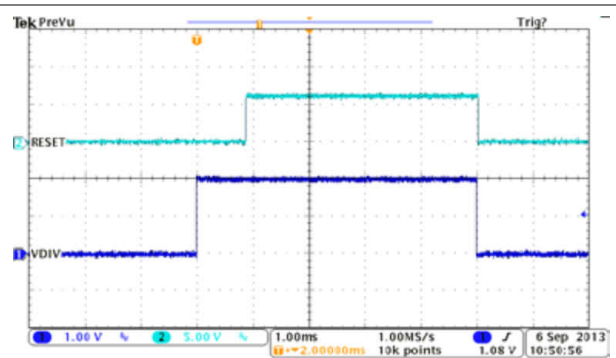


図 8-34. Deglitch Time, Reset vs VDIV
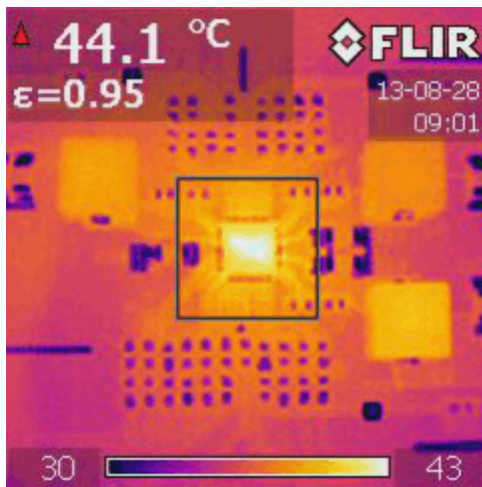


$V_{IN}$ = 12 V      $V_{OUT1}$ = 1.2 V/1.5 A      $V_{OUT2}$ = 3.3 V/1 A
$V_{OUT3}$ = 1.8 V/1 A
EVM Condition 4 Layers, 64 mm × 69 mm, $T_A$ = 27.2°C

図 8-35. Thermal Signature of TPS65261EVM
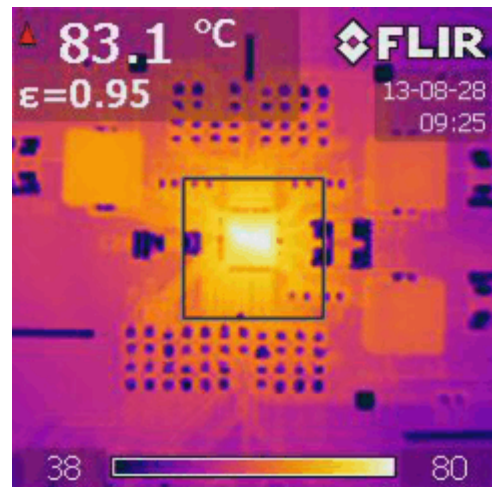


$V_{IN}$ = 12 V      $V_{OUT1}$ = 1.2 V/3 A      $V_{OUT2}$ = 3.3 V/2 A
$V_{OUT3}$ = 1.8 V/2 A
EVM Condition 4 Layers, 64 mm × 69 mm, $T_A$ = 27.2°C

図 8-36. Thermal Signature of TPS65261EVM

## 8.3 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 4.5 V and 18 V. This input power supply must be well regulated. If the input supply is located more than a few inches from the TPS65261 or TPS65261-1 converter additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 μF is a typical choice.

## 8.4 Layout

### 8.4.1 Layout Guidelines

The TPS65261, TPS65261-1 can be laid out on 2-layer PCB, illustrated in 図 8-37.

Layout is a critical portion of good power supply design. See 図 8-37 for a PCB layout example. The top contains the main power traces for PVIN, VOUT, and LX. Also on the top layer are connections for the remaining pins of the TPS65261, TPS65261-1 and a large top side area filled with ground. The top layer ground area must be connected to the bottom layer ground using vias at the input bypass capacitor, the output filter capacitor and directly under the TPS65261, TPS65261-1 device to provide a thermal path from the exposed thermal pad land to ground. The bottom layer acts as ground plane connecting analog ground and power ground.

For operation at full rated load, the top side ground area together with the bottom side ground plane must provide adequate heat dissipating area. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power

supplies performance. To help eliminate these problems, the PVIN pin must be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care must be taken to minimize the loop area formed by the bypass capacitor connections, the PVIN pins and the ground connections. The VIN pin must also be bypassed to ground using a low ESR ceramic capacitor with X5R or X7R dielectric.

Because the LX connection is the switching node, the output inductor must be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The output filter capacitor ground must use the same power ground trace as the PVIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width. The small signal components must be grounded to the analog ground path.

The FB and COMP pins are sensitive to noise so the resistors and capacitors must be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown.

### 8.4.2 Layout Example



**図 8-37. PCB Layout**

**図 8-37. PCB Layout**

Product Folder Links: *TPS65261 TPS65261-1*

English Data Sheet: SLVSCD3
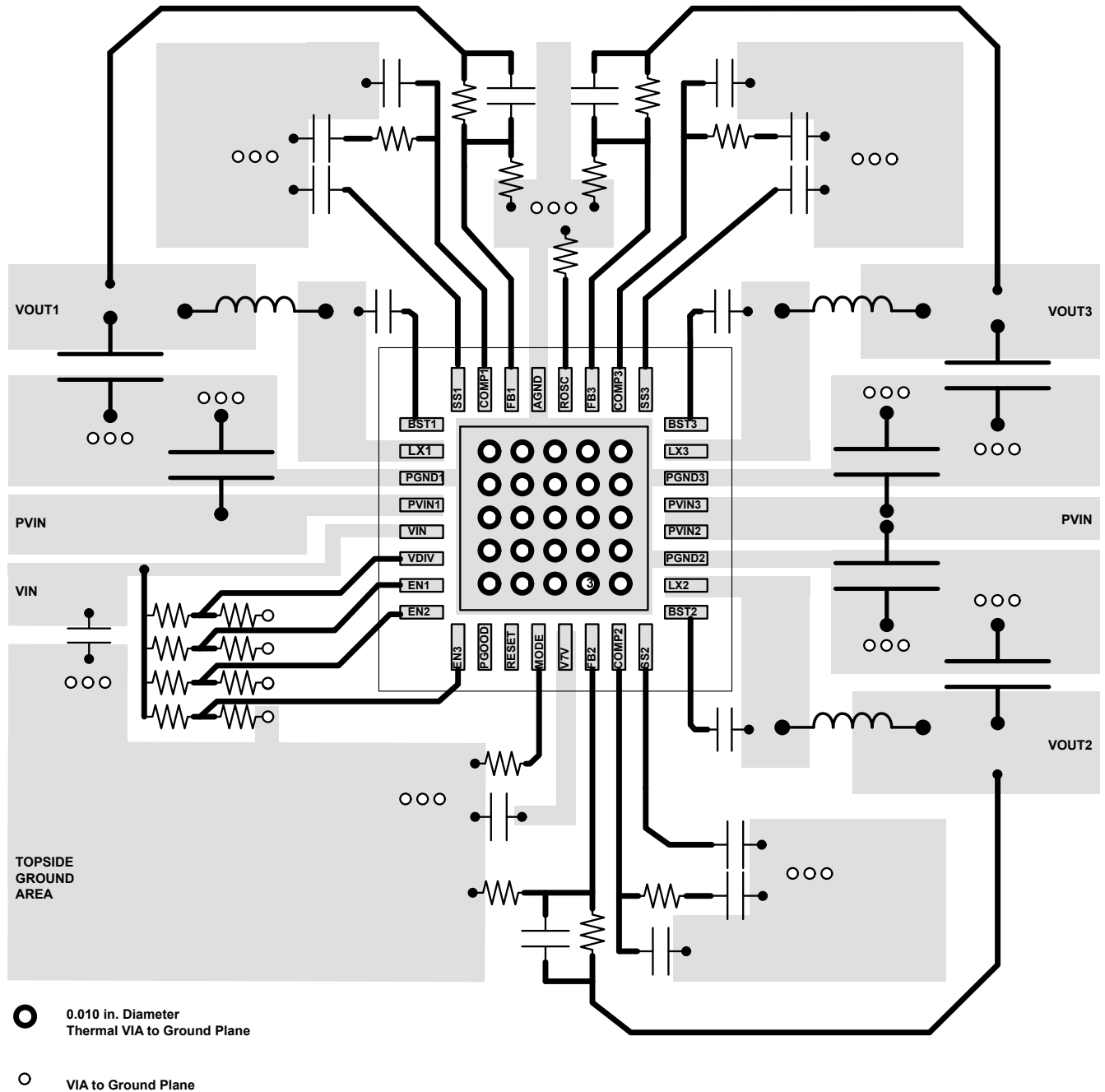
# 9 Device and Documentation Support

## 9.1 Documentation Support

### 9.1.1 Related Parts

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| TPS65262 | 4.5 V to 18 V, triple buck with dual adjustable LDOs | Triple buck 3-A/1-A/1-A output current, dual LDOs 100-mA/200-mA output current, automatic power sequencing |
| TPS65263 | 4.5 V to 18 V, triple buck with I2C interface | Triple buck 3-A/2-A/2-A output current, I2C controlled dynamic voltage scaling (DVS) |
| TPS65651-1/2/3 | 4.5 V to 18 V, triple buck with different PGOOD deglitch time | Triple buck 3-A/2-A/2-A output current, support 1s, 32-ms, 256-ms PGOOD deglitch time, adjustable current limit setting by external resistor |
| TPS65287 | 4.5 V to 18 V, triple buck with power switch and push button control | Triple buck 3-A/2-A/2-A output current, up to 2.1-A USB power with overcurrent setting by external resistor, push button control for intelligent system power-on/power-off operation |
| TPS65288 | 4.5 V to 18 V, triple buck with dual power switches | Triple buck 3-A/2-A/2-A output current, 2 USB power switches current limiting at typical 1.2 A (0.8/1.0/1.4/1.6/1.8/2.0/2.2A available with manufacture trim options) |

## 9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

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## 9.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

## 9.6 用語集

テキサス・インスツルメンツ用語集　　　この用語集には、用語や略語の一覧および定義が記載されています。

# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS65261-1RHBR | ACTIVE | VQFN | RHB | 32 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TPS 65261-1 | Samples |
| TPS65261-1RHBT | ACTIVE | VQFN | RHB | 32 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TPS 65261-1 | Samples |
| TPS65261RHBR | ACTIVE | VQFN | RHB | 32 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TPS 65261 | Samples |
| TPS65261RHBT | ACTIVE | VQFN | RHB | 32 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TPS 65261 | Samples |

**(1)** The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

Reel Diameter

Reel Width (W1)

**TAPE DIMENSIONS**

Cavity

| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

Sprocket Holes

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS65261-1RHBR | VQFN | RHB | 32 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS65261-1RHBT | VQFN | RHB | 32 | 250 | 180.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS65261RHBR | VQFN | RHB | 32 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS65261RHBT | VQFN | RHB | 32 | 250 | 180.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |

# PACKAGE MATERIALS INFORMATION

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS65261-1RHBR | VQFN | RHB | 32 | 3000 | 346.0 | 346.0 | 33.0 |
| TPS65261-1RHBT | VQFN | RHB | 32 | 250 | 210.0 | 185.0 | 35.0 |
| TPS65261RHBR | VQFN | RHB | 32 | 3000 | 346.0 | 346.0 | 33.0 |
| TPS65261RHBT | VQFN | RHB | 32 | 250 | 210.0 | 185.0 | 35.0 |

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224745/A

A ◄——————— 5.1 ———————► B
            4.9

PIN 1 INDEX AREA

5.1
4.9

(0.1)

SIDE WALL DETAIL
OPTIONAL METAL THICKNESS

1 MAX

0.05
0.00

C

SEATING PLANE

⌒ | 0.08 | C

2X | 3.5

□ 3.45 ± 0.1

9          16

28X | 0.5

8

(0.2) TYP

EXPOSED
THERMAL PAD

17

SEE SIDE WALL
DETAIL

2X
3.5

33          SYMM
            ₵

32X  0.3
     0.2

1

24

⊕ | 0.1Ⓜ | C | A | B
  | 0.05Ⓜ | C

32          25

PIN 1 ID
(OPTIONAL)

SYMM
₵

32X  0.5
     0.3

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

(□ 3.45)

SYMM ₵

32

25

32X (0.6)

1

32X (0.25)

28X (0.5)

24

(1.475)

33

SYMM ₵

(Ø 0.2) TYP
VIA

(4.8)

8

17

(R0.05)
TYP

9

16

(1.475)

(4.8)

### LAND PATTERN EXAMPLE
SCALE:18X

0.07 MAX
ALL AROUND

METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

SOLDER MASK
DEFINED

### SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature
    number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown
    on this view. It is recommended that vias under paste be filled, plugged or tented.
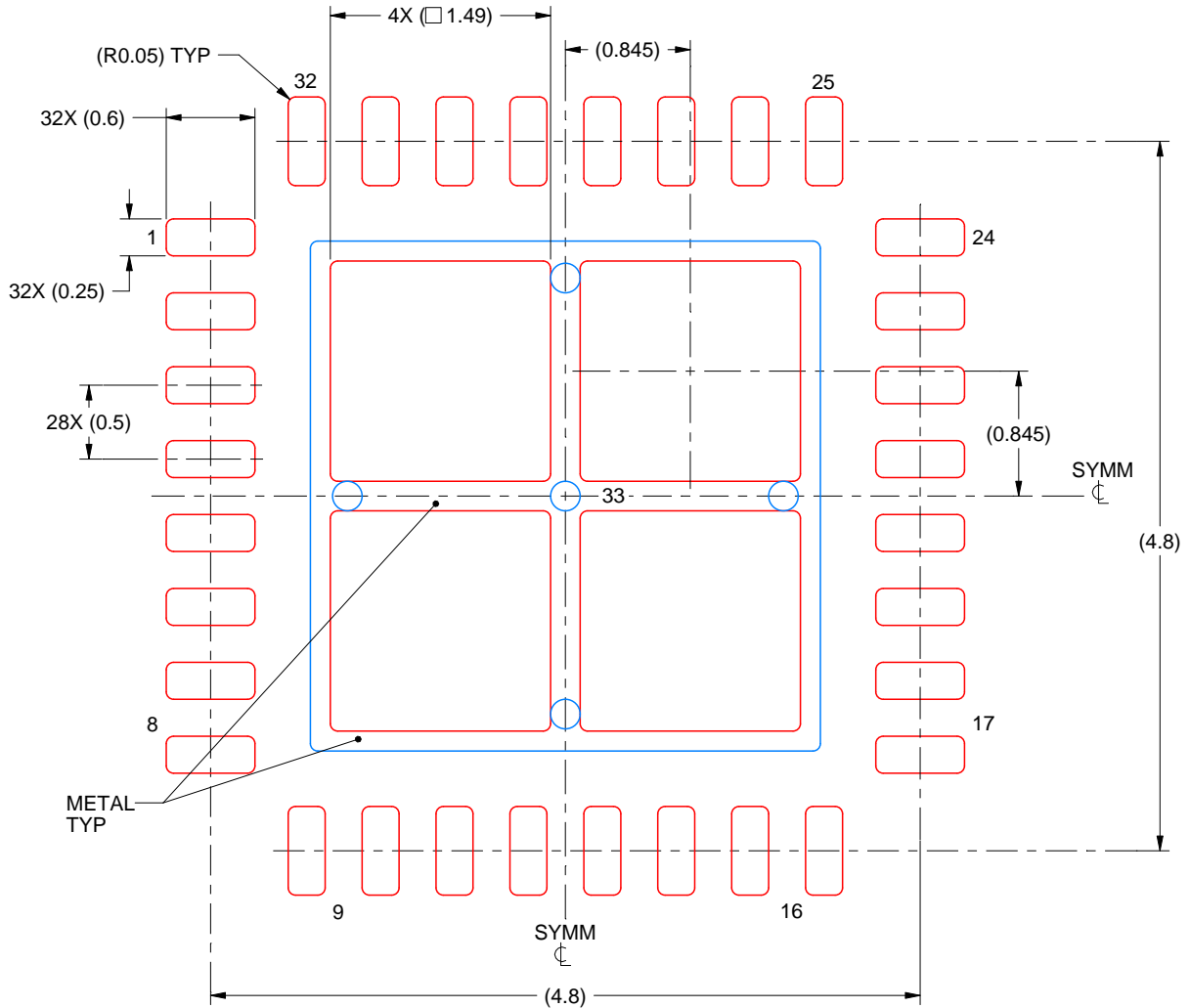
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.