

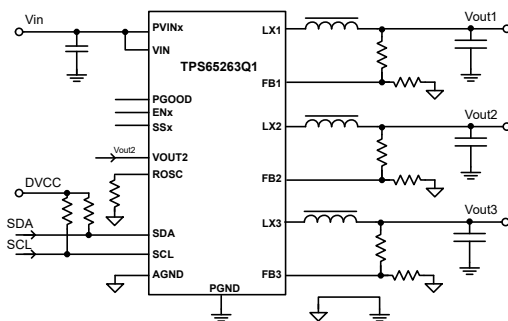
# TPS65263-Q1 入力電圧 4.0~18V、出力電流 3A/2A/2A の車載用トリプル同期整流降圧型コンバータ、I<sup>2</sup>C 制御の動的電圧スケーリング搭載

## 1 特長

- 車載アプリケーション認定済み
- 下記内容で AEC-Q100 認定済み:
  - デバイス温度グレード 1: 動作時の接合部温度範囲: -40°C~125°C
  - デバイス HBM ESD 分類レベル H2
  - デバイス CDM ESD 分類レベル C4B
- 動作入力電圧範囲 4.0~18V、最大連続出力電流 3A、2A、2A
- Buck2 の出力電圧は I<sup>2</sup>C 制御の 7 ビット VID により 0.68~1.95V の範囲で 10mV 刻みにプログラム可能
- Buck2 の VID 電圧遷移スルー・レートを I<sup>2</sup>C により制御
- I<sup>2</sup>C によりパワー・グッド・ステータス、過電流警告、ダイ温度警告を読み出し
- I<sup>2</sup>C 互換のインターフェイス、スタンダード・モード (100kHz) とファスト・モード (400kHz) に対応
- 帰還基準電圧: 0.6V±1%
- 可変クロック周波数: 200kHz~2.3MHz
- 外部クロック同期
- 各降圧コンバータに専用のイネーブル・ピンとソフト・スタート・ピン
- 出力電圧パワー・グッド・インジケータ
- 過熱保護

## 2 アプリケーション

- 車載用
- 車載用オーディオおよびビデオ
- ホーム・ゲートウェイおよびアクセス・ポイント・ネットワーク
- 監視機器



アプリケーション回路図

## 3 概要

TPS65263-Q1 には、トリプル同期整流降圧型コンバータが組み込まれており、4.0~18V の広い入力電圧範囲に対応します。コンバータは一定周波数のピーク電流モードで、アプリケーションを簡素化しながら、目的のアプリケーションに合わせてシステムを最適化するオプションを設計者が選択できるように設計されています。コンバータのスイッチング周波数は、外付け抵抗により 200kHz~2.3MHz の範囲で調整できます。buck1 と buck2、buck3 は位相差 180°で動作するため (buck2 と buck3 は同相動作)、入力フィルタの要件が最小化されます。

それぞれの buck の初期スタートアップ電圧は、外付けのフィードバック抵抗で設定できます。buck2 の出力電圧は、0.68~1.95V の範囲で、I<sup>2</sup>C 制御の 7 ビット VID を使用して 10mV 刻みで動的に設定可能です。VID 電圧の遷移スルー・レートは、I<sup>2</sup>C バスによる 3 ビットの制御によりプログラム可能なため、VID 電圧遷移時のオーバーシュートやアンダーシュートを最適化できます。

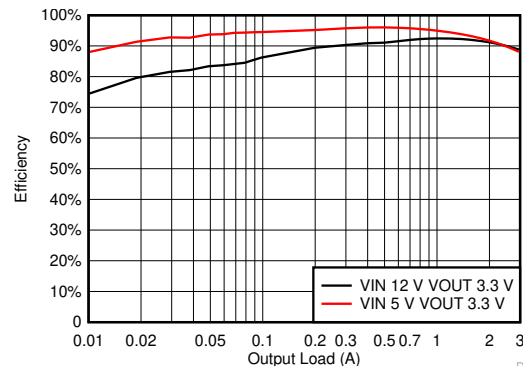
TPS65263-Q1 の各バックについて、出力電圧のイネーブルとディセーブル、軽負荷時のパルス・スキップ・モード (PSM) または強制連続電流 (FCC) モードの設定、パワー・グッド・ステータス、過電流警告、ダイ温度警告の読み出しを、I<sup>2</sup>C で制御できます。

TPS65263-Q1 には過電圧、過電流、短絡、過熱保護が搭載されています。

### パッケージ情報 (1)

部品番号	パッケージ	本体サイズ (公称)
TPS65263-Q1	RHB (VQFN, 32)	5.00mm × 5.00mm

- (1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



効率と出力負荷との関係



## Table of Contents

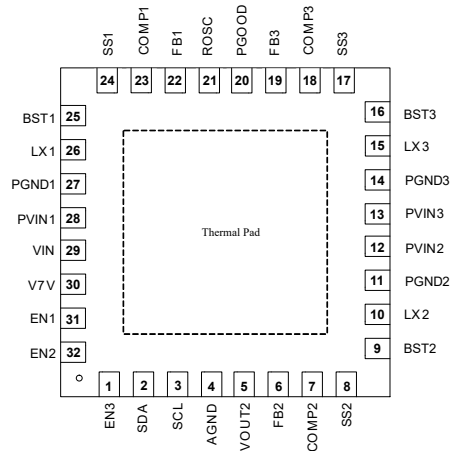
1 特長.....	1	7.4 Device Functional Modes.....	23
2 アプリケーション.....	1	7.5 Register Maps.....	25
3 概要.....	1	<b>8 Application and Implementation.....</b>	<b>28</b>
4 Revision History.....	2	8.1 Application Information.....	28
5 Pin Configuration and Functions.....	3	8.2 Typical Application.....	28
6 Specifications.....	5	8.3 Power Supply Recommendations.....	36
6.1 Absolute Maximum Ratings.....	5	8.4 Layout.....	36
6.2 ESD Ratings.....	5	<b>9 Device and Documentation Support.....</b>	<b>39</b>
6.3 Recommended Operating Conditions.....	5	9.1 ドキュメントの更新通知を受け取る方法.....	39
6.4 Thermal Information.....	5	9.2 サポート・リソース.....	39
6.5 Electrical Characteristics.....	6	9.3 Trademarks.....	39
6.6 Typical Characteristics.....	8	9.4 静電気放電に関する注意事項.....	39
7 Detailed Description.....	12	9.5 用語集.....	39
7.1 Overview.....	12	<b>10 Mechanical, Packaging, and Orderable</b>	
7.2 Functional Block Diagram.....	13	<b>Information.....</b>	<b>39</b>
7.3 Feature Description.....	13		

## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (November 2015) to Revision D (May 2023)	Page
• データシートのタイトルに「車載用」という言葉を追加.....	1
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....	1
• ドキュメント全体にわたって画像の色を除去.....	1
• Change description of V7V pin in 表 5-1 .....	3
• Update the ESD table to be in accordance with automotive specification.....	5
• Changed the recommended value of capacitor from V7V pin to power ground in <i>V7V Low-Dropout Regulator and Bootstrap</i> .....	19
• Changed all instances of legacy terminology to controller and target where I <sup>2</sup> C is mentioned.....	23
• Changed recommended value of C9 in 図 8-1.....	28
Changes from Revision B (January 2015) to Revision C (November 2015)	Page
• Added more pin information for SDA and SCL .....	3
• Added more information about SDA and SCL pins .....	12
• Added <i>Community Resources</i> .....	39
Changes from Revision A (January 2015) to Revision B (January 2015)	Page
• デバイスのステータスを「量産データ」に更新.....	1
Changes from Revision * (December 2014) to Revision A (January 2015)	Page
• 「特長」のフィードバック基準電圧を 0.6V±2% から 0.6V±1% に変更 .....	1
• Updated values for feedback voltage, PGOOD pin leakage, V7V LDO output voltage, buck1 low-side sink current limit, and buck2/buck3 low-side sink current limit in <i>Electrical Characteristics</i> .....	6
• Updated current value in セクション 7.3.8, 式 6, and 図 7-10 .....	20

## 5 Pin Configuration and Functions



There is no electric signal down bonded to thermal pad inside IC. Exposed thermal pad must be soldered to PCB for optimal thermal performance.

**图 5-1. RHB Package 32-Pin VQFN Top View**

**表 5-1. Pin Functions**

PIN		DESCRIPTION
NAME	NO.	
EN3	1	Enable for buck3. Float to enable. Can use this pin to adjust the input UVLO of buck3 with a resistor divider.
SDA	2	I <sup>2</sup> C interface data pin; float or connect to GND to disable I <sup>2</sup> C communication
SCL	3	I <sup>2</sup> C interface clock pin; float or connect to GND to disable I <sup>2</sup> C communication
AGND	4	Analog ground common to buck controllers and other analog circuits. It must be routed separately from high-current power grounds to the (–) terminal of bypass capacitor of input voltage VIN.
VOUT2	5	Buck2 output voltage sense pin
FB2	6	Feedback Kelvin sensing pin for buck2 output voltage. Connect this pin to buck2 resistor divider.
COMP2	7	Error amplifier output and loop compensation pin for buck2. Connect a series resistor and capacitor to compensate the control loop of buck2 with peak current PWM mode.
SS2	8	Soft-start and tracking input for buck2. An internal 5.2- $\mu$ A pullup current source is connected to this pin. The soft-start time can be programmed by connecting a capacitor between this pin and ground.
BST2	9	Boot-strapped supply to the high-side floating gate driver in buck2. Connect a capacitor (recommend 47 nF) from BST2 pin to LX2 pin.
LX2	10	Switching node connection to the inductor and bootstrap capacitor for buck2. The voltage swing at this pin is from a diode voltage below the ground up to PVIN2 voltage.
PGND2	11	Power ground connection of buck2. Connect PGND2 pin as close as practical to the (–) terminal of VIN2 input ceramic capacitor.
PVIN2	12	Input power supply for buck2. Connect PVIN2 pin as close as practical to the (+) terminal of an input ceramic capacitor (suggest 10 $\mu$ F).
PVIN3	13	Input power supply for buck3. Connect PVIN3 pin as close as practical to the (+) terminal of an input ceramic capacitor (suggest 10 $\mu$ F).
PGND3	14	Power ground connection of buck3. Connect PGND3 pin as close as practical to the (–) terminal of VIN3 input ceramic capacitor.
LX3	15	Switching node connection to the inductor and bootstrap capacitor for buck3. The voltage swing at this pin is from a diode voltage below the ground up to PVIN3 voltage.
BST3	16	Boot-strapped supply to the high-side floating gate driver in buck3. Connect a capacitor (recommend 47 nF) from BST3 pin to LX3 pin.
SS3	17	Soft-start and tracking input for buck3. An internal 5.2- $\mu$ A pullup current source is connected to this pin. The soft-start time can be programmed by connecting a capacitor between this pin and ground.

表 5-1. Pin Functions (continued)

PIN		DESCRIPTION
NAME	NO.	
COMP3	18	Error amplifier output and loop compensation pin for buck3. Connect a series resistor and capacitor to compensate the control loop of buck3 with peak current PWM mode.
FB3	19	Feedback Kelvin sensing pin for buck3 output voltage. Connect this pin to buck3 resistor divider.
PGOOD	20	Output voltage supervision pin. When all bucks are in PGOOD monitor's regulation range, PGOOD is asserted high.
ROSC	21	Clock frequency adjustment pin. Connect a resistor from this pin to ground to adjust the clock frequency. When connected to an external clock, the internal oscillator synchronizes to the external clock.
FB1	22	Feedback Kelvin sensing pin for buck1 output voltage. Connect this pin to buck1 resistor divider.
COMP1	23	Error amplifier output and loop compensation pin for buck1. Connect a series resistor and capacitor to compensate the control loop of buck1 with peak current PWM mode.
SS1	24	Soft-start and tracking input for buck1. An internal 5.2- $\mu$ A pullup current source is connected to this pin. The soft-start time can be programmed by connecting a capacitor between this pin and ground.
BST1	25	Boot-strapped supply to the high-side floating gate driver in buck1. Connect a capacitor (recommend 47 nF) from BST1 pin to LX1 pin.
LX1	26	Switching node connection to the inductor and bootstrap capacitor for buck1. The voltage swing at this pin is from a diode voltage below the ground up to PVIN1 voltage.
PGND1	27	Power ground connection of buck1. Connect PGND1 pin as close as practical to the (–) terminal of VIN1 input ceramic capacitor.
PVIN1	28	Input power supply for buck1. Connect PVIN1 pin as close as practical to the (+) terminal of an input ceramic capacitor (suggest 10 $\mu$ F).
VIN	29	Buck controller power supply
V7V	30	Internal LDO for gate driver and internal controller. Connect a 10- $\mu$ F ceramic capacitor from the pin to power ground.
EN1	31	Enable for buck1. Float to enable. Can use this pin to adjust the input UVLO of buck1 with a resistor divider.
EN2	32	Enable for buck2. Float to enable. Can use this pin to adjust the input UVLO of buck2 with a resistor divider.
PAD	—	There is no electric signal down bonded to thermal pad inside IC. Exposed thermal pad must be soldered to PCB for optimal thermal performance.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) <sup>(1)</sup>

	MIN	MAX	UNIT
PVIN1, PVIN2, PVIN3, VIN	-0.3	20	V
LX1, LX2, LX3 (Maximum withstand voltage transient < 20 ns)	-1.0	20	V
BST1, BST2, BST3 referenced to LX1, LX2, LX3 pins respectively	-0.3	7	V
EN1, EN2, EN3, V7V, VOUT2, SCL, SDA, PGOOD	-0.3	7	V
FB1, FB2, FB3, COMP1, COMP2, COMP3, ROSC, SS1, SS2, SS3	-0.3	3.6	V
AGND, PGND1, PGND2, PGND3	-0.3	0.3	V
T <sub>J</sub> Operating junction temperature	-40	150	°C
T <sub>stg</sub> Storage temperature	-55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2, all pins <sup>(1)</sup>		±2000	V
	Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C4B		±500	

- (1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
PVIN1, PVIN2, PVIN3, VIN	4	18	V
LX1, LX2, LX3 (Maximum withstand voltage transient <20 ns)	-0.8	18	V
BST1, BST2, BST3 referenced to LX1, LX2, LX3 pins respectively	-0.1	6.8	V
EN1, EN2, EN3, V7V, VOUT1, VOUT2, VOUT3, SCL, SDA	-0.1	6.3	V
FB1, FB2, FB3, COMP1, COMP2, COMP3, SS1, SS2, SS3	-0.1	3	V
T <sub>J</sub> Operating junction temperature	-40	125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS65263-Q1	UNIT
		RHB (VQFN)	
		32 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	33.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	25.7	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	7.4	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.3	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	7.3	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	2.1	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

$V_{IN} = 12\text{ V}$ ,  $F_{SW} = 500\text{ kHz}$ ,  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ , typical values are at  $T_J = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT SUPPLY VOLTAGE</b>						
$V_{IN}$	Input voltage range		4		18	V
$UVLO$	VIN UVLO	VIN rising	3.5	3.8	4	V
		VIN falling	3.1	3.3	3.5	V
		Hysteresis		500		mV
$I_{DDSDN}$	Shutdown supply current	EN1 = EN2 = EN3 = 0 V	4	9.5	18	$\mu\text{A}$
$I_{DDQNSW}$	Input quiescent current without buck1/2/3 switching	EN1 = EN2 = EN3 = 5 V, FB1 = FB2 = FB3 = 0.8 V	550	780	1150	$\mu\text{A}$
$I_{DDQNSW1}$		EN1 = 5 V, EN2 = EN3 = 0 V, FB1 = 0.8 V	180	370	590	$\mu\text{A}$
$I_{DDQNSW2}$		EN2 = 5 V, EN1 = EN3 = 0 V, FB2 = 0.8 V	180	370	590	$\mu\text{A}$
$I_{DDQNSW3}$		EN3 = 5 V, EN1 = EN2 = 0 V, FB3 = 0.8 V	180	370	590	$\mu\text{A}$
$V_{7V}$	V7V LDO output voltage	$V_{7V}$ load current = 0 A		6.3		V
$I_{OCP\_V7V}$	V7V LDO current limit		78	185	260	mA
<b>FEEDBACK VOLTAGE REFERENCE</b>						
$V_{FB}$	Feedback voltage	$V_{COMP} = 1.2\text{ V}$	0.594	0.6	0.606	V
<b>BUCK1, BUCK2, BUCK3</b>						
$V_{ENXH}$	EN1/2/3 high-level input voltage		1.12	1.2	1.26	V
$V_{ENXL}$	EN1/2/3 low-level input voltage		1.05	1.15	1.21	V
$I_{ENX1}$	EN1/2/3 pullup current	ENx = 1 V	2.5	3.9	5.9	$\mu\text{A}$
$I_{ENX2}$	EN1/2/3 pullup current	ENx = 1.5 V	5.1	6.9	9.2	$\mu\text{A}$
$I_{ENhys}$	Hysteresis current		2.6	3	3.3	$\mu\text{A}$
$I_{SSX}$	Soft-start charging current		3.9	5.2	6.5	$\mu\text{A}$
$t_{ON\_MIN}$	Minimum on-time		50	75	110	ns
$G_{m\_EA}$	Error amplifier transconductance	$-2\ \mu\text{A} < I_{COMPX} < 2\ \mu\text{A}$	140	300	450	$\mu\text{s}$
$G_{m\_PS1/2/3}$	COMP1/2/3 voltage to inductor current $G_m$ <sup>(1)</sup>	$I_{LX} = 0.5\text{ A}$		7.4		A/V
$I_{LIMIT1}$	Buck1 peak inductor current limit		4.3	5.4	6.5	A
$I_{LIMITSINK1}$	Buck1 low-side sink current limit		0.7	1.3	1.8	A
$I_{LIMIT2/3}$	Buck2/buck3 peak inductor current limit		2.55	3.3	3.9	A
$I_{LIMITSINK2/3}$	Buck2/buck3 low-side sink current limit		0.5	1	1.4	A
$R_{dson\_HS1}$	Buck1 high-side switch resistance	$V_{IN} = 12\text{ V}$		105		m $\Omega$
$R_{dson\_LS1}$	Buck1 low-side switch resistance	$V_{IN} = 12\text{ V}$		65		m $\Omega$
$R_{dson\_HS2}$	Buck2 high-side switch resistance	$V_{IN} = 12\text{ V}$		140		m $\Omega$
$R_{dson\_LS2}$	Buck2 low-side switch resistance	$V_{IN} = 12\text{ V}$		90		m $\Omega$
$R_{dson\_HS3}$	Buck3 high-side switch resistance	$V_{IN} = 12\text{ V}$		140		m $\Omega$
$R_{dson\_LS3}$	Buck3 low-side switch resistance	$V_{IN} = 12\text{ V}$		90		m $\Omega$
<b>HICCUP TIMING</b>						
$t_{Hiccup\_wait}$	Overcurrent wait time <sup>(1)</sup>			256		cycles
$t_{Hiccup\_re}$	Hiccup time before restart <sup>(1)</sup>			8192		cycles
<b>POWER GOOD</b>						
$V_{th\_PG}$	Feedback voltage threshold	FBx undervoltage falling		92.5		% $V_{REF}$
		FBx undervoltage rising		95		
		FBx overvoltage rising		107.5		
		FBx overvoltage falling		105		
$t_{DEGLITCH(PG)_F}$	PGOOD falling edge deglitch time			112		cycles
$t_{RDEGLITCH(PG)_R}$	PGOOD rising edge deglitch time			616		cycles
$I_{PG}$	PGOOD pin leakage				0.1	$\mu\text{A}$

## 6.5 Electrical Characteristics (continued)

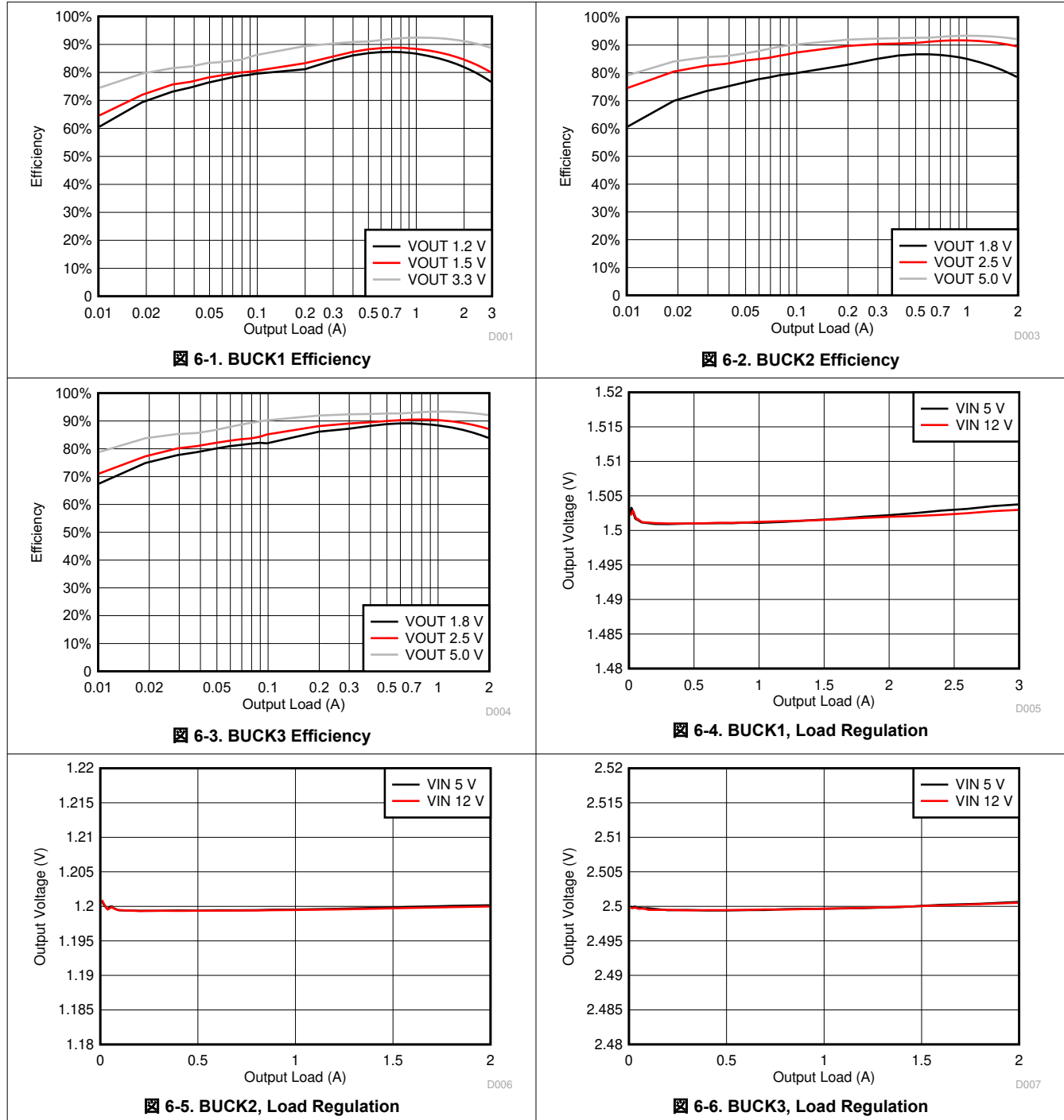
$V_{IN} = 12\text{ V}$ ,  $F_{SW} = 500\text{ kHz}$ ,  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ , typical values are at  $T_J = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{LOW\_PG}$	PGOOD pin low voltage	$I_{SINK} = 1\text{ mA}$			0.4	V
<b>OSCILLATOR</b>						
$F_{SW}$	Switching frequency	$R_{OSC} = 88.7\text{ k}\Omega$	430	500	560	kHz
$F_{SW\_range}$	Switching frequency		200		2300	kHz
$T_{SYNC\_w}$	Clock sync minimum pulse width		80			ns
$F_{SYNC\_HI}$	Clock sync high threshold				2	V
$V_{SYNC\_LO}$	Clock sync low threshold		0.4			V
$F_{SYNC}$	Clock sync frequency range		200		2300	kHz
<b>THERMAL PROTECTION</b>						
$T_{TRIP\_OTP}$	Thermal protection trip point <sup>(1)</sup>	Temperature rising		160		$^\circ\text{C}$
$T_{HYST\_OTP}$		Hysteresis		20		$^\circ\text{C}$
<b>I<sup>2</sup>C INTERFACE</b>						
Addr	Address <sup>(2)</sup>	0x60H				
$V_{IH\ SDA,SCL}$	Input high voltage				2	V
$V_{IL\ SDA,SCL}$	Input low voltage		0.4			V
$I_I$	Input current	SDA, SCL, $V_I = 0.4$ to $4.5\text{ V}$	-10		10	$\mu\text{A}$
$V_{OL\ SDA}$	SDA output low voltage	SDA open drain, $I_{OL} = 4\text{ mA}$			0.4	V
$f_{(SCL)}$	Maximum SCL clock frequency <sup>(2)</sup>		400			kHz
$t_{BUF}$	Bus free time between a STOP and START condition <sup>(2)</sup>		1.3			$\mu\text{s}$
$t_{HD\_STA}$	Hold time (repeated) START condition <sup>(2)</sup>		0.6			$\mu\text{s}$
$t_{SU\_STO}$	Setup time for STOP condition <sup>(2)</sup>		0.6			$\mu\text{s}$
$t_{LOW}$	Low period of the SCL clock <sup>(2)</sup>		1.3			$\mu\text{s}$
$t_{HIGH}$	High period of the SCL clock <sup>(2)</sup>		0.6			$\mu\text{s}$
$t_{SU\_STA}$	Setup time for a repeated START condition <sup>(2)</sup>		0.6			$\mu\text{s}$
$t_{SU\_DAT}$	Data setup time <sup>(2)</sup>		0.1			$\mu\text{s}$
$t_{HD\_DAT}$	Data hold time <sup>(2)</sup>		0		0.9	$\mu\text{s}$
$t_{RCL}$	Rise time of SCL signal <sup>(2)</sup>	Capacitance of one bus line (pF)	$20 + 0.1CB$		300	ns
$t_{RCL1}$	Rise time of SCL signal after a repeated START condition and after an acknowledge bit <sup>(2)</sup>	Capacitance of one bus line (pF)	$20 + 0.1CB$		300	ns
$t_{FCL}$	Fall time of SCL signal <sup>(2)</sup>	Capacitance of one bus line (pF)	$20 + 0.1CB$		300	ns
$t_{RDA}$	Rise time of SDA signal <sup>(2)</sup>	Capacitance of one bus line (pF)	$20 + 0.1CB$		300	ns
$t_{FDA}$	Fall time of SDA signal <sup>(2)</sup>	Capacitance of one bus line (pF)	$20 + 0.1CB$		300	ns
$C_B$	Capacitance of bus line(SCL and SDA) <sup>(2)</sup>				400	pF

- (1) Lab validation result  
 (2) Not production tested

## 6.6 Typical Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_{IN} = 12\text{ V}$ ,  $V_{OUT1} = 1.5\text{ V}$ ,  $V_{OUT2} = 1.2\text{ V}$ ,  $V_{OUT3} = 2.5\text{ V}$ ,  $F_{SW} = 500\text{ kHz}$  (unless otherwise noted)





## 6.6 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ ,  $V_{IN} = 12\text{ V}$ ,  $V_{OUT1} = 1.5\text{ V}$ ,  $V_{OUT2} = 1.2\text{ V}$ ,  $V_{OUT3} = 2.5\text{ V}$ ,  $F_{SW} = 500\text{ kHz}$  (unless otherwise noted)

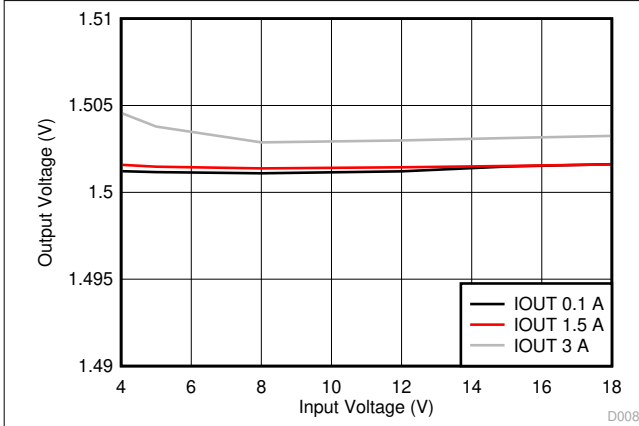


FIG 6-7. BUCK1, Line Regulation

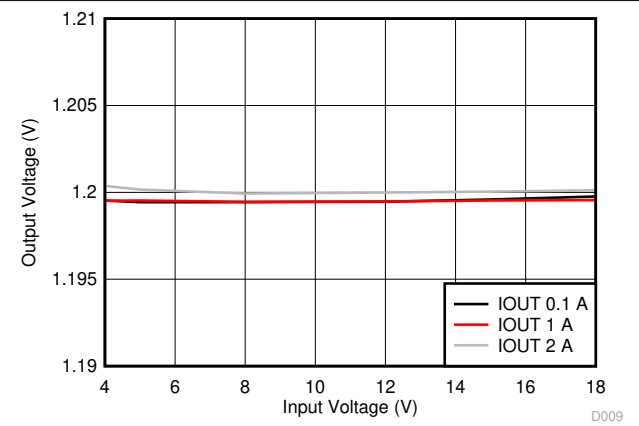


FIG 6-8. BUCK2, Line Regulation

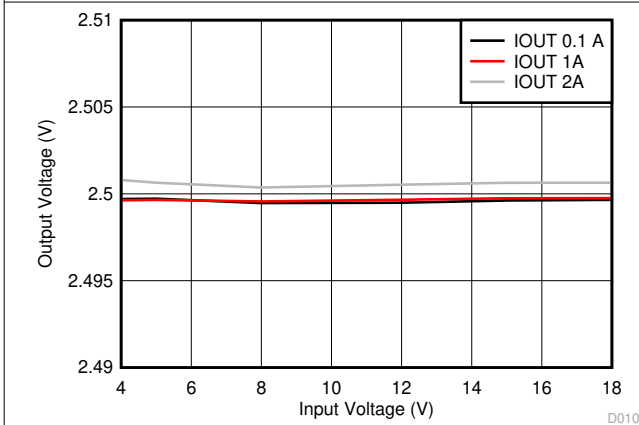


FIG 6-9. BUCK3, Line Regulation

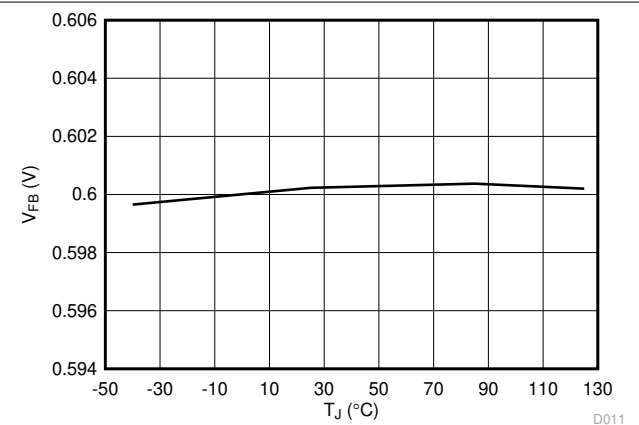


FIG 6-10. Voltage Reference vs Temperature

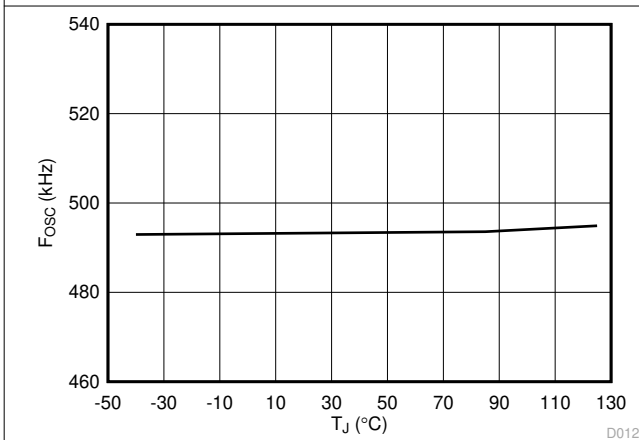


FIG 6-11. Oscillator Frequency vs Temperature

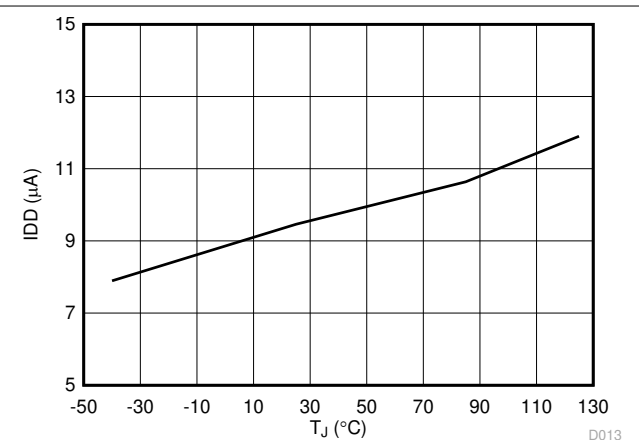
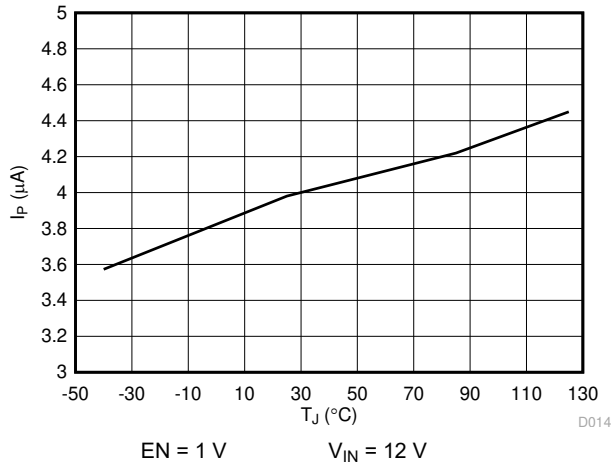


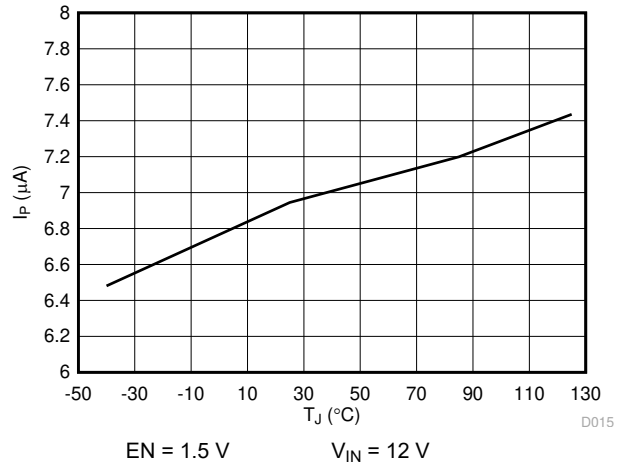
FIG 6-12. Shutdown Quiescent Current vs Temperature

## 6.6 Typical Characteristics (continued)

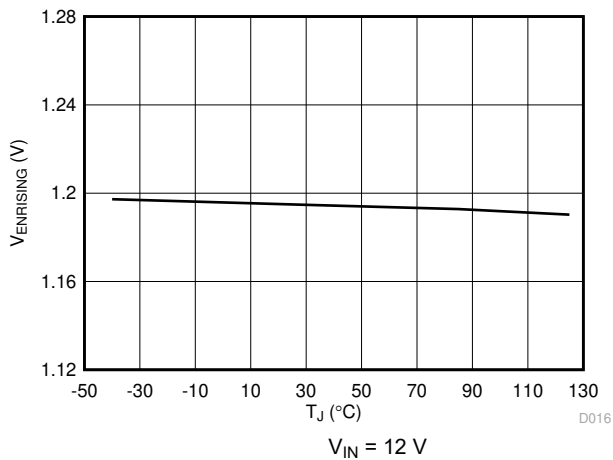
$T_A = 25^\circ\text{C}$ ,  $V_{IN} = 12\text{ V}$ ,  $V_{OUT1} = 1.5\text{ V}$ ,  $V_{OUT2} = 1.2\text{ V}$ ,  $V_{OUT3} = 2.5\text{ V}$ ,  $F_{SW} = 500\text{ kHz}$  (unless otherwise noted)



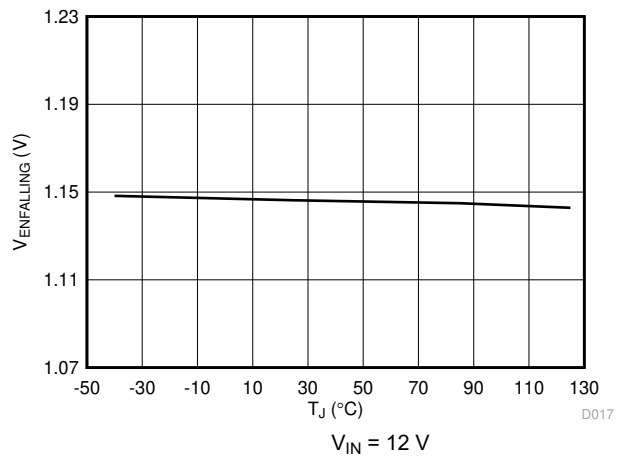
6-13. EN Pin Pullup Current vs Temperature, EN = 1.0 V



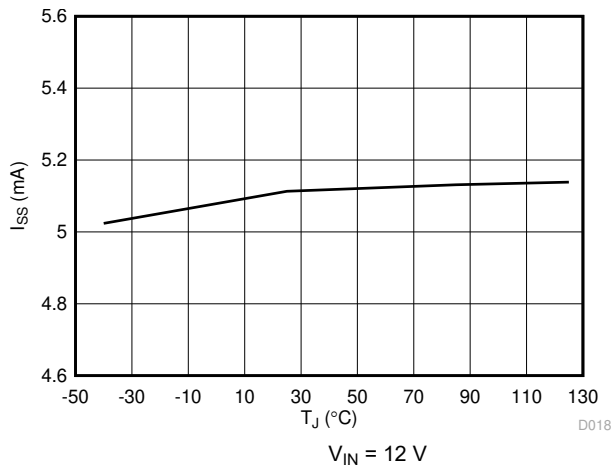
6-14. EN Pin Pullup Current vs Temperature, EN = 1.5 V



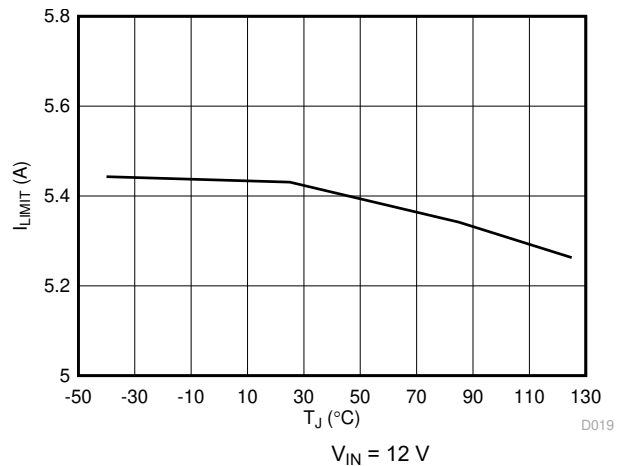
6-15. EN Pin Threshold Rising vs Temperature



6-16. EN Pin Threshold Falling vs Temperature



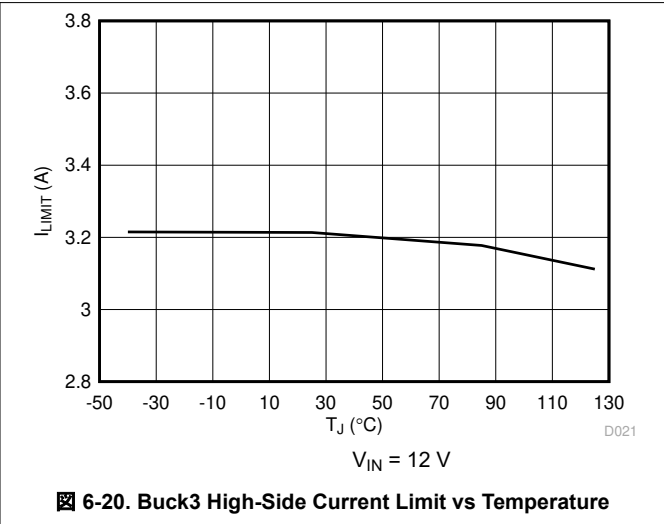
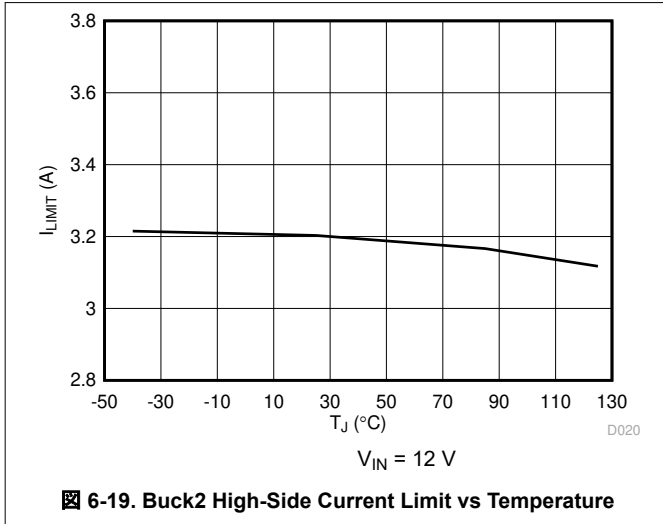
6-17. SS Pin Charge Current vs Temperature



6-18. Buck1 High-Side Current Limit vs Temperature

## 6.6 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ ,  $V_{IN} = 12\text{ V}$ ,  $V_{OUT1} = 1.5\text{ V}$ ,  $V_{OUT2} = 1.2\text{ V}$ ,  $V_{OUT3} = 2.5\text{ V}$ ,  $F_{SW} = 500\text{ kHz}$  (unless otherwise noted)



## 7 Detailed Description

### 7.1 Overview

The TPS65263-Q1 is a monolithic, triple-synchronous step-down (buck) converter with 3-A/2-A/2-A output currents. A wide 4- to 18-V input supply voltage range encompasses most intermediate bus voltages operating off 5-, 9-, 12-, or 15-V power bus. The feedback voltage reference for each buck is 0.6 V. Each buck is independent with dedicated enable, soft-start, and loop compensation pins.

The TPS65263-Q1 is equipped with an I<sup>2</sup>C compatible bus for communication with SoC to control buck converters. Through the I<sup>2</sup>C interface, SoC can enable or disable the buck converters, set output voltage (BUCK2 only), and read status registers. External feedback divider resistors can set the initial start-up voltage of the buck2. After the voltage identification VID DAC is updated via the I<sup>2</sup>C, output voltage of the buck2 can be independently programmed with 7 bits VID from 0.68 to 1.95 V in 10-mV voltage step resolution. Output voltage of the buck2 transition begins after the I<sup>2</sup>C interface receives the command for the GO bit in the command register.

If SDA and SCL pins are floated or are connected to GND, the I<sup>2</sup>C communication is rejected and the TPS65263-Q1 operates as a traditional triple buck. Each buck on or off is separately controlled by the relevant enable pin. Buck2's output voltage is set with the external feedback divider resistors.

In the light load condition, the converter automatically operates in pulse skipping mode (PSM) to save power. PSM can be disabled through I<sup>2</sup>C so that the converter operates at continuous current mode (CCM) at light load with a fixed frequency for optimized output ripple.

The TPS65263-Q1 implements a constant frequency, peak current mode control that simplifies external loop compensation. The wide switching frequency of 200 kHz to 2.3 MHz allows for optimizing system efficiency, filtering size, and bandwidth. The switching frequency can be adjusted with an external resistor connecting between the ROOSC pin and ground. The TPS65263-Q1 also has an internal phase locked loop (PLL) controlled by the ROOSC pin that can be used to synchronize the switching cycle to the falling edge of an external system clock. The switching clock of buck1 is 180° out-of-phase operation from the clocks of buck2 and buck3 channels to reduce input current ripple, input capacitor size, and power-supply-induced noise.

The TPS65263-Q1 is designed for safe monotonic start-up into prebiased loads. The default start-up is when VIN is typically 3.8 V. The ENx pin can also be used to adjust the input voltage undervoltage lockout (UVLO) with an external resistor divider. In addition, the ENx pin has an internal 3.9-μA current source, so the EN pin can be floating for automatically powering up the converters.

The TPS65263-Q1 reduces the external component count by integrating the bootstrap circuit. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BST and LX pins. A UVLO circuit monitors the bootstrap capacitor voltage  $V_{BST}-V_{LX}$  in each buck. When  $V_{BST}-V_{LX}$  voltage drops to the threshold, LX pin is pulled low to recharge the bootstrap capacitor. The TPS65263-Q1 can operate at 100% duty cycle as long as the bootstrap capacitor voltage is higher than the BOOT-LX UVLO threshold, which is typically 2.1 V.

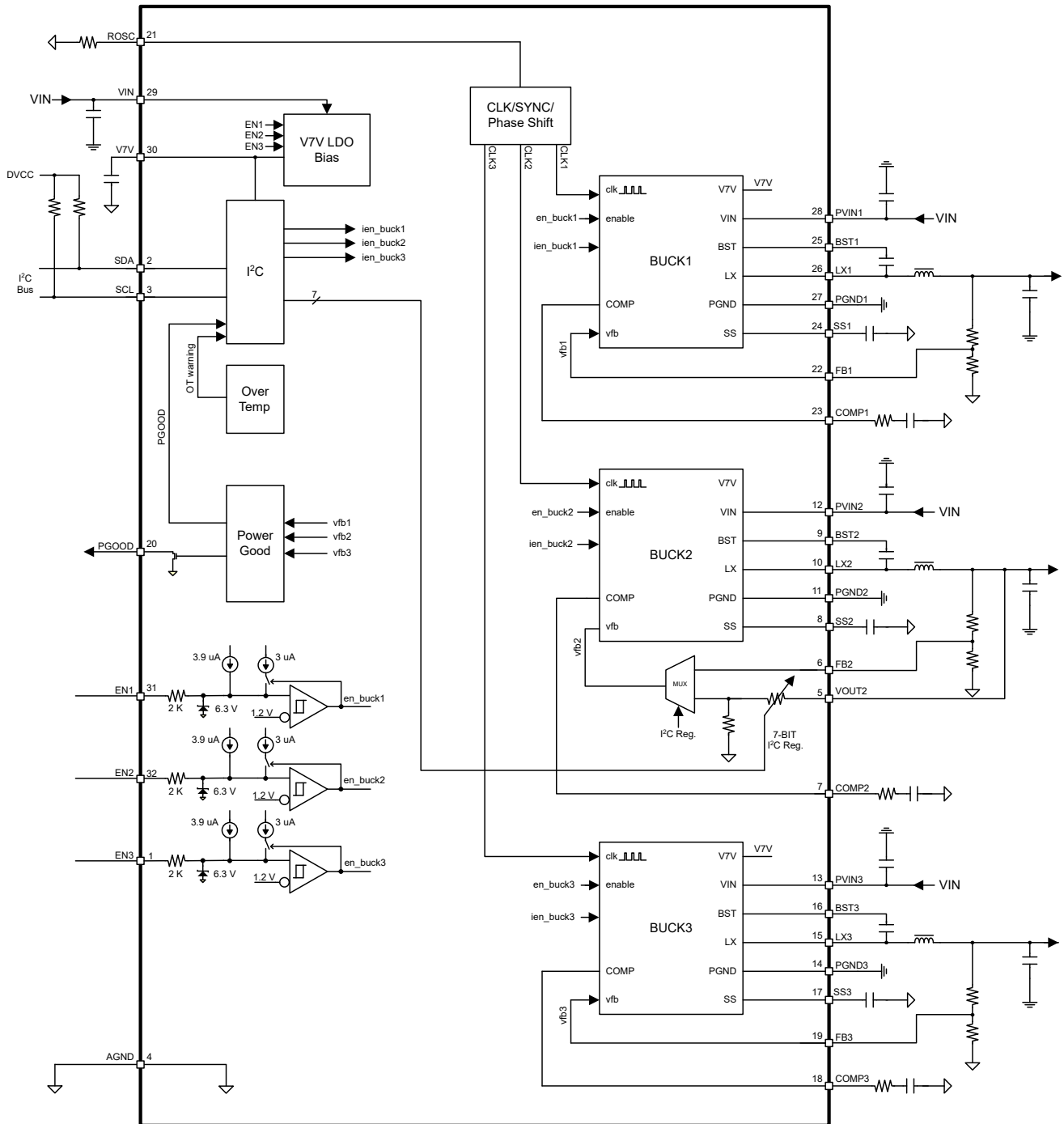
The TPS65263-Q1 has power-good comparators with hysteresis, which monitor the output voltages through internal feedback voltages. I<sup>2</sup>C can read the power-good status with the command register. The device also features the PGOOD pin to supervise output voltages of the buck converter. When all bucks are in regulation range and power sequence is done, PGOOD is asserted high.

The SS (soft-start/tracking) pin is used to minimize inrush currents or provide power-supply sequencing during power up. A small value capacitor or resistor divider is connected to the pin for soft start or voltage tracking.

The TPS65263-Q1 is protected from overload and overtemperature fault conditions. The converter minimizes excessive output overvoltage transients by taking advantage of the power-good comparator. When the output is over, the high-side MOSFET is turned off until the internal feedback voltage is lower than 105% of the 0.6-V reference voltage. The TPS65263-Q1 implements both high-side MOSFET overload protection and bidirectional low-side MOSFET overload protections to avoid inductor current runaway. If the overcurrent condition has lasted for more than the OC wait time (256 clock cycle), the converter shuts down and restarts after the hiccup time (8192 clock cycles). The TPS65263-Q1 shuts down if the junction temperature is higher than thermal shutdown

trip point. When the junction temperature drops 20°C typically below the thermal shutdown trip point, the TPS65263-Q1 is restarted under control of the soft-start circuit automatically.

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Adjusting the Output Voltage

The output voltage of each buck is set with a resistor divider from the output of buck to the FB pin. TI recommends to use 1% tolerance or better resistors.

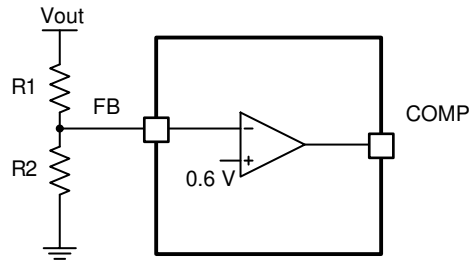


图 7-1. Voltage Divider Circuit

$$R_2 = R_1 \times \frac{0.6}{V_{out} - 0.6} \tag{1}$$

To improve efficiency at light loads consider using larger value resistors. If the values are too high, the regulator is more sensitive to noise. 表 7-1 shows the recommended resistor values.

表 7-1. Output Resistor Divider Selection

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)
1	10	15
1.2	10	10
1.5	15	10
1.8	20	10
2.5	31.6	10
3.3	45.3	10
3.3	22.6	4.99
5	73.2	10
5	36.5	4.99

The output voltage of the buck converter can be dynamically scaled by I<sup>2</sup>C-controlled 7-bit register, VOUTx\_SEL. Before I<sup>2</sup>C communication, the output voltage is set with the resistor divider from the output of buck to the FB pin. When the GO bit is set to 1 through the I<sup>2</sup>C interface, the buck converter switches the external resistor divider to the internal resistor divider as shown in 图 7-2. The output voltage can be selected among 128 voltages with voltage identifications (VID) shown in 表 7-2. The output voltage range of dynamic voltage scaling is 0.68 to 1.95 V with 10-mV resolution of each voltage step.

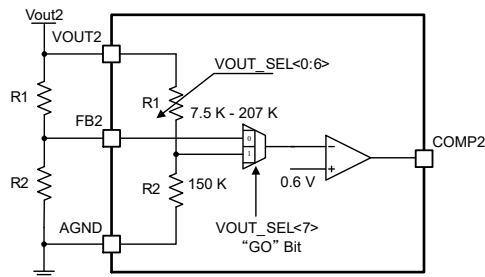


图 7-2. Voltage Divider Circuit

表 7-2. V<sub>OUT</sub> Output Voltage Setting

OUT_SEL <7:0>	V <sub>OUT</sub> (V)	VOUT_SEL <7:0>	V <sub>OUT</sub> (V)	VOUT_SEL <7:0>	V <sub>OUT</sub> (V)	VOUT_SEL <7:0>	V <sub>OUT</sub> (V)
0	0.68	20	1	40	1.32	60	1.64

**表 7-2. V<sub>OUT</sub> Output Voltage Setting (continued)**

OUT_SEL <7:0>	V <sub>OUT</sub> (V)	VOUT_SEL <7:0>	V <sub>OUT</sub> (V)	VOUT_SEL <7:0>	V <sub>OUT</sub> (V)	VOUT_SEL <7:0>	V <sub>OUT</sub> (V)
1	0.69	21	1.01	41	1.33	61	1.65
2	0.7	22	1.02	42	1.34	62	1.66
3	0.71	23	1.03	43	1.35	63	1.67
4	0.72	24	1.04	44	1.36	64	1.68
5	0.73	25	1.05	45	1.37	65	1.69
6	0.74	26	1.06	46	1.38	66	1.7
7	0.75	27	1.07	47	1.39	67	1.71
8	0.76	28	1.08	48	1.4	68	1.72
9	0.77	29	1.09	49	1.41	69	1.73
A	0.78	2A	1.1	4A	1.42	6A	1.74
B	0.79	2B	1.11	4B	1.43	6B	1.75
C	0.8	2C	1.12	4C	1.44	6C	1.76
D	0.81	2D	1.13	4D	1.45	6D	1.77
E	0.82	2E	1.14	4E	1.46	6E	1.78
F	0.83	2F	1.15	4F	1.47	6F	1.79
10	0.84	30	1.16	50	1.48	70	1.8
11	0.85	31	1.17	51	1.49	71	1.81
12	0.86	32	1.18	52	1.5	72	1.82
13	0.87	33	1.19	53	1.51	73	1.83
14	0.88	34	1.2	54	1.52	74	1.84
15	0.89	35	1.21	55	1.53	75	1.85
16	0.9	36	1.22	56	1.54	76	1.86
17	0.91	37	1.23	57	1.55	77	1.87
18	0.92	38	1.24	58	1.56	78	1.88
19	0.93	39	1.25	59	1.57	79	1.89
1A	0.94	3A	1.26	5A	1.58	7A	1.9
1B	0.95	3B	1.27	5B	1.59	7B	1.91
1C	0.96	3C	1.28	5C	1.6	7C	1.92
1D	0.97	3D	1.29	5D	1.61	7D	1.93
1E	0.98	3E	1.3	5E	1.62	7E	1.94
1F	0.99	3F	1.31	5F	1.63	7F	1.95

### 7.3.2 Enable and Adjusting UVLO

The ENx pin provides electrical on and off control of the device. After the ENx pin voltage exceeds the threshold voltage, the device starts operation. If each ENx pin voltage is pulled below the threshold voltage, the regulator stops switching and enters a low Iq state.

The EN pin has an internal pullup current source, allowing the user to float the EN pin for enabling the device. If an application requires controlling the EN pin, use open-drain or open-collector output logic to interface with the pin.

The device implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 500 mV. If an application requires either a higher UVLO threshold on the VIN pin or a secondary UVLO on the PVINx in split rail applications, then the user can configure the ENx pin as shown in [Figure 7-3](#), [Figure 7-4](#), and [Figure 7-5](#). When using the external UVLO function, TI recommends to set the hysteresis >500 mV.

The EN pin has a small pullup current,  $I_p$ , which sets the default state of the pin to enable when no external components are connected. The pullup current is also used to control the voltage hysteresis for the UVLO function because it increases by  $I_h$  after the EN pin crosses the enable threshold. The UVLO thresholds can be calculated using 式 2 and 式 3.

$$R_1 = \frac{V_{START} \left( \frac{V_{ENFALLING}}{V_{ENRISING}} \right) - V_{STOP}}{I_p \left( 1 - \frac{V_{ENFALLING}}{V_{ENRISING}} \right) + I_h} \quad (2)$$

$$R_2 = \frac{R_1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R_1 (I_h + I_p)} \quad (3)$$

where

- $I_h = 3 \mu A$
- $I_p = 3.9 \mu A$
- $V_{ENRISING} = 1.2 V$
- $V_{ENFALLING} = 1.15 V$

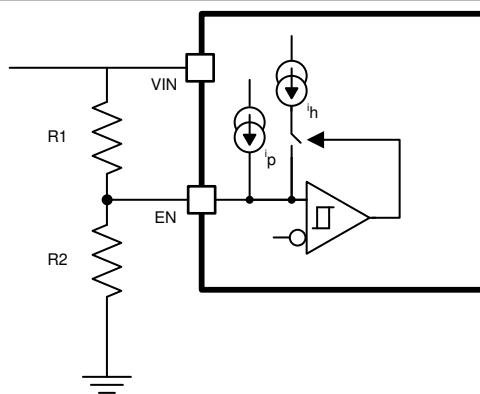


图 7-3. Adjustable VIN UVLO

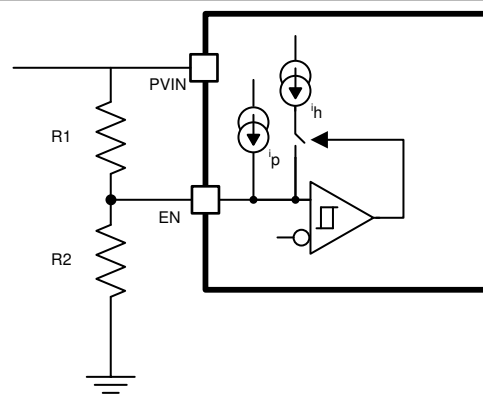


图 7-4. Adjustable PVIN UVLO, VIN > 4 V

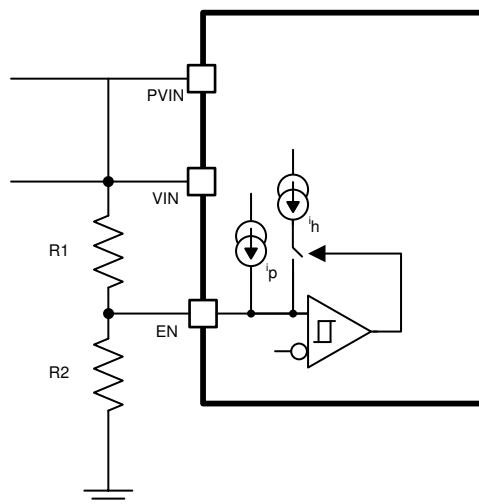


图 7-5. Adjustable VIN and PVIN UVLO



### 7.3.3 Soft-Start Time

The voltage on the respective SS pin controls the start-up of buck output. When the voltage on the SS pin is less than the internal 0.6-V reference, The TPS65263-Q1 regulates the internal feedback voltage to the voltage on the SS pin instead of 0.6 V. The SS pin can be used to program an external soft-start function or to allow output of buck to track another supply during start-up. The device has an internal pullup current source of 5.2  $\mu\text{A}$  (typical) that charges an external soft-start capacitor to provide a linear ramping voltage at the SS pin. The TPS65263-Q1 regulates the internal feedback voltage to the voltage on the SS pin, allowing VOUT to rise smoothly from 0 V to its regulated voltage without inrush current. The soft-start time can be calculated approximately by 式 4.

$$T_{ss}(\text{ms}) = \frac{C_{ss}(\text{nF}) \times V_{\text{ref}}(\text{V})}{I_{ss}(\mu\text{A})} \quad (4)$$

Many of the common power-supply sequencing methods can be implemented using the SSx and ENx pins. 図 7-6 shows the method implementing ratiometric sequencing by connecting the SSx pins of three buck channels together. The regulator outputs ramp up and reach regulation at the same time. When calculating the soft-start time, the pullup current source must be tripled in 式 4.

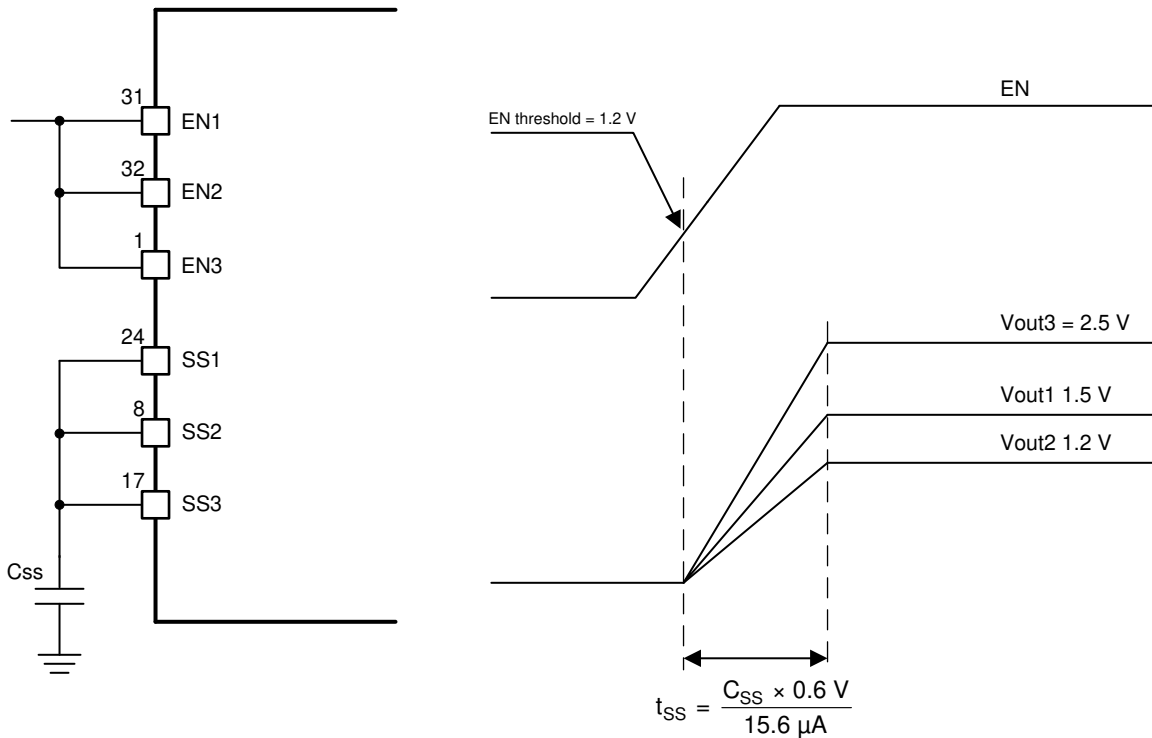
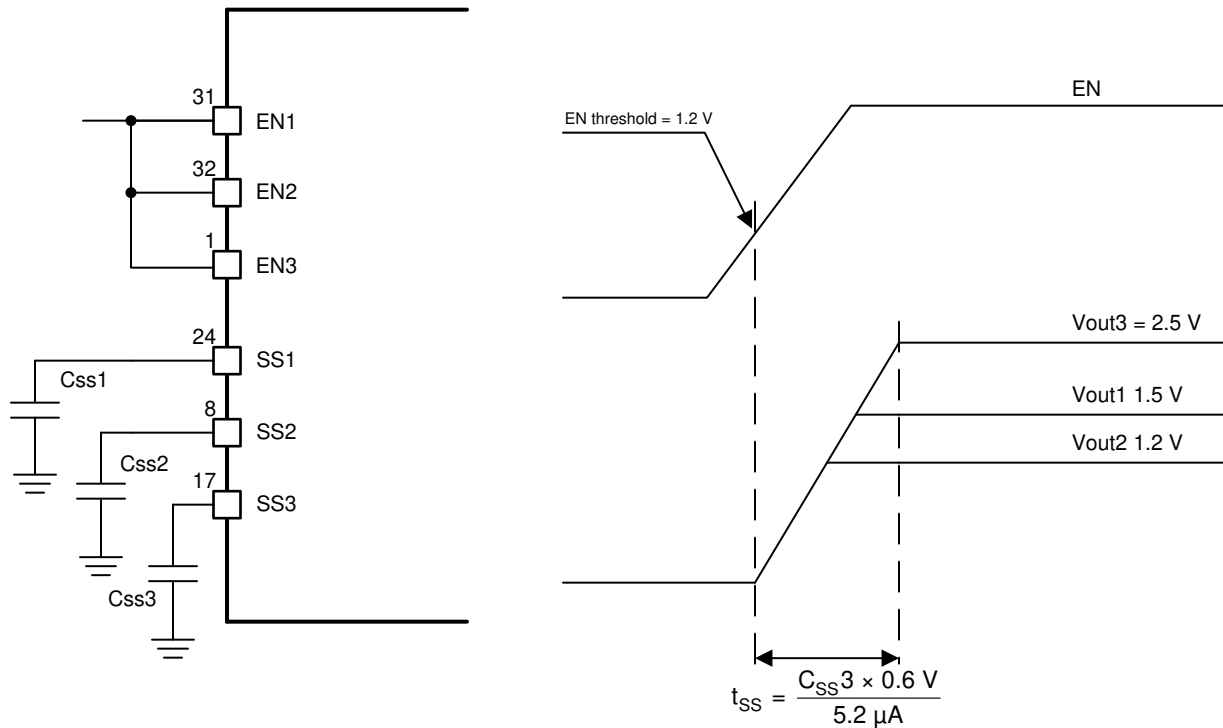


图 7-6. Ratiometric Power-Up Using SSx Pins

The user can implement simultaneous power-supply sequencing by connecting the capacitor to the SSx pin, shown in 图 7-7. Using 式 4 and 式 5, the capacitors can be calculated.

$$\frac{C_{ss1}}{V_{out1}} = \frac{C_{ss2}}{V_{out2}} = \frac{C_{ss3}}{V_{out3}} \quad (5)$$

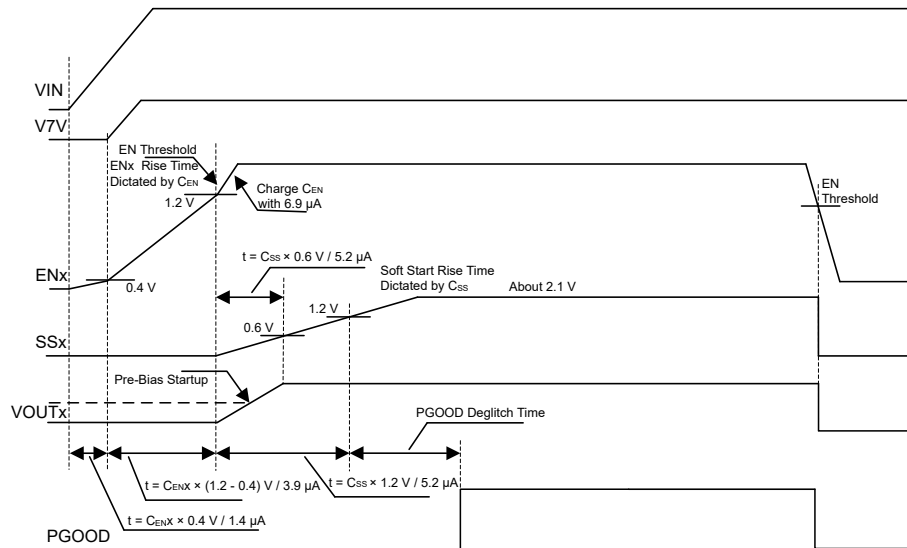


**7-7. Simultaneous Start-up Sequence Using SSx Pins**

### 7.3.4 Power-Up Sequencing

The TPS65263-Q1 has a dedicated enable pin and soft-start pin for each converter. The converter enable pins are biased by a current source that allows for easy sequencing by the addition of an external capacitor. Disabling the converter with an active pulldown transistor on the ENx pin allows for predictable power-down timing operation. [7-8](#) shows the timing diagram of a typical buck power-up sequence with connecting a capacitor at the ENx pin.

A typical 1.4- $\mu$ A current is charging the ENx pin from input supply. When the ENx pin voltage rises to typical 0.4 V, the internal V7V LDO turns on. A 3.9- $\mu$ A pullup current is sourcing ENx. After the ENx pin voltage reaches the ENx enabling threshold, a 3.0- $\mu$ A hysteresis current sources to the pin to improve noise sensitivity. The internal soft-start comparator compares the SS pin voltage to 1.2 V. When the SS pin voltage ramps up to 1.2 V, PGOOD monitor is enabled. After PGOOD deglitch time, PGOOD is deasserted. The SS pin voltage is eventually clamped around 2.1 V.



7-8. Start-up Power Sequence

### 7.3.5 V7V Low-Dropout Regulator and Bootstrap

Power for the high-side and low-side MOSFET drivers and most other internal circuitry is derived from the V7V pin. The internal built-in low-dropout linear regulator (LDO) supplies 6.3 V (typical) from VIN to V7V. The user must connect a 10- $\mu\text{F}$  ceramic capacitor from V7V pin to power ground.

If the input voltage, VIN, decreases to the UVLO threshold voltage, the UVLO comparator detects the V7V pin voltage and forces the converter off.

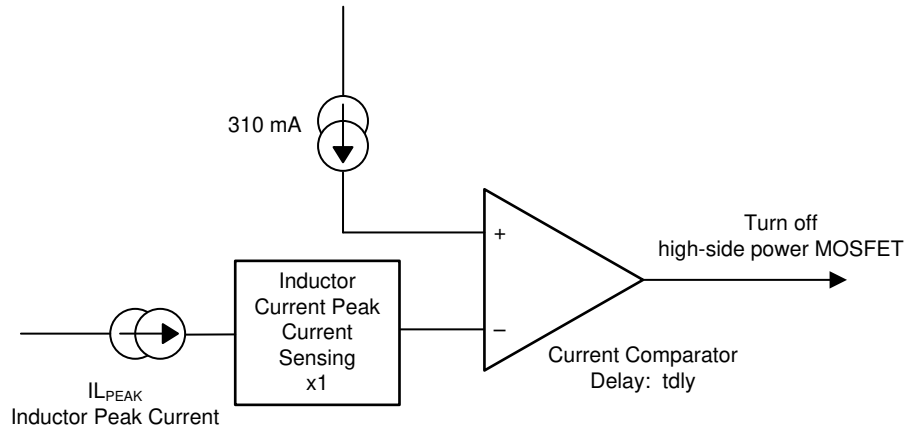
Each high-side MOSFET driver is biased from the floating bootstrap capacitor, CB, shown in 7-9, which is normally recharged during each cycle through an internal low-side MOSFET or the body diode of a low-side MOSFET when the high-side MOSFET turns off. The boot capacitor is charged when the BST pin voltage is less than VIN and BST-LX voltage is below regulation. TI recommends a 47-nF ceramic capacitor. TI recommends a ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher because of the stable characteristics over temperature and voltage. Each low-side MOSFET driver is powered from the V7V pin directly.

To improve dropout, the device is designed to operate at 100% duty cycle as long as the BST to LX pin voltage is greater than the BST-LX UVLO threshold, which is typically 2.1 V. When the voltage between BST and LX drops below the BST-LX UVLO threshold, the high-side MOSFET is turned off and the low-side MOSFET is turned on allowing the boot capacitor to be recharged.



$$I_{L\_PEAK} = 310 \text{ mA} + \frac{V_{in} - V_{out}}{L} \times t_{dly} \quad (6)$$

After the charge accumulated on the Vout capacitor is more than loading need, the COMP pin voltage drops to a low voltage driven by the error amplifier. There is an internal comparator at COMP pin. If the comp voltage is <0.35 V, the power stage stops switching to save power.



7-10. PSM Current Comparator

### 7.3.9 Slope Compensation

To prevent the subharmonic oscillations when the device operates at duty cycles greater than 50%, the TPS65263-Q1 adds built-in slope compensation, which is a compensating ramp to the switch current signal.

### 7.3.10 Overcurrent Protection

The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side MOSFET and low-side MOSFET.

#### 7.3.10.1 High-Side MOSFET Overcurrent Protection

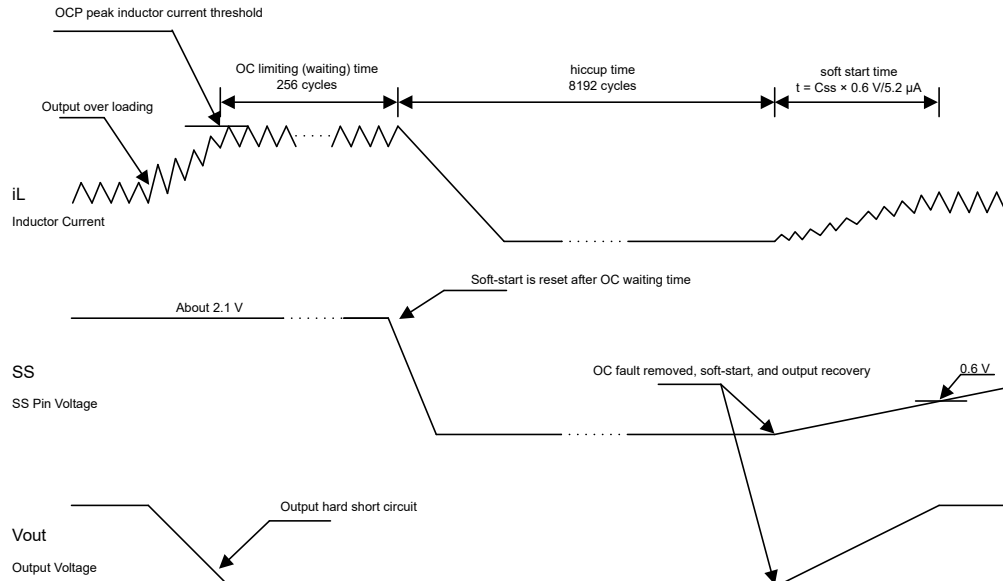
The device implements current mode control that uses the COMP pin voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle-by-cycle basis. Each cycle the switch current and the current reference generated by the COMP pin voltage are compared, when the peak switch current intersects the current reference, the high-side switch is turned off.

#### 7.3.10.2 Low-Side MOSFET Overcurrent Protection

While the low-side MOSFET is turned on, its conduction current is monitored by the internal circuitry. During normal operation, the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current limit. If the low-side sourcing current is exceeded, the high-side MOSFET is not turned on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET is turned on again when the low-side current is below the low-side sourcing current limit at the start of a cycle.

The low-side MOSFET can also sink current from the load. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario both MOSFETs are off until the start of the next cycle.

Furthermore, if an output overload condition (as measured by the COMP pin voltage) has lasted for more than the hiccup wait time which is programmed for 256 switching cycles shown in 7-11, the device shuts down and restarts after the hiccup time of 8192 cycles. The hiccup mode helps to reduce the device power dissipation under severe overcurrent condition.



☒ 7-11. Overcurrent Protection

### 7.3.11 Power Good

The PGOOD pin is an open-drain output. When feedback voltage of each buck is between 95% (rising) and 105% (falling) of the internal voltage reference, the PGOOD pin pulldown is deasserted and the pin floats. TI recommends to use a pullup resistor between the values of 10 and 100 kΩ to a voltage source that is 5.5 V or less. The PGOOD is in a defined state when the VIN input voltage is greater than 1 V, but with reduced current sinking capability. The PGOOD achieves full current sinking capability after the VIN input voltage is above UVLO threshold, which is 3.8 V.

The PGOOD pin is pulled low when any feedback voltage of buck is lower than 92.5% (falling) or greater than 107.5% (rising) of the nominal internal reference voltage. Also, when the PGOOD is pulled low, if the input voltage is undervoltage locked up, thermal shutdown is asserted, the EN pin is pulled low or the converter is in soft-start period.

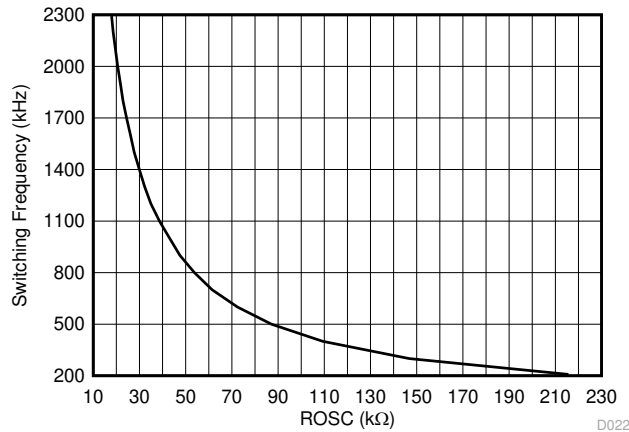
The power-good indicator for each buck channel can be read back through I<sup>2</sup>C. The bits in SYS\_STATUS[2:0] (address 0x06H) present the feedback voltage in regulation (logic 1) or not (logic 0) for buck1, buck2, and buck3 respectively

#### 7.3.11.1 Adjustable Switching Frequency

The ROSC pin can be used to set the switching frequency by connecting a resistor to GND. The switching frequency of the device is adjustable from 200 kHz to 2.3 MHz.

To determine the ROSC resistance for a given switching frequency, use 式 7 or the curve in ☒ 7-12. To reduce the solution size, the user must set the switching frequency as high as possible, but consider tradeoffs of the supply efficiency and minimum controllable on-time.

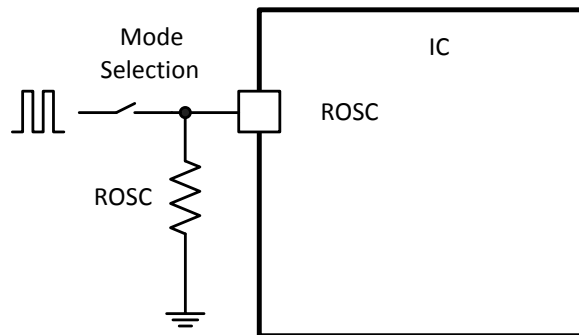
$$f_{\text{osc}} (\text{kHz}) = 37254 \times R(\text{k}\Omega)^{-0.966} \quad (7)$$



7-12. ROSC vs Switching Frequency

When an external clock applies to ROSC pin, the internal PLL has been implemented to allow internal clock synchronizing to an external clock between 200 and 2300 kHz. To implement the clock synchronization feature, connect a square wave clock signal to the ROSC pin with a duty cycle between 20% to 80%. The clock signal amplitude must transition lower than 0.4 V and higher than 2.0 V. The start of the switching cycle is synchronized to the falling edge of ROSC pin.

In applications where both resistor mode and synchronization mode are needed, the user can configure the device as shown in 7-13. Before an external clock is present, the device works in resistor mode and ROSC resistor sets the switching frequency. When an external clock is present, the synchronization mode overrides the resistor mode. The first time the ROSC pin is pulled above the ROSC high threshold (2.0 V), the device switches from the resistor mode to the synchronization mode and the ROSC pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock. TI does not recommend to switch from the synchronization mode back to the resistor mode because the internal switching frequency drops to 100 kHz first before returning to the switching frequency set by ROSC resistor.



7-13. Works With Resistor Mode and Synchronization Mode

### 7.3.12 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160°C typically. The device reinitiates the power-up sequence when the junction temperature drops below 140°C typically.

## 7.4 Device Functional Modes

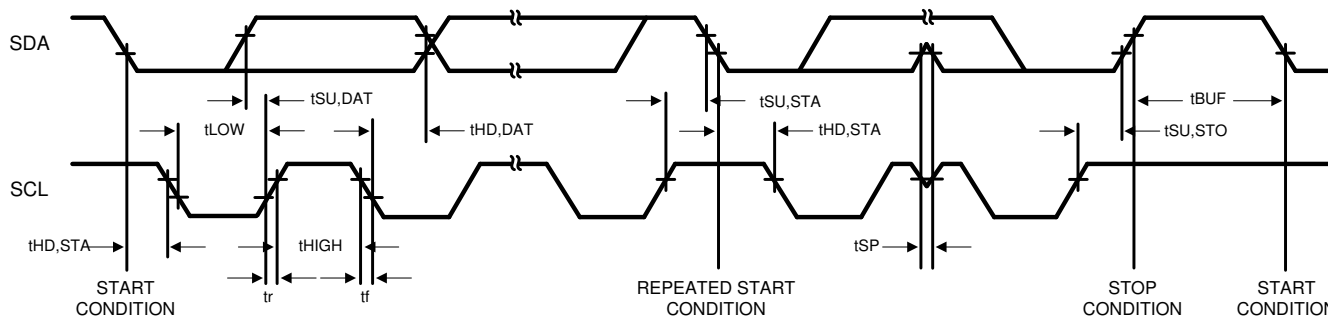
### 7.4.1 Serial Interface Description

I<sup>2</sup>C is a 2-wire serial interface developed by NXP Semiconductor (see *I<sup>2</sup>C-Bus Specification, Version 2.1*, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I<sup>2</sup>C-compatible devices connect to the I<sup>2</sup>C bus through open-drain I/O pins, SDA and SCL. A controller device, usually a microcontroller or a digital signal

processor, controls the bus. The controller is responsible for generating the SCL signal and device addresses. The controller also generates specific conditions that indicate the START and STOP of data transfer. A target device receives and/or transmits data on the bus under control of the controller device.

The TPS65263-Q1 device works as a target and supports the following data transfer modes, as defined in the I<sup>2</sup>C-Bus Specification: standard mode (100 kbps) and fast mode (400 kbps). The interface adds flexibility to the power-supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as supply voltage remains above 3.8 V (typical).

The data transfer protocol for standard and fast modes is exactly the same. Therefore, they are referred to as F/S-mode in this document. The TPS65263-Q1 device supports 7-bit addressing. 10-bit addressing and general call address are not supported.

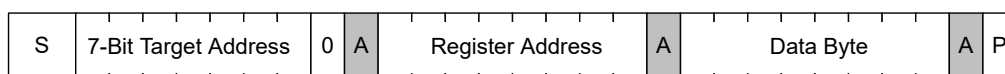


7-14. I<sup>2</sup>C Interface Timing Diagram

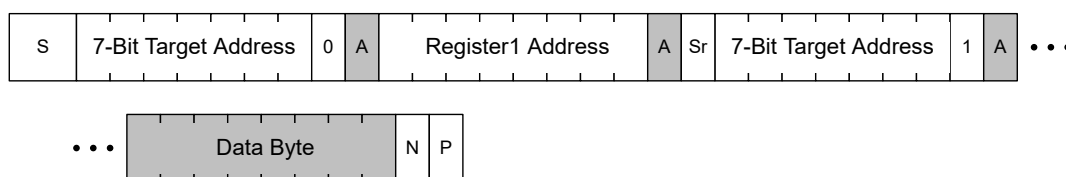
### 7.4.2 I<sup>2</sup>C Update Sequence

The TPS65263-Q1 requires a start condition, a valid I<sup>2</sup>C address, a register address byte, and a data byte for a single update. After the receipt of each byte, TPS65263-Q1 device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I<sup>2</sup>C address selects the TPS65263-Q1. TPS65263-Q1 performs an update on the falling edge of the LSB byte.

When the TPS65263-Q1 is in hardware shutdown (EN1, EN2, and EN3 pin tied to ground) the device cannot be updated through the I<sup>2</sup>C interface. Conversely, the I<sup>2</sup>C interface is fully functional during software shutdown (EN1, EN2, and EN3 bit = 0).



7-15. I<sup>2</sup>C Write Data Format



- A: Acknowledge
- N: Not Acknowledge
- S: Start
- P: Stop
- Sr: Repeated Start
- System Host
- Chip

7-16. I<sup>2</sup>C Read Data Format



## 7.5 Register Maps

**表 7-3. Register Addresses**

NAME	BITS	ADDRESS
VOUT2_SEL	8	0x01H
VOUT1_COM	8	0X03H
VOUT2_COM	8	0x04H
VOUT3_COM	8	0X05H
SYS_STATUS	8	0x06H

### 7.5.1 VOUT2\_SEL: Vout2 Voltage Selection Register (Address = 0x01H)

**图 7-17. VOUT2\_SEL: Vout2 Voltage Selection Register**

7	6	5	4	3	2	1	0
Vout2_Bit7	Vout2_Bit6	Vout2_Bit5	Vout2_Bit4	Vout2_Bit3	Vout2_Bit2	Vout2_Bit1	Vout2_Bit0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**表 7-4. VOUT2\_SEL: Vout2 Voltage Selection Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	Vout2_Bit7	R/W	0	"Go" bit, must set 1 to enable I <sup>2</sup> C controlled VID voltages
6	Vout2_Bit6	R/W	0	128 voltage selections with 7-bits control Voltage range: 0.68 to 1.95 V Voltage step resolution: 10 mV  0x00H: Vout2 = 0.68 V; 0x7FH: Vout2 = 1.95 V
5	Vout2_Bit5	R/W	0	
4	Vout2_Bit4	R/W	0	
3	Vout2_Bit3	R/W	0	
2	Vout2_Bit2	R/W	0	
1	Vout2_Bit1	R/W	0	
0	Vout2_Bit0	R/W	0	

### 7.5.2 VOUT1\_COM: Buck1 Command Register (offset = 0x03H)

**图 7-18. VOUT1\_COM: Buck1 Command Register**

7	6	5	4	3	2	1	0
N/A						Mode1	nEN1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**表 7-5. VOUT1\_COM: Buck1 Command Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:2	N/A	R/W	000000	Not used
1	Mode1	R/W	0	0: Enable buck 1 PSM operation at light load; 1: Forced buck 1 PWM mode operation
0	nEN1	R/W	0	0: Enable buck1; 1: Disable buck1

### 7.5.3 VOUT2\_COM: Buck2 Command Register (offset = 0x04H)

图 7-19. VOUT2\_COM: Buck2 Command Register

7	6	5	4	3	2	1	0
N/A	SR3	SR2	SR1	N/A	N/A	Mode2	nEN2

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-6. VOUT2\_COM: Buck2 Command Register Field Descriptions

Bit	Field	Type	Reset	Description
7	N/A	R/W	0	Not used
6	SR3	R/W	0	Vout2 VID voltage transition Slew Rate control.
5	SR2	R/W	0	000: 10 mV/cycle;                      001: 10 mV/2 cycles;
4	SR1	R/W	0	010: 10 mV/4 cycles;                011: 10 mV/8 cycles;
				100: 10 mV/16 cycles;               101: 10 mV/32 cycles;
				110: 10 mV/64 cycles;               111: 10 mV/128 cycles
3	N/A	R/W	0	Not used
2	N/A	R/W	0	Not used
1	Mode2	R/W	0	0: Enable buck 2 PSM operation at light load; 1: Forced buck 2 PWM mode operation
0	nEN2	R/W	0	0: Enable buck2; 1: Disable buck2

### 7.5.4 VOUT3\_COM: Buck3 Command Register (offset = 0x05H)

图 7-20. VOUT3\_COM: Buck3 Command Register

7	6	5	4	3	2	1	0
N/A						Mode3	nEN3

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-7. VOUT3\_COM: Buck3 Command Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	N/A	R/W	000000	Not used
1	Mode3	R/W	0	0: Enable buck 3 PSM operation at light load; 1: Forced buck 3 PWM mode operation
0	nEN3	R/W	0	0: Enable buck3; 1: Disable buck3

### 7.5.5 SYS\_STATUS: System Status Register (offset = 0x06H)

**图 7-21. SYS\_STATUS: System Status Register**

7	6	5	4	3	2	1	0
OTP	OC3	OC2	OC1	OTW	PGOOD3	PGOOD2	PGOOD1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**表 7-8. SYS\_STATUS: System Status Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	OTP	R	0	1: Die temperature over 160°C, which triggers over temperature protection; 0: Die overtemperature protection is not triggered.
6	OC3	R	0	1: Buck3 over current limiting and hiccup protection is triggered; 0: Buck3 current <b>not</b> beyond the current limit.
5	OC2	R	0	1: Buck2 overcurrent limiting and hiccup protection is triggered; 0: Buck2 current <b>not</b> beyond the current limit.
4	OC1	R	0	1: Buck1 overcurrent limiting and hiccup protection is triggered; 0: Buck1 current <b>not</b> beyond the current limit.
3	OTW	R	0	1: Die temperature over 125°C; 0: Die temperature below 125°C.
2	PGOOD3	R	0	1: Vout3 in power good monitor's range; 0: Vout3 not in power good monitor's range.
1	PGOOD2	R	0	1: Vout2 in power good monitor's range; 0: Vout2 not in power good monitor's range.
0	PGOOD1	R	0	1: Vout1 in power good monitor's range ; 0: Vout1 not in power good monitor's range.

## 8 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 8.1 Application Information

The device is triple-synchronous step-down dc/dc converter with I<sup>2</sup>C interface. It is typically used to convert a higher dc voltage to lower dc voltages with continuous available output current of 3 A/2 A/2 A.

### 8.2 Typical Application

The following design procedure can be used to select component values for the TPS65263-Q1. This section presents a simplified discussion of the design process.

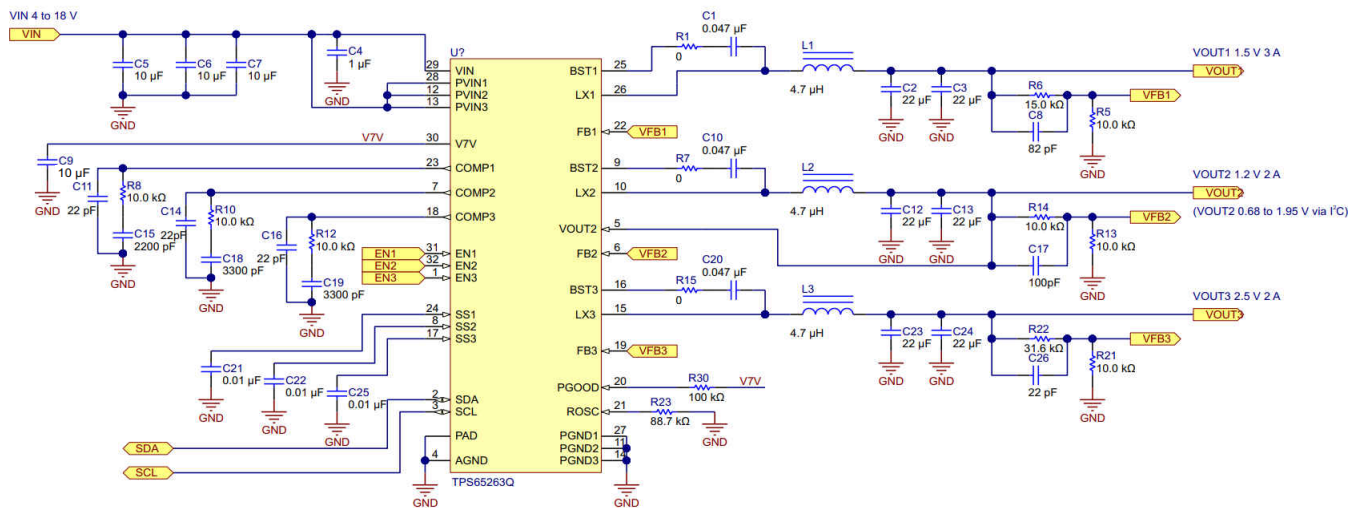


図 8-1. Typical Application Schematic

#### 8.2.1 Design Requirements

This example details the design of triple-synchronous step-down converter. A few parameters must be known to start the design process. These parameters are typically determined at the system level. For this example, we start with the following known parameters:

表 8-1. Design Parameters

PARAMETER	VALUE
Vout1	1.5 V
Iout1	3 A
Vout2	1.2 V
Iout2	2 A
Vout3	2.5 V
Iout3	2 A
Transient response 1-A load step	±5%
Input voltage	12 V normal, 4 to 18 V
Output voltage ripple	±1%

**表 8-1. Design Parameters (continued)**

PARAMETER	VALUE
Switching frequency	500 kHz

## 8.2.2 Detailed Design Procedure

### 8.2.2.1 Output Inductor Selection

To calculate the value of the output inductor, use 式 8. LIR is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impact the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, LIR is normally from 0.1 to 0.3 for the majority of applications.

$$L = \frac{V_{inmax} - V_{out}}{I_o \times LIR} \times \frac{V_{out}}{V_{inmax} \times f_{sw}} \quad (8)$$

For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. Calculate the RMS and peak inductor current from 式 10 and 式 11.

$$I_{ripple} = \frac{V_{inmax} - V_{out}}{L} \times \frac{V_{out}}{V_{inmax} \times f_{sw}} \quad (9)$$

$$I_{Lrms} = \sqrt{I_o^2 + \frac{\left( \frac{V_{out} \times (V_{inmax} - V_{out})}{V_{inmax} \times L \times f_{sw}} \right)^2}{12}} \quad (10)$$

$$I_{Lpeak} = I_{out} + \frac{I_{ripple}}{2} \quad (11)$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

### 8.2.2.2 Output Capacitor Selection

The three primary considerations for selecting the value of the output capacitor are:

- Output capacitor determines the modulator pole
- Output voltage ripple
- How the regulator responds to a large change in load current

The output capacitance must be selected based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criterion. The output capacitor needs to supply the load with current when the regulator cannot. This situation can occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as a transition from no load to full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a

tolerable amount of droop in the output voltage. 式 12 shows the minimum output capacitance necessary to accomplish this.

$$C_o = \frac{2 \times \Delta I_{out}}{f_{sw} \times \Delta V_{out}} \quad (12)$$

where

- $\Delta I_{out}$  is the change in output current
- $f_{sw}$  is the regulators switching frequency
- $\Delta V_{out}$  is the allowable change in the output voltage

式 13 calculates the minimum output capacitance needed to meet the output voltage ripple specification.

$$C_o > \frac{1}{8 \times f_{sw}} \times \frac{1}{\frac{V_{ripple}}{I_{ripple}}} \quad (13)$$

where

- $f_{sw}$  is the switching frequency
- $V_{ripple}$  is the maximum allowable output voltage ripple
- $I_{ripple}$  is the inductor ripple current

式 14 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification.

$$R_{esr} < \frac{V_{ripple}}{I_{ripple}} \quad (14)$$

Additional capacitance deratings for aging, temperature, and DC bias must be factored in, which increases this minimum value. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. The user must specify an output capacitor that can support the inductor ripple current. Some capacitor data sheets specify the root mean square (RMS) value of the maximum ripple current. Use 式 15 to calculate the RMS ripple current the output capacitor needs to support.

$$I_{corms} = \frac{V_{out} \times (V_{inmax} - V_{out})}{\sqrt{12} \times V_{inmax} \times L \times f_{sw}} \quad (15)$$

### 8.2.2.3 Input Capacitor Selection

The TPS65263-Q1 requires a high-quality ceramic, type X5R or X7R, input decoupling capacitor of at least 10  $\mu$ F of effective capacitance on the PVIN input voltage pins. In some applications, additional bulk capacitance can also be required for the PVIN input. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS65263-Q1. The input ripple current can be calculated using 式 16.

$$I_{inrms} = I_{out} \times \sqrt{\frac{V_{out}}{V_{inmin}} \times \frac{(V_{inmin} - V_{out})}{V_{inmin}}} \quad (16)$$

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance-to-volume ratio and are fairly stable over temperature. The output

capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases. The input capacitance value determines the input ripple voltage of the regulator. Use 式 17 to calculate the input voltage ripple.

$$\Delta V_{in} = \frac{I_{outmax} \times 0.25}{C_{in} \times f_{sw}} \quad (17)$$

### 8.2.2.4 Loop Compensation

The TPS65263-Q1 incorporates a peak current mode control scheme. The error amplifier is a transconductance amplifier with a gain of 300  $\mu$ S. A typical type II compensation circuit adequately delivers a phase margin between 40° and 90°.  $C_b$  adds a high-frequency pole to attenuate high-frequency noise when needed. To calculate the external compensation components, follow these steps.

1. Select switching frequency,  $f_{sw}$ , that is appropriate for application depending on L and C sizes, output ripple, EMI, and so forth. Switching frequency between 500 kHz to 1 MHz gives best trade-off between performance and cost. To optimize efficiency, lower switching frequency is desired.
2. Set up crossover frequency,  $f_c$ , which is typically between 1/5 and 1/20 of  $f_{sw}$ .
3.  $R_C$  can be determined by:

$$R_C = \frac{2\pi \times f_c \times V_o \times C_o}{G_{m-EA} \times V_{ref} \times G_{m-PS}} \quad (18)$$

where

- $G_{m-EA}$  is the error amplifier gain (300  $\mu$ S).
- $G_{m-PS}$  is the power stage voltage to current conversion gain (7.4 A/V).

4. Calculate  $C_C$  by placing a compensation zero at or before the dominant pole  $\left( f_p = \frac{1}{C_o \times R_L \times 2\pi} \right)$ .

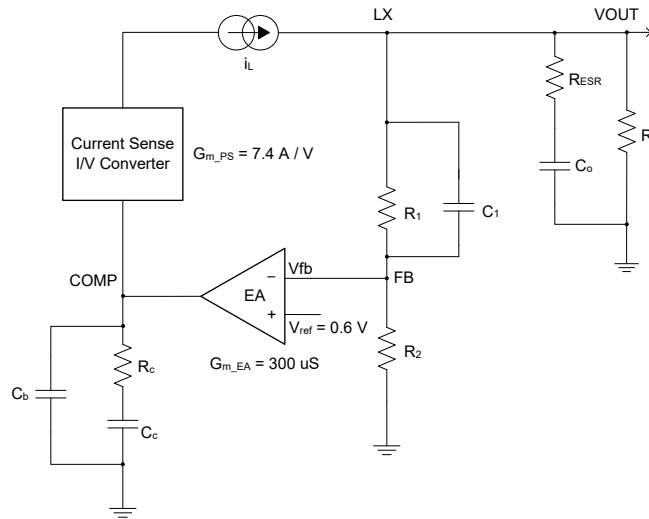
$$C_C = \frac{R_L \times C_o}{R_C} \quad (19)$$

5. Optional  $C_b$  can be used to cancel the zero from the ESR associated with  $C_o$ .

$$C_b = \frac{R_{ESR} \times C_o}{R_C} \quad (20)$$

6. Type III compensation can be implemented with the addition of one capacitor,  $C_1$ . This allows for slightly higher loop bandwidths and higher phase margins. If used, calculate  $C_1$  from 式 21.

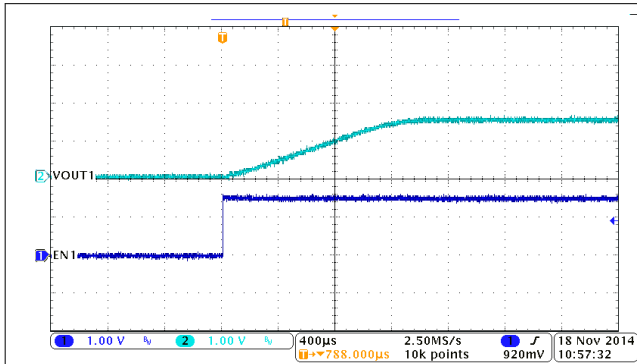
$$C_1 = \frac{1}{2\pi \times R_1 \times f_c} \quad (21)$$



8-2. DC/DC Loop Compensation

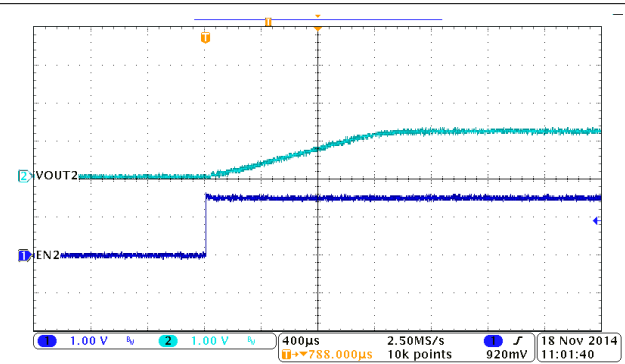


### 8.2.3 Application Curves



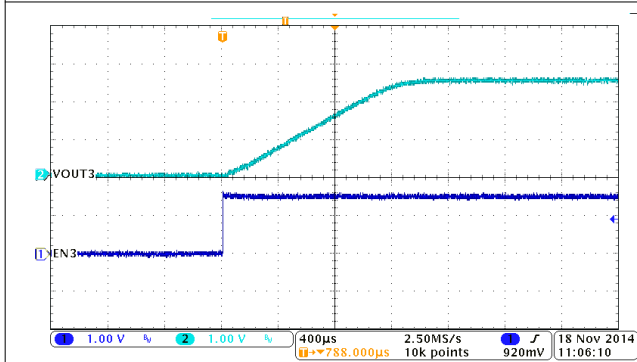
lout = 3 A

**8-3. BUCK1, Soft Start**



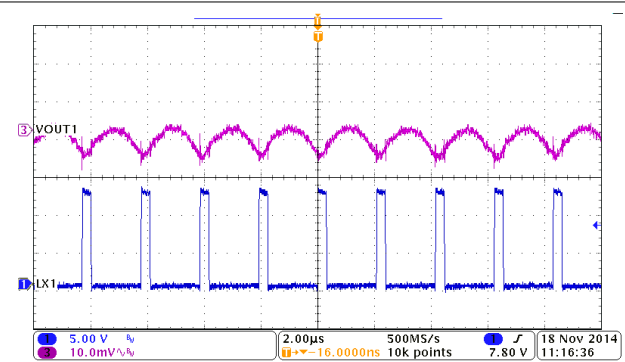
lout = 2 A

**8-4. BUCK2, Soft Start**



lout = 2 A

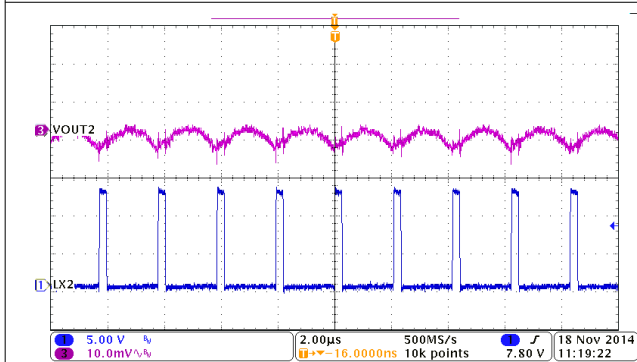
**8-5. BUCK3, Soft Start**



A.

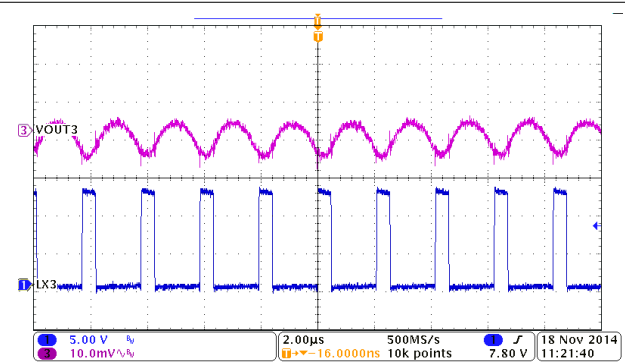
lout = 3 A

**8-6. BUCK1, Output Voltage Ripple**



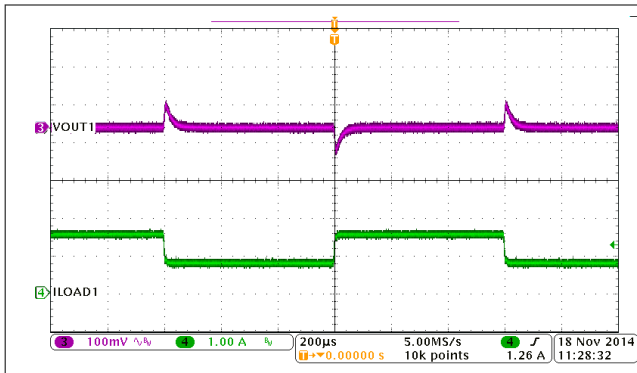
lout = 2 A

**8-7. BUCK2, Output Voltage Ripple**



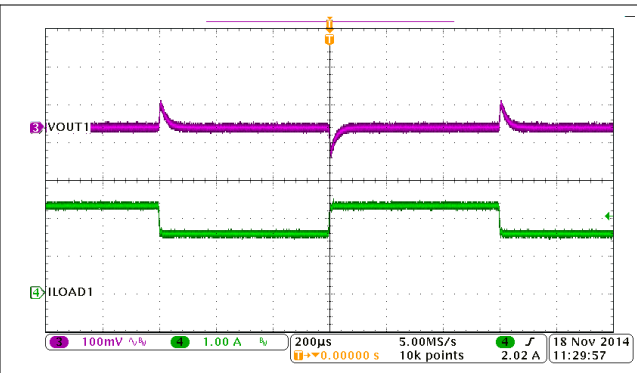
lout = 2 A

**8-8. BUCK3, Output Voltage Ripple**



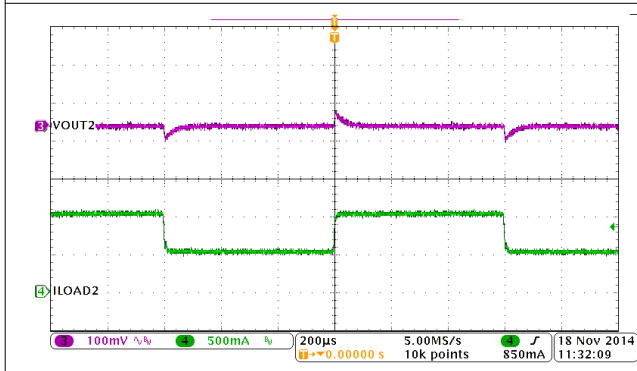
0.75 to 1.5 A SR = 0.25 A/µs

**8-9. BUCK1, Load Transient**



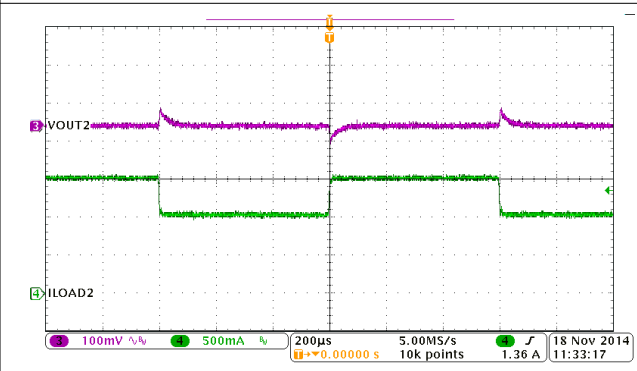
1.5 to 2.25 A SR = 0.25 A/µs

**8-10. BUCK1, Load Transient**



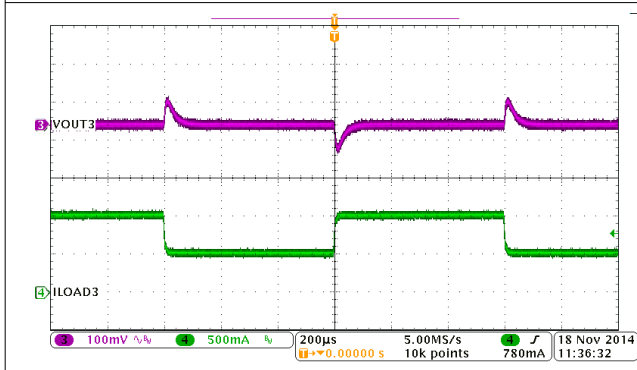
0.5 to 1.0 A SR = 0.25 A/µs

**8-11. BUCK2, Load Transient**



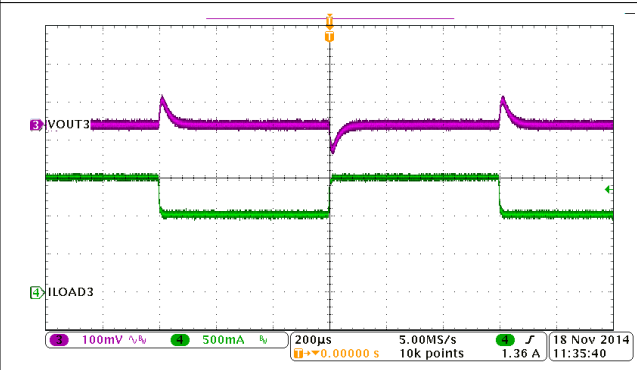
1.0 to 1.5 A SR = 0.25 A/µs

**8-12. BUCK2, Load Transient**



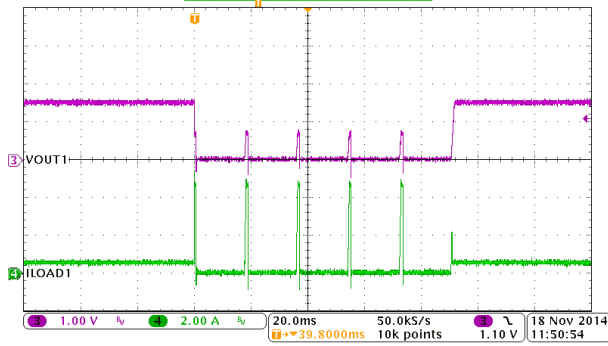
0.5 to 1.0 A SR = 0.25 A/µs

**8-13. BUCK3, Load Transient**

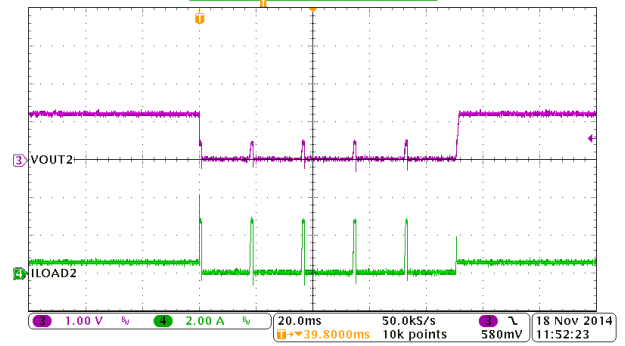


1.0 to 1.5 A SR = 0.25 A/µs

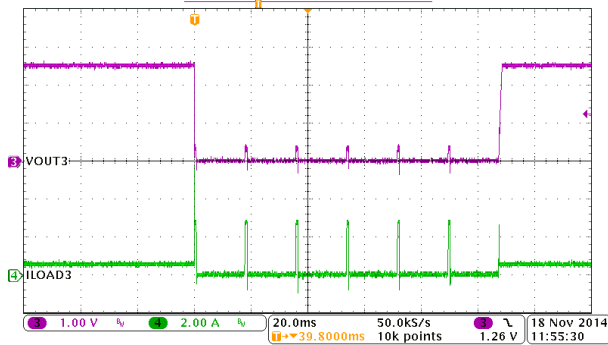
**8-14. BUCK3, Load Transient**



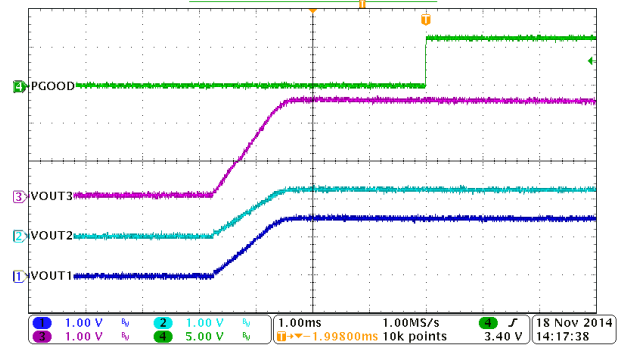
8-15. BUCK1, Hiccup and Recovery



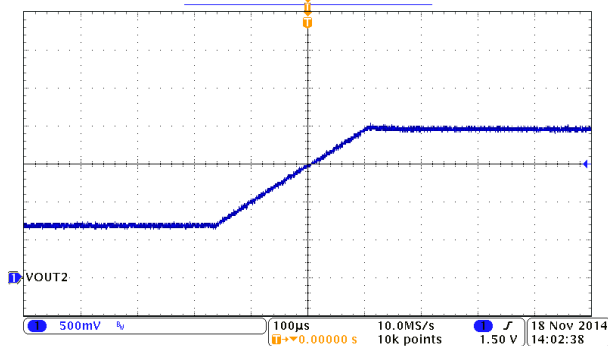
8-16. BUCK2, Hiccup and Recovery



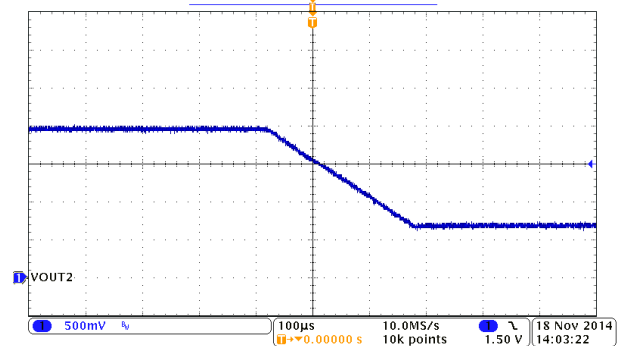
8-17. BUCK3, Hiccup and Recovery



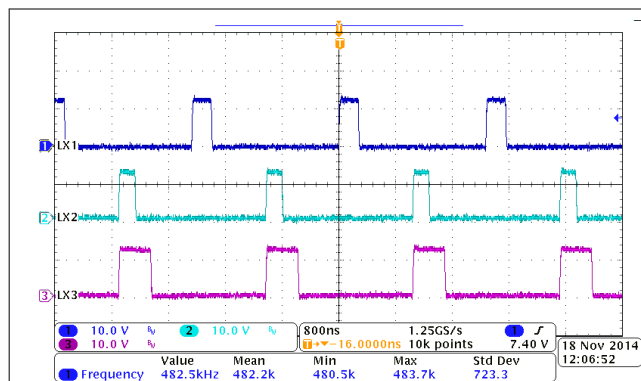
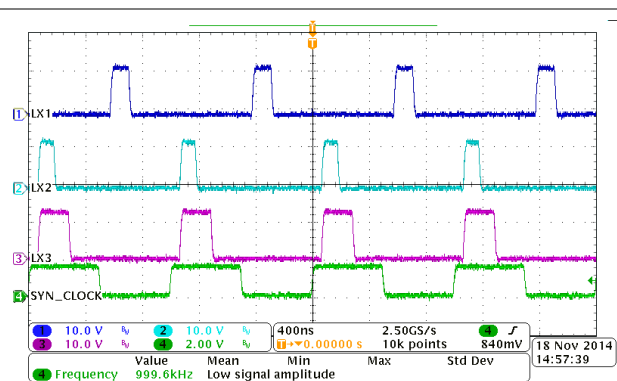
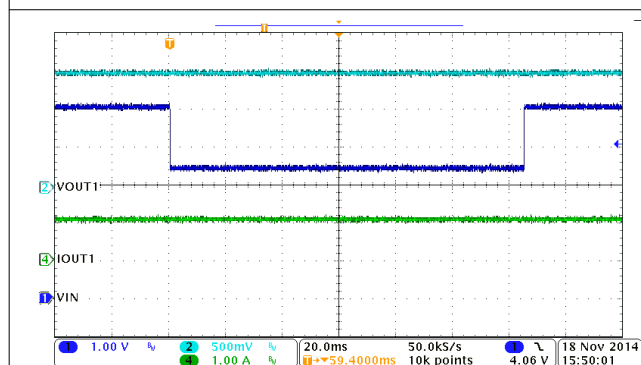
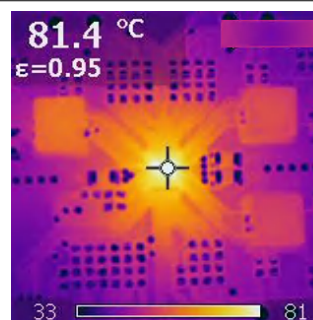
8-18. PGOOD



8-19. VID2 from 00 to 7F, SR = 10 mV/Cycle



8-20. VID2 from 7F to 00, SR = 10 mV/Cycle


**8-21. 180° Out-of-Phase**

**8-22. Synchronization with External Clock**

**8-23. Operation at VIN Drop to 2.5 V**


VIN = 12 V, VOUT1 = 1.5 V/3 A, VOUT2 = 1.2 V/2 A,  
VOUT3 = 2.5 V/2 A,  
T<sub>A</sub> = 26.8°C EVM condition 4 layers, 75 mm × 75 mm

**8-24. Thermal Signature of TPS65263-Q1EVM Operating**

## 8.3 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 4 and 18 V. This input power supply must be well regulated. If the input supply is located more than a few inches from the TPS65263-Q1 converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47  $\mu$ F is a typical choice.

## 8.4 Layout

### 8.4.1 Layout Guidelines

[8-25](#) shows the TPS65263-Q1 on a 2-layer PCB.

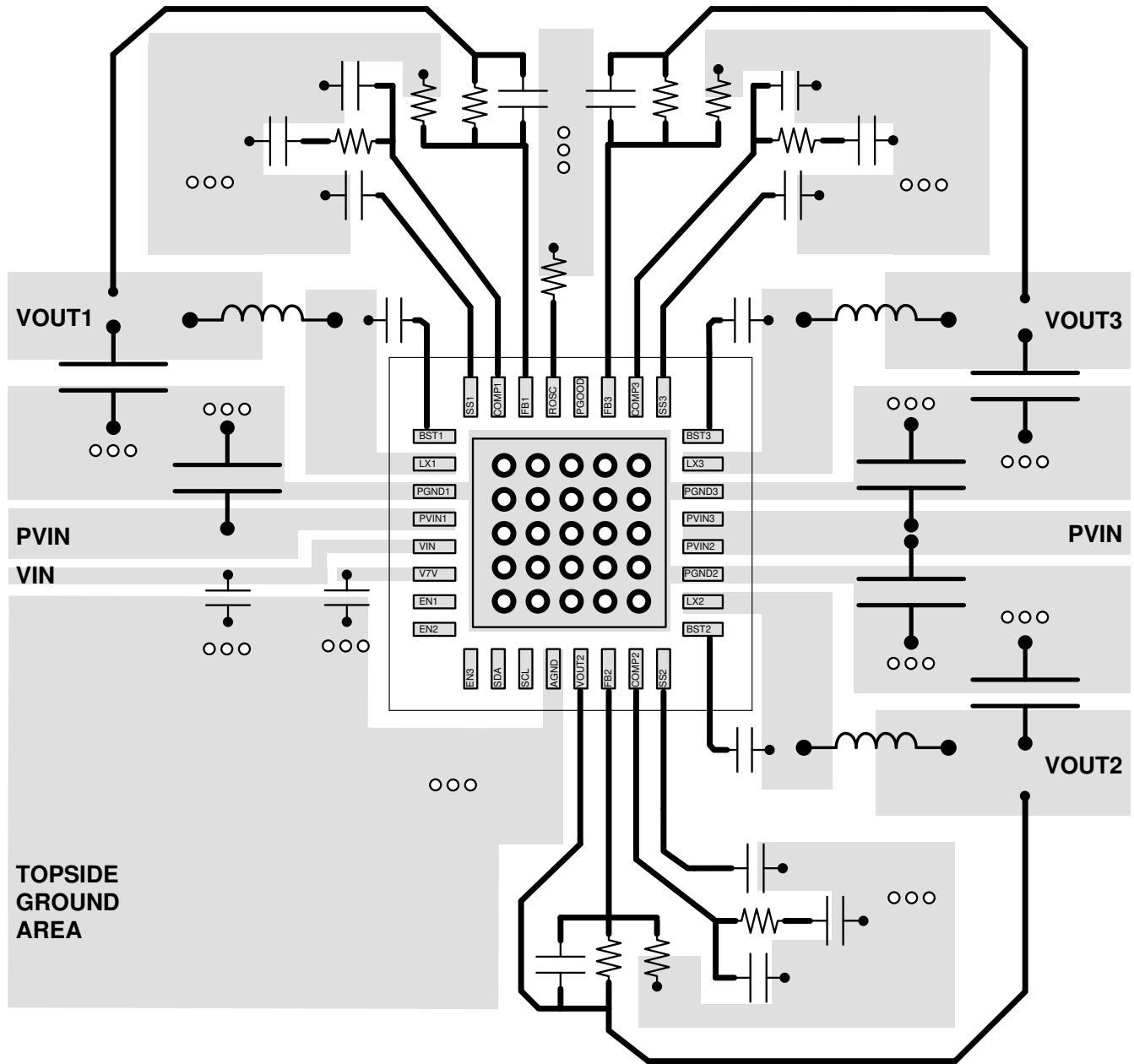
Layout is a critical portion of good power-supply design. See [8-25](#) for a PCB layout example. The top contains the main power traces for PVIN, VOUT, and LX. The top layer also has connections for the remaining pins of the TPS65263-Q1 and a large top-side area filled with ground. The top-layer ground area must be connected to the bottom layer ground using vias at the input bypass capacitor, the output filter capacitor, and directly under the TPS65263-Q1 device to provide a thermal path from the exposed thermal pad land to ground. The bottom layer acts as ground plane connecting analog ground and power ground.

For operation at full rated load, the top-side ground area together with the bottom-side ground plane must provide adequate heat dissipating area. Several signals paths conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies' performance. To help eliminate these problems, bypass the PVIN pin to ground with a low-ESR ceramic bypass capacitor with X5R or X7R dielectric. Take care to minimize the loop area formed by the bypass capacitor connections, the PVIN pins, and the ground connections. The VIN pin must also be bypassed to ground using a low-ESR ceramic capacitor with X5R or X7R dielectric.

Because the LX connection is the switching node, the output inductor must be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The output filter capacitor ground must use the same power ground trace as the PVIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width. The small signal components must be grounded to the analog ground path.

The FB and COMP pins are sensitive to noise so the resistors and capacitors must be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown.

### 8.4.2 Layout Example



- 0.010-inch Diameter Thermal VIA to Ground Plane
- VIA to Ground Plane

8-25. PCB Layout

## 9 Device and Documentation Support

### 9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 9.2 サポート・リソース

**TI E2E™ サポート・フォーラム**は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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### 9.3 Trademarks

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### 9.4 静電気放電に関する注意事項



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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。



### 9.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65263QRHBRQ1	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 65263Q	
TPS65263QRHBTQ1	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 65263Q	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**OTHER QUALIFIED VERSIONS OF TPS65263-Q1 :**

- Catalog : [TPS65263](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65263QRHBRQ1	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS65263QRHBTQ1	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65263QRHBRQ1	VQFN	RHB	32	3000	346.0	346.0	33.0
TPS65263QRHBTQ1	VQFN	RHB	32	250	210.0	185.0	35.0

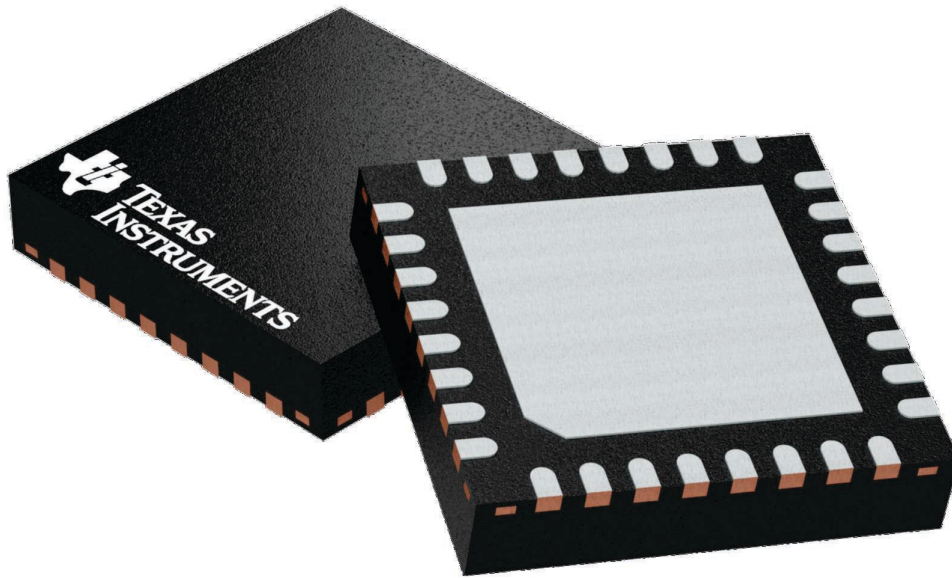
## GENERIC PACKAGE VIEW

**RHB 32**

**VQFN - 1 mm max height**

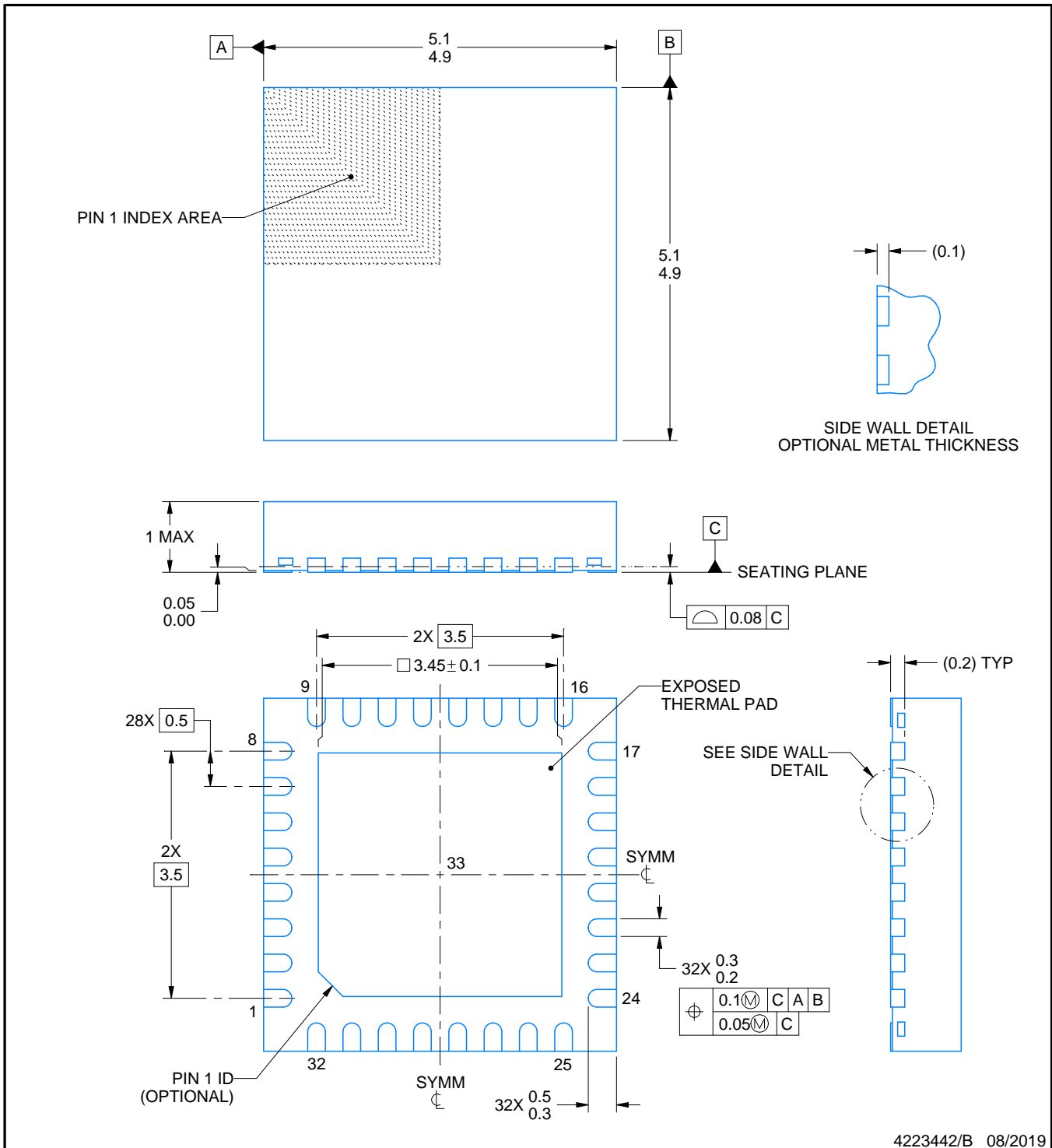
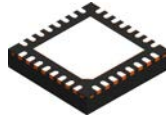
5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

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4223442/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

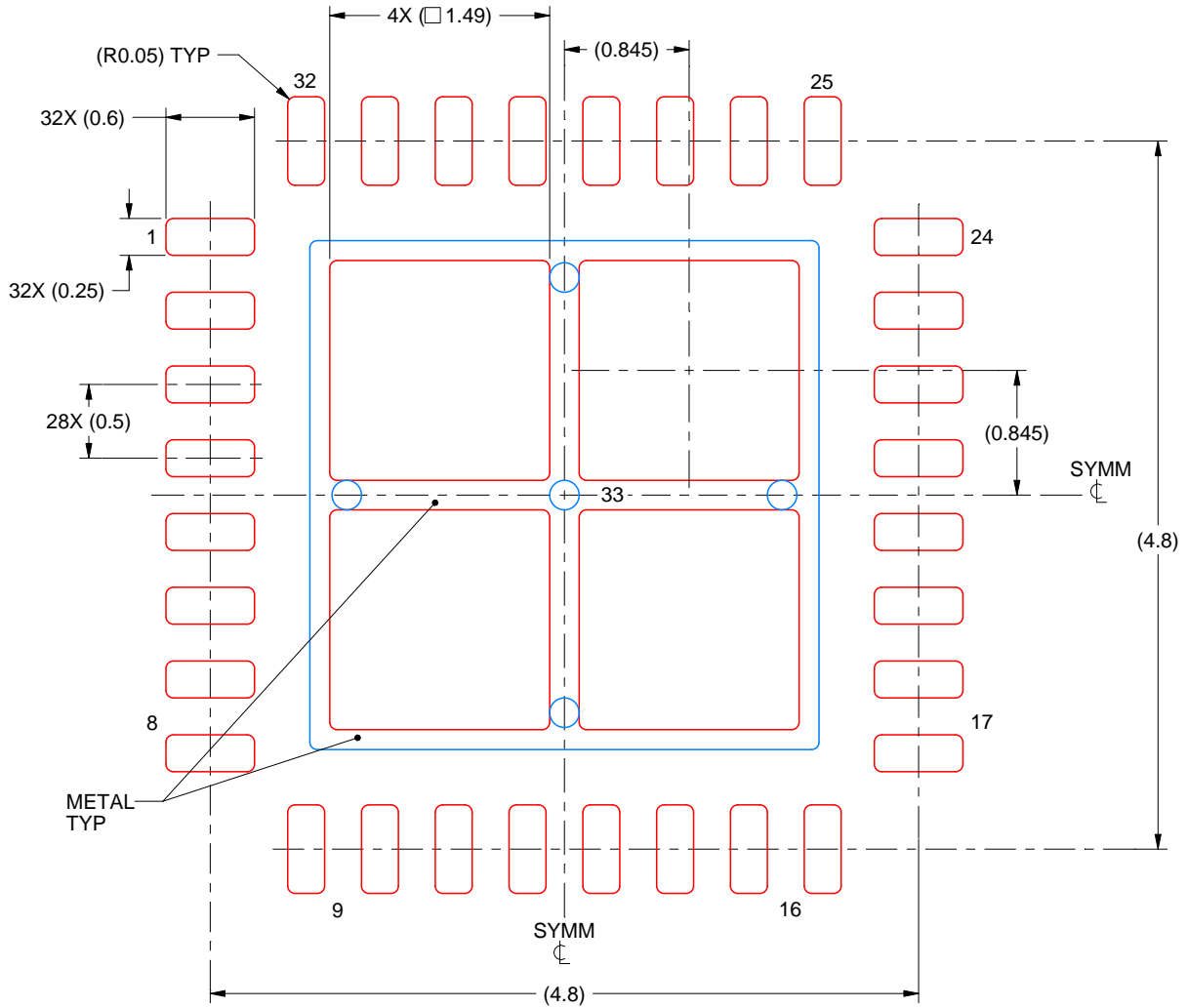


# EXAMPLE STENCIL DESIGN

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:  
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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