TEXAS INSTRUMENTS
TPS65283, TPS65283-1
JAJSHI2E – JUNE 2014 – REVISED MAY 2019

TPS65283、TPS65283-1 入力電圧 4.5V～18V、最大電流 3.5A および 2.5A、電力分配スイッチ搭載のデュアル同期整流降圧型コンバータ

1 特長

- 降圧型コンバータ
  - 広い入力電圧範囲:4.5～18V
  - 統合型デュアル降圧コンバータ、最大連続電流 3.5A (Buck1)/2.5A (Buck2)
  - 帰還基準電圧:0.6V±1%
  - 可変スイッチング周波数:200kHz～2MHz
  - ソフト・スタート時間 (2.4ms) を内部生成
  - 外部クロックへの同期
  - サイクル単位の電流制限
  - 各コンバータのパワー・グッド・インジケータ
  - 軽負荷時の連続電流モード (TPS65283) またはパルス・スキップ・モード (PSM) (TPS65283-1)
- 電力分配スイッチ
  - オン抵抗 60mΩ の電力分配スイッチを内蔵
  - 動作入力電圧範囲:2.4～6V
  - 調整可能な電流制限 (最高 2.7A)
  - 1.25A (標準値) で ±10% の電流制限精度
  - 自動復帰機能付きの過電流保護
  - 入力から出力への逆電圧保護
  - 過熱保護
  - 24 リード VQFN (RGE) 4mm × 4mm パッケージ

2 アプリケーション

- ポートおよび USB ハブ
- セットトップ・ボックス
- デジタル TV
- DSL / ケーブル・モデム、ワイヤレス・ルータ
- ホーム・ゲートウェイおよびアクセス・ポイント・ネットワーク
- 車載用インフォテインメント

3 概要

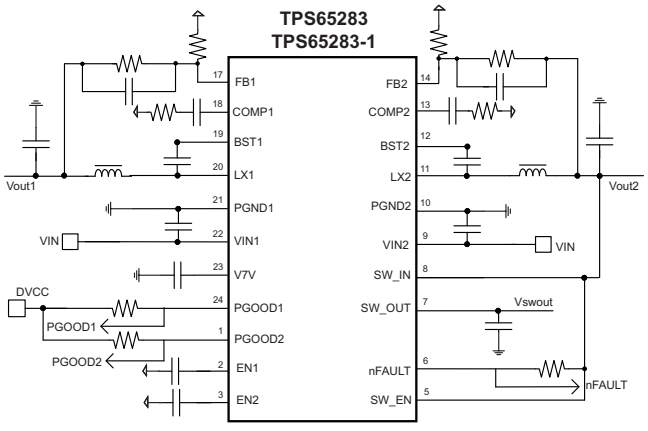
熱的に強化された 4mm × 4mm の VQFN パッケージの TPS65283、TPS65283-1 は、入力電圧 4.5V～18V、出力電流 3.5A/2.5A のフル機能の同期整流降圧型 DC-DC コンバータです。このコンバータは、高い効率とハイサイドおよびローサイド MOSFET の内蔵により小型の設計に最適化されています。このデバイスは、電力分配システム用の 1 つの N チャネル MOSFET パワー・スイッチも内蔵しています。このデバイスは、高精度の電流制限と高速な保護応答を必要とする総合的な電力分配ソリューションに利用できます。

製品情報(1)

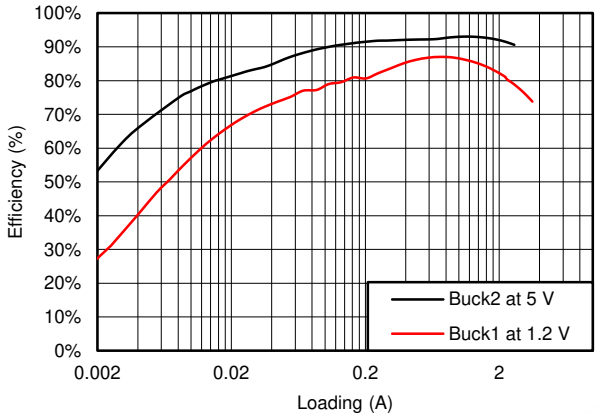
型番	パッケージ	本体サイズ(公称)
TPS65283	VQFN (24)	4.00mm×4.00mm
TPS65283-1		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

4 代表的な回路図



効率、Vin = 12V、PSM



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5 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision D (August 2017) から **Revision E** に変更 **Page**

- Added R_{OSC} resistor in Figure 26 ... 17

Revision C (August 2014) から **Revision D** に変更 **Page**

- 「特長」の箇条書き項目を「100mA～2.7A」から「最高 2.7A」に 変更 ... 1
- 「概要」の 1 番目および 2 番目の段落でテキスト「標準値 100mA から約 2.7A まで」を 削除 ... 3
- Changed "232 kΩ" to "80.6 kΩ" in the Description for RSET in the Pin Functions table. ... 4
- Added I_{OS} spec condition for R_{SET} = 80.6 kΩ ... 7
- Changed from "RSET is 9.1 kΩ ≤ RLIM ≤ 232 kΩ" to "RSET is 9.1 kΩ ≤ RLIM ≤ 80.6 kΩ" in the *Programming the Current-Limit Threshold* section. ... 15
- Changed from "...adjustable 75 mA to 2.7 A" to "up to 2.7 mA..." in the Comments section of Table 2 (4 places). ... 22

Revision B (July 2014) から **Revision C** に変更 **Page**

- Updated V_{7V} and V_{SYNC_LO} minimum in *Electrical Characteristics* ... 6
- Updated transition voltage to lower than 0.4 V for clock signal amplitude ... 17

Revision A (June 2014) から **Revision B** に変更 **Page**

- デバイスのステータスを「量産データ」に変更 ... 1

2014年6月 発行のものから更新 **Page**

- Changed Equation 3 From: f_{osc} (kHz) = 41008 × R (kΩ)$^{-0.979}$ To: f_{osc} (kHz) = 47863 × R (kΩ)$^{-0.988}$ ... 16

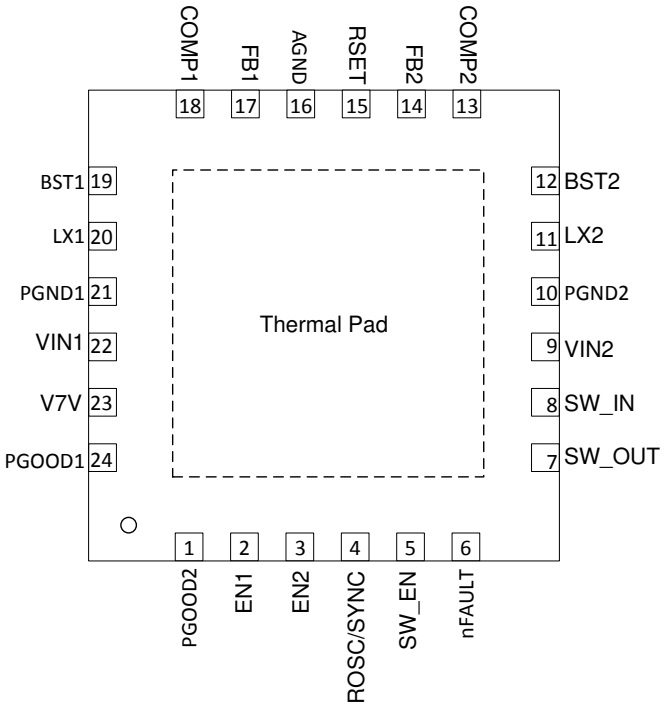
6 概要（続き）

独立した 60mΩ の電力分配スイッチは、外付け抵抗を使用してプログラムできる電流制限スレッショルドに出力電流を制限します。1.25A (標準値) で ±10% の電流制限精度を達成できます。過電流および逆電圧条件では、nFAULT 出力が LOW にアサートされます。

DC-DC コンバータの固定周波数ピーク電流モード制御により、補償が簡素化され、過渡応答が最適化されます。サイクル単位の過電流保護とヒカップ・モード動作により、降圧出力の短絡または過負荷条件中の MOSFET の消費電力が制限されます。ダイ温度が熱過負荷スレッショルドを超えると、過熱保護機能によりデバイスはシャットダウンされます。

7 Pin Configuration and Functions

24 Leads
Plastic VQFN (RGE)
(Top View)



(There is no electric signal down boned to thermal pad inside IC. Exposed thermal pad must be soldered to PCB for optimal thermal performance.)

Pin Functions

PIN		DESCRIPTION
NAME	NO.	
PGOOD2	1	Power good indicator pin. Asserts low if the output voltage of buck2 is out of range due to thermal shutdown, dropout, over-voltage, EN, shutdown, or during slow start.
EN1	2	Enable pin for buck 1. A high signal on this pin enables buck1. For a delayed start-up, add a small ceramic capacitor from this pin to ground.
EN2	3	Enable pin for buck 2. A high signal on this pin enables buck2. For a delayed start-up, add a small ceramic capacitor from this pin to ground.
ROSC/SYNC	4	Automatically select clock frequency program mode and clock synchronization mode. Program the switching frequency of the device from 200 kHz to 2 MHz with an external resistor connecting to the pin. In clock synchronization mode, the device automatically synchronizes to an external clock applied to the pin.
SW_EN	5	Enable power switch. Float to enable.

Pin Functions (continued)

PIN		DESCRIPTION
NAME	NO.	
nFAULT	6	Active low open-drain output. Asserted during overcurrent or reverse-voltage condition of power switch.
SW_OUT	7	Power switch output
SW_IN	8	Power switch input
VIN2	9	Input power supply for buck2. Connect this pin as close as possible to the (+) terminal of input ceramic capacitor (10 µF suggested).
PGND2	10	Power ground connection. Connect this pin as close as possible to the (–) terminal of input capacitor of buck2.
LX2	11	Switching node connection to the inductor and bootstrap capacitor for buck2 converter. This pin voltage swings from a diode voltage below the ground up to input voltage of buck2.
BST2	12	Bootstrapped supply to the high-side floating gate driver in buck converter. Connect a capacitor (47 nF recommended) from this pin to LX2.
COMP2	13	Error amplifier output and loop compensation pin for buck2. Connect a series resistor and capacitor to compensate the control loop of buck2 with peak current PWM mode.
FB2	14	Feedback sensing pin for buck2 output voltage. Connect this pin to the resistor divider of buck2 output. The feedback reference voltage is 0.6 V ±1%.
RSET	15	Power switch current limit control pin. An external resistor used to set current limit threshold of power switch. Recommended 9.1 kΩ ≤ R_{SET} ≤ 80.6 kΩ.
AGND	16	Analog ground common to buck controller and power switch controller. AGND must be routed separately from high current power grounds to the (–) terminal of bypass capacitor of internal V7V LDO output.
FB1	17	Feedback sensing pin for buck1 output voltage. Connect this pin to the resistor divider of buck1 output. The feedback reference voltage is 0.6 V ±1%.
COMP1	18	Error amplifier output and loop compensation pin for buck1. Connect a series resistor and capacitor to compensate the control loop of buck1 converter with peak current PWM mode.
BST1	19	Bootstrapped supply to the high side floating gate driver in buck converter. Connect a capacitor (recommend 47 nF) from this pin to LX1.
LX1	20	Switching node connection to the inductor and bootstrap capacitor for buck1. This pin voltage swings from a diode voltage below the ground up to input voltage of buck1.
PGND1	21	Power ground connection. Connect this pin as close as possible to the (–) terminal of input capacitor of buck1.
VIN1	22	Input power supply for buck1 and internal analog bias circuitries. Connect this pin as close as possible to the (+) terminal of an input ceramic capacitor (10 µF suggested).
V7V	23	Internal linear regulator (LDO) output with input from VIN1. The internal driver and control circuits are powered from this voltage. Decouple this pin to power ground with a minimum 1-µF ceramic capacitor. The output voltage level of LDO is regulated to typical 6.3 V for optimal conduction on-resistances of internal power MOSFETs. In PCB design, the power ground and analog ground should have one-point common connection at the (–) terminal of V7V bypass capacitor.
PGOOD1	24	Power good indicator pin. Asserts low if the output voltage of buck1 is out of range due to thermal shutdown, dropout, over-voltage, EN shutdown or during slow start.
PowerPAD™	—	Exposed pad beneath the IC. Connect to the power ground. Always solder power pad to the board, and have as many vias as possible on the PCB to enhance power dissipation. There is no electric signal down bonded to paddle inside the IC package.

8 Specifications

8.1 Absolute Maximum Ratings

(Operating in a typical application circuit) over operating free-air temperature range and all voltages are with respect to AGND (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage	VIN1, LX1, VIN2, LX2	–0.3	20	V
	LX1, LX2 (Maximum withstand voltage transient <20 ns)	–1	20	V
	BST1, BST2 referenced to LX1, LX2 pin respectively	–0.3	7	V
	EN1, EN2, SW_EN, PGOOD1, PGOOD2, nFAULT, V7V, SW_IN, SW_OUT, ROSC	–0.3	7	V
	COMP1, COMP2, RSET, FB1, FB2	–0.3	3.6	V
	AGND, PGND1, PGND2	–0.3	0.3	V
T_J	Operating junction temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–55	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	–2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	–500	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Supply input voltage	4.5		18	V
T_J	Operating junction temperature	–40		125	°C
V_O	Output voltage	0.6		9	V
I_{O1}	DC output current	0		3.5	A
I_{O2}	DC output current	0		2.5	A

8.4 Thermal Information

THERMAL METRIC (1)		TPS65283, TPS65283-1	UNIT
		RGE (24 PINS)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	14.5	
ψ_{JT}	Junction-to-top characterization parameter	0.7	
ψ_{JB}	Junction-to-board characterization parameter	14.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

T_J = 25°C, V_{IN1} = V_{IN2} = 12 V, f_{SW} = 500 kHz, R_{PG1} = R_{PG2} = $R_{nFAULTx}$ = 100 kΩ, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{IN}	Input voltage range		4.5		18	V
IDD_{SDN}	Shutdown supply current	V_{SW_EN} = V_{EN1} = V_{EN2} = 0		5.5	10	µA
IDD_{Q_NSW}	None switching quiescent current	EN1 = EN2 = high, V_{FB1} = V_{FB2} = 1 V, With buck1 and buck2 not switching		0.5		mA
UVLO	Input voltage undervoltage lockout (UVLO)	V_{IN1} rising	4	4.25	4.5	V
		V_{IN1} falling	3.5	3.75	4	V
		Hysteresis		500		mV
V_{7V}	Internal biasing supply	V_{V7V} load current = 0 A, V_{IN1} = 12 V	6.05	6.3	6.49	V
I_{OCP_V7V}	Current limit of V7V LDO			180		mA
OSCILLATOR						
f_{SW}	Switching frequency	ROSC = 100 kΩ	400	500	600	kHz
T_{SYNC_w}	Clock sync minimum pulse width		80			ns
V_{SYNC_HI}	Clock sync high threshold				2	V
V_{SYNC_LO}	Clock sync low threshold		0.4			V
V_{SYNC_D}	Clock falling edge to LX rising edge delay				120	ns
F_{SYNC}	Clock sync frequency range		200		2000	kHz
BUCK1/BUCK2 CONVERTER						
V_{FB}	Feedback voltage	V_{COMP1} = V_{COMP2} = 1.2 V, T_J = 25°C	0.594	0.6	0.606	V
		V_{COMP1} = V_{COMP2} = 1.2 V, T_J = –40°C to 125°C	0.588	0.6	0.612	V
G_{m_EA}	Error amplifier transconductance	–2 µA < ICOMPX < 2 µA		300		µS
G_{m_SRC}	COMP1/COMP2 voltage to inductor current Gm(1)	I_{LX1} = I_{LX2} = 0.5 A		7.4		A/V
V_{ENXH}	EN1, EN2 high level input voltage			1.2	1.26	V
V_{ENXL}	EN1, EN2 low-level input voltage		1.1	1.15		V
I_{ENX}	EN1, EN2 pullup current	V_{EN1} = V_{EN2} = 1 V		3.6		µA
I_{ENX}	EN1, EN2 pullup current	V_{EN1} = V_{EN2} = 1.5 V		6.6		µA
I_{ENhys}	I_{EN1} / I_{EN2} hysteresis current			3		µA
T_{ON_MIN}	Minimum on time	T_J = 25°C		80	100	ns
		T_J = –40°C to 125°C			120	
T_{SS_INT}	Internal soft-start time			2.4		ms
I_{LIMIT1}	Buck1 peak inductor current limit		4.25	5	5.75	A
$I_{LIMITS1}$	Buck1 low-side sink current limit			1.7		A
I_{LIMIT2}	Buck2 peak inductor current limit		3.2	3.75	4.3	A
$I_{LIMITS2}$	Buck2 low side sink current limit			1.3		A
Rdson1_HS	High-side FET on-resistance in Buck1	V7V = 6.25 V		100		mΩ
Rdson1_LS	Low-side FET on-resistance in buck1	V7V = 6.25 V		65		mΩ
Rdson2_HS	High-side FET on-resistance in Buck2	V7V = 6.25 V		140		mΩ
Rdson2_LS	Low-side FET on-resistance in buck2	V7V = 6.25 V		95		mΩ
T_{HICCUP_WAIT}	Hiccup wait time			4		ms
T_{HICCUP_RE}	Hiccup time before restart			64		ms
POWER GOOD						
V_{th_PG}	Feedback voltage threshold	V_{FB1} / V_{FB2} UV falling		92.5%		
		V_{FB1} / V_{FB2} UV rising		95%		
		V_{FB1} / V_{FB2} OV rising		107.5%		
		V_{FB1} / V_{FB2} OV falling		105%		
$T_{DEGLITCH(PGF)}$	PG1/PG2 deglitch time (falling edge)			1		ms
$T_{DEGLITCH(PGR)}$	PG1/PG2 deglitch time (rising edge)			2		ms
I_{PG}	Power Good pin leakage	V_{FB1} = V_{FB2} = 0.6 V			1	µA
V_{LOW_PG}	PG1/PG2 pin low voltage	Force FB_1 = FB_2 = 0.5 V, sink 1 mA to PG1/PG2 pin			0.4	V

(1) Specified by design.

Electrical Characteristics (continued)

T_J = 25°C, V_{IN1} = V_{IN2} = 12 V, f_{SW} = 500 kHz, R_{PG1} = R_{PG2} = $R_{nFAULTx}$ = 100 kΩ, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER DISTRIBUTION SWITCH						
V_{SWIN}	Power switch input voltage range		2.4		6	V
IDD_{QH}	Supply current, device enabled	No load on SW_OUT, RSET = 20 kΩ		140		µA
V_{UVLO_SW}	Power switch input undervoltage lockout	V_{SWIN} rising	2.15	2.25	2.35	V
		V_{SWIN} falling	2.05	2.15	2.25	V
		Hysteresis		100		mV
R_{DSON_SW}	Power switch NMOS on-resistance	RGE package, V_{SWIN} = 5 V, I_{OUT} = 0.5 A, T_J = 25°C, including bond wire resistance		60		mΩ
		RGE package, V_{SWIN} = 2.5 V, I_{OUT} = 0.5 A, T_J = 25°C, including bond wire resistance		60		mΩ
t_{D_on}	Turn-on delay time	V_{SWIN} = 5 V, C_L= 10 µF, R_L= 100 Ω		1.1		ms
t_{D_off}	Turn-off delay time	(See Figure 1)		1.2		ms
t_r	Output rise time			0.65		ms
t_f	Output fall time			1.54		ms
I_{OS}	Current limit threshold (maximum DC current delivered to load) and short circuit current, OUT connect to ground	R_{SET} = 14.3 kΩ	1.575	1.75	1.925	A
		R_{SET} = 20 kΩ	1.125	1.25	1.375	
		R_{SET} = 50 kΩ	0.4	0.5	0.6	
		R_{SET} = 80.6 kΩ, T_J = 0°C to 90°C	0.15	0.325	0.5	
$T_{DEGLITCH(OCP)}$	Switch overcurrent fault deglitch	Fault assertion or deassertion due to overcurrent condition	6	8	10	ms
V_{L_nFAULT}	nFAULT pin output low voltage	I_{nFAULT} = 1 mA		150	300	mV
V_{ENSWH}	SW_EN high-level input voltage		2			V
V_{ENSWL}	SW_EN low-level input voltage				0.4	V
R_{DIS}	Discharge resistance(2)	V_{SW_IN} = 5 V, V_{SW_EN} = 0 V		100		Ω
THERMAL SHUTDOWN						
T_{TRIP_BUCK}	Thermal protection trip point	Temperature rising		160		°C
T_{HYST_BUCK}		Hysteresis		20		
T_{TRIP_SW}	Power switch thermal protection trip point Power switch in overcurrent condition	Temperature rise		145		°C
T_{HYST_SW}		Hysteresis		20		

(2) The discharge function is active when the device is disabled (when enable is deasserted). The discharge function offers a resistive discharge path for the external storage capacitor.

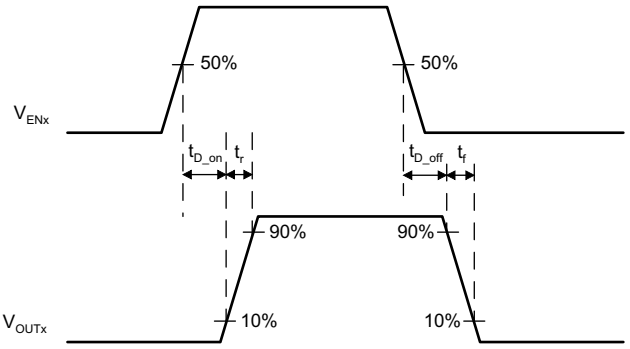


Figure 1. Power Switches Test Circuit and Voltage Waveforms

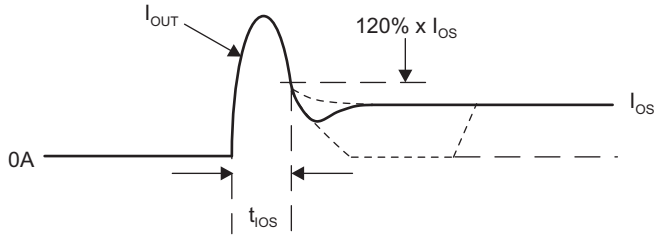


Figure 2. Response Time to Short Circuit Waveform

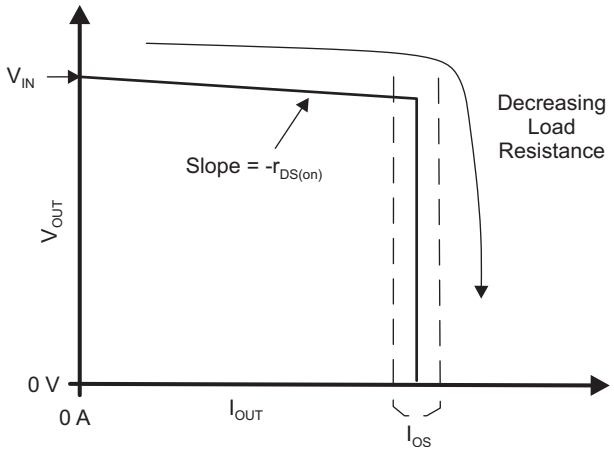


Figure 3. Output Voltage vs Current Limit Threshold

8.6 Typical Characteristics

T_J = 25°C, Vin = 12 V, Vout1 = 1.2 V, Vout2 = 5 V, f_{SW} = 500 kHz, $R_{nFAULT1}$ = $R_{nFAULT2}$ = 100 kΩ (unless otherwise noted)

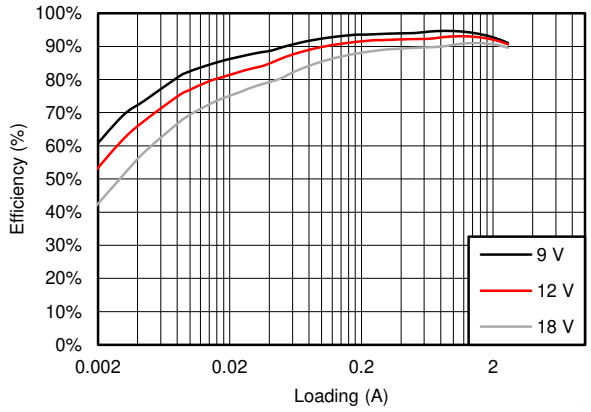


Figure 4. Buck Efficiency (PSM) at Vout1 = 1.2 V

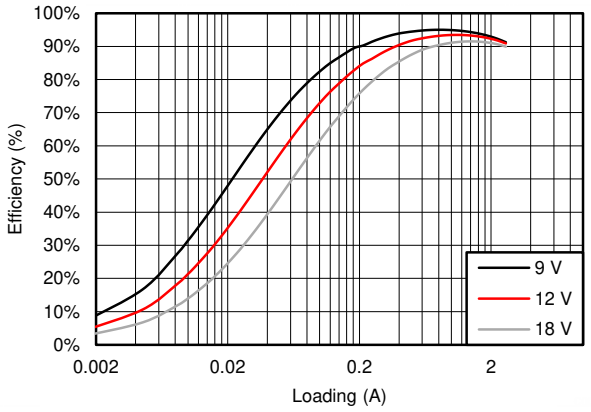


Figure 5. Buck Efficiency (PWM) at Vout1 = 1.2 V

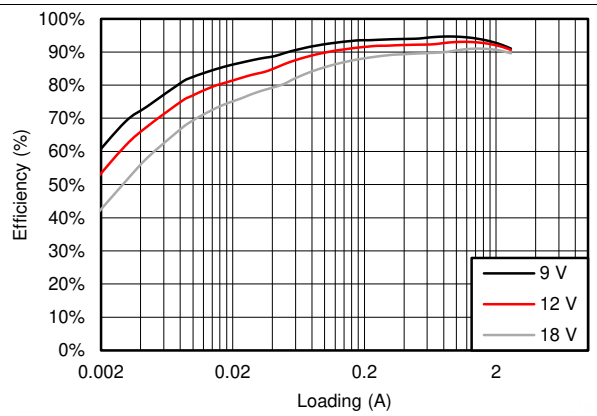


Figure 6. Buck Efficiency (PSM) at Vout2 = 5 V

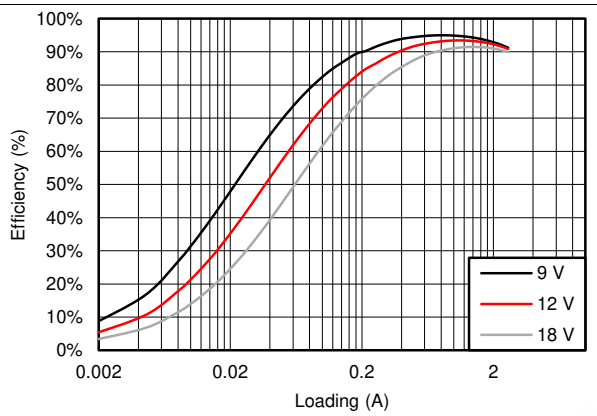


Figure 7. Buck Efficiency (PWM) at Vout2 = 5 V

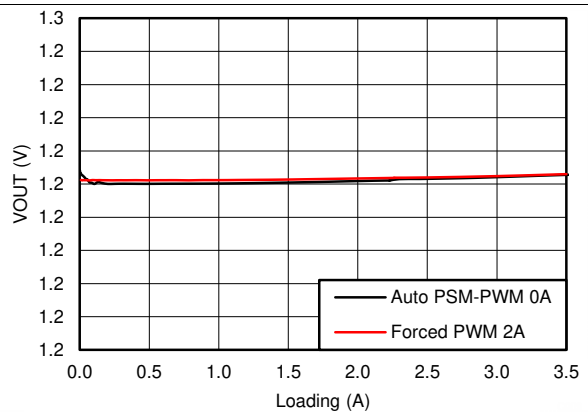


Figure 8. Buck Line Regulation at Vout1 = 1.2 V

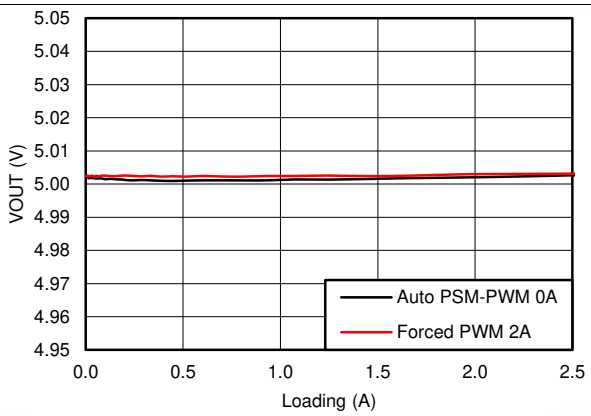


Figure 9. Buck Line Regulation at Vout2 = 5 V

Typical Characteristics (continued)

T_J = 25°C, Vin = 12 V, Vout1 = 1.2 V, Vout2 = 5 V, f_{SW} = 500 kHz, $R_{nFAULT1}$ = $R_{nFAULT2}$ = 100 kΩ (unless otherwise noted)

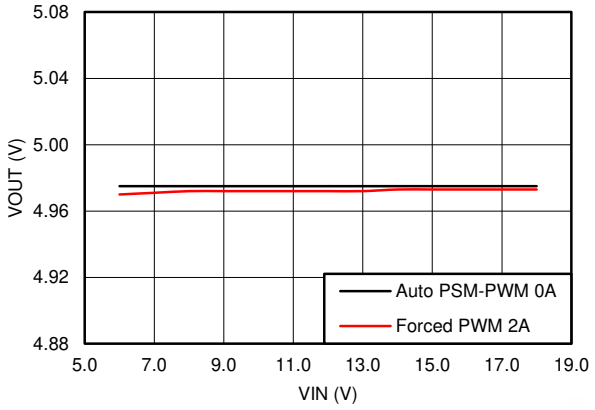


Figure 10. Buck Load Regulation at Vout1 = 1.2 V

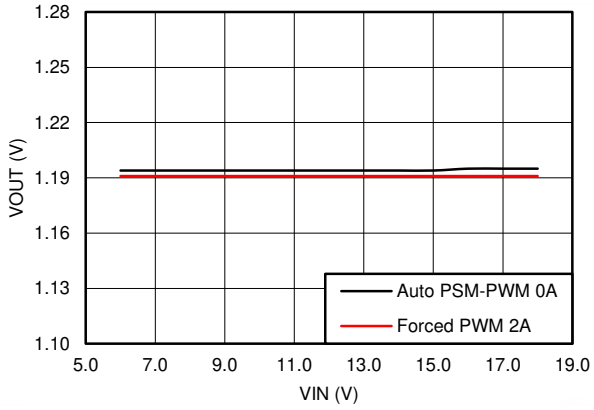


Figure 11. Buck Load Regulation at Vout2 = 5 V

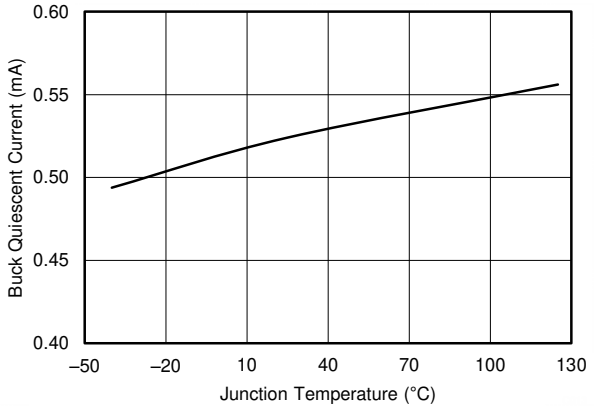


Figure 12. I_{IN} (Without Switching) vs Temperature

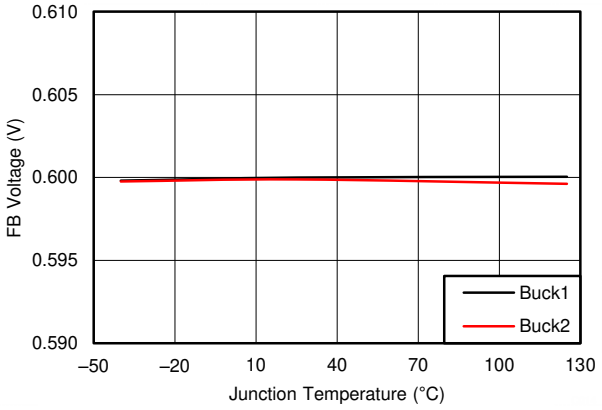


Figure 13. Reference Voltage vs Temperature

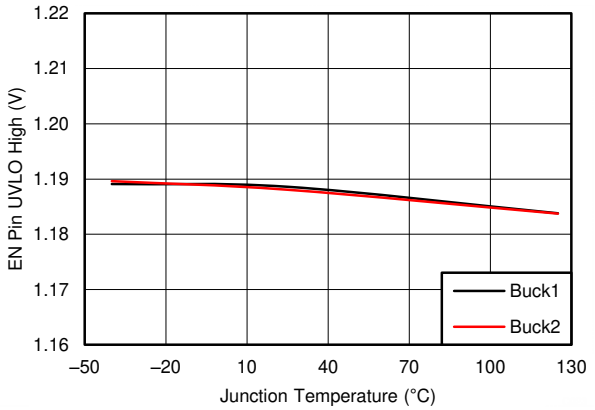


Figure 14. EN UVLO Start Up vs Temperature

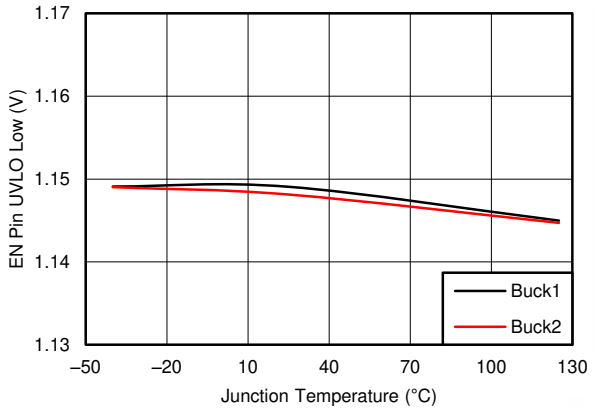


Figure 15. EN UVLO Shut Down vs Temperature

Typical Characteristics (continued)

T_J = 25°C, Vin = 12 V, Vout1 = 1.2 V, Vout2 = 5 V, f_{SW} = 500 kHz, $R_{nFAULT1}$ = $R_{nFAULT2}$ = 100 kΩ (unless otherwise noted)

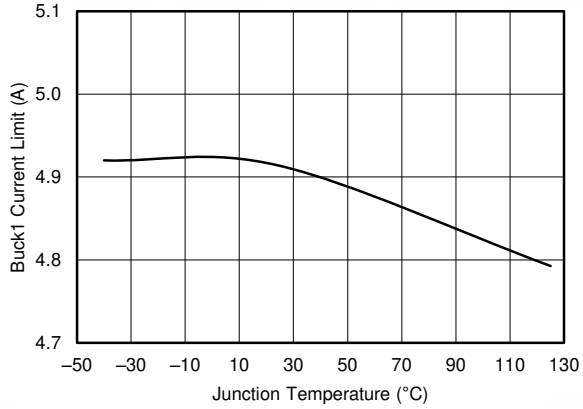


Figure 16. Buck1 Current Limit vs Temperature

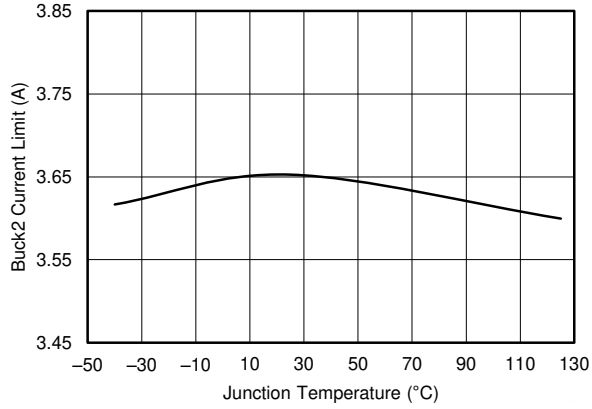


Figure 17. Buck2 Current Limit vs Temperature

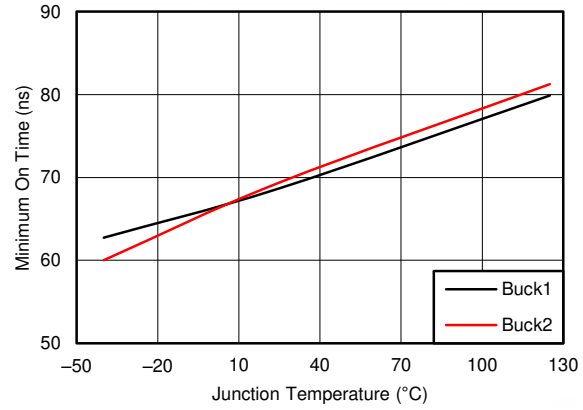


Figure 18. Buck Minimum On Time vs Temperature

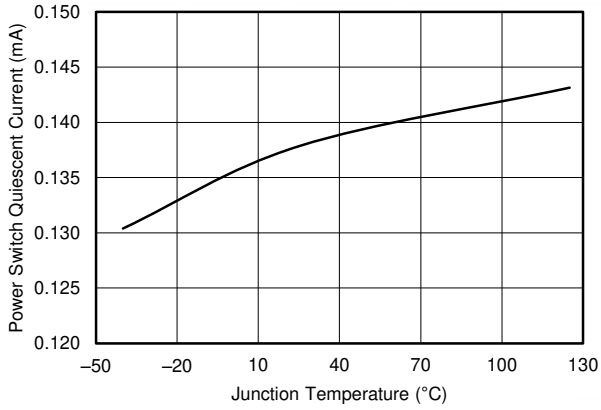


Figure 19. Supply Current (Switch Enabled) vs Temperature

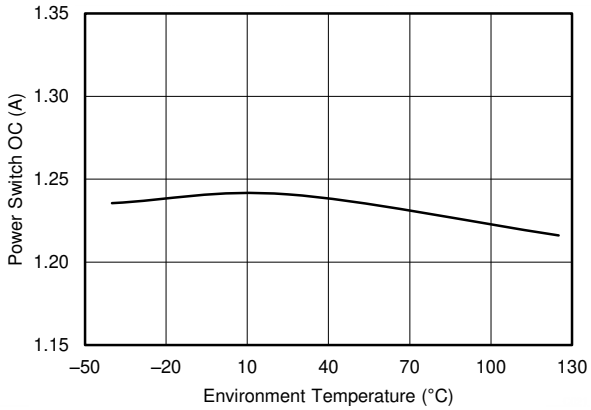


Figure 20. Switch Current Limit vs Temperature (Rset = 20 kΩ)

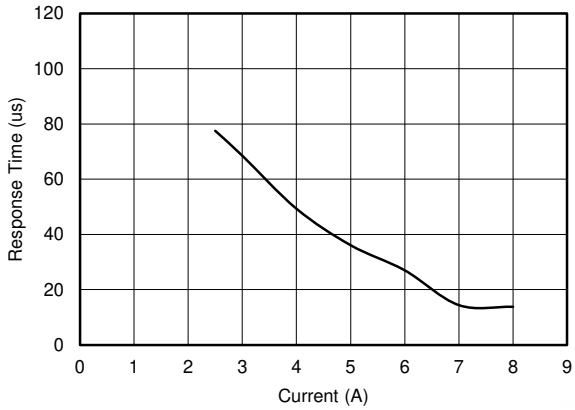


Figure 21. Response Time vs SW_OUT Current

9 Detailed Description

9.1 Overview

TPS65283, TPS65283-1 PMIC integrates dual synchronous step-down converter with regulated 0.6-V ±1% feedback reference voltage, 4.5- to 18-V Vin, 3.5-A/2.5-A output current, which is optimized for small designs through high efficiency and integrating the high-side and low-side MOSFETs. The device also incorporates one N-channel MOSFET power switches for power distribution systems. This device provides a total power distribution solution, where precision current limiting and fast protection response are required.

The TPS65283, TPS65283-1 implements a constant frequency, peak current mode control that simplifies external loop compensation. The wide switching frequency of 250 kHz to 2 MHz allows optimizing system efficiency and filtering size. The switching frequency can be adjusted with an external resistor connecting between ROSC pin and ground. The switch clock of buck1 is 180° out-of-phase operation from the clock of buck2 channel to reduce input current ripple, input capacitor size, and power supply induced noise.

The TPS65283, TPS65283-1 has been designed for safe monotonic start-up into pre-biased loads. The default start-up is when VIN is typically 4.5 V. The ENx pin has an internal pullup current source that can be used to adjust the input voltage UVLO with two external resistors. In addition, the ENx pin can be floating for automatically starting up the converters with the internal pullup current.

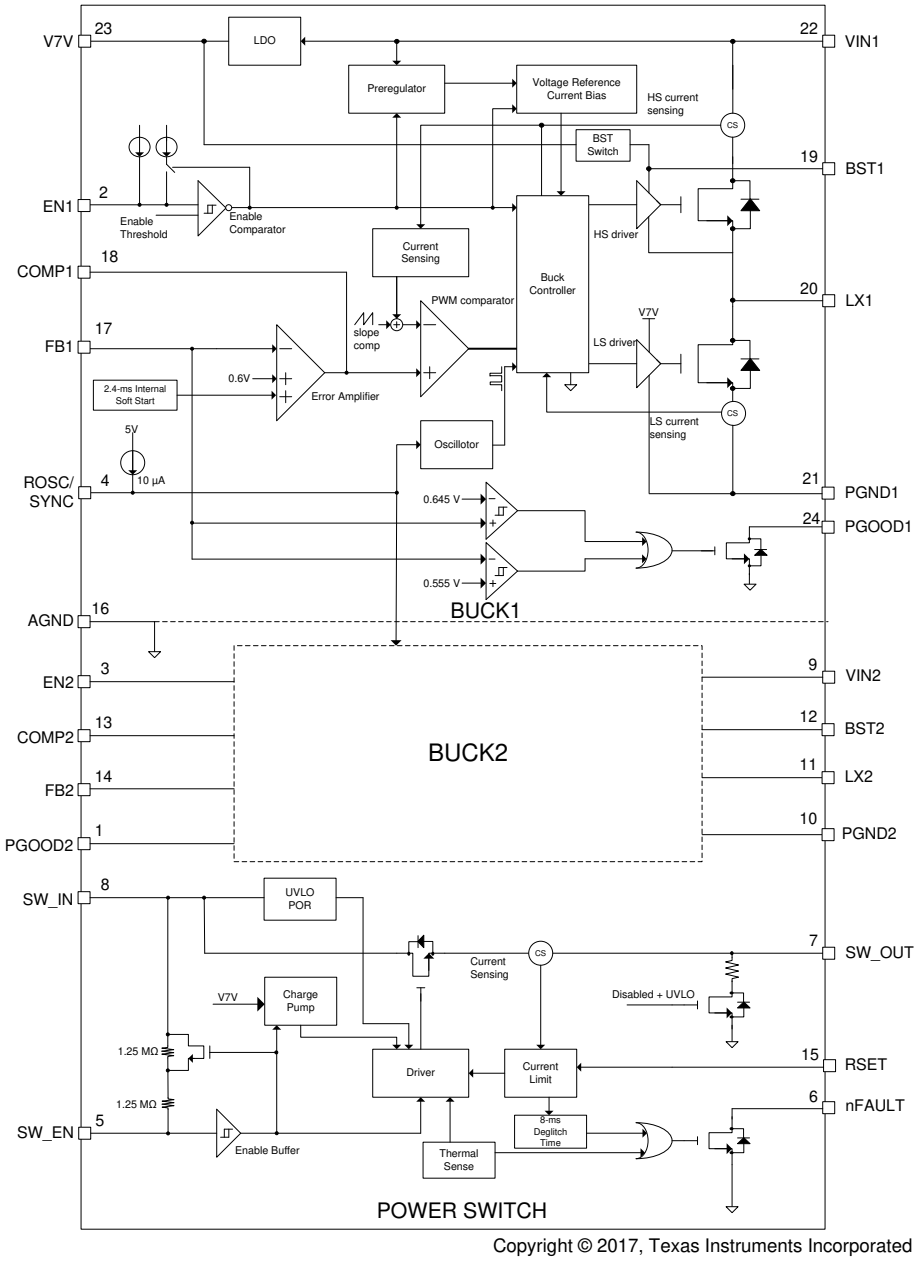
The TPS65283, TPS65283-1 reduces the external component count by integrating the bootstrap circuit. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BST and LX pins. A UVLO circuit monitors the bootstrap capacitor voltage VBST-VLX in each buck. When VBST-VLX voltage drops to the threshold, LX pin to be pulled low to recharge the boot capacitor. The TPS65283, TPS65283-1 can operate at 100% duty cycle as long as the boot capacitor voltage is higher than the preset BOOT-LX UVLO threshold, which is typically 2.1 V.

The TPS65283, TPS65283-1 features PGOOD pin to supervise output voltages of buck converter. The TPS65283, TPS65283-1 has power good comparators with hysteresis, which monitor the output voltages through internal feedback voltages. When the buck is in regulation range and power sequence is done, PGOOD is asserted to high.

The TPS65283, TPS65283-1 is protected from overload and thermal fault conditions. The converter minimizes excessive output overvoltage transients by taking advantage of the power good comparator. When the overvoltage comparator is activated, the high-side MOSFET is turned off and prevented from turning on until the internal feedback voltage is lower than 107.5% of the 0.6-V reference voltage. The TPS65283, TPS65283-1 implements both high-side MOSFET overload protection and bidirectional low-side MOSFET overload protections to avoid inductor current runaway. If the overcurrent condition has lasted for more than the hiccup wait time (4 ms), the converter shuts down and restarts after the hiccup time (64 ms). The TPS65283, TPS65283-1 shuts down if the junction temperature is higher than the thermal shutdown trip point. When the junction temperature drops 20°C typically below the thermal shutdown trip point, the TPS65283, TPS65283-1 is restarted under control of the soft-start circuit automatically. In light loading condition, TPS65283-1 automatically operates in PSM to save power.

Power distribution switches of TPS65283, TPS65283-1 use N-channel MOSFET for applications where short circuits or heavy capacitive loads will be encountered and provide a precision current limit protection. Additional device features include overtemperature protection and reverse-voltage protection. The device incorporates an internal charge pump and gate drive circuitry necessary to drive the N-channel MOSFET. The charge pump supplies power to the driver circuit and provide the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltage of power switches as low as 2.4 V and requires little supply current. The driver controls the gate voltage of power switch. The driver incorporates circuitry that controls the rise and fall times of output voltage to limit large current and voltage surges and provides built-in soft-start functionality. TPS65283, TPS65283-1 device limits output current to a safe level when output load exceeds the current limit threshold. The device asserts the nFAULT signal when overs current limit or reverse voltage faulty condition last longer than deglitching time. When the output voltage and current return normally, the device will auto recovery and nFAULT signal will be released.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Power Switch Detailed Description

9.3.1.1 Overcurrent Condition

The TPS65283, TPS65283-1 responds to overcurrent conditions on power switches by limiting the output currents to I_{OCP_SW} level, which is set by external resistor. When the load current is less than the current-limit threshold, the devices are not limiting current. During normal operation, the N-channel MOSFET is fully enhanced, and $V_{SW\_OUT} = V_{SW\_IN} – (I_{SW\_OUT} × R_{dson\_SW})$. The voltage drop across the MOSFET is relatively small compared to V_{SW_IN}, and $V_{SW\_OUT} ≈ V_{SW\_IN}$. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. During current-limit operation, the N-channel MOSFET is no longer fully enhanced and the resistance of the device increases. This allows the device to

Feature Description (continued)

effectively regulate the current to the current-limit threshold. The effect of increasing the resistance of the MOSFET is that the voltage drop across the device is no longer negligible ($V_{SW\_IN} \neq V_{SW\_OUT}$), and V_{SW_OUT} decreases. The amount that V_{SW_OUT} decreases is proportional to the magnitude of the overload condition. The expected V_{SW_OUT} can be calculated by $I_{OCP\_SW} \times R_{LOAD}$, where I_{OCP_SW} is the current-limit threshold and R_{LOAD} is the magnitude of the overload condition.

Table 1 shows three possible overload conditions that can occur.

Table 1. Overload Conditions

CONDITIONS	BEHAVIORS
Short circuit or partial short circuit present when the device is powered up or enabled	The output voltage is held near zero potential with respect to ground and the TPS65283, TPS65283-1 ramps output current to I_{OCP_SW}. The device limits the current to IOS until the overload condition is removed or the internal deglitch time (8 ms typical) is reached and the device is turned off. The device auto recovers when the overcurrent status is removed.
Gradually increasing load (<100 A/s) from normal operating current to I_{OCP_SW}	The current rises until current limit. After the threshold has been reached, the device switches into its current limiting at I_{OCP_SW}. The device limits the current to IOS until the overload condition is removed or the internal deglitch time (8 ms typical) is reached and the device is turned off. The device auto recovers when the overcurrent status is removed.
Short circuit, partial short circuit or fast transient overload occurs while the device is enabled and powered on	The device responds to the overcurrent condition within time T_{IOS} (see Figure 3).The current sensing amplifier is overdriven during this time, and needs time for loop response. After T_{IOS} has passed, the current sensing amplifier recovers and limits the current to I_{OCP_SW}. The device limits the current to IOS until the overload condition is removed or the internal deglitch time (8 ms typical) is reached and the device is turned off. The device auto recovers when the overcurrent status is removed.

9.3.1.2 Reverse Current and Voltage Protection

The power switch in TPS65283, TPS65283-1 incorporates one N-channel power MOSFETs for lower resistance and the bulk of the MOSFET is connected to ground to prevent the reverse current flowing back the input through body diode of MOSFET when power switch is off.

When power switch is enabled, the reverse-voltage protection feature turns off the N-channel MOSFET whenever the output voltage exceeds the input voltage by 55 mV (typical) for 4-ms (typical). This prevents damage to devices on the input side of the TPS65283, TPS65283-1 by preventing significant current from sinking into the input capacitance of power switch or buck output capacitance. The TPS65283, TPS65283-1 device keeps the power switch turned off even if the reverse-voltage condition is removed and does not allow the N-channel MOSFET to turn on until power is cycled or the device enable is toggled. The reverse-voltage comparator also asserts the nFAULT output (active-low) after 4 ms.

9.3.1.3 nFAULT Response

The nFAULT open-drain output is asserted (active low) during an overcurrent, overtemperature, or reverse-voltage condition. The TPS65283, TPS65283-1 asserts the nFAULT signal during a fault condition and remains asserted while the part is latched-off. The nFAULT signal is deasserted when device power is cycled or the enable is toggled, and the device resumes normal operation. The TPS65283, TPS65283-1 is designed to eliminate false nFAULT reporting by using an internal delay "deglitch" circuit for over-current (8 ms typical) and reverse-voltage (4 ms typical) conditions without the need for external circuitry. This ensures that nFAULT is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. Deglitching circuitry delays entering and leaving fault conditions. Overtemperature conditions are not deglitched and assert the FAULT signal immediately.

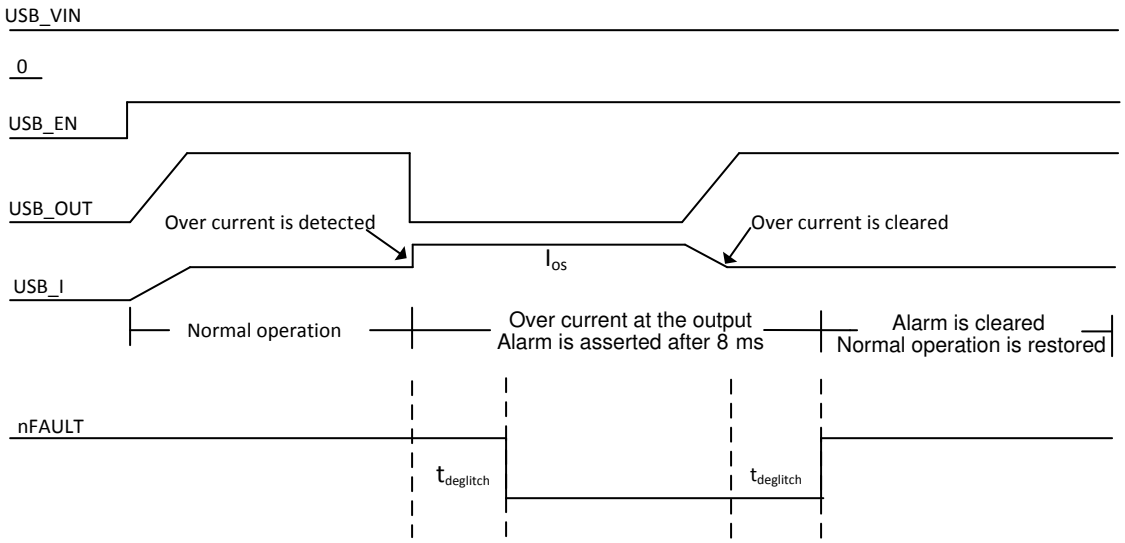


Figure 22. USB Switches Over Current

9.3.1.4 UVLO

The UVLO circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage drop from large current surges.

9.3.1.5 Enable and Output Discharge

The logic enable EN_SW controls the power switch, bias for the charge pump, driver, and other circuits. The supply current from power switch driver is reduced to less than 1 µA when a logic low is present on EN_SW. A logic high input on EN_SW enables the driver, control circuits, and power switch. The enable input is compatible with both TTL and CMOS logic levels.

When enable is deasserted, the discharge function is active. The output capacitor of power switch is discharged through an internal NMOS that has a discharge resistance of 100 Ω. Hence, the output voltage drops down to 0. The time taken for discharge depends on the RC time constant of the resistance and the output capacitor.

9.3.1.6 Power Switch Input and Output Capacitance

Input and output capacitance improves the performance of the device. The actual capacitance should be optimized for the particular application. TI recommends to place the output capacitor in buck converter between SW_IN and AGND as close to the device as possible for local noise decoupling. Additional capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during heavy transient conditions. This is especially important during bench testing when long, inductive cables are used to connect the input of power switches in the evaluation board to the bench power-supply. TI recommends placing a high-value electrolytic capacitor on the output pin when large transient currents are expected on the output.

9.3.1.7 Programming the Current-Limit Threshold

The overcurrent threshold is user programmable through an external resistor. The TPS65283, TPS65283-1 uses an internal regulation loop to provide a regulated voltage on the RLIM pin. The current-limit threshold is proportional to the current sourced out of RSET. The recommended 1% resistor range for RSET is 9.1 kΩ ≤ RLIM ≤ 80.6 kΩ to adjust the current limit of the switch. Many applications require that the minimum current limit is above a certain current level or that the maximum current limit is below a certain current level, so it is important to consider the tolerance of the overcurrent threshold when selecting a value for RLIM. The following equations and Figure 23 can be used to calculate the resulting overcurrent threshold for a given external resistor value (RSET).

Current-Limit Threshold Equations (IOS):

$$ILIMIT = 37.793(RSET)^{-1.149} \quad (1)$$

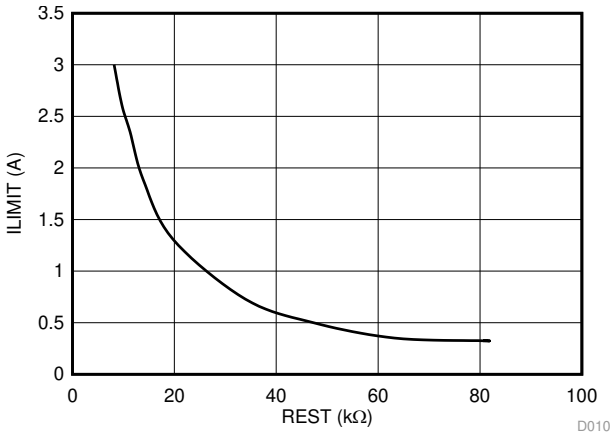


Figure 23. Current-Limit Threshold vs RLIM

9.3.2 Buck DC-DC Converter Detailed Description

9.3.2.1 Output Voltage

The TPS65283, TPS65283-1 regulate output voltage set by a feedback resistor divider to 0.6-V reference voltage. This pin should be directly connected to middle of resistor divider. TI recommends to use 1% tolerance or better divider resistors. Take care to route the FB line away from noise sources, such as the inductor or the LX switching node line. Start with 39 kΩ for the R_1 resistor and use Equation 2 to calculate R_2 and ensure the $R_2 \leq 10$ kΩ.

$$R_2 = R_1 \times \left(\frac{0.6V}{V_{OUT} - 0.6V} \right) \quad (2)$$

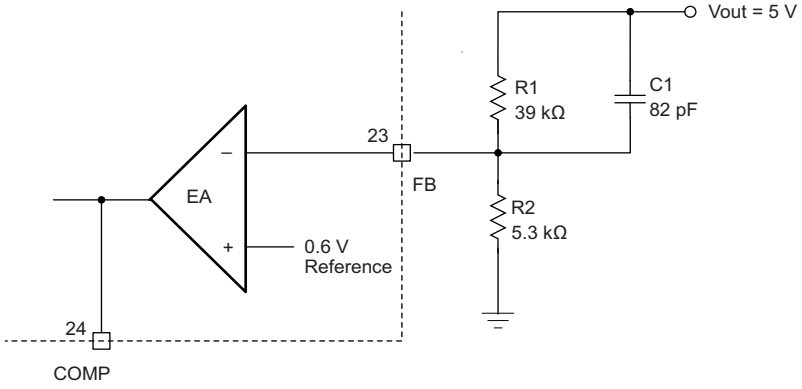


Figure 24. Buck Internal Feedback Resistor Divider

9.3.2.2 Adjustable Switching Frequency

The ROSC pin can be used to set the switching frequency by connecting a resistor to GND. The switching frequency of the device is adjustable from 200 kHz to 2 MHz.

To determine the ROSC resistance for a given switching frequency, use Equation 3 or the curve in Figure 25. To reduce the solution size, set the switching frequency as high as possible, but consider tradeoffs of the supply efficiency and minimum controllable on-time.

$$f_{osc}\,(\text{kHz}) = 47863 \times R\,(\text{k}\Omega)^{-0.988} \quad (3)$$

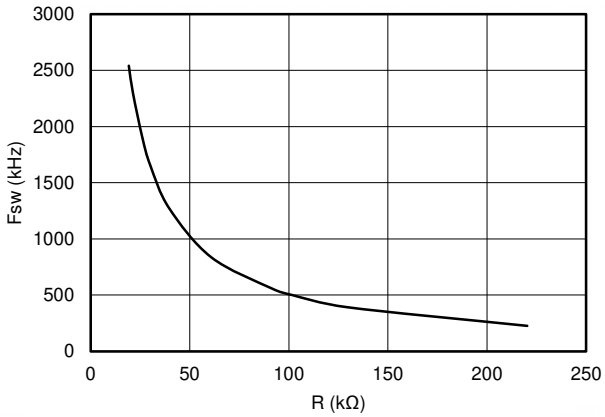


Figure 25. ROSC vs Switching Frequency

9.3.2.3 Synchronization

The user can implement an internal phase locked loop (PLL) to allow synchronization between 200 kHz to 2 MHz, and to easily switch from resistor mode to synchronization mode. To implement the synchronization feature, connect a square wave clock signal to the ROSC pin with a duty cycle between 20% and 80%. The clock signal amplitude must transition lower than 0.4 V and higher than 2 V. The start of the switching cycle is synchronized to the falling edge of ROSC pin.

In applications where both resistor mode and synchronization mode are needed, configure the device as shown in Figure 26. Before the external clock is present, the device works in resistor mode and the switching frequency is set by ROSC resistor. When the external clock is present, the synchronization mode overrides the resistor mode.

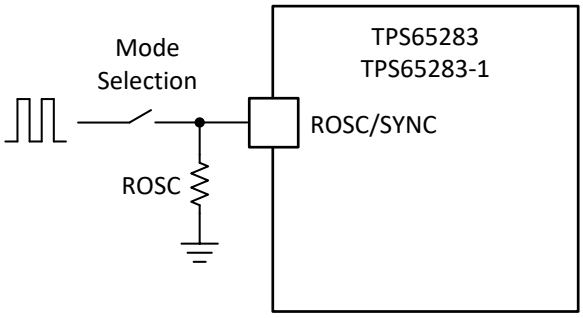


Figure 26. Works With Resistor Mode and Synchronization Mode

9.3.2.4 Error Amplifier

The device uses a transconductance error amplifier. The error amplifier compares the FB pin voltage to the lower of the SS pin voltage or the internal 0.6-V voltage reference. The transconductance of the error amplifier is 300 µA/V during normal operation. The frequency compensation network is connected between the COMP pin and ground.

9.3.2.5 Slope Compensation

To prevent subharmonic oscillations when the device operates at duty cycles greater than 50%, the device adds built-in slope compensation, which is a compensating ramp to the switch current signal.

9.3.2.6 Enable and Adjusting UVLO

The ENx pin provides electrical on and off control of the device. When the ENx pin voltage exceeds the threshold voltage, the device starts operation. If the ENx pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low Iq state. The ENx pin has an internal pullup current source, allowing the user to float the ENx pin for enabling the device. If an application requires controlling the ENx pin, use open-drain or open-collector output logic to interface with the pin. The device implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 500 mV. If an application requires either a higher UVLO threshold on the VIN pin, or a secondary UVLO on the PVIN, in split rail applications, then the user can configure the ENx pin as shown in Figure 27. When using the external UVLO function, TI recommends to set the hysteresis to be greater than 500 mV.

The ENx pin has a small pullup current Ip which sets the default state of the pin to enable when no external components are connected. The pullup current is also used to control the voltage hysteresis for the UVLO function since it increases by Ih once the ENx pin crosses the enable threshold. The UVLO thresholds can be calculated using Equation 4 and Equation 5.

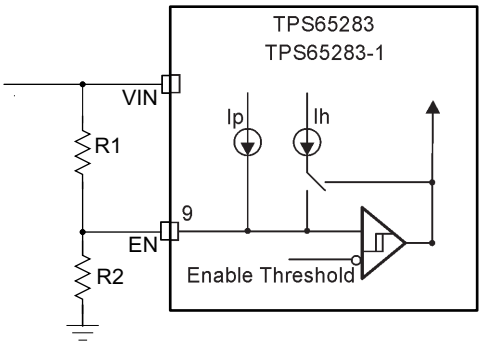


Figure 27. Adjustable VIN Undervoltage Lockout

$$R_1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_P\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \quad (4)$$

$$R_2 = \frac{R_1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R_1\left(I_h + I_p\right)} \quad (5)$$

where

- I_h = 3 µA
- I_p = 3.6 µA
- $V_{ENRISING}$ = 1.2 V
- $V_{ENFALLING}$ = 1.15 V

9.3.2.7 Internal V7V Regulator

The TPS65283, TPS65283-1 features an internal P-channel low dropout linear regulator (LDO) that supply power at the V7V pin from VIN supply. V7V powers the gate drivers and much of the TPS65283's, TPS65283-1's internal circuitry. The LDO regulates V7V to 6.3 V of overdrive voltage on power MOSFET for the best efficiency performance. The LDO can supply a peak current of 50 mA and must be bypassed to ground with a minimum of 1-µF ceramic capacitor. TI highly recommends that the capacitor placed directly adjacent to the V7V and PGND pins supply the high transient currents required by the MOSFET gate drivers.

9.3.2.8 Short Circuit Protection

The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET.

9.3.2.8.1 High-Side MOSFET Overcurrent Protection

The device implements current mode control, which uses the COMP pin voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle by cycle basis. Each cycle the switch current and the current reference generated by the COMP pin voltage are compared, when the peak switch current intersects the current reference the high-side switch is turned off.

9.3.2.8.2 Low-Side MOSFET Overcurrent Protection

While the low-side MOSFET is turned on, its conduction current is monitored by the internal circuitry. During normal operation, the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally-set low-side sourcing current limit. If the low-side sourcing current is exceeded, the high-side MOSFET is not turned on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET is turned on again when the low-side current is below the low-side sourcing current limit at the start of a cycle.

The low-side MOSFET may also sink current from the load. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario, both MOSFETs are off until the start of the next cycle.

Furthermore, if an output overload condition (as measured by the COMP pin voltage) has lasted for more than the hiccup wait time, which is programmed for 4 ms, the device shuts down and restarts after the hiccup time of 64 ms. The hiccup mode helps to reduce the device power dissipation under severe overcurrent conditions

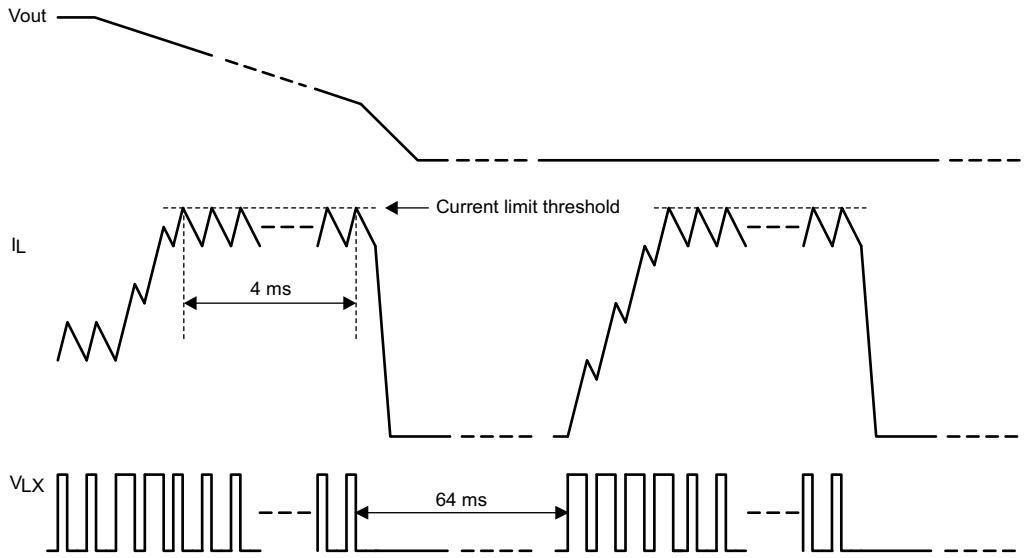


Figure 28. DC-DC Overcurrent Protection

9.3.2.9 Bootstrap Voltage (BST) and Low Dropout Operation

The device has an integrated boot regulator and requires a small ceramic capacitor between the BST and LX pins to provide the gate drive voltage for the high-side MOSFET. The boot capacitor is charged when the BST pin voltage is less than VIN and BST-LX voltage is below regulation. The value of this ceramic capacitor should be 47 nF. TI recommends a ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher because of the stable characteristics over temperature and voltage. To improve dropout, the device is designed to operate at 100% duty cycle as long as the BST to LX pin voltage is greater than the BST-LX UVLO threshold, which is typically 2.1 V. When the voltage between BST and LX drops below the BST-LX UVLO threshold, the high-side MOSFET is turned off and the low-side MOSFET is turned on allowing the boot capacitor to be recharged.

9.3.2.10 Output Overvoltage Protection (OVP)

The device incorporates an output OVP circuit to minimize output voltage overshoot. For example, when the power supply output is overloaded, the error amplifier compares the actual output voltage to the internal reference voltage. If the FB pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier demands maximum output current. After the condition is removed, the regulator output rises and the error amplifier output transitions to the steady state voltage. In some applications with small output capacitance, the power supply output voltage can respond faster than the error amplifier. This leads to the possibility of an output overshoot. The OVP feature minimizes the overshoot by comparing the FB pin voltage to the OVP threshold. If the FB pin voltage is greater than the OVP threshold, the high-side MOSFET is turned off, preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVP threshold, the high-side MOSFET is allowed to turn on at the next clock cycle.

9.3.2.11 Power Good

The PGOOD pin is an open-drain output. The PGOOD pin is pulled low when buck converter is pulled below 92.5% or over 107.5% of the nominal output voltage. The PGOOD is pulled up when the buck converters' outputs are more than 95% and lower than 105% of its nominal output voltage. The default reset time is 2 ms. The polarity of the PGOOD is active high.

9.3.2.12 Power-Up Sequencing

The TPS65283, TPS65283-1 has a dedicated enable pin for each converter. The converter enable pins are biased by a current source that allows for easy sequencing by the addition of an external capacitor. Disabling the converter with an active pulldown transistor on the ENx pin allows for predictable power-down timing operation. Figure 29 shows the timing diagram of a typical buck power-up sequence with connecting a capacitor at ENx pin.

A typical 1.4-µA current is charging ENx pin from input supply. When ENx pin voltage rise to typical 0.4 V, the internal V7V LDO turns on. A 3.6-µA pullup current is sourcing ENx. After ENx pin voltage reaches to ENx enabling threshold, 3-µA hysteresis current sources to the pin to improve noise sensitivity. The internal soft-start comparator compares internal SS voltage to 0.6 V, When internal SS voltage ramps up to 0.6 V, PGOODx monitor is enabled. After PGOODx deglitch time, and if output voltages are in the regulation, PGOODx is asserted.

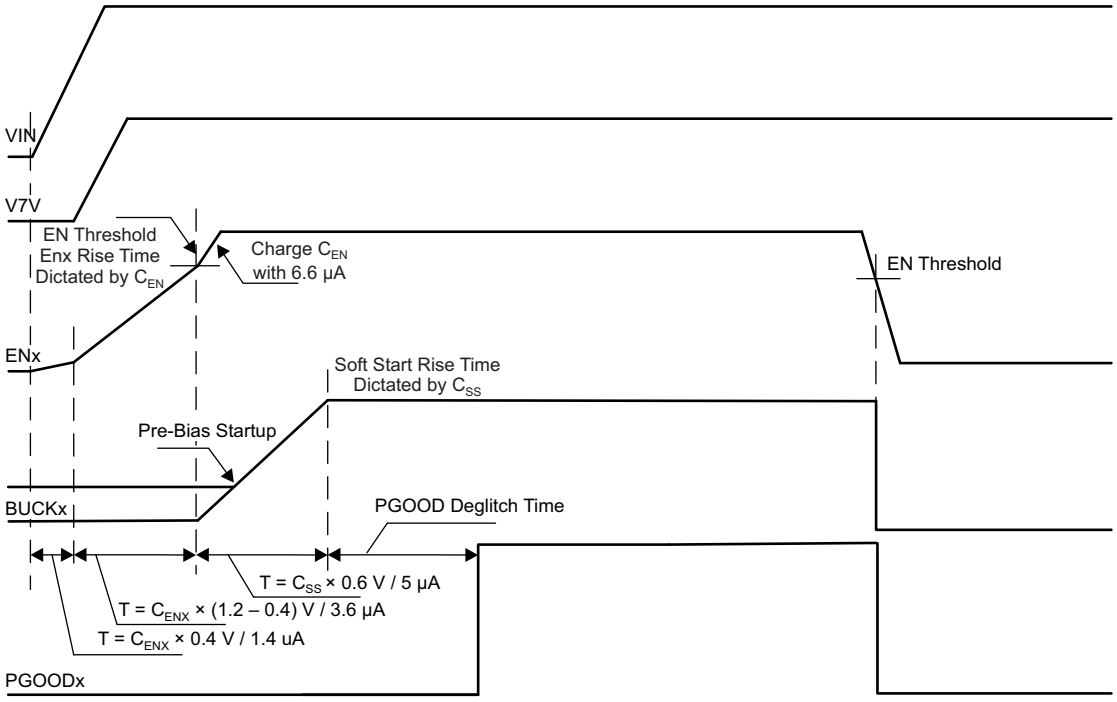


Figure 29. Start-Up Power Sequence

9.3.2.13 Thermal Performance

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 160°C. The thermal shutdown forces the buck converter to stop switching when the junction temperature exceeds thermal trip threshold. After the die temperature decreases below 140°C, the device reinitiates the power-up sequence. The thermal shutdown hysteresis is 20°C. When USB is over-current, the internal thermal shut down of power switch will be changed to 145°C to avoid influencing the normal operation of buck converters.

9.4 Device Functional Modes

9.4.1 Operation With V_{IN} < 4.5 V (Minimum VIN)

The devices operate with input voltages above 4.5 V. The maximum UVLO voltage is 4.5 V and operates at input voltages above 4.5 V. The typical UVLO voltage is 4 V, and the devices may operate at input voltages above that point. The devices also may operate at lower input voltage; the minimum UVLO voltage is not specified. At input voltages below the actual UVLO voltage, the devices do not operate.

9.4.2 Operation With EN Control

The enable rising edge threshold voltage is 1.2 V typical and 1.26 V maximum. With EN held below that voltage the device is disabled and switching is inhibited. The IC quiescent current is reduced in this state. When input voltage is above the UVLO threshold and the EN voltage is increased above the rising edge threshold, the device becomes active. Switching is enabled, and the slow start sequence is initiated. The TPS65283, TPS65283-1 output voltage ramps up at the internal slow-start time of 2.4 ms.

9.4.3 Operation at Light Loads

The devices are designed to operate in high-efficiency PSM under light load conditions. Pulse skipping is initiated when the switch current falls to 0 A. During pulse skipping, the low-side FET is turned off when the switch current falls to 0 A. The switching node (LX) waveform takes on the characteristics of DCM operation and the apparent switching frequency decreases.

10 Application and Implementation

10.1 Application Information

The devices are step-down DC-DC converters. They are typically used to convert a higher dc voltage to a lower dc voltage with a maximum available output current of 3.5/2.5 A. The following design procedure can be used to select component values for the TPS65283 and TPS65283-1. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

10.2 Typical Application

The application schematic in Figure 30 was developed to meet the previous requirements. This circuit is available as the TPS65283, TPS65283-1 evaluation module (EVM). The sections provides the design procedure.

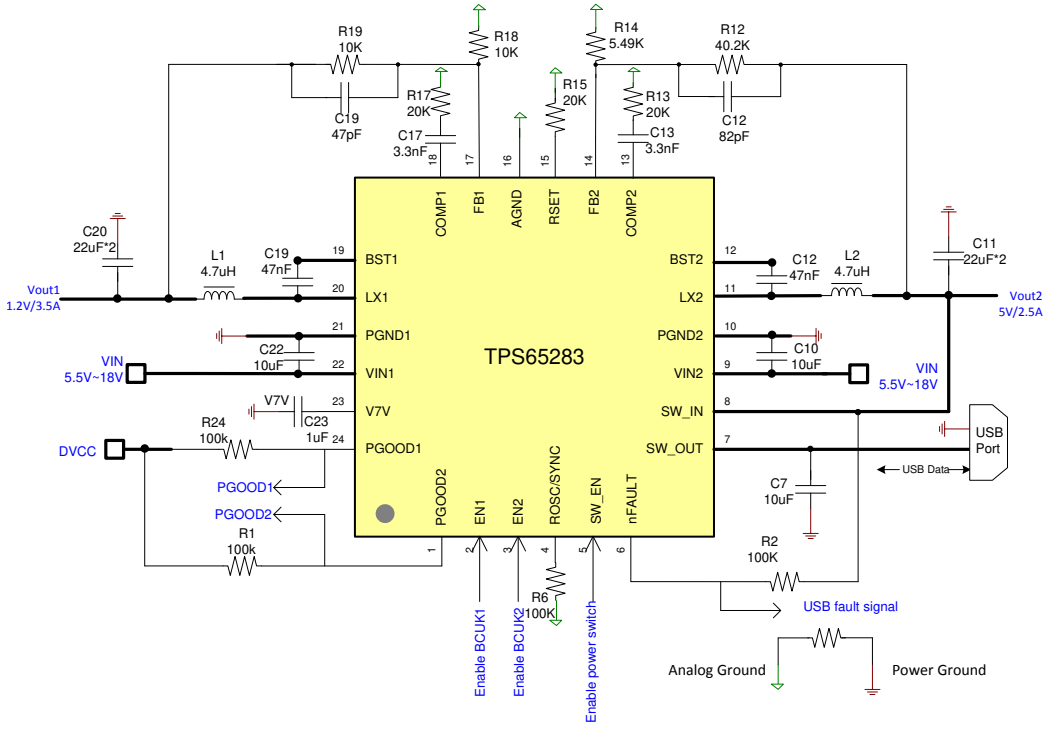


Figure 30. Typical Application Schematic

Table 2. Related Parts

PART NUMBER	DESCRIPTION	COMMENTS
TPS65280	4.5 to 18 V Vin, 4 A, synchronous buck converter with dual power switch	Fixed 5V Vout, 0.3 ≤ Fsw ≤ 1.4 MHz, Power switch: 2.5 V ≤ Vsw_in ≤ 6 V, fixed 1.2-A current limit
TPS65281, TPS65281-1	4.5 to 18 V Vin, 3 A, synchronous buck converter with a power switch	0.3 ≤ Fsw ≤ 1.4 MHz, Power switch: 2.5 V ≤ Vsw_in ≤ 6 V, adjustable up to 2.7 A current limit
TPS65282	4.5 to 18 V Vin, 4 A, synchronous buck converter with dual power switches	0.3 ≤ Fsw ≤ 1.4 MHz, PSM at light load, Power switch: 2.5 V ≤ Vsw_in ≤ 6 V, adjustable up to 2.7 A current limit
TPS65286	4.5 to 28 V Vin, 6 A, synchronous buck converter with dual power switches	0.3 ≤ Fsw ≤ 2.2 MHz, PSM at light load, Power switch: 2.5 V ≤ Vsw_in ≤ 6 V, adjustable up to 2.7 A current limit

Typical Application (continued)

Table 2. Related Parts (continued)

PART NUMBER	DESCRIPTION	COMMENTS
TPS65287	4.5 to 18 V Vin, 3 A / 2 A / 2 A, triple synchronous buck converter with a power switch and pushbutton control	0.3 ≤ Fsw ≤ 2.2 MHz, PSM at light load, Power switch: 2.5 V ≤ Vsw_in ≤ 6 V, adjustable up to 2.7 A current limit
TPS65288	4.5 to 18 V Vin, 3 A / 2 A / 2 A, triple synchronous buck converter with dual power switch	0.3 ≤ Fsw ≤ 2.2 MHz, PSM at light load, Power switch: 2.5 V ≤ Vsw_in ≤ 6 V, Fixed 1.2 A current limit

10.2.1 Design Requirements

For this design example, use the following as the input parameters.

Table 3. Input Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	4.5 to 18 V
Output voltage	1.2 / 5 V
Transient response, 1.5-A load step	ΔVout = ±5%
Input ripple voltage	400 mV
Output ripple voltage	30 mV
Output current rating	3.5 / 2.5 A
Operating frequency	500 kHz

10.2.2 Detailed Design Procedure

10.2.2.1 Output Voltage Setting

To improve efficiency at light loads, consider using larger value resistors. If the values are too high, the regulator is more sensitive to noise. Table 4 shows the recommended resistor values. Ensure the R_2 ≤ 10 kΩ.

Table 4. Output Resistor Divider Selection

OUTPUT VOLTAGE (V)	R_1 (kΩ)	R_2 (kΩ)
1	6.8	10
1.2	10	10
1.5	15	10
1.8	20	10
2.5	31.6	10
3.3	45.3	10
3.3	22.6	4.99
5	73.2	10
5	36.5	4.99

10.2.2.2 Bootstrap Capacitor Selection

A 47-nF ceramic capacitor must be connected between the BST to LX pin for proper operation. TI recommends to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have 10 V or higher voltage rating.

10.2.2.3 Inductor Selection

The higher operating frequency allows the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of MOSFET gate charge losses. In addition to this basic trade-off, consider the effect of inductor value on ripple current and low current operation. The ripple current depends on the inductor value. The inductor ripple current i_L decreases with higher inductance or higher frequency and increases with higher input voltage V_{IN}. Accepting larger values of i_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses.

To calculate the value of the output inductor, use Equation 6. LIR is a coefficient that represents inductor peak-to-peak ripple to dc load current. LIR is suggested to choose to 0.1 to about 0.3 for most applications.

Actual core loss of inductor is independent of core size for a fixed inductor value, but it is very dependent on inductance value selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses increase. Ferrite designs have very-low core loss and are preferred for high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. It results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate. It is important that the RMS current and saturation current ratings are not exceeding the inductor specification. Calculate the RMS and peak inductor current from Equation 8 and Equation 9.

$$L = \frac{V_{in} - V_{out}}{I_O \times LIR} \times \frac{V_{out}}{V_{in} \times fsw} \tag{6}$$

$$\Delta i_L = \frac{V_{in} - V_{out}}{L} \times \frac{V_{out}}{V_{in} \times fsw} \tag{7}$$

$$i_{Lrms} = \sqrt{I_O^2 + \frac{\left(\frac{V_{out} \times (V_{inmax} - V_{out})}{V_{inmax} \times L \times fsw}\right)^2}{12}} \tag{8}$$

$$I_{Lpeak} = I_O + \frac{\Delta i_L}{2} \tag{9}$$

For this design example, use LIR = 0.3, and inductor is calculated to be 2.1 µH with Vin = 12 V, Vout = 1.2 V, Iout = 3.5 A. Choose 4.7-µH value of standard inductor, the peak-to-peak inductor ripple is about 13.1% of 3.5-A dc load current.

10.2.2.4 Output Capacitor Selection

There are two primary considerations for selecting the value of the output capacitor. The output capacitors are selected to meet load transient and output ripple's requirements. Equation 10 gives the minimum output capacitance to meet the transient specification. For this example, Lo = 4.7 µH, ΔIout = 2 A – 0.0 A = 2 A, and ΔVout = 250 mV (5% of regulated 5 V) for Buck2. Using these numbers gives a minimum capacitance of 15 µF. This design uses a standard 2 × 22-µF ceramic.

$$Co > \frac{\Delta I_{OUT}{}^2 \times L}{V_{out} \times \Delta V_{out}} \tag{10}$$

The selection of C_{OUT} is driven by the effective series resistance (ESR). Equation 11 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where $f$sw is the switching frequency, ΔVout is the maximum allowable output voltage ripple, and ΔiL is the inductor ripple current. In this case, the maximum output voltage ripple is 25 mV (0.5% of regulated 5 V). From Equation 9, the output current ripple is 1.24 A. From Equation 11, the minimum output capacitance meeting the output voltage ripple requirement is 14.5 µF with 3-mΩ ESR resistance.

$$Co > \frac{1}{8 \times fsw} \times \frac{1}{\frac{\Delta V_{out}}{\Delta i_L} - esr} \tag{11}$$

After considering both requirements, for this example, four 22-µF 6.3-V X7R ceramic capacitor with 3 mΩ of ESR are used. Equation 12 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 12 indicates the ESR should be less than 20.2 mΩ. In this case, the ceramic caps' ESR is much smaller than 20.2 mΩ.

$$\frac{Voripple}{Iripple} \leq Resr \tag{12}$$

Factor in additional capacitance deratings for aging, temperature, and dc bias, which increase this minimum value. This example uses a 22-µF 6.3-V X5R ceramic capacitor with 3 mΩ of ESR. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the root mean square (RMS) value of the maximum ripple current. Equation 13 can be used to calculate the RMS ripple current the output capacitor needs to support. For this application, Equation 13 yields 385 mA.

$$Icorms = \frac{Vout \times (Vin\ max\ - Vout)}{\sqrt{12} \times Vin\ max\ \times L1 \times f_{SW}} \tag{13}$$

10.2.2.5 Input Capacitor Selection

TI recommends a minimum 10-µF X7R/X5R ceramic input capacitor to be added between VIN and GND. Connect these capacitors as close as physically possible to the input pins of the converters as they handle the RMS ripple current shown in Equation 14. For this example, Iout = 2 A, Vout = 5 V, minimum Vin_min = 12 V, from Equation 14, the input capacitors must support a ripple current of 998-mA RMS.

$$I_{inrms} = I_{out} \times \sqrt{\frac{V_{out}}{V_{inmin}} \times \frac{(V_{inmin} - V_{out})}{V_{inmin}}} \tag{14}$$

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 15. Using the design example values, Iout_max = 2.5 A, C_{in} = 10 µF, f_{SW} = 500 kHz for buck2, yields an input voltage ripple of 125 mV.

$$\Delta V_{in} = \frac{I_{outmax} \times 0.25}{C_{in} \times f_{sw}} \tag{15}$$

To prevent large voltage transients, use a low-ESR capacitor sized for the maximum RMS current.

10.2.2.6 Minimum Output Voltage

Due to the internal design of the TPS65283, TPS65283-1, there is a minimum output voltage limit for any given input voltage. The output voltage can never be lower than the internal voltage reference of 0.6 V. Above 0.6 V, the output voltage may be limited by the minimum controllable on-time. The minimum output voltage in this case is given by Equation 16.

Voutmin = $Ontime_{min}$ × Fs max (Vin max + Iout min (RDS2 min – RDS1 min))_Iout min (RL + RDS2 min)

where

- Voutmin = Minimum achievable output voltage
- Ontimemin = Minimum controllable on-time (120-ns maximum)
- Fsmax = Maximum switching frequency including tolerance
- Vinmax = Maximum input voltage
- Ioutmin = Minimum load current RDS1min = Minimum high-side MOSFET on-resistance (52-mΩ typical)

- RDS2min = Minimum low-side MOSFET on-resistance (27-mΩ typical)
- RL = Series resistance of output inductor. (16)

For the example circuit, Vin = 12 V, Fs = 500 kHz, when Iout = 0 A, the minimum output voltage is 0.72 V.

10.2.2.7 Compensation Component Selection

Integrated buck converters in TPS65283, TPS65283-1 incorporate a peak current mode. The error amplifier is a transconductance amplifier with a gain of 300 µA/V. A typical type II compensation circuit adequately delivers a phase margin between 60° and 90°. Cb adds a high-frequency pole to attenuate high-frequency noise when needed. To calculate the external compensation components, follow these steps.

1. Select switching frequency f_{SW} that is appropriate for application depending on L and C sizes, output ripple, EMI, and so forth. Switching frequency between 500 kHz to 1 MHz gives the best trade-off between performance and cost. To optimize efficiency, lower switching frequency is desired.
2. Set up crossover frequency, f_c, which is typically between 1/5 and 1/20 of f_{SW}.
3. RC can be determined by:

$$R_C = \frac{2\pi \cdot f_c \cdot Vo \cdot Co}{g_M \cdot Vref \cdot gm_{ps}}$$

where

- g_M is the error amplifier gain (300 µA/V),
- gm_{ps} is the power stage voltage to current conversion gain (7.4 A/V). (17)

4. Calculate C_C by placing a compensation zero at or before the dominant pole ($f_p = \frac{1}{C_O \cdot R_L \cdot 2\pi}$)

$$C_C = \frac{R_L \cdot Co}{R_C} \quad (18)$$

5. Optional C_b can be used to cancel the 0 from the ESR associated with C_b.

$$C_b = \frac{R_{ESR} \cdot Co}{R_C} \quad (19)$$

6. Type III compensation can be implemented with the addition of one capacitor, C_1. This allows for slightly higher loop bandwidths and higher phase margins. If used, C_1 is calculated from Equation 20.

$$C_1 = \frac{1}{2\pi \cdot R_1 \cdot f_C} \quad (20)$$

For this design, the calculated values for the compensation components are Rc = 20 kΩ, C_C = 3.3 nF, and Cb = 22 pF.

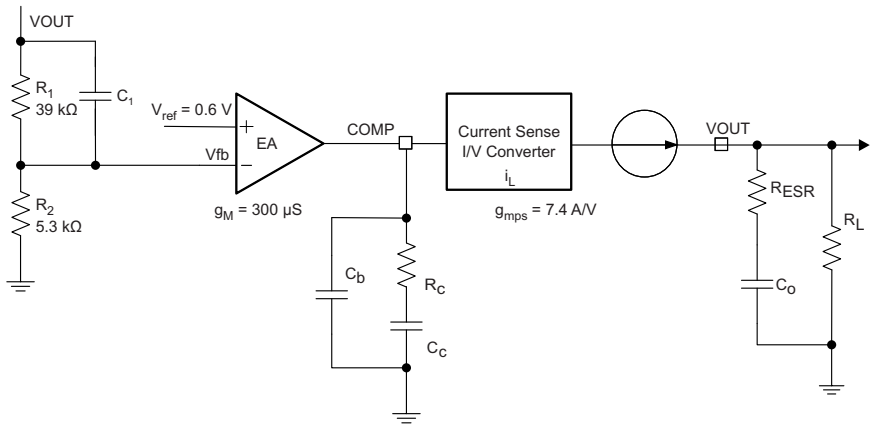


Figure 31. DC-DC Loop Compensation

10.2.3 Application Curves

T_J = 25°C, Vin = 12 V, Vout1 = 1.2 V, Vout2 = 5 V, f_{SW} = 500 kHz, $R_{nFAULT1}$ = $R_{nFAULT2}$ = 100 kΩ (unless otherwise noted)

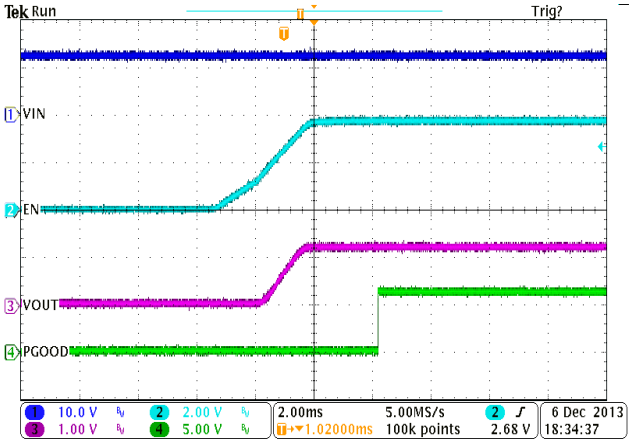


Figure 32. Buck1 Start Up by EN1 Pin With 2-A Loading

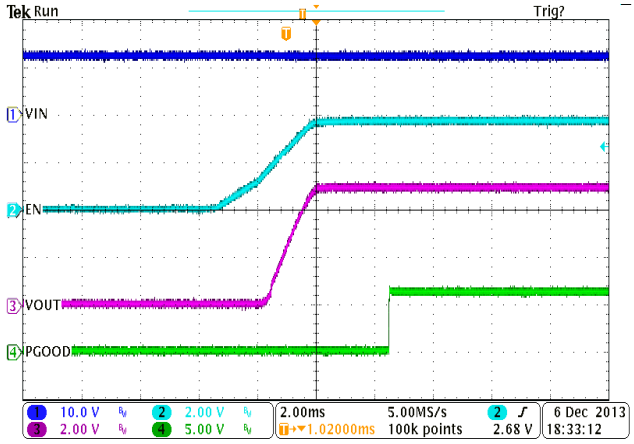


Figure 33. Buck2 Start Up by EN2 Pin With 2-A Loading

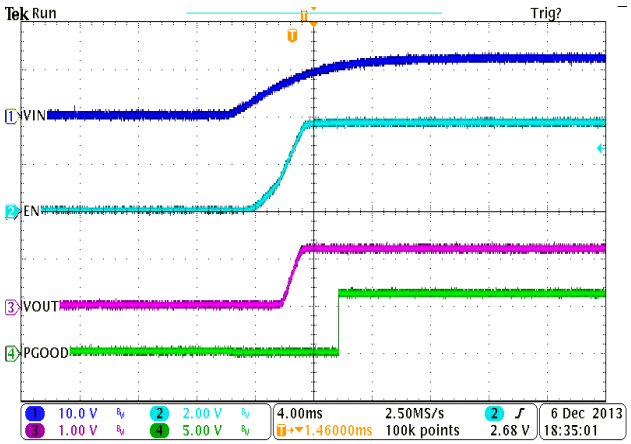


Figure 34. Ramp Vin to Start Up Buck1 With 2-A Loading

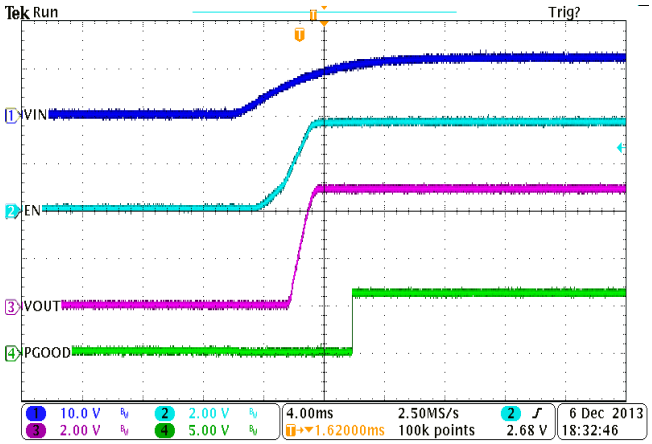


Figure 35. Ramp Vin to Start Up Buck2 With 2-A Loading

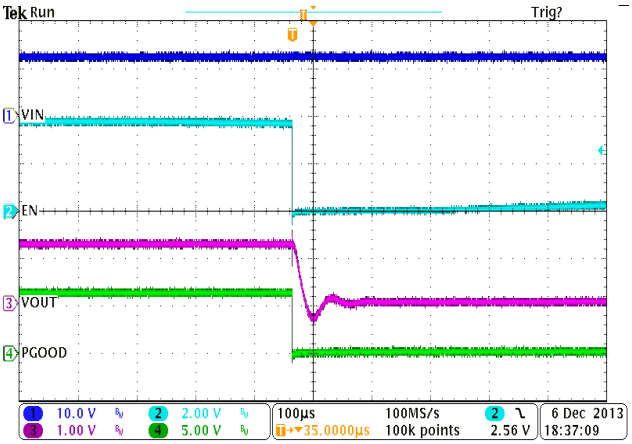


Figure 36. Buck1 Shut Down by EN1 Pin With 2-A Loading

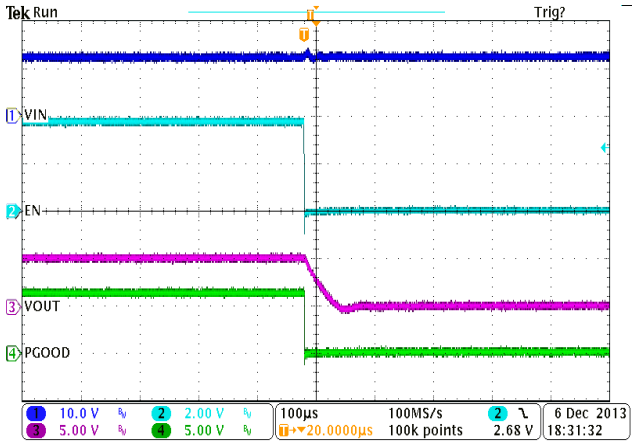
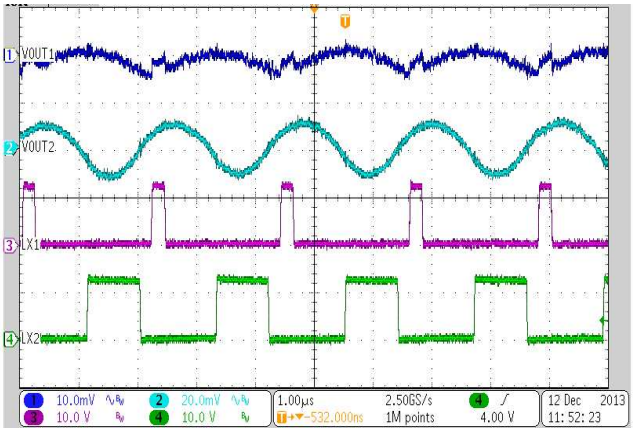


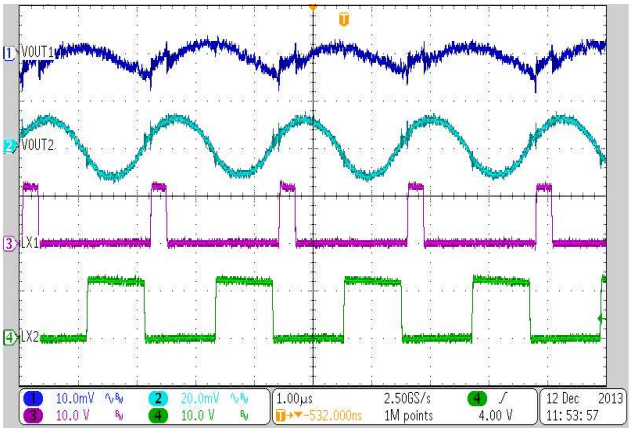
Figure 37. Buck2 Shut Down by EN2 Pin With 2-A Loading

T_J = 25°C, Vin = 12 V, Vout1 = 1.2 V, Vout2 = 5 V, f_{SW} = 500 kHz, $R_{nFAULT1}$ = $R_{nFAULT2}$ = 100 kΩ (unless otherwise noted)



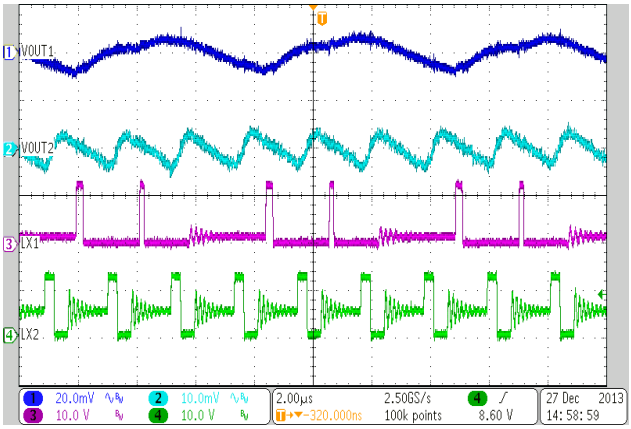
Iout1 = Iout2 = 0 A

Figure 38. Buck Output Voltage Ripple in PWM Mode



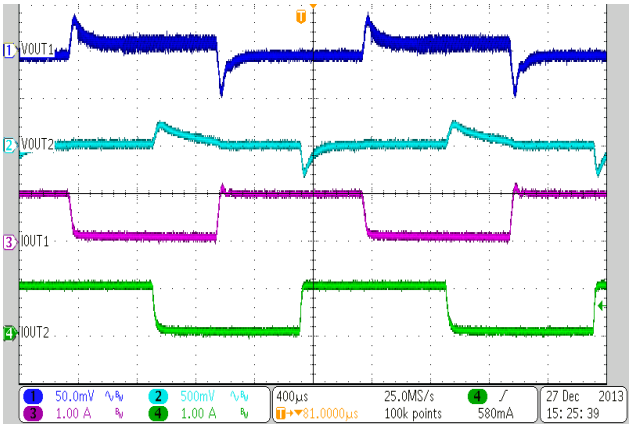
Iout1 = Iout2 = 2.5 A

Figure 39. Buck Output Voltage Ripple in PWM Mode



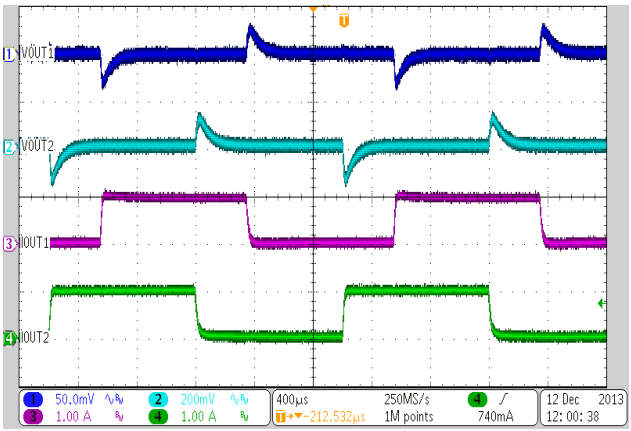
Iout1 = Iout2 = 0.1 A

Figure 40. Buck Output Voltage Ripple in PSM Mode



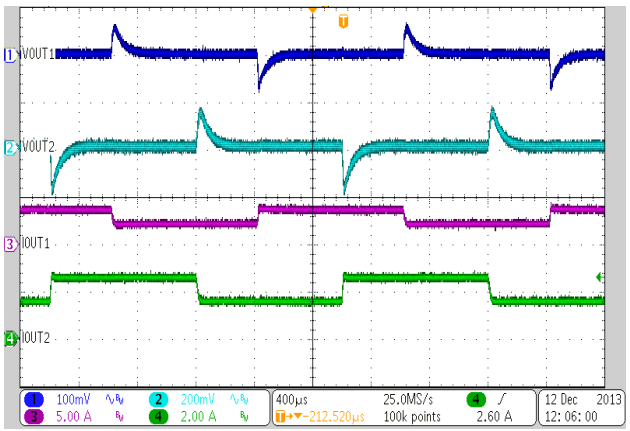
Iout1 = Iout2 = 0 to 1 A

Figure 41. Buck Output Load Transient in PSM Mode



Iout1 = Iout2 = 0 to 1 A

Figure 42. Buck Output Load Transient in PWM Mode



Iout1 = 2.5 to 3.5 A, Iout2 = 1.5 to 2.5 A

Figure 43. Buck Output Load Transient in PWM Mode

T_J = 25°C, Vin = 12 V, Vout1 = 1.2 V, Vout2 = 5 V, f_{SW} = 500 kHz, $R_{nFAULT1}$ = $R_{nFAULT2}$ = 100 kΩ (unless otherwise noted)

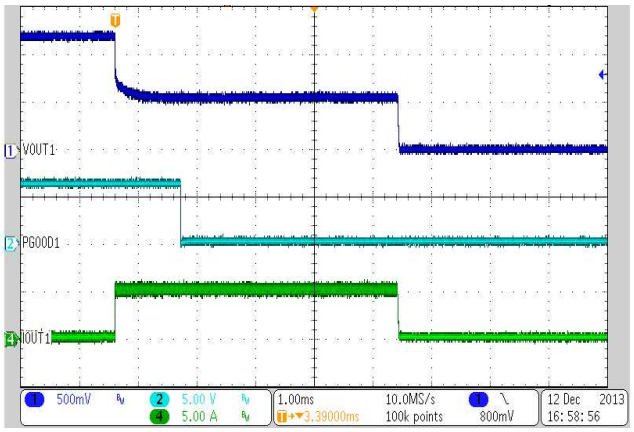


Figure 44. Buck1 Response to Hard Short

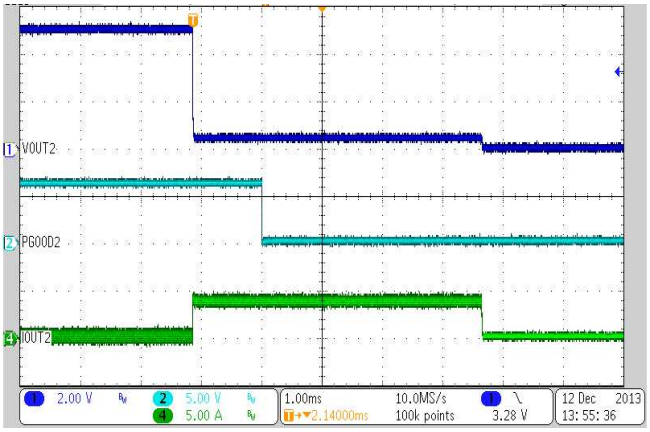


Figure 45. Buck2 Response to Hard Short

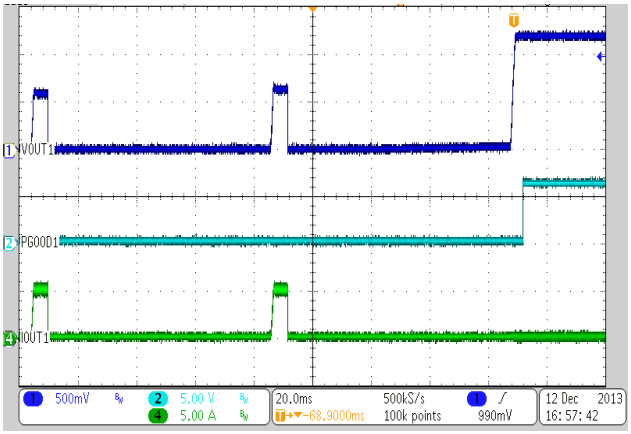


Figure 46. Buck1 Recovery from Hiccup

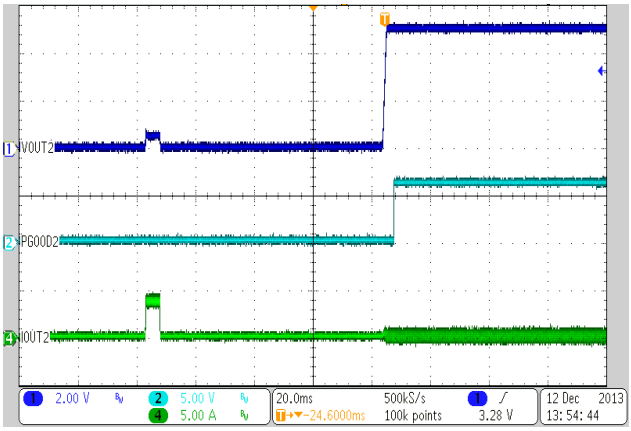


Figure 47. Buck2 Recovery from Hiccup

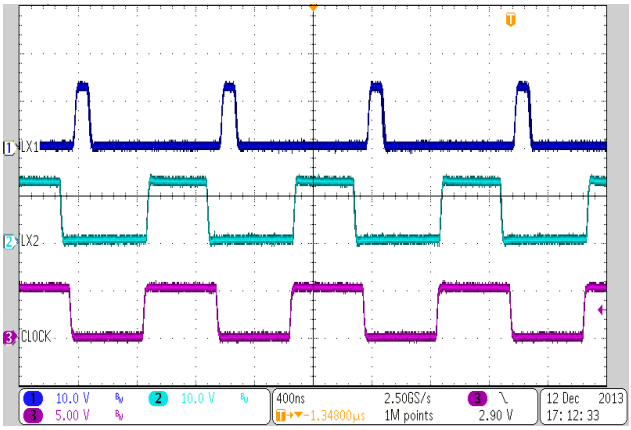
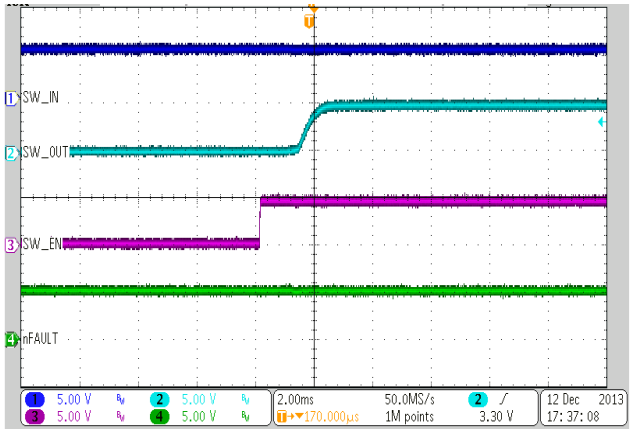


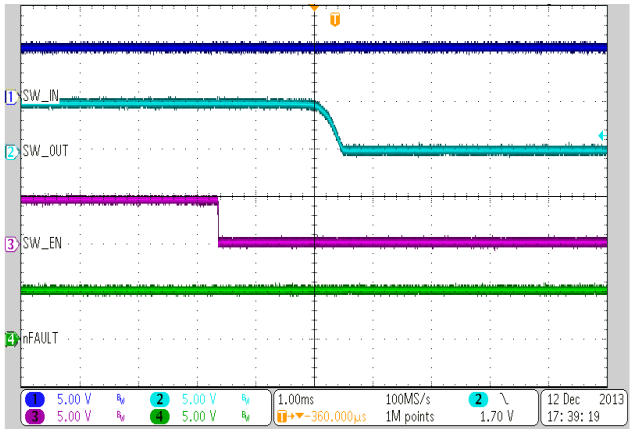
Figure 48. Clock Synchronization at 1 MHz



Rout = 50 Ω, Cout = 10 µF

Figure 49. Power Switch Turn on Delay and Rising Time

T_J = 25°C, Vin = 12 V, Vout1 = 1.2 V, Vout2 = 5 V, f_{SW} = 500 kHz, $R_{nFAULT1}$ = $R_{nFAULT2}$ = 100 kΩ (unless otherwise noted)



Rout = 50 Ω, Cout = 10 µF

Figure 50. Power Switch Turn off Delay and Fall Time

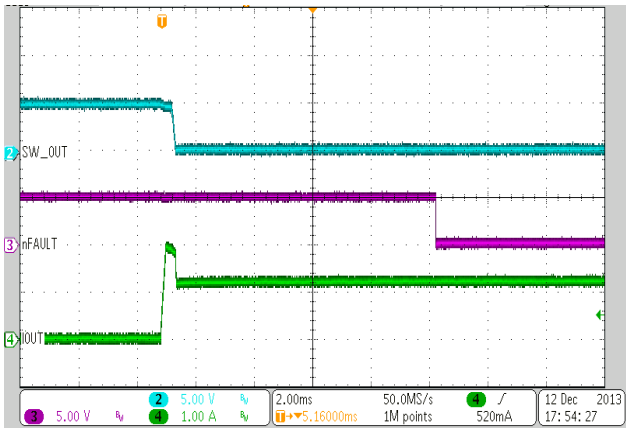


Figure 51. Power Switch Over Current With 2-A Loading

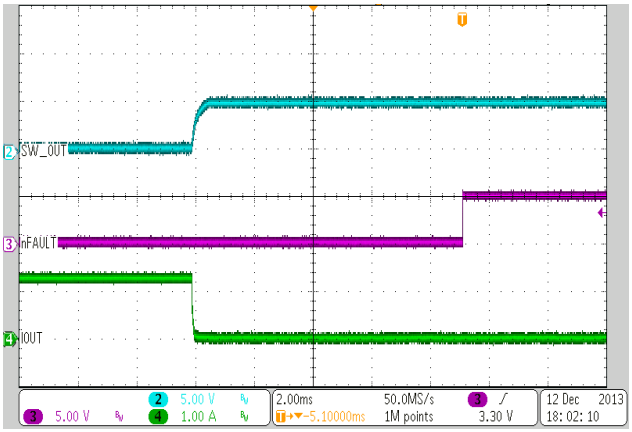


Figure 52. Power Switch Recovery from Over-Current

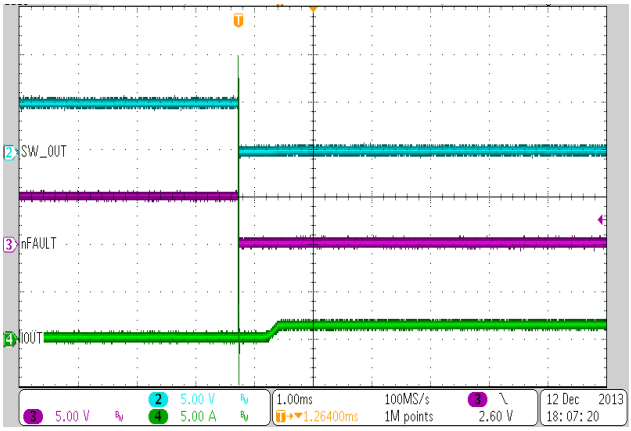


Figure 53. Power Switch Hard Short Operation

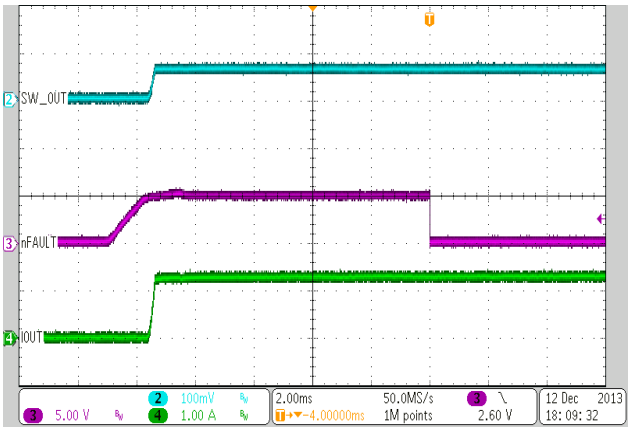


Figure 54. Power Switch Enable into Short Circuit

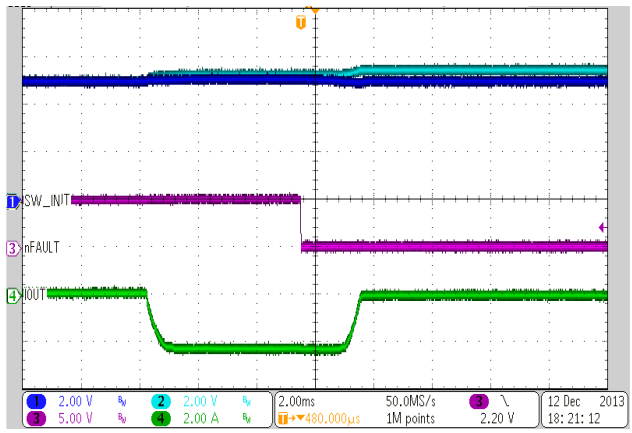


Figure 55. Power Switch Reverse Voltage Protection Response

11 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 4.5 to 18 V. This input supply should be well regulated. If the input supply is located more than a few inches from the TPS65283 or TPS65283-1 converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. A typical choice is an electrolytic capacitor with a value of 10 μF.

12 Layout

12.1 Layout Guidelines

12.1.1 PCB Layout Recommendation

When laying out the PCB, use the following guidelines to ensure proper operation of the IC. These items are also shown in the layout diagram of Figure 58.

- There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supply's performance. To help eliminate these problems, the VIN pin should be bypassed to ground with a low-ESR ceramic bypass capacitor with X5R or X7R dielectric. This capacitor provides the ac current into the internal power MOSFETs. Connect the (+) terminal of the input capacitor as close as possible to the VIN pin, and connect the (–) terminal of the input capacitor as close as possible to the PGND pin. Take care to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the power ground PGND connections.
- Because the LX connection is the switching node, the output inductor should be located close to the LX pin, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. Keep the switching node, LX, away from all sensitive small-signal nodes.
- Connect V7V decoupling capacitor connected close to the IC, between the V7V and the power ground PGND pin. This capacitor carries the MOSFET drivers' current peaks.
- Place the output filter capacitor of buck converter close to SW_IN pins. Try to minimize the ground conductor length while maintaining adequate width.
- AGND pin should be separately routed to the (–) terminal of V7V bypass capacitor to avoid switching grounding path. TI recommends a ground plane connecting to this ground path.
- The compensation should be as close as possible to the COMP pins. The COMP and ROSC pins are sensitive to noise, so the components associated to these pins should be located as close as possible to the IC and routed with minimal lengths of trace. Flood all unused areas on all layers with copper. Flooding with copper reduces the temperature rise of power components. You can connect the copper areas to PGND, AGND, VIN, or any other dc rail in the system.
- There is no electric signal internally connected to thermal pad in the device. Nevertheless, connect exposed pad beneath the IC to ground. Always solder thermal pad to the board and have as many vias as possible on the PCB to enhance power dissipation.

12.1.2 Power Dissipation and Junction Temperature

The total power dissipation inside TPS65283, TPS65283-1 should not to exceed the maximum allowable junction temperature of 125°C. The maximum allowable power dissipation is a function of the thermal resistance of the package ($R_{\theta JA}$) and ambient temperature.

The following analysis gives an approximation in calculating junction temperature based on the power dissipation in the package. However, note that thermal analysis is strongly dependent on additional system-level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal design practice must include all system-level factors in addition to individual component analysis.

To calculate the temperature inside the device under continuous load, use the following procedure.

1. Define the total continuous current through buck converter (including the load current through power switches). Make sure the continuous current does not exceed maximum load current requirement.
2. From the graphs in this section, determine the expected losses (y-axis) in watts for buck converter inside the device. The loss P_{D_BUCK} depends on the input supply and the selected switching frequency.
3. Determine the load current I_{OUT} through the power switches. Read $R_{DS(on)}$ of power switch from the typical

Layout Guidelines (continued)

characteristics graph.

4. Calculate the power loss through power switches with $P_{D\_PW} = R_{DS(on)} \times I_{OUT}$.
5. The *Thermal Information* table provides the thermal resistance $R_{\theta JA}$ for specific packages and board layouts.
6. To calculate the maximum temperature inside the IC, use Equation 21.

$$T_J = (P_{D\_BUCK} + P_{D\_PW}) \times R_{\theta JA} + T_A \quad (21)$$

where

- T_A = Ambient temperature (°C)
- $R_{\theta JA}$ = Thermal resistance (°C/W)
- P_{D_BUCK} = Total power dissipation in buck converter (W)
- P_{D_PW} = Total power dissipation in power switches (W)

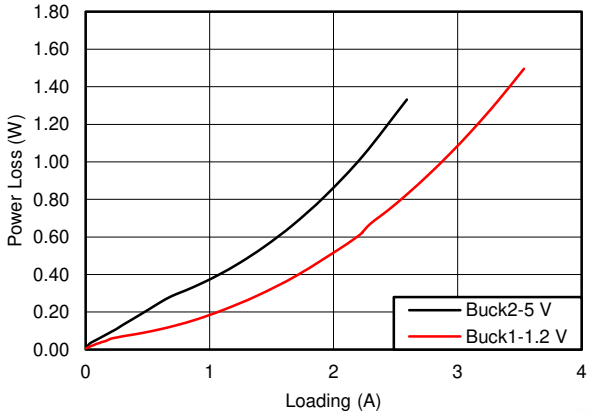
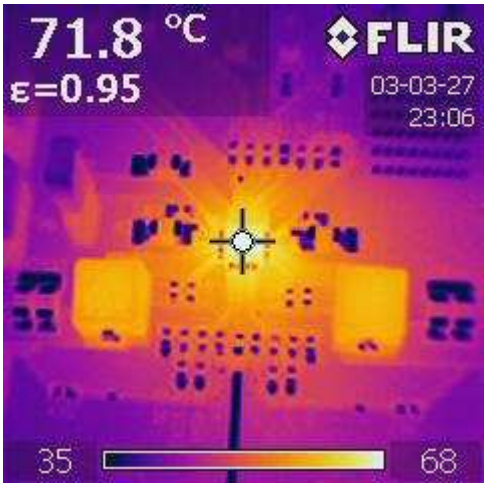


Figure 56. Power Dissipation of TPS65283



A. VIN = 12 V, Vout1 = 1.2 V / 3 A, Vout2 = 5 V / 2 A, VSW_in = 5 V, ISW_OUT = 1.2 A

B. EVM board: 4-layer PCB, 1.6-mm thickness, 35-µm copper thickness, 68-mm × 68-mm size, 9 vias at thermal pad

Figure 57. Thermal Signature of TPS65283EVM

12.2 Layout Example

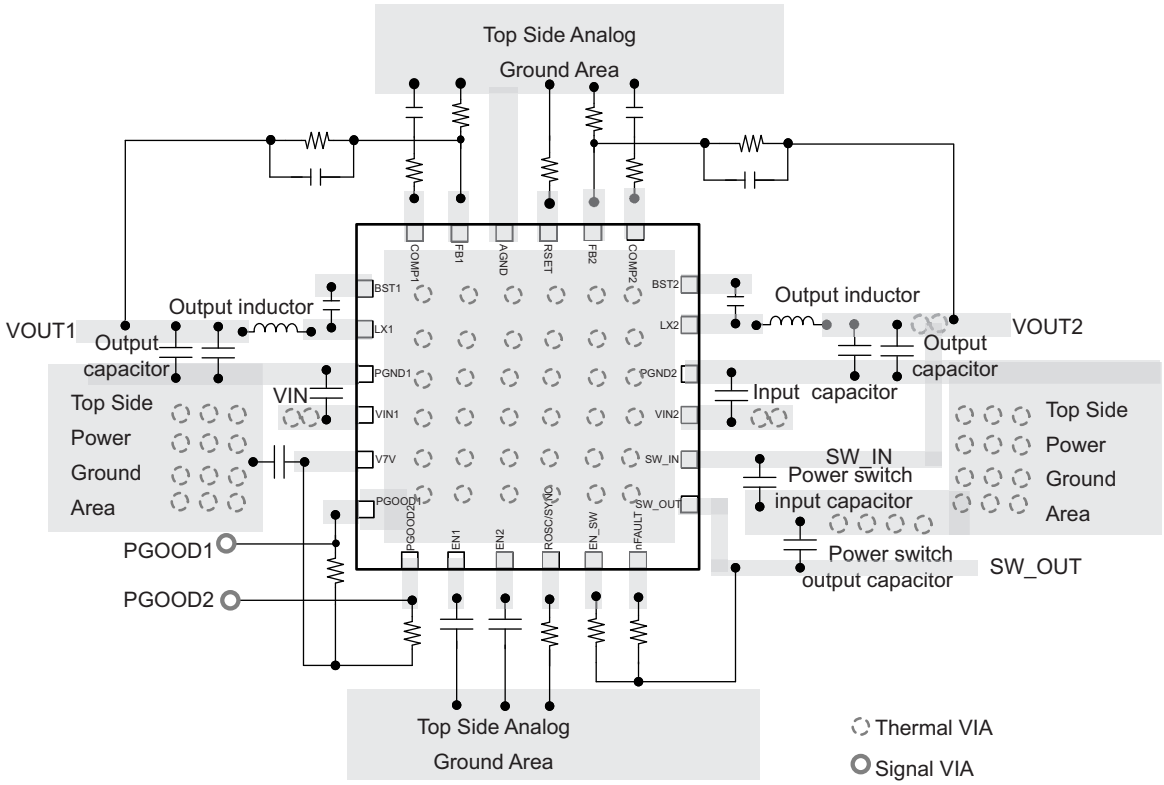


Figure 58. 4-Layer PCB Layout Recommendation

13 デバイスおよびドキュメントのサポート

13.1 ドキュメントのサポート

13.1.1 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 5. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
TPS65283	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS65283-1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

13.2 商標

PowerPAD is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.

13.3 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65283-1RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65283-1	Samples
TPS65283-1RGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65283-1	Samples
TPS65283RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 65283	Samples
TPS65283RGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 65283	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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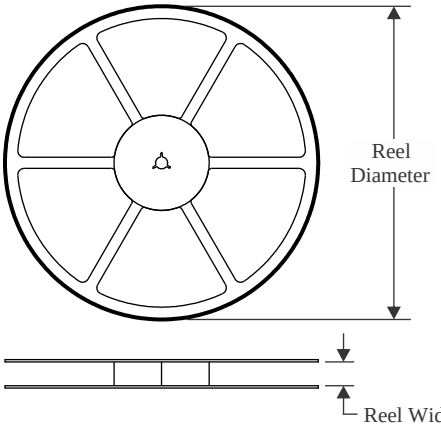
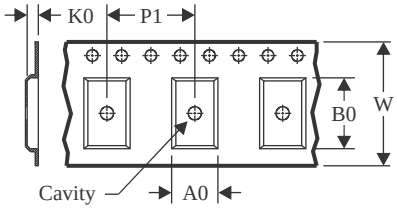
TAPE AND REEL INFORMATION

REEL DIMENSIONS

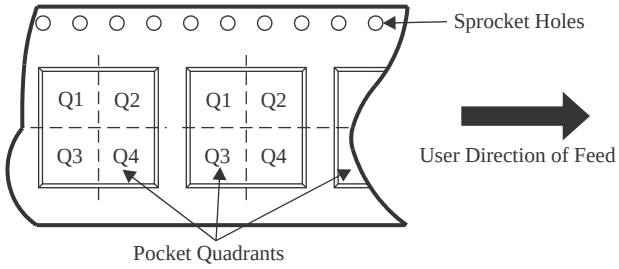


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

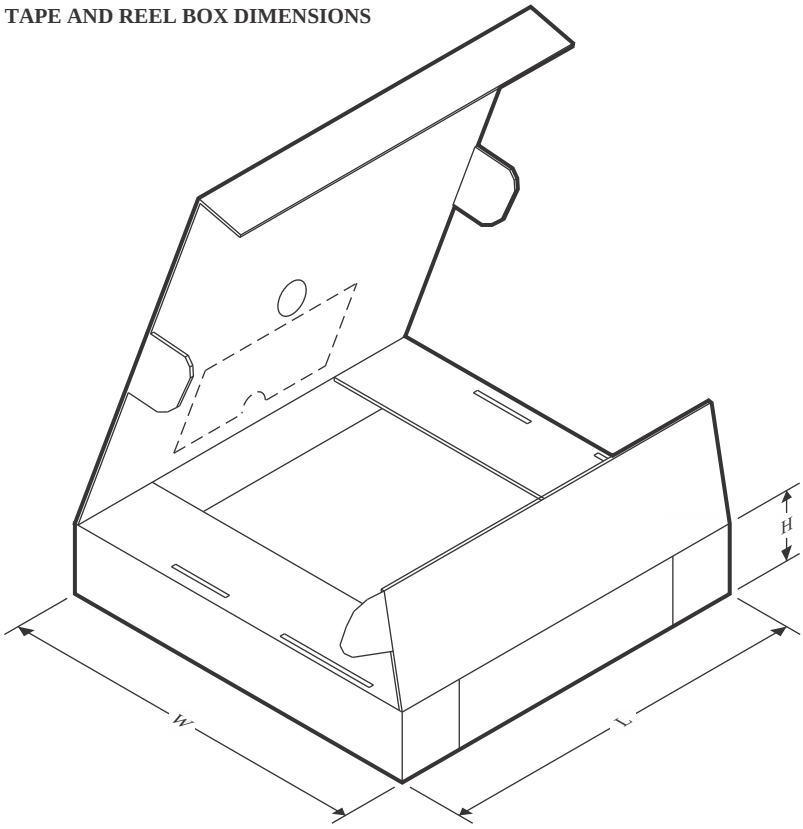
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65283-1RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65283-1RGER	VQFN	RGE	24	3000	330.0	12.4	4.35	4.35	1.1	8.0	12.0	Q2
TPS65283-1RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65283-1RGET	VQFN	RGE	24	250	180.0	12.5	4.35	4.35	1.1	8.0	12.0	Q2
TPS65283RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65283RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



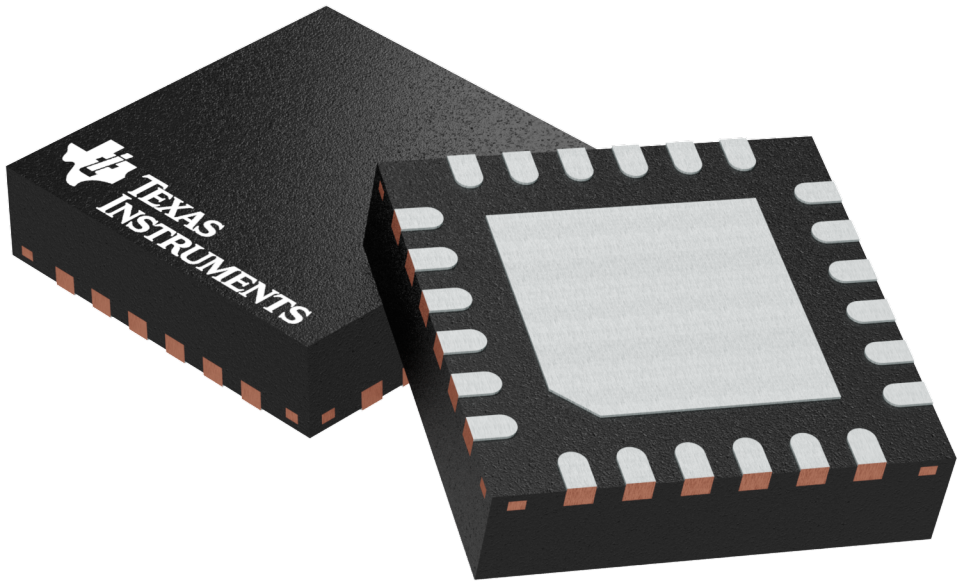
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65283-1RGER	VQFN	RGE	24	3000	346.0	346.0	33.0
TPS65283-1RGER	VQFN	RGE	24	3000	338.0	355.0	50.0
TPS65283-1RGET	VQFN	RGE	24	250	210.0	185.0	35.0
TPS65283-1RGET	VQFN	RGE	24	250	338.0	355.0	50.0
TPS65283RGER	VQFN	RGE	24	3000	346.0	346.0	33.0
TPS65283RGET	VQFN	RGE	24	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

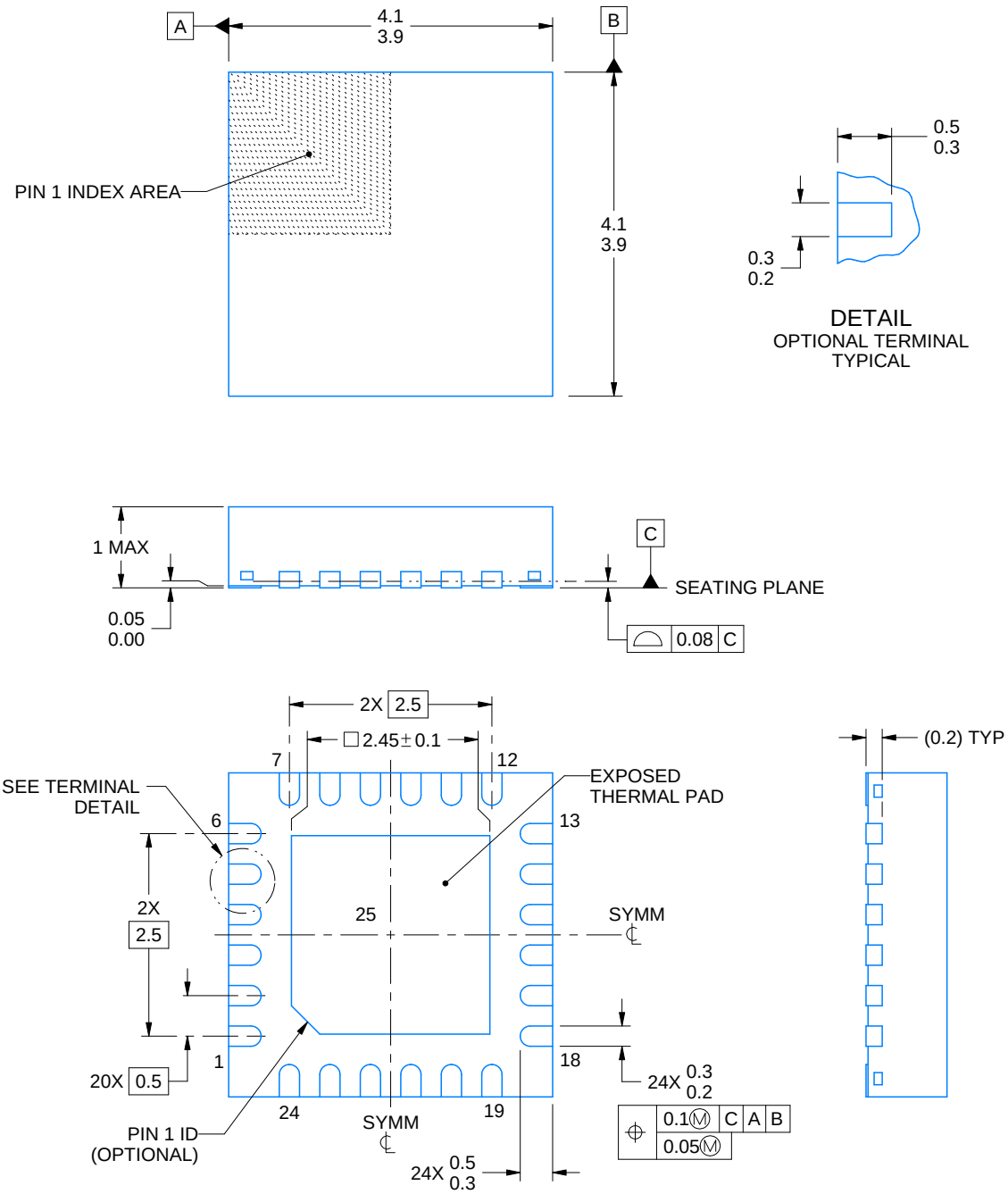
4204104/H

PACKAGE OUTLINE

RGE0024B

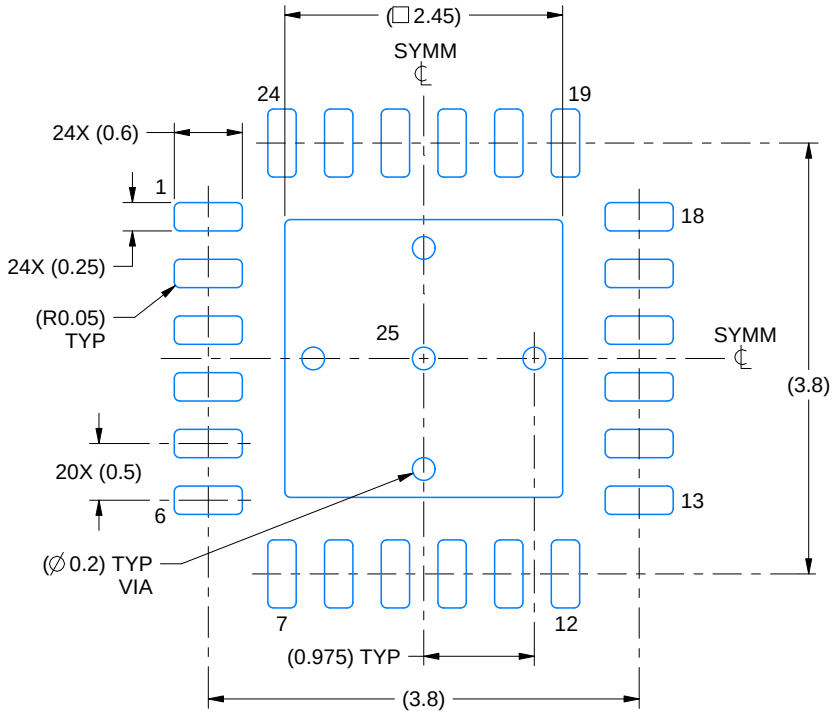
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

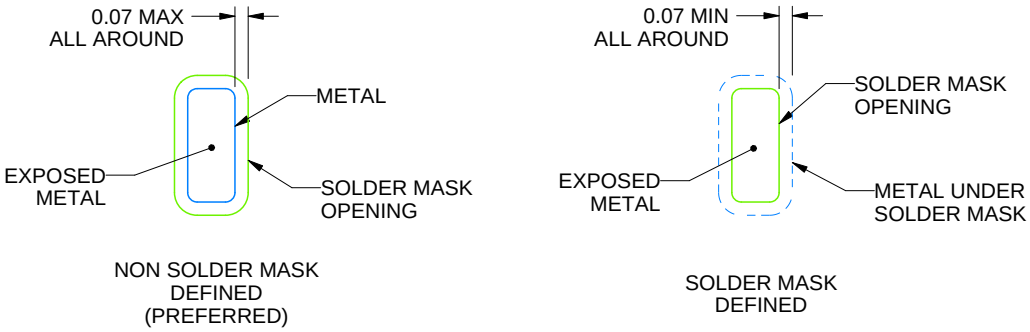


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

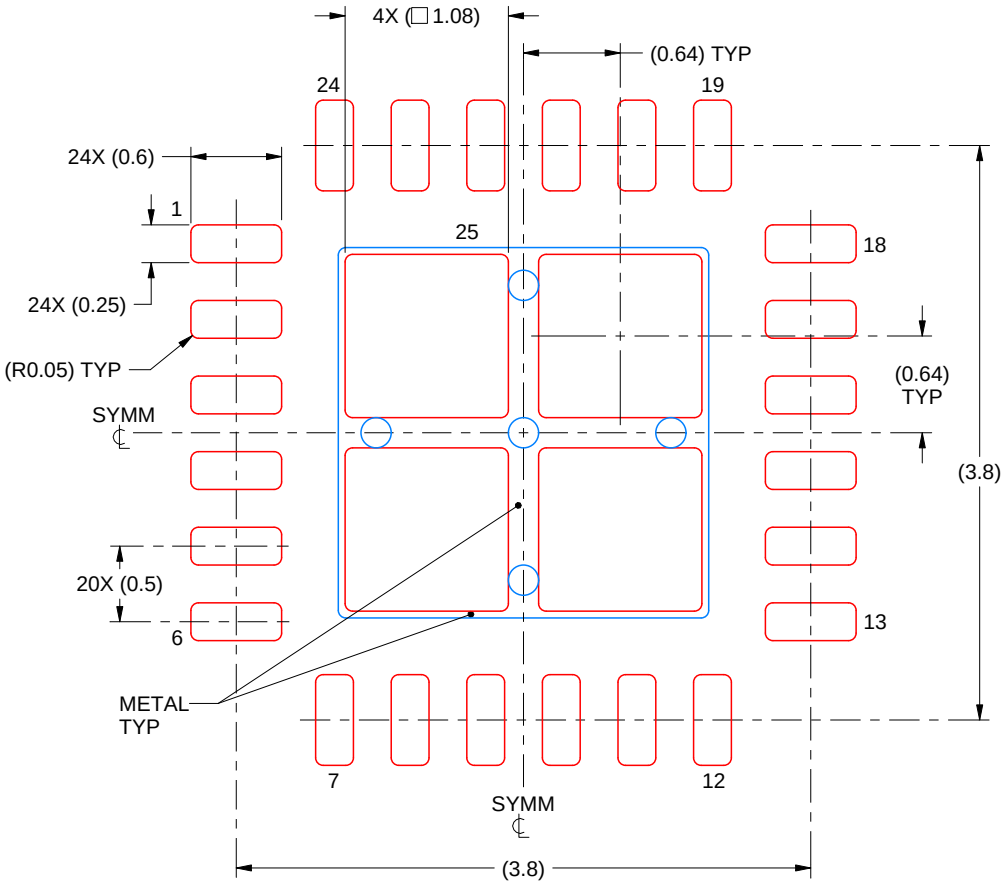


SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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