参考資料

Texas Instruments

TPS65295

JAJSH01 – FEBRUARY 2019

# TPS65295 包括的な DDR4 メモリ向け電源ソリューション

## 1 特長

- 同期整流降圧コンバータ (VDDQ)
  - 入力電圧範囲: 4.5V～18V
  - 出力電圧は 1.2V 固定
  - D-CAP3™モード制御による高速過渡応答
  - 連続出力電流:8A
  - 高度な Eco-mode™パルス・スキップ
  - $R_{DS(on)}$ が 22mΩ および 8.6mΩ の内蔵パワー・スイッチ
  - 600kHz のスイッチング周波数
  - 内部ソフト・スタート:1.6ms
  - サイクル単位の過電流保護
  - ラッチ付きの出力 OV および UV 保護
- 同期整流降圧コンバータ (VPP)
  - 入力電圧範囲: 3V～5.5V
  - 出力電圧は 2.5V 固定
  - D-CAP3™モード制御による高速過渡応答
  - 連続出力電流:1A
  - 高度な Eco-mode™パルス・スキップ
  - $R_{DS(on)}$ が 150mΩ および 120mΩ の内蔵パワー・スイッチ
  - 580kHz のスイッチング周波数
  - 内部ソフト・スタート:1ms
  - サイクル単位の過電流保護
  - ラッチ付きの出力 OV および UV 保護
- 1A LDO (VTT)
  - 1A の連続シンクおよびソース電流
  - 10µF のセラミック出力コンデンサのみで動作
  - S3 での高インピーダンスをサポート
  - ±30mV の VTT 出力精度 (DC+AC)
- バッファ付き基準電圧 (VTTREF)
  - バッファ付きで低ノイズの ±10mA 能力
  - 0.8% の出力精度
- 低い静止電流：150µA
- パワー・グッド・インジケータ
- 出力放電機能
- 電源オンおよび電源オフのシーケンシング制御
- ラッチなしの OT および UVLO 保護
- 18 ピン、3.0mm × 3.0mm の HotRod™ VQFN パッケージ

## 2 アプリケーション

- DDR4 メモリの電源
- ノートおよびデスクトップ PC、およびサーバー
- ウルトラブック、タブレット
- シングル・ボード・コンピュータ、モジュール型コンピュータ

## 3 概要

TPS65295 デバイスは、DDR4 メモリ・システム用の包括的な電源ソリューションを最小の総コストとスペースで実現します。DDR4 の電源オンおよび電源オフ・シーケンス要件に関する JEDEC 規格を満たしています。TPS65295 は、2 つの同期整流降圧コンバータ (VPP および VDDQ)、1A シンクおよびソース・トラッキング LDO (VTT)、バッファ付き低ノイズ基準電圧 (VTTREF) を内蔵しています。TPS65295 は D-CAP3™モードと 600kHz のスイッチング周波数を採用することで、使いやすさ、高速過渡応答、セラミック出力コンデンサのサポート (外部補償回路不要) を実現しています。

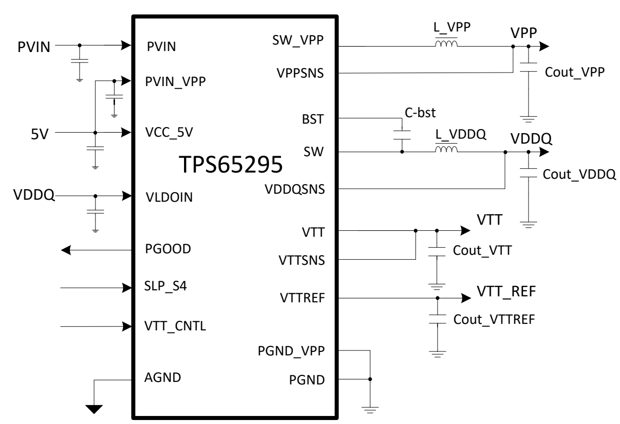
VTTREF は、½ VDDQ を 0.8% という非常に優れた精度でトラッキングします。VTT は、1A のシンクおよびソース電流を連続的に供給でき、わずか 10µF のセラミック出力コンデンサだけで動作します。

製品情報[(1)]

| 型番 | パッケージ | 本体サイズ(公称) |
|---|---|---|
| TPS65295 | VQFN (18) | 3.00mm×3.00mm |

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

代表的なアプリケーション






English Data Sheet: SLUSDK5

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## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

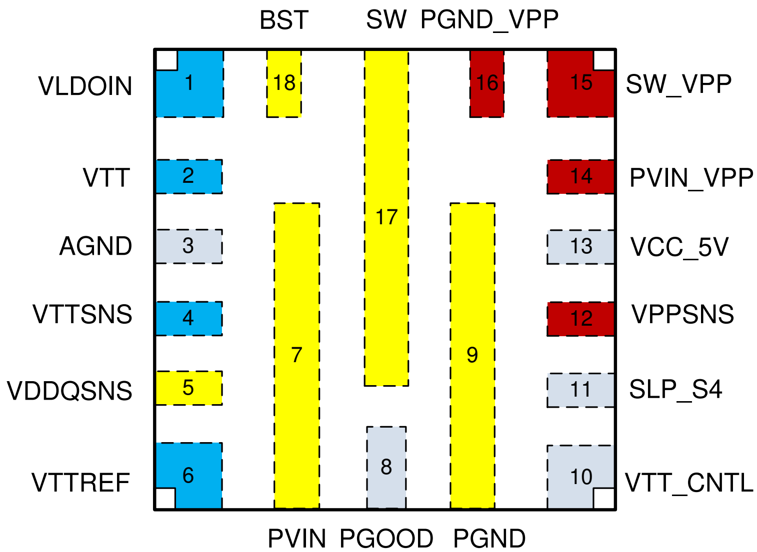
| 日付 | リビジョン | 注 |
|---|---|---|
| 2019 年 2 月 | * | 初版 |

## 5 概要（続き）

TPS65295 は非常に優れた電源性能だけでなく、豊富な機能も備えています。柔軟な電力状態制御をサポートしており、S3 状態では VTT を高インピーダンスにし、S4 または S5 状態では VDDQ、VTT、VTTREF を放電します。OVP、UVP、OCP、UVLO、サーマル・シャットダウン保護機能も使用できます。この製品は、放熱特性の優れた 18 ピンの HotRod™ VQFN パッケージで供給され、－40°C ～125°C の接合部温度範囲で動作するよう設計されています。

# 6 Pin Configuration and Functions

**RJE Package**
**18-Pin VQFN**
**Top View**




**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| VLDOIN | 1 | P | Power supply input for VTT LDO. Connect VDDQ in typical application. |
| VTT | 2 | O | VTT 1-A LDO output. Recommend to connect to 10-µF or larger capacitance for stability. |
| AGND | 3 | G | Signal ground. |
| VTTSNS | 4 | I | VTT output voltage feedback. |
| VDDQSNS | 5 | I | VDDQ output voltage feedback. |
| VTTREF | 6 | O | Buffered VTT reference output. Recommend to connect to 0.22-µF or larger capacitance for stability. |
| PVIN | 7 | P | Input power supply for VDDQ buck. |
| PGOOD | 8 | O | Power good signal open-drain output. PGOOD goes high when VPP and VDDQ output voltage are within the target range. |
| PGND | 9 | G | Power ground for VDDQ buck. |
| VTT_CNTL | 10 | I | VTT_CNTL signal input for VTT LDO enable control. For detail control setup, please refer to表 1. |
| SLP_S4 | 11 | I | SLP_S4 signal input for VDDQ buck and VPP buck enable control. For detail control setup, please refer to 表 1. |
| VPPSNS | 12 | I | VPP output voltage feedback. |
| VCC_5V | 13 | P | Power supply for VPP and VDDQ buck converter control logic circuit. |
| PVIN_VPP | 14 | P | Input power supply for VPP buck. |
| SW_VPP | 15 | O | VPP switching node connection to the inductor and bootstrap capacitor. |
| PGND_VPP | 16 | G | Power ground for VPP buck. |
| SW | 17 | O | VDDQ switching node connection to the inductor and bootstrap capacitor. |
| BST | 18 | I | High-side MOSFET gate driver bootstrap voltage input for VDDQ buck. Connect a capacitor between the BST pin and the SW pin. |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [(1)]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Input voltage | | PVIN | –0.3 | 20 | V |
| | | VBST | –0.3 | 25 | V |
| | | VBST-SW | –0.3 | 6 | V |
| | | VTT_CNTL, SLP_S4, VCC_5V, PVIN_VPP, VLDOIN, VDDQSNS, VTTSNS, VPPSNS | –0.3 | 6 | V |
| | | PGND, AGND,PGND_VPP | –0.3 | 0.3 | V |
| Output voltage | | SW DC | –0.3 | 20 | V |
| | | SW (20-ns transient) | –3 | 22 | V |
| | | SW_VPP DC | –0.3 | 7 | V |
| | | SW_VPP (20-ns transient) | –3 | 8 | V |
| | | PGOOD, VTT,VTTREF | –0.3 | 6 | V |
| $T_J$ | Operating junction temperature | | –40 | 150 | °C |
| $T_{stg}$ | Storage temperature | | –55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [(1)] | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22- V C101 [(2)] | ±500 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Input voltage | | PVIN | 4.5 | 18 | V |
| | | VBST | –0.3 | 23 | V |
| | | VBST-SW | –0.3 | 5.5 | V |
| | | VTT_CNTL, SLP_S4, VCC_5V, PVIN_VPP, VLDOIN, VDDQSNS, VTTSNS, VPPSNS | –0.3 | 5.5 | V |
| | | PGND, AGND,PGND_VPP | –0.3 | 0.3 | V |
| Output voltage | | SW DC | –0.3 | 18 | V |
| | | SW (20-ns transient) | –3 | 20 | V |
| | | SW_VPP DC | –0.3 | 5.5 | V |
| | | SW_VPP (20-ns transient) | –3 | 6.5 | V |
| | | PGOOD, VTT,VTTREF | –0.3 | 5.5 | V |
| $I_{VDDQOUT}$ | VDDQ Output current | | | 8 | A |
| $T_J$ | Operating junction temperature | | –40 | 125 | °C |

## 7.4 Thermal Information

| THERMAL METRIC(1) | | TPS65295 RJE (VQFN) 18 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 58.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 26.1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 17.7 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 17.7 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

## 7.5 Electrical Characteristics

$T_J$=-40°C to 125°C, $V_{PVIN}$=12V, $V_{PVIN\_VPP}$=5V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT SUPPLY VOLTAGE** | | | | | | |
| $I_{VCC\_5V}$ | VCC_5V supply current | $V_{SLP\_S4}$ = $V_{VTT\_CNTL}$ = 0 V | | 5 | | µA |
| | | $V_{SLP\_S4}$ = 5 V, $V_{VTT\_CNTL}$ = 0 V, no load | | 110 | | µA |
| | | $V_{SLP\_S4}$ = $V_{VTT\_CNTL}$ = 5 V, no load | | 150 | | µA |
| VIN | PVIN input voltage range | | 4.5 | | 18 | V |
| **UVLO** | | | | | | |
| UVLO | VCC_5V under-voltage lockout | Wake up VCC_5V voltage | | 4.1 | 4.5 | V |
| | | Shut down VCC_5V voltage | 3.3 | 3.6 | | V |
| | | Hysteresis VCC_5V voltage | | 500 | | mV |
| **VDDQ** | | | | | | |
| $V_{VDDQSNS}$ | VDDQ sense voltage | | 1.188 | 1.2 | 1.212 | V |
| $I_{VDDQSNS}$ | VDDQSNS input current | $V_{VDDQSNS}$ =1.2 V | | 40 | | µA |
| $I_{VDDQDIS}$ | VDDQ discharge current | $V_{SLP\_S4}$ = $V_{VTT\_CNTL}$ = 0 V, $V_{VDDQSNS}$ = 0.5 V | | 12 | | mA |
| $t_{VDDQSS}$ | VDDQ soft-start time | | | 1.6 | 2.65 | ms |
| $t_{VDDQDLY}$ | VDDQ ramp up delay time | | | 2 | | ms |
| $R_{DSONH}$ | High-side switch resistance | $T_J$ = 25°C, $V_{PVIN}$ = 19V, $V_{VCC\_5V}$ = 5V | | 22 | | mΩ |
| $R_{DSONL}$ | Low-side switch resistance | $T_J$ = 25°C, $V_{PVIN}$ = 19V, $V_{VCC\_5V}$ = 5V | | 8.6 | | mΩ |
| $I_{VDDQOCL}$ | Low-side valley current limited | $V_{OUT}$ = 1.2 V, L = 0.68 µH | 8.2 | 9.8 | 11.5 | A |
| $f_{SW}$ | VDDQ switching freqency | | | 600 | | kHz |
| $t_{OFF(MIN)}$ | Minimum off time | | | 198 | | ns |
| **PGOOD (VDDQ, VPP)** | | | | | | |
| $V_{THPG}$ | PGOOD threshold | VDDQSNS / VPPSNS falling (Fault) | | 87 | | % |
| | | VDDQSNS / VPPSNS rising (Good) | | 93 | | % |
| | | VDDQSNS / VPPSNS rising (Fault) | | 115 | | % |
| | | VDDQSNS / VPPSNS falling (Good) | | 110 | | % |
| $I_{PGMAX}$ | PG sink current | $V_{PGOOD}$ =0.5V, $V_{SLP\_S4}$ =$V_{VTT\_CNTL}$ = 5 V, no load | | 46 | | mA |
| $t_{PGDLY}$ | PG start-up delay | PG from low to high | | 1 | | ms |
| **VPP** | | | | | | |
| $V_{VPPSNS}$ | VPP sense voltage | | 2.45 | 2.5 | 2.55 | V |
| $I_{VPPSNS}$ | VPPSNS input current | $V_{VPPSNS}$ =2.5 V | | 20 | | µA |

## Electrical Characteristics (continued)

$T_J$=-40°C to 125°C, $V_{PVIN}$=12V, $V_{PVIN\_VPP}$=5V (unless otherwise noted)

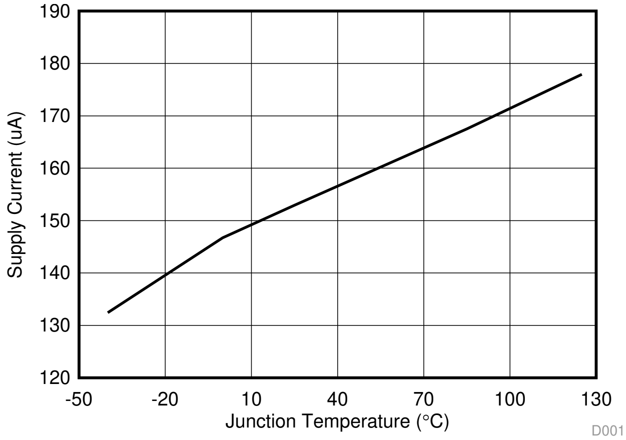
| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{VPPDIS}$ | VPP discharge current | $V_{SLP\_S4}$ = $V_{VTT\_CNTL}$ = 0 V, $V_{VPPSNS}$ = 0.5 V | | 12 | | mA |
| $t_{VPPSS}$ | VPP soft-start time | | | 1 .0 | 2 | ms |
| $R_{DSONH}$ | High-side switch resistance | $T_J$ = 25°C, $V_{PVIN\_VPP}$ = 5V, $V_{VCC\_5V}$ = 5V | | 150 | | mΩ |
| $R_{DSONL}$ | Low-side switch resistance | $T_J$ = 25°C, $V_{PVIN\_VPP}$=5V, $V_{VCC\_5V}$ = 5V | | 120 | | mΩ |
| $I_{VPPOCL}$ | Low-side valley current limited | $V_{OUT}$ = 2.5 V, L = 4.7 µH | 1.05 | 1.6 | 2.1 | A |
| $f_{sw}$ | VPP switching frequency | | | 580 | | kHz |
| $t_{OFF(MIN)}$ | Minimum off time | | | 195 | | ns |
| $t_{OOA}$ | OOA mode operation period | $V_{VPPSNS}$ =2.5 V | | 31 | | µs |
| **OVP AND UVP (VDDQ, VPP)** | | | | | | |
| $V_{OVP}$ | OVP threshold voltage | OVP detect voltage | 120 | 125 | 130 | % |
| $V_{UVP1}$ | UVP threshold voltage | UVP detect voltage | 55 | 60 | 65 | % |
| $t_{OVPDLY}$ | OVP delay | | | 20 | | µs |
| $t_{UVPDLY}$ | UVP delay | | | 250 | | µs |
| **VTTREF OUTPUT** | | | | | | |
| $V_{VTTREF}$ | Output voltage | | | 1/2* $V_{VDDQSNS}$ | | V |
| $V_{VTTREF}$ | Output voltage tolerance to VDDQ | $T_J$ = 25°C, $\lvert I_{VTTREF}\rvert$ ≤100 µA, $V_{VDDQSNS}$ = 1.2 V | 49.2 | | 50.8 | % |
| | | $T_J$ = 25°C, $\lvert I_{VTTREF}\rvert$ ≤10mA, $V_{VDDQSNS}$ = 1.2 V | 49 | | 51 | |
| $I_{VTTREFOCLSRC}$ | Source current limit | $V_{VDDQSNS}$ = 1.2 V, $V_{VTTREF}$= 0 V | 10 | 18 | | mA |
| $I_{VTTREFOCLSnk}$ | Sink current limit | $V_{VDDQSNS}$ = 1.2 V, $V_{VTTREF}$= 1.2 V | 10 | 18 | | mA |
| $I_{VTTREFDIS}$ | VTTREF discharge current | $T_J$ = 25°C, $V_{SLP\_S4}$ = $V_{VTT\_CNTL}$ = 0 V, $V_{VTTREF}$ = 0.5 V | 0.8 | 1.3 | | mA |
| **VTT OUTPUT** | | | | | | |
| $V_{VTT}$ | Output voltage | | | $V_{VTTREF}$ | | V |
| $V_{VTTTOL}$ | Output voltage tolerance | $\lvert I_{VTT}\rvert$ ≤10 mA, $V_{VDDQSNS}$ = 1.2 V, $I_{VTTREF}$= 0 A | –20 | | 20 | mV |
| | | $T_J$ = 25°C,$\lvert I_{VTT}\rvert$ ≤1A, $V_{VDDQSNS}$ = 1.2 V, $I_{VTTREF}$= 0 A | –30 | | 30 | |
| $I_{VTTOCLSRC}$ | Source current limit | $V_{VDDQSNS}$ = 1.2 V, $V_{VTT}$= $V_{VTTSNS}$= 0.5 V, $I_{VTTREF}$=0 A | 1 | 1.7 | | A |
| $I_{VTTOCLSnk}$ | Sink current limit | $V_{VDDQSNS}$ = 1.2 V, $V_{VTT}$= $V_{VTTSNS}$= 0.7 V, $I_{VTTREF}$=0 A | 1 | 1.7 | | A |
| $I_{VTTLK}$ | Leakage current | $T_J$ = 25°C, $V_{SLP\_S4}$ = 5 V, $V_{VTT\_CNTL}$ = 5 V, $V_{VTT}$ =$V_{VTTREF}$ | | | 5 | µA |
| $I_{VTTSNSBIAS}$ | VTTSNS input bias current | $V_{SLP\_S4}$ = 5 V, $V_{VTT\_CNTL}$ = 5 V, $V_{VTT}$ =$V_{VTTREF}$ | –0.5 | 0 | 0.5 | |
| $I_{VTTSNSLK}$ | VTTSNS leakage current | $V_{SLP\_S4}$ = 5 V, $V_{VTT\_CNTL}$ = 0 V, $V_{VTT}$ =$V_{VTTREF}$ | –1 | 0 | 1 | |
| $I_{VTTDLY}$ | VTT output delay relative to VTT_CNTL | | | | 35 | us |
| $I_{VTTDIS}$ | VTT discharge current | $T_J$ = 25°C, $V_{SLP\_S4}$ = $V_{VTT\_CNTL}$ = 0 V, $V_{VDDQSNS}$ = 1.2 V, $V_{VTT}$ =0.5V, $I_{VTTREF}$ =0 A | | 5.7 | | mA |
| **SLP_S4, VTT_CNTL LOGIC THRESHOLD** | | | | | | |
| $V_{IH}$ | SLP_S4/VTT_CNTL high-level voltage | | 1.6 | | | V |

## Electrical Characteristics (continued)

$T_J$=-40°C to 125°C, $V_{PVIN}$=12V, $V_{PVIN\_VPP}$=5V (unless otherwise noted)

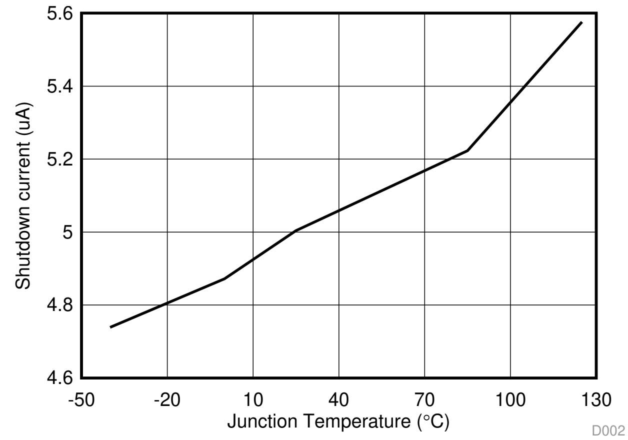
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IL}$ | SLP_S4/VTT_CNTL low-level voltage | | | | 0.5 | V |
| $R_{TOGND}$ | SLP_S4/VTT_CNTL resistance to GND | | | 500 | | kΩ |
| **THERMAL PROTECTION** | | | | | | |
| $T_{OTP}$ | OTP trip threshold | | | 150 | | °C |
| $T_{OTPHSY}$ | OTP hysteresis | | | 20 | | °C |

## 7.6 Typical Characteristics




$V_{SLP\_S4}$ = 5 V $V_{VTT\_CNTL}$ = 5 V

**図 1. VCC_5V Supply Current vs Junction Temperature**




$V_{SLP\_S4}$ = 0 V $V_{VTT\_CNTL}$ = 0 V

**図 2. VCC_5V Shutdown Current vs Temperature**

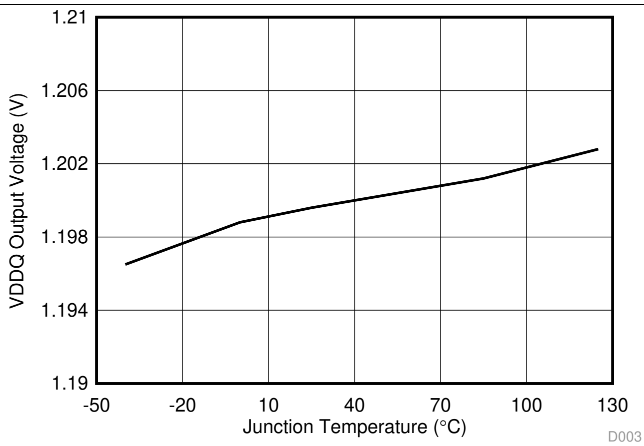



**図 3. VDDQ Output Voltage vs Junction Temperature**

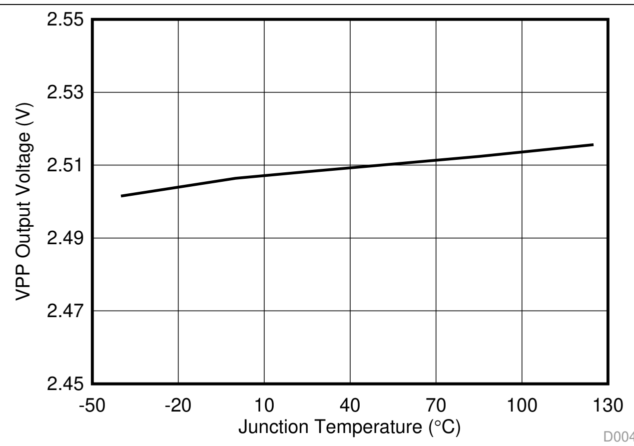



**図 4. VPP Output Voltage vs Junction Temperature**

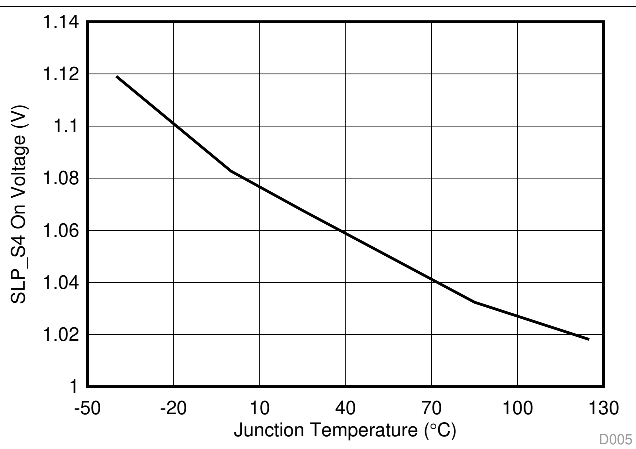



**図 5. Enable On Voltage (SLP_S4) vs Junction Temperature**

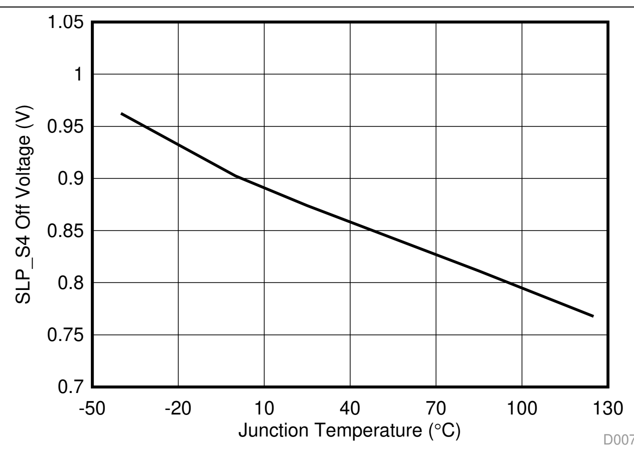



**図 6. Enable Off Voltage (SLP_S4) vs Junction Temperature**

## Typical Characteristics (continued)

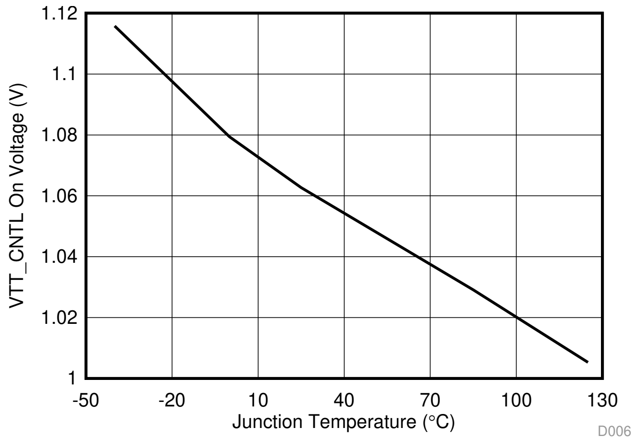



**図 7. Enable On Voltage (VTT_CNTL) vs Junction Temperature**

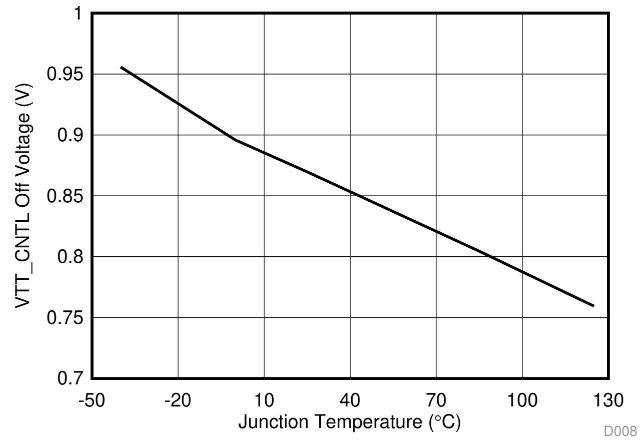



**図 8. Enable Off Voltage (VTT_CNTL) vs Junction Temperature**

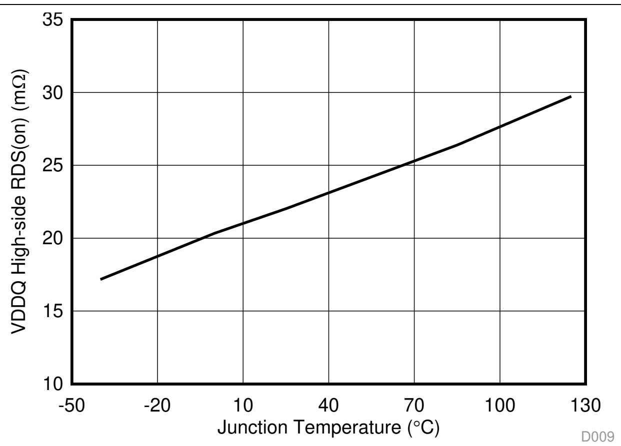



**図 9. VDDQ High-Side $R_{DS(on)}$ vs Junction Temperature**

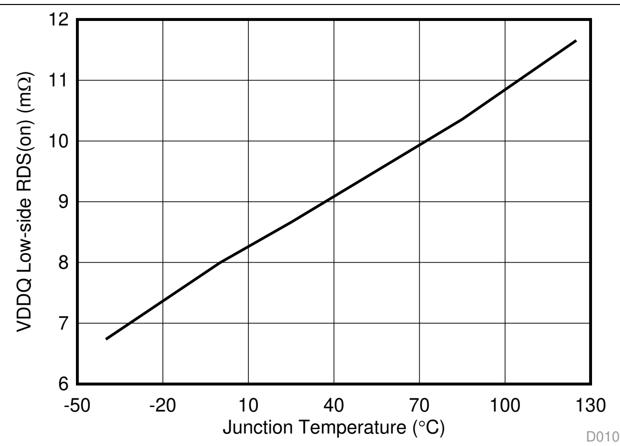



**図 10. VDDQ Low-Side $R_{DS(on)}$ vs Junction Temperature**

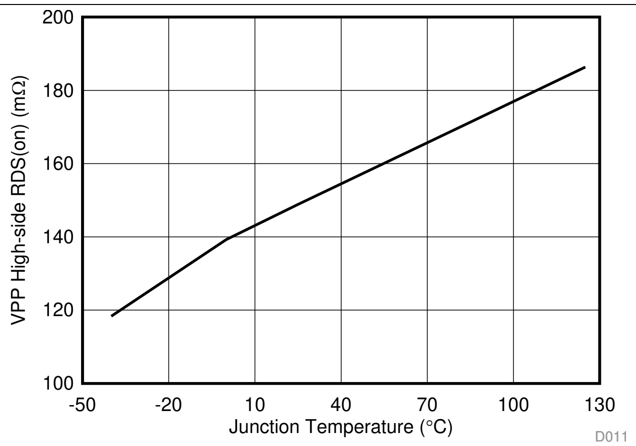



**図 11. VPP High-Side $R_{DS(on)}$ vs Junction Temperature**

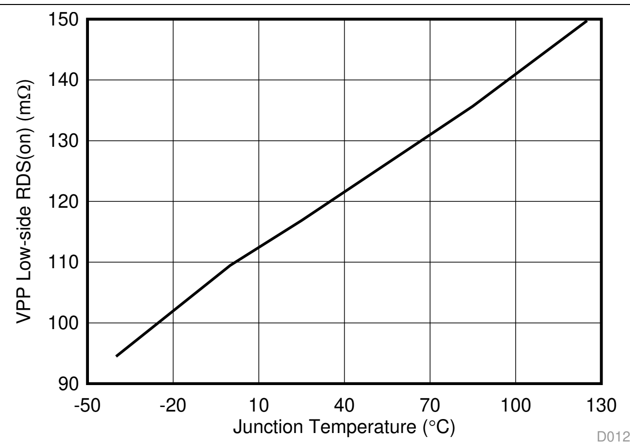



**図 12. VPP Low-Side $R_{DS(on)}$ vs Junction Temperature**

## Typical Characteristics (continued)

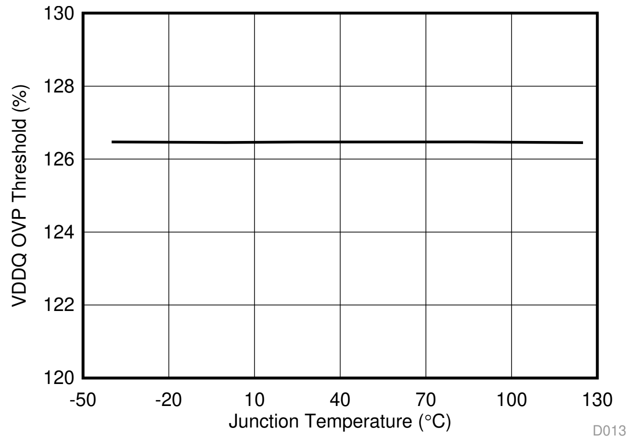



図 13. VDDQ OVP Threshold vs Junction Temperature

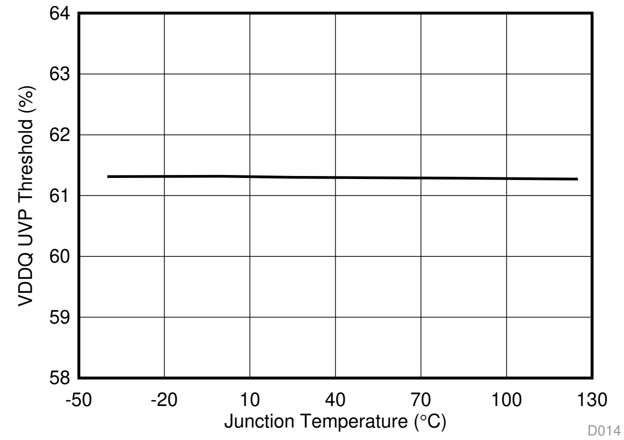



図 14. VDDQ UVP Threshold vs Junction Temperature

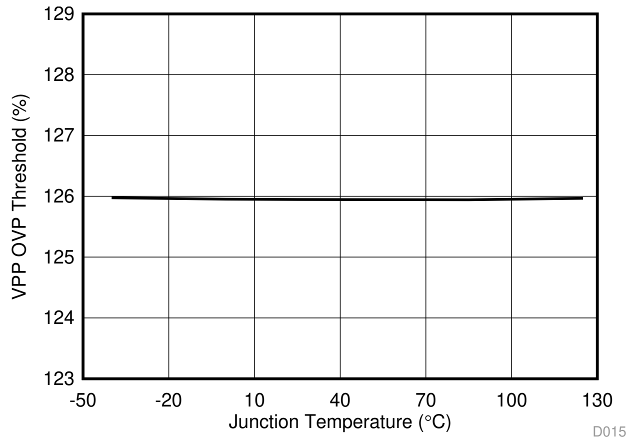



図 15. VPP OVP Threshold vs Junction Temperature

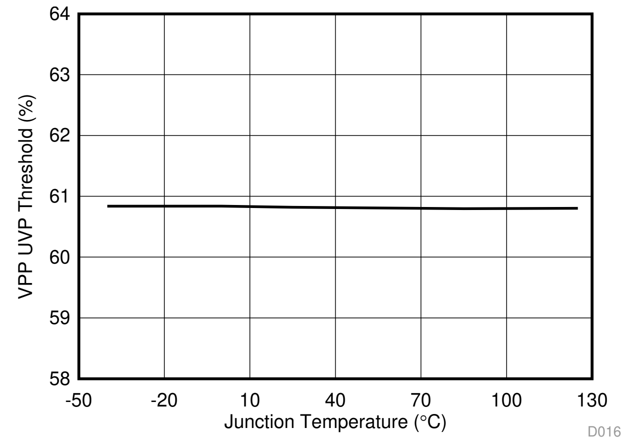



図 16. VPP UVP Threshold vs Junction Temperature

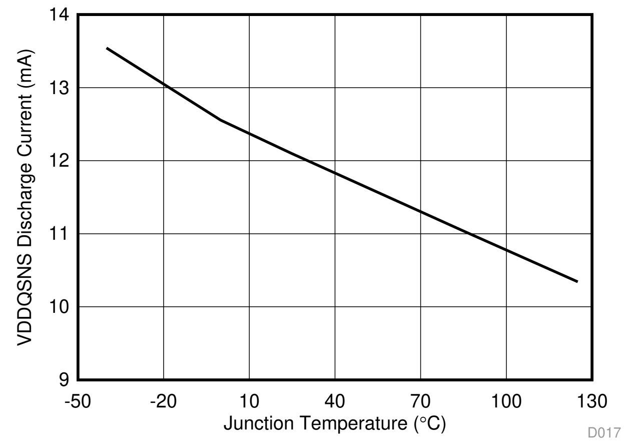



図 17. VDDQSNS Discharge Current vs Junction Temperature

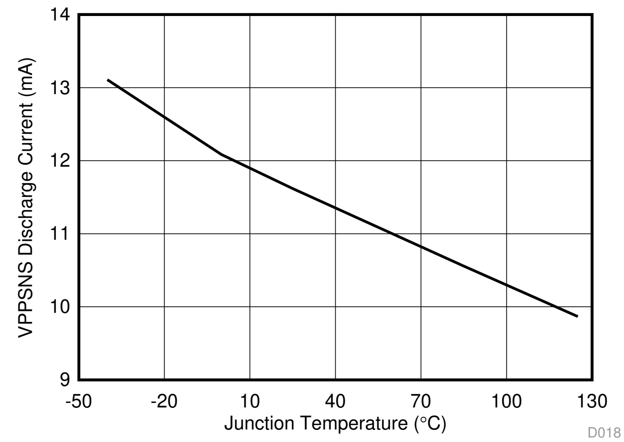



図 18. VPPSNS Discharge Current vs Junction Temperature

## Typical Characteristics (continued)

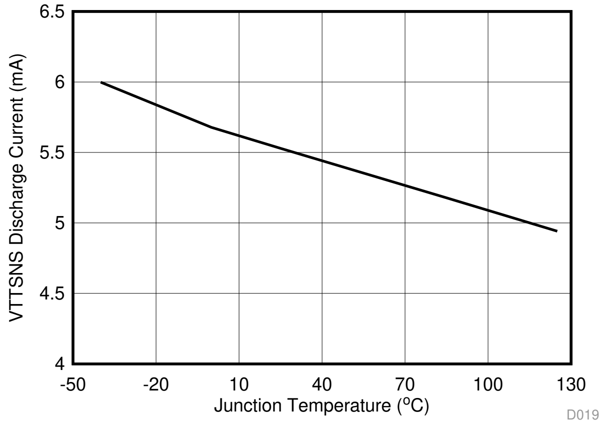



図 19. VTTSNS Discharge Current vs Junction Temperature

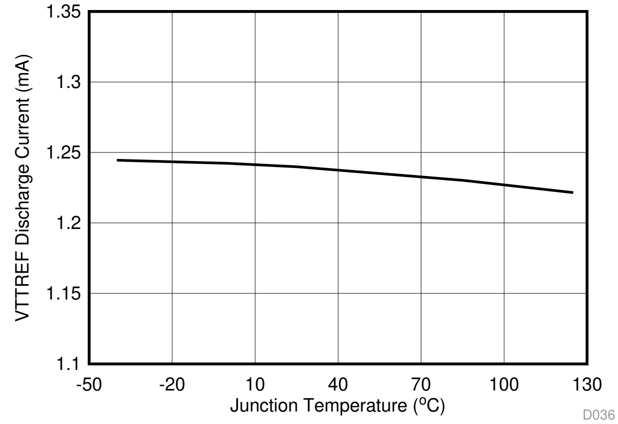



図 20. VTTREF Discharge Current vs Junction Temperature

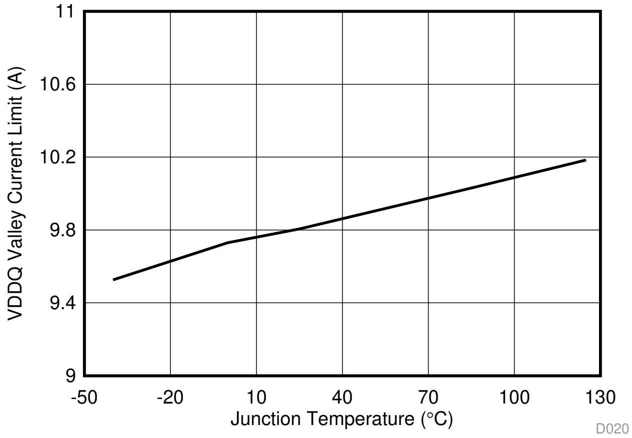



図 21. VDDQ Valley Current Limit vs Junction Temperature

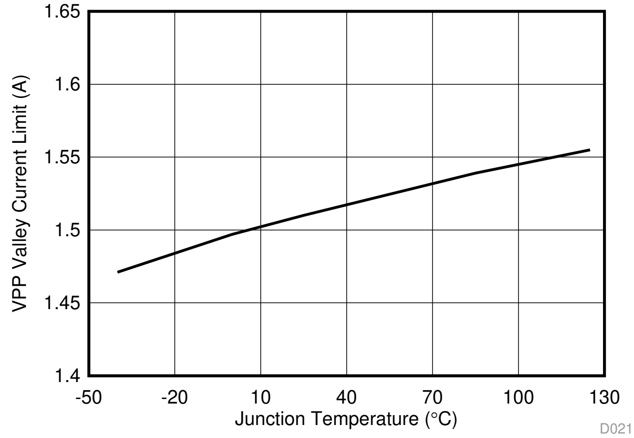



図 22. VPP Valley Current Limit vs Junction Temperature

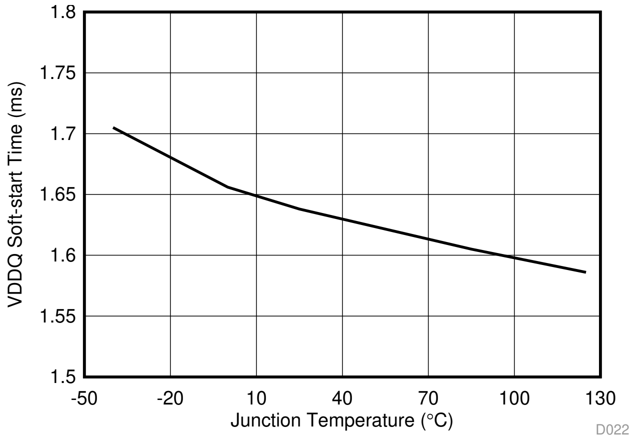



図 23. VDDQ Soft-Start Time vs Junction Temperature

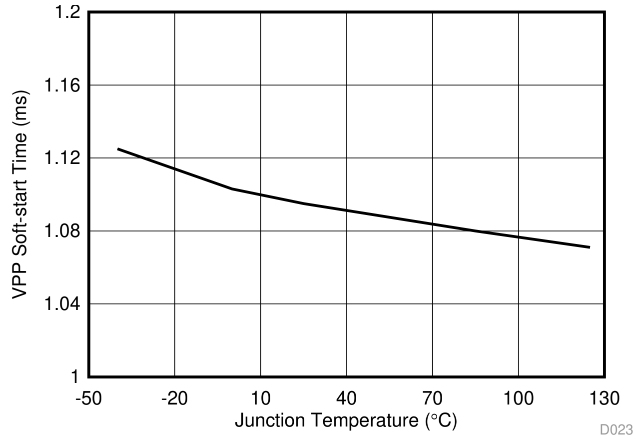
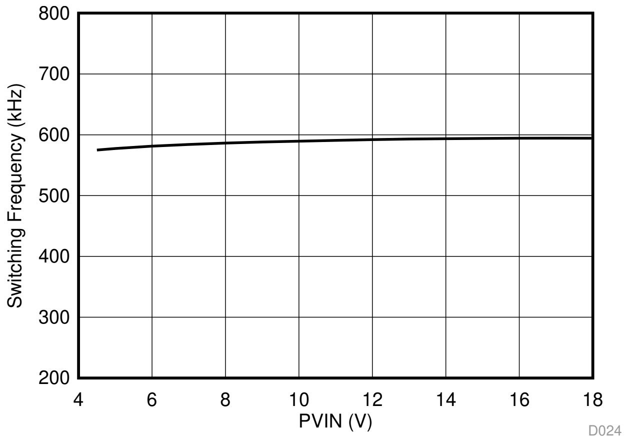


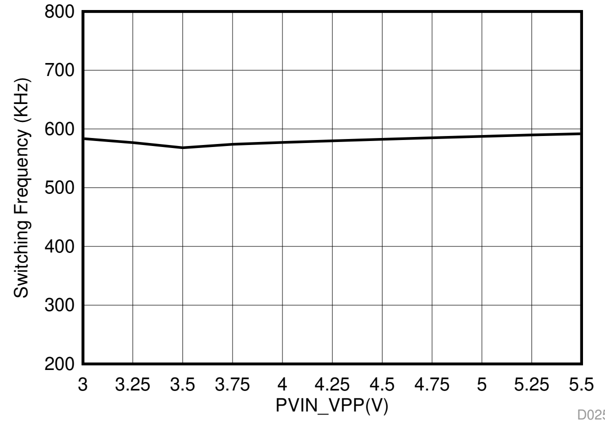

図 24. VPP Soft-Start Time vs Junction Temperature

## Typical Characteristics (continued)




$I_{OUT}$ = 8 A

図 25. VDDQ Switching Frequency vs Input Voltage




$I_{OUT}$ = 1 A

図 26. VPP Switching Frequency vs Input Voltage

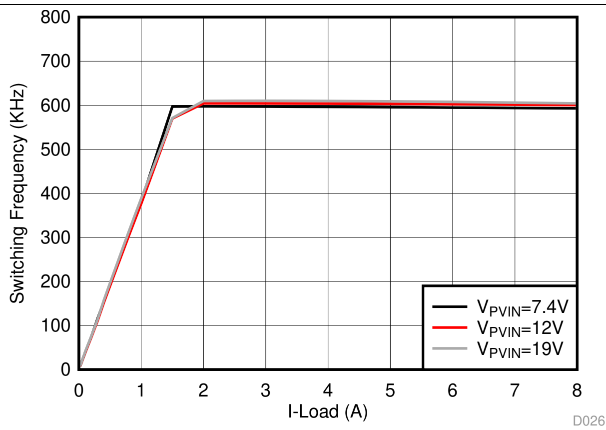



図 27. VDDQ Switching Frequency vs Load Current

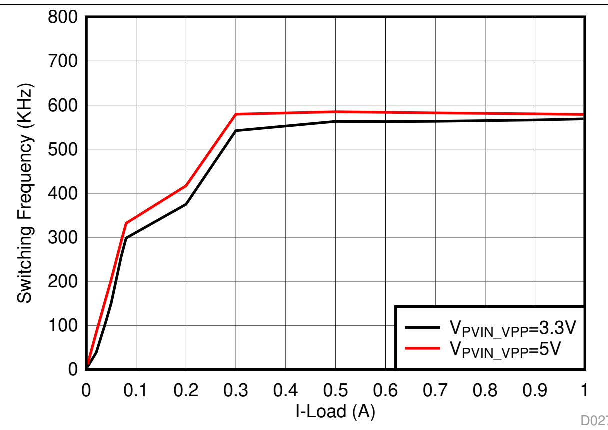


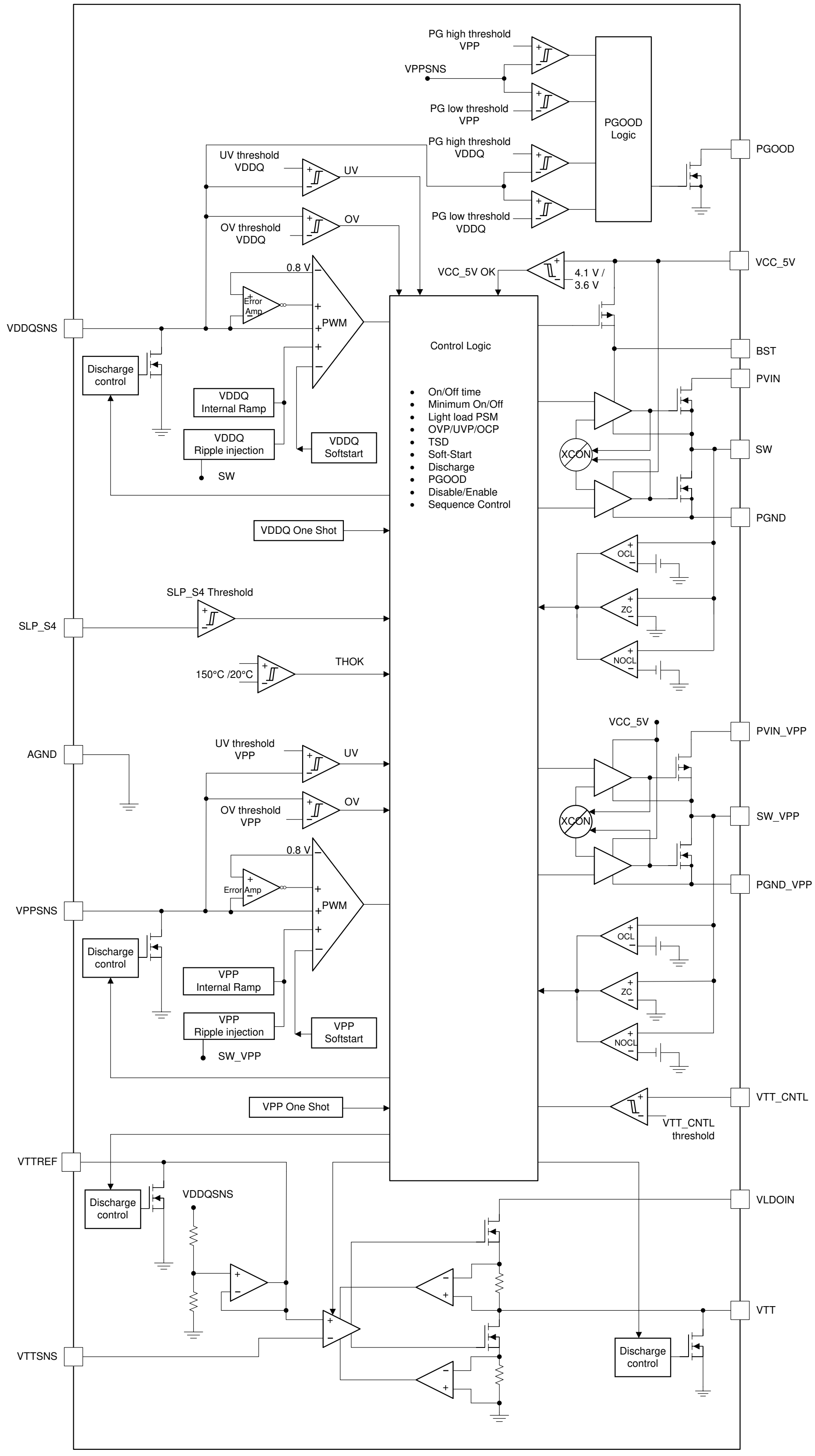

図 28. VPP Switching Frequency vs Load Current

# 8 Detailed Description

## 8.1 Overview

The TPS65295 integrates two synchronous step-down buck converters and two LDOs to support complete DDR4 power solution. The VDDQ buck converter has the fixed 1.2-V output and supports continuous 8-A output current, and it can operate from 4.5-V to 18-V PVIN input voltage. The VPP buck converter has the fixed 2.5-V output and supports continuous 1-A output current, and can operate from 3-V to 5.5-V PVIN_VPP input voltage. The VTTREF LDO tracks the ½ VDDQ output and has about 10-mA both sink and source current capability. The VTT LDO tracks the VTTREF output and has continuous 1-A both sink and source current capability.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 PWM Operation and D-CAP3™ Control

The main control loop of the two bucks is adaptive on-time pulse width modulation (PWM) controller that supports a proprietary DCAP3™ mode control. The DCAP3™ mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output. The TPS65295 also includes an error amplifier that makes the output voltage very accurate.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one-shot timer expires. This one-shot duration is set proportional to the converter input voltage, VIN, and is inversely proportional to the output voltage, VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ripple generation circuit is added to reference voltage for emulating the output ripple, this enables the use of very low-ESR output capacitors such as multi-layered ceramic caps (MLCC). No external current sense network or loop compensation is required for DCAP3™ control topology.

Both VDDQ buck and VPP buck include an error amplifier that makes the output voltage very accurate. For any control topology that is compensated internally, there is a range of the output filter it can support. The output filter used with the TPS65295 is a low-pass L-C circuit. This L-C filter has a double-pole frequency described in 式 1.

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (1)$$

At low frequencies, the overall loop gain is set by the internal output set-point resistor divider network and the internal gain of the TPS65295. The low-frequency L-C double pole has a 180 degree in phase. At the output filter frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40 dB to –20 dB per decade and increases the phase to 90 degree one decade above the zero frequency. The internal ripple injection high-frequency zero is related to the switching frequency. The inductor and capacitor selected for the output filter must be such that the double pole is placed close enough to the high-frequency zero, so that the phase boost provided by this high-frequency zero provides adequate phase margin for the stability requirement. The crossover frequency of the overall system should usually be targeted to be less than one-fifth of the switching frequency ($F_{SW}$).

### 8.3.2 Advanced Eco-mode™ Control

The VDDQ buck and VPP buck are designed with advanced Eco-mode™ control schemes to maintain high light load efficiency. As the output current decreases from heavy load conditions, the inductor current is also reduced and eventually comes to a point where the rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode, so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The light load current where the transition to Eco-mode™ operation happens ( $I_{OUT(LL)}$ ) can be calculated from 式 2.

$$I_{OUT(LL)} = \frac{1}{2 \times L_{OUT} \times F_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (2)$$

After identifying the application requirements, design the output inductance ($L_{OUT}$) so that the inductor peak-to-peak ripple current is approximately between 20% and 30% of the $I_{OUT(max)}$ (peak current in the application). It is also important to size the inductor properly so that the valley current does not hit the negative low-side current limit.

### 8.3.3 Soft Start and Prebiased Soft Start

The VDDQ buck has an internal 1.6-ms soft start and VPP buck has an internal 1-ms soft start. Provide the voltage supply to PVIN, PVIN_VPP and VCC_5V before asserting SLP_S4 to be high, when the SLP_S4 pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator.

## Feature Description (continued)

If the output capacitor is prebiased at start-up, the devices initiate switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage. This scheme ensures that the converters ramp up smoothly into regulation point.

### 8.3.4 Power Good

The Power Good (PGOOD) pin is an open-drain output. Once the VDDQSNS and VPPSNS pins voltage are between 90% and 110% of the target output voltage, the PGOOD is deasserted and floats after a 1-ms de-glitch time. A pullup resistor of 100 kΩ is recommended to pull the voltage up to VCC_5V. The PGOOD pin is pulled low when:

- the VDDQSNS pin voltage or VPPSNS pin voltage is lower than 85% or greater than 115% of the target output voltage
- in an OVP, UVP, or thermal shutdown event
- during the soft-start period.

### 8.3.5 Overcurrent Protection and Undervoltage Protection

Both VDDQ and VPP bucks have the overcurrent protection and undervoltage protection, and the implementation is same. The output overcurrent limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-time of the high-side FET switch, the switch current increases at a linear rate determined by Vin, Vout, the on-time and the output inductor value. During the on-time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current $I_{OUT}$. If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of overcurrent protection. When the load current is higher than the overcurrent threshold by one half of the peak-to-peak inductor ripple current, the OCL is triggered and the current is being limited, the output voltage tends to drop because the load demand is higher than what the converter can support. When the output voltage falls below 60% of the target voltage, the UVP comparator detects it, the output will be discharged and latched after a wait time of 256 µs. When the overcurrent condition is removed, the output voltage is latched till the SLP_S4 is toggled or repower the VCC_5V power input.

### 8.3.6 Overvoltage Protection

Both VDDQ and VPP bucks have the overvoltage protection feature and have the same implementation. When the output voltage becomes higher than 125% of the target voltage, the OVP comparator output goes high, and then the output will be discharged and latched after a wait time of 20 µs. When the over current condition is removed, the output voltage is latched till the SLP_S4 is toggled or repower the VCC_5V power input.

### 8.3.7 UVLO Protection

Undervoltage Lockout protection (UVLO) monitors the VCC_5V power input. When the voltage is lower than UVLO threshold voltage, the device is shut off and outputs are discharged. This is a non-latch protection.

### 8.3.8 Output Voltage Discharge

The VPP buck, VDDQ buck, VTT LDO, and VTTREF LDO block all have the discharge function by using internal MOSFETs, which are connected to the corresponding output terminals VPPSNS, VDDQSNS, VTT, and VTTREF. The discharge is slow due to the lower current capability of these MOSFETs.

### 8.3.9 Thermal Shutdown

The TPS65295 monitors the internal die temperature. If the temperature exceeds the threshold value (typically 150°C), the device is shut off and the output will be discharged. This is a non-latch protection. The device restarts switching when the temperature goes below the thermal shutdown recover threshold.

## 8.4 Device Functional Modes

### 8.4.1 Light Load Operation for VDDQ Buck and VPP Buck

When the load is light on the VDDQ or VPP output, the buck enters pulse skip mode after the inductor current crosses zero. This is the Eco-mode™ which improves the efficiency at light load with a lower switching frequency. Each switching cycle is followed by a period of energy saving sleep time. The sleep time ends when the VDDQSNS or VPPSNS voltage falls below the Eco-mode™ threshold voltage. As the output current decreases, the period time between switching pulses increases.

### 8.4.2 Output State Control

The TPS65295 has two enable input pins, SLP_S4 and VTT_CNTL, to provide simple control scheme of output state. All of VPP, VDDQ, VTTREF and VTT are turned on at S0 state (SLP_S4=VTT_CNTL=high). In S3 state (VTT_CNTL=low, SLP_S4=high), VPP, VDDQ, and VTTREF voltages are kept on while VTT is turned off and left at high impedance state (high-Z). The VTT output floats and does not sink or source current in this state. In S4/S5 states (SLP_S4=VTT_CNTL =low), all of the three outputs are turned off and discharged to GND. Each state code represents as follow: S0 = full ON, S3 = suspend to RAM (STR), S4 = suspend to disk (STD), S5 = soft OFF (see 表 1).

**表 1. VTT_CNTL and SLP_S4 Control for Output State**

| STATE | VTT_CNTL | SLP_S4 | VPP | VDDQ | VTTREF | VTT |
|---|---|---|---|---|---|---|
| S0 | HI | HI | ON | ON | ON | ON |
| S3 | LO | HI | ON | ON | ON | OFF (High-Z) |
| S5/S4 | LO | LO | OFF (discharge) | OFF (discharge) | OFF (discharge) | OFF (discharge) |

### 8.4.3 Output Sequence Control

There are specific sequencing requirements for the DDR4 VDDQ and VPP rails. The TPS65295 follows the DDR4 power rail sequence requirements as shown in 図 29 and 図 30. VPP is greater than VDDQ at all times during ramp up, operating, and ramp down. The VTT output ramp and stable within 35 µs after VTT_CNTL asserted.

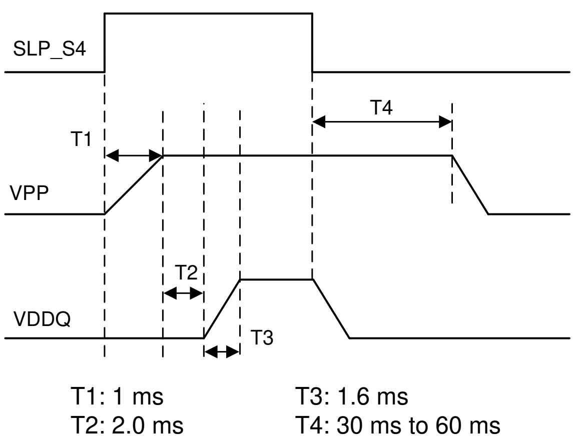



**図 29. Power Sequence, VPP and VDDQ vs SLP_S4**

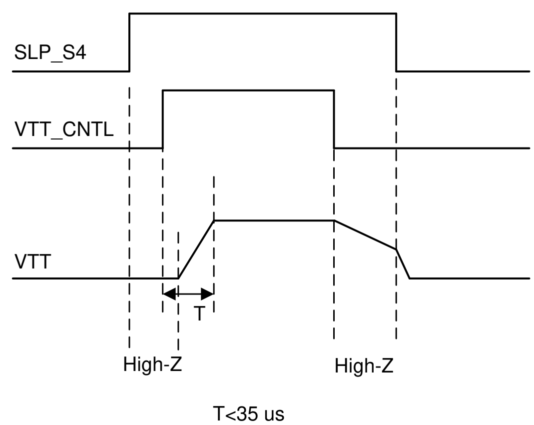



**図 30. Power Sequence, VTT vs VTT_CNTL**

# 9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The schematic of 図 31 shows a typical application for TPS65295. For VDDQ buck, the PVIN supports 4.5-V to 18-V input range with 1.2-V VDDQ output, the continuous current capability is 8 A. Usually the PVIN_VPP and VCC_5V can share one 5-V power input and supports 2.5-V VPP output with 1-A continuous current capability, of course the PVIN_VPP can be lowered down to a 3.3-V power supply. The VLDOIN power input usually is connected to VDDQ output, while also it can be connected to external 1.2-V power supply input. The VTTREF output voltage will follow the ½ VDDQSNS voltage, and VTT output voltage will follow the VTTREF output voltage, this is required by DDR4 power supply standard.

## 9.2 Typical Application

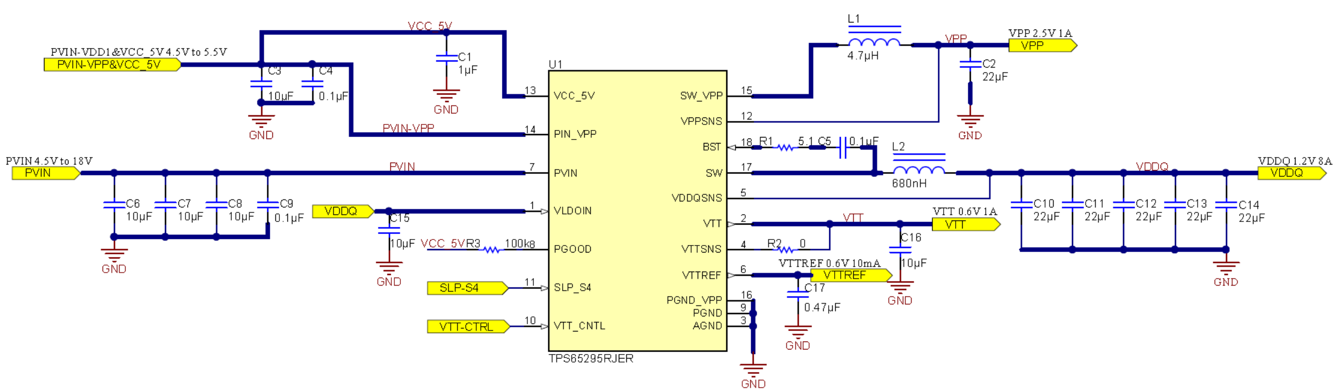



図 31. Application Schematic

### 9.2.1 Design Requirements

表 2 lists the design parameters for this example.

表 2. Design Parameters

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **VDDQ OUTPUT** | | | | | | |
| $V_{OUT}$ | Output voltage | | | 1.2 | | V |
| $I_{OUT}$ | Output current | | | 8 | | A |
| $\Delta V_{OUT}$ | Transient response | 8-A load step | | ±60 | | mV |
| $V_{IN}$ | Input voltage | | 4.5 | 12 | 18 | V |
| $V_{OUT(ripple)}$ | Output voltage ripple | | | 40 | | $mV_{(P-P)}$ |
| $F_{SW}$ | Switching frequency | | | 600 | | kHz |
| **VPP OUTPUT** | | | | | | |
| $V_{OUT}$ | Output voltage | | | 2.5 | | V |
| $I_{OUT}$ | Output current | | | 1 | | A |
| $\Delta V_{OUT}$ | Transient response | 1-A load step | | ±125 | | mV |
| $V_{IN}$ | Input voltage | | 3 | 5 | 5.5 | V |

## Typical Application (continued)

**表 2. Design Parameters (continued)**

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OUT(ripple)}$ | Output voltage ripple | | | 40 | | $mV_{(P-P)}$ |
| $F_{SW}$ | Switching frequency | | | 580 | | kHz |
| **OTHERS** | | | | | | |
| $V_{VCC\_5V}$ | Start VCC_5V input voltage | VCC_5V Input voltage rising | | Internal UVLO | | V |
| | Stop VCC_5V input voltage | VCC_5V Input voltage falling | | Internal UVLO | | V |
| | Light load operating mode | | | ECO | | |
| $T_A$ | Ambient temperature | | | 25 | | °C |

### 9.2.2 Detailed Design Procedure

#### *9.2.2.1 External Component Selection*

##### 9.2.2.1.1 Inductor Selection

The inductor ripple current is filtered by the output capacitor. A higher inductor ripple current means the output capacitor should have a ripple current rating higher than the inductor ripple current. See 表 3 for recommended inductor values.

The RMS and peak currents through the inductor can be calculated using 式 3 and 式 4. It is important that the inductor is rated to handle these currents.

$$I_{L(rms)} = \sqrt{\left(I_{OUT}^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{V_{IN(max)} \times L_{OUT} \times F_{SW}}\right)^2\right)} \tag{3}$$

$$I_{L(peak)} = I_{OUT} + \frac{I_{OUT(ripple)}}{2} \tag{4}$$

During transient and short-circuit conditions, the inductor current can increase up to the current limit of the device so it is safe to choose an inductor with a saturation current higher than the peak current under current limit condition.

##### 9.2.2.1.2 Output Capacitor Selection

After selecting the inductor the output capacitor needs to be optimized. In DCAP3, the regulator reacts within one cycle to the change in the duty cycle so the good transient performance can be achieved without needing large amounts of output capacitance. The recommended output capacitance range is given in 表 3.

Ceramic capacitors have very low ESR, otherwise the maximum ESR of the capacitor should be less than $V_{OUT(ripple)}/I_{OUT(ripple)}$.

**表 3. Recommended Component Values**

| $V_{OUT}$ (V) | $F_{SW}$ (kHz) | $L_{OUT}$ (µH) | $C_{OUT(min)}$ (µF) | $C_{OUT(max)}$ (µF) |
|---|---|---|---|---|
| 1.2 | 600 | 0.68 | 88 | 132 |
| | 600 | 0.56 | 88 | 132 |
| | 600 | 0.47 | 88 | 132 |
| 2.5 | 580 | 6.8 | 20 | 66 |
| | 580 | 4.7 | 20 | 66 |
| | 580 | 3.3 | 20 | 66 |

For VTT output, high quality X5R or X7R 10-µF capacitor is recommended and a 0.47 µF is recommended for VTTREF output.

#### 9.2.2.1.3 Input Capacitor Selection

The TPS65295 requires input decoupling capacitors on both power supply input PVIN and PVIN_VPP, and the bulk capacitors are needed depending on the application. The minimum input capacitance required is given in 式 5.

$$C_{IN(min)} = \frac{I_{OUT} \times V_{OUT}}{V_{INripple} \times V_{IN} \times F_{SW}} \quad (5)$$

TI recommends using a high-quality X5R or X7R input decoupling capacitors of 30 µF on the VDDQ buck input voltage pin PVIN, and 10 µF on the VPP buck input voltage pin PVIN_VPP. The voltage rating on the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the application. The input ripple current is calculated by 式 6:

$$I_{CIN(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{(V_{IN(min)} - V_{OUT})}{V_{IN(min)}}} \quad (6)$$

An additional 0.1-µF capacitor from PVIN to ground and from PVIN_VPP to ground is optional to provide additional high frequency filtering. One ceramic capacitor of 10 µF is recommended for the decoupling capacitor on VLDOIN pin for providing stable power on VTT LDO block. A 1-µF ceramic capacitor is needed for the decoupling capacitor on VCC_5V input.

#### 9.2.2.1.4 Bootstrap Capacitor and Resistor Selection

A 0.1-µF ceramic capacitor serialized with a 5.1-Ω resistor is recommended between the BST and SW pin for proper operation. TI recommends using a ceramic capacitor.

### 9.2.3 Application Curves

図 32 through 図 60 apply to the circuit of 図 31. $V_{IN}$ = 12 V. $T_A$ = 25°C unless otherwise specified.

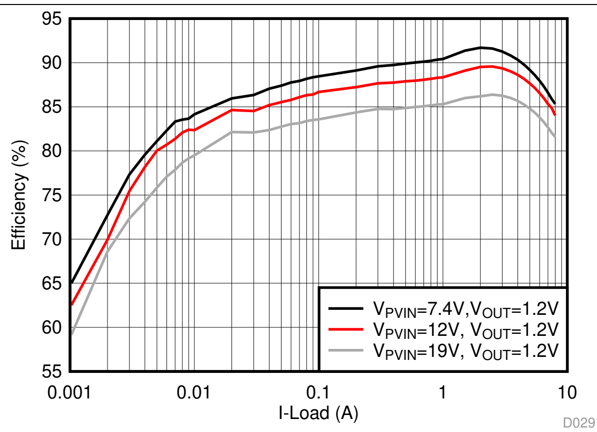



図 32. VDDQ Efficiency Curve, $V_{OUT}$ = 1.2 V

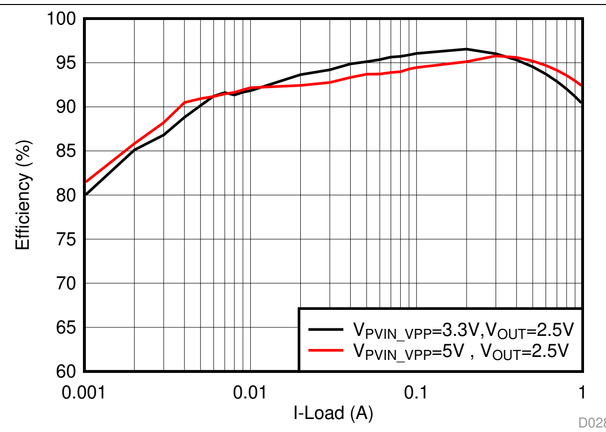



図 33. VPP Efficiency Curve, $V_{OUT}$ = 2.5 V

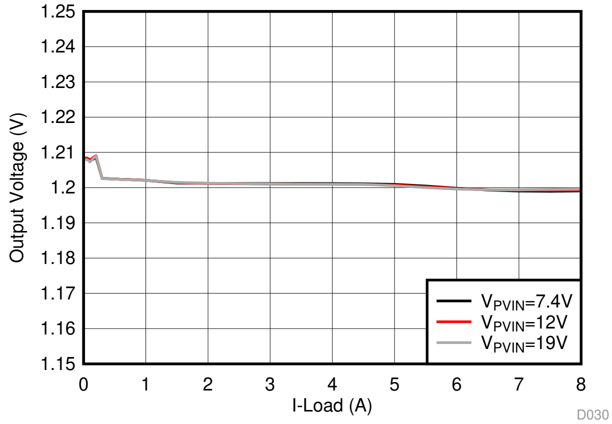



図 34. VDDQ Load Regulation, $V_{OUT}$ = 1.2 V

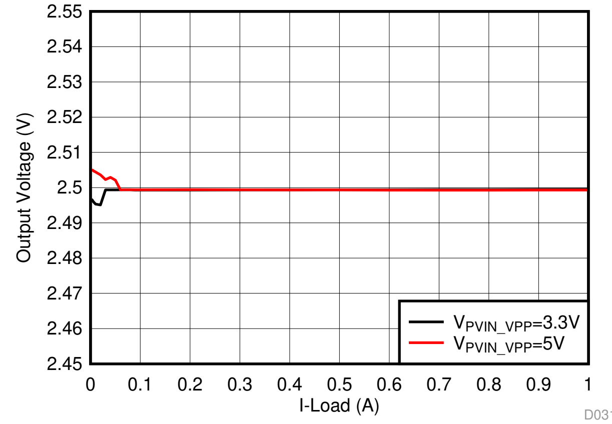



図 35. VPP Load Regulation, $V_{OUT}$ = 2.5 V

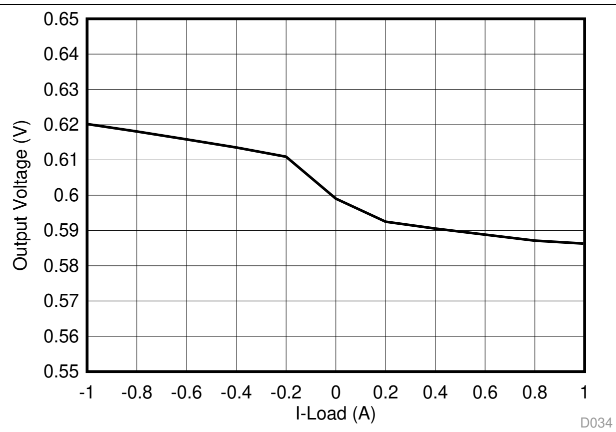



図 36. VTT Load Regulation, $V_{OUT}$ = 0.6 V

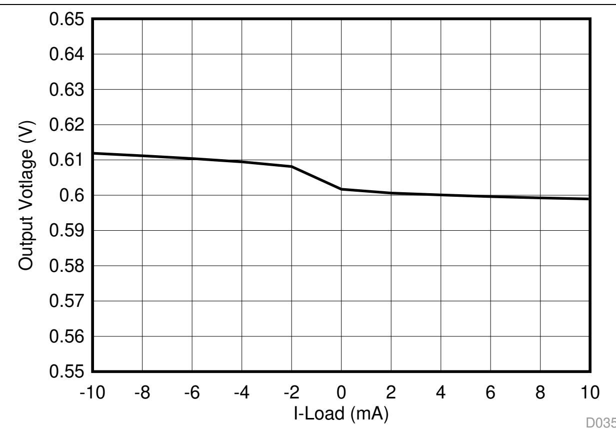



図 37. VTTREF Load Regulation, $V_{OUT}$ = 0.6 V

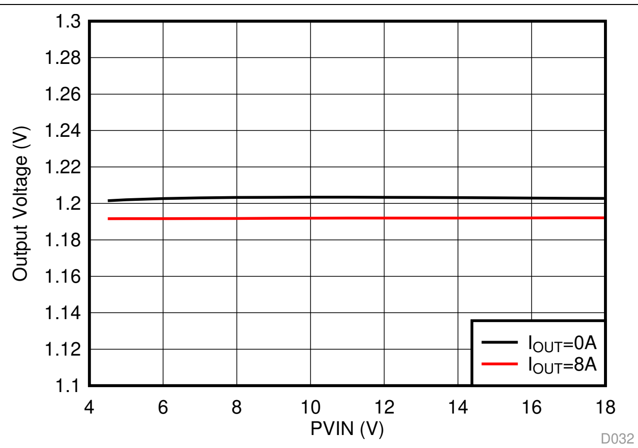



図 38. VDDQ Line Regulation,$V_{OUT}$ = 1.2 V

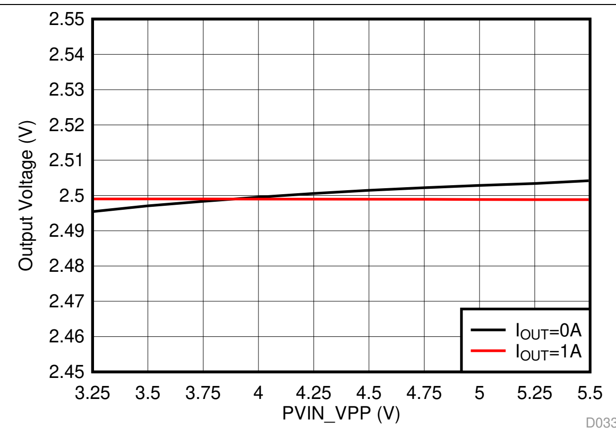



図 39. VPP Line Regulation, $V_{OUT}$ = 2.5 V

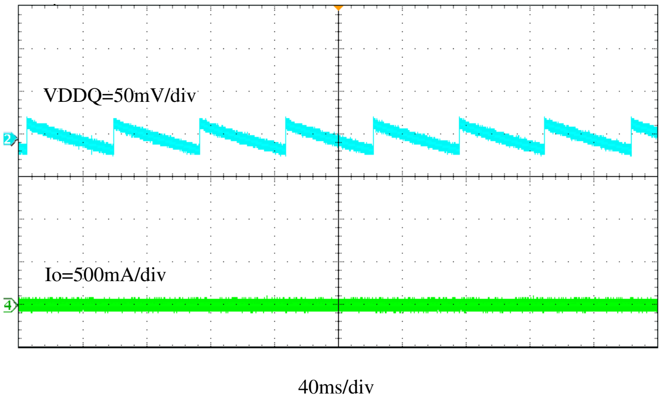



**図 40. VDDQ Output Voltage Ripple, $I_{OUT}$ = 0 A**

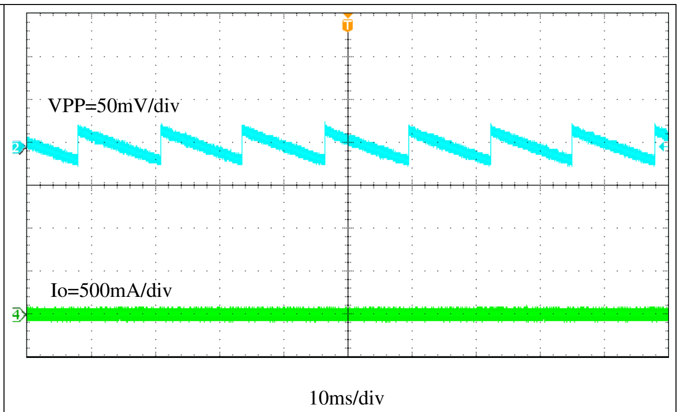



**図 41. VPP Output Voltage Ripple, $I_{OUT}$ = 0 A**

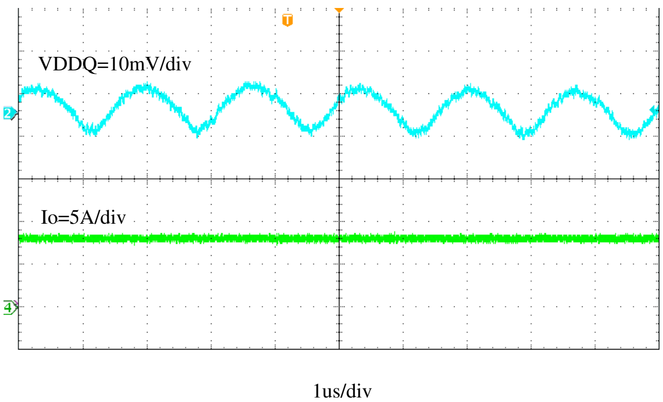



**図 42. VDDQ Output Voltage Ripple, $I_{OUT}$ = 8 A**

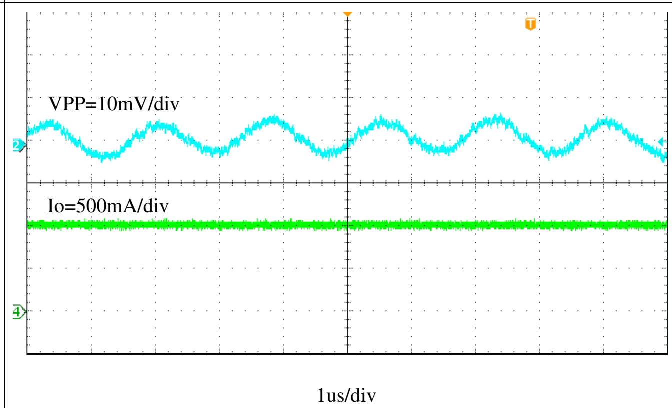



**図 43. VPP Output Voltage Ripple, $I_{OUT}$ = 1 A**

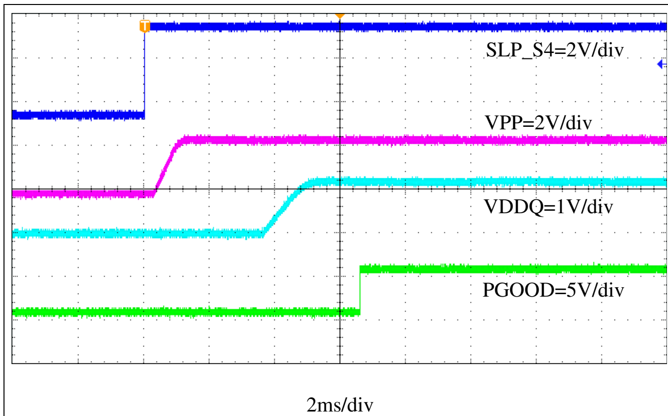



**図 44. Start-Up Through SLP_S4, $I_{VPPOUT}$ = 0 A, $I_{VDDQOUT}$ = 0 A**

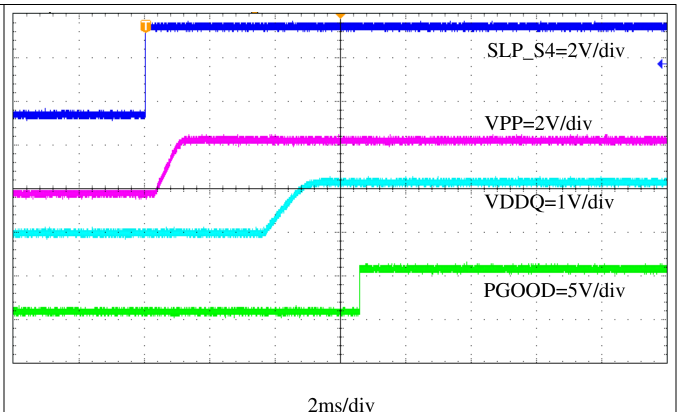



**図 45. Start-Up Through SLP_S4, $I_{VPPOUT}$ = 1 A, $I_{VDDQOUT}$ = 8 A**

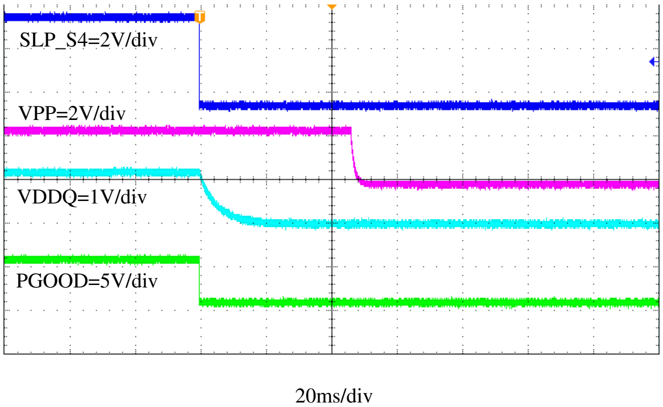



**図 46. Shutdown Through SLP_S4, $I_{VPPOUT}$ = 0 A, $I_{VDDQOUT}$ = 0 A**

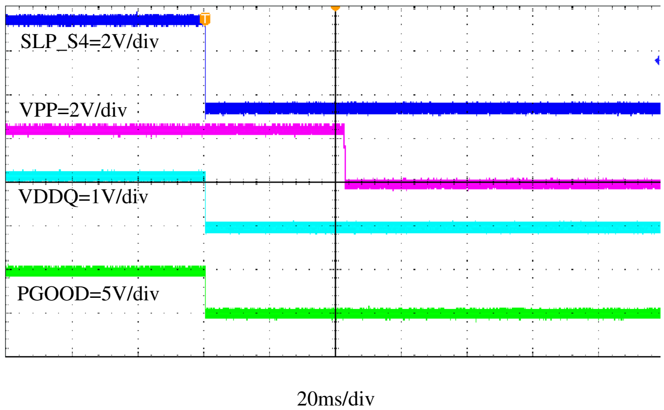
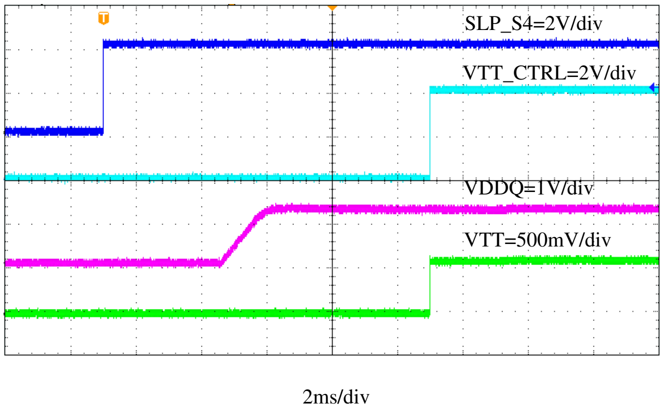
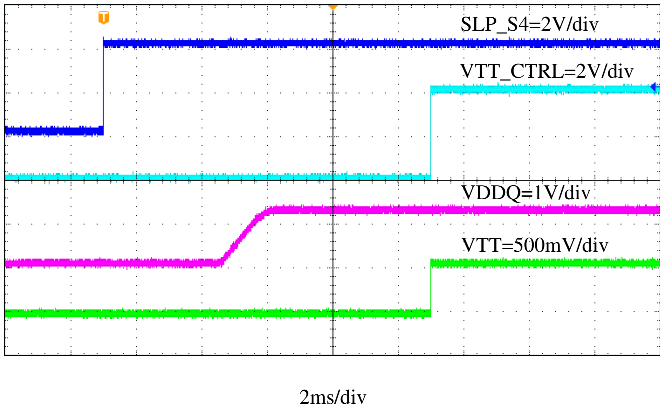



**図 47. Shutdown Through SLP_S4, $I_{VPPOUT}$ = 1 A, $I_{VDDQOUT}$ = 8 A**



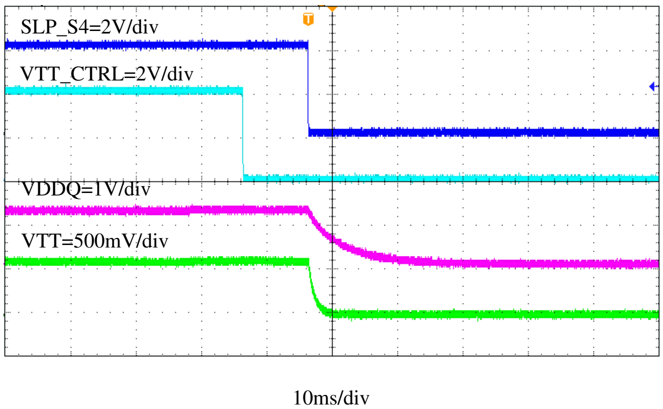

$I_{VDDQOUT}$ = 0 A $I_{VTT}$ = 0 A $I_{VTTREF}$ = 0 A

**図 48. VTT Start-Up Through VTT_CNTL**



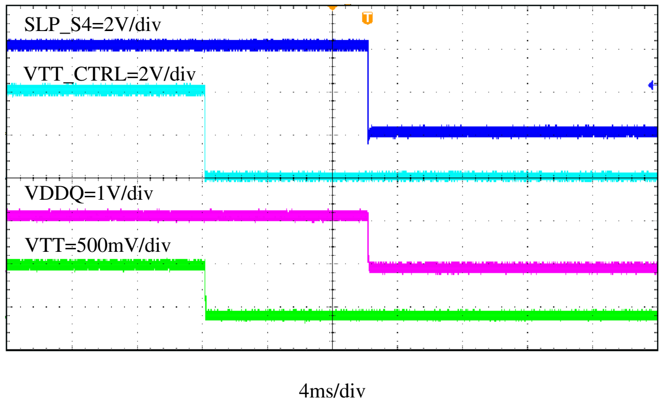

$I_{VDDQOUT}$ = 8 A $I_{VTT}$ = 1 A $I_{VTTREF}$ = 10m A

**図 49. VTT Start-Up Through VTT_CNTL**



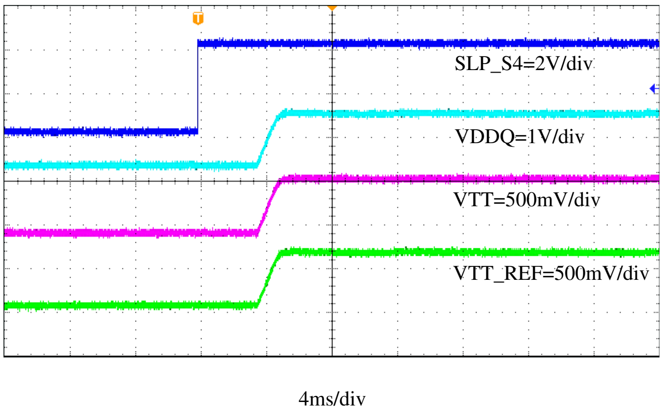

$I_{VDDQOUT}$ = 0 A $I_{VTT}$ = 0 A $I_{VTTREF}$ = 0 A

**図 50. VTT Shutdown Through VTT_CNTL**



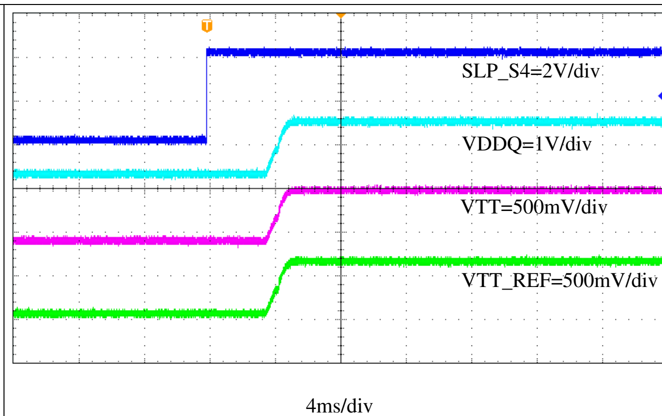

$I_{VDDQOUT}$ = 8 A $I_{VTT}$ = 1 A $I_{VTTREF}$ = 10 mA

**図 51. VTT Shutdown Through VTT_CNTL**



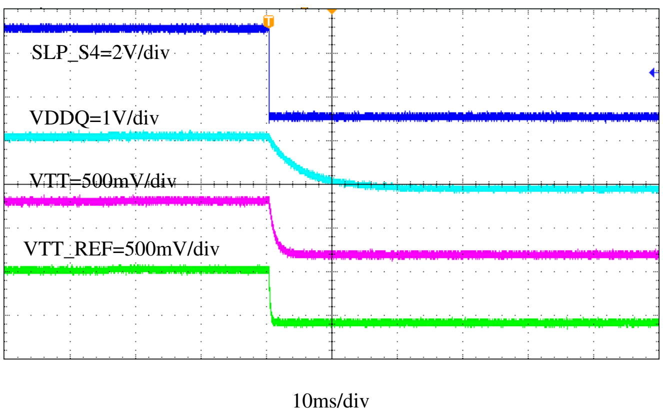

$I_{VDDQOUT}$ = 0 A $I_{VTT}$ = 0 A $I_{VTTREF}$ = 0 A

**図 52. VTT Start-Up Through SLP_S4**



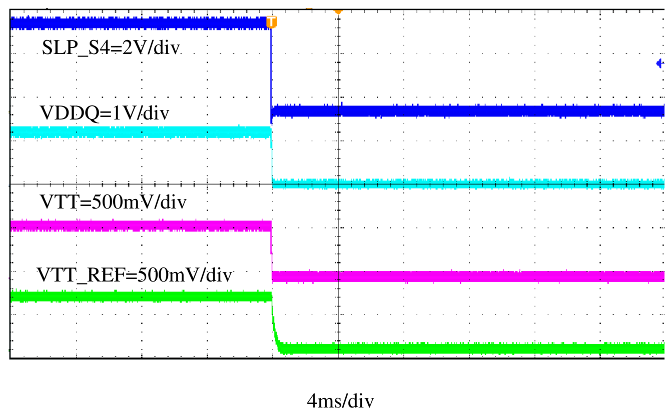

$I_{VDDQOUT}$ = 8 A $I_{VTT}$ = 1 A $I_{VTTREF}$ = 10 mA

**図 53. VTT Start-Up Through SLP_S4**



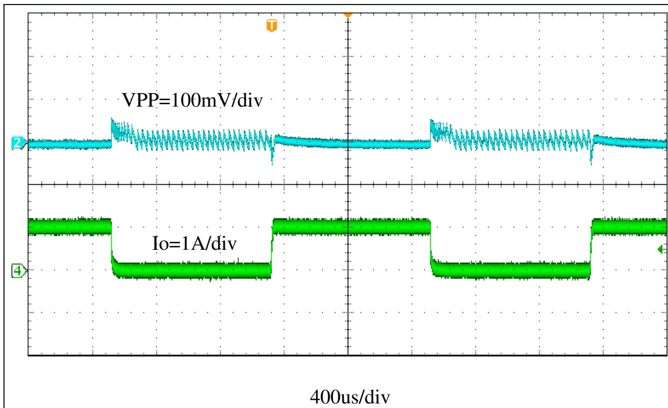

$I_{VDDQOUT}$ = 0 A $I_{VTT}$ = 0 A $I_{VTTREF}$ = 0 A

**図 54. VTT Shutdown Through SLP_S4**



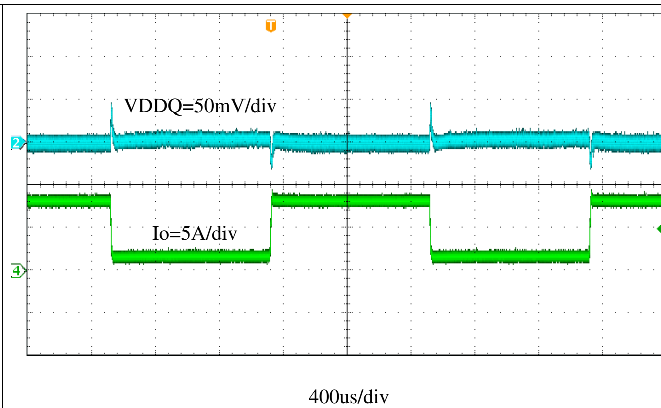

$I_{VDDQOUT}$ = 8 A $I_{VTT}$ = 1 A $I_{VTTREF}$ = 10 mA

**図 55. VTT Shutdown Through SLP_S4**




Slew Rate=2.5A/us

**図 56. VPP Transient Response, 0 A to 1 A**




Slew Rate=2.5A/us

**図 57. VDDQ Transient Response, 1.6 A to 8 A**

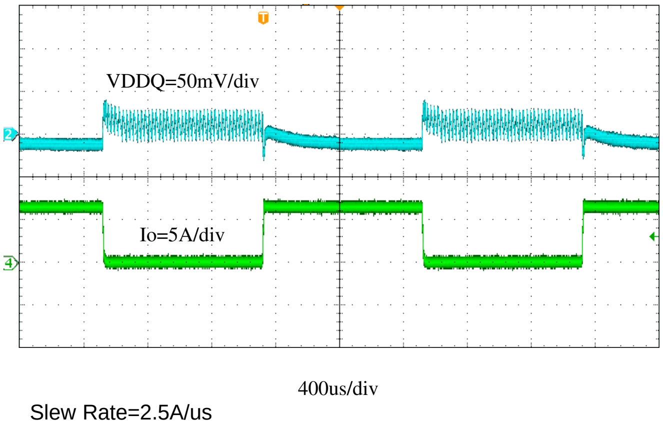



図 58. VDDQ Transient Response, 0.1 A to 6.4 A

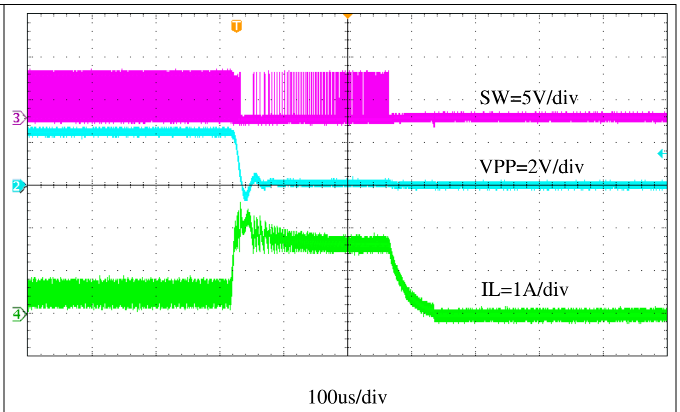



図 59. VPP Normal Operation to Output Hard Short

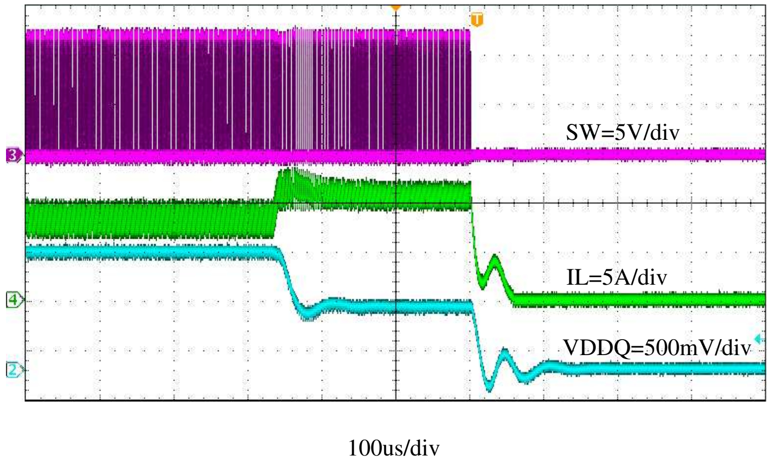



図 60. VDDQ Normal Operation to Output Hard Short

## 10 Power Supply Recommendations

TPS65295 is designed for DDR4 complete power solution. PVIN is the power input for VDDQ buck, PVIN_VPP is the power input for VPP buck, VLDOIN input is for VTT LDO power supply, VCC_5V is power supply for internal control logic. Below lists the power on sequence scenarios.

- SLP_S4 is high before PVIN or PVIN_VPP has the power input, VCC_5V power supply must be provided after or same time with PVIN or PVIN_VPP, otherwise the output will be latched, this latch can be recovered by toggling the SLP_S4 pin or re-power the VCC_5V
- SLP_S4 is low before PVIN and PVIN_VPP has the power input, then there is no power supply input sequence requirement for VCC_5V, PVIN and PVIN_VPP.

# 11 Layout

## 11.1 Layout Guidelines

- Recommend a four-layer PCB for good thermal performance and with maximum ground plane. 3-inch × 3-inch, four-layer PCB with 2-oz. copper used as example.
- Place the decoupling capacitors right across PVIN, PVIN_VPP, and VLDOIN as close as possible.
- Place output inductors and capacitors with IC at the same layer, SW routing should be as short as possible to minimize EMI, and should be a width plane to carry big current, enough vias should be added to the PGND connection of output capacitor and also as close to the output pin as possible. Reserve some space between VDDQ choke and VPP choke, just minimize radiation crosstalk.
- Place BST resistor and capacitor with IC at the same layer, close to BST and SW plane, >15 mil width trace is recommended to reduce line parasitic inductance.
- VPPSNS/VDDQSNS/VTTSNS could be 10 mil and must be routed away from the switching node, BST node or other high efficiency signal.
- PVIN and PVIN_VPP trace must be wide to reduce the trace impedance and provide enough current capability.
- Output capacitors for VTT and VTTREF should be put as close as output pin.

## 11.2 Layout Example

図 61 shows the recommended top-side layout. Component reference designators are the same as the circuit shown in 図 31.

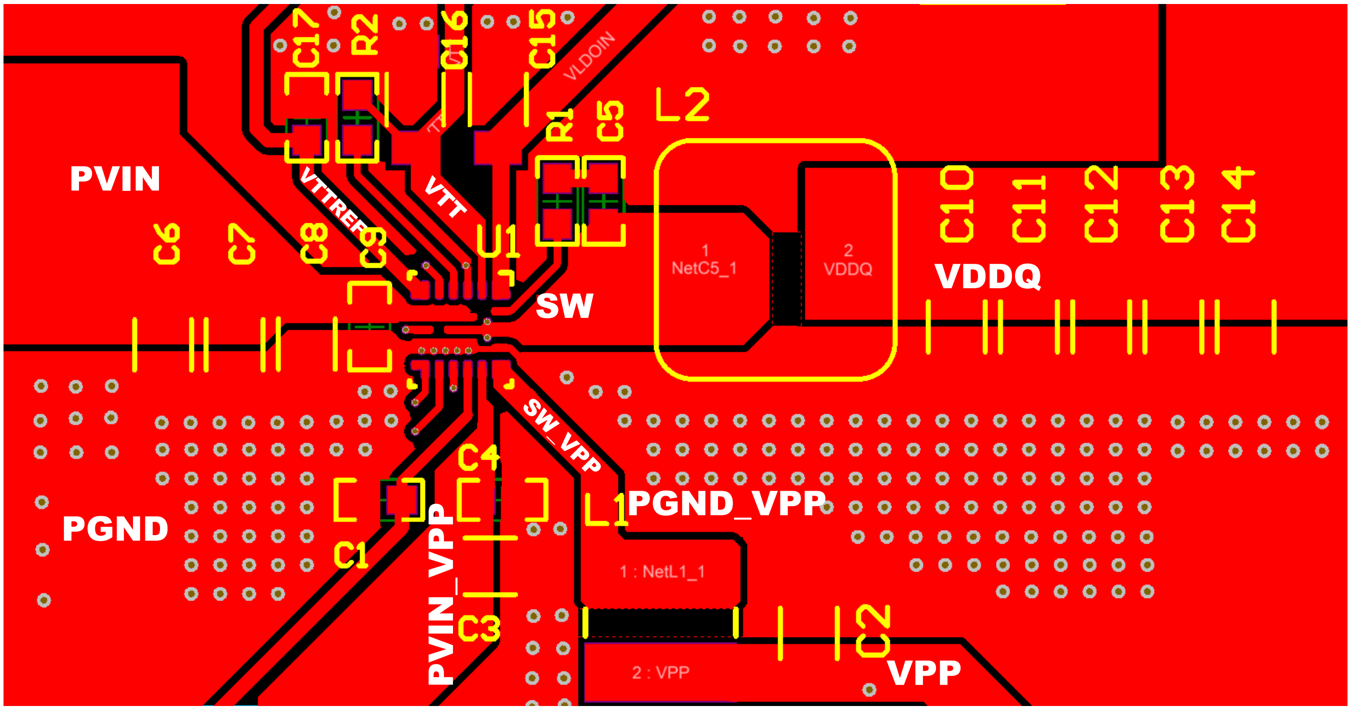



**図 61. Top-Side Layout**

# 12 デバイスおよびドキュメントのサポート

## 12.1 デバイス・サポート

### 12.1.1 デベロッパー・ネットワークの製品に関する免責事項

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## 12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.4 商標

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All other trademarks are the property of their respective owners.

## 12.5 静電気放電に関する注意事項

これらのデバイスは、限定的なESD(静電破壊)保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

## 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

## 13.1 Package Option Addendum

### 13.1.1 Packaging Information

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish(3) | MSL Peak Temp (4) | Op Temp (°C) | Device Marking(5)(6) |
|---|---|---|---|---|---|---|---|---|---|---|
| TPS65295RJER | PRE_PROD | VQFN-HR | RJE | 18 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 65295 |
| TPS65295RJET | PRE_PROD | VQFN-HR | RJE | 18 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 65295 |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PRE_PROD** Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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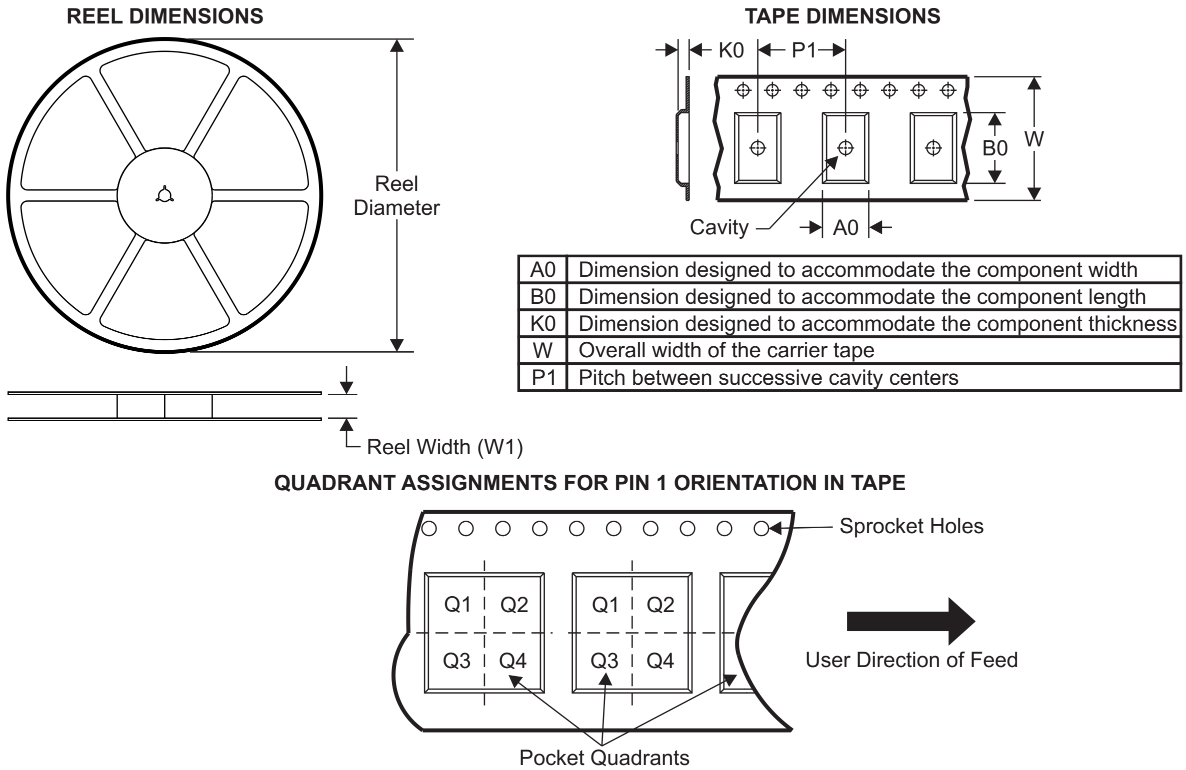
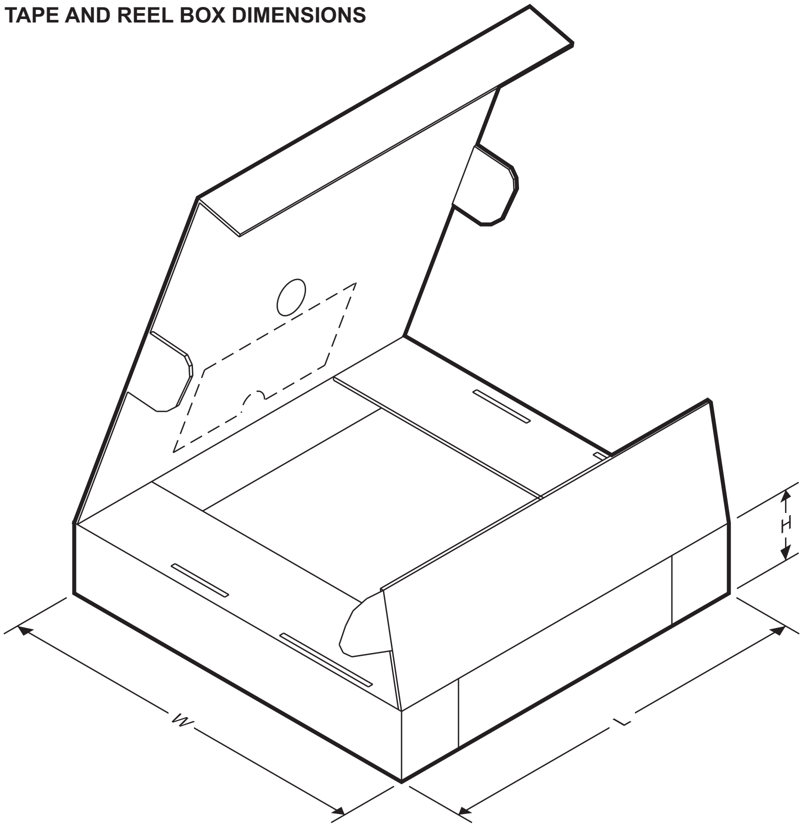
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

### 13.1.2 Tape and Reel Information




| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS65295RJER | VQFN-HR | RJE | 18 | 3000 | 330 | 12.4 | 3.3 | 3.3 | 1.1 | 8 | 12 | Q2 |
| TPS65295RJET | VQFN-HR | RJE | 18 | 250 | 180 | 12.4 | 3.3 | 3.3 | 1.1 | 8 | 12 | Q2 |

**TAPE AND REEL BOX DIMENSIONS**



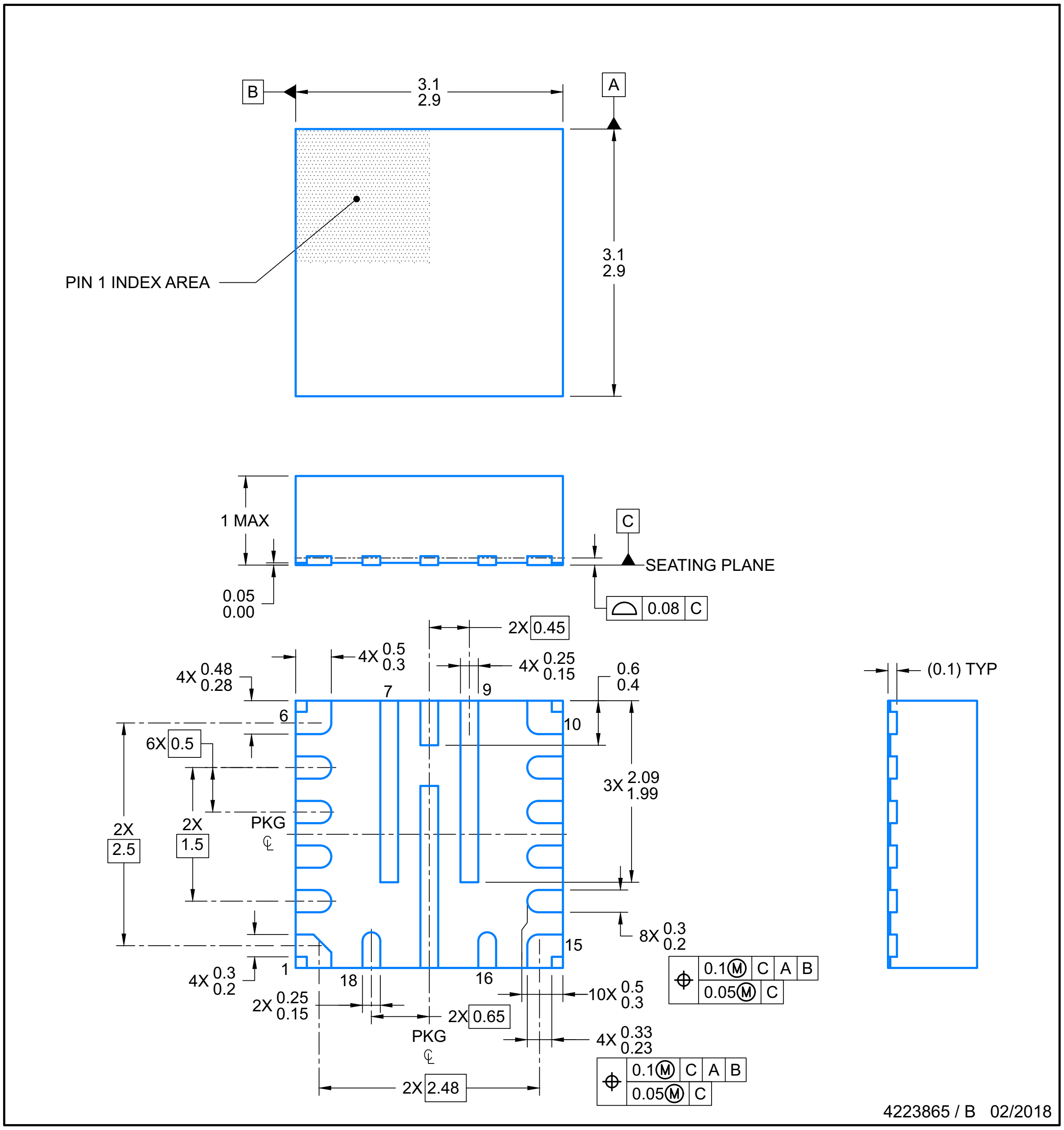

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS65295RJER | VQFN-HR | RJE | 18 | 3000 | 367 | 367 | 35 |
| TPS65295RJET | VQFN-HR | RJE | 18 | 250 | 210 | 185 | 35 |

# PACKAGE OUTLINE

## RJE0018B

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD




NOTES:

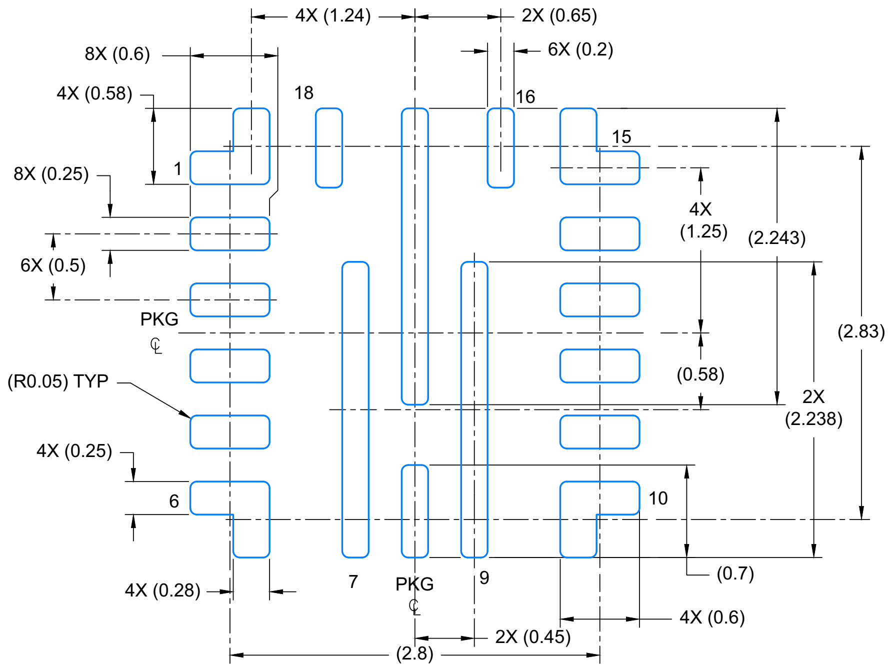
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

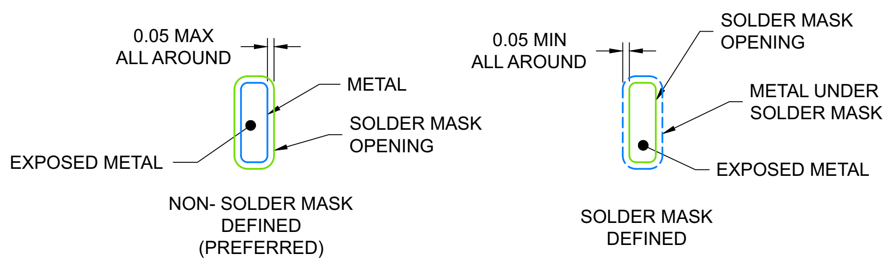
## RJE0018B

### VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X




SOLDER MASK DETAILS

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NOTES: (continued)

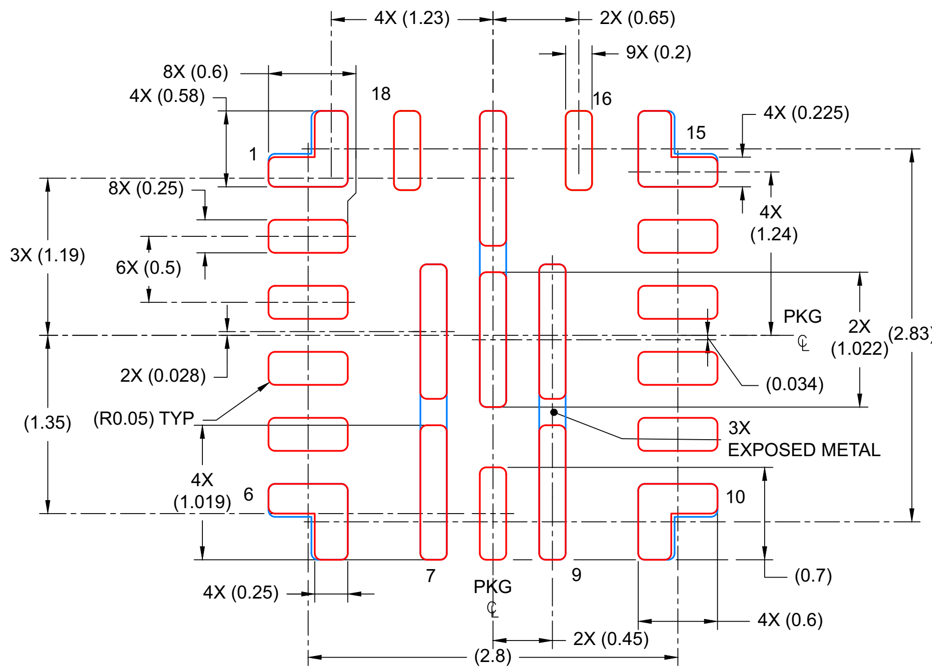
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## RJE0018B

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1, 6, 10 &15: 93% & PADS 7-9,17:89%
SCALE: 20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS65295RJER | ACTIVE | VQFN-HR | RJE | 18 | 3000 | RoHS & Green | Call TI \| SN \| NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 65295 | Samples |
| TPS65295RJET | ACTIVE | VQFN-HR | RJE | 18 | 250 | RoHS & Green | Call TI \| SN \| NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 65295 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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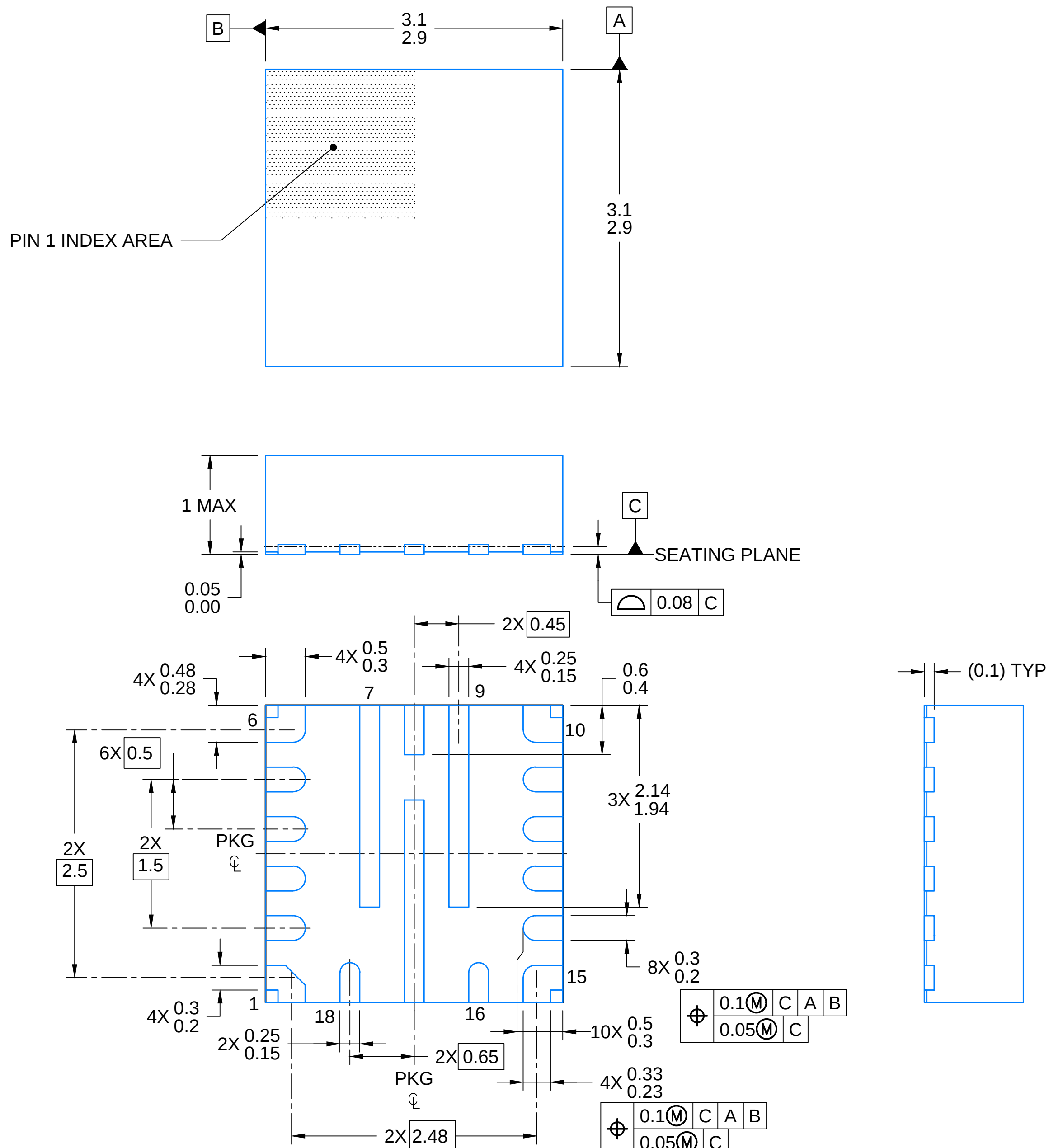


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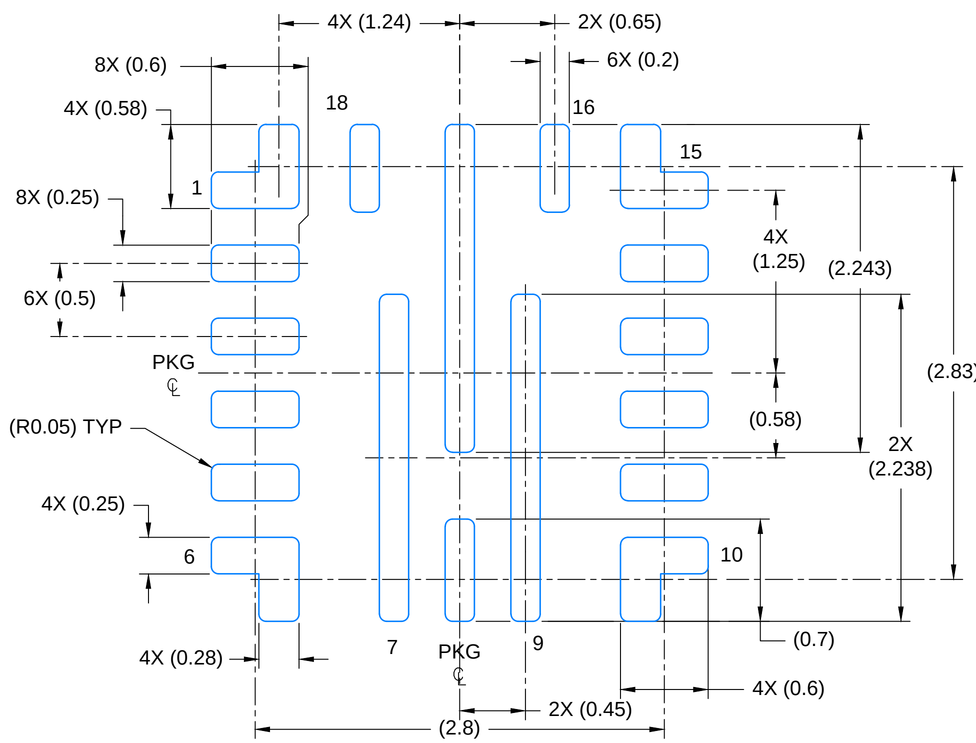
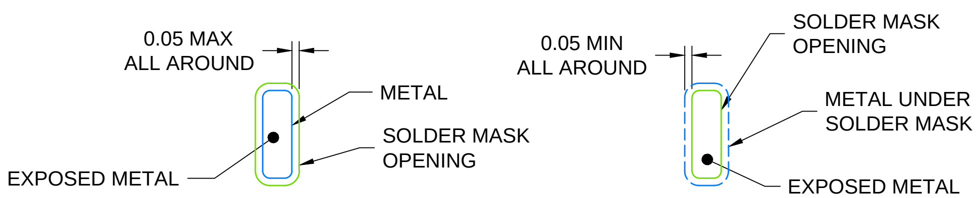
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X




NON- SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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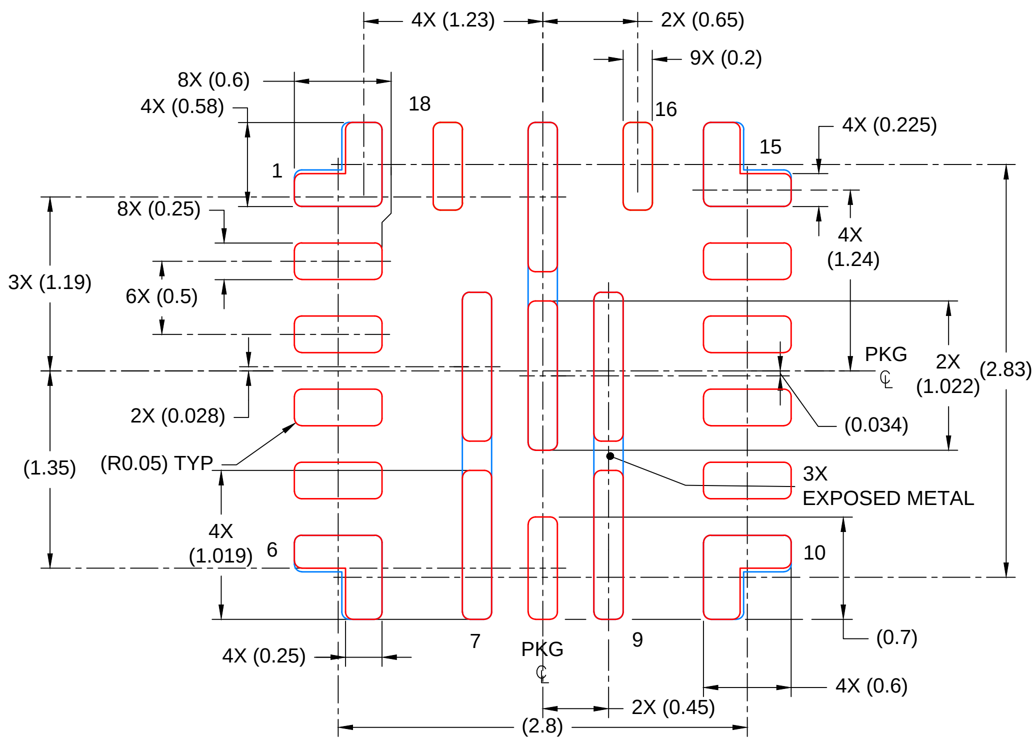
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1, 6, 10 &15: 93% & PADS 7-9,17:89%
SCALE: 20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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