

TPS709-Q1 150mA、30V、1 μ A I_Qのイネーブル付き電圧レギュレータ

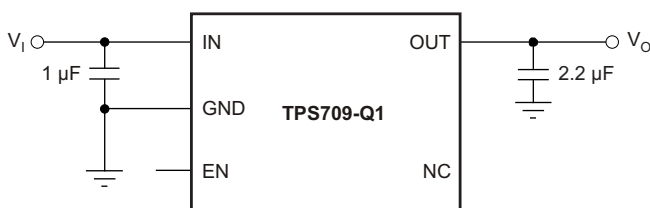
1 特長

- 車載用途に認定済み
- 次の結果でAEC-Q100認定済み
 - デバイス温度グレード1: 動作時周囲温度 -40°C~125°C
 - デバイスHBM ESD分類レベル2
 - デバイスCDM ESD分類レベルC4B
- 入力電圧範囲: 2.7V~30V
- 非常に低いI_Q: 1 μ A
- 逆電流保護
- 低いI_{SHUTDOWN}: 150nA
- 200mAのピーク出力をサポート
- 温度範囲全体で2%の精度
- 固定出力電圧で利用可能: 1.2V~6.5V
- サーマル・シャットダウンおよび過電流保護機能
- パッケージ: SOT-23-5、WSON-6

2 アプリケーション

- 自動車
- インフォテインメント
- 車体制御モジュール
- ナビゲーション・システム
- マイクロコントローラのスタンバイ電力

代表的なアプリケーション回路



3 概要

TPS709-Q1シリーズのリニア・レギュレータは、消費電力が重要なアプリケーション用に設計された、静止電流が非常に低いデバイスです。高精度のバンドギャップおよびエラー・アンプにより、温度範囲全体にわたって2%の精度が得られます。静止電流がわずか1 μ Aであるため、アイドル時の消費電力を最小限に抑える必要のある、常時オンのバッテリー駆動システムに最適なソリューションです。これらのデバイスは、サーマル・シャットダウン、電流制限、逆電流保護機能により安全性が強化されています。

これらのレギュレータは、ENピンをLowにすることでシャットダウン・モードに設定できます。このモードでのシャットダウン電流は、150nA (標準値)に低下します。

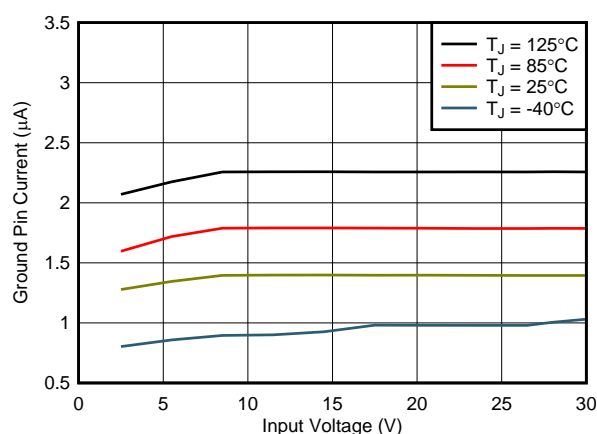
TPS709-Q1シリーズは、WSON-6およびSOT-23-5パッケージで供給されます。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
TPS709-Q1	SOT-23 (5)	2.90mm×1.60mm
	WSON (6)	2.00mm×2.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

GND電流とV_{IN}および温度との関係



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision B (March 2015) から Revision C に変更	Page
• Changed from: Dropout Voltage (V) to: Dropout Voltage (mV) in Figure 8 , Figure 9 , and Figure 10	7
• Deleted last sentence from <i>Shutdown</i> section	14
• Changed text From: "input supply range of 2.7 V to 6.5 V:" To: " input supply range of 2.7 V to 30 V." in the Power Supply Recommendations section	18

Revision A (December 2013) から Revision B に変更	Page
• DRVパッケージをドキュメントに追加、「ESD定格」、「推奨動作条件」、「タイミング要件」表、および「概要」、「デバイスの機能モード」、「代表的なアプリケーション」、「デバイスおよびドキュメントのサポート」、「メカニカル、パッケージ、および注文情報」セクションを追加	1
• 「アプリケーション情報」、「機能説明」、「電源に関する推奨事項」、「レイアウト」セクションを変更	1
• 「特長」簡条書きの「低ドロップアウト」項目を削除	1
• 「アプリケーション」セクションを変更	1
• 「概要」セクションの最後の文を変更	1
• 「製品情報」表を追加	1
• 表紙の曲線を追加	1
• Added DRV package drawing to <i>Pin Configuration and Functions</i> section	4
• Changed <i>Pin Functions</i> table: added DRV and I/O columns, added Thermal pad row, and changed EN pin description	4
• Changed Recommended Operating Conditions table	5
• Added DRV column to Thermal Information table	5
• Changed Electrical Characteristics conditions	6
• Changed V_{OUT} , I_{CL} , I_{SHDN} , and I_{REV} symbols in Electrical Characteristics table	6
• Changed $V_{EN(HI)}$ parameter into $V_{EN(HI)}$ and $V_{EN(LO)}$ parameters in Electrical Characteristics table	6
• Changed T_A parameter to T_J in Electrical Characteristics table	6
• Changed Typical Characteristics section	7
• Changed junction temperature values in first paragraph of Thermal Protection section	15

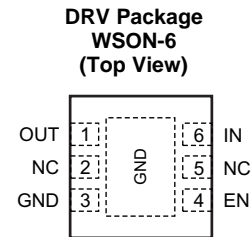
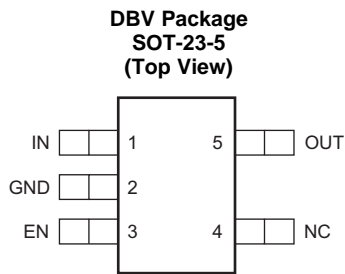
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- Changed 6.3-V to 10-V in second sentence of *Detailed Design Procedure* section 18
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2013年12月発行のものから更新

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5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION	
NAME	NO.			
	DRV	DBV		
EN	4	3	I	Enable pin. Driving this pin high enables the device. Driving this pin low puts the device into low current shutdown. This pin can be left floating to enable the device. The maximum voltage must remain below 6.5 V.
GND	3	2	—	Ground
IN	6	1	I	Unregulated input to the device
NC	2, 5	4	—	No internal connection
OUT	1	5	O	Regulated output voltage. Connect a small 2.2- μ F or greater ceramic capacitor from this pin to ground to assure stability.
Thermal pad	—	—	—	The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

specified at $T_J = -40^\circ\text{C}$ to 125°C , unless otherwise noted; all voltages are with respect to GND⁽¹⁾

		MIN	MAX	UNIT
Voltage	V_{IN}	-0.3	32	V
	V_{EN}	-0.3	7	V
	V_{OUT}	-0.3	7	V
Maximum output current	I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation	P_{DISS}	See Thermal Information		
Junction temperature, T_J		-55	150	$^\circ\text{C}$
Ambient temperature, T_A		-40	125	$^\circ\text{C}$
Storage temperature, T_{stg}		-55	150	$^\circ\text{C}$

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	± 750	

- (1) JEDEC document JEP155 states that 2-kV HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.7		30	V
V_{OUT}	Output voltage	1.2		6.5	V
I_{OUT}	Output current	0		150	mA
V_{EN}	Enable voltage	0		6.5	V
C_{IN}	Input capacitor		1		μF
C_{OUT}	Output capacitor	2	2.2	47	μF
T_J	Operating junction temperature	-40		125	$^\circ\text{C}$

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS709-Q1		UNIT
		DBV (SOT-23)	DRV (WSON)	
		5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	210.9	73.1	$^\circ\text{C}/\text{W}$
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	127.4	97.0	$^\circ\text{C}/\text{W}$
$R_{\theta JB}$	Junction-to-board thermal resistance	39.4	42.6	$^\circ\text{C}/\text{W}$
Ψ_{JT}	Junction-to-top characterization parameter	16.8	2.9	$^\circ\text{C}/\text{W}$
Ψ_{JB}	Junction-to-board characterization parameter	38.4	42.9	$^\circ\text{C}/\text{W}$
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	12.8	$^\circ\text{C}/\text{W}$

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

At $-40^{\circ}\text{C} \leq T_J, T_A \leq 125^{\circ}\text{C}$, $V_{IN} = V_{OUT(nom)} + 1\text{ V}$ or 2.7 V (whichever is greater), $I_{OUT} = 1\text{ mA}$, $V_{EN} = 2\text{ V}$, and $C_{IN} = C_{OUT} = 2.2\text{-}\mu\text{F}$ ceramic, unless otherwise noted. Typical values are at $T_J = 25^{\circ}\text{C}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		2.7		30	V
V_{OUT}	Output voltage range		1.2		6.5	V
V_{OUT}	DC output accuracy	$V_{OUT} < 3.3\text{ V}$	-2%		2%	
		$V_{OUT} \geq 3.3\text{ V}$	-1%		1%	
ΔV_{OUT}	Line regulation	$(V_{OUT(nom)} + 1\text{ V}, 2.7\text{ V}) \leq V_{IN} \leq 30\text{ V}$		3	10	mV
	Load regulation	$V_{IN} = V_{OUT(nom)} + 1.5\text{ V}$ or 3 V (whichever is greater), $100\text{ }\mu\text{A} \leq I_{OUT} \leq 150\text{ mA}$		20	50	mV
V_{DO}	Dropout voltage ⁽¹⁾⁽²⁾	TPS70933-Q1, $I_{OUT} = 50\text{ mA}$		295	650	mV
		TPS70933-Q1, $I_{OUT} = 150\text{ mA}$		975	1540	
		TPS70950-Q1, $I_{OUT} = 50\text{ mA}$		245	500	
		TPS70950-Q1, $I_{OUT} = 150\text{ mA}$		690	1200	
I_{CL}	Output current limit ⁽³⁾	$V_{OUT} = 0.9 \times V_{OUT(nom)}$	200	320	500	mA
I_{GND}	Ground pin current	$I_{OUT} = 0\text{ mA}, V_{OUT} \leq 3.3\text{ V}$		1.3	2.55	μA
		$I_{OUT} = 0\text{ mA}, V_{OUT} > 3.3\text{ V}$		1.4	2.7	
		$I_{OUT} = 100\text{ }\mu\text{A}, V_{IN} = 30\text{ V}$		6.7	10	
		$I_{OUT} = 150\text{ mA}$		350		
I_{SHDN}	Shutdown current	$V_{EN} \leq 0.4\text{ V}, V_{IN} = 2.7\text{ V}$		150		nA
PSRR	Power-supply rejection ratio	$f = 10\text{ Hz}$		80		dB
		$f = 100\text{ Hz}$		62		
		$f = 1\text{ kHz}$		52		
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, $I_{OUT} = 10\text{ mA}$, $V_{IN} = 2.7\text{ V}, V_{OUT} = 1.2\text{ V}$		190		μV_{RMS}
$V_{EN(HI)}$	Enable pin high (enabled)		0.9			V
$V_{EN(LO)}$	Enable pin high (disabled)		0		0.4	V
I_{EN}	Enable pin current	$EN = 1.0\text{ V}, V_{IN} = 5.5\text{ V}$		300		nA
I_{REV}	Reverse current (flowing out of IN pin)	$V_{OUT} = 3\text{ V}, V_{IN} = V_{EN} = 0\text{ V}$		10		nA
	Reverse current (flowing into OUT pin)	$V_{OUT} = 3\text{ V}, V_{IN} = V_{EN} = 0\text{ V}$		100		nA
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		158		$^{\circ}\text{C}$
		Reset, temperature decreasing		140		
T_J	Operating junction temperature		-40		125	$^{\circ}\text{C}$

(1) V_{DO} is measured with $V_{IN} = 0.98 \times V_{OUT(nom)}$.

(2) Dropout is only valid when $V_{OUT} \geq 2.8\text{ V}$ because of the minimum input voltage limits.

(3) Measured with $V_{IN} = V_{OUT} + 3\text{ V}$ for $V_{OUT} \leq 2.5\text{ V}$. Measured with $V_{IN} = V_{OUT} + 2.5\text{ V}$ for $V_{OUT} > 2.5\text{ V}$.

6.6 Timing Requirements

At $T_J = -40^{\circ}\text{C}$ to 125°C , $V_{IN} = V_{OUT(nom)} + 1\text{ V}$ or 2.7 V (whichever is greater), $R_L = 47\text{ }\Omega$, $V_{EN} = 2\text{ V}$, and $C_{IN} = C_{OUT} = 2.2\text{-}\mu\text{F}$ ceramic, unless otherwise noted. Typical values are at $T_J = 25^{\circ}\text{C}$.

		MIN	NOM	MAX	UNIT
t_{STR}	Start-up time ⁽¹⁾	$V_{OUT(nom)} \leq 3.3\text{ V}$	200	600	μs
		$V_{OUT(nom)} > 3.3\text{ V}$	500	1500	μs

(1) Start-up time = time from EN assertion to $0.95 \times V_{OUT(nom)}$ and load = $47\text{ }\Omega$.

6.7 Typical Characteristics

Over operating temperature range ($T_J = -40^{\circ}\text{C}$ to 125°C), $I_{OUT} = 10\text{ mA}$, $V_{EN} = 2\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, and $V_{IN} = V_{OUT(nom)} + 1\text{ V}$ or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at $T_J = 25^{\circ}\text{C}$.

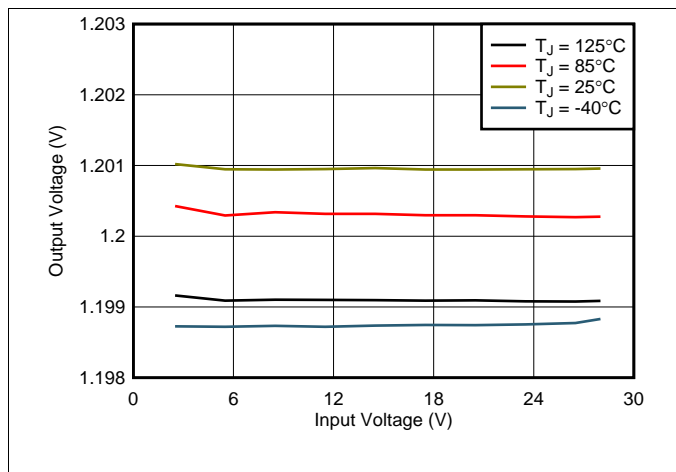


Figure 1. 1.2-V Line Regulation vs V_{IN} and Temperature

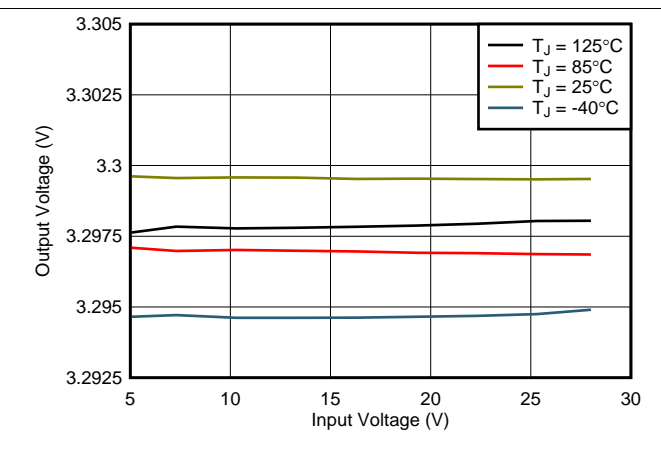


Figure 2. 3.3-V Line Regulation vs V_{IN} and Temperature

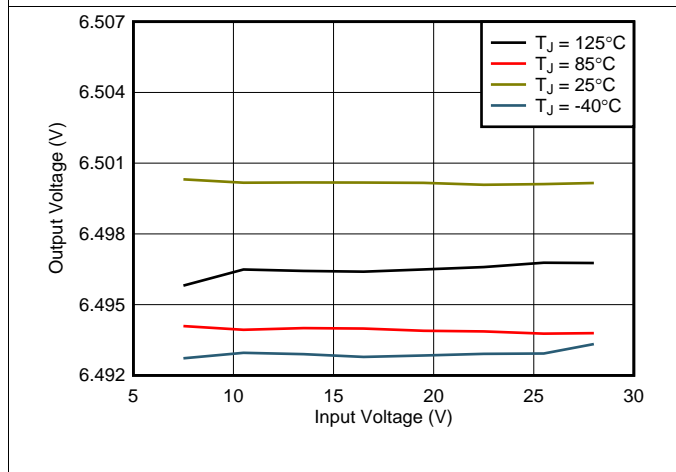


Figure 3. 6.5-V Line Regulation vs V_{IN} and Temperature

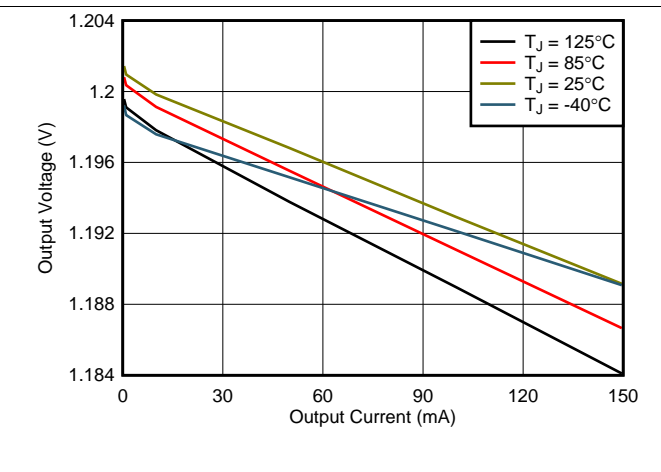


Figure 4. 1.2-V Load Regulation vs I_{OUT} and Temperature

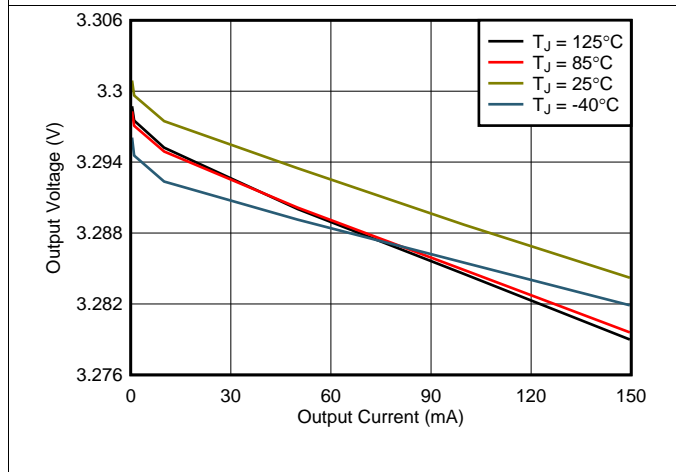


Figure 5. 3.3-V Load Regulation vs I_{OUT} and Temperature

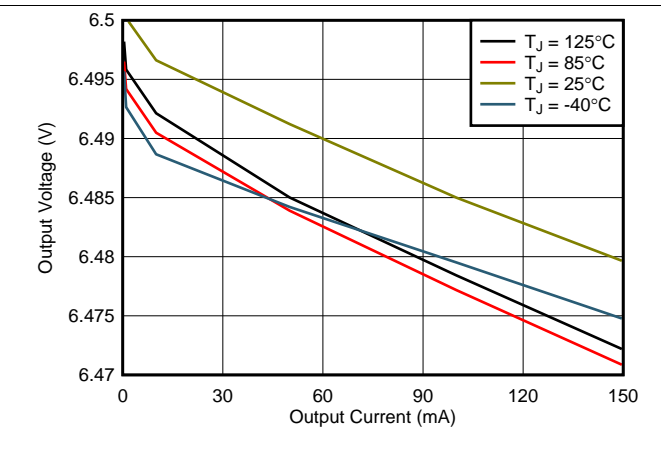


Figure 6. 6.5-V Load Regulation vs I_{OUT} and Temperature

Typical Characteristics (continued)

Over operating temperature range ($T_J = -40^{\circ}\text{C}$ to 125°C), $I_{OUT} = 10\text{ mA}$, $V_{EN} = 2\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, and $V_{IN} = V_{OUT(nom)} + 1\text{ V}$ or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at $T_J = 25^{\circ}\text{C}$.

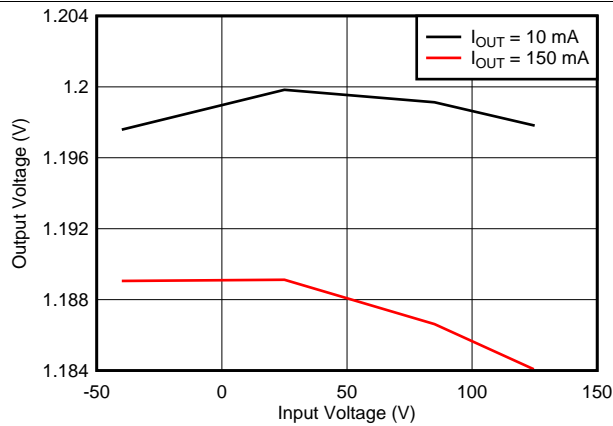


Figure 7. 1.2-V Output Voltage vs Temperature

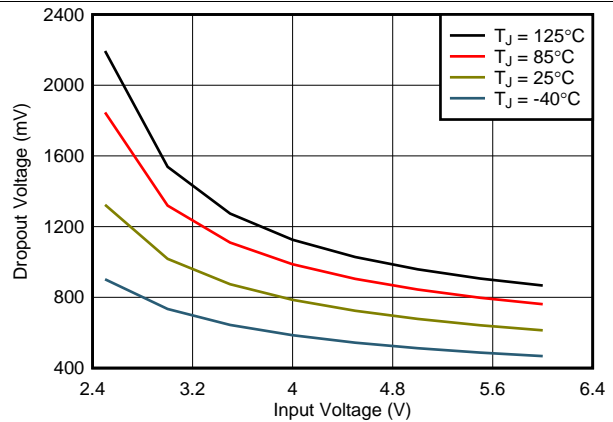


Figure 8. 6.5-V Dropout Voltage vs V_{IN} and Temperature

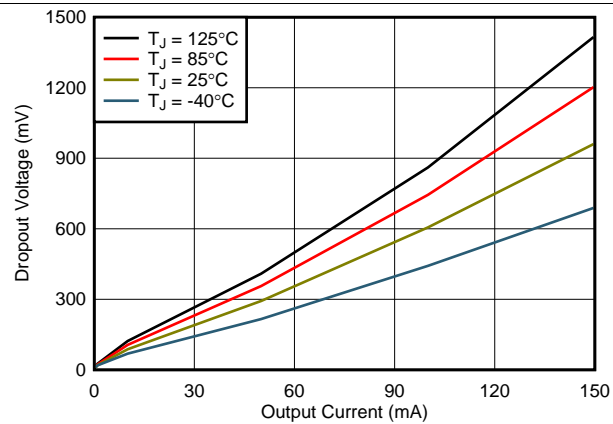


Figure 9. 3.3-V Dropout Voltage vs I_{OUT} and Temperature

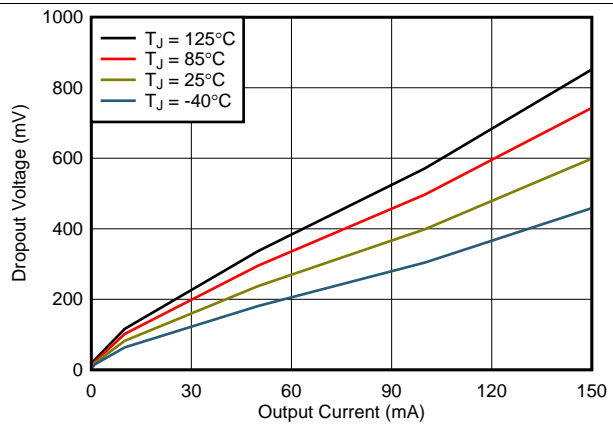


Figure 10. Dropout Voltage vs I_{OUT} and Temperature

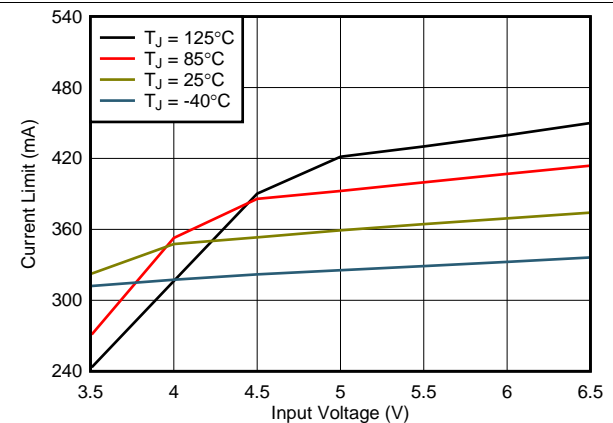


Figure 11. 1.2-V Current Limit vs V_{IN} and Temperature

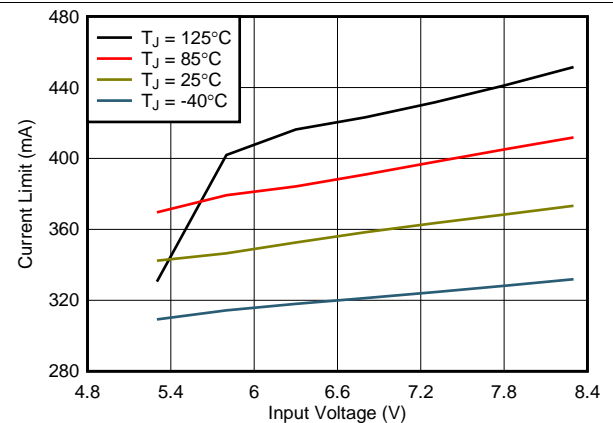


Figure 12. 3.3-V Current Limit vs V_{IN} and Temperature

Typical Characteristics (continued)

Over operating temperature range ($T_J = -40^{\circ}\text{C}$ to 125°C), $I_{\text{OUT}} = 10\text{ mA}$, $V_{\text{EN}} = 2\text{ V}$, $C_{\text{OUT}} = 2.2\text{ }\mu\text{F}$, and $V_{\text{IN}} = V_{\text{OUT(nom)}} + 1\text{ V}$ or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at $T_J = 25^{\circ}\text{C}$.

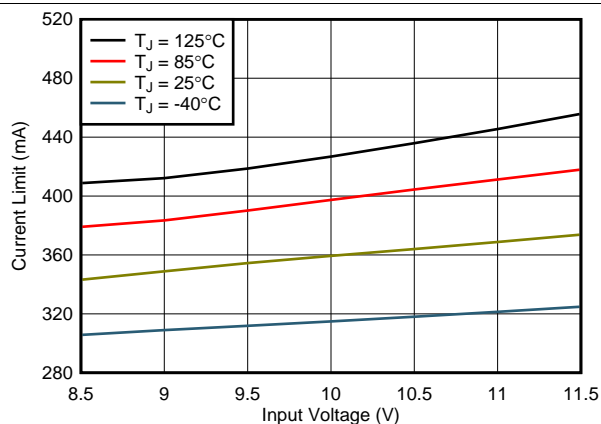


Figure 13. 6.5-V Current Limit vs V_{IN} and Temperature

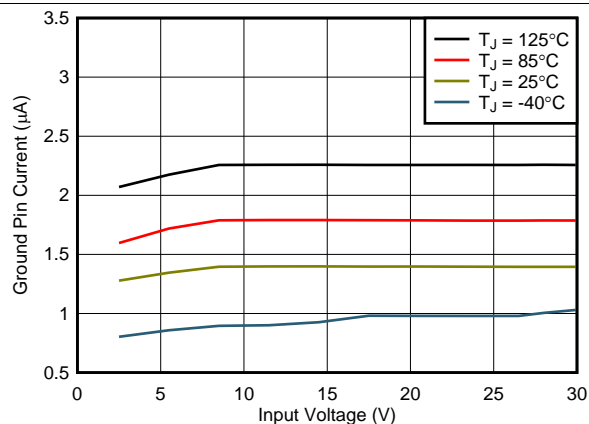


Figure 14. 1.2-V Ground Pin Current vs V_{IN} and Temperature

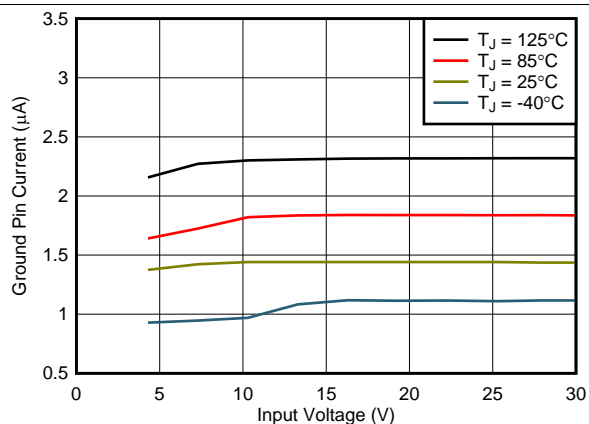


Figure 15. 3.3-V Ground Pin Current vs V_{IN} and Temperature

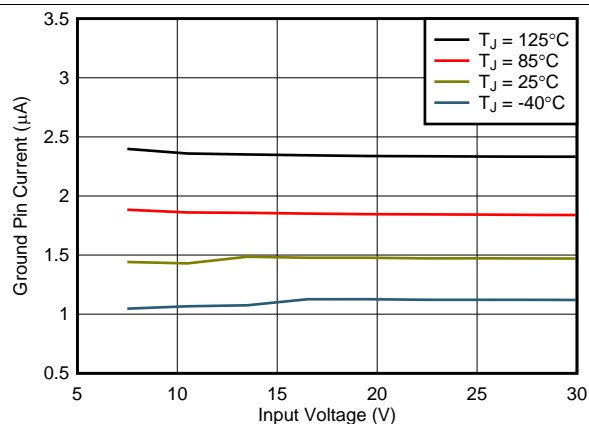


Figure 16. 6.5-V Ground Pin Current vs V_{IN} and Temperature

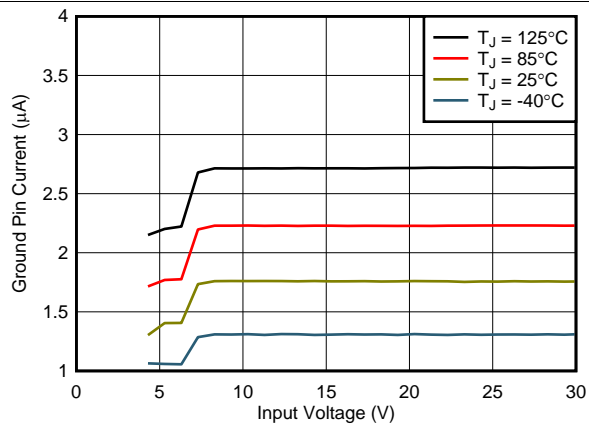


Figure 17. 3.3-V Ground Current vs V_{IN} and Temperature with EN Floating

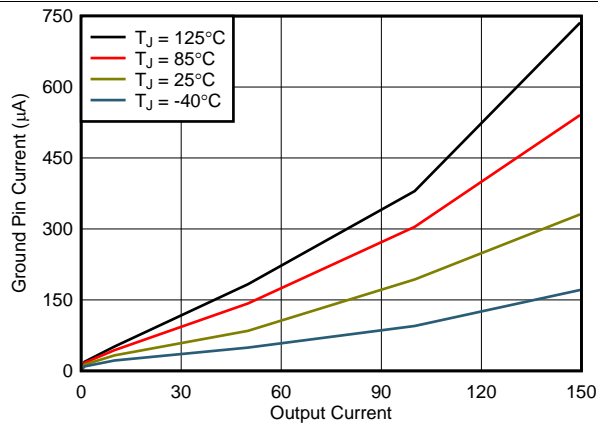


Figure 18. 1.2-V Ground Pin Current vs I_{OUT} and Temperature

Typical Characteristics (continued)

Over operating temperature range ($T_J = -40^{\circ}\text{C}$ to 125°C), $I_{\text{OUT}} = 10\text{ mA}$, $V_{\text{EN}} = 2\text{ V}$, $C_{\text{OUT}} = 2.2\text{ }\mu\text{F}$, and $V_{\text{IN}} = V_{\text{OUT(nom)}} + 1\text{ V}$ or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at $T_J = 25^{\circ}\text{C}$.

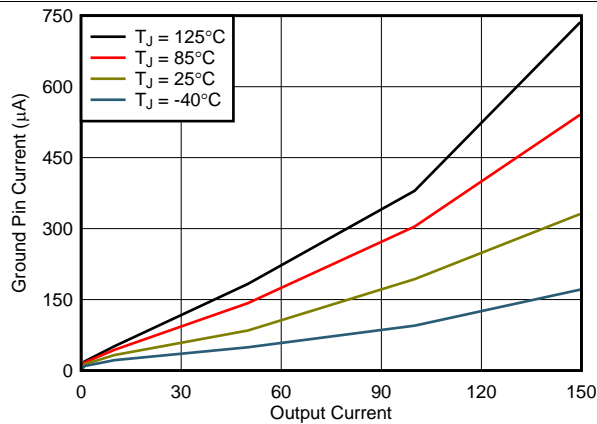


Figure 19. 3.3-V Ground Pin Current vs I_{OUT} and Temperature

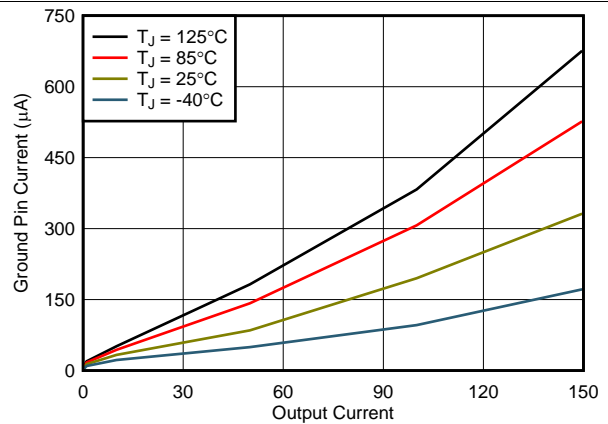


Figure 20. 6.5-V Ground Pin Current vs I_{OUT} and Temperature

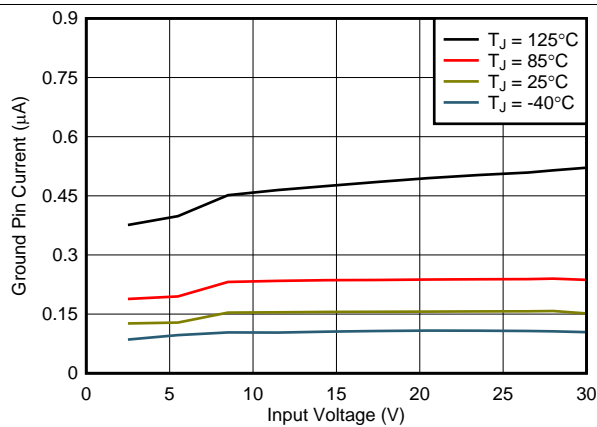


Figure 21. 1.2-V Shutdown Current vs V_{IN} and Temperature

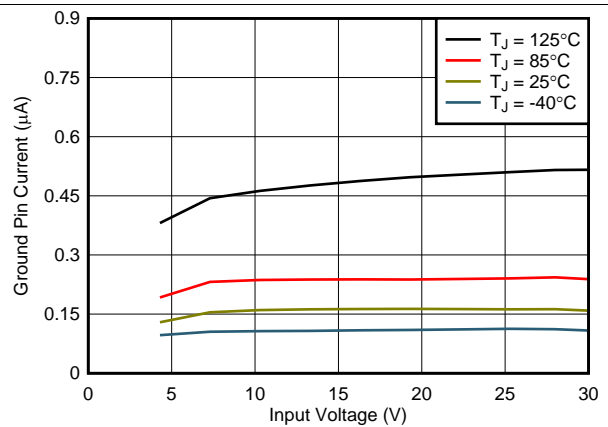


Figure 22. 3.3-V Shutdown Current vs V_{IN} and Temperature

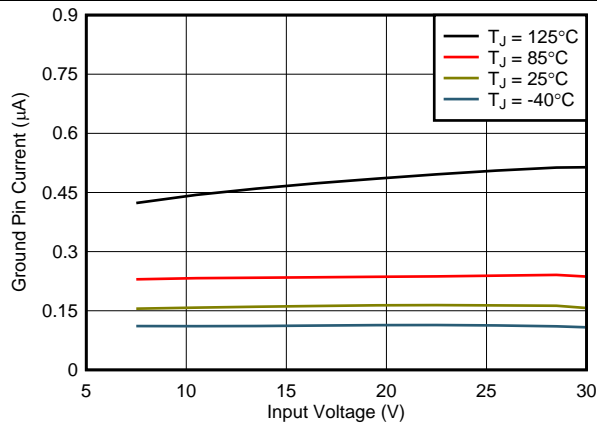


Figure 23. 6.5-V Shutdown Current vs V_{IN} and Temperature

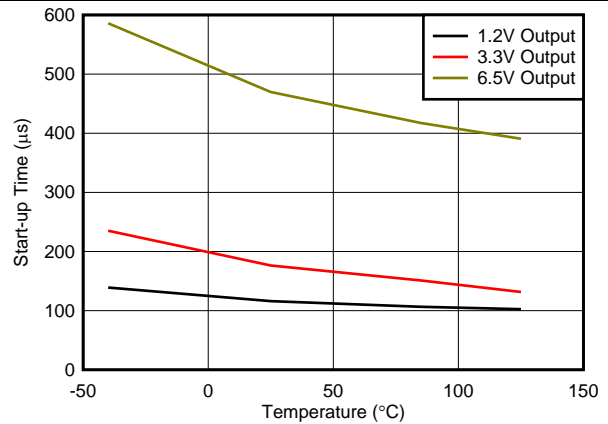


Figure 24. Start-Up Time vs Temperature

Typical Characteristics (continued)

Over operating temperature range ($T_J = -40^{\circ}\text{C}$ to 125°C), $I_{OUT} = 10\text{ mA}$, $V_{EN} = 2\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, and $V_{IN} = V_{OUT(nom)} + 1\text{ V}$ or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at $T_J = 25^{\circ}\text{C}$.

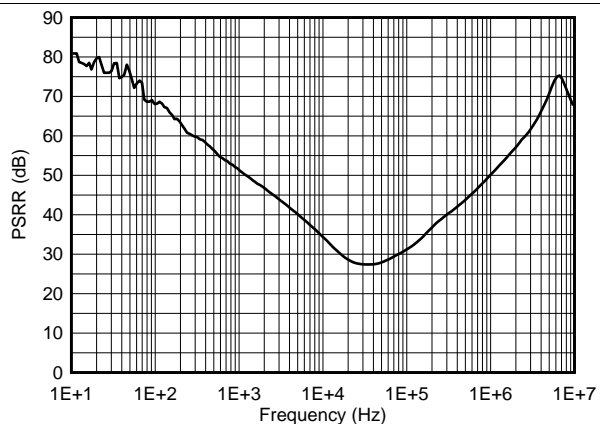


Figure 25. Power-Supply Rejection Ratio vs Frequency

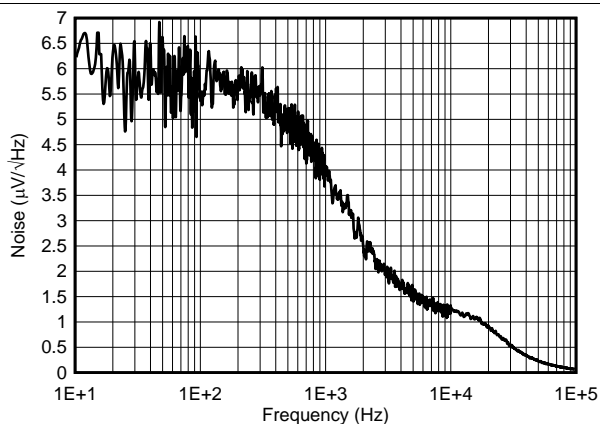
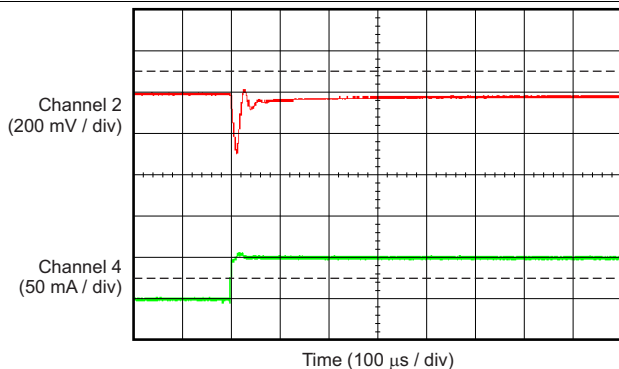
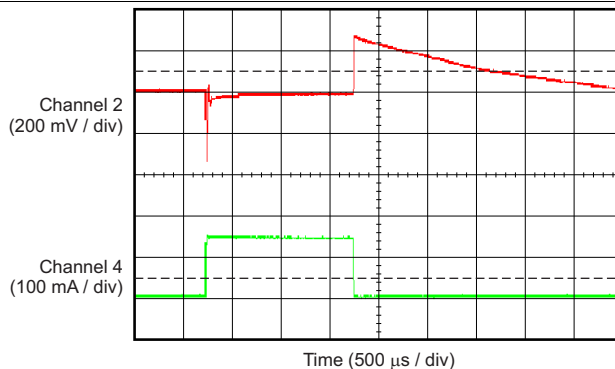


Figure 26. Noise



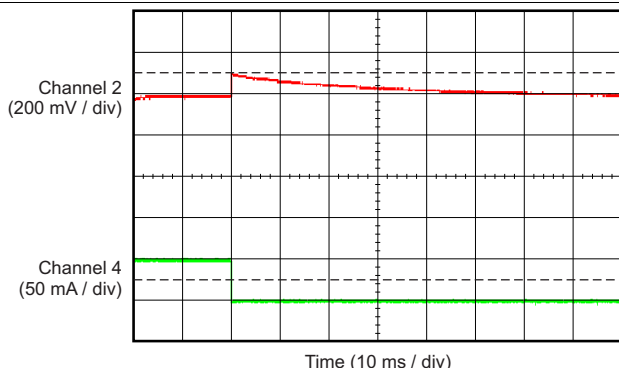
Channel 2 = V_{OUT} , channel 4 = I_{OUT} , $V_{IN} = 2.7\text{ V}$

Figure 27. TPS70912-Q1 Load Transient (0 mA to 50 mA)



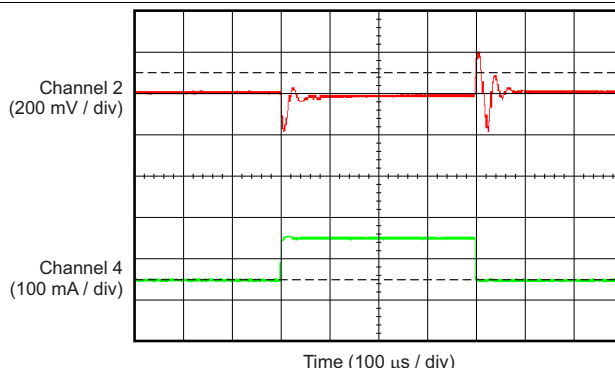
Channel 2 = V_{OUT} , channel 4 = I_{OUT} , $V_{IN} = 2.7\text{ V}$

Figure 28. TPS70912-Q1 Load Transient (1 mA to 150 mA)



Channel 2 = V_{OUT} , channel 4 = I_{OUT} , $V_{IN} = 2.7\text{ V}$

Figure 29. TPS70912-Q1 Load Transient (50 mA to 0 mA)

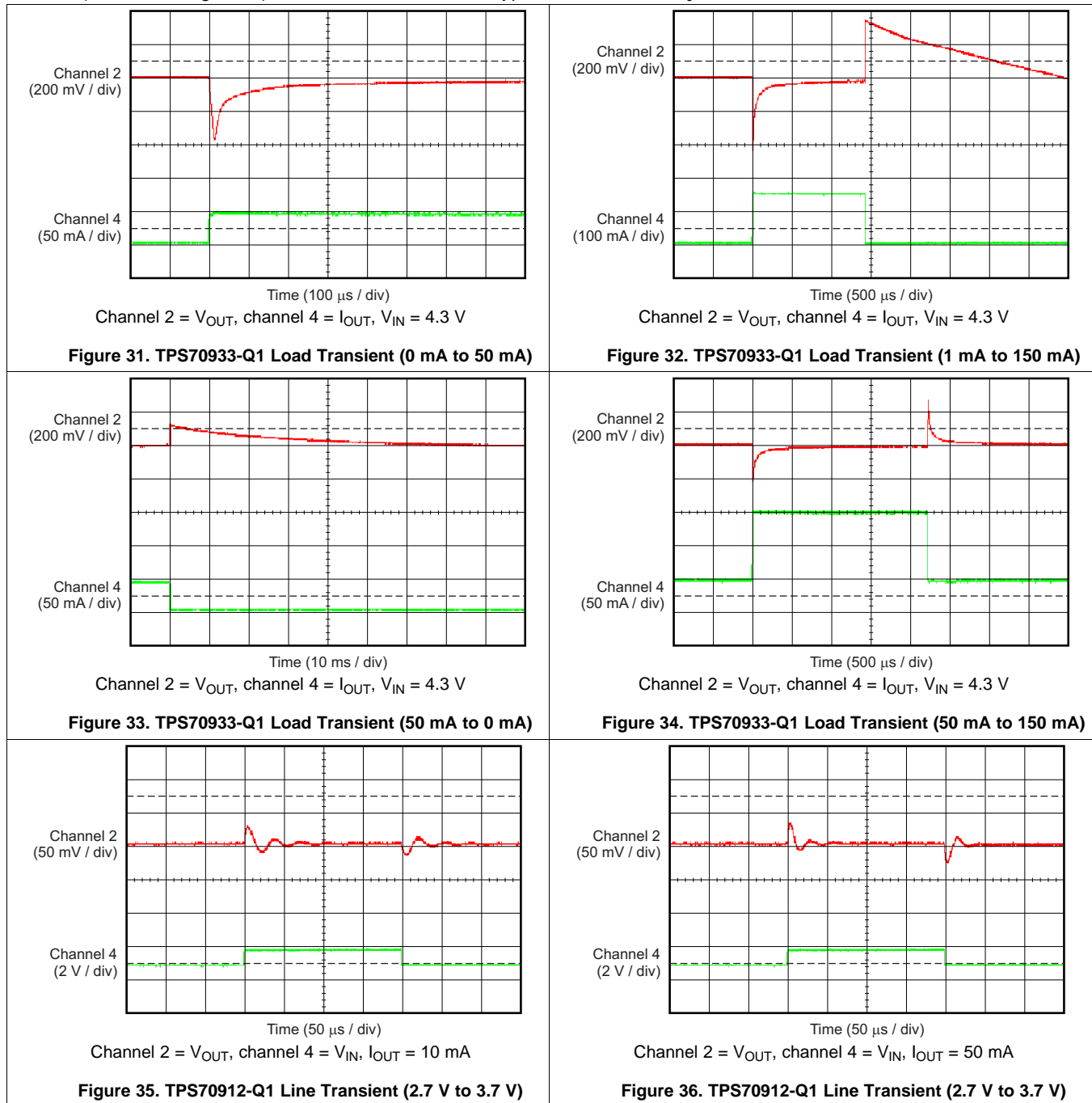


Channel 2 = V_{OUT} , channel 4 = I_{OUT} , $V_{IN} = 2.7\text{ V}$

Figure 30. TPS70912-Q1 Load Transient (50 mA to 150 mA)

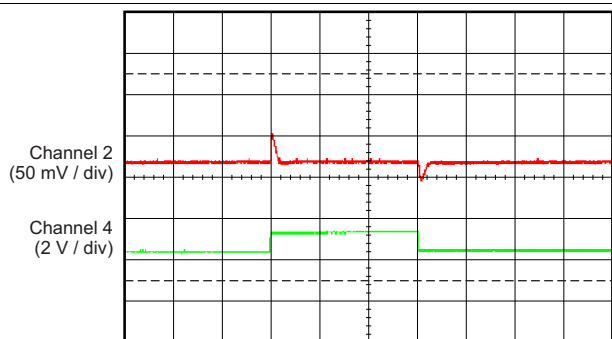
Typical Characteristics (continued)

Over operating temperature range ($T_J = -40^{\circ}\text{C}$ to 125°C), $I_{OUT} = 10\text{ mA}$, $V_{EN} = 2\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, and $V_{IN} = V_{OUT(nom)} + 1\text{ V}$ or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at $T_J = 25^{\circ}\text{C}$.



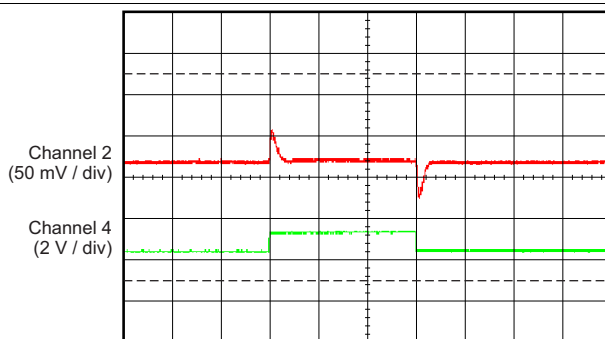
Typical Characteristics (continued)

Over operating temperature range ($T_J = -40^{\circ}\text{C}$ to 125°C), $I_{OUT} = 10\text{ mA}$, $V_{EN} = 2\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, and $V_{IN} = V_{OUT(nom)} + 1\text{ V}$ or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at $T_J = 25^{\circ}\text{C}$.



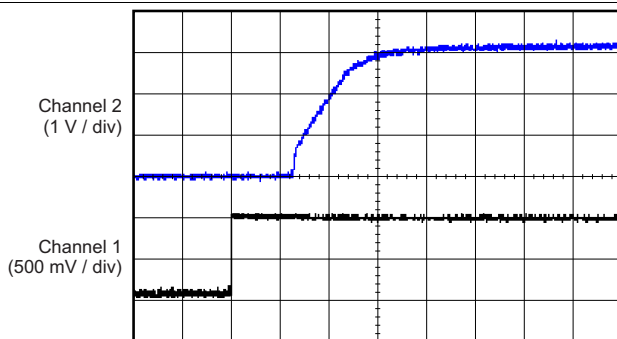
Time (50 μs / div)
Channel 2 = V_{OUT} , channel 4 = V_{IN} , $I_{OUT} = 10\text{ mA}$

Figure 37. TPS70933-Q1 Line Transient (4.3 V to 5.3 V)



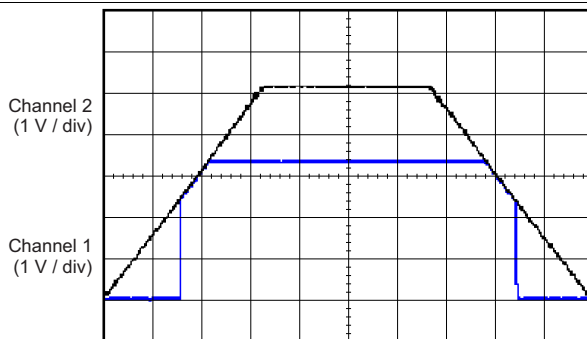
Time (50 μs / div)
Channel 2 = V_{OUT} , channel 4 = V_{IN} , $I_{OUT} = 50\text{ mA}$

Figure 38. TPS70933-Q1 Line Transient (4.3 V to 5.3 V)



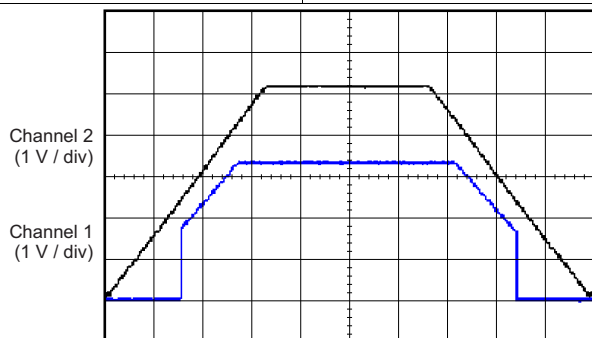
Time (50 μs / div)
Channel 1 = EN, channel 2 = V_{OUT} , $V_{IN} = 4.3\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$,
TPS70633

Figure 39. Power-Up with Enable



Time (500 ms / div)
Channel 1 = V_{IN} , channel 2 = V_{OUT} , $I_{OUT} = 3\text{ mA}$, TPS70633

Figure 40. Power-Up and Power-Down Response



Time (500 ms / div)
Channel 1 = V_{IN} , channel 2 = V_{OUT} , $I_{OUT} = 150\text{ mA}$, TPS70633

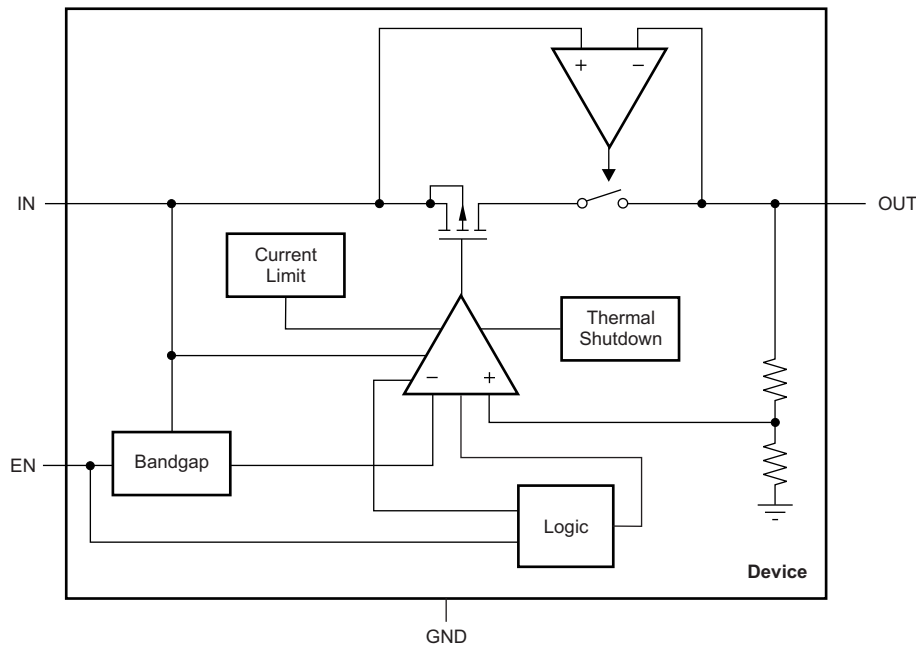
Figure 41. Power-Up and Power-Down Response

7 Detailed Description

7.1 Overview

The TPS709-Q1 series are ultralow quiescent current, low-dropout (LDO) linear regulators. The TPS709-Q1 offers reverse current protection to block any discharge current from the output into the input. The TPS709-Q1 also features current limit and thermal shutdown for reliable operation.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

The TPS709-Q1 uses an undervoltage lockout (UVLO) circuit to keep the output shut off until the internal circuitry operates properly.

7.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(HI)}$ (0.9 V, minimum). Turn off the device by forcing the EN pin to drop below 0.4 V.

7.3.3 Reverse Current Protection

The TPS709-Q1 has integrated reverse current protection. Reverse current protection prevents the flow of current from the OUT pin to the IN pin when output voltage is higher than input voltage. The reverse current protection circuitry places the power path in high impedance when the output voltage is higher than the input voltage. This setting reduces leakage current from the output to the input to 10 nA, typical. The reverse current protection is always active regardless of the enable pin logic state or if the OUT pin voltage is greater than 1.8 V. Reverse current can flow if the output voltage is less than 1.8 V and if input voltage is less than the output voltage.

If voltage is applied to the input pin, then the maximum voltage that can be applied to the OUT pin is the lower of three times the nominal output voltage or 6.5 V. For example, if the 1.2-V output voltage version is used, then the maximum reverse bias voltage that can be applied to the OUT pin is 3.6 V. If the 3.3-V output voltage version is used, then the maximum reverse bias voltage that can be applied to the OUT pin is 6.5 V.

Feature Description (continued)

7.3.4 Internal Current Limit

The TPS709-Q1 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. In such a case, the output voltage is not regulated, and can be measured as ($V_{OUT} = I_{LIMIT} \times R_{LOAD}$). The PMOS pass transistor dissipates $[(V_{IN} - V_{OUT}) \times I_{LIMIT}]$ until a thermal shutdown is triggered and the device turns off. When cool, the device is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown; see the [Thermal Information](#) section for more details.

The TPS709-Q1 is characterized over the recommended operating output current range up to 150 mA. The internal current limit begins to limit the output current at a minimum of 200 mA of output current.

7.3.5 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 158°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to 125°C, maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The TPS709-Q1 internal protection circuitry is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS709-Q1 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as $V_{IN(min)}$.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in the linear region and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 shows the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{LIM}$	$T_J < 125^{\circ}\text{C}$
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	—	$T_J < 125^{\circ}\text{C}$
Disabled mode (any true condition disables the device)	—	$V_{EN} < V_{EN(low)}$	—	$T_J > 158^{\circ}\text{C}$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS709-Q1 consumes low quiescent current and delivers excellent line and load transient performance. This performance, combined with low noise and good PSRR with little ($V_{IN} - V_{OUT}$) headroom, makes these devices ideal for RF portable applications, current limit, and thermal protection. The TPS709-Q1 devices are specified from -40°C to 125°C .

8.1.1 Input and Output Capacitor Considerations

The TPS709-Q1 devices are stable with output capacitors with an effective capacitance of $2.0\ \mu\text{F}$ or greater for output voltages below $1.5\ \text{V}$. For output voltages equal or greater than $1.5\ \text{V}$, the minimum effective capacitance for stability is $1.5\ \mu\text{F}$. The maximum capacitance for stability is $47\ \mu\text{F}$. The equivalent series resistance (ESR) of the output capacitor must be between $0\ \Omega$ and $0.2\ \Omega$ for stability.

The effective capacitance is the minimum capacitance value of a capacitor after taking into account variations resulting from tolerances, temperature, and dc bias effects. X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and ESR over temperature.

Although an input capacitor is not required for stability, good analog design practice is to connect a $0.1\text{-}\mu\text{F}$ to $2.2\text{-}\mu\text{F}$ capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple rejection, and PSRR.

8.1.2 Dropout Voltage

The TPS709-Q1 uses a PMOS pass transistor to achieve low dropout. When ($V_{IN} - V_{OUT}$) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} approximately scales with the output current because the PMOS device functions like a resistor in dropout.

The ground pin current of many linear voltage regulators increases substantially when the device is operated in dropout. This increase in ground pin current while operating in dropout can be several orders of magnitude larger than when the device is not in dropout. The TPS709-Q1 employs a special control loop that limits the increase in ground pin current while operating in dropout. This functionality allows for the most efficient operation while in dropout conditions that can greatly increase battery run times.

8.1.3 Transient Response

As with any regulator, increasing the output capacitor size reduces over- and undershoot magnitude, but increases transient response duration.

8.2 Typical Application

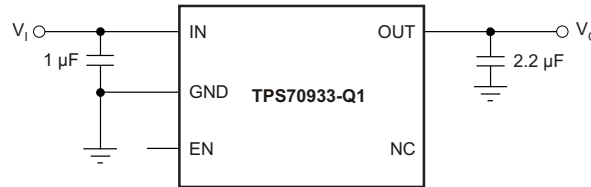


Figure 42. 3.3-V, Low- I_Q Rail

8.2.1 Design Requirements

Table 2 summarizes the design requirements for Figure 42.

Table 2. Design Requirements for a 3.3-V, Low- I_Q Rail Application

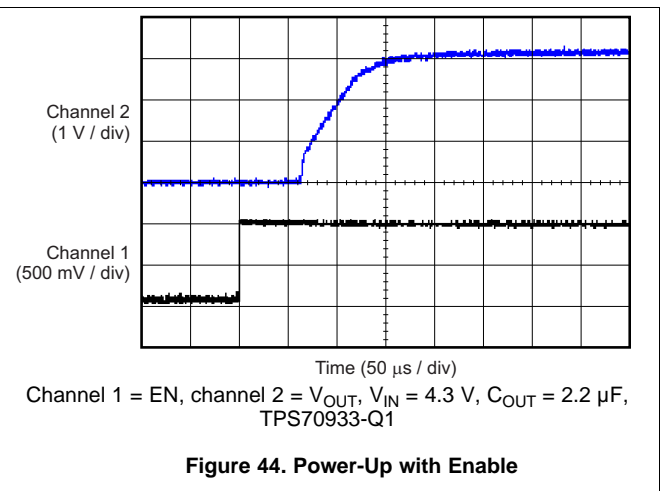
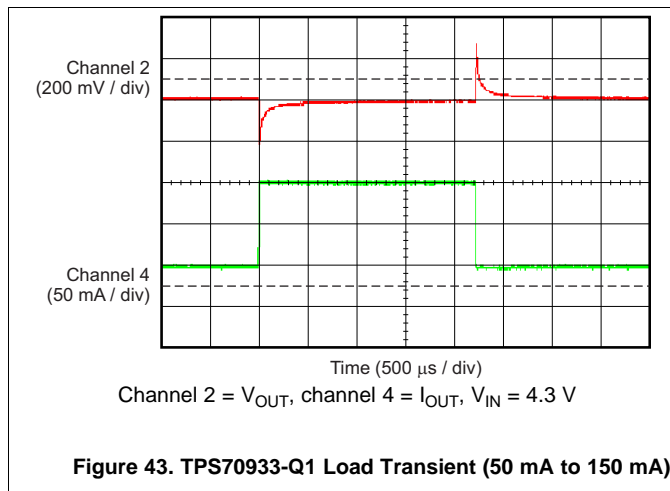
PARAMETER	DESIGN SPECIFICATION
V_{IN}	4.3 V
V_{OUT}	3.3 V
$I_{(IN)}$ (no load)	< 5 μ A
I_{OUT} (max)	150 mA

8.2.2 Detailed Design Procedure

Select a 2.2- μ F, 10-V X7R output capacitor to satisfy the minimum output capacitance requirement with a 3.3-V dc bias.

Select a 1.0- μ F, 10-V X7R input capacitor to provide input noise filtering and eliminate high-frequency voltage transients.

8.2.3 Application Curves



9 Power Supply Recommendations

This device is designed to operate with an input supply range of 2.7 V to 30 V. The input voltage range must provide adequate headroom in order for the device to have a regulated output. This input supply must be well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

Input and output capacitors must be placed as close to the device pins as possible. To improve ac performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT} , with the ground plane connected only at the device GND pin. In addition, the output capacitor ground connection must be connected directly to the device GND pin. High ESR capacitors may degrade PSRR performance.

10.1.2 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the [Thermal Information](#). Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) can be approximated by the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in [Equation 1](#).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{1}$$

[Figure 45](#) shows the maximum ambient temperature versus the power dissipation of the TPS709-Q1. This figure assumes the device is soldered on a JEDEC standard, high-K layout with no airflow over the board. Actual board thermal impedances vary widely. If the application requires high power dissipation, having a thorough understanding of the board temperature and thermal impedances is helpful to ensure the TPS709-Q1 does not operate above a junction temperature of 125°C.

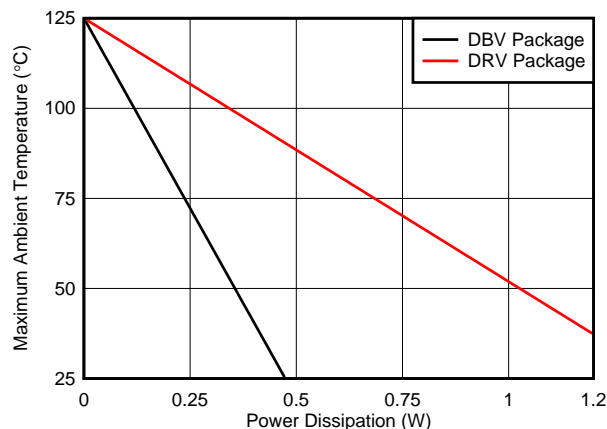


Figure 45. Maximum Ambient Temperature vs Device Power Dissipation

Layout Guidelines (continued)

Estimating the junction temperature can be done by using the thermal metrics Ψ_{JT} and Ψ_{JB} , shown in the [Thermal Information](#). These metrics are a more accurate representation of the heat transfer characteristics of the die and the package than $R_{\theta JA}$. The junction temperature can be estimated with [Equation 2](#).

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \cdot P_D$$

$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \cdot P_D$$

where:

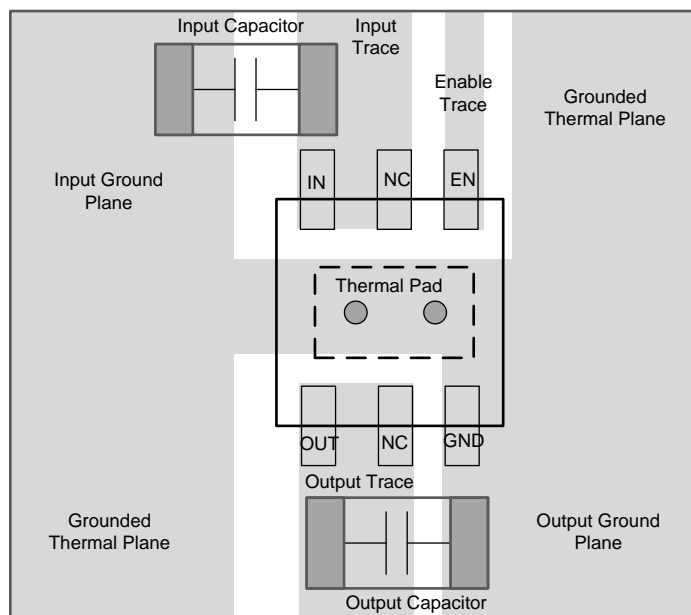
- P_D is the power dissipation shown by [Equation 1](#),
- T_T is the temperature at the center-top of the IC package,
- T_B is the PCB temperature measured 1 mm away from the IC package *on the PCB surface*. (2)

NOTE

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

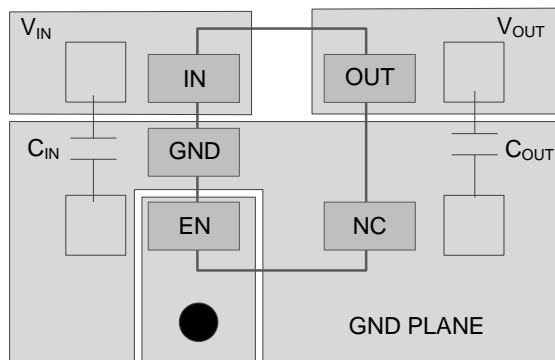
For more information about measuring T_T and T_B , see the application note [Using New Thermal Metrics \(SBVA025\)](#), available for download at www.ti.com.

10.2 Layout Examples



● Designates thermal vias.

Figure 46. WSON Layout Example



● Represents via used for application-specific connections.

Figure 47. SOT23-5 Layout Example

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

11.1.1.1 評価モジュール

TPS709-Q1を使用する回路の性能の初期評価に役立てるため、評価モジュール(EVM)を利用可能です。[TPS70933EVM-110評価モジュール](#)(および[関連するユーザー・ガイド](#))は、テキサス・インスツルメンツのWebサイトの製品フォルダから請求するか、[TI eStore](#)から直接お求めになれます。

11.1.1.2 SPICEモデル

SPICEを使用した回路パフォーマンスのコンピュータによるシミュレーションは、アナログ回路やシステムのパフォーマンスを分析するため多くの場合に有用です。TPS709用のSPICEモデルは、製品フォルダの「シミュレーション・モデル」で入手できます。

11.1.2 デバイスの項目表記

表 3. デバイスの項目表記⁽¹⁾

製品名	V _{OUT}
TPS709xx(x)yyyz-Q1	<p>xx(x)は公称出力電圧です。出力電圧の分解能が100mVの場合、注文番号に2桁が使用されます。それ以外の場合は3桁が使用されます(例: 28 = 2.8V、125 = 1.25V)。</p> <p>YYYはパッケージ指定子です。</p> <p>Zはテープ・アンド・リール数量です(R = 3,000、T = 250)。</p>

(1) 最新のパッケージおよび発注情報については、このデータシートの末尾にあるパッケージ・オプションについての付録を参照するか、TIのWebサイト(www.ti.com)をご覧ください。

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

[『TPS70933EVM-110評価モジュール・ユーザー・ガイド』](#)

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™オンライン・コミュニティ TIのE2E (*Engineer-to-Engineer*) コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

設計サポート TIの設計サポート役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.5 商標

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

11.6 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS70912QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLR	Samples
TPS70912QDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJD	Samples
TPS70915QDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJE	Samples
TPS70918QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLS	Samples
TPS70918QDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJF	Samples
TPS70925QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLT	Samples
TPS70925QDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJG	Samples
TPS70927QDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJH	Samples
TPS70928QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLU	Samples
TPS70928QDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJI	Samples
TPS70930QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLV	Samples
TPS70930QDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJJ	Samples
TPS70933QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLJ	Samples
TPS70933QDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJK	Samples
TPS70936QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLW	Samples
TPS70950QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLX	Samples
TPS70950QDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJL	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS70912QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70912QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70915QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70918QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70918QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70925QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70925QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70927QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70928QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70928QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70930QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70930QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70933QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70933QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70936QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70950QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70950QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS70912QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70912QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS70915QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS70918QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70918QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS70925QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70925QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS70927QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS70928QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70928QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS70930QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70930QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS70933QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70933QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS70936QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70950QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70950QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0

GENERIC PACKAGE VIEW

DRV 6

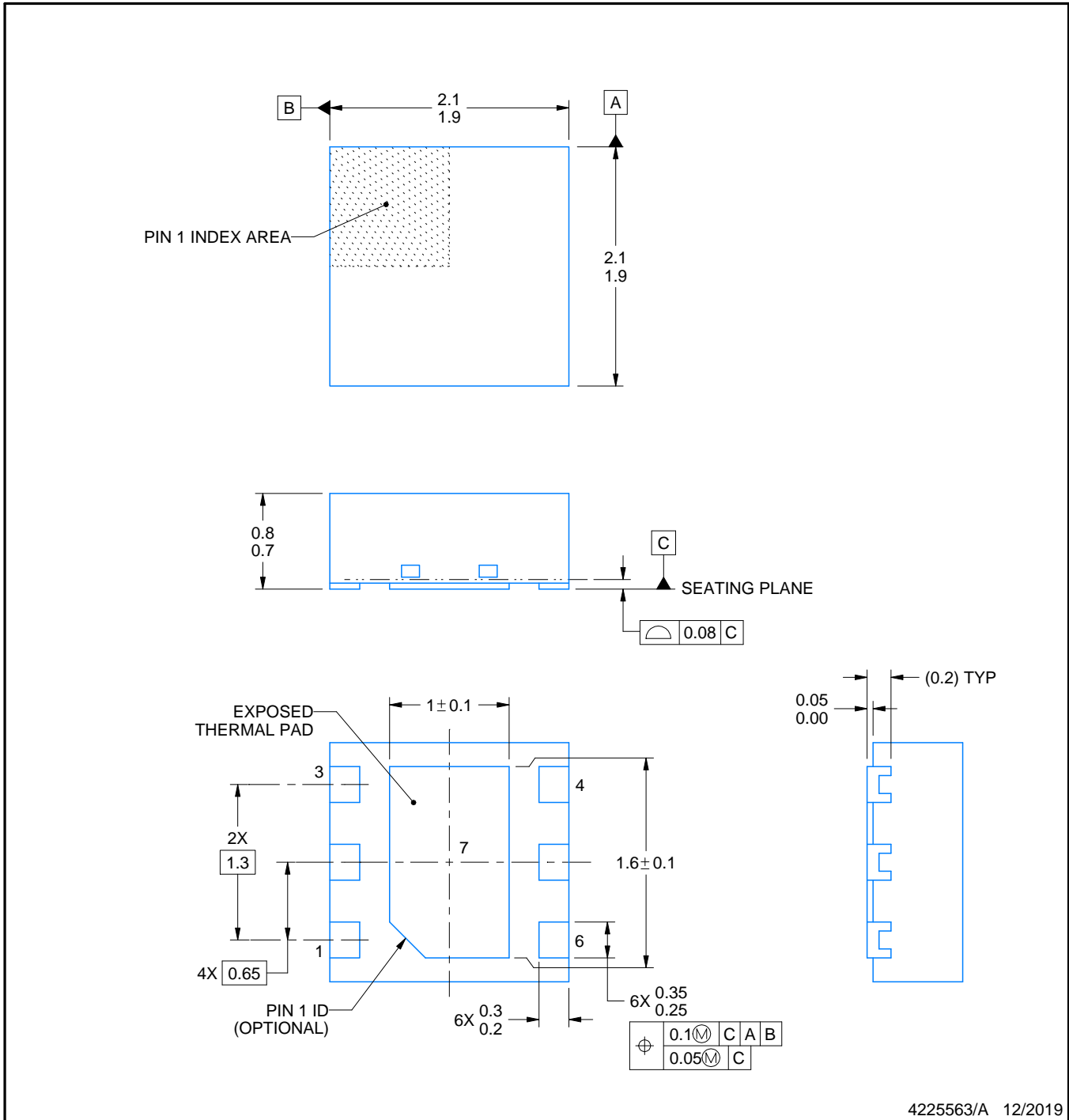
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4206925/F



4225563/A 12/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE STENCIL DESIGN

DRV0006D

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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