TPS74701 プログラマブル・ソフトスタート機能付き、500mA 低ドロップアウト・リニア・レギュレータ

1 特長

- V_{OUT} 範囲：0.8V～3.6V
- 非常に低い V_{IN} 範囲：0.8V～5.5V
- V_{BIAS} 範囲：2.7V～5.5V
- 低いドロップアウト：
  - 50mV (500mA 時の代表値、V_{BIAS} = 5V)
- パワー・グッド (PG) 出力により、電源電圧の監視、他の電源へのシーケンシング信号の供給が可能
- 入力電圧、負荷、温度に関する精度：2%
- プログラム可能なソフトスタートにより、直線的に電圧が立ち上がるようにスタートアップさせることが可能
- V_{BIAS} により、優れた過渡応答の低 V_{IN} 動作を実現
- 任意の出力コンデンサ (≥ 2.2µF) で安定に動作
- 3mm × 3mm × 1mm の小型 10 ピン・パッケージで供給

2 アプリケーション

- ネットワーク接続ストレージ (NAS) - エンタープライズ
- ラック・サーバー
- ネットワーク・インターフェイス・カード (NIC)
- 商用ネットワークとサーバーの PSU (電源)

3 概要

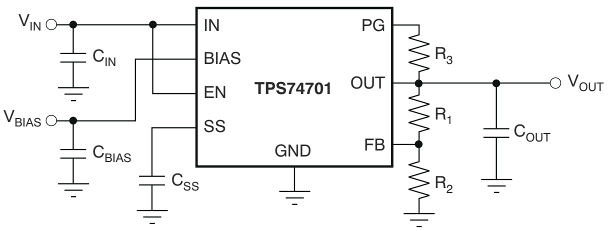
TPS74701 低ドロップアウト (LDO) リニア・レギュレータは、広範なアプリケーション向けの使いやすく堅牢なパワー・マネージメント・ソリューションです。ソフトスタートをユーザーがプログラムできるので、スタートアップ時の容量性突入電流を低減して、入力電源のストレスを最小限に抑えることができます。ソフトスタートは単調性で、多くの種類のプロセッサおよび特定用途向け IC (ASIC) の電源供給に適しています。イネーブル入力とパワー・グッド出力により、外部レギュレータとの間でシーケンシングを簡単に実行できます。このような高い柔軟性により、FPGA や DSP、その他の特殊なスタートアップ条件を持つアプリケーションのシーケンス制御条件を満たすソリューションを構成できます。

高精度の基準電圧およびエラー・アンプは、負荷、ライン、温度、プロセスの範囲全体にわたって 2% の精度を維持します。本デバイスは 2.2µF 以上の任意のタイプのコンデンサで安定して動作し、-40℃～+125℃で仕様が規定されています。TPS74701 は、小型の 3mm × 3mm VSON-10 パッケージで供給されるため、TPS74801 との互換性があります。

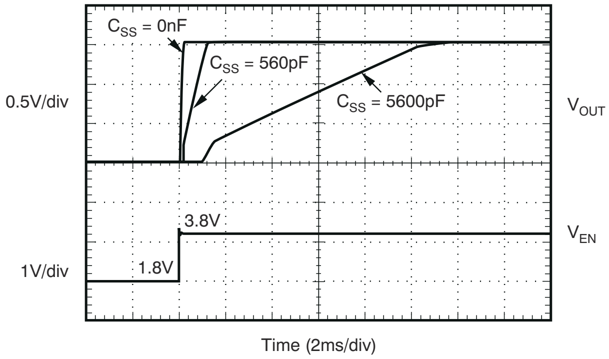
パッケージ情報

部品番号	パッケージ(1)	本体サイズ (公称)
TPS74701	DRC (VSON、10)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



代表的なアプリケーション回路 (可変)



ターンオン応答

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

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- *文書全体にわたって表、図、相互参照の採番方法を更新* 1
- ドキュメント全体で SON を VSON に変更............ 1
- ドキュメントに M3 サフィックス・デバイスを追加............ 1
- Added M3-suffix *Typical Characteristics* sections............ 12

Changes from Revision F (November 2010) to Revision G (September 2015) — Page

- 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。............ 1

5 Pin Configuration and Functions

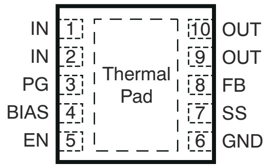


図 5-1. DRC Package, 10-Pin VSON (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	**NO.**		
IN	1, 2	I	Input to the device.
EN	5	I	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. This pin must not be left unconnected.
SS	7	—	Soft-start pin. A capacitor connected on this pin to ground sets the start-up time. If this pin is left unconnected, the regulator output soft-start ramp time is typically 200 μs.
BIAS	4	I	Bias input voltage for error amplifier, reference, and internal control circuits.
PG	3	O	Power-good pin. An open-drain, active-high output that indicates the status of V_{OUT}. When V_{OUT} exceeds the PG trip threshold, the PG pin goes into a high-impedance state. When V_{OUT} is below this threshold the pin is driven to a low-impedance state. A pullup resistor from 10 kΩ to 1 MΩ must be connected from this pin to a supply of up to 5.5 V. The supply can be higher than the input voltage. Alternatively, the PG pin can be left unconnected if output monitoring is not necessary.
FB	8	I	Feedback pin. The feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating.
OUT	9, 10	O	Regulated output voltage. A small capacitor (total typical capacitance ≥ 2.2 μF, ceramic) is needed from this pin to ground to assure stability.
NC	N/A	I	No connection. This pin can be left floating or connected to GND to allow better thermal contact to the top-side plane.
GND	6	I	Ground
Thermal Pad	—	I	Solder this pad to the ground plane for increased thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{IN}, V_{BIAS}	Input voltage	–0.3	6	V
V_{EN}	Enable voltage	–0.3	6	V
V_{PG}	Power good voltage	–0.3	6	V
I_{PG}	PG sink current	0	1.5	mA
V_{SS}	Soft-start voltage	–0.3	6	V
V_{FB}	Feedback voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	V_{IN} + 0.3	V
I_{OUT}	Maximum output current	Internally limited		
	Output short-circuit duration	Indefinite		
P_{DISS}	Continuous total power dissipation	See Thermal Information		
T_J	Junction Temperature	–40	150	°C
T_{stg}	Storage Temperature	–55	150	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	V_{OUT} + V_{DO} (V_{IN})	V_{OUT} + 0.3	5.5	V
V_{EN}	Enable supply voltage	0	V_{IN}	5.5	V
V_{BIAS} [1]	BIAS supply voltage	V_{OUT} + V_{DO} (V_{BIAS})[2]	V_{OUT} + 1.4 [2]	5.5	V
V_{OUT}	Output voltage	0.8		3.3	V
I_{OUT}	Output current	0		500	mA
C_{OUT}	Output capacitor	2.2			µF
C_{IN}	Input capacitor[3]	1			µF
C_{BIAS}	Bias capacitor	0.1	1		µF
T_J	Operating junction temperature	–40		125	°C

(1) BIAS supply is required when V_{IN} is below V_{OUT} + 1.62 V.
(2) V_{BIAS} has a minimum voltage of 2.7 V or V_{OUT} + V_{DO} (V_{BIAS}), whichever is higher.
(3) If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for the supply is 4.7 µF.

6.4 Thermal Information

THERMAL METRIC[1]		TPS747[2]		UNIT
		DRC (VSON)	DRC (VSON) [2]	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.5	47.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78	63.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	N/A	19.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	4.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.3	19.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.6	3.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.
(2) M3 suffix.

6.5 Electrical Characteristics: Other Orderable Devices (non-M3 Suffix)

At V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3 V, C_{BIAS} = 0.1 µF, C_{IN} = C_{OUT} = 10 µF, C_{NR} = 1 nF, I_{OUT} = 50 mA, V_{BIAS} = 5.0 V, and T_J = –40°C to 125°C, (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Internal reference (Adj.)	T_A = +25°C	0.796	0.8	0.804	V
$\Delta V_{OUT\ (\Delta VIN)}$	Output voltage range	V_{IN} = 5 V, I_{OUT} = 0.5 A	V_{REF}		3.6	V
	Accuracy(1)	2.97 V ≤ V_{BIAS} ≤ 5.5 V, 50 mA ≤ I_{OUT} ≤ 0.5 A	–2	±0.5	2	%
$\Delta V_{OUT\ (\Delta IOUT)}$	Line regulation	$V_{OUT(nom)}$ + 0.3 ≤ V_{IN} ≤ 5.5 V		0.03		%/V
V_{OUT}	Load regulation	50 mA ≤ I_{OUT} ≤ 0.5 A		0.09		%/A
V_{DO}	V_{IN} dropout voltage(2)	I_{OUT} = 0.5 A, V_{BIAS} – $V_{OUT(nom)}$ ≥ 3.25 V(3)		50	120	mV
	V_{BIAS} dropout voltage(2)	I_{OUT} = 0.5 A, V_{IN} = V_{BIAS}		1.31	1.39	V
I_{CL}	Output current limit	V_{OUT} = 80% × $V_{OUT(nom)}$	800		1350	mA
I_{BIAS}	BIAS pin current			1	2	mA
I_{SHDN}	Shutdown supply current (I_{GND})	V_{EN} ≤ 0.4 V		1	50	µA
I_{FB}	Feedback pin current		–1	0.15	1	µA
PSRR	Power-supply rejection (V_{IN} to V_{OUT})	1 kHz, I_{OUT} = 0.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		60		dB
		300 kHz, I_{OUT} = 0.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		30		dB
	Power-supply rejection (V_{BIAS} to V_{OUT})	1 kHz, I_{OUT} = 0.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		50		dB
		300 kHz, I_{OUT} = 0.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		30		dB
V_n	Output noise voltage	BW = 100 Hz to 100 kHz, I_{OUT} = 0.5 A, C_{SS} = 1 nF		25		µVrms x Vout
V_n	Output noise voltage	BW = 100 Hz to 100 kHz, I_{OUT} = 0.5 A, C_{SS} = 1 nF		25 × V_{OUT}		µVrms
t_{STR}	Minimum start-up time	R_{LOAD} for I_{OUT} = 0.5 A, C_{SS} = open		200		µs
I_{SS}	Soft-start charging current	V_{SS} = 0.4 V		440		nA
$V_{EN(hi)}$	Enable input high level		1.1		5.5	V
$V_{EN(lo)}$	Enable input low level		0		0.4	V
$V_{EN(hys)}$	Enable pin hysteresis			50		mV
$V_{EN(dg)}$	Enable pin deglitch time			20		µs
I_{EN}	Enable pin current	V_{EN} = 5 V		0.1	1	µA
V_{IT}	PG trip threshold	V_{OUT} decreasing	85	90	94	%V_{OUT}
V_{HYS}	PG trip hysteresis			3		%V_{OUT}
$V_{PG(lo)}$	PG output low voltage	I_{PG} = 1 mA (sinking), V_{OUT} < V_{IT}			0.3	V
$I_{PG(lkg)}$	PG leakage current	V_{PG} = 5.25 V, V_{OUT} > V_{IT}		0.1	1	µA
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		165		°C
		Reset, temperature decreasing		140		

(1) Adjustable devices tested at 0.8 V; resistor tolerance is not taken into account.
(2) Dropout is defined as the voltage from V_{IN} to V_{OUT} when V_{OUT} is 3% below nominal.
(3) 3.25 V is a test condition of this device and can be adjusted by referring to Figure 6-6.

6.6 Electrical Characteristics: Orderable Device (M3 Suffix)

At V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3 V, C_{BIAS} = 0.1 µF, C_{IN} = C_{OUT} = 10 µF, C_{NR} = 1 nF, I_{OUT} = 50 mA, V_{BIAS} = 5.0 V, and T_J = –40°C to 125°C, (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Internal reference (Adj.)	T_A = +25°C	0.796	0.8	0.804	V
$\Delta V_{OUT\ (\Delta VIN)}$	Output voltage range	V_{IN} = 5 V, I_{OUT} = 500 mA	V_{REF}		3.6	V
	Accuracy(1)	2.97 V ≤ V_{BIAS} ≤ 5.5 V, 50 mA ≤ I_{OUT} ≤ 500 mA	–0.95	±0.3	0.95	%
$\Delta V_{OUT\ (\Delta IOUT)}$	Line regulation	$V_{OUT(nom)}$ + 0.3 ≤ V_{IN} ≤ 5.5 V		0.001		%/V
V_{OUT}	Load regulation	50 mA ≤ I_{OUT} ≤ 500 mA		0.11		%/A
V_{DO}	V_{IN} dropout voltage(2)	I_{OUT} = 500 mA, V_{BIAS} – $V_{OUT(nom)}$ ≥ 1.62 V(3)		20	35	mV
	V_{BIAS} dropout voltage(2)	I_{OUT} = 500 mA, V_{IN} = V_{BIAS}		1.1	1.25	V
I_{CL}	Output current limit	V_{OUT} = 80% × $V_{OUT(nom)}$	800		1300	mA
I_{BIAS}	BIAS pin current			1	1.2	mA
I_{SHDN}	Shutdown supply current (I_{GND})	V_{EN} ≤ 0.4 V		0.85	2.75	µA
I_{FB}	Feedback pin current		–30	0.15	30	nA
PSRR	Power-supply rejection (V_{IN} to V_{OUT})	1 kHz, I_{OUT} = 500 mA, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		76		dB
		300 kHz, I_{OUT} = 500 mA, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		50		dB
	Power-supply rejection (V_{BIAS} to V_{OUT})	1 kHz, I_{OUT} = 500 mA, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		59		dB
		300 kHz, I_{OUT} = 500 mA, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		49		dB
V_n	Output noise voltage	BW = 100 Hz to 100 kHz, I_{OUT} = 500 mA, C_{SS} = 1 nF		20		µVrms x Vout
t_{STR}	Minimum start-up time	R_{LOAD} for I_{OUT} = 1.0 A, C_{SS} = open		250		µs
I_{SS}	Soft-start charging current	V_{SS} = 0.4 V		530		nA
$V_{EN(hi)}$	Enable input high level		1.1		5.5	V
$V_{EN(lo)}$	Enable input low level		0		0.4	V
$V_{EN(hys)}$	Enable pin hysteresis			55		mV
$V_{EN(dg)}$	Enable pin deglitch time			20		µs
I_{EN}	Enable pin current	V_{EN} = 5 V		0.1	0.25	µA
V_{IT}	PG trip threshold	V_{OUT} decreasing	85	90	94	$\%V_{OUT}$
V_{HYS}	PG trip hysteresis			3		$\%V_{OUT}$
$V_{PG(lo)}$	PG output low voltage	I_{PG} = 1 mA (sinking), V_{OUT} < V_{IT}			0.12	V
$I_{PG(lkg)}$	PG leakage current	V_{PG} = 5.25 V, V_{OUT} > V_{IT}		0.001	0.05	µA
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		165		℃
		Reset, temperature decreasing		140		

(1) Adjustable devices tested at 0.8 V; resistor tolerance is not taken into account.
(2) Dropout is defined as the voltage from V_{IN} to V_{OUT} when V_{OUT} is 3% below nominal.
(3) 3.25 V is a test condition of this device and can be adjusted by referring to Figure 6-29.

6.7 Typical Characteristics: $V_{EN} = V_{IN}$ (All Other Orderable Devices, Non-M3 Suffix)

at T_J = 25°C, $V_{IN} = V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, $V_{EN} = V_{IN}$, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF (unless otherwise noted)

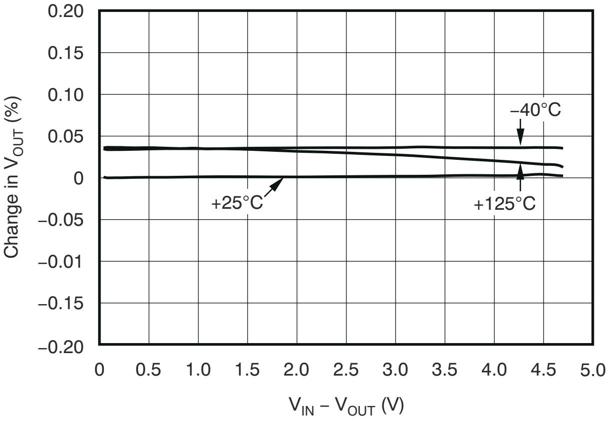


図 6-1. V_{IN} Line Regulation

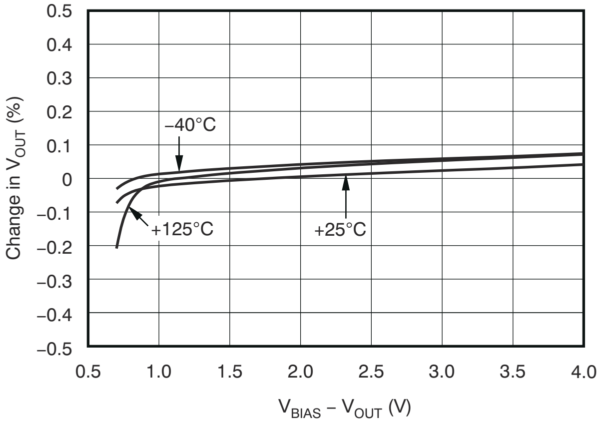


図 6-2. V_{BIAS} Line Regulation

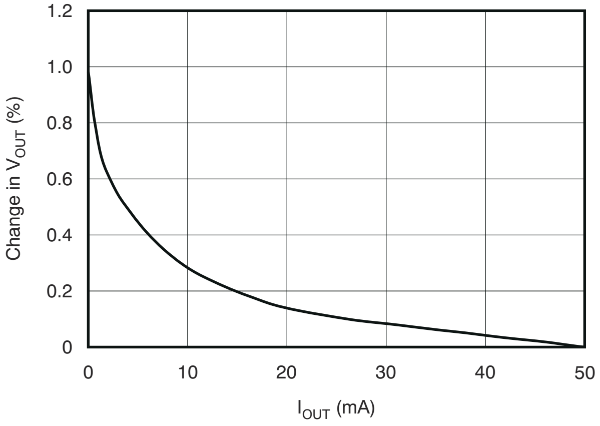


図 6-3. Load Regulation

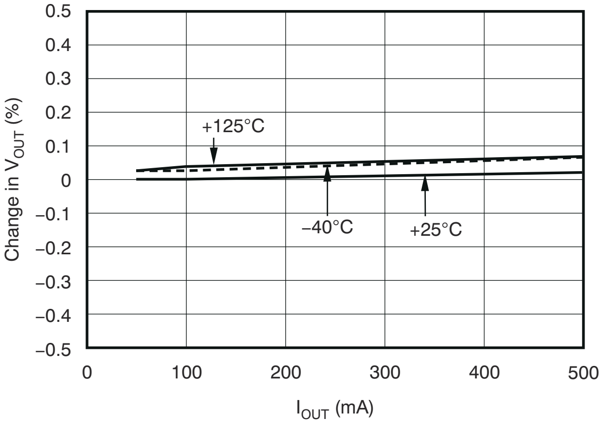


図 6-4. Load Regulation

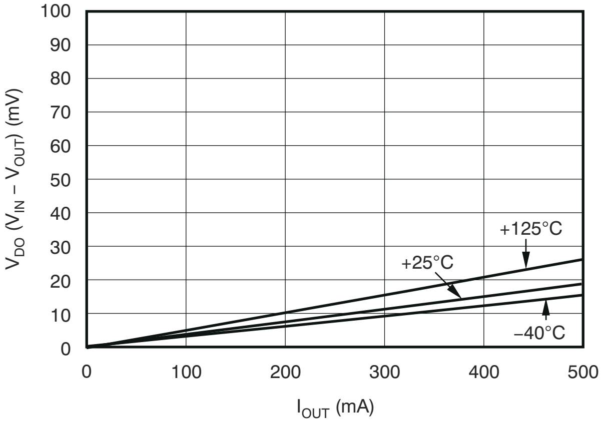


図 6-5. Dropout Voltage vs I_{OUT} and Temperature (T_J)

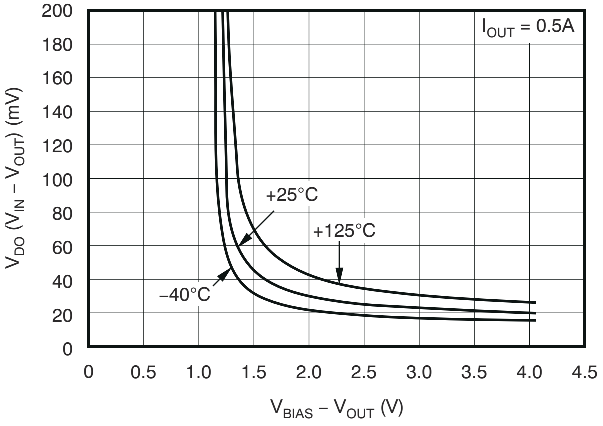


図 6-6. Dropout Voltage vs (V_{BIAS} – V_{OUT}) and Temperature (T_J)

6.7 Typical Characteristics: V_{EN} = V_{IN} (All Other Orderable Devices, Non-M3 Suffix) (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF (unless otherwise noted)

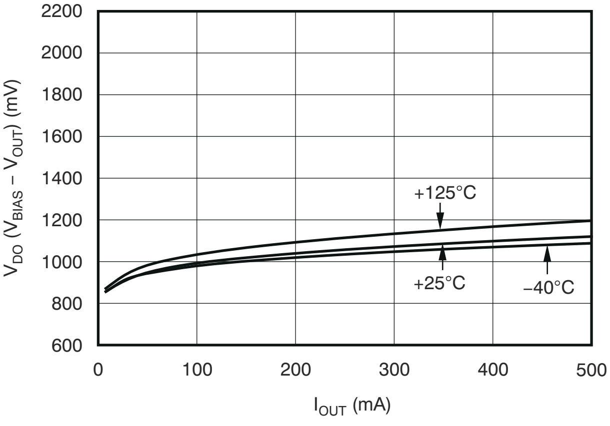


図 6-7. V_{BIAS} Dropout Voltage vs I_{OUT} and Temperature (T_J)

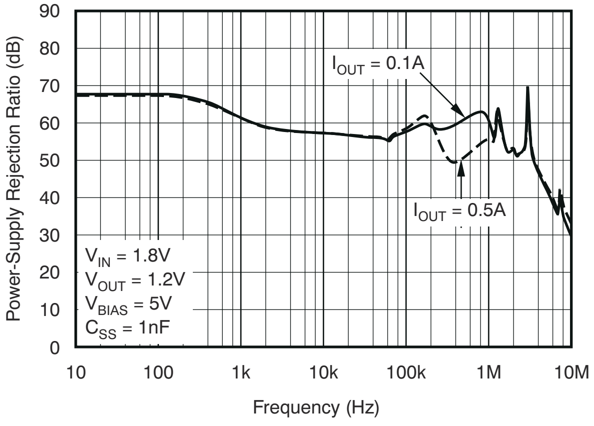


図 6-8. V_{BIAS} PSRR vs Frequency

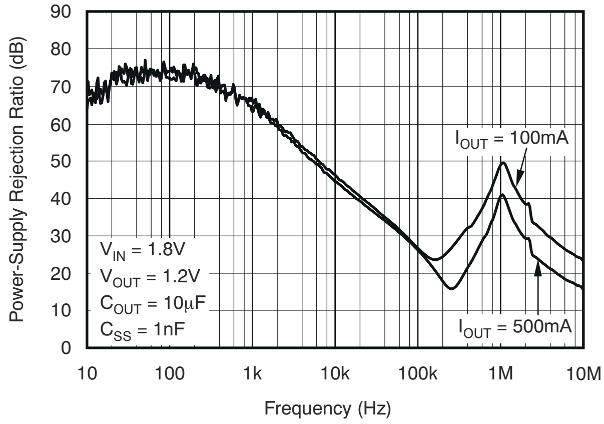


図 6-9. V_{IN} PSRR vs Frequency

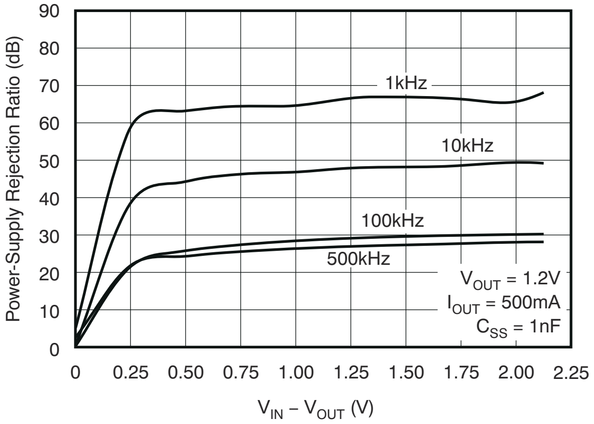


図 6-10. V_{IN} PSRR vs (V_{IN} – V_{OUT})

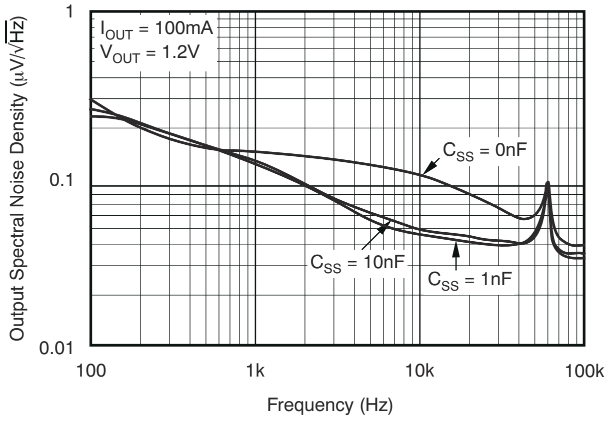


図 6-11. Noise Spectral Density

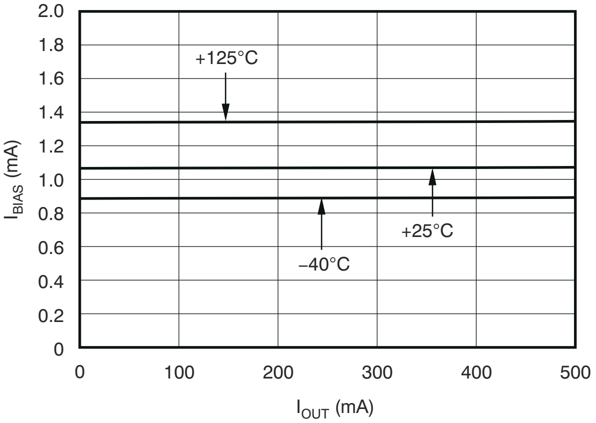


図 6-12. BIAS Pin Current vs I_{OUT} and Temperature (T_J)

6.7 Typical Characteristics: V_{EN} = V_{IN} (All Other Orderable Devices, Non-M3 Suffix) (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF (unless otherwise noted)

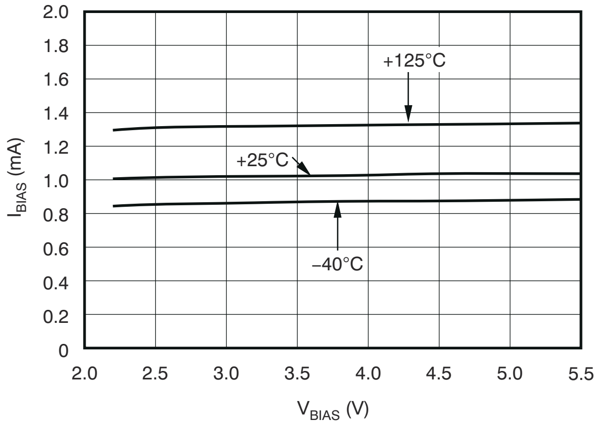


図 6-13. BIAS Pin Current vs V_{BIAS} and Temperature (T_J)

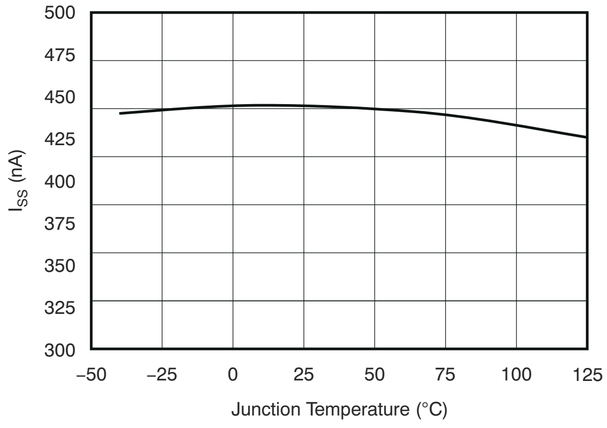


図 6-14. Soft-Start Charging Current (I_{SS}) vs Temperature (T_J)

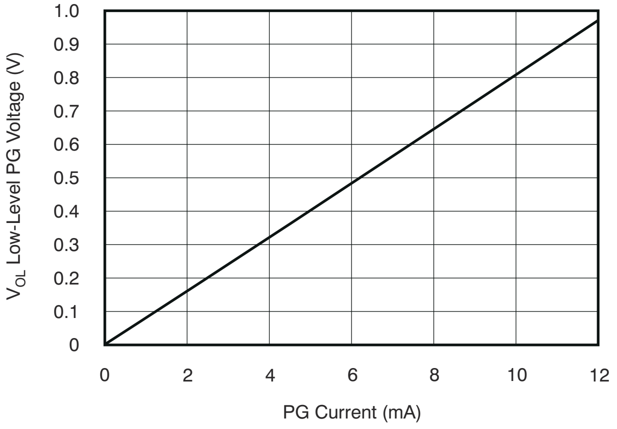


図 6-15. Low-Level PG Voltage vs Current

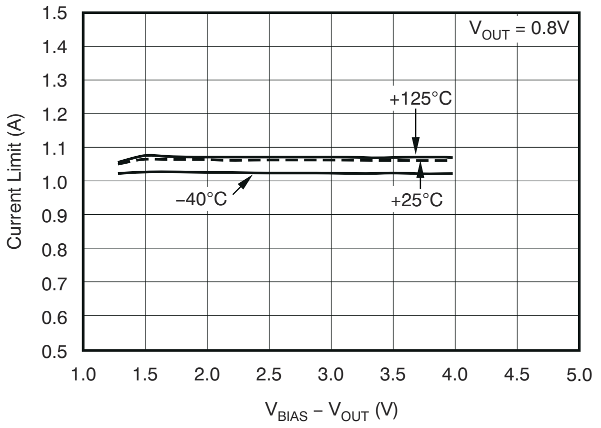


図 6-16. Current Limit vs (V_{BIAS} – V_{OUT})

6.8 Typical Characteristics: V_{EN} = V_{IN} = 1.8 V, V_{OUT} = 1.5 V (All Other Orderable Devices, Non-M3 Suffix)

at T_J = 25°C, V_{IN} = $V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, V_{EN} = V_{IN} = 1.8 V, V_{OUT} = 1.5 V, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF (unless otherwise noted)

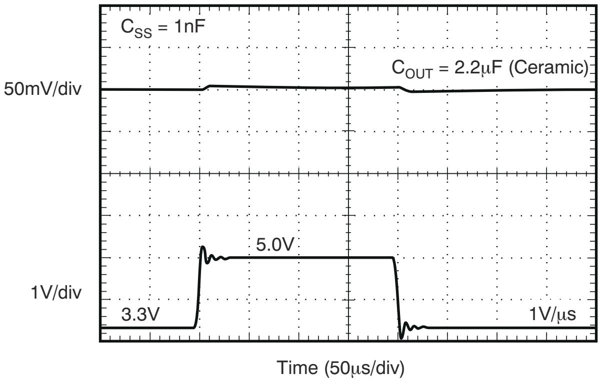


図 6-17. V_{BIAS} Line Transient

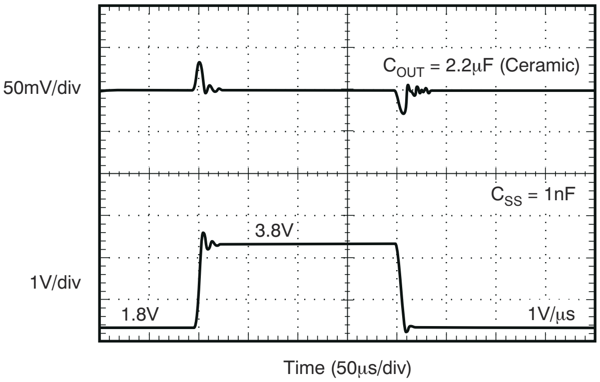


図 6-18. V_{IN} Line Transient

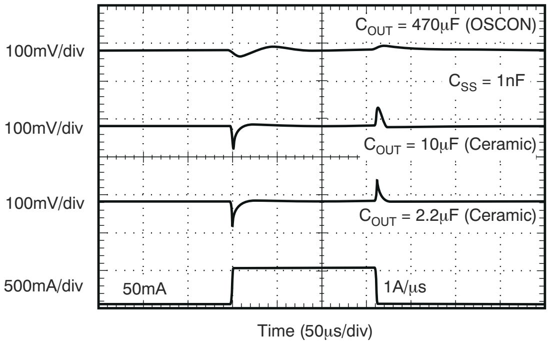


図 6-19. Output Load Transient Response

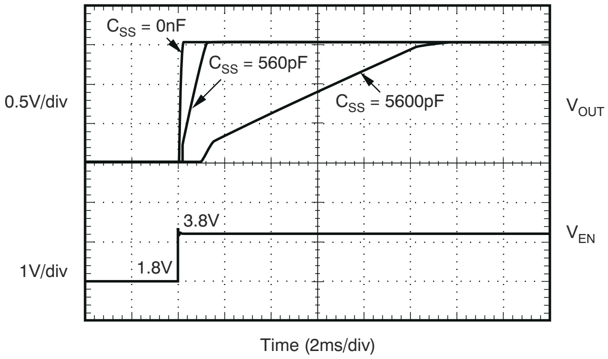


図 6-20. Turn-On Response

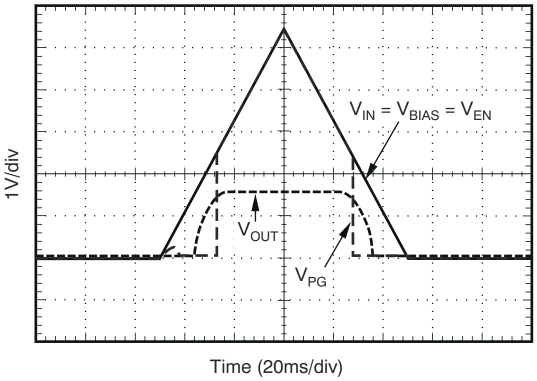


図 6-21. Power-Up and Power-Down

6.9 Typical Characteristics: I_{OUT} = 50 mA (M3 Suffix)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF (unless otherwise noted)

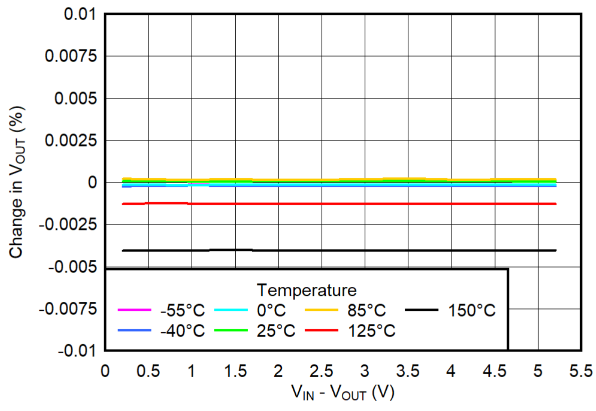


図 6-22. V_{IN} Line Regulation

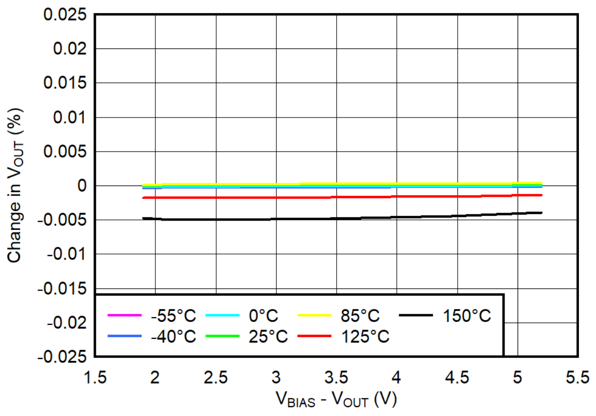


図 6-23. V_{BIAS} Line Regulation

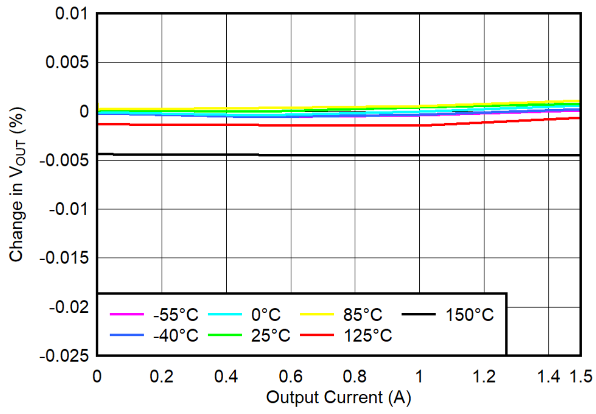


図 6-24. Load Regulation

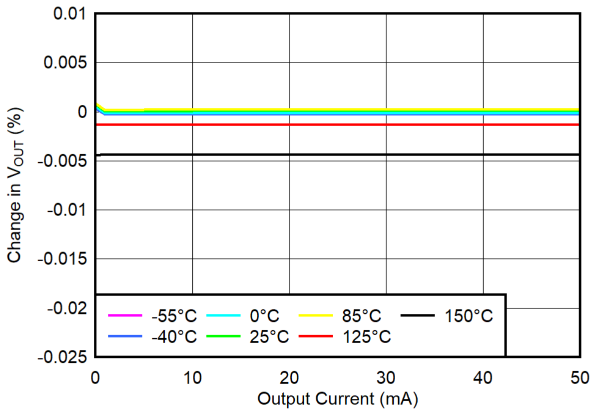


図 6-25. Load Regulation at Light Load

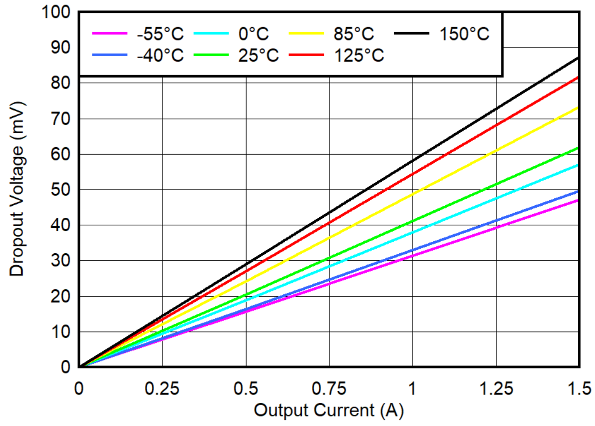


図 6-26. V_{IN} Dropout Voltage vs I_{OUT} and Temperature (T_J)

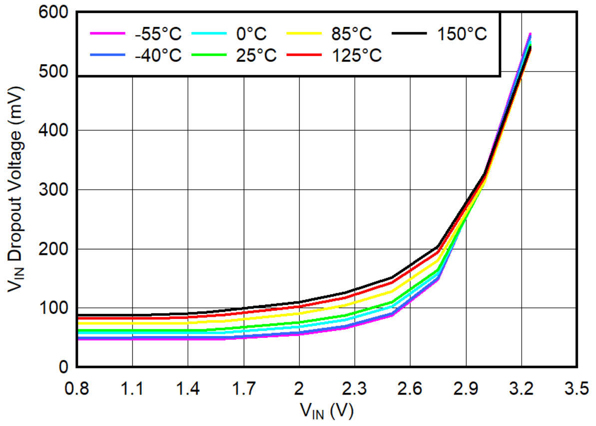


図 6-27. V_{IN} Dropout Voltage vs V_{IN} and Temperature (T_J) for I_{OUT} = 500 mA

6.9 Typical Characteristics: I_{OUT} = 50 mA (M3 Suffix) (continued)

at T_J = 25°C, $V_{IN} = V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, $V_{EN} = V_{IN}$, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF (unless otherwise noted)

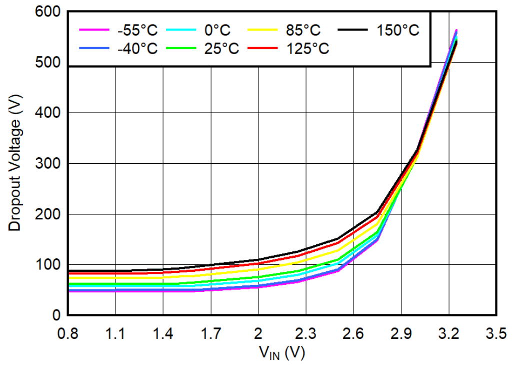


図 6-28. V_{IN} Dropout Voltage vs V_{IN} and Temperature (T_J) for I_{OUT} = 1.5 A

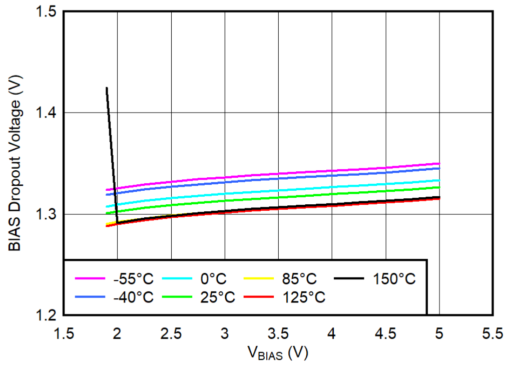


図 6-29. V_{IN} Dropout Voltage vs ($V_{BIAS} – V_{OUT}$) and Temperature (T_J)

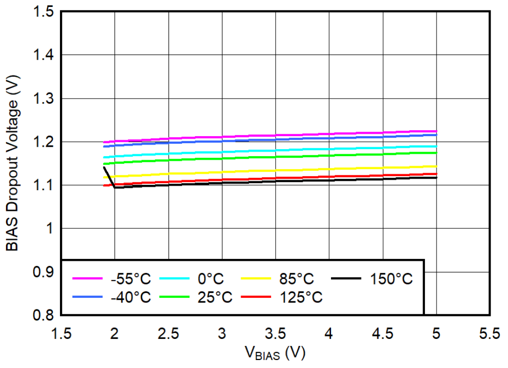


図 6-30. V_{IN} Dropout Voltage vs ($V_{BIAS} – V_{OUT}$) and Temperature (T_J)

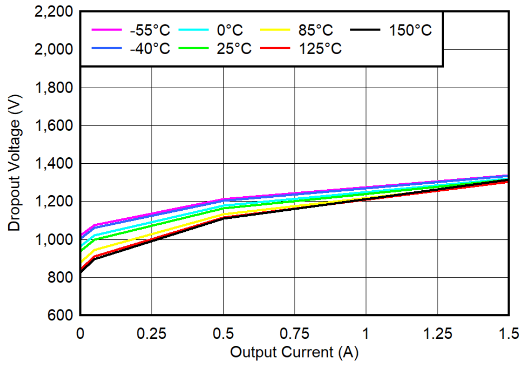


図 6-31. V_{BIAS} Dropout Voltage vs I_{OUT} and Temperature (T_J)

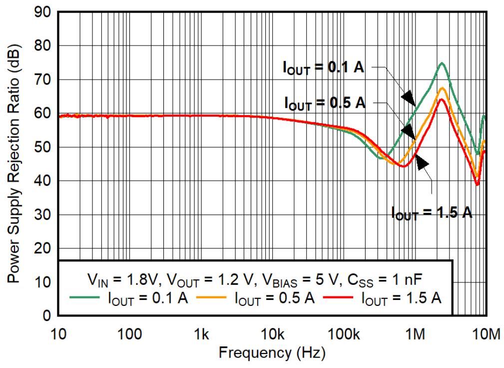


図 6-32. V_{BIAS} PSRR vs Frequency

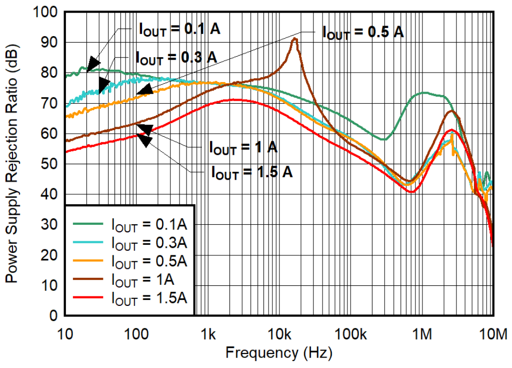


図 6-33. V_{IN} PSRR vs Frequency

6.9 Typical Characteristics: I_{OUT} = 50 mA (M3 Suffix) (continued)

at T_J = 25°C, $V_{IN} = V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, $V_{EN} = V_{IN}$, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF (unless otherwise noted)

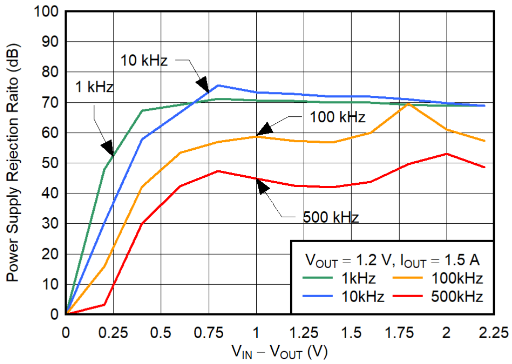


図 6-34. V_{IN} PSRR vs ($V_{IN} - V_{OUT}$)

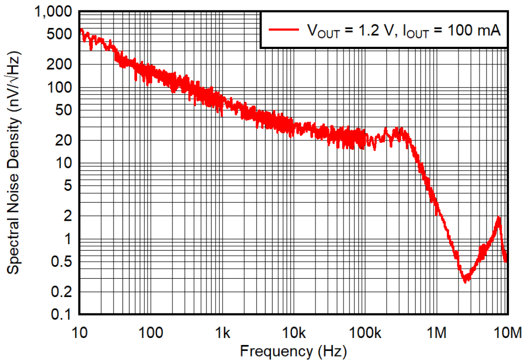


図 6-35. Noise Spectral Density

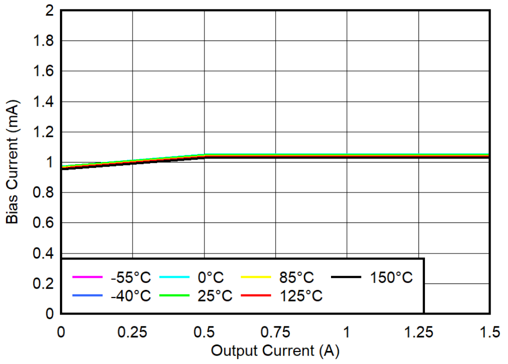


図 6-36. BIAS Pin Current vs Output Current and Temperature (T_J)

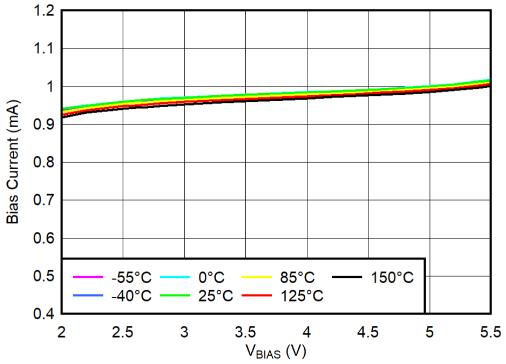


図 6-37. BIAS Pin Current vs V_{BIAS} and Temperature (T_J)

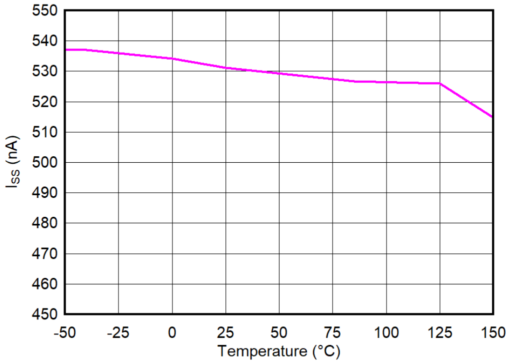


図 6-38. Soft-Start Charging Current (I_{SS}) vs Temperature (T_J)

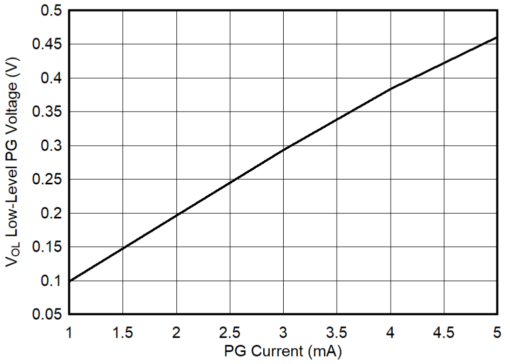


図 6-39. Low-Level PG Voltage vs Current

6.9 Typical Characteristics: I_{OUT} = 50 mA (M3 Suffix) (continued)

at T_J = 25°C, $V_{IN} = V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, $V_{EN} = V_{IN}$, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF (unless otherwise noted)

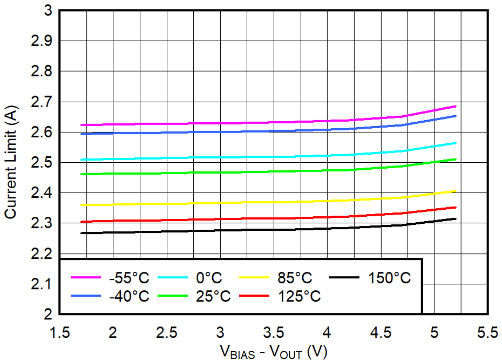


図 6-40. Current Limit vs ($V_{BIAS} - V_{OUT}$)

6.10 Typical Characteristics: V_{EN} = V_{IN} = 1.8 V, V_{OUT} = 1.5 V (M3 Suffix)

at T_J = 25°C, V_{IN} = $V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, V_{EN} = V_{IN} = 1.8 V, V_{OUT} = 1.5 V, C_{IN} = 1 μF, C_{BIAS} = 4.7 μF, and C_{OUT} = 10 μF (unless otherwise noted)

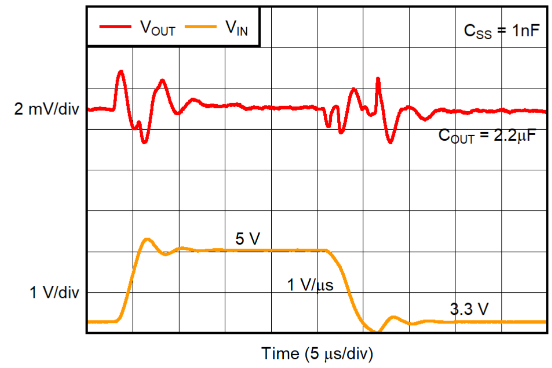


図 6-41. V_{BIAS} Line Transient

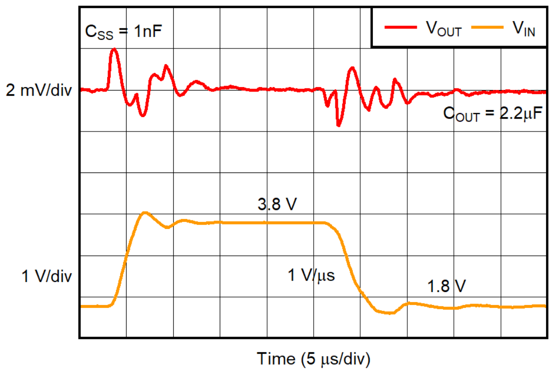


図 6-42. V_{IN} Line Transient

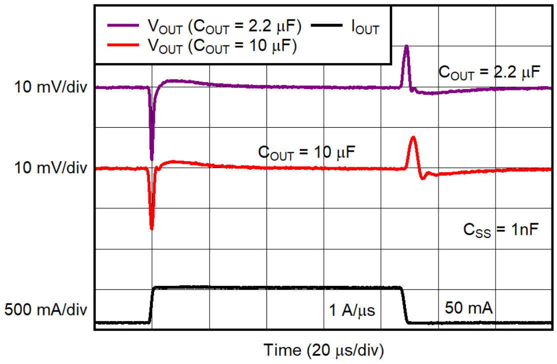


図 6-43. Output Load Transient Response

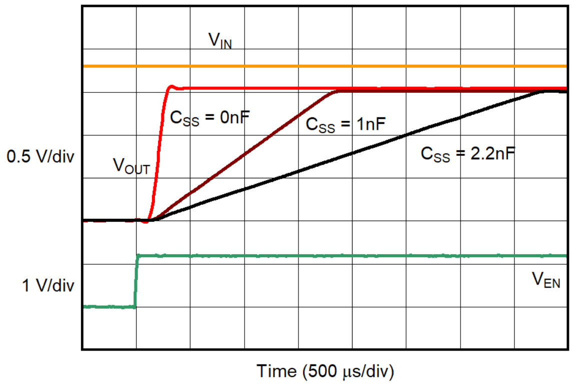


図 6-44. Turn-On Response

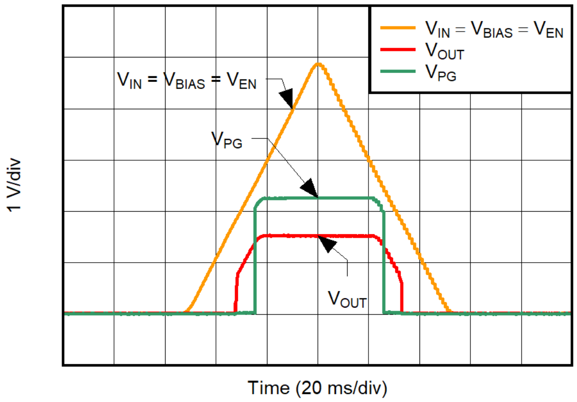


図 6-45. Power-Up and Power-Down

7 Detailed Description

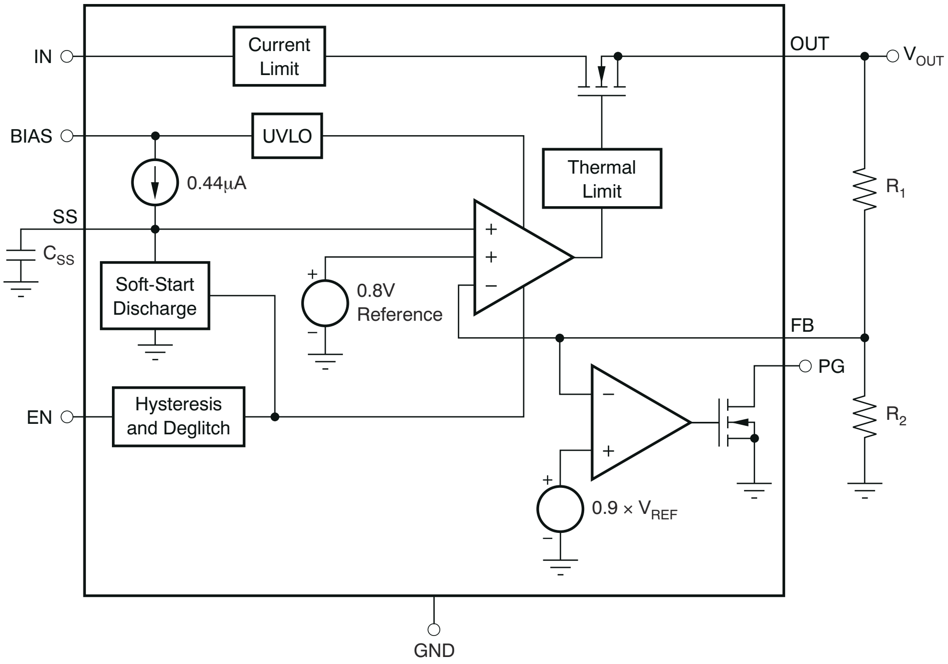
7.1 Overview

The TPS74701 is a low-dropout (LDO) regulator that features soft-start capability. This regulator uses a low current bias input to power all internal control circuitry, allowing the NMOS pass transistor to regulate very low input and output voltages.

The use of an NMOS pass transistor offers several critical advantages for many applications. Unlike a p-channel metal-oxide-semiconductor field effect transistor (PMOS) topology device, the output capacitor has little effect on loop stability. This architecture allows the TPS74701 to be stable with any capacitor type of value 2.2 μF or greater. Transient response is also superior to PMOS topologies, particularly for low V_{IN} applications.

The TPS74701 features a programmable voltage-controlled soft-start circuit that provides a smooth, monotonic start-up and limits start-up inrush currents that can be caused by large capacitive loads. A power-good (PG) output is available to allow supply monitoring and sequencing of other supplies. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low V_{IN} and V_{OUT} capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often present in processor-intensive systems.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Programmable Soft-Start

The TPS74701 features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor (C_{SS}). This feature is important for many applications because soft-start eliminates power-up initialization problems when powering FPGAs, DSPs, or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transient events to the input power bus.

To achieve a linear and monotonic soft-start, the TPS74701 error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage exceeds the internal reference. The soft-start ramp time depends on the soft-start charging current (I_{SS}), soft-start capacitance (C_{SS}), and the internal reference voltage (V_{REF}), and can be calculated using 式 1:

$$t_{SS} = \frac{(V_{REF} \times C_{SS})}{I_{SS}} \tag{1}$$

If large output capacitors are used, the device current limit (I_{CL}) and the output capacitor can set the start-up time. In this case, the start-up time is given by 式 2:

$$t_{SSCL} = \frac{(V_{OUT(NOM)} \times C_{OUT})}{I_{CL(MIN)}} \tag{2}$$

where:

- $V_{OUT(NOM)}$ is the nominal output voltage
- C_{OUT} is the output capacitance
- $I_{CL(MIN)}$ is the minimum current limit for the device

In applications where monotonic start-up is required, the soft-start time given by 式 1 must be set greater than 式 2.

The maximum recommended soft-start capacitor is 0.015 μF. Larger soft-start capacitors can be used, and do not damage the device; however, the soft-start capacitor discharge circuit can possibly be unable to fully discharge the soft-start capacitor when enabled.

Soft-start capacitors larger than 0.015 μF can be a problem in applications where the enable pin must be rapidly pulsed while still requiring the device to soft-start from ground. C_{SS} must be low-leakage; X7R, X5R, or C0G dielectric materials are preferred. See 表 8-2 for suggested soft-start capacitor values.

7.3.2 Enable and Shutdown

The enable (EN) pin is active high and is compatible with standard digital signaling levels. V_{EN} below 0.4 V turns the regulator off, while V_{EN} above 1.1 V turns the regulator on. Unlike many regulators, the enable circuitry has hysteresis and deglitching for use with relatively slowly ramping analog signals. This configuration allows the TPS74701 to be enabled by connecting the output of another supply to the EN pin. The enable circuitry typically has 50 mV of hysteresis and a deglitch circuit to help avoid on-off cycling as a result of small glitches in the V_{EN} signal.

The enable threshold is typically 0.8 V and varies with temperature and process variations. Temperature variation is approximately –1 mV/°C; process variation accounts for most of the rest of the variation to the 0.4-V and 1.1-V limits. If precise turn-on timing is required, a fast rise-time signal must be used to enable the TPS74701.

If not used, EN can be connected to either IN or BIAS. If EN is connected to IN, connect this pin as close as possible to the largest capacitance on the input to prevent voltage droops on that line from triggering the enable circuit.

7.3.3 Power Good

The power-good (PG) pin is an open-drain output and can be connected to any 5.5-V or lower rail through an external pullup resistor. This pin requires at least 1.1 V on V_{BIAS} to have a valid output. The PG output is high-impedance when V_{OUT} is greater than V_{IT} + V_{HYS}. If V_{OUT} drops below V_{IT} or if V_{BIAS} drops below 1.9 V, the open-drain output turns on and pulls the PG output low. The PG pin also asserts when the device is disabled. The recommended operating condition of the PG pin sink current is up to 1 mA, so the pullup resistor for PG must be in the range of 10 kΩ to 1 MΩ. If output voltage monitoring is not needed, the PG pin can be left floating.

7.3.4 Internal Current Limit

The TPS74701 features a factory-trimmed, accurate current limit that is flat over temperature and supply voltage. The current limit allows the device to supply surges of up to 1 A and maintain regulation. The current limit responds in approximately 10 µs to reduce the current during a short-circuit fault.

The internal current limit protection circuitry of the TPS74701 is designed to protect against overload conditions. This circuitry is not intended to allow operation above the rated current of the device. Continuously running the TPS74701 above the rated current degrades device reliability.

7.3.5 Thermal Shutdown

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting the regulator from damage as a result of overheating.

Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heat sinking. For reliable operation, junction temperature must be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 40°C above the maximum expected ambient condition of the application. This condition produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS74701 is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the TPS74701 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

表 7-1 shows the conditions that lead to the different modes of operation.

表 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER				
	V_{IN}	V_{EN}	V_{BIAS}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO} (V_{IN})$	$V_{EN} > V_{EN, HI}$	$V_{BIAS} \geq V_{OUT} + 1.39$ V	$I_{OUT} < I_{CL}$	$T_J < 125°C$
Dropout mode	$V_{IN} < V_{OUT(nom)} + V_{DO} (V_{IN})$	$V_{EN} > V_{EN, HI}$	$V_{BIAS} < V_{OUT} + 1.39$ V	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	$V_{IN} < V_{IN(min)}$	$V_{EN} < V_{EN, LO}$	$V_{BIAS} < V_{BIAS(min)}$	—	$T_J > 165°C$

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage and bias voltage are both at least at the respective minimum specifications
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold
- The output current is less than the current limit
- The device junction temperature is less than the maximum specified junction temperature

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass transistor is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The input or bias voltages are below the respective minimum specifications
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold
- The device junction temperature is greater than the thermal shutdown temperature

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

R_1 and R_2 can be calculated for any output voltage using the formula in 図 8-4. 表 8-1 lists sample resistor values of common output voltages. To achieve the maximum accuracy specifications, R_2 must be less than or equal to 4.99 kΩ. 表 8-2 lists the capacitor values for setting the soft-start time.

表 8-1. Standard 1% Resistor Values for Programming the Output Voltage(1)

R_1 (kΩ)	R_2 (kΩ)	V_{OUT} (V)
Short	Open	0.8
0.619	4.99	0.9
1.13	4.53	1
1.37	4.42	1.05
1.87	4.99	1.1
2.49	4.99	1.2
4.12	4.75	1.5
3.57	2.87	1.8
3.57	1.69	2.5
3.57	1.15	3.3

(1) $V_{OUT} = 0.8 \times (1 + R_1 / R_2)$.

表 8-2. Standard Capacitor Values for Programming the Soft-Start Time(1)

C_{SS}	SOFT-START TIME
Open	0.1 ms
270 pF	0.5 ms
560 pF	1 ms
2.7 nF	5 ms
5.6 nF	10 ms
0.01 μF	18 ms

(1) $$t_{SS}(s) = \frac{V_{REF} \times C_{SS}}{I_{SS}} = \frac{0.8V \times C_{SS}(F)}{0.44\mu A}$$ where $t_{SS}(s)$ = soft-start time in seconds.

8.1.1 Input, Output, and Bias Capacitor Requirements

The device is designed to be stable for all available types and values of output capacitors greater than or equal to 2.2 μF. The device is also stable with multiple capacitors in parallel, which can be of any type or value.

The capacitance required on the IN and BIAS pins strongly depends on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for V_{IN} and V_{BIAS} is 1 μF. If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for V_{BIAS} is 4.7 μF. Use good-quality, low-ESR capacitors on the input; ceramic X5R and X7R capacitors are preferred. Place these capacitors as close the pins as possible for optimum performance.

8.1.2 Transient Response

The TPS74701 was designed to have excellent transient response for most applications with a small amount of output capacitance. In some cases, the transient response can be limited by the transient response of the input supply. This limitation is especially true in applications where the difference between the input and output is less than 300 mV. In this case, adding additional input capacitance improves the transient response much more than just adding additional output capacitance otherwise does. With a solid input supply, adding additional output capacitance reduces undershoot and overshoot during a transient event; see 図 6-43 in the *Typical Characteristics* section. Because the TPS74701 is stable with output capacitors as low as 2.2 µF, many applications can then need very little capacitance at the LDO output. For these applications, local bypass capacitance for the powered device can be sufficient to meet the transient requirements of the application. This design reduces the total solution cost by avoiding the need to use expensive, high-value capacitors at the LDO output.

8.1.3 Dropout Voltage

The TPS74701 offers very low dropout performance, making the device designed for high-current, low V_{IN} and low V_{OUT} applications. The low dropout of the TPS74701 allows the device to be used in place of a DC/DC converter and still achieve good efficiency. This feature provides designers with the power architecture for applications to achieve the smallest, simplest, and lowest cost solution.

There are two different specifications for dropout voltage with the TPS74701. The first specification (shown in 図 8-1) is referred to as *V_{IN} dropout* and is used when an external bias voltage is applied to achieve low dropout. This specification assumes that V_{BIAS} is at least 1.39 V[1] above V_{OUT}, which is the case for V_{BIAS} when powered by a 3.3-V rail with 5% tolerance and with V_{OUT} = 1.5 V. If V_{BIAS} is higher than V_{OUT} +1.39 V[1], V_{IN} dropout is less than specified.[1]

The second specification (shown in 図 8-2) is referred to as *V_{BIAS} dropout* and applies to applications where IN and BIAS are tied together. This option allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. Dropout is limited by BIAS in these applications because V_{BIAS} provides the gate drive to the pass transistor; therefore, V_{BIAS} must be 1.39 V above V_{OUT}. Because of this usage, IN and BIAS tied together easily consume a huge amount of power. Pay attention not to exceed the power rating of the device package.

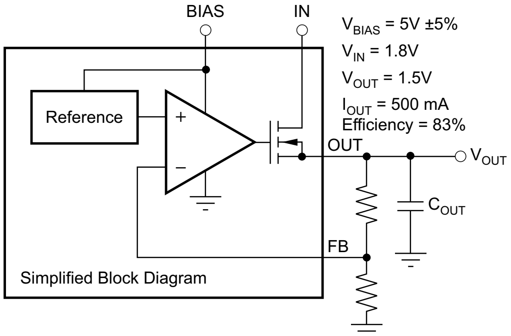


図 8-1. Typical Application of the TPS74701 Using an Auxiliary Bias Rail

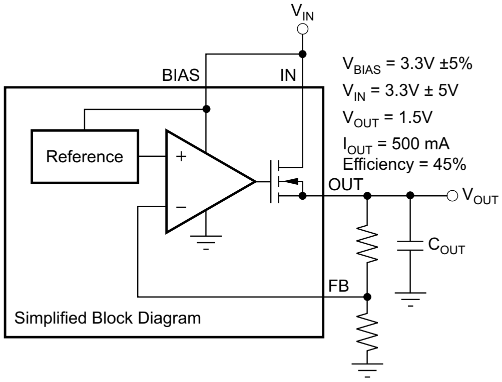


図 8-2. Typical Application of the TPS74701 Without an Auxiliary Bias Rail

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[1] 1.62 V is a test condition of this device and can be adjusted by referring to 図 6-6.

8.1.4 Sequencing Requirements

V_{IN}, V_{BIAS}, and V_{EN} can be sequenced in any order without causing damage to the device. However, for the soft-start function to work as intended, certain sequencing rules must be applied. Connecting EN to IN is acceptable for most applications, as long as V_{IN} is greater than 1.1 V and the ramp rate of V_{IN} and V_{BIAS} is faster than the set soft-start ramp rate. If the ramp rate of the input sources is slower than the set soft-start time, the output tracks the slower supply minus the dropout voltage until the set output voltage is reached. If EN is connected to BIAS, the device soft-starts as programmed, provided that V_{IN} is present before V_{BIAS}. If V_{BIAS} and V_{EN} are present before V_{IN} is applied and the set soft-start time has expired, then V_{OUT} tracks V_{IN}. If the soft-start time has not expired, the output tracks V_{IN} until V_{OUT} reaches the value set by the charging soft-start capacitor. 図 8-3 shows the use of an RC-delay circuit to hold off V_{EN} until V_{BIAS} has ramped. This technique can also be used to drive EN from V_{IN}. An external control signal can also be used to enable the device after V_{IN} and V_{BIAS} are present.

注

When V_{BIAS} and V_{EN} are present and V_{IN} is not supplied, this device outputs approximately 50 µA of current from OUT. Although this condition does not cause any damage to the device, the output current can charge up the OUT node if total resistance between OUT and GND (including external feedback resistors) is greater than 10 kΩ.

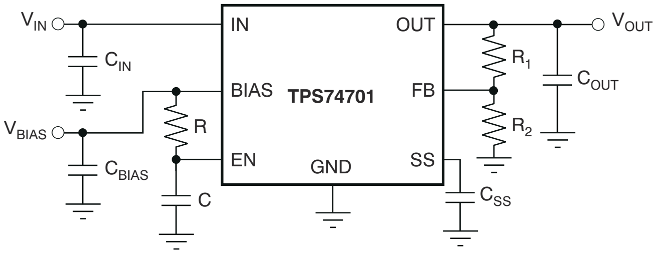


図 8-3. Soft-Start Delay Using an RC Circuit to Enable the Device

8.1.5 Output Noise

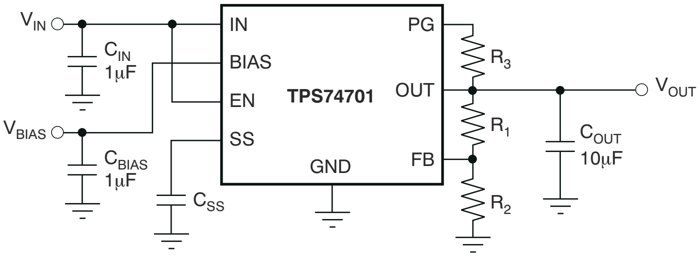
The TPS74701 provides low-output noise when a soft-start capacitor is used. When the device reaches the end of the soft-start cycle, the soft-start capacitor serves as a filter for the internal reference. By using a 0.001-µF soft-start capacitor, the output noise is reduced by half and is typically 30 μV_{RMS} for a 1.2-V output (10 Hz to 100 kHz). Further increasing C_{SS} has little effect on noise. Because most of the output noise is generated by the internal reference, the noise is a function of the set output voltage. The RMS noise with a 0.001-µF soft-start capacitor is given in 式 3:

$$V_N(\mu V_{RMS}) = 25\left(\frac{\mu V_{RMS}}{V}\right) x\ V_{OUT}(V) \tag{3}$$

The low-output noise of the TPS74701 makes the device a good choice for powering transceivers, PLLs, or other noise-sensitive circuitry.

8.2 Typical Application

図 8-4 shows a typical application circuit for the TPS74701 adjustable output device.



$$V_{OUT} = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

図 8-4. Typical Application Circuit for the TPS74701 (Adjustable)

8.2.1 Design Requirements

表 8-3 shows the design parameters for this application.

表 8-3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	1.8 V ± 10%
V_{BIAS}	3.3 V ±10%
V_{OUT}	1.5 V ± 3%
I_{OUT}	500 mA
Start-up time	< 2 ms

8.2.2 Detailed Design Procedure

1. Select R_1 and R_2 based on the required output voltage. 表 8-1 gives example calculations for many common output voltages.
2. Select C_{SS} to be the highest capacitance while still achieving the desired start-up time. 表 8-2 gives examples of this calculation.
3. Select a minimum of a 2.2-µF ceramic output capacitor. Increased output capacitance helps the output load transient response. 図 8-6 gives examples of the load transient response with different output capacitor values and types.

8.2.3 Application Curves

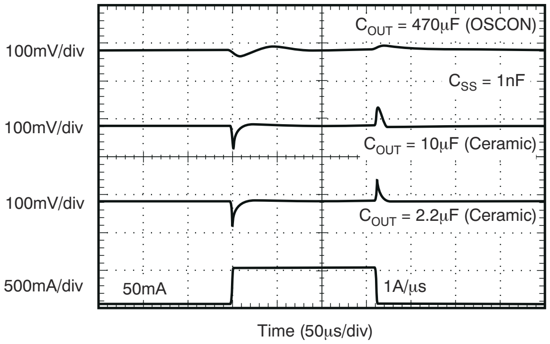


図 8-5. Output Load Transient Response

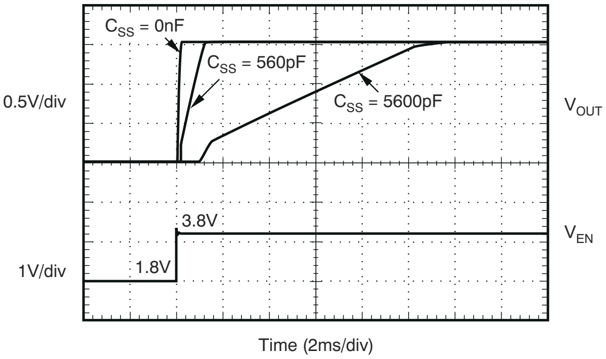


図 8-6. Turn-On Response

8.3 Power Supply Recommendations

The TPS74701 is designed to operate from an input voltage up to 5.5 V, provided the bias rail is at least 1.39-V higher than the input supply and dropout requirements are met. The bias rail and the input supply must both provide adequate headroom and current for the device to operate normally. Connect a low-output impedance power supply directly to the IN pin of the TPS74701. This supply must have at least 1 μF of capacitance near the IN pin for optimal performance. A supply with similar requirements must also be connected directly to the bias rail with a separate 1-μF or larger capacitor. If the IN pin is tied to the bias pin, a minimum 4.7 μF of capacitance is needed for performance. To increase the overall PSRR of the solution at higher frequencies, use a pi-filter or ferrite bead before the input capacitor.

8.4 Layout

8.4.1 Layout Guidelines

An optimal layout can greatly improve transient performance, PSRR, and noise. To minimize the voltage droop on the input of the device during load transients, connect the capacitance on IN, OUT, and BIAS as close as possible to the device. If BIAS is connected to IN, connect BIAS as close to the input supply as possible. This connection minimizes the voltage droop on BIAS during transient conditions and can improve the turn-on response.

8.4.1.1 Power Dissipation

An optimal layout can greatly improve transient performance, PSRR, and noise. To minimize the voltage drop on the input of the device during load transients, the capacitance on IN and BIAS must be connected as close as possible to the device. This capacitance also minimizes the effects of parasitic inductance and resistance of the input source and can therefore improve stability. To achieve optimal transient performance and accuracy, the top side of R_1 in 図 8-4 must be connected as close as possible to the load. If BIAS is connected to IN, connect BIAS as close to the sense point of the input supply as possible. This connection minimizes the voltage drop on BIAS during transient conditions and can improve the turn-on response.

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the thermal pad is critical to avoiding thermal shutdown and ensuring reliable operation. Power dissipation of the device depends on input voltage and load conditions and can be calculated using 式 4:

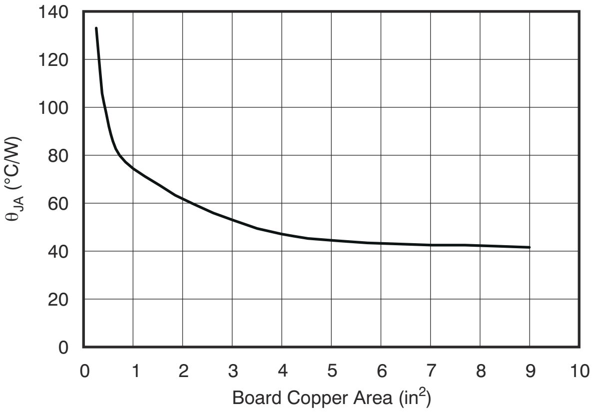
$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{4}$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the VSON (DRC) package, the primary conduction path for heat is through the exposed pad to the printed-circuit-board (PCB). The pad can be connected to ground or be left floating; however, the pad must be attached to an appropriate amount of copper PCB area to make sure the device does not overheat. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using 式 5:

$$R_{\theta JA} = \frac{(+125°C - T_A)}{P_D} \tag{5}$$

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heat sinking can be estimated using 図 8-7.



$R_{\theta JA}$ value at board size of 9 in^2 (that is, 3 inches × 3 inches) is a JEDEC standard.

図 8-7. $R_{\theta JA}$ vs Board Size

図 8-7 shows the variation of $R_{\theta JA}$ as a function of ground plane copper area in the board. This figure is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and is not meant to be used to estimate actual thermal performance in real application environments.

注

When the device is mounted on an application PCB, TI strongly recommends using Ψ_{JT} and Ψ_{JB}, as explained in the *Estimating Junction Temperature* section.

8.4.1.2 Estimating Junction Temperature

Using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in 式 6). For backwards compatibility, an older *$R_{\theta JC}$, Top* parameter is listed as well.

$$\begin{aligned} \Psi_{JT}&: \quad T_J = T_T + \Psi_{JT} \bullet P_D \\ \Psi_{JB}&: \quad T_J = T_B + \Psi_{JB} \bullet P_D \end{aligned} \tag{6}$$

where:

- P_D is the power dissipation shown by 式 5
- T_T is the temperature at the center-top of the device package
- T_B is the PCB temperature measured 1mm away from the device package *on the PCB surface* (as 図 8-9 shows)

注

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the *Using New Thermal Metrics* application note, available for download at www.ti.com.

From 図 8-8, the new thermal metrics (Ψ_{JT} and Ψ_{JB}) obviously have very little dependency on board size. That is, using Ψ_{JT} or Ψ_{JB} with 式 6 is a good way to estimate T_J by simply measuring T_T or T_B, regardless of the application board size.

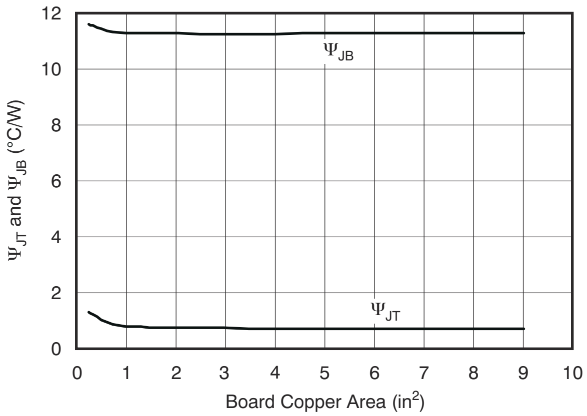


図 8-8. Ψ_{JT} and Ψ_{JB} vs Board Size

For a more detailed discussion of why TI does not recommend using $R_{\theta JC(top)}$ to determine thermal characteristics, see the *Using New Thermal Metrics* application note, available for download at www.ti.com. For further information, see the *Semiconductor and IC Package Thermal Metrics* application note, also available on the TI website.

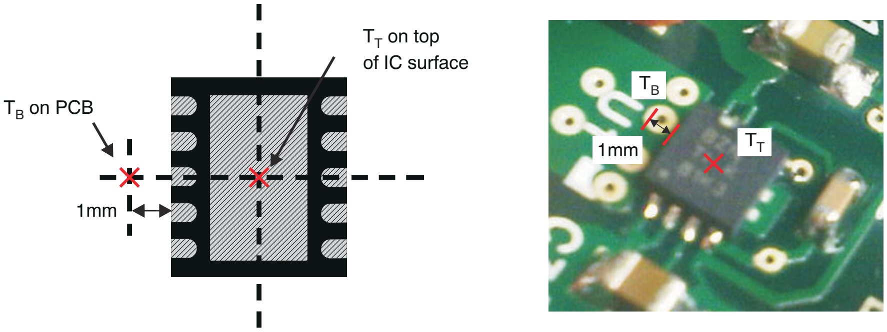


図 8-9. Measuring Points for T_T and T_B

8.4.2 Layout Example

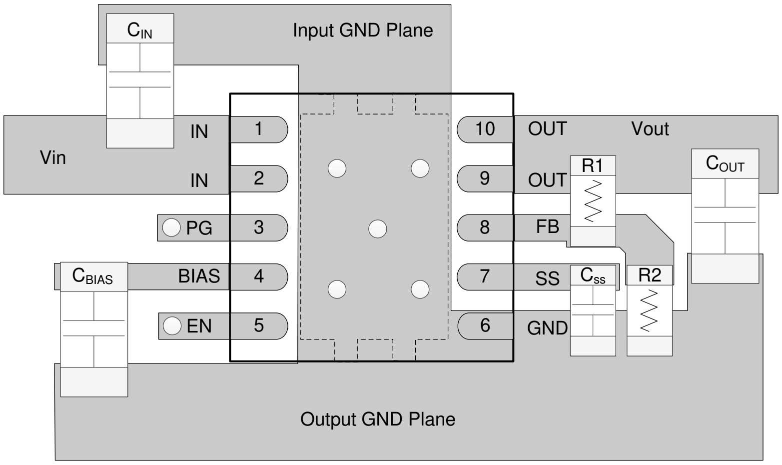


図 8-10. TPS547 Layout Recommendation

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS74701. The TPS74701EVM-177 evaluation module (and related user guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

9.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for TPS74701 is available through the product folders under *Simulation Models*.

9.1.2 Device Nomenclature

表 9-1. Device Nomenclature(1)

PRODUCT	V_{OUT} (2)
TPS747**xxyyyz**	**xx** is the nominal output voltage (for example, 12 = 1.2 V, 15 = 1.5 V, 01 = Adjustable).(3) **YYY** is the package designator. **Z** is the package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Fixed output voltages from 0.8 V to 3.3 V are available; minimum order quantities may apply. Contact factory for details and availability.
(3) For fixed 0.8-V operation, tie FB to OUT.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Using New Thermal Metrics* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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すべての商標は、それぞれの所有者に帰属します。

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この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS74701DRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CEG	Samples
TPS74701DRCRG4	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CEG	Samples
TPS74701DRCRM3	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CEG	Samples
TPS74701DRCT	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CEG	Samples
TPS74701DRCTG4	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CEG	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS74701 :

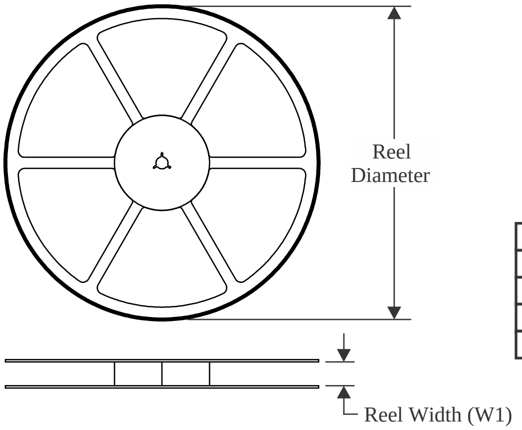
- Automotive : TPS74701-Q1

NOTE: Qualified Version Definitions:

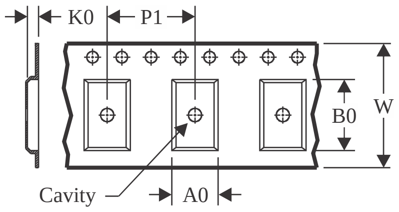
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

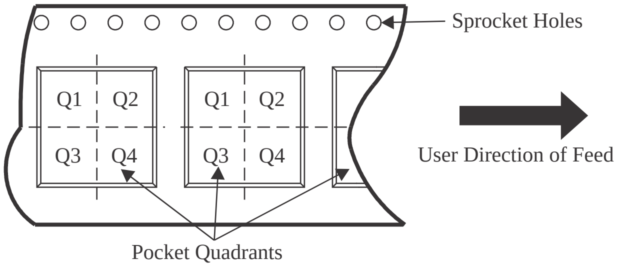


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

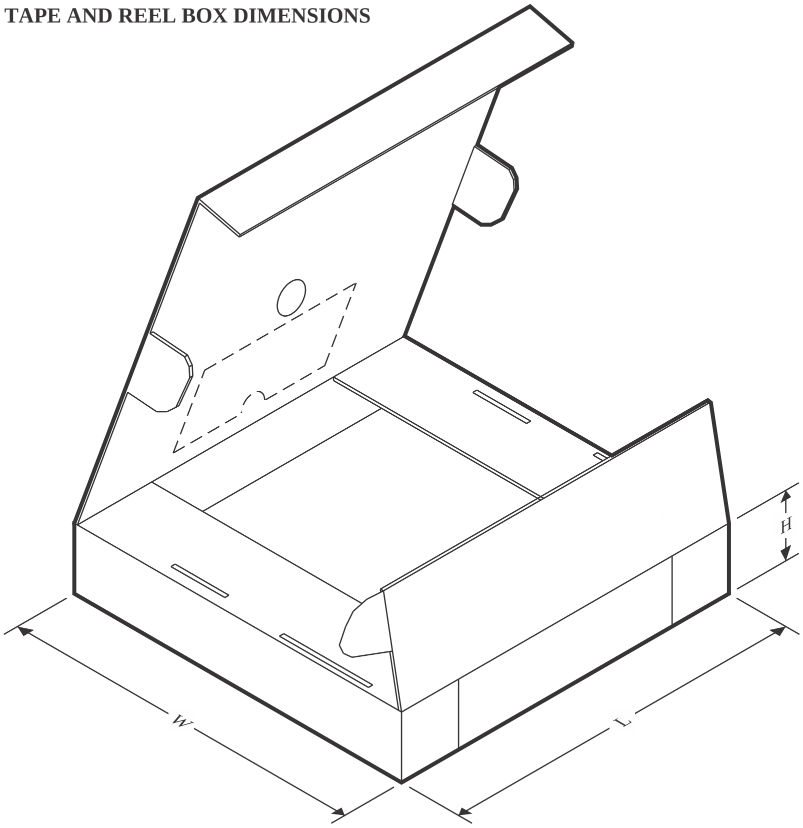
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS74701DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74701DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74701DRCRM3	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74701DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74701DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS74701DRCR	VSON	DRC	10	3000	356.0	356.0	35.0
TPS74701DRCR	VSON	DRC	10	3000	346.0	346.0	33.0
TPS74701DRCRM3	VSON	DRC	10	3000	367.0	367.0	35.0
TPS74701DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS74701DRCT	VSON	DRC	10	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

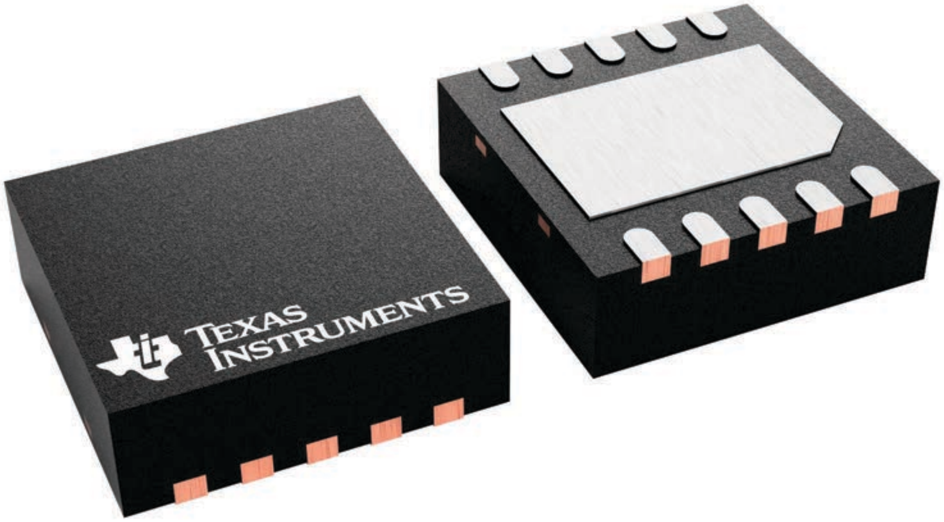
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

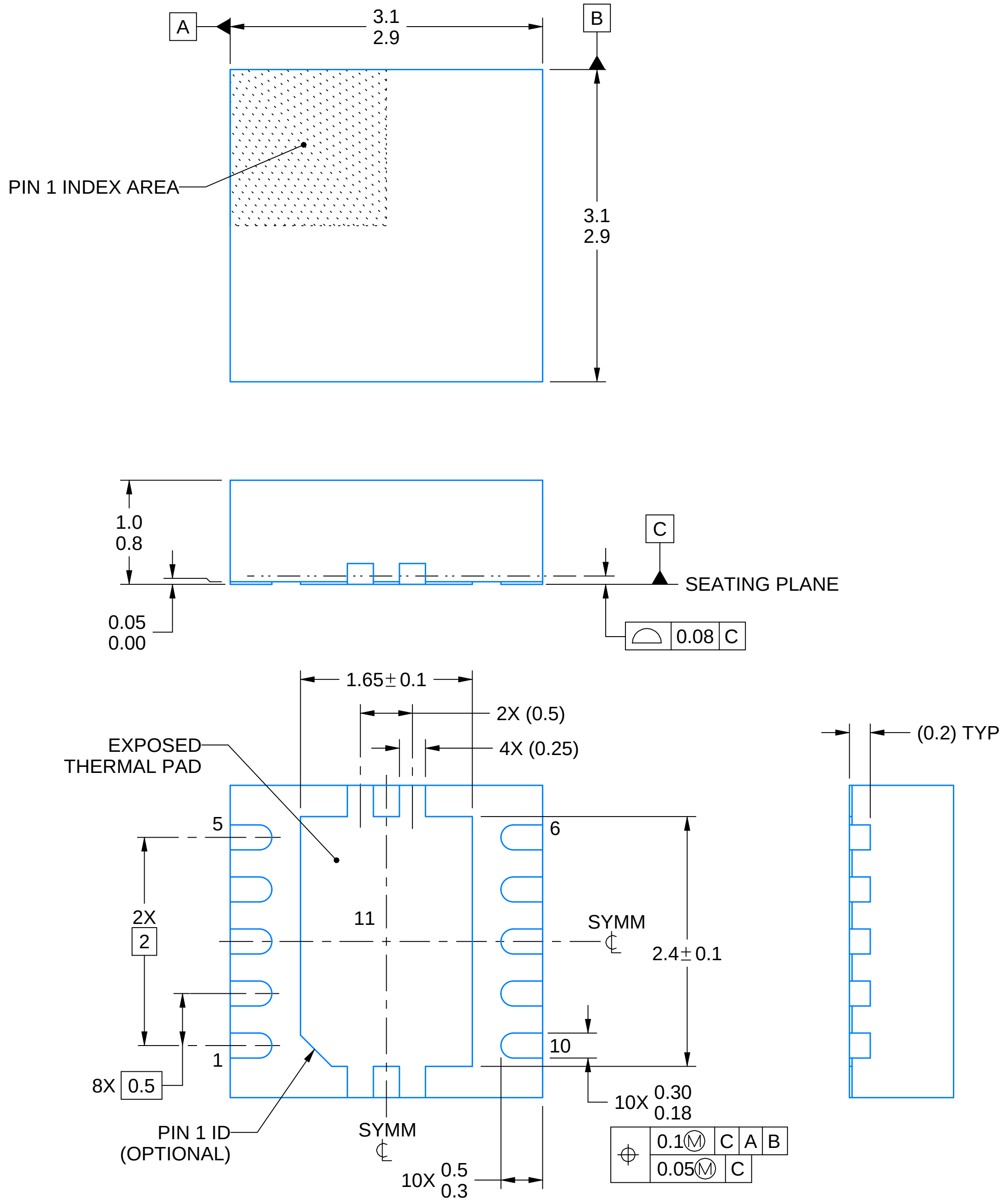


PACKAGE OUTLINE

DRC0010J

VSON - 1 mm max height

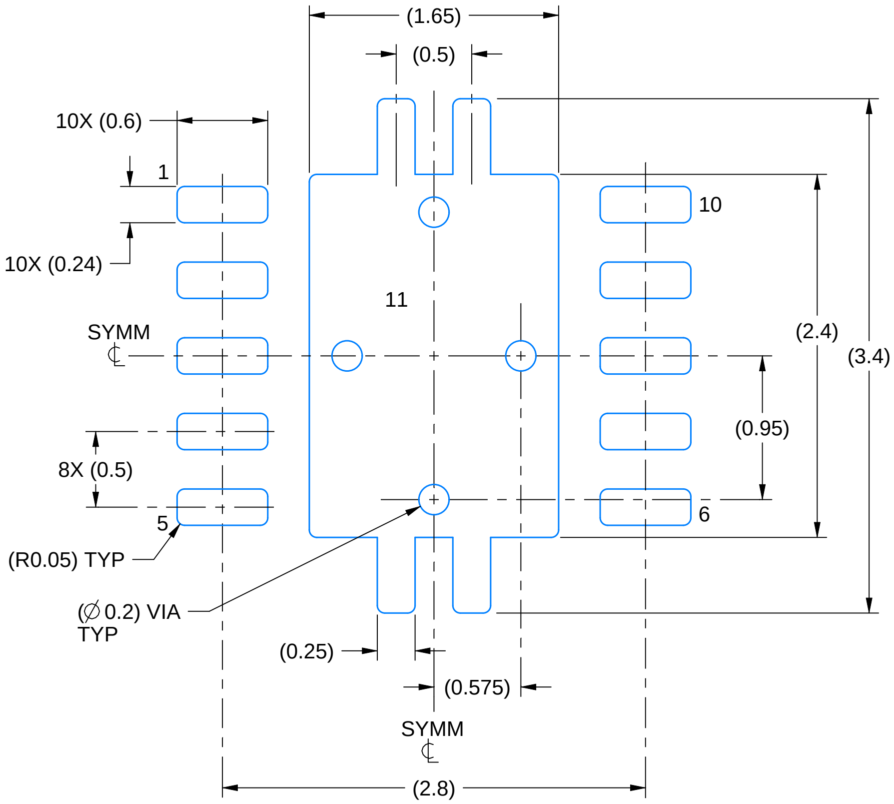
PLASTIC SMALL OUTLINE - NO LEAD



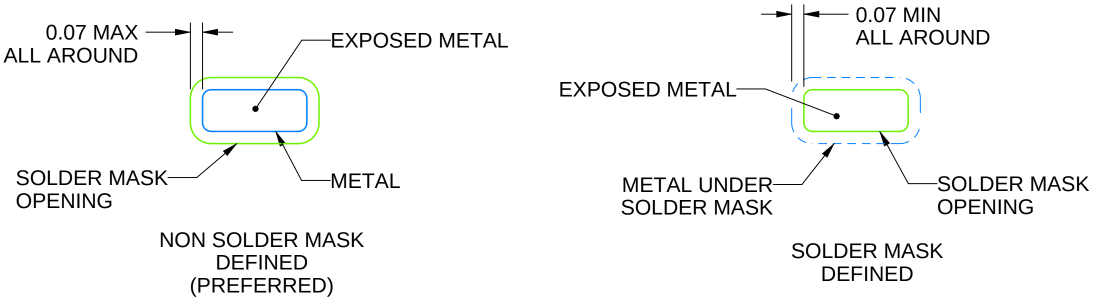
4218878/B 07/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



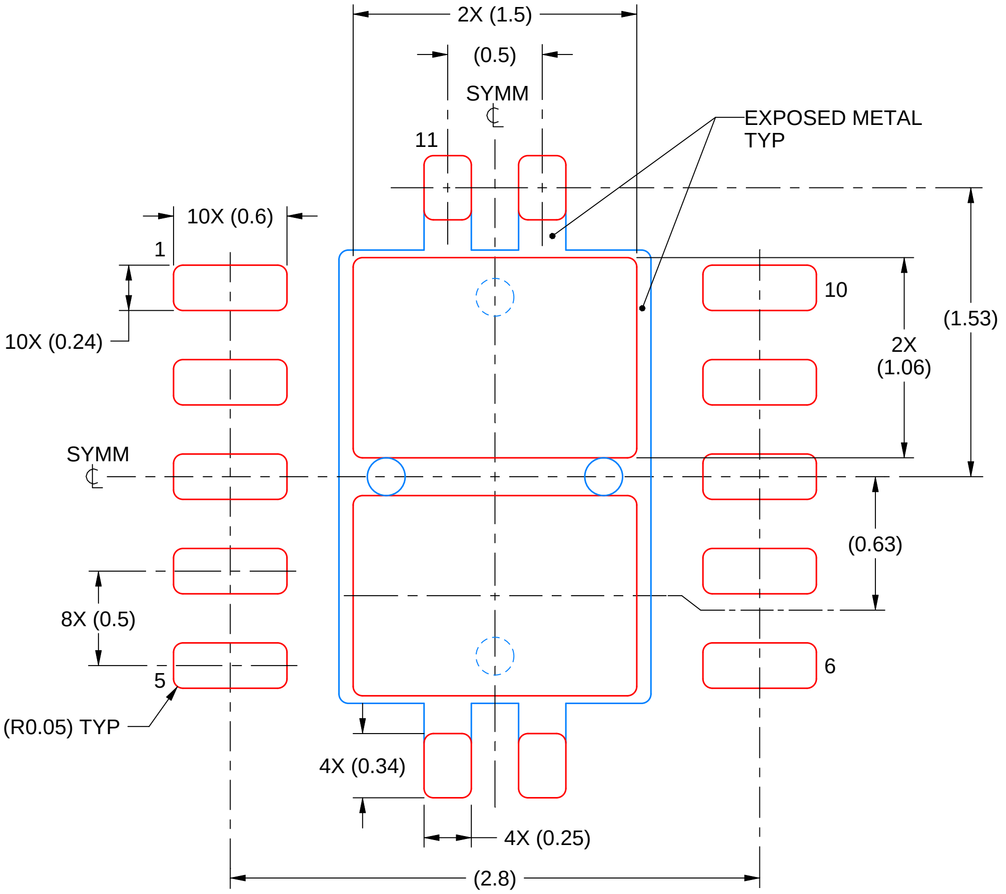
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.