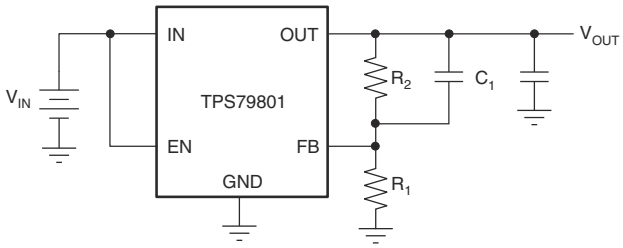
# TPS798-Q1 車載用、50mA、3V～50V、マイクロパワー、低ドロップアウト リニア レギュレータ

## 1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - 温度グレード 1:-40℃～+125℃、$T_A$
- 幅広い入力電圧範囲:3V～50V
- 低い静止電流:40µA (標準値)
- Low ドロップアウト電圧:300mV (標準値)
- 出力電流:50mA
- 入力保護ダイオード不要
- 調整可能な出力:1.275V～28V
- シャットダウン時の静止電流:1µA
- 1µF 出力コンデンサで安定
- アルミニウム、タンタル、セラミックのコンデンサで安定動作
- 逆極性入力バッテリ保護
- 逆出力電流フロー保護
- 熱制限
- 8 ピン HVSSOP PowerPAD デバイス パッケージで供給されます。

## 2 アプリケーション

- 小電流、高電圧レギュレータ
- バッテリ駆動システム用レギュレータ
- テレコム
- 自動車




$V_{OUT} = 1.275\ V\ (1 + R_2 / R_1) + I_{FB}R_2$
$V_{FB} = 1.275\ V$
$I_{FB} = 0.2\ \mu A$ at 25°C
Output Range = 1.275 V to 28 V

**代表的なアプリケーション**

## 3 概要

TPS798-Q1 は、50V 高電圧マイクロパワー、低ドロップアウト (LDO) のリニア レギュレータ シリーズに属する最初のデバイスです。このデバイスは、わずか 300mV のドロップアウト電圧で 50mA の出力電流を供給することができます。低静止電流、高電圧 (50V) アプリケーション向けに設計された TPS798-Q1 は、40µA で動作し、シャットダウン時の静止電流は 1µA なので、バッテリー駆動または高電圧システムに最適です。ドロップアウト時の静止電流もよく制御されます。

TPS798-Q1 のその他の特長として、等価直列抵抗 (ESR) が小さいセラミック出力コンデンサで動作できることが挙げられます。このデバイスは、出力に 1µF を接続するだけで安定動作します。一方、従来のほとんどのデバイスでは、安定させるために 10µF～100µF のタンタル コンデンサが必要です。他のレギュレータのように ESR を追加しなくても、小さなセラミック コンデンサを使用できます。内部保護回路として逆入力バッテリ保護、逆出力電流保護、電流制限、過熱制限機能を備えており、各種フォルト条件でデバイスを保護できます。

このデバイスは、5V 固定出力電圧品 (TPS79850) と、1.275V リファレンス電圧を使った可変出力電圧品 (TPS79801) として提供しています。TPS798-Q1 レギュレータは、放熱性能を高めるための露出パッドを備えた 8 ピン HVSSOP PowerPAD (DGN) パッケージで供給されます。

**パッケージ情報**

| 部品番号 | パッケージ (1) | パッケージ サイズ(2) |
|---|---|---|
| TPS798-Q1 | DGN (HVSSOP、8) | 3mm × 4.9mm |

(1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

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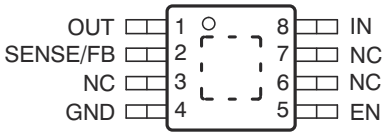
## 4 Pin Configuration and Functions




The exposed thermal pad is connected to ground through pin 4 (GND).

**図 4-1. DGN Package, 8-Pin HVSSOP With PowerPAD™ (Top View)**

**表 4-1. Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| EN | 5 | I | Enable pin. Driving the EN pin high turns on the regulator over full operating range. Driving this pin low puts the regulator into shutdown mode over full operating range. |
| GND | 4 | O | Ground. The exposed thermal pad is connected to ground through this pin. |
| IN | 8 | I | Input pin. Place a 0.1µF ceramic or greater capacitor from this pin to ground to provide stability. Both input and output capacitor grounds must be tied back to the device ground with no significant impedance between them. |
| NC | 3, 6, 7 | — | No internal connection |
| OUT | 1 | O | Regulated output voltage pin. A small (1µF) capacitor is needed from this pin to ground to provide stability. |
| SENSE/FB | 2 | I | This pin is the input to the control loop error amplifier. Use this pin to set the output voltage of the device. |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage range | IN(2) | –65 | 60 | V |
| | | OUT | –0.3 | 28 | |
| | | FB | –0.3 | 7 | |
| | | EN(2) | –65 | 60 | |
| | | Enable to IN differential | 0.6 | $V_{IN}$ | |
| $T_J$ | Junction temperature range(3) | | –40 | 125 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Transient: 500ms for $V_{IN}$ > 50V.
(3) The junction temperature must not exceed 125°C. See 図 5-13 to determine the maximum ambient operating temperature versus the supply voltage and load current. The safe operating area curves assume a 50°C/W thermal impedance and may need to be adjusted to match actual system thermal performance.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002(1) | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | ±1000 | |

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 5.3 Recommended Operating Conditions

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage | IN | –65 | 50 | V |
| | | OUT | –0.3 | 28 | |
| | | FB | –0.3 | 7 | |
| | | EN | –65 | 50 | |
| $I_{OUT}$ | Output current | | | 50 | mA |
| $T_J$ | Operating junction temperature(1) (2) (3) | | –40 | 125 | °C |
| $T_A$ | Ambient free-air temperature | | –40 | 105 | °C |

(1) Operating conditions are limited by maximum junction temperature. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current, the input voltage range must be limited.
(2) The TPS798-Q1 is specified to meet performance specifications from –40°C to 125°C operating junction temperature. Specifications over the full operating junction temperature range are specified by design, characterization, and correlation with statistical process controls.
(3) This device includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature exceeds 125°C (minimum) when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

## 5.4 Thermal Information

| THERMAL METRIC[1] | | TPS798-Q1 DGN (HVSSOP) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance (JEDEC 51-5[2]) | 57.1 | °C/W |
| | Junction-to-ambient thermal resistance (JEDEC 51-7[3]) | 130 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 50.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 30.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 30.3 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 6.5 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) The thermal data is based on using JEDEC 51-5. The copper pad is soldered to the thermal land pattern and using 5 by 8 thermal array (vias). Correct attachment procedure must be incorporated.
(3) The thermal data is based on using JEDEC 51-7. The copper pad is soldered to the thermal land. No thermal vias. Correct attachment procedure must be incorporated.

## 5.5 Electrical Characteristics

$V_{IN}$ = $V_{OUT(NOM)}$ + 1V or 4V (whichever is greater for either fixed or adjustable versions), $I_{LOAD}$ = 1mA, $V_{EN}$ = 3V, and $C_{OUT}$ = $C_{IN}$ = 2.2µF (unless otherwise noted); for the TPS79801, the FB pin is tied to $V_{OUT}$; typical values are at $T_J$ = 25°C

| PARAMETER | | TEST CONDITIONS | | $T_J$ [1] | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Minimum input voltage | $I_{LOAD}$ = 50mA | | Full range | | 3 | 4 | V |
| Fixed $V_{OUT}$ | Initial output voltage accuracy | $V_{IN}$ = $V_{OUT}$ nom + 0.5V | | 25°C | –1.5% | | 1.5% | |
| | Output voltage accuracy over line, load, and full temperature range | $V_{IN}$ = $V_{OUT}$ nom + 1V to 50V, $I_{LOAD}$ = 1mA to 50mA | | Full range | –3% | | 3% | |
| Adjustable $V_{OUT}$ | Initial output voltage accuracy | $V_{IN}$ = 3V | | 25°C | 1.256 | 1.275 | 1.294 | V |
| | Output voltage accuracy over line, load, and full temperature range | $V_{IN}$ = 4V to 50V, $I_{LOAD}$ = 1mA to 50mA | | Full range | 1.237 | 1.275 | 1.313 | V |
| $\Delta V_{OUT}/\Delta V_{IN}$ | Line regulation, adjustable $V_{OUT}$ | $\Delta V_{IN}$ = 3V to 50V | | Full range | | | 13 | mV |
| | Line regulation, TPS79850 | $V_{IN}$ = $V_{OUT}$ nom + 0.5V to 50V | | | | | 15 | mV |
| $\Delta V_{OUT}/\Delta I_{OUT}$ | Load regulation, adjustable $V_{OUT}$ | $\Delta I_{LOAD}$ = 1mA to 50mA | | 25°C | | | 20 | mV |
| | | | | Full range | | | 32 | |
| | Load regulation, fixed $V_{OUT}$ | $\Delta I_{LOAD}$ = 1mA to 50mA | | 25°C | | | 50 | mV |
| | | | | Full range | | | 90 | |
| Adjustable $V_{OUT}$ | Output voltage range[2] [3] | | | Full range | 1.275 | | 28 | V |
| $V_{DO}$ | Dropout voltage[4] [5] | $V_{IN}$ = $V_{OUT(NOM)}$ – 0.1V | | 25°C | | 85 | 150 | mV |
| | | | | Full range | | | 190 | |
| | | $I_{LOAD}$ = 10mA, $V_{IN}$ = $V_{OUT(NOM)}$ – 0.1V | | 25°C | | 170 | 260 | |
| | | | | Full range | | | 350 | |
| | | $I_{LOAD}$ = 50mA, $V_{IN}$ = $V_{OUT(NOM)}$ – 0.1V | | 25°C | | 300 | 370 | |
| | | | | Full range | | | 550 | |
| $I_{GND}$ | GND pin current[6] | $V_{IN}$ = $V_{OUT(NOM)}$ | $I_{LOAD}$ = 0mA | Full range | | 30 | 80 | µA |
| | | | $I_{LOAD}$ = 1mA | Full range | | 100 | 180 | |
| | | | $I_{LOAD}$ = 10mA | Full range | | 400 | 700 | |
| | | | $I_{LOAD}$ = 50mA | Full range | | 1.8 | 3.3 | mA |
| $V_N$ | Output voltage noise | $C_{OUT}$ = 10µF, $I_{LOAD}$ = 50mA, BW = 10Hz to 100kHz, $V_{IN}$ = 4.3V, $V_{OUT}$ = 3.3V (adjustable used) | | 25°C | | 100 | | $\mu V_{RMS}$ |
| $I_{FB}$ | FB pin bias current[7] | $V_{IN}$ = 3V | | 25°C | | 0.05 | 0.2 | µA |

## 5.5 Electrical Characteristics (続き)

$V_{IN}$ = $V_{OUT(NOM)}$ + 1V or 4V (whichever is greater for either fixed or adjustable versions), $I_{LOAD}$ = 1mA, $V_{EN}$ = 3V, and $C_{OUT}$ = $C_{IN}$ = 2.2µF (unless otherwise noted); for the TPS79801, the FB pin is tied to $V_{OUT}$; typical values are at $T_J$ = 25°C

| PARAMETER | | TEST CONDITIONS | $T_J$ (1) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{EN}$ | EN pin high (enabled)(8) | OFF to ON, $V_{IN}$ = 6V | Full range | | | 1.5 | V |
| | EN pin low (shutdown)(8) | ON to OFF, $V_{IN}$ = 6V | 25°C | 0.4 V | | | V |
| | EN pin low (shutdown)(8) | ON to OFF, $V_{IN}$ = 6V | Full range | 0.2 V | | | V |
| $I_{EN}$ | EN pin current(8) | $V_{EN}$ = 0V $V_{IN}$ = 6V, $I_{LOAD}$ = 0mA | Full range | | 0.4 | 2 | µA |
| | | $V_{EN}$ = 3V, $V_{IN}$ = 6V, $I_{LOAD}$ = 0mA | Full range | | 0.4 | 0.5 | |
| $I_{shutdown}$ | GND pin current(6) | $V_{IN}$ = 6V, $V_{EN}$ = 0V, $I_{LOAD}$ = 0mA | Full range | | 3 | 25 | µA |
| PSRR | Power-supply rejection ratio | $V_{IN}$ = 4.3V, $V_{OUT}$ 3.3V $V_{RIPPLE}$ = 0.5$V_{PP}$, $f_{RIPPLE}$ = 120Hz, $I_{LOAD}$ = 50mA | 25°C | | 65 | | dB |
| $I_{LIMIT}$ | Fixed current limit(9) | $\Delta V_{OUT}$ = $V_{OUT(NOM)}$ – 0.1V | Full range | 60 | | 200 | mA |
| | Adjustable current limit | $\Delta V_{OUT}$ = $V_{OUT(NOM)}$ – 0.1V | Full range | 60 | | 200 | mA |
| $I_{RL}$ | Input reverse leakage current(reverse battery test) | $V_{IN}$ = –60V, $V_{OUT}$ = open, $C_{IN}$ open | Full range | | | 6 | mA |
| $I_{RO}$ | Reverse output current(10) | $V_{OUT}$ = $V_{OUT(NOM)}$, $V_{IN}$ = ground | 25°C | | 19 | 25 | µA |
| $T_{SD}$ | Thermal shutdown temperature ($T_J$) (11) | Shutdown, temperature increasing | | 135 | | | °C |
| | | Reset, temperature decreasing | | 135 | | | |

(1) Full range $T_J$ = –40°C to 125°C.
(2) This parameter is tested and specified under pulse load conditions such that $T_J$ = $T_A$. This device is 100% production tested at $T_A$ = 25°C. Performance at full range is specified by design, characterization, bench to ATE correlation testing, and other statistical process controls.
(3) This device is limited by a maximum junction temperature of $T_J$ = 125°C. The regulated output voltage specification cannot be applied to all combinations of various $V_{IN}$, $V_{OUT}$, ambient temperature, and $I_{OUT}$ conditions. When operating with large voltage differentials across the device, the output load must be limited so as not to violate the maximum junction temperature for a given ambient temperature.
(4) In the adjustable version test, the output uses an external voltage divider. This resistor voltage divider is made up of $R_1$ = 215kΩ and R2 (bottom resistor) = 340kΩ. This configuration preloads the output with 6µA.
(5) By definition, dropout voltage is the minimum input voltage needed to maintain a given output voltage at a specific load current. For dropout testing, minimum $V_{IN}$ = $V_{OUT(NOM)}$ × 0.96. This specification ensures that the device is in dropout and takes into account the output voltage tolerance over the full temperature range.
(6) Ground pin current is tested with $V_{IN}$ = $V_{OUT(NOM)}$ or 3V, whichever is greater.
(7) FB pin current flows into the FB pin.
(8) EN pin current flows into the EN pin.
(9) Current limit is tested with $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5V or 3V, whichever is greater. $V_{OUT}$ is forced to $V_{OUT(NOM)}$ – 0.1V and the output current is measured.
(10) Reverse output current is tested with the IN pin tied to ground and the output forced to $V_{OUT(NOM)}$ +0.1V. This current flows into the OUT pin and out of the GND pin and then measured.
(11) Specified by design.

## 5.6 Dissipation Ratings

see (1)

| BOARD | PACKAGE | DERATING FACTOR ABOVE $T_A$ = 25°C | $T_A \le$ 25°C POWER RATING | $T_A$ = 70°C POWER RATING | $T_A$ = 85°C POWER RATING |
|---|---|---|---|---|---|
| High-K(2) | DGN | 16.6mW/°C | 1.83W | 1.08W | 0.833W |

(1) See the *Thermal Considerations* for more information related to thermal design.
(2) The JEDEC High-K (1s) board design used to derive this data was a 4.5 inch × 3 inch, 2-layer board with 2 ounce copper traces on top of the board.

## 5.7 Typical Characteristics

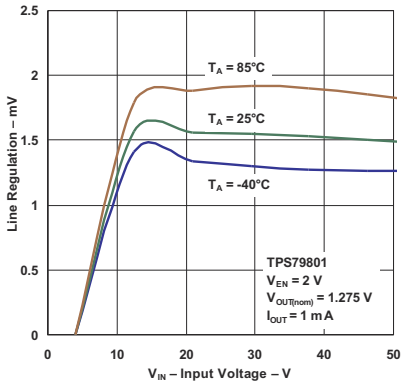



**図 5-1. Line Regulation vs Input Voltage**

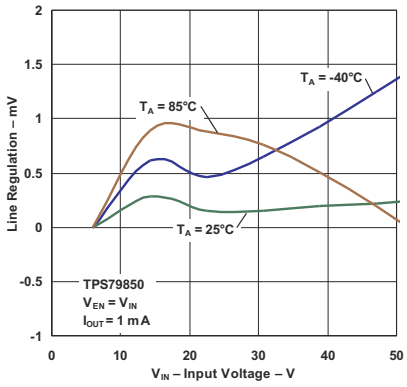



**図 5-2. Line Regulation vs Input Voltage**

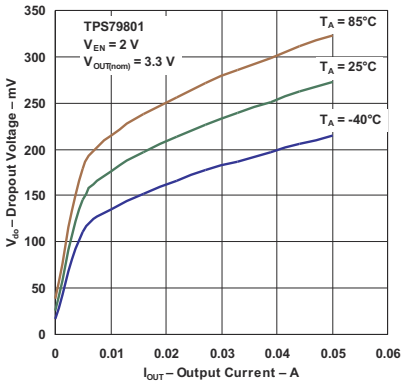



**図 5-3. Dropout Voltage vs Output Current**

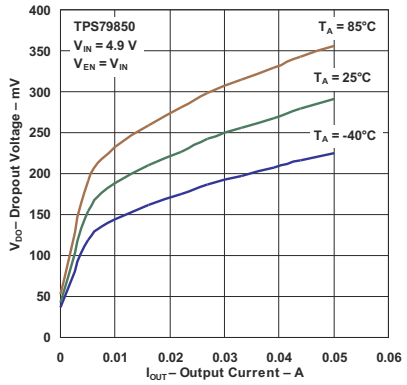



**図 5-4. Dropout Voltage vs Output Current**

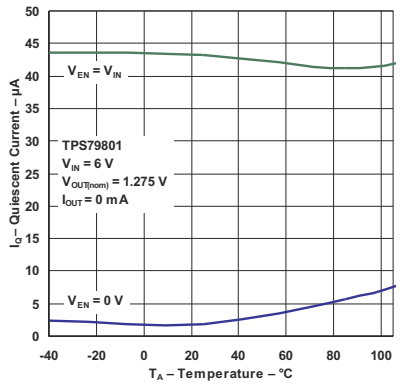



**図 5-5. Quiescent Current vs Temperature**

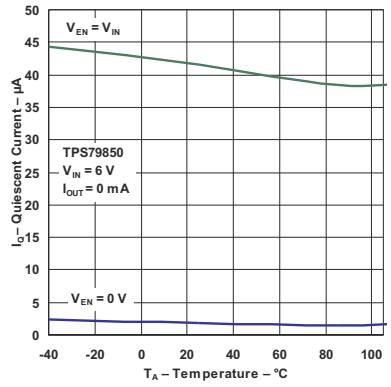



**図 5-6. Quiescent Current vs Temperature**

## 5.7 Typical Characteristics (continued)

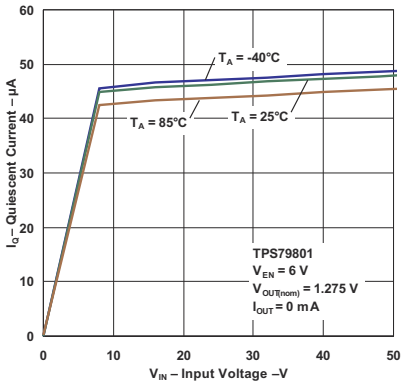



図 5-7. Quiescent Current vs Input Voltage

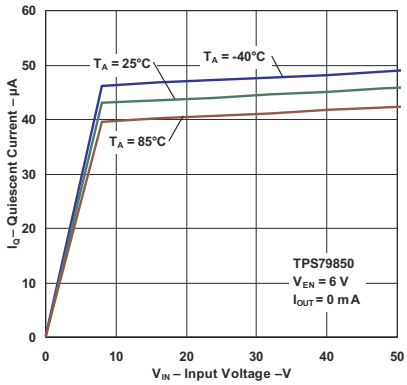



図 5-8. Quiescent Current vs Input Voltage

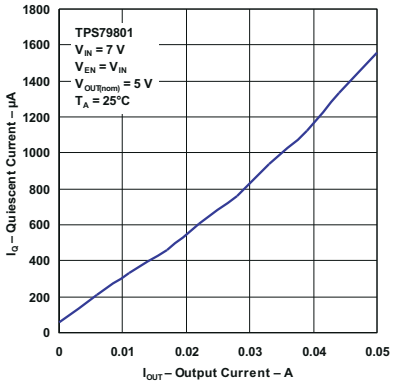



図 5-9. Quiescent Current vs Output Current

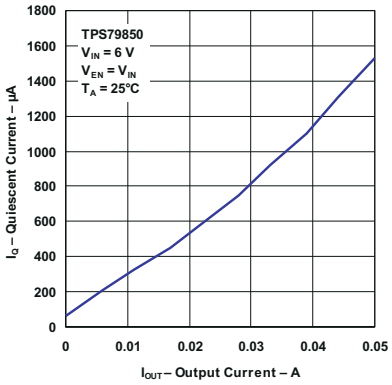



図 5-10. Quiescent Current vs Output Current

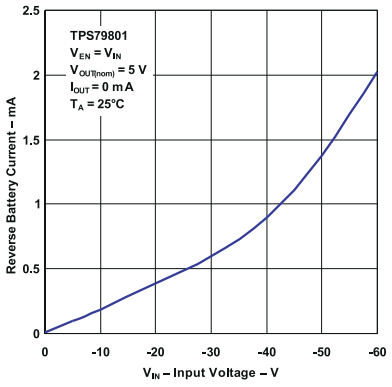



図 5-11. Reverse Battery Leakage vs Input Voltage

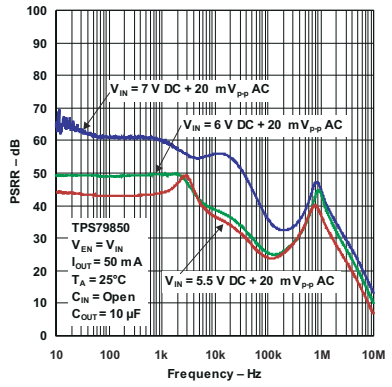



図 5-12. Power Supply Ripple Rejection vs Frequency

## 5.7 Typical Characteristics (continued)

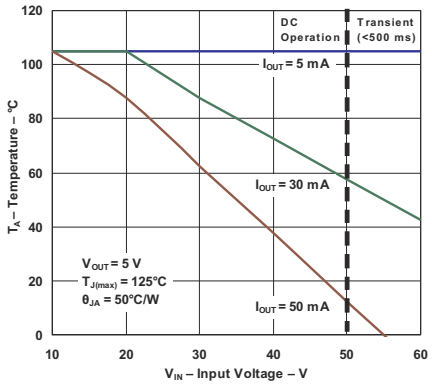


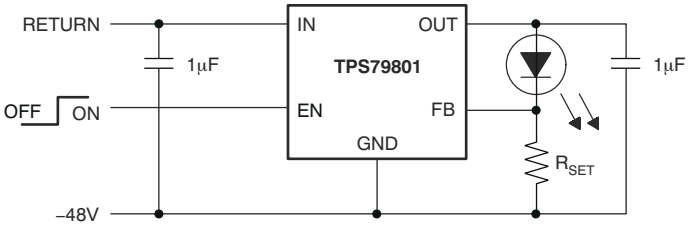

**図 5-13. Safe Operating Area**

# 6 Detailed Description

## 6.1 Overview

The TPS798-Q1 is a 50mA high-voltage LDO regulator with micropower quiescent current and shutdown. The device is capable of supplying 50mA at a dropout voltage of 300mV (typical). The low operating quiescent current (40µA) drops to 1µA in shutdown. In addition to the low quiescent current, the TPS798-Q1 incorporates several protection features that make it ideal for battery-powered applications.

The device is protected against both reverse-input and reverse-output voltages. In battery-backup applications, where the output can be held up by a backup battery when the input is pulled to ground, the TPS798-Q1 acts as if a diode is in series with the device output and prevents reverse current flow. 図 6-1 and 図 6-2 illustrate two typical applications.




$I_{LED}$ = 1.275V / $R_{SET}$ –48V can vary from –4V to –50V.

**図 6-1. Constant Brightness for Indicator LED Over Wide Input Voltage Range**

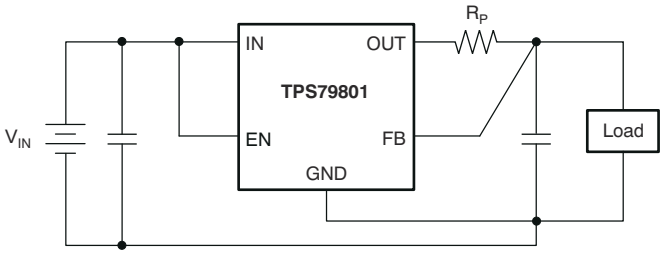



**図 6-2. Kelvin Sense Connection**

## 6.2 Functional Block Diagrams

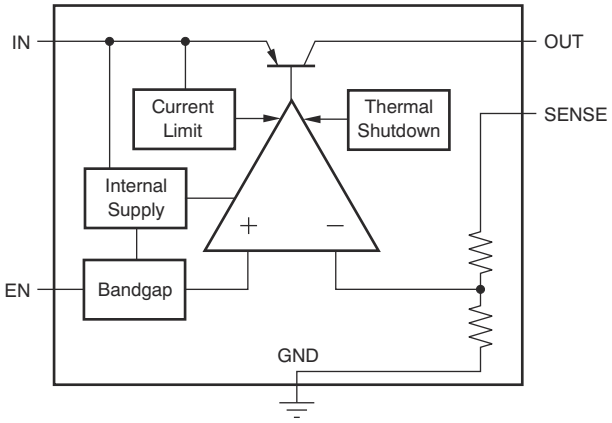



**図 6-3. Fixed Voltage Output Version**

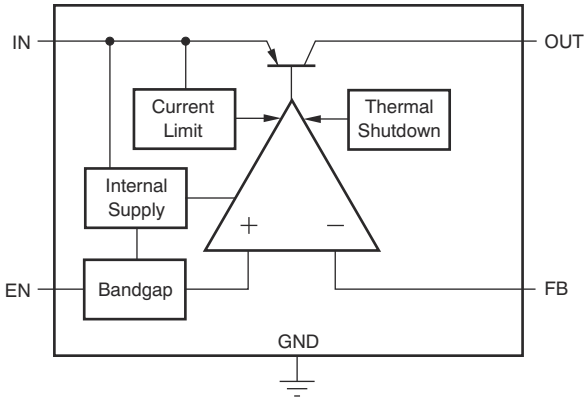
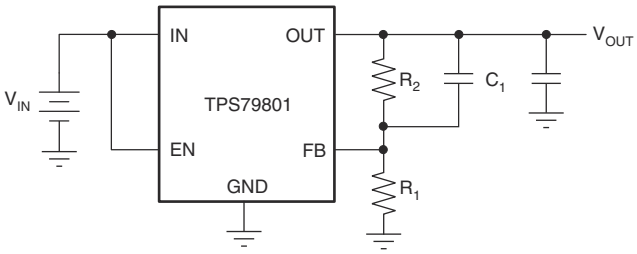



**図 6-4. Adjustable Voltage Output Version**

## 6.3 Feature Description

### *6.3.1 Adjustable Operation*

The TPS798-Q1 has an output voltage range of 1.275V to 28V. The output voltage is set by the ratio of two external resistors as shown in 図 6-5. The feedback loop monitors the output to maintain the voltage at the adjust pin at 1.275V referenced to ground. The current in $R_1$ is then equal to 1.275V / $R_1$, and the current in $R_2$ is the current in $R_1$ plus the FB pin bias current. The FB pin bias current, 0.2µA at 25°C, flows through $R_2$ into the FB pin. The output voltage can be calculated using the formula in 図 6-5. The value of $R_1$ must be less than 250kΩ to minimize errors in the output voltage caused by the FB pin bias current. When in shutdown, the output is turned off and the divider current is zero.




$V_{OUT}$ = 1.275 V (1 + $R_2$ / $R_1$) + $I_{FB}R_2$
$V_{FB}$ = 1.275 V
$I_{FB}$ = 0.2 µA at 25°C
Output Range = 1.275 V to 28 V

**図 6-5. Adjustable Operation**

A 100pF capacitor ($C_1$) placed in parallel with the top resistor ($R_2$) of the output divider is necessary for stability and transient performance of the adjustable TPS798-Q1. The impedance of $C_1$ at 10kHz must be less than the value of $R_2$.

The adjustable device is tested and specified with the FB pin tied to the OUT pin and a 1mA DC load (unless otherwise specified) for an output voltage of 1.275V. Specifications for output voltages greater than 1.275V are proportional to the ratio of the desired output voltage to 1.275V ($V_{OUT}$ / 1.275V). For example, load regulation for an output current change of 1mA to 50mA is –10mV (typical) at $V_{OUT}$ = 1.275V.

At $V_{OUT}$ = 12V, load regulation is:

(12V / 1.275V) × (–10mV) = –94mV (1)

### 6.3.2 Output Capacitance and Transient Response

The TPS798-Q1 is designed to be stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. To prevent oscillations, use a minimum output capacitor of 1µF with an ESR of 3Ω or less. The TPS798-Q1 is a micropower device, and output transient response is a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the TPS798-Q1, increase the effective output capacitor value.

Extra consideration must be given to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. The most common dielectrics used are Z5U, Y5V, X5R, and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but exhibit strong voltage and temperature coefficients. When used with a 5V regulator, a 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across the terminals because of mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients.

### 6.3.3 Calculating Junction Temperature

Given an output voltage of 5V, an input voltage range of 15V to 24V, an output current range of 0mA to 50mA, and a maximum ambient temperature of 50°C, the maximum junction temperature is calculated as follows.

The power dissipated ($P_{DISS}$) by the DGN package is equal to:

$$I_{OUT(MAX)}(V_{IN(MAX)} - V_{OUT}) + I_{GND}(V_{IN(MAX)}) \quad (2)$$

where:

- $I_{OUT(MAX)}$ = 50mA
- $V_{IN(MAX)}$ = 24V
- $V_{OUT}$ = 5V
- $I_{GND}$ at ($I_{OUT}$ = 50mA, $V_{IN}$ = 24V) = 1mA

Therefore,

$$P_{DISS} = 50mA\ (24V - 5V) + 1mA\ (24V) = 0.974W \quad (3)$$

The thermal resistance is approximately 60°C/W, based on JEDEC 51-5 profile. Therefore, the junction temperature rise above ambient is approximately equal to:

$$0.974W \times 60°C/W = 58.44°C \quad (4)$$

The maximum junction temperature is then equal to the maximum junction temperature rise above ambient plus the maximum ambient temperature or:

$$T_J\ max = 50°C + 58.44°C = 108.44°C \quad (5)$$

### 6.3.4 Protection Features

The TPS798-Q1 incorporates several protection features that make the device designed for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the device is protected against reverse-input voltages, and reverse currents from output to input.

Current limit protection and thermal-overload protection are intended to protect the device against current overload conditions at the output of the device. The junction temperature must not exceed 125°C.

The input of the device withstands reverse voltages of –60V. Current flow into the device is limited to less than 6mA (typically, less than 100µA), and no negative voltage appears at the output. The TPS798-Q1 protects both the device and the load. This architecture also provides protection against batteries that can be plugged in backwards.

The FB pin of the adjustable device can be pulled above or below ground by as much as 7V without damaging the device. If the input is left open or grounded, the FB pin behaves as an open circuit when pulled below ground, or as a large resistor (typically, 100kΩ) in series with a diode when pulled above ground. If the input is powered by a voltage source, pulling the FB pin below the reference voltage increases the output voltage. This configuration causes the output to go to a unregulated high voltage. Pulling the FB pin above the reference voltage turns off all output current.

In situations where the FB pin is connected to a resistor divider that pulls the FB pin above the 7V clamp voltage if the output is pulled high, the FB pin input current must be limited to less than 5mA. For example, a resistor divider provides a regulated 1.5V output from the 1.275V reference when the output is forced to 28V. The top resistor of the resistor divider must be chosen to limit the current into the FB pin to less than 5mA when the FB pin is at 7V. The 21V difference between the OUT and FB pins divided by the 5mA maximum current into the FB pin yields a minimum top resistor value of 5.8kΩ.

In circuits where a backup battery is required, several different input and output conditions can occur. The output voltage can be held up while the input is either pulled to ground, pulled to some intermediate voltage, or is left open. The rise in reverse output current above 7V occurs from the breakdown of the 7V clamp on the FB pin. With a resistor divider on the regulator output, this current is reduced, depending on the size of the resistor divider.

When the IN pin of the TPS798-Q1 is forced below the OUT pin, or the OUT pin is pulled above the IN pin, input current typically drops to less than 0.6mA. This scenario can occur if the input of the TPS798-Q1 is connected to a discharged (low voltage) battery and the output is held up by either a backup battery or a second regulator circuit. The state of the EN pin has no effect on the reverse output current when the output is pulled above the input.

## 6.4 Device Functional Modes

### 6.4.1 Low-Voltage Tracking

At low input voltages, the regulator drops out of regulation and the output voltage tracks input minus a voltage based on the load current and switch resistance. This allows for a smaller input capacitor and can possibly eliminate the need of using a boost convertor during cold-crank conditions.

# 7 Application and Implementation

注

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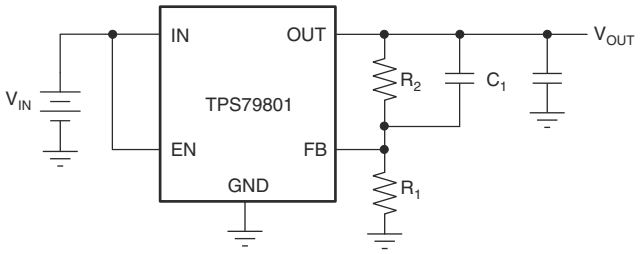
## 7.1 Application Information

図 7-1 shows typical application circuits for the TPS79801-Q1 device. Based on the end-application, different values of external components can be used.

## 7.2 Typical Application




$V_{OUT} = 1.275\ V\ (1 + R_2 / R_1) + I_{FB}R_2$
$V_{FB} = 1.275\ V$
$I_{FB} = 0.2\ \mu A$ at 25°C
Output Range = 1.275 V to 28 V

**図 7-1. Adjustable Operation Example**

### 7.2.1 Design Requirements

表 7-1 lists the design parameters for this example.

**表 7-1. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Input voltage range | 3V to 50V |
| Output voltage | 5V |
| Output current rating | 50mA |
| Output capacitor range | 1µF to 100µF |

### 7.2.2 Detailed Design Procedure

To begin the design process, determine the following:

1. Input voltage range
2. Output voltage
3. Output current rating
4. Output capacitor

### 7.2.3 Application Curves

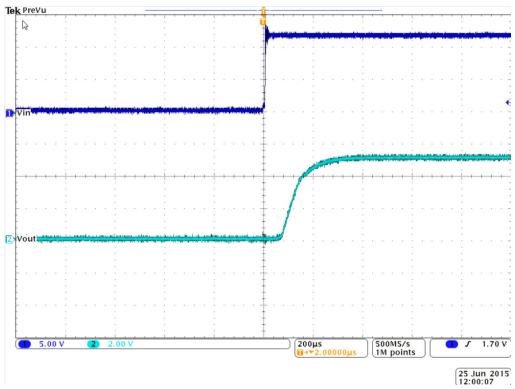



図 7-2. CH1: Vin, CH2: Vout Power-Up Waveform (Load = 50mA)

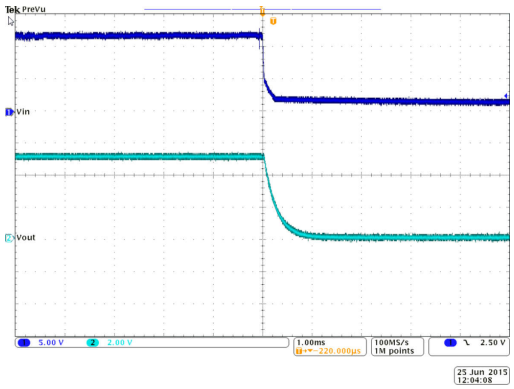



図 7-3. CH1: Vin, CH2: Vout Power-Down Waveform (Load = 50mA)

## 7.3 Power Supply Recommendations

### 7.3.1 Thermal Considerations

The power handling capability of the device is limited by the maximum rated junction temperature (125°C). The power dissipated by the device consists of two components:

- Output current multiplied by the input/output voltage differential: $I_{OUT} \times (V_{IN} – V_{OUT})$
- GND pin current multiplied by the input voltage: $I_{GND} \times V_{IN}$

The GND pin current can be found by examining the GND pin current curves in the *Typical Characteristics*. Power dissipation is equal to the sum of the two components listed previously.

The TPS798-Q1 series regulators have internal thermal limiting designed to protect the device during overload conditions. Do not exceed the maximum junction temperature rating of 125°C. All sources of thermal resistance from junction to ambient must be carefully considered. Additional heat sources mounted nearby must also be considered.

For surface-mount devices, heat sinking is accomplished by using the heat-spreading capabilities of the printed-circuit-board (PCB) and its copper traces. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by power devices.

### 7.3.2 Thermal Layout Considerations

The amount of heat that an LDO linear regulator generates is directly proportional to the amount of power the device dissipates during operation. All integrated circuits have a maximum allowable junction temperature ($T_J$ max) above which normal operation is not assured. The operating environment must be designed so that the operating junction temperature ($T_J$) does not exceed the maximum junction temperature ($T_J$ max). The two primary environmental variables that can be used to improve thermal performance are air flow and external heat sinks. The purpose of this section is to help determine the proper operating environment for a linear regulator that operates at a specific power level.

In general, the maximum expected power ($P_D$ max) consumed by a linear regulator is computed as shown in 式 6:

$$P_D max = (V_{IN(avg)} – V_{OUT(avg)}) × I_{OUT(avg)} + V_{I(avg)} × I_Q \quad (6)$$

where:

- $V_{IN(avg)}$ is the average input voltage
- $V_{OUT(avg)}$ is the average output voltage
- $I_{OUT(avg)}$ is the average output current
- $I_Q$ is the quiescent current

For most TI LDO regulators, the quiescent current is insignificant compared to the average output current; therefore, the term $V_{IN(avg)} × I_Q$ can be ignored. The operating junction temperature is computed by adding the ambient temperature ($T_A$) and the increase in temperature as a result of the regulator power dissipation. The temperature rise is computed by multiplying the maximum expected power dissipation by the sum of the thermal resistances between the junction and the case ($R_{θJC}$), the case to heat sink ($R_{θCS}$), and the heat sink to ambient ($R_{θSA}$). Thermal resistances are measurements of how effectively an object dissipates heat. Typically, the larger the device, the more surface area available for power dissipation and the lower the device thermal resistance. 図 7-4 shows the relationship between power dissipation and temperature.

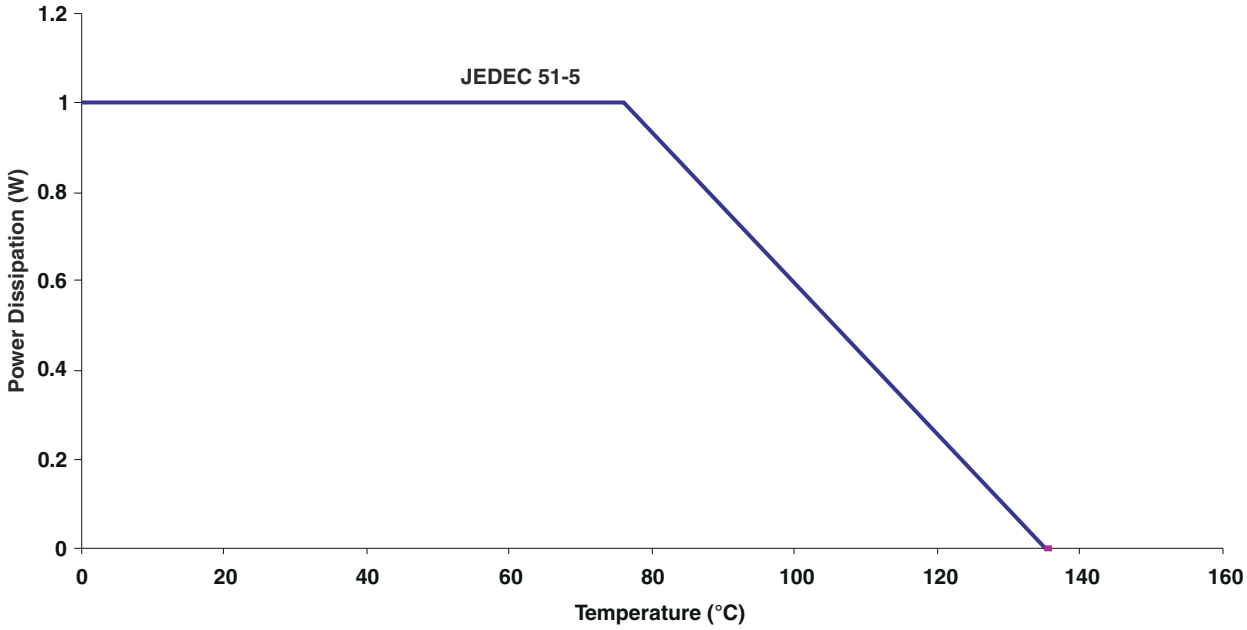


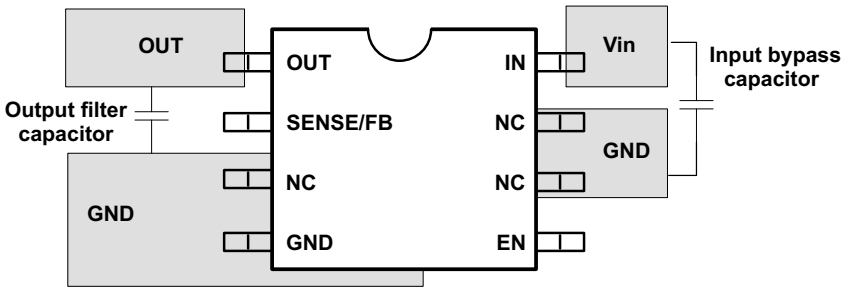

**図 7-4. Power Dissipation vs Temperature**

## 7.4 Layout

### 7.4.1 Layout Guidelines

- Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. TI strongly discourages using vias and long traces because of the negative impact on system performance. Vias and long traces can also cause instability.
- Equivalent series inductance (ESL) and ESR must be minimized to maximize performance and ensure stability. Every capacitor must be placed as close to the device as possible and on the same side of the PCB as the regulator.

### 7.4.2 Layout Example



# 8 Device and Documentation Support

## 8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

## 8.2 サポート・リソース

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## 8.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

# 9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision E (September 2015) to Revision F (April 2024) | Page |
|---|---|
| • ドキュメント全体を通してデバイス名を TPS798xx-Q1 から TPS798-Q1 に変更 | 1 |
| • ドキュメント全体で「MSOP」を「HVSSOP」に変更 | 1 |
| • 「特長」セクションに車載用の箇条書き項目を追加 | 1 |

| Changes from Revision D (August 2011) to Revision E (September 2015) | Page |
|---|---|
| • 「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 | 1 |

# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS79801QDGNRQ1 | ACTIVE | HVSSOP | DGN | 8 | 2500 | RoHS & Green | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | PMRQ | Samples |
| TPS79850QDGNRQ1 | ACTIVE | HVSSOP | DGN | 8 | 2500 | RoHS & Green | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | OOLQ | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

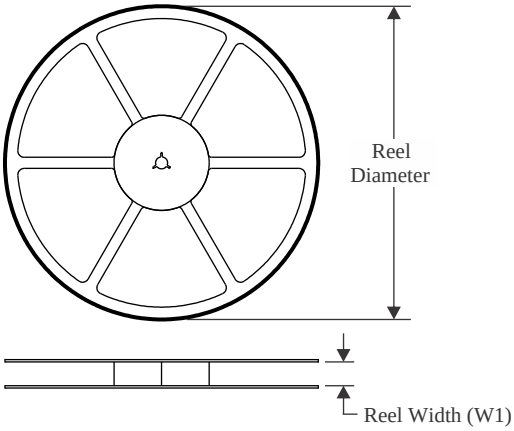
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

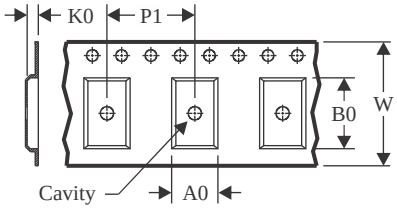
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

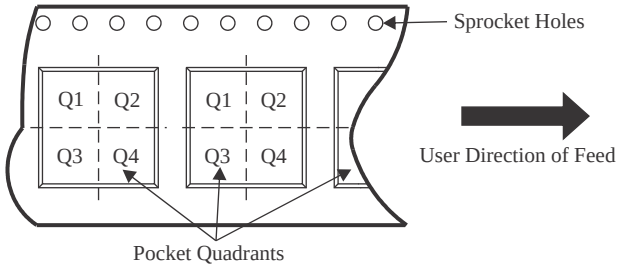



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

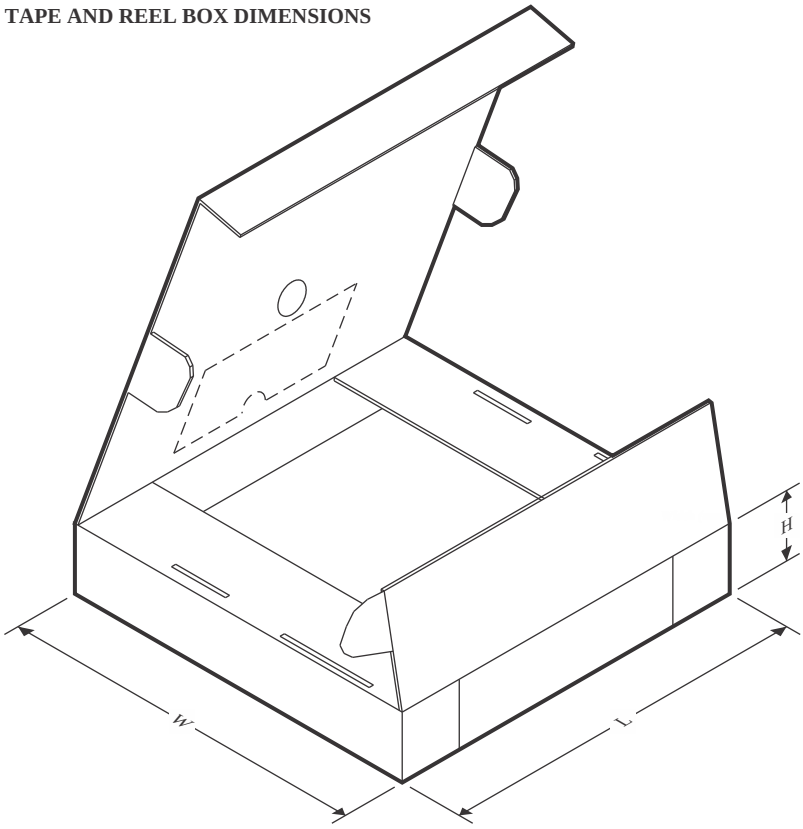
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS79801QDGNRQ1 | HVSSOP | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.3 | 1.3 | 8.0 | 12.0 | Q1 |
| TPS79850QDGNRQ1 | HVSSOP | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.3 | 1.3 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS79801QDGNRQ1 | HVSSOP | DGN | 8 | 2500 | 367.0 | 367.0 | 38.0 |
| TPS79850QDGNRQ1 | HVSSOP | DGN | 8 | 2500 | 367.0 | 367.0 | 38.0 |

# GENERIC PACKAGE VIEW

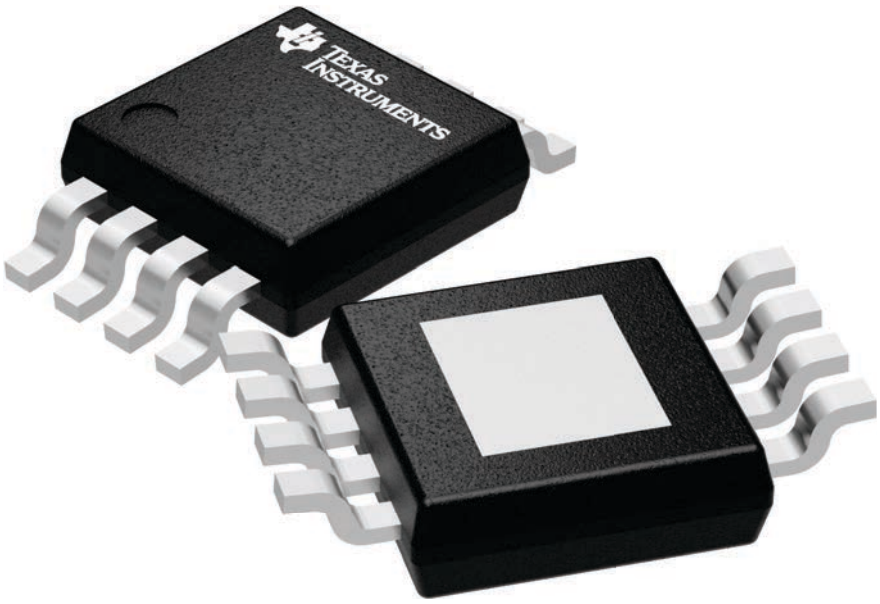
## DGN 8

## PowerPAD VSSOP - 1.1 mm max height

**3 x 3, 0.65 mm pitch**

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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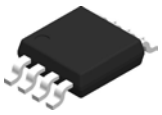
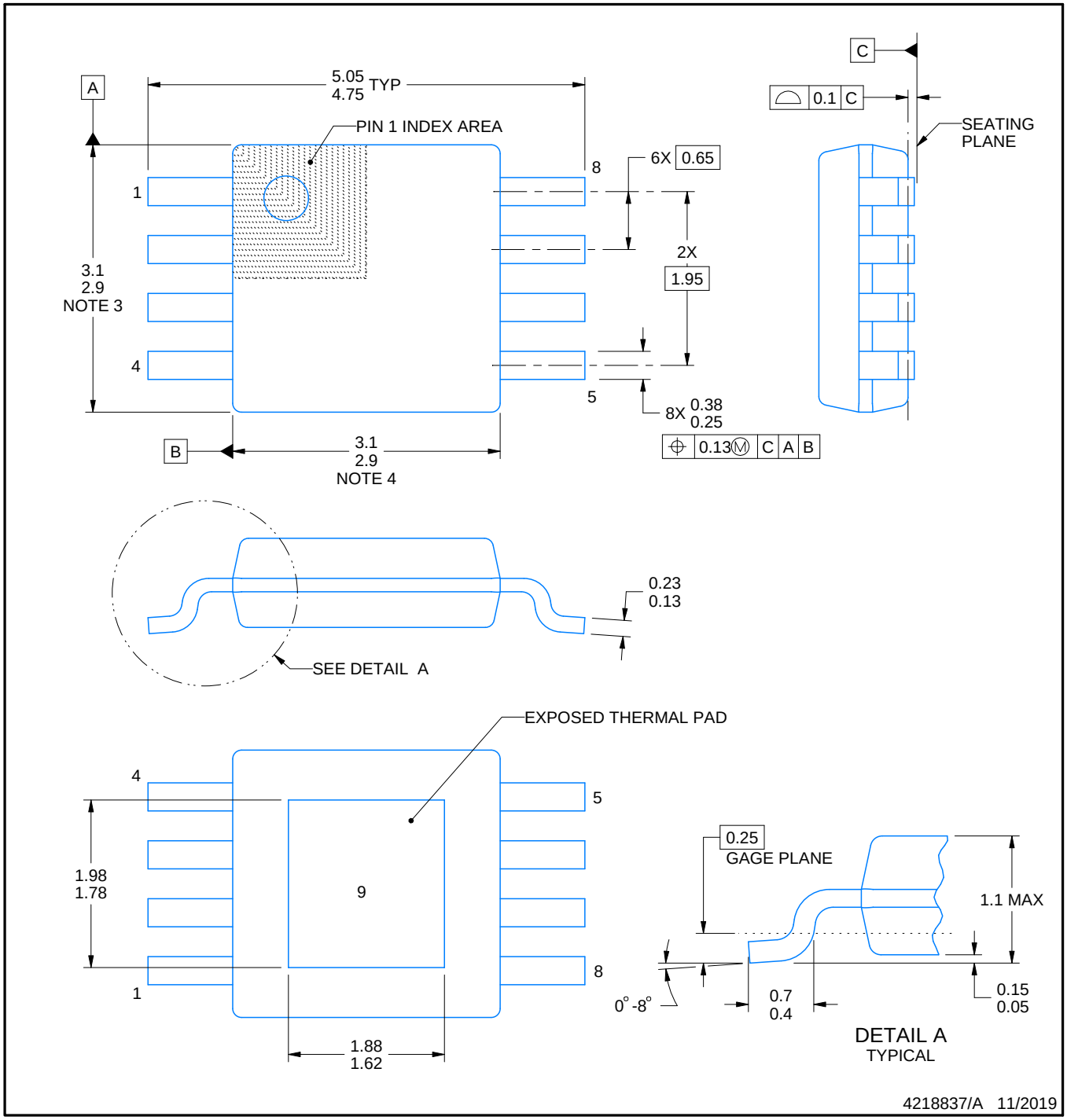
# PACKAGE OUTLINE

## DGN0008B



## PowerPAD™ VSSOP - 1.1 mm max height

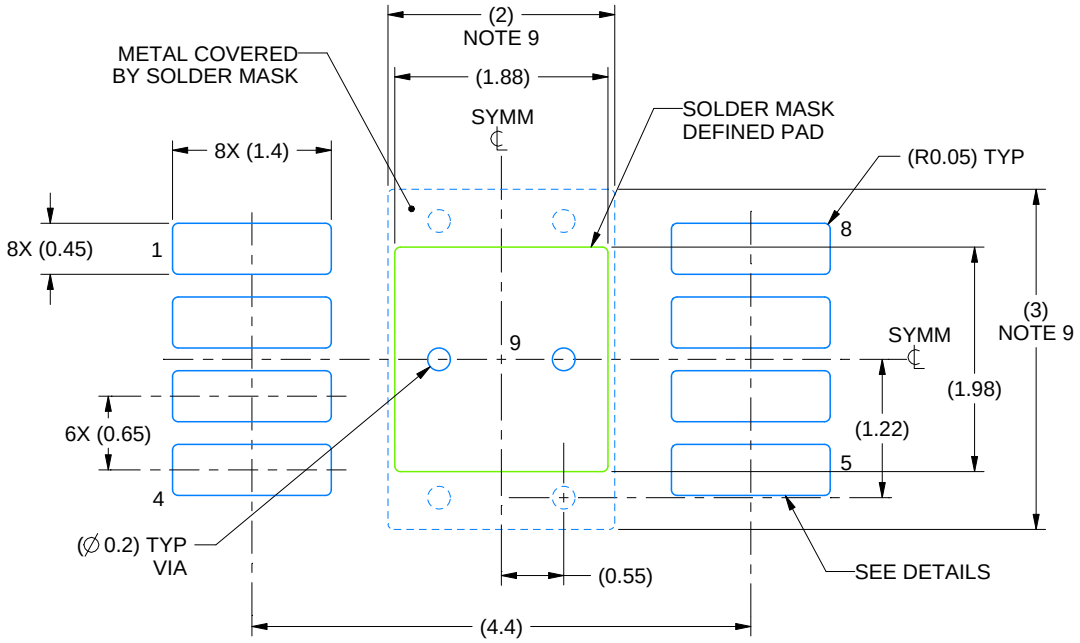
SMALL OUTLINE PACKAGE



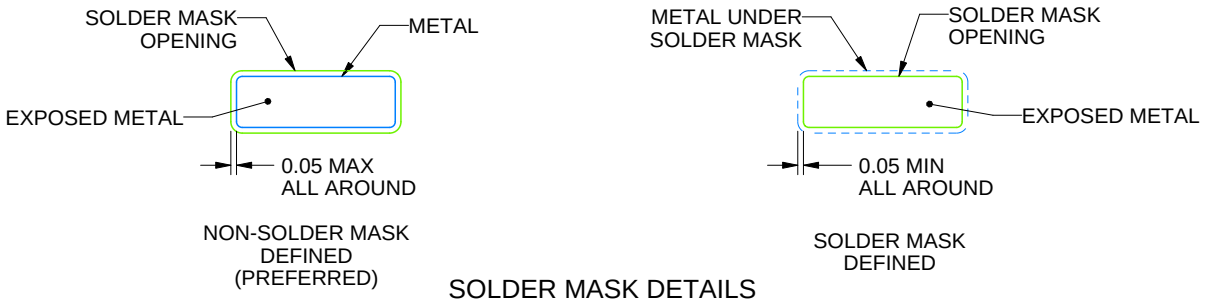

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X




SOLDER MASK DETAILS

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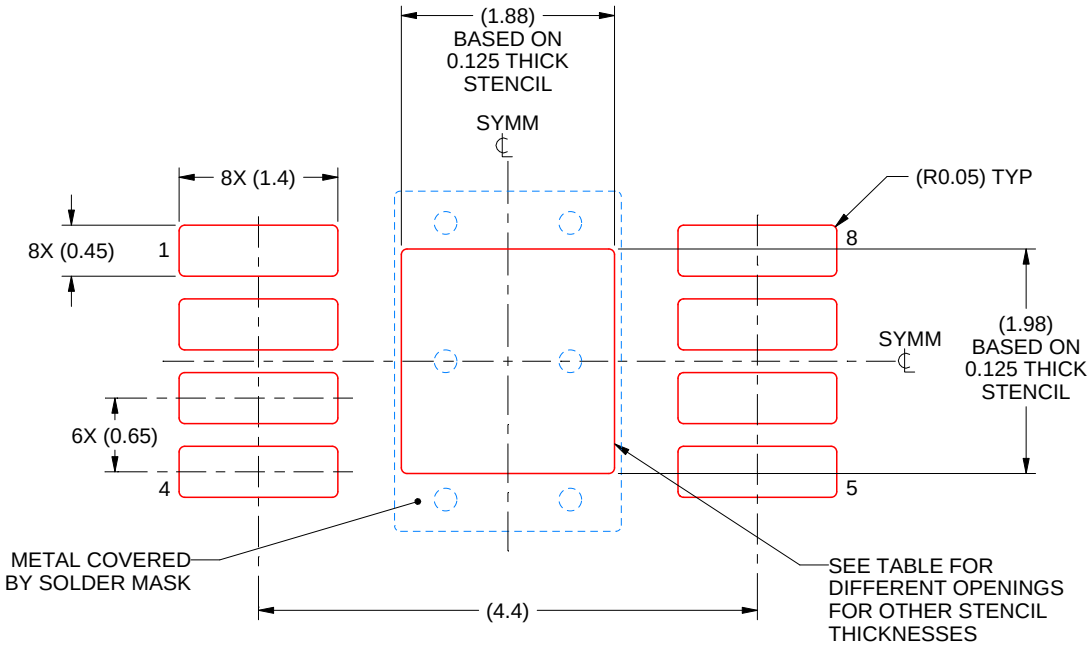
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 2.10 X 2.21 |
| 0.125 | 1.88 X 1.98 (SHOWN) |
| 0.15 | 1.72 X 1.81 |
| 0.175 | 1.59 X 1.67 |

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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