TPS79901-EP 200mA、低静止電流、超低ノイズ、高PSRR 低ドロップアウト・リニア・レギュレータ

1 特長

- ENを備えた200mA低ドロップアウト・レギュレータ
- 複数の出力電圧バージョンを利用可能:
  - 可変出力: 1.2V～6.5V
- ENトグルによる突入電流保護
- 低いI_Q: 40µA
- 高PSRR:
  - 1kHz時に66dB
  - 10kHz時に51dB
- 標準2µFの低ESR出力容量で安定動作
- 非常に優れた負荷/ライン過渡応答
- 総合精度2% (負荷、ライン、温度)
- 非常に低いドロップアウト: 100mV
- パッケージ: 6ピンSON
- 防衛、航空宇宙、および医療アプリケーションをサポート
  - 管理されたベースライン
  - 単一のアセンブリ/テスト施設
  - 単一の製造施設
  - 軍用温度範囲(-55℃～125℃)で利用可能
  - 長期にわたる製品ライフ・サイクル
  - 製品変更通知の延長
  - 製品のトレーサビリティ

2 アプリケーション

- 基地局
- スマートフォン
- EPOS
- ウェアラブル・エレクトロニクス
- VCO、RF
- ワイヤレスLAN、 Bluetooth®

3 概要

TPS79901ファミリの低ドロップアウト(LDO)低消費電力リニア・レギュレータは、極めて低いグランド電流で優れたAC性能を提供します。高い電源除去比(PSRR)、低ノイズ、高速スタートアップ、優れたライン/負荷過渡応答を実現しながら、消費するグランド電流はわずか40µA (標準)です。

TPS79901は、セラミック・コンデンサで安定動作が可能であり、また、先進のBiCMOS製造プロセスの採用により、200mA出力で標準100mVのドロップアウト電圧を実現しています。高性能な電圧リファレンスと帰還ループにより、すべての負荷、ライン、製造プロセス、および温度変化に対して2%の総合精度を達成できます。TPS79901は、ENトグルを使用したデバイス起動時の突入電流保護を特長としており、即座に電流をクランプします。

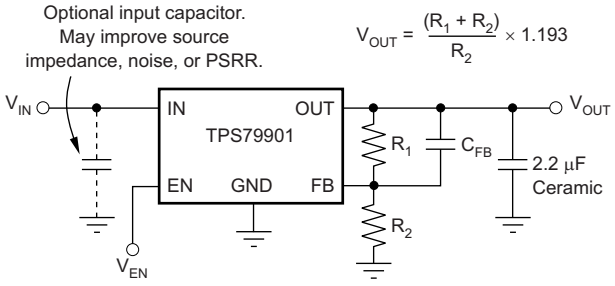
TPS79901は、T_J＝－55℃～＋125℃の温度範囲で仕様が完全に規定されています。低プロファイルで供給され、ワイヤレス・ハンドセットやWLANカードに最適です。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS79901-EP	SON (6)	2.00mm×2.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

代表的なアプリケーション回路



目次

4 改訂履歴

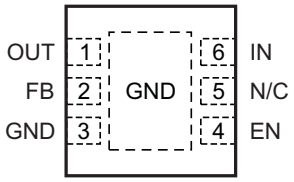
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2017年9月発行のものから更新 **Page**

- 「*特長*」セクションの内容 変更 ... 1
- 「*概要*」セクションの内容 変更 ... 1
- Deleted NR from the Pin Functions table ... 3
- Changed HBM value from ±2000 : to ±1500 in the *ESD Ratings* section ... 4
- Deleted errant part numbers from the *Electrical Characteristics* section ... 5
- Deleted errant part numbers from the *Typical Characteristics* section ... 7

5 Pin Configuration and Functions

DRV Package
6-Pin SON With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN	6	I	Input supply.
GND	3, Pad	—	Ground. The pad must be tied to GND.
EN	4	I	Driving this pin high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
FB	2	I	Adjustable voltage version only. Feedback; this pin is the input to the control loop error amplifier and sets the output voltage of the device.
OUT	1	O	Output of the regulator. To assure stability, a small ceramic capacitor (total typical capacitance ≥ 2 μF) is required from this pin to ground.
N/C	5	—	Not internally connected. This pin must either be left open or tied to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	IN	–0.3	7	V
	EN	–0.3	V_{IN} + 0.3	
	OUT	–0.3	V_{IN} + 0.3	
Current	OUT	Internally limited		mA
Temperature	Operating virtual junction, T_J	–55	150	°C
	Storage temperature range, T_{stg}	–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage(1)	2.7		6.5	V
I_{OUT}	Output current	0.5		200	mA
T_J	Operating junction temperature	–55		125	°C

(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 2.7 V, whichever is greater.

6.4 Thermal Information

THERMAL METRIC(1)		TPS799 DRV (SON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	145.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.2	°C/W

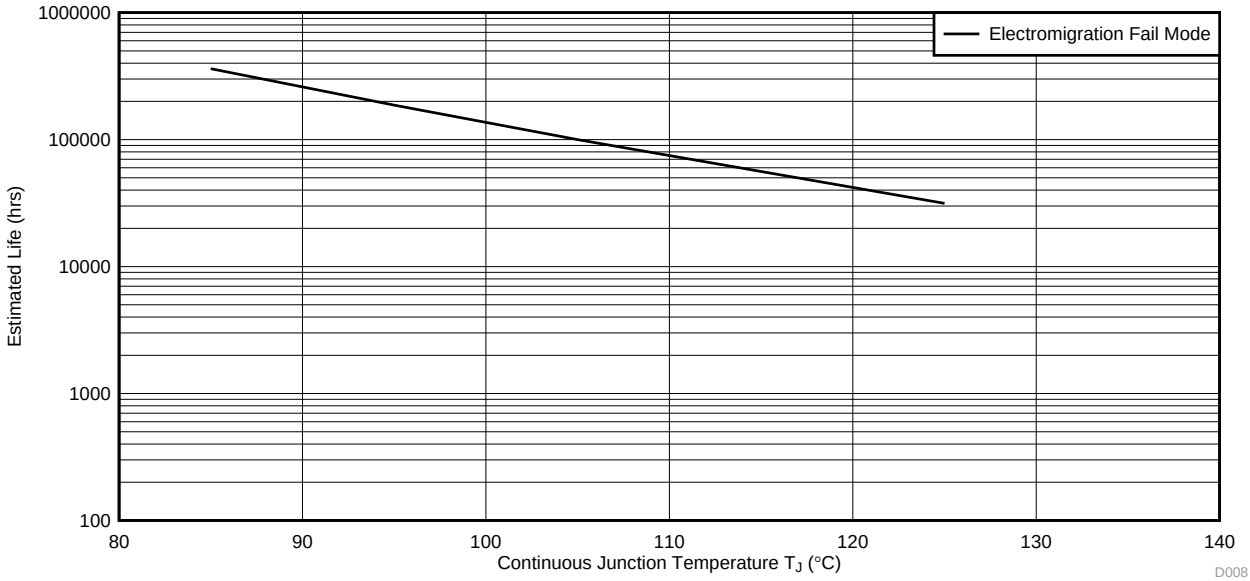
(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

at T_J = –55°C to +125°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, C_{NR} = 0.01 µF, and V_{OUT} = 3 V (unless otherwise noted). Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range			2.7		6.5	V
V_{FB}	Internal reference			1.169	1.193	1.217	V
V_{OUT}	Output voltage range			V_{FB}	6.5 – V_{DO}		V
	Output accuracy, nominal	T_J = 25°C		–1%		1%	
	Output accuracy(1) over V_{IN}, I_{OUT}, temperature	V_{OUT} + 0.3 V ≤ V_{IN} ≤ 6.5 V 500 µA ≤ I_{OUT} ≤ 200 mA		–2%	±1%	2%	
$\Delta V_{O(\Delta VI)}$	Line regulation(1)	$V_{OUT(NOM)}$ + 0.3 V ≤ V_{IN} ≤ 6.5 V			0.02		%/V
$\Delta V_{O(\Delta IO)}$	Load regulation	500 µA ≤ I_{OUT} ≤ 200 mA			0.002		%/mA
V_{DO}	Dropout voltage(2) (V_{IN} = $V_{OUT(nom)}$ – 0.1 V)	I_{OUT} = 200 mA	$V_{OUT(nom)}$ ≤ 3.3 V		100	175	mV
			$V_{OUT(nom)}$ ≥ 3.3 V		90	160	
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(nom)}$		220	400	600	mA
I_{GND}	Ground pin current	500 µA ≤ I_{OUT} ≤ 200 mA			40	60	µA
I_{SHDN}	Shutdown current (I_{GND})	V_{EN} ≤ 0.4 V, 2.7 V ≤ V_{IN} ≤ 6.5 V			0.15	1	µA
I_{FB}	Feedback pin current			–0.5		0.5	µA
PSRR	Power-supply rejection ratio	V_{IN} = 3.85 V, V_{OUT} = 2.85 V, C_{NR} = 0.01 µF, I_{OUT} = 100 mA	f = 100 Hz		70		dB
			f = 1 kHz		66		
			f = 10 kHz		51		
			f = 100 kHz		38		
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, V_{OUT} = 2.85 V	C_{NR} = 0.01 µF		10.5 × V_{OUT}		μV_{RMS}
			C_{NR} = none		94 × V_{OUT}		
	Start-up time	V_{OUT} = 2.85 V, R_L = 14 Ω, C_{OUT} = 2.2 µF	C_{NR} = 0.001 µF		45		µs
			C_{NR} = 0.047 µF		45		
			C_{NR} = 0.01 µF		50		
			C_{NR} = none		50		
$V_{EN(HI)}$	Enable high (enabled)			1.2		V_{IN}	V
$V_{EN(LO)}$	Enable low (shutdown)			0		0.4	V
$I_{EN(HI)}$	Enable pin current, enabled	V_{EN} = V_{IN} = 6.5 V			0.03	1	µA
UVLO	Undervoltage lockout	V_{IN} rising		1.90	2.20	2.65	V
	UVLO hysteresis	V_{IN} falling			70		mV
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing			165		°C
		Reset, temperature decreasing			145		

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 2.7 V, whichever is greater.
(2) V_{DO} is not measured for $V_{OUT(nom)}$ < 2.8 V because minimum V_{IN} = 2.7 V.



(1) See data sheet for absolute maximum and minimum recommended operating conditions.

(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

(3) Enhanced plastic product disclaimer applies.

Figure 1. TPS79901-EP Derating Chart

6.6 Typical Characteristics

at T_J= –55°C to +125°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, C_{NR} = 0.01 µF, and V_{OUT} = 3 V (unless otherwise noted). Typical values are at T_J = 25°C.

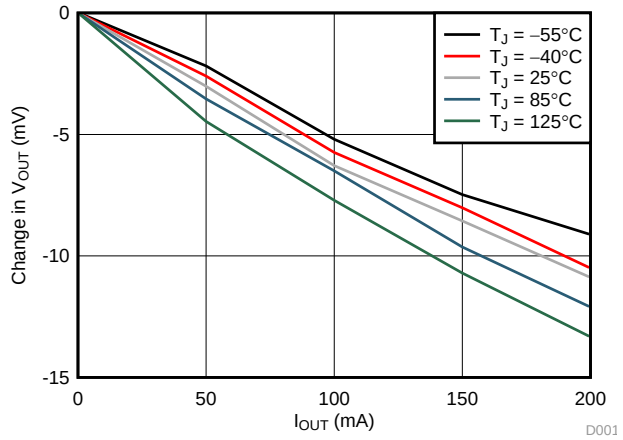


Figure 2. Load Regulation

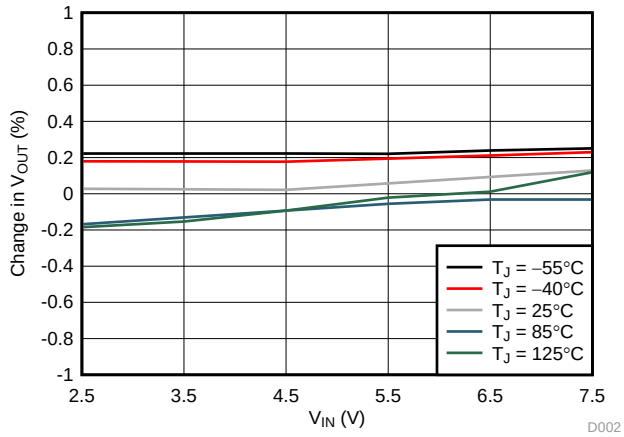


Figure 3. Line Regulation

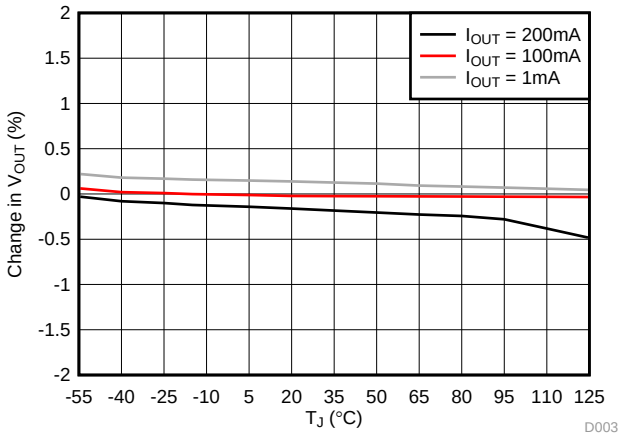


Figure 4. Output Voltage vs Junction Temperature

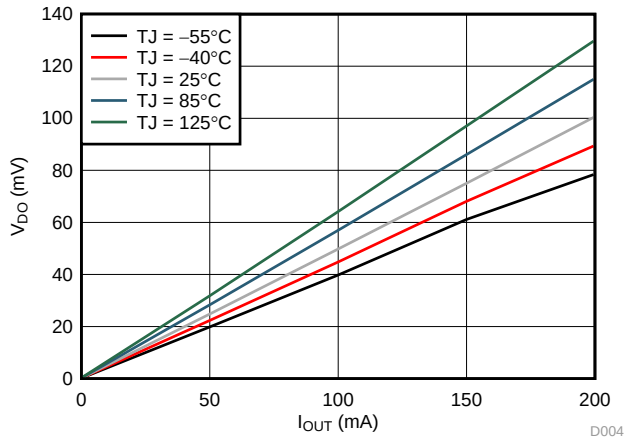


Figure 5. Dropout Voltage vs Output Current

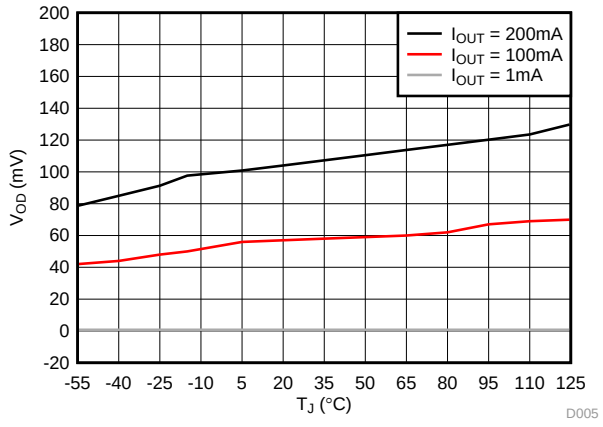


Figure 6. Dropout Voltage vs Junction Temperature

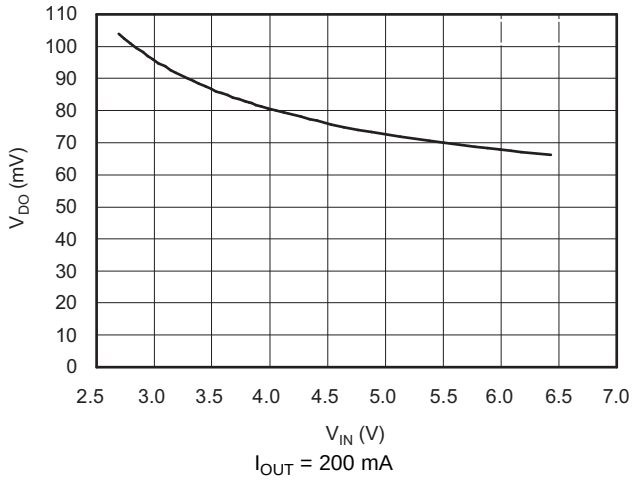


Figure 7. Dropout vs Input Voltage

Typical Characteristics (continued)

at T_J= –55°C to +125°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, C_{NR} = 0.01 µF, and V_{OUT} = 3 V (unless otherwise noted). Typical values are at T_J = 25°C.

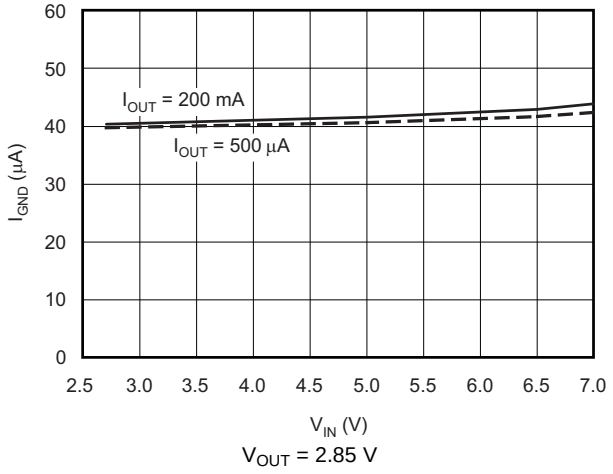


Figure 8. Ground Pin Current vs Input Voltage

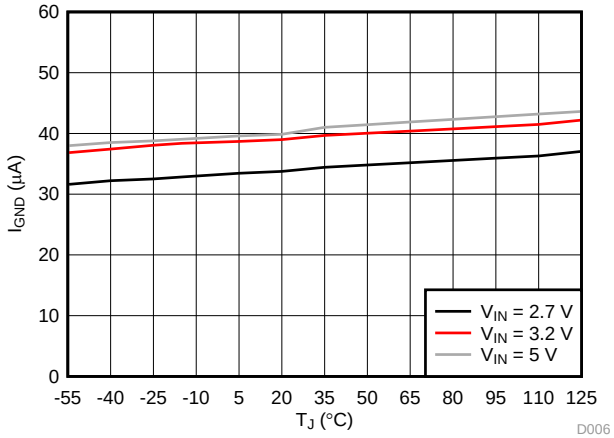


Figure 9. Ground Pin Current vs Junction Temperature

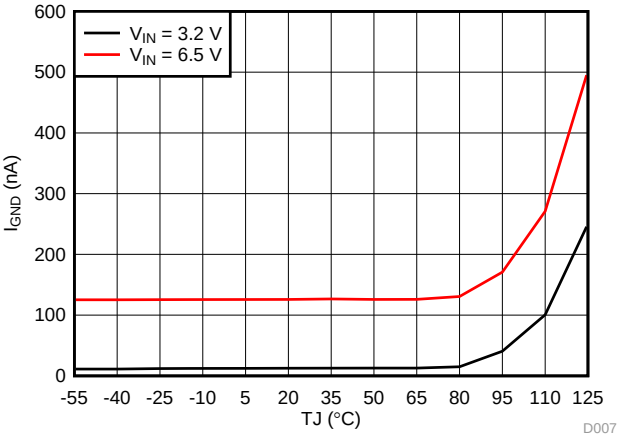
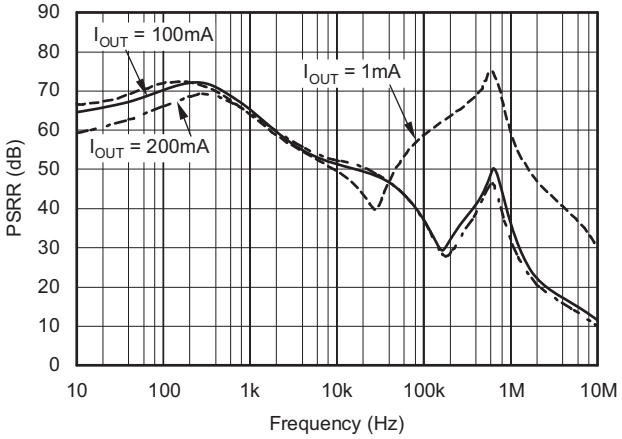
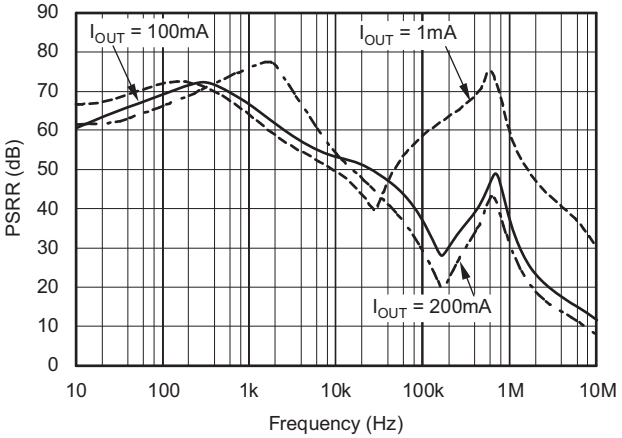


Figure 10. Ground Pin Current (Disabled) vs Junction Temperature



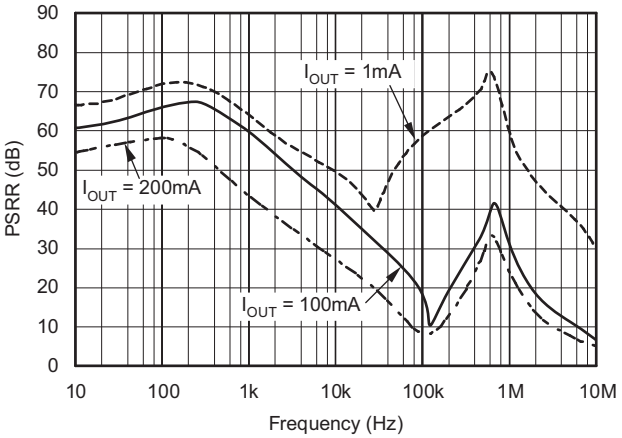
V_{IN} – V_{OUT} = 1 V
C_{NR} = 0.01 µF
V_{OUT} = 2.85 V
C_{OUT} = 2.2 µF

Figure 11. Power-Supply Ripple Rejection vs Frequency



V_{IN} – V_{OUT} = 0.5 V
C_{NR} = 0.01 µF
V_{OUT} = 2.85 V
C_{OUT} = 2.2 µF

Figure 12. Power-Supply Ripple Rejection vs Frequency

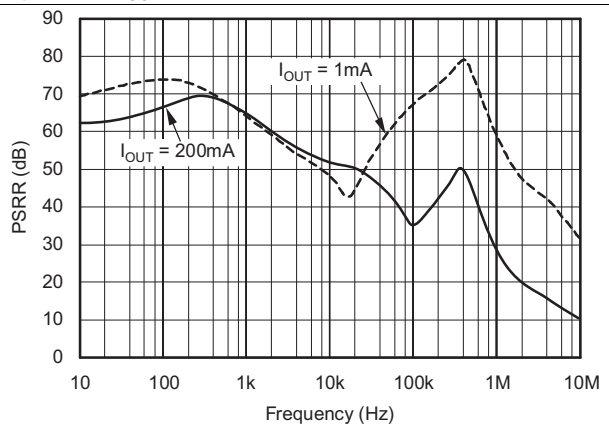


V_{IN} – V_{OUT} = 0.25 V
C_{NR} = 0.01 µF
V_{OUT} = 2.85 V
C_{OUT} = 2.2 µF

Figure 13. Power-Supply Ripple Rejection vs Frequency

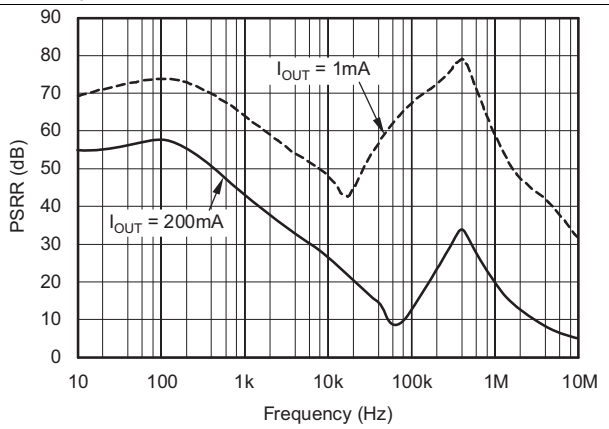
Typical Characteristics (continued)

at T_J= –55°C to +125°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, C_{NR} = 0.01 µF, and V_{OUT} = 3 V (unless otherwise noted). Typical values are at T_J = 25°C.



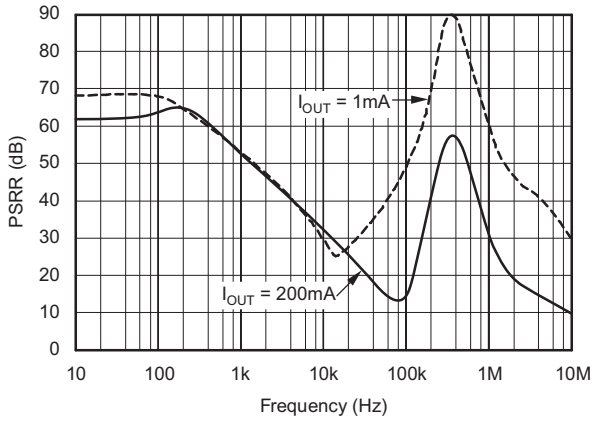
V_{IN} – V_{OUT} = 1 V
V_{OUT} = 2.85 V
C_{NR} = 0.01 µF
C_{OUT} = 10 µF

Figure 14. Power-Supply Ripple Rejection vs Frequency



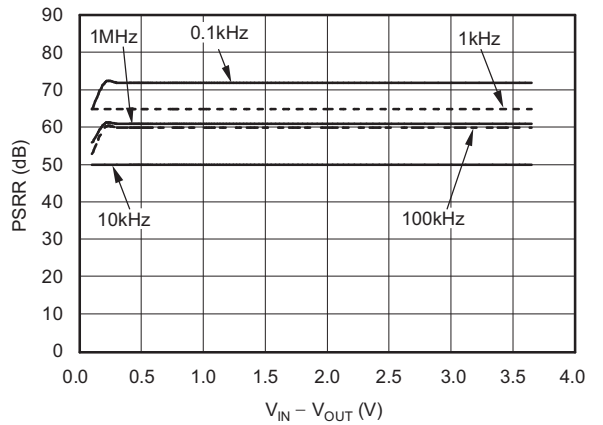
V_{IN} – V_{OUT} = 0.25 V
V_{OUT} = 2.85 V
C_{NR} = 0.01 µF
C_{OUT} = 10 µF

Figure 15. Power-Supply Ripple Rejection vs Frequency



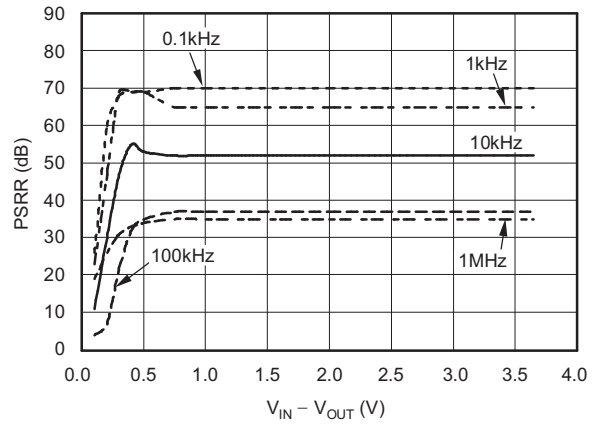
V_{IN} – V_{OUT} = 1 V
V_{OUT} = 2.85 V
C_{OUT} = 10 µF

Figure 16. Power-Supply Ripple Rejection vs Frequency



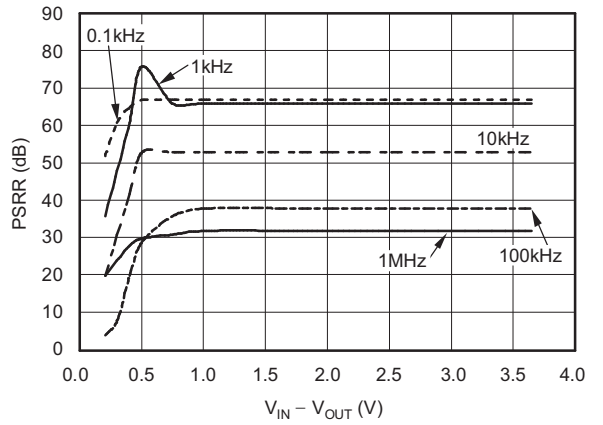
I_{OUT} = 1 mA
C_{NR} = 0.01 µF
C_{OUT} = 2.2 µF

Figure 17. Power-Supply Ripple Rejection vs V_{IN} – V_{OUT}



I_{OUT} = 100 mA
C_{NR} = 0.01 µF
C_{OUT} = 2.2 µF

Figure 18. Power-Supply Ripple Rejection vs V_{IN} – V_{OUT}

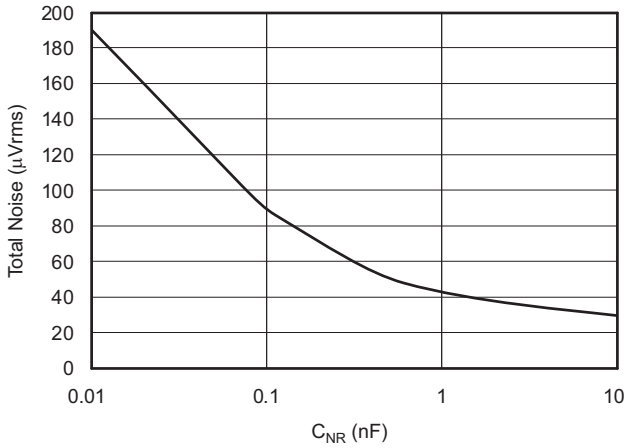


I_{OUT} = 200 mA
C_{NR} = 0.01 µF
C_{OUT} = 2.2 µF

Figure 19. Power-Supply Ripple Rejection vs V_{IN} – V_{OUT}

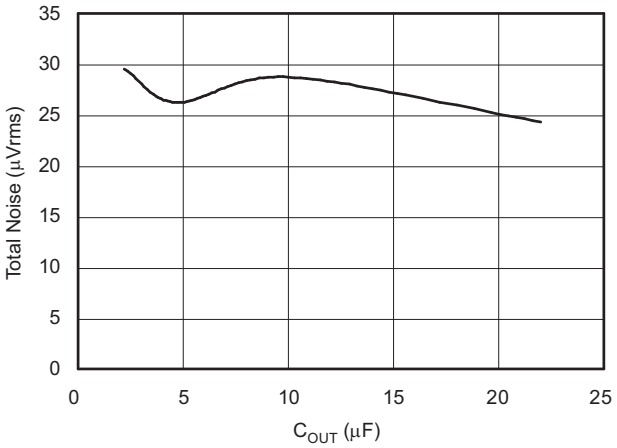
Typical Characteristics (continued)

at T_J= –55°C to +125°C, $V_{IN} = V_{OUT(nom)}$ + 0.3 V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, $V_{EN} = V_{IN}$, C_{OUT} = 2.2 µF, C_{NR} = 0.01 µF, and V_{OUT} = 3 V (unless otherwise noted). Typical values are at T_J = 25°C.



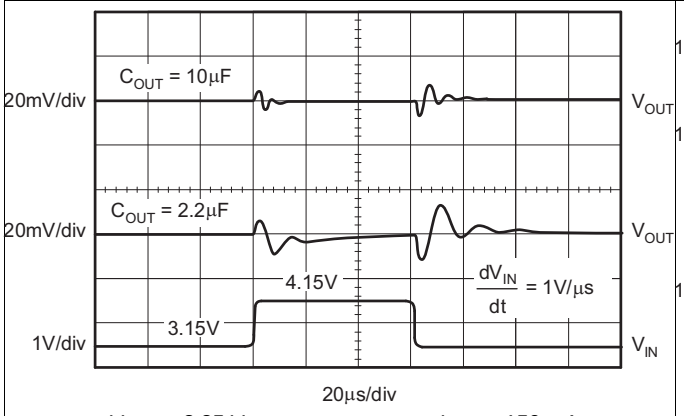
V_{OUT} = 2.85 V I_{OUT} = 1 mA
C_{OUT} = 2.2 µF

Figure 20. Total Noise vs C_{NR}



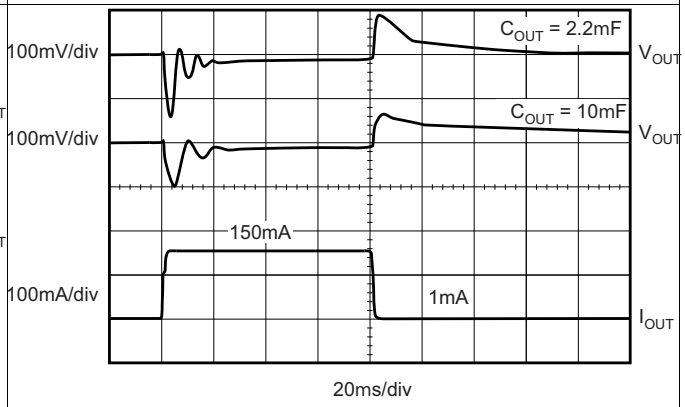
V_{OUT} = 2.85 V I_{OUT} = 1 mA
C_{NR} = 0.01 µF

Figure 21. Total Noise vs C_{OUT}



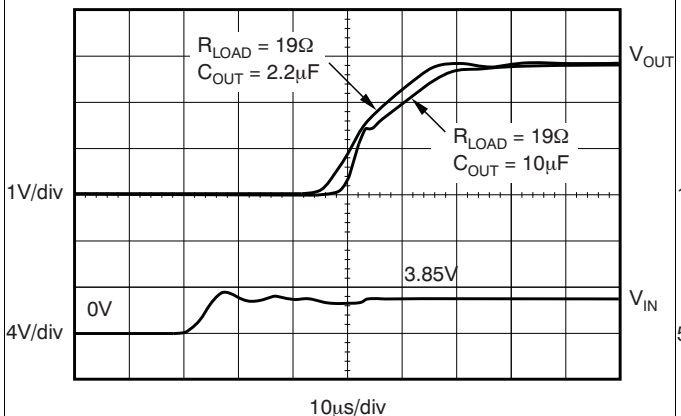
V_{OUT} = 2.85 V I_{OUT} = 150 mA

Figure 22. Line Transient Response



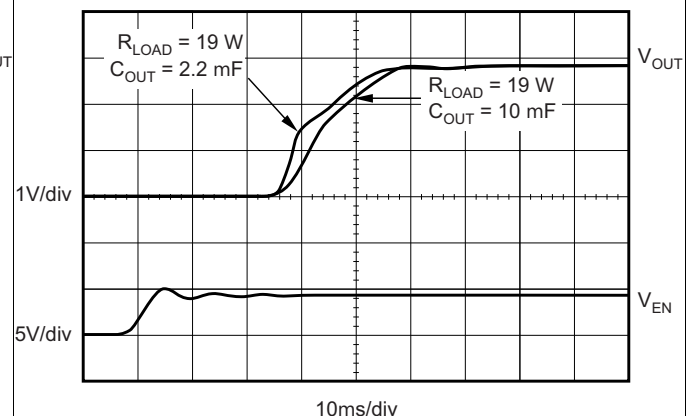
V_{IN} = 3.35 V V_{OUT} = 2.85 V

Figure 23. Load Transient Response



$V_{EN} = V_{IN}$ V_{OUT} = 2.85 V

Figure 24. Turn-On Response



V_{IN} = 3.85 V V_{OUT} = 2.85 V

Figure 25. Enable Response

Typical Characteristics (continued)

at T_J= –55°C to +125°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 μF, C_{NR} = 0.01 μF, and V_{OUT} = 3 V (unless otherwise noted). Typical values are at T_J = 25°C.

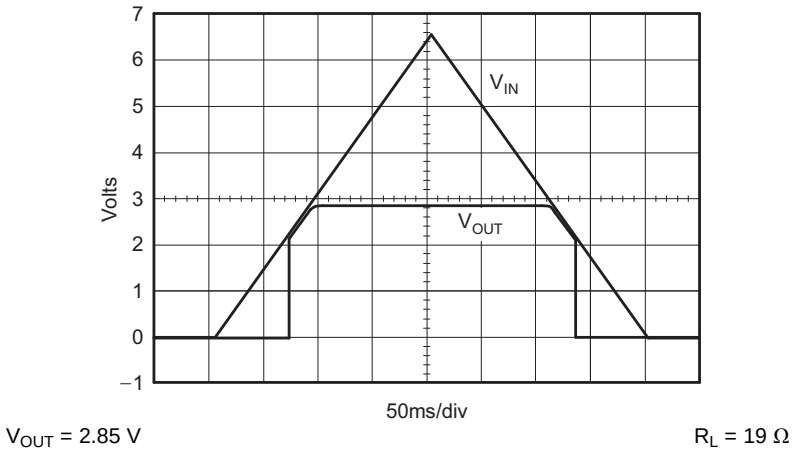


Figure 26. Power-Up and Power-Down

7 Detailed Description

7.1 Overview

The TPS79901 low-dropout (LDO) regulator combines the high performance required of many RF and precision analog applications with ultra-low-current consumption. High PSRR is provided by a high-gain, high-bandwidth error loop with good supply rejection at very low headroom (V_{IN} – V_{OUT}). A noise-reduction pin is provided to bypass noise generated by the band-gap reference and to improve PSRR, while a quick-start circuit quickly charges this capacitor at start-up. The combination of high performance and low ground current also make these devices an excellent choice for portable applications. All versions have thermal and overcurrent protection, and are fully specified from –55°C to +125°C.

The TPS79901 also features inrush current protection with an EN toggle start-up, and overshoot detection at the output. When the EN toggle is used to start the device, current limit protection is immediately activated, restricting the inrush current to the device. If voltage at the output overshoots 5% from the nominal value, a pulldown resistor reduces the voltage to normal operating conditions, as shown in the *Functional Block Diagram*.

7.2 Functional Block Diagram

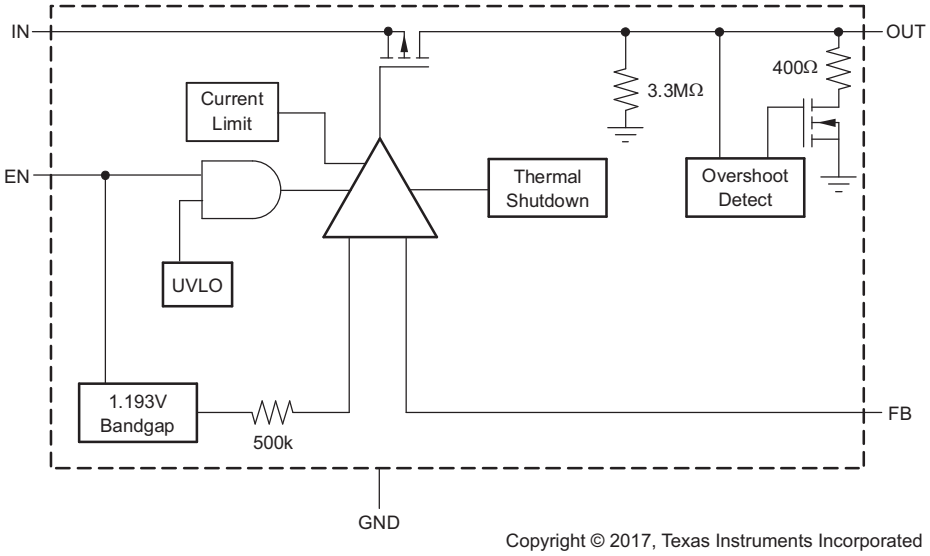


Figure 27. Adjustable-Voltage Versions

7.3 Feature Description

7.3.1 Internal Current Limit

The TPS79901 internal current limit helps protect the regulator during fault conditions. In current limit mode, the output sources a fixed amount of current that is largely independent of the output voltage. For reliable operation, do not operate the device in a current-limit state for extended periods of time.

The PMOS pass element in the TPS79901 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited; therefore, if extended reverse voltage operation is anticipated, external limiting may be required.

7.3.2 Shutdown

The enable pin (EN) is active high and is compatible with standard and low-voltage TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

Feature Description (continued)

7.3.3 Start Up

The TPS79901 uses a start-up circuit to quickly charge the noise reduction capacitor, C_{NR}, if present (see the *Functional Block Diagram*). This circuit allows for the combination of very low output noise and fast start-up times. The NR pin is high impedance so a low leakage C_{NR} capacitor must be used; most ceramic capacitors are appropriate for this configuration.

Note that for fastest start-up, apply V_{IN} first, and then drive the enable pin (EN) high. If EN is tied to IN, start-up is somewhat slower. The start-up switch is closed for approximately 135 μs. To ensure that C_{NR} is fully charged during start-up, use a 0.01-μF or smaller capacitor.

7.3.4 Undervoltage Lockout (UVLO)

The TPS79901 use an undervoltage lockout circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has a deglitch feature so that undershoot transients are typically ignored on the input if these transients are less than 50 μs in duration.

7.4 Device Functional Modes

Driving EN over 1.2-V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode, thus reducing the operating current to 150 nA, nominal.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS79901 LDO regulator provides high PSRR while maintaining ultra-low-current consumption. The device also features inrush current protection and overshoot detection at the output.

8.2 Typical Applications

Figure 28 shows the basic circuit connections.

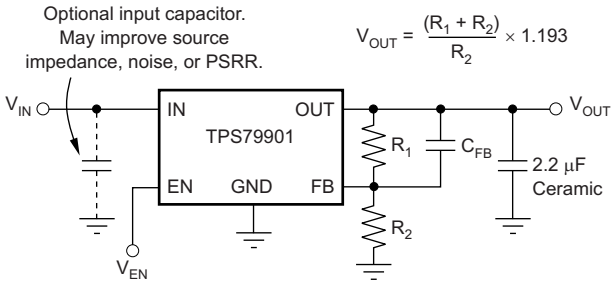


Figure 28. Typical Application Circuit for Adjustable Voltage Version

8.2.1 Design Requirements

Select the desired device based on the output voltage.

Provide an input supply with adequate headroom to account for dropout and output current to account for the GND terminal current, and power the load.

Typical Applications (continued)

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1-μF to 1-μF low ESR capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1-μF input capacitor may be necessary to ensure stability.

The TPS79901 is designed to be stable with standard ceramic capacitors with values of 2.2 μF or greater. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR must be less than 1 Ω.

8.2.2.2 Output Noise

In most LDOs, the band gap is the dominant noise source. If a noise-reduction capacitor (C_{NR}) is used with the TPS79901, the band gap does not contribute significantly to noise. Instead, noise is dominated by the output resistor divider and the error amplifier input. To minimize noise in a given application, use a 0.01-μF noise reduction capacitor. To further optimize noise, equivalent series resistance of the output capacitor can be set to approximately 0.2 Ω. This configuration maximizes phase margin in the control loop, reducing total output noise by up to 10%.

Noise can be referred to the feedback point; with C_{NR} = 0.01 μF total noise is approximately given by Equation 1:

$$V_N = \frac{10.5\mu V_{RMS}}{V} \times V_{OUT} \quad (1)$$

8.2.2.3 Dropout Voltage

The TPS79901 uses a PMOS pass transistor to achieve a low-dropout voltage. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and $r_{DS(on)}$ of the PMOS pass element is the input-to-output resistance. Because the PMOS device behaves like a resistor in dropout, V_{DO} approximately scales with the output current.

As with any linear regulator, PSRR degrades as (V_{IN} – V_{OUT}) approaches dropout. This effect is illustrated in Figure 11 through Figure 19 in the *Typical Characteristics* section.

8.2.2.4 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude, but increases the duration of the transient response. The transient response of the TPS799 is enhanced by an active pulldown device that engages when the output overshoots by approximately 5% or more when the device is enabled. When enabled, the pulldown device behaves like a 350-Ω resistor to ground.

8.2.2.5 Minimum Load

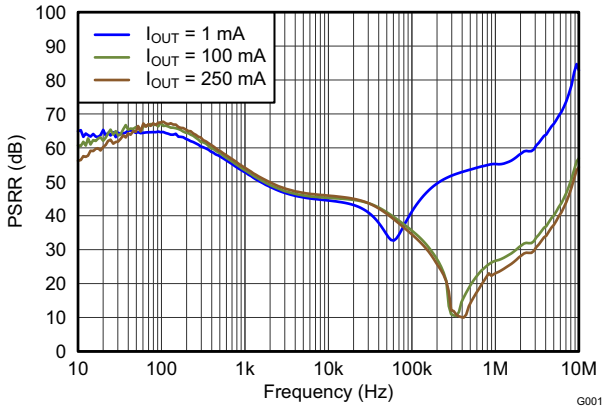
The TPS79901 is stable with no output load. To meet the specified accuracy, a minimum load of 500 μA is required. With loads less than 500 μA at junction temperatures near 125°C, the output can drift up enough to cause the output pulldown device to turn on. The output pulldown device limits voltage drift to 5% typically; however, ground current can increase by approximately 50 μA. In typical applications, the junction cannot reach high temperatures at light loads because there is no noticeable dissipated power. The specified ground current is then valid at no load in most applications.

8.2.2.6 Feedback Capacitor Requirements

The feedback capacitor, C_{FB}, shown in Figure 28 is required for stability. For a parallel combination of R_1 and R_2 equal to 250 kΩ, any value from 3 pF to 1 nF can be used. Values below 5 pF should be used to ensure fast startup; values above 47 pF can be used to implement an output voltage soft-start. Larger value capacitors also improve noise slightly. The TPS79901 is stable in unity-gain configuration (OUT tied to FB) without C_{FB}.

Typical Applications (continued)

8.2.3 Application Curve



C_{OUT} = 2.2 µF C_{NR} = 0.01 µF

Figure 29. Power-Supply Rejection Ratio vs Frequency

8.3 Do's and Don'ts

Do place at least one 2.2-µF ceramic capacitor as close as possible to the OUT pin of the regulator.

Do not place the output capacitor more than 10 mm away from the regulator.

Do connect a 0.1-µF to 1-µF low equivalent series resistance (ESR) capacitor across the IN pin and GND input of the regulator.

Do not exceed the absolute maximum ratings.

9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range between 2.7 V and 6.5 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply is well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance (such as PSRR, output noise, and transient response), design the board with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, connect the bypass capacitor directly to the GND pin of the device.

10.1.2 Thermal Information

10.1.2.1 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 145°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage resulting from overheating.

Layout Guidelines (continued)

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection triggers at least 35°C above the maximum expected ambient condition of a particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS799 is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the device into thermal shutdown degrades device reliability.

10.1.2.2 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the head from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Thermal Information* table near the front of this data sheet. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current times the voltage drop across the output pass element, as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \cdot I_{OUT} \quad (2)$$

10.1.2.3 Package Mounting

Solder pad footprint recommendations for the TPS799 are available from the TI's website at www.ti.com.

10.2 Layout Example

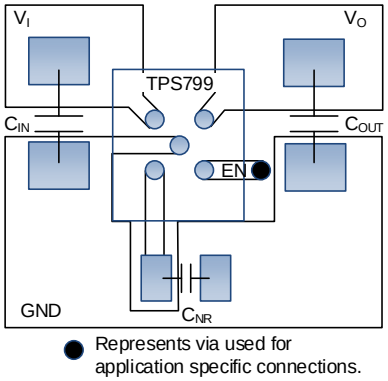


Figure 30. Layout Example

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

11.1.1.1 評価モジュール

TPS799を使用する回路の性能の初期評価に役立てるため、評価モジュール(EVM)を利用可能です。このEVM、TPS799評価モジュールは、テキサス・インスツルメンツのWebサイトの製品フォルダからご請求されるか、TI eStoreから直接お求めになれます。

11.1.1.2 SPICEモデル

SPICEを使用した回路パフォーマンスのコンピュータによるシミュレーションは、アナログ回路やシステムのパフォーマンスを分析するため多くの場合に有用です。TPS799用のSPICEモデルは、製品フォルダの「シミュレーション・モデル」で入手できます。

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- アプリケーション・レポート: *『新しい熱測定基準の使用』*、SBVA025
- アプリケーション・レポート: *『ICパッケージの熱指標』*、SPRA953
- *『TPS799xxEVM-105 ユーザー・ガイド』*、SLVU130

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E (Engineer-to-Engineer) コミュニティ。*** エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.5 商標

E2E is a trademark of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
All other trademarks are the property of their respective owners.

11.6 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79901MDRVTEP	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	17L	Samples
V62/17614-01XE	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	17L	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

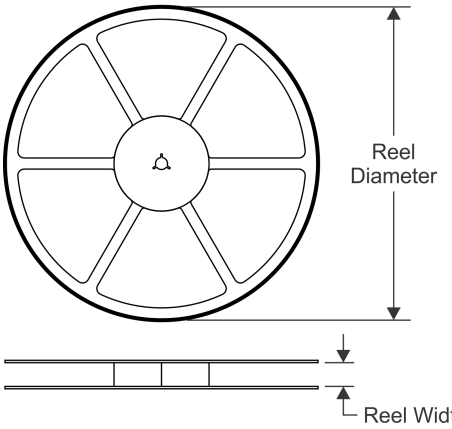
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

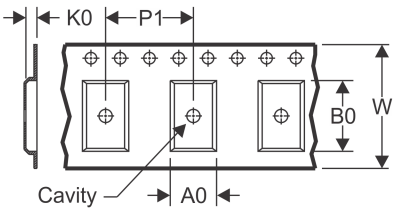
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

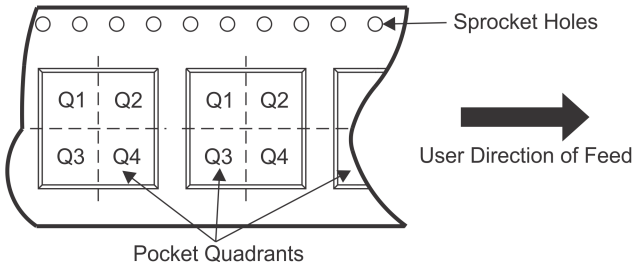


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

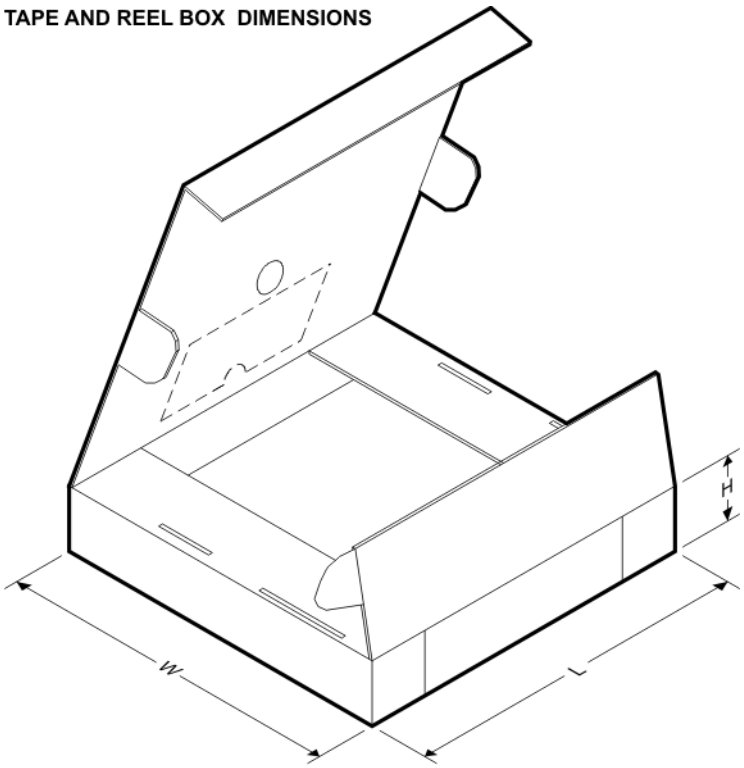
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79901MDRVTEP	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

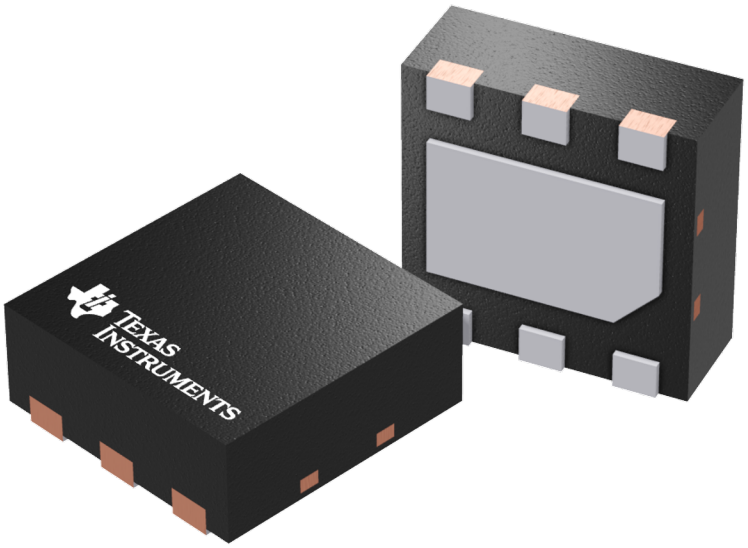


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79901MDRVTEP	WSON	DRV	6	250	203.0	203.0	35.0

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



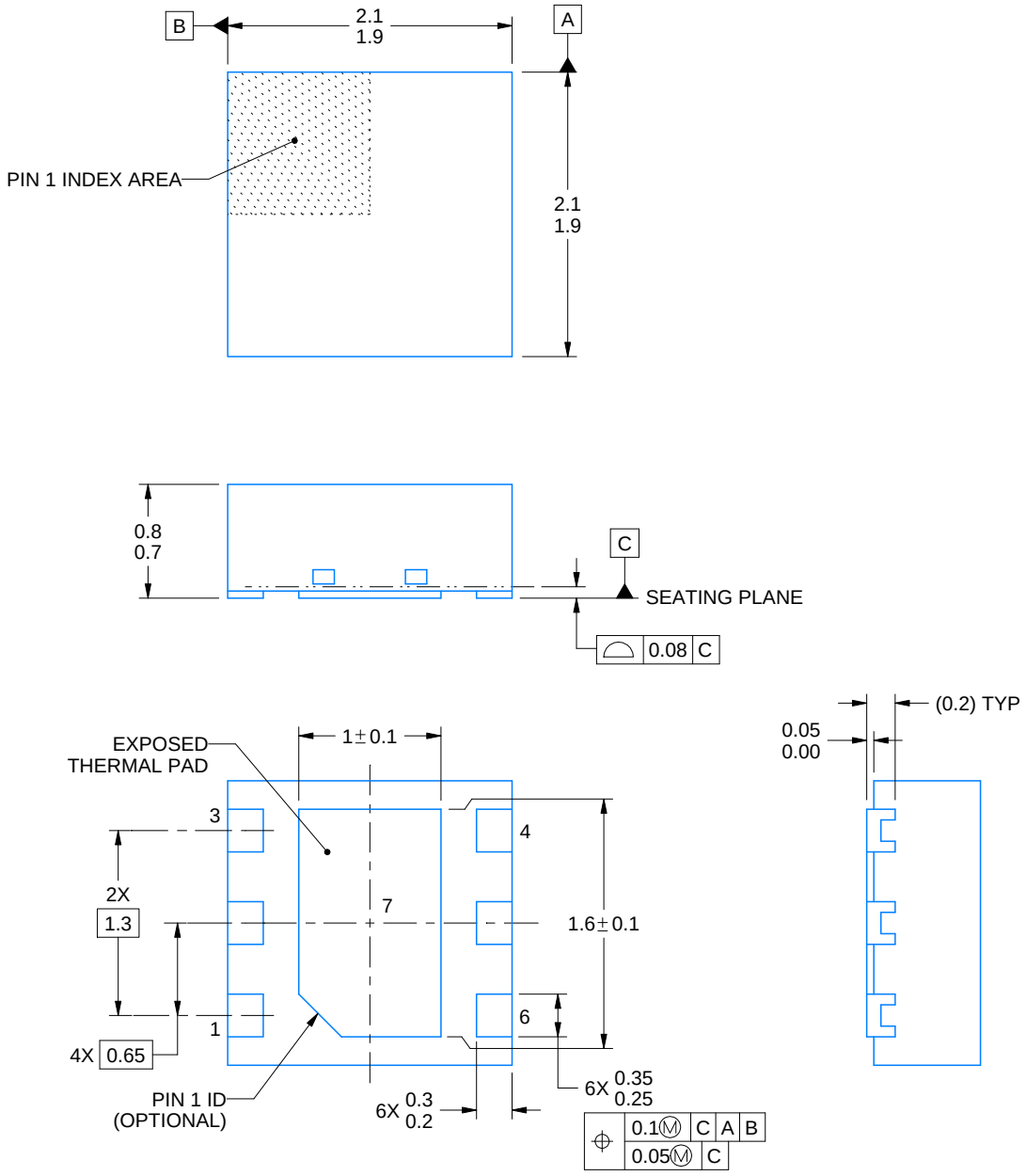
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DRV0006D

PACKAGE OUTLINE

WSON - 0.8 mm max height

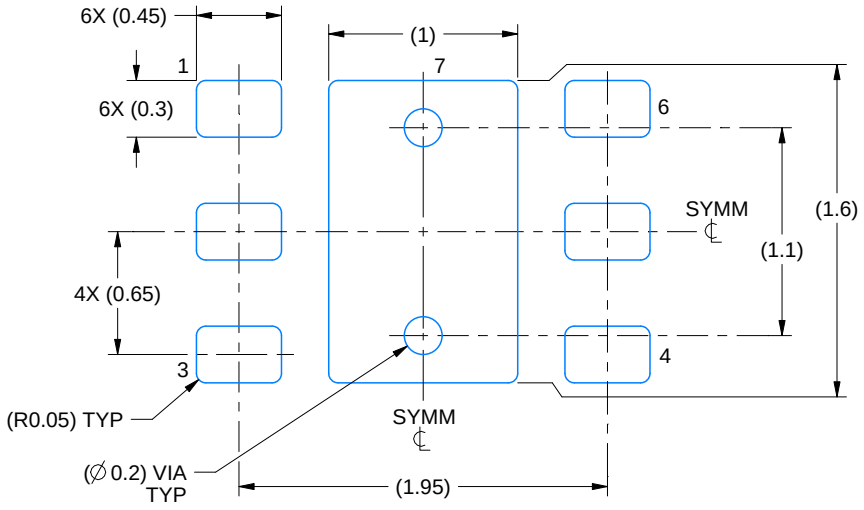
PLASTIC SMALL OUTLINE - NO LEAD



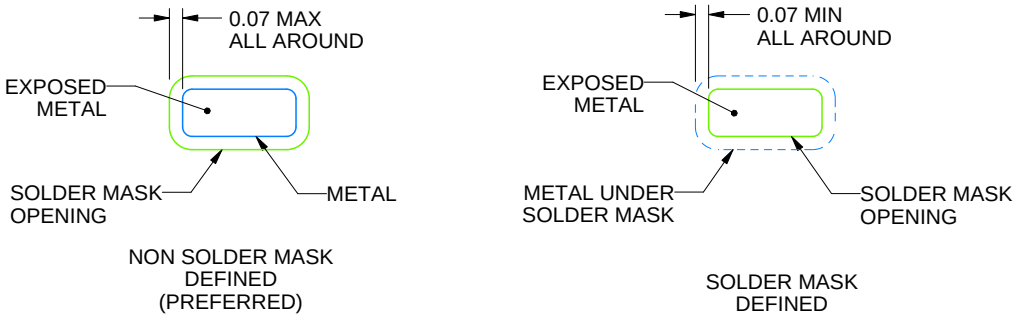
4225563/A 12/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

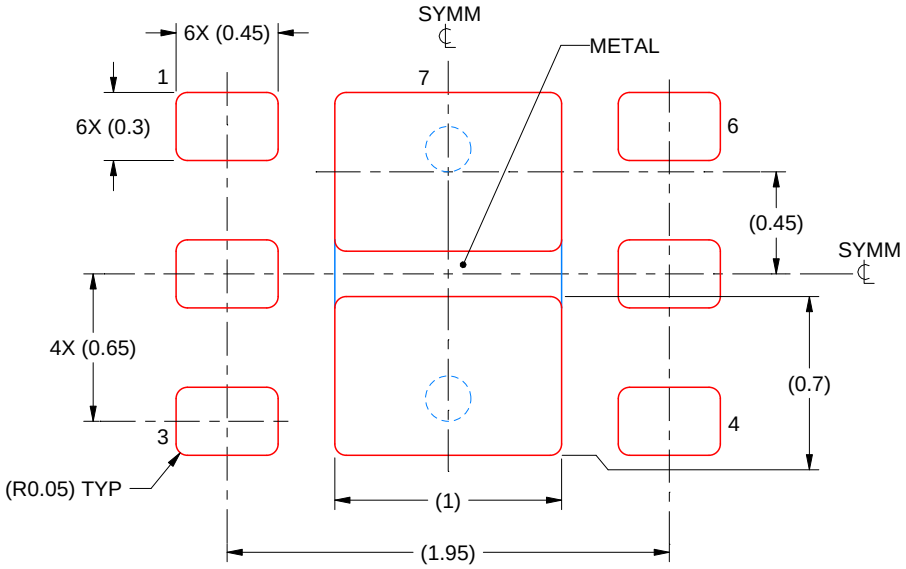


SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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