

TPS7A19

40V、450mA、広 V_{IN} 、低 I_Q 、低ドロップアウト電圧レギュレータ、パワー・グッド搭載

1 特長

- 広い入力電圧範囲: 4V~40V
- 出力電圧を1.5V~18Vの範囲で変更可能
- 出力電流: 450mA
- 低い静止電流(I_Q): 15 μ A
- 低いドロップアウト電圧: 400mAで450mV (最大値)
- 遅延時間をプログラム可能なパワー・グッド
- サーマル・シャットダウンおよび過電流保護機能
- セラミック出力コンデンサで安定動作
 - $V_{OUT} \geq 2.5V$ のとき10 μ F~500 μ F
 - $V_{OUT} < 2.5V$ のとき22 μ F~500 μ F
- 動作温度範囲: -40°C~+125°C
- パッケージ: 3mmx3mm SON-8

2 アプリケーション

- スマート電力網インフラストラクチャと計量
- 電動工具
- モータ・ドライブ
- アクセス制御システム
- 試験/測定機器

3 概要

TPS7A19は低ドロップアウトのリニア・レギュレータ(LDO)で、入力電圧範囲(V_{IN})が最高40Vと広く、最大450mAまでの大きな出力電流(I_{OUT})を供給できます。この電圧レギュレータは、広い入力電圧レールから低電圧の電源を生成するために理想的です。TPS7A19は、適切にレギュレートされた電圧レールを供給するだけでなく、単純なサージ保護回路として機能するため、過渡電圧に耐えられ、その間もレギュレーションを維持できます。

TPS7A19は軽負荷時にわずか15 μ Aの静止電流(I_Q)しか消費しないため、常時オンまたはバッテリー駆動のアプリケーションにおいて消費電力を削減できます。

TPS7A19には、サーマル・シャットダウンと過電流保護機能が搭載されています。また、TPS7A19には、出力電圧がレギュレーション範囲になったことを示すパワー・グッド出力(PG)があり、遅延時間をプログラム可能です。この機能は、電力レールのシーケンス機能に便利です。

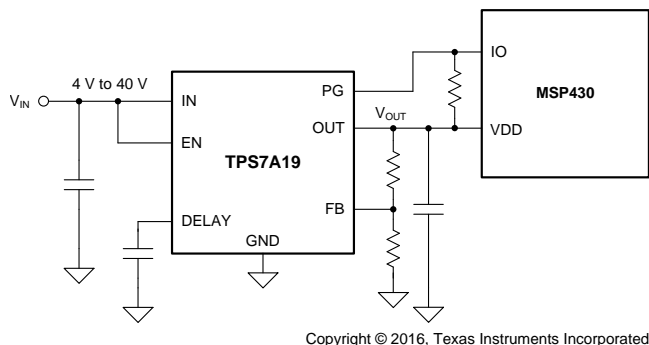
このLDOは、熱特性が強化された3mmx3mmの小さな8ピンSONパッケージで供給されます。

製品情報⁽¹⁾

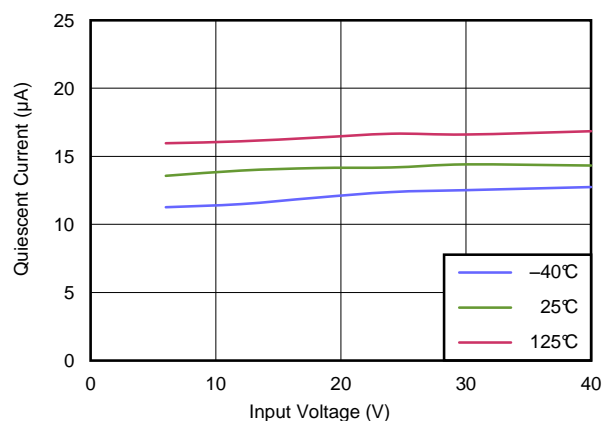
型番	パッケージ	本体サイズ(公称)
TPS7A19	SON (8)	3.00mmx3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

標準アプリケーション回路図



静止電流と入力電圧との関係
($V_{OUT} = 1.5V$)



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4 改訂履歴

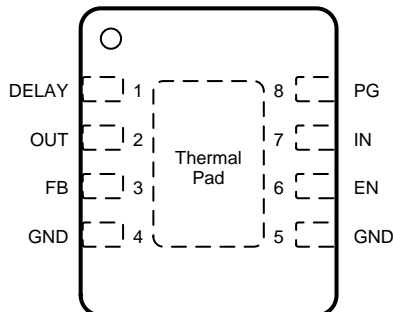
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5 Pin Configuration and Functions

**DRB Package
8-Pin SON With Thermal Pad
Top View**



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DELAY	1	—	Delay pin. Connect a capacitor to GND to adjust the PG delay time; leave open if the PG function is not needed.
EN	6	I	Enable pin. This pin turns the regulator on or off. If $V_{EN} \geq V_{EN_HI}$, the regulator is enabled. If $V_{EN} \leq V_{EN_LO}$, the regulator is disabled. If not used, the EN pin can be connected to IN.
FB	3	I	Feedback pin. The feedback pin is the input to the control-loop error amplifier.
GND	4,5	—	Ground pin.
IN	7	I	Regulator input supply pin.
OUT	2	O	Regulator output pin. When the output voltage is larger than 2.5 V, connect a 10- μ F to 500- μ F ceramic capacitor with an equivalent series resistance (ESR) from 0.001 to 20 Ω to assure stability. When the output voltage is from 1.5 V to 2.5 V, the minimum, stable capacitor value should be 22 μ F.
PG	8	O	Power good. This open-drain pin must be connected to V_{OUT} through an external resistor. PG is pulled low when the output voltage goes below threshold.
Thermal pad		—	Solder to printed-circuit-board (PCB) to enhance thermal performance. Although the thermal pad can be left floating, connect the thermal pad to the ground plane for optimal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range -40°C to 125°C (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
Voltage ⁽²⁾	Input	IN, EN	-0.3	45	V
	Output	OUT ⁽³⁾	-0.3	$V_{\text{IN}} + 0.3$	
		DELAY ⁽⁴⁾	-0.3	45	
		FB, PG	-0.3	22	
Current	Peak output	Internally limited			
Temperature	Operating junction, T_{J}		-40	150	$^{\circ}\text{C}$
	Storage, T_{stg}		-65	150	

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.
- (3) The absolute maximum rating is $V_{\text{IN}} + 0.3\text{ V}$ or 22 V , whichever is lower.
- (4) The voltage at the DELAY pin must be lower than the V_{IN} voltage.

6.2 ESD Ratings

			VALUE	UNIT
$V_{\text{(ESD)}}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	± 500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Input supply voltage		4	40	V
V_{OUT}	Output voltage		1.5	18	V
V_{EN}	Enable voltage		0	40	V
T_{J}	Operating junction temperature		-40	125	$^{\circ}\text{C}$

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾			TPS7A19	UNIT
			DRB (VSON)	
			8 PINS	
$R_{\theta\text{JA}}$	Junction-to-ambient thermal resistance		48	$^{\circ}\text{C}/\text{W}$
$R_{\theta\text{JC(top)}}$	Junction-to-case (top) thermal resistance		56.3	$^{\circ}\text{C}/\text{W}$
$R_{\theta\text{JB}}$	Junction-to-board thermal resistance		22.4	$^{\circ}\text{C}/\text{W}$
Ψ_{JT}	Junction-to-top characterization parameter		0.9	$^{\circ}\text{C}/\text{W}$
Ψ_{JB}	Junction-to-board characterization parameter		22.5	$^{\circ}\text{C}/\text{W}$
$R_{\theta\text{JC(bot)}}$	Junction-to-case (bottom) thermal resistance		4.6	$^{\circ}\text{C}/\text{W}$

- (1) For information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

at $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{IN} = 14\text{ V}$, $V_{EN} = V_{IN}$, $I_{OUT} = 200\ \mu\text{A}$, $C_{IN} = 22\ \mu\text{F}$, and $C_{OUT} = 47\ \mu\text{F}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT						
V_{IN}	Input voltage	$V_{OUT} \leq 3.5\text{ V}$, $I_{OUT} = 0\text{ mA}$ to 450 mA	4		40	V
		$V_{OUT} \geq 3.5\text{ V}$, $I_{OUT} = 0\text{ mA}$ to 450 mA	$V_{OUT} + 0.5$		40	V
I_Q	Quiescent current	$V_{IN} = 4\text{ V}$ to 40 V , $V_{OUT} = 1.5\text{ V}$, $V_{EN} = 5\text{ V}$, $I_{OUT} = 0.2\text{ mA}$		15	25	μA
		$V_{IN} = 18.5\text{ V}$ to 40 V , $V_{OUT} = 18\text{ V}$, $V_{EN} = 5\text{ V}$, $I_{OUT} = 0.2\text{ mA}$		25	40	μA
I_{SHDN}	Shutdown current	$V_{EN} = 0\text{ V}$, $I_{OUT} = 0\text{ mA}$, $V_{IN} = 18\text{ V}$, $V_{OUT} = 1.5\text{ V}$			4	μA
V_{FB}	Feedback voltage	Reference voltage for FB pin	1.208	1.233	1.258	V
V_{IN_UVLO}	Undervoltage lockout	Ramp V_{IN} down until output is turned off			2.6	V
$UVLO_{Hys}$	Undervoltage detection hysteresis	V_{IN} rising		1		V
ENABLE INPUT (EN)						
V_{EN_LO}	Logic input low level		0		0.4	V
V_{EN_HI}	Logic input high level		1.7			V
I_{EN}	EN pin current	$V_{EN} = 40\text{ V}$, $V_{IN} = 14\text{ V}$			1	μA
REGULATED OUTPUT						
V_{OUT}	Regulated output ⁽¹⁾	$V_{IN} = V_{OUT} + 1\text{ V}$ to 40 V and $V_{IN} \geq 4\text{ V}$, $I_{OUT} = 100\ \mu\text{A}$ to 450 mA	-2%		2%	
$\Delta V_{O(\Delta VI)}$	Line regulation	$V_{IN} = V_{OUT} + 1\text{ V}$ to 40 V and $V_{IN} \geq 4\text{ V}$, $I_{OUT} = 100\text{ mA}$			10	mV
$\Delta V_{O(\Delta IL)}$	Load regulation	$I_{OUT} = 1\text{ mA}$ to 450 mA , $V_{IN} = V_{OUT} + 1\text{ V}$ and $V_{IN} \geq 4\text{ V}$			10	mV
V_{DO}	Dropout voltage	$V_{IN} - V_{OUT}$, $I_{OUT} = 400\text{ mA}$		240	450	mV
		$V_{IN} - V_{OUT}$, $I_{OUT} = 200\text{ mA}$		160	300	
I_{OUT}	Output current	V_{OUT} in regulation	0		450	mA
I_{CL}	Output current-limit	V_{OUT} short to ground	140		360	mA
		$V_{OUT} = V_{OUT\text{ nominal}} \times 0.9$	470		850	
PSRR	Power-supply ripple rejection ⁽²⁾	$I_{OUT} = 100\text{ mA}$, $C_{OUT} = 22\ \mu\text{F}$	$f = 100\text{ Hz}$	60		dB
			$f = 100\text{ kHz}$	40		
PG						
V_{OL}	PG output low voltage	$I_{OL} = 0.5\text{ mA}$			0.4	V
I_{OH}	PG leakage current	PG pulled to V_{OUT} with $10\text{-k}\Omega$ resistor			1	μA
$V_{T(PG)}$	Power good threshold	V_{OUT} power-up	89.6	91.6	93.6	% of V_{OUT}
V_{hys}	Hysteresis	V_{OUT} power-down		2		% of V_{OUT}
PG DELAY						
I_{Delay}	Delay capacitor charging current		5	9.5	14	μA
$V_{T(PG_DLY)}$	Delay pin comparator threshold voltage			1		V
TEMPERATURE						
T_{sd}	Junction shutdown temperature	Temperature increasing		175		$^\circ\text{C}$
T_{hys}	Hysteresis of thermal shutdown			24		$^\circ\text{C}$

(1) Accuracy specification does not apply on any application condition that exceeds the power dissipation limit of the package under test. External resistor divider variation is not considered for accuracy measurement.

(2) Design information; not tested, specified by characterization.

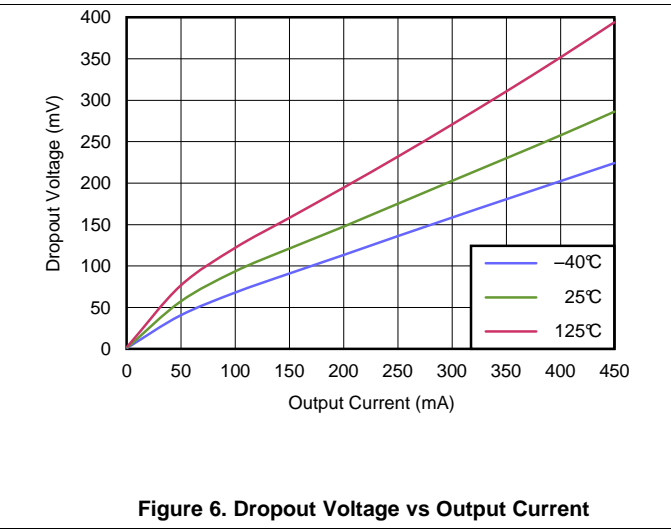
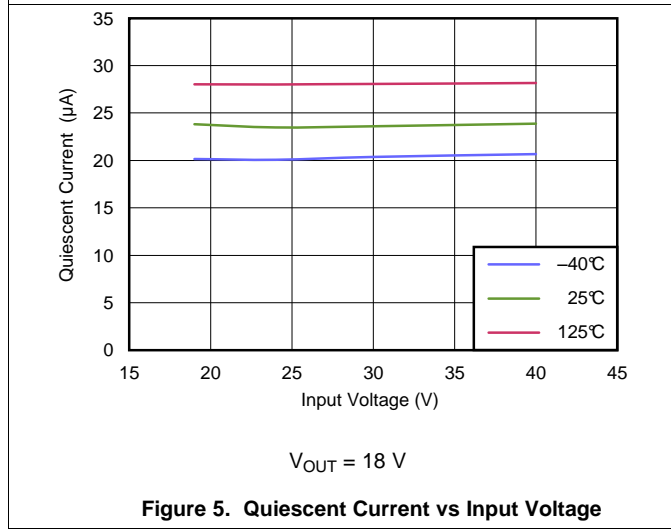
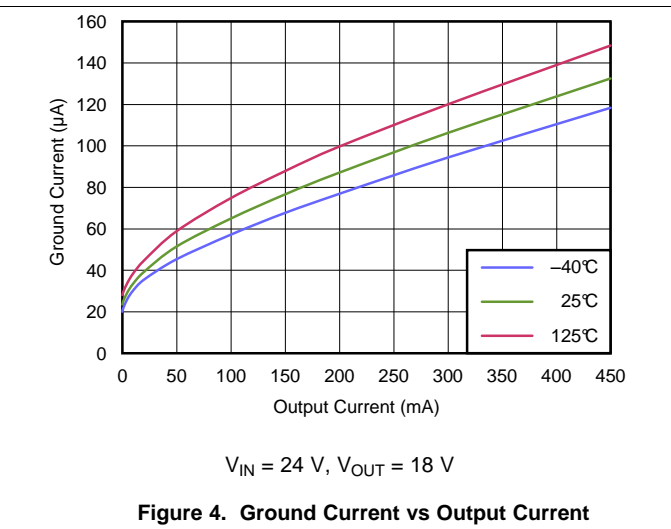
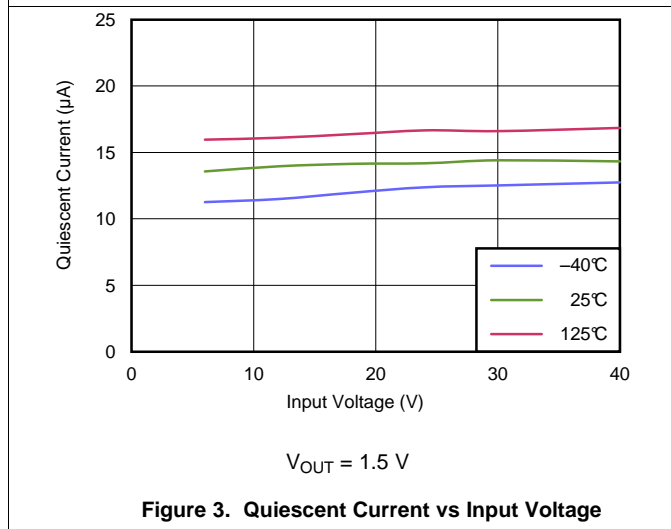
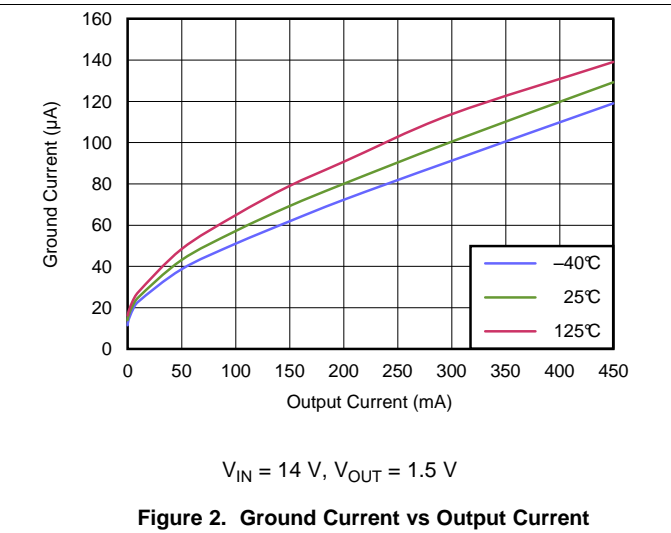
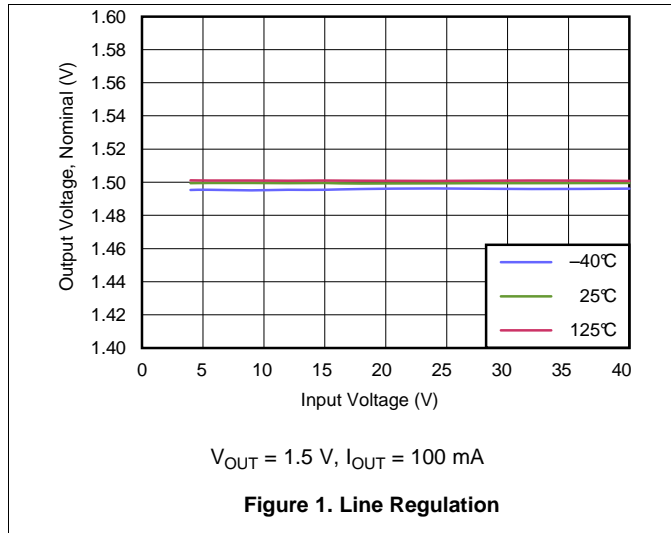
6.6 Timing Requirements

		MIN	TYP	MAX	UNIT
TIMING FOR PG					
t_{PG_DLY}	Power good delay	$C = \text{delay-capacitor value capacitance} = 100\text{ nF}^{(1)}$		10.5	ms
t_{PG_fixed}	Power good delay	No capacitor on pin		325	μs
$t_{PG(HL)}$	PG falling propagation delay	V_{OUT} low to PG low		180	μs

(1) Information only; not tested in production. The equation is based on: $(C \times 1) / (9.5 \times 10^{-6}) = t_{PG_DLY}$, where $C = \text{delay capacitor value capacitance}$; range = 100 pF to 500 nF .

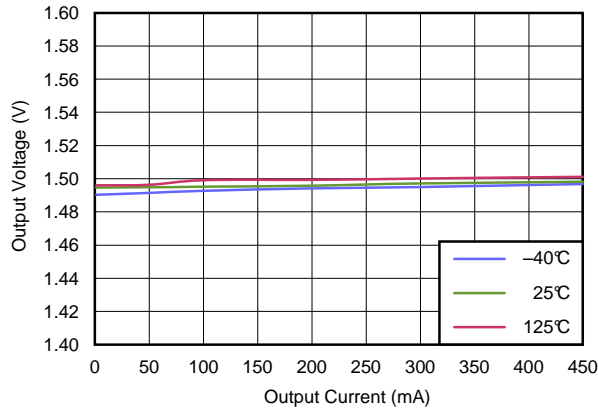
6.7 Typical Characteristics

at $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{IN} = 14\text{ V}$, $V_{EN} = V_{IN}$, $I_{OUT} = 200\ \mu\text{A}$, $C_{IN} = 22\ \mu\text{F}$, and $C_{OUT} = 47\ \mu\text{F}$ (unless otherwise noted)



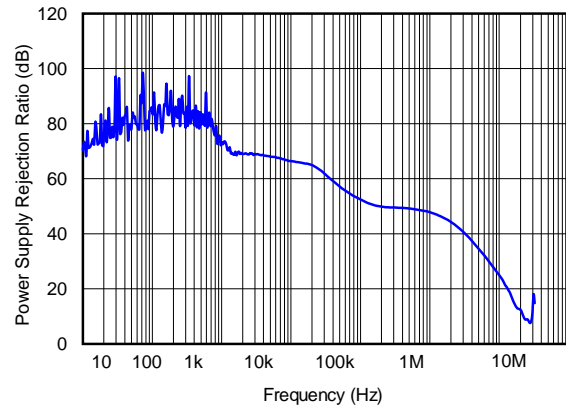
Typical Characteristics (continued)

at $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{IN} = 14\text{ V}$, $V_{EN} = V_{IN}$, $I_{OUT} = 200\ \mu\text{A}$, $C_{IN} = 22\ \mu\text{F}$, and $C_{OUT} = 47\ \mu\text{F}$ (unless otherwise noted)



$V_{IN} = 14\text{ V}$, $V_{OUT} = 1.5\text{ V}$

Figure 7. Load Regulation



$V_{OUT} = 5\text{ V}$, $C_{OUT} = 47\ \mu\text{F}$, $I_{OUT} = 10\text{ mA}$

Figure 8. Power-Supply Rejection Ratio vs Frequency

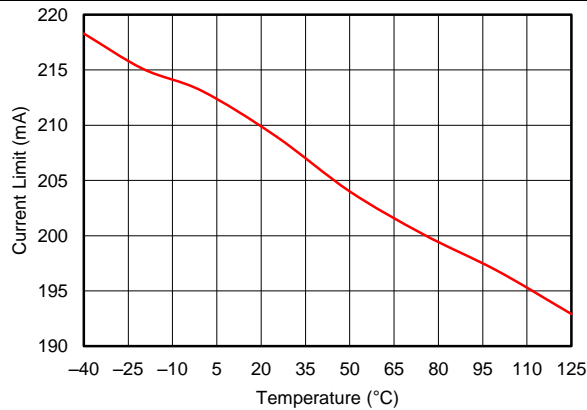


Figure 9. Short to GND Current-Limit vs Temperature

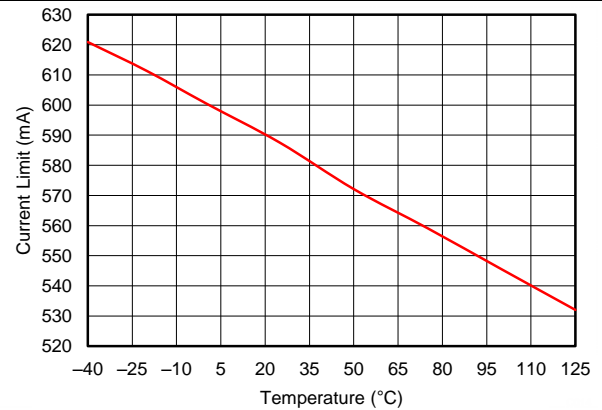


Figure 10. Current-Limit vs Temperature

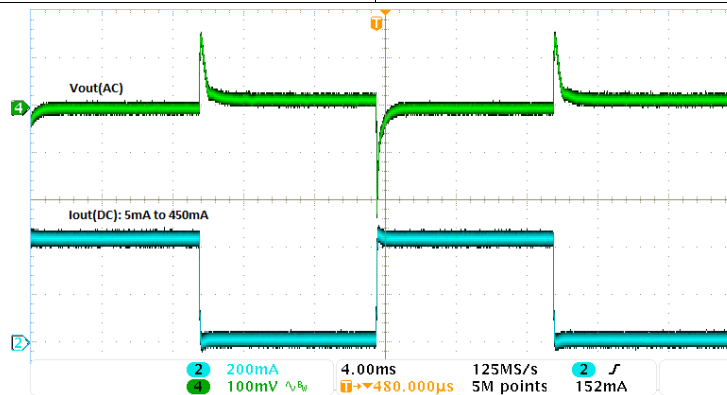


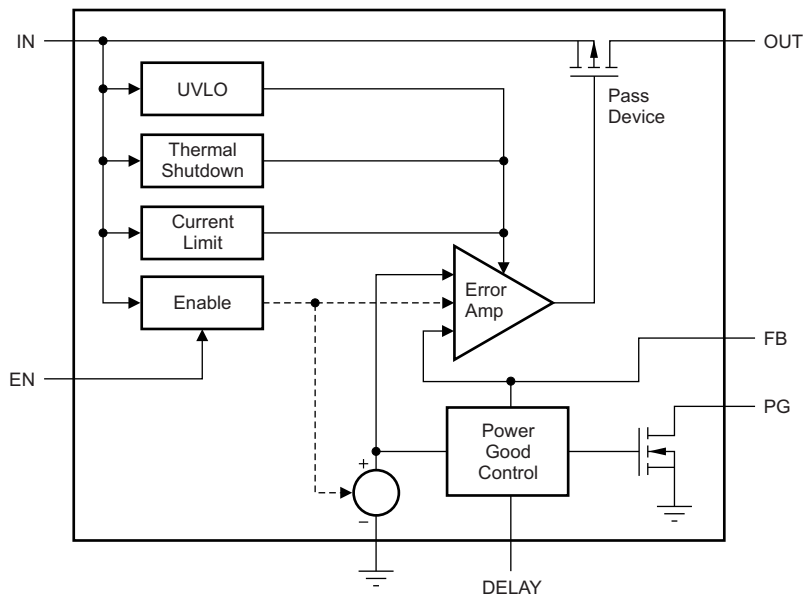
Figure 11. Load Transient
10-µF Ceramic Output Capacitor

7 Detailed Description

7.1 Overview

The TPS7A19 is a low-dropout linear regulator (LDO) combined with enable and power good functions. The power good pin initializes when the output voltage, V_{OUT} , exceeds $V_{T(PG)}$. The power good delay is a function of the value set by an external capacitor on the DELAY pin before releasing the PG pin high.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Enable Pin (EN)

The enable pin is a high-voltage-tolerant pin. A logic-high input on EN activates the device and turns on the LDO. For self-bias applications, connect this input to the IN pin.

7.3.2 Regulated Output Pin (OUT)

The OUT pin is the regulated output based on the required voltage. The output is protected by internal current limiting. During initial power up, the LDO has a soft start feature incorporated to control the initial current through the pass element.

In the event that the LDO drops out of regulation, the output tracks the input minus a voltage drop based on the load current. When the input voltage drops below the UVLO threshold, the LDO shuts down until the input voltage exceeds the minimum start-up level.

7.3.3 Power-Good Pin (PG)

The power good pin is an output with an external pullup resistor to the regulated supply. The output remains low until the regulated V_{OUT} exceeds approximately 91.6% of the set value, and the power good delay has expired. The regulated output falling below the 89.6% level asserts this output low after a short deglitch time of approximately 180 μ s (typical).

Feature Description (continued)

7.3.4 Delay Timer Pin (DELAY)

An external capacitor on the DELAY pin sets the timer delay before the PG pin is asserted high. The constant output current charges an external capacitor until the voltage exceeds a threshold that trips an internal comparator. If this pin is open, the default delay time is 325 μ s (typical).

The pulse delay time, t_{PG_DLY} , is defined with the charge time of an external capacitor DELAY, as shown in Equation 1.

$$t_{PG_DLY} = \left(\frac{C_{DELAY} \times 1\text{ V}}{9.5\ \mu\text{A}} \right) + 325\ \mu\text{s} \quad (1)$$

The PG pin initializes when V_{OUT} exceeds 91.6% of the programmed value. The delay is a function of the value set by an external capacitor on the DELAY pin before the PG pin is released high.

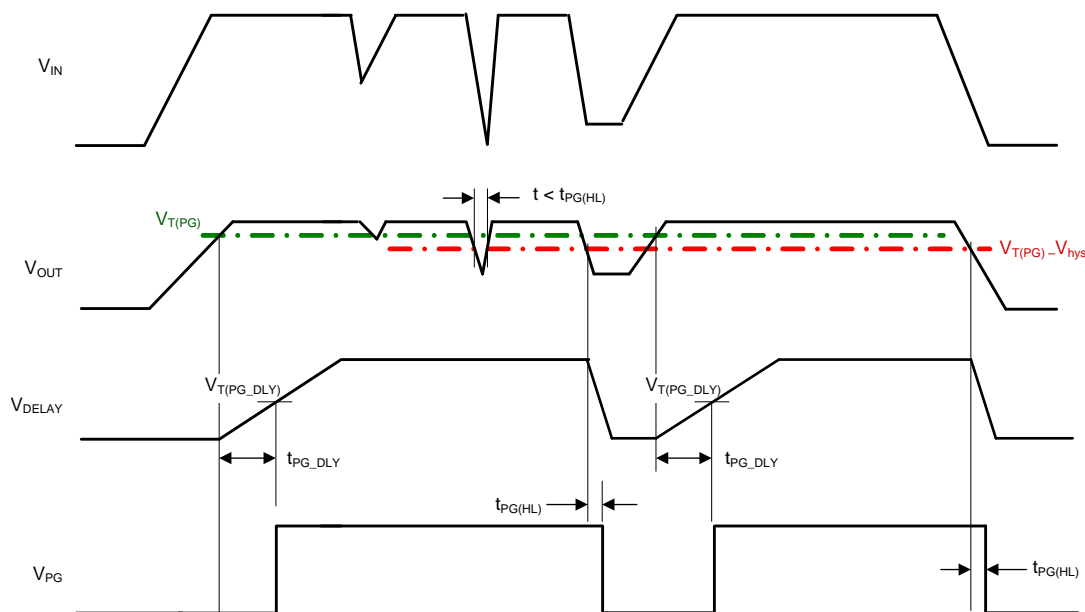


Figure 12. Conditions to Activate PG

7.3.5 Adjustable Output Voltage (ADJ for TPS7A1901)

An output voltage between 1.5 V and 18 V can be selected by using the external resistor dividers. Use Equation 2 to calculate the output voltage, where $V_{FB} = 1.233\text{ V}$. In order to avoid a large leakage current and to prevent a divider error, the value of $(R1 + R2)$ must be between 10 k Ω and 100 k Ω .

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2} \right) \quad (2)$$

7.3.6 Undervoltage Shutdown

The TPS7A19 family of devices has an internally-fixed, undervoltage-shutdown threshold. Undervoltage shutdown activates when the input voltage on V_{IN} drops below V_{IN_UVLO} . This activation makes sure that the regulator is not latched in an unknown state when there is a low-input supply voltage. If the input voltage has a negative transient that drops below the UVLO threshold and recovers, the regulator shuts down and powers up, similar to a typical power-up sequence when the input voltage exceeds the required levels.

Feature Description (continued)

7.3.7 Thermal Shutdown

The TPS7A19 incorporates a thermal shutdown (TSD) circuit as protection from overheating. For continuous standard operation, the junction temperature must not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output turns off. When the junction temperature falls below the TSD trip point minus the TSD hysteresis value, the output turns on again.

Thermal protection disables the output when the junction temperature rises to approximately 175°C, and allows the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the temperature of the regulator, and protects the device from damage as a result of overheating.

Although the internal protection circuitry of the TPS7A19 device is designed to protect against overload conditions, the circuitry is not intended to replace proper heat-sink methods. Continuously running the TPS7A19 device into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Operation With $V_{IN} < 4\text{ V}$

The devices operate with input voltages above 4 V. The devices do not operate at input voltages below the actual UVLO voltage.

7.4.2 Operation With EN Control

The enable rising edge threshold voltage is 1.7 V, maximum. When the EN pin is held above 1.7 V, and the input voltage is greater than the UVLO rising voltage, the device enables.

The enable falling edge is 0.4 V, minimum. When the EN pin is held below 0.4 V, the device is disabled. The quiescent current is reduced in this state.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Figure 13 shows a typical application circuit for the TPS7A1901. Based on the end-application, different values of external components can be used. Some applications may require a larger output capacitor during fast load steps in order to prevent a PG low from occurring. Use a low-ESR ceramic capacitor with a dielectric of type X5R or X7R for better load transient response.

8.2 Typical Application

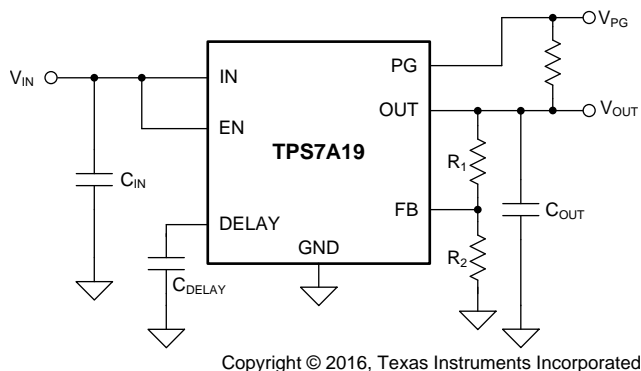


Figure 13. Adjustable Operation

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	12 V, $\pm 10\%$
Output voltage	3.3 V
Output current	50 mA (max)
PG delay time	1 ms

8.2.2 Detailed Design Procedure

To begin the design process:

1. First, make sure that the combination of maximum current, maximum ambient temperature, maximum input voltage, and minimum output voltage does not exceed the maximum operating condition of $T_J = 125^\circ\text{C}$. The [Power Dissipation and Thermal Considerations](#) section describes how to calculate the maximum ambient temperature and power dissipation.
2. Next, set the feedback resistors to give the desired output voltage. See [Equation 2](#) for the V_{OUT} relationship to R_1 and R_2 . A good nominal value for R_2 is 10 k Ω .
3. Then, calculate the required C_{DELAY} capacitor to achieve the desired PG delay time using [Equation 1](#). For 1 ms of delay, the nearest standard value capacitor is 10 nF.
4. Finally, select an output capacitor with a total effective capacitance between 22 μF and 500 μF , a sufficient voltage rating, and an ESR below 20 Ω . Higher capacitance gives improved transient response, but results in higher inrush current at startup.

8.2.2.1 Power Dissipation and Thermal Considerations

Device power dissipation is calculated with [Equation 3](#).

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + I_Q \times V_{IN}$$

where

- P_D = continuous power dissipation
- I_{OUT} = output current
- V_{IN} = input voltage
- V_{OUT} = output voltage

(3)

As $I_Q \ll I_{OUT}$, the term $I_Q \times V_{IN}$ in [Equation 3](#) can be ignored.

For a device under operation at a given ambient air temperature (T_A), calculate the junction temperature (T_J) with [Equation 4](#).

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where

- θ_{JA} = junction-to-ambient air thermal impedance

(4)

A rise in junction temperature because of power dissipation can be calculated with [Equation 5](#).

$$\Delta T = T_J - T_A = (\theta_{JA} \times P_D)$$

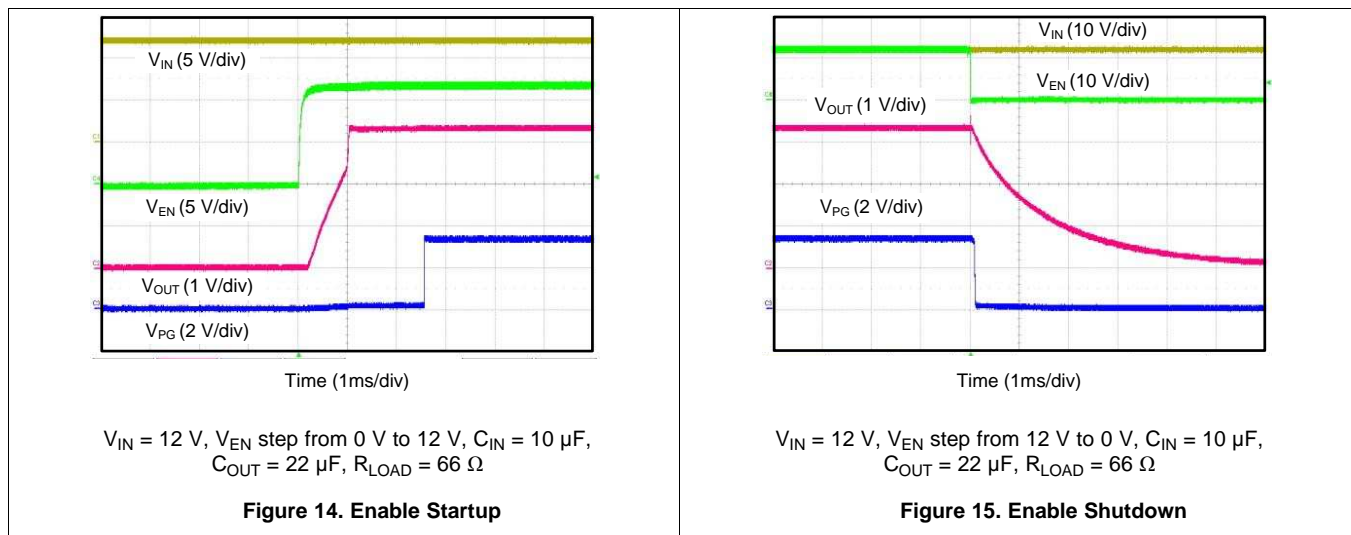
(5)

For a given maximum junction temperature (T_{JM}), the maximum ambient air temperature (T_{AM}) at which the device can operate is calculated with [Equation 6](#).

$$T_{AM} = T_{JM} - (\theta_{JA} \times P_D)$$

(6)

8.2.3 Application Curves



9 Power Supply Recommendations

The device operates from an input voltage supply range between 4 V and 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7A19 device, add an electrolytic capacitor with a value of 47 μ F and a ceramic bypass capacitor at the input.

10 Layout

10.1 Layout Guidelines

- To improve ac performance such as PSRR, output noise, and transient response, design the board with separate ground planes for V_{IN} and V_{OUT} , with each ground plane connected only at the GND pin of the device. In addition, connect the ground connection for the output capacitor directly to the GND pin of the device.
- Minimize equivalent series inductance (ESL) and equivalent series resistance (ESR) in order to maximize performance and stability. Place every capacitor as close to the device as possible, and on the same side of the PCB as the regulator.
- Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces are strongly discouraged because of the negative impact on system performance. Vias and long traces can also cause instability.
- If possible, and to maximize the performance listed in this data sheet, use the same layout pattern used for the TPS7A19 evaluation module, [TPS7A1901EVM-760](#) (SBVU031).

10.2 Layout Example

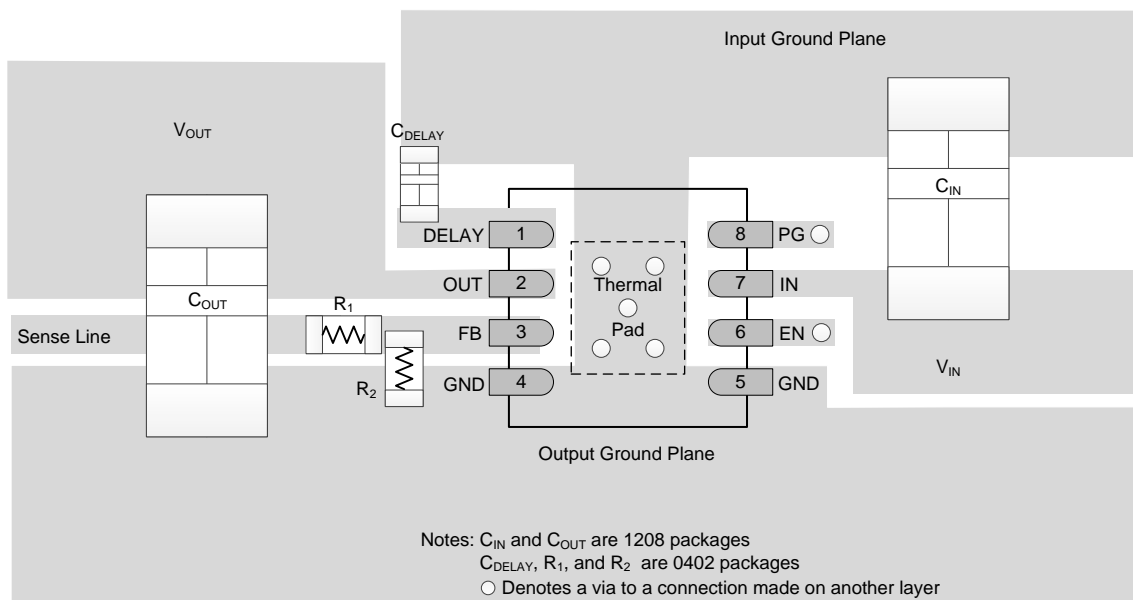


Figure 16. TPS7A19 Layout Example

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

11.1.1.1 評価モジュール

TPS7A19を使用する回路の性能の初期評価に役立てるため、評価モジュール(EVM)を利用可能です。この機器の概要情報を、表 2に示します。

表 2. 評価モジュール

名前	評価モジュール・フォルダ
TPS7A19 40V、450mA、高電圧、超低IQ、低ドロップアウト・レギュレータ評価モジュール	TPS7A1901EVM-760

11.1.1.2 SPICEモデル

SPICEを使用した回路性能のコンピュータによるシミュレーションは、アナログ回路やシステムの性能を分析するため多くの場合に有用です。TPS7A19用のSPICEモデルは、TPS7A19製品フォルダの「ツールとソフトウェア」タブから入手できます。

11.1.2 デバイスの項目表記

表 3. 製品情報⁽¹⁾

製品名	概要
TPS7A19XXYYYYZ	XXは公称出力電圧オプションで、01は可変を意味します。 YYYはパッケージ指定子です。 Zはパッケージ数量です。

(1) 最新のパッケージと発注情報については、このデータシートの末尾にあるパッケージ・オプションの付録を参照するか、www.ti.comにあるデバイスの製品フォルダをご覧ください。

11.2 ドキュメントのサポート

11.2.1 関連資料

『TPS7A1901EVM-760評価モジュール ユーザー・ガイド』(SBVU031)

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 商標

E2E is a trademark of Texas Instruments.
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11.6 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A1901DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A1901	Samples
TPS7A1901DRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A1901	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A1901DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS7A1901DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A1901DRBR	SON	DRB	8	3000	346.0	346.0	33.0
TPS7A1901DRBT	SON	DRB	8	250	210.0	185.0	35.0

DRB 8

GENERIC PACKAGE VIEW

VSON - 1 mm max height

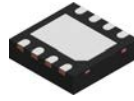
PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

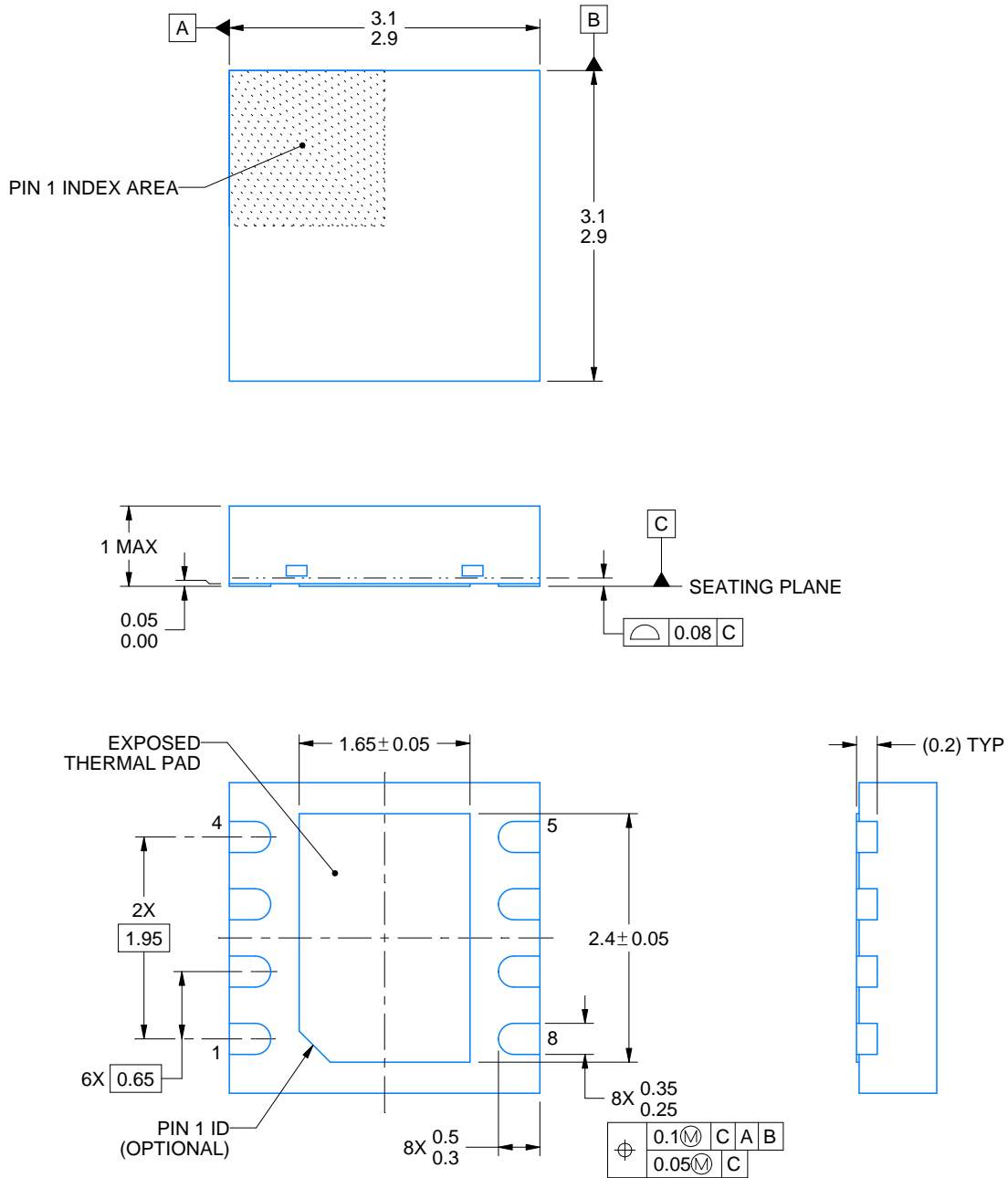
DRB0008B



PACKAGE OUTLINE

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4218876/A 12/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

DRB0008B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

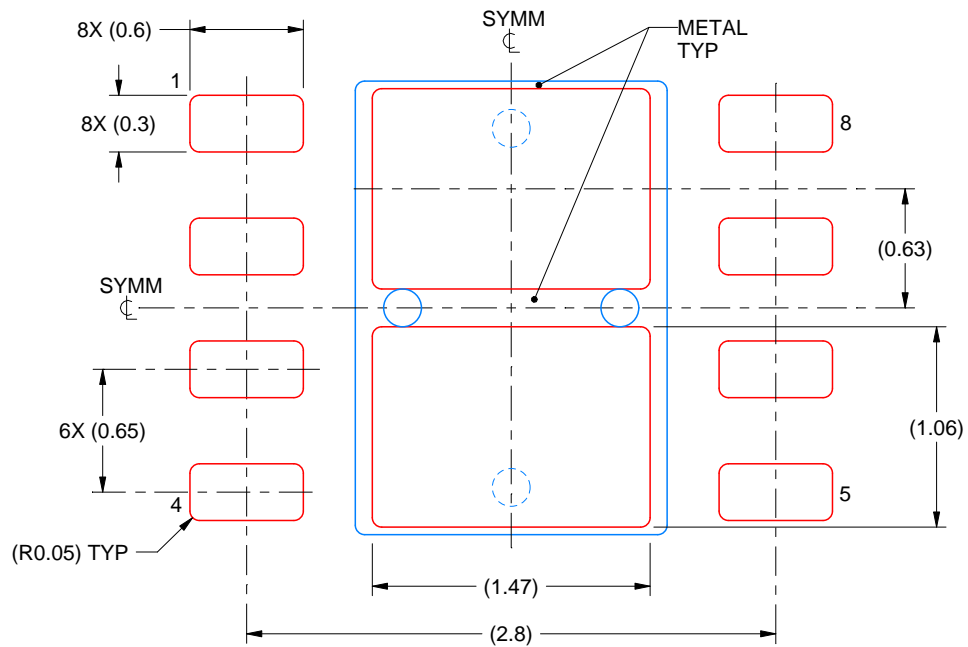
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRB0008B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218876/A 12/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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