TPS7A7001 超低電圧入力、超低ドロップアウト、イネーブル付き2A レギュレータ

1 特長

- 最低1.425Vの入力電圧
- 2Aにおいて最大380mVのドロップアウト
- 出力を0.5V以上で調整可能
- 電流制限およびサーマル・シャットダウン保護機能
- イネーブル・ピン
- シャットダウン・モードでの静止電流1μA
- 完全な産業用温度範囲
- RoHS完全準拠のSO-8パッケージで供給

2 アプリケーション

- テレコムおよびネットワーク・カード
- マザーボードおよび周辺機器カード
- 産業用
- ワイヤレス・インフラストラクチャ
- セットトップ·ボックス
- 医療用機器
- ノートブック・コンピュータ
- バッテリ駆動システム

3 概要

TPS7A7001は高性能の正電圧、低ドロップアウト(LDO)レギュレータで、非常に低い入力電圧と、最大2Aにおいて非常に低いドロップアウト電圧を必要とするアプリケーション用に設計されています。このデバイスは最低1.425Vの単一の入力電圧で動作し、出力電圧は最低0.5Vにプログラム可能です。出力電圧は外付けの分圧抵抗で設定可能です。

TPS7A7001はドロップアウトが非常に低く、V_{OUT}とV_{IN}とが非常に近いアプリケーションに理想的です。また、TPS7A7001にはイネーブル・ピンがあり、シャットダウン・モードではさらに消費電力を削減できます。TPS7A7001はライン、負荷、温度の変化に対しても非常に優れたレギュレーションを行います。

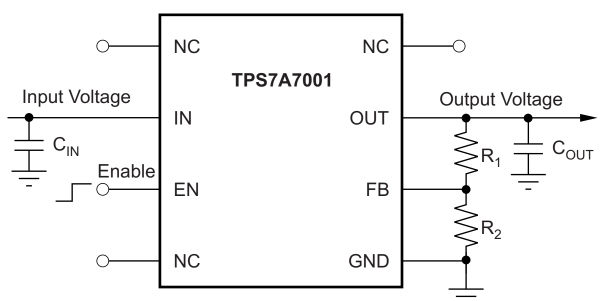
TPS7A7001は8ピンのSO PowerPAD™パッケージで供給されます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS7A7001	SO PowerPAD (8)	3.90mm×4.89mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。

代表的なアプリケーション



$$V_{OUT} = 0.5 \times \left(1 + \frac{R_1}{R_2}\right)$$

目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision E (August 2015) から Revision F に変更 | **Page**

- Changed "operating free-air" to "junction" in *Absolute Maximum Ratings* table condition line ... 5
- Changed OUT pin max voltage from 7 to V_{IN} + 0.3 V or 7 V, whichever is smaller, in *Absolute Maximum Ratings* table (moved OUT from first row to second row) ... 5
- Deleted T_A, ambient temperature range, from *Recommended Operating Conditions* table ... 5
- Changed C_{OUT} max value from 47 µF to 200 µF in *Recommended Operating Conditions* table ... 5
- Added note (2) to *Recommended Operating Conditions* table regarding C_{OUT} max value ... 5
- Added feedforward capacitance to *Recommended Operating Conditions* table ... 5
- Deleted redundant notes 2 to 7 in the *Thermal Information* table; all information from deleted notes available in application report shown in note (1) ... 5
- Changed note (1) in *Electrical Characteristics*; deleted initial reference to R_1 and updated R_2 resistor range ... 6
- Changed *Output Capacitor (OUT)* section; reworded for clarity ... 10

Revision D (September 2013) から Revision E に変更 | **Page**

- *「ESD定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加* ... 1

Revision C (January 2013) から Revision D に変更 | **Page**

- Added new text to *Internal Current Limit* section ... 8

Revision B (July 2012) から Revision C に変更 | **Page**

- Deleted maximum value for Output Current Limit parameter in *Electrical Characteristics* table ... 6

Revision A (June 2012) から **Revision B** に変更 **Page**

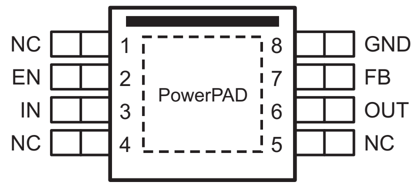
- Changed Output Voltage, I_{LIM} parameter test conditions in *Electrical Characteristics* table 6

2012年1月発行のものから更新 **Page**

- 「特長」の「*出力を調整可能*」の箇条書きを変更 1
- 「*概要*」セクションの最初の段落で、出力電圧の最低値を変更 1
- Changed *Electrical Characteristics* condition line.. 6
- Changed *Output Voltage Accuracy* parameter in *Electrical Characteristics* 6
- Changed test conditions for *Dropout Voltage* parameter in *Electrical Characteristics*.. 6
- Changed note (1) in *Electrical Characteristics* 6
- Added new note (4) to *Electrical Characteristics*... 6

5 Pin Configuration and Functions

DDA Package
8-Pin SO PowerPAD
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	2	I	Enable input. Pulling this pin below 0.5 V turns the regulator off. Connect to V_{IN} if not being used.
FB	7	I	This pin is the output voltage feedback input through voltage dividers. See the Table 2 for more details.
GND	8	–	Ground pin
IN	3	I	Unregulated supply voltage pin. It is recommended to connect an input capacitor to this pin.
NC	1, 4, 5	–	Not internally connected. The NC pins are not connected to any electrical node. It is recommended to connect the NC pins to large-area planes.
OUT	6	O	Regulated output pin. A 4.7-μF or larger capacitor of any type is required for stability.
PowerPAD			TI strongly recommends connecting the thermal pad to a large-area ground plane. If an electrically floating, dedicated thermal plane is available, the thermal pad can also be connected to it.

6 Specifications

6.1 Absolute Maximum Ratings

over junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	IN	–0.3	7	V
	EN, FB, OUT	–0.3	V_{IN} + 0.3 (2)	
Current	OUT		Internally limited	A
Temperature	Operating virtual junction, T_J	–55	150	°C
	Storage, T_{stg}	–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{IN} + 0.3 V or 7.0 V, whichever is smaller.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	1.425		6.5	V
V_{EN}	Enable pin voltage	0		V_{IN}	V
C_{IN}	Input capacitor	1		10	µF
C_{OUT}	Output capacitor (1) (2)	4.7	10	200	µF
C_{FB}	Feedforward capacitance	0		100	nF
I_{OUT}	Output current	0		2	A
T_J	Junction temperature	–40		125	°C

(1) See Figure 1 and Figure 2 for additional output capacitor ESR requirements.
(2) For output capacitors larger than 47 µF, a feedforward capacitor of at least 220 pF must be used.

6.4 Thermal Information

THERMAL METRIC (1)		TPS7A7001 DDA (SO PowerPAD) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

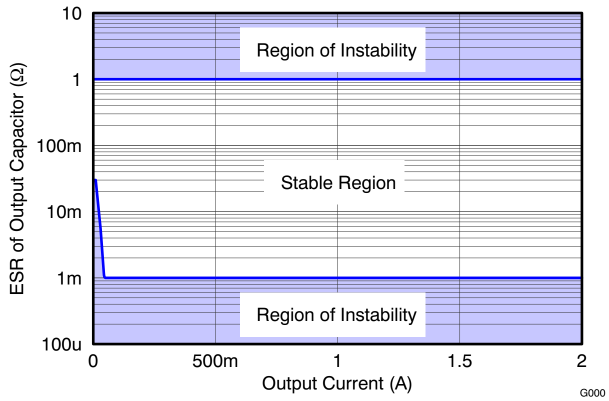
Over the full operating temperature range (see *Recommended Operating Conditions*), V_{EN} = 1.1 V, V_{FB} = V_{OUT} (1), 1.425 V ≤ V_{IN} ≤ 6.5 V, 10 µA ≤ I_{OUT} ≤ 2 A, C_{OUT} = 10 µF (unless otherwise noted). Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE						
I_{GND}	GND pin current (small)	V_{IN} = 3.3 V, 50-Ω load resistor between OUT and GND			3	mA
	GND pin current (shutdown)	V_{IN} = 6.5 V, V_{EN} = 0 V			5	µA
OUTPUT VOLTAGE						
V_{OUT}	Output voltage accuracy (2) (3)	V_{IN} = V_{OUT} + 0.5 V (4), I_{OUT} = 10 mA	–2%		2%	
		V_{IN} = 1.8 V, I_{OUT} = 0.8 A, 0°C ≤ T_J = T_A ≤ +85°C	–2%		2%	
		I_{OUT} = 10 mA	–3%		3%	
$\Delta V_{O(\Delta VI)}$	Line regulation	I_{OUT} = 10 mA		0.2	0.4	%/V
$\Delta V_{O(\Delta IO)}$	Load regulation (3)	10 mA ≤ I_{OUT} ≤ 2 A		0.25	0.75	%/A
V_{DO}	Dropout voltage (5)	I_{OUT} = 1.0 A, 0.5 V ≤ V_{OUT} ≤ 5.0 V			200	mV
		I_{OUT} = 1.5 A, 0.5 V ≤ V_{OUT} ≤ 5.0 V			300	
		I_{OUT} = 2.0 A, 0.5 V ≤ V_{OUT} ≤ 5.0 V			380	
I_{LIM}	Output current limit	V_{IN} = 1.425 V, V_{OUT} = 0.9 × $V_{OUT(NOM)}$	2.1			A
FEEDBACK						
V_{REF}	Reference voltage accuracy	V_{IN} = 3.3 V, V_{FB} = V_{OUT}, I_{OUT} = 10 mA	0.490	0.500	0.510	V
I_{FB}	FB pin current	V_{FB} = 0.5 V			1	µA
ENABLE						
I_{EN}	EN pin current	V_{EN} = 0 V, V_{IN} = 3.3 V			0.2	µA
VIL_{EN}	EN pin input low (disable)	V_{IN} = 3.3 V	0		0.5	V
VIH_{EN}	EN pin input high (enable)	V_{IN} = 3.3 V	1.1		V_{IN}	V
TEMPERATURE						
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		160		°C
		Reset, temperature decreasing		140		°C

(1) When setting V_{OUT} to a value other than 0.5 V, connect R_2 to the FB pin using 27-kΩ ≤ R_2 ≤ 33-kΩ resistors. See Functional Block Diagram for details of R_1 and R_2.
(2) Accuracy does not include error on feedback resistors R_1 and R_2.
(3) TPS7A7001 is not tested at V_{OUT} = 0.5 V, 2.3 V ≤ V_{IN} ≤ 6.5 V, and 500 mA ≤ I_{OUT} ≤ 2 A because the power dissipation is higher than the maximum rating of the package. Also, this accuracy specification does not apply to any application condition that exceeds the power dissipation limit of the package.
(4) V_{IN} = V_{OUT} + 0.5 V or 1.425 V, whichever is greater.
(5) V_{DO} = V_{IN} – V_{OUT} with V_{FB} = GND configuration.

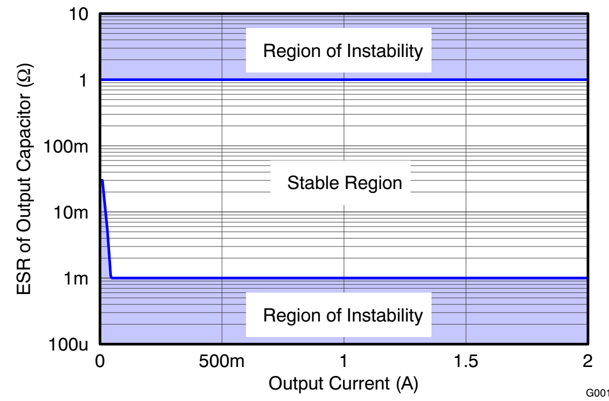
6.6 Typical Characteristics

for all fixed voltage versions and an adjustable version at T_J = 25°C, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{OUT} = 10 µF, and using the component values in Table 2 (unless otherwise noted)



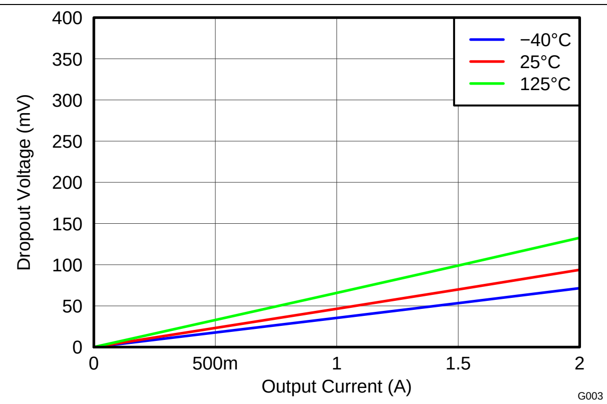
C_{OUT} = 10 µF

Figure 1. Stability Curve



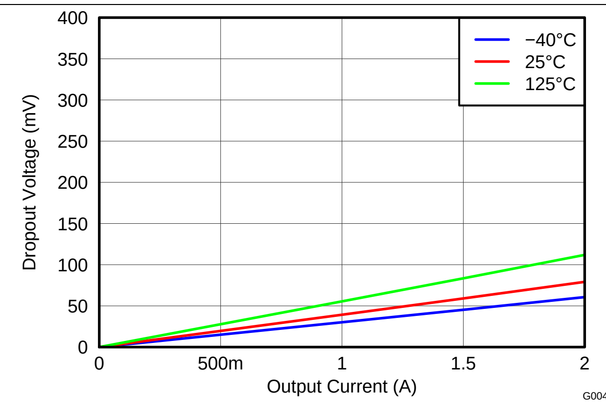
C_{OUT} = 100 µF

Figure 2. Stability Curve



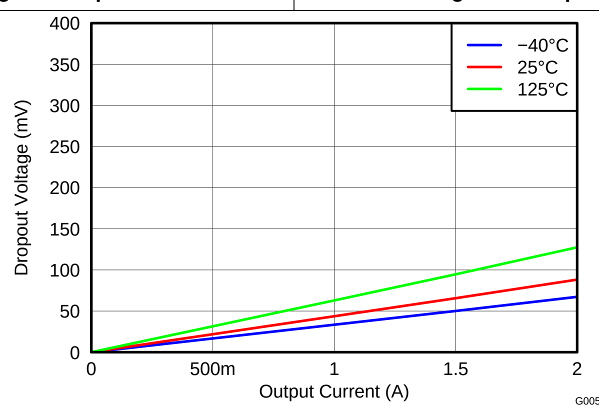
V_{OUT} = 3.3 V

Figure 3. Dropout Voltage vs Output Current



V_{OUT} = 1.6 V

Figure 4. Dropout Voltage vs Output Current



V_{OUT} = 1.4 V

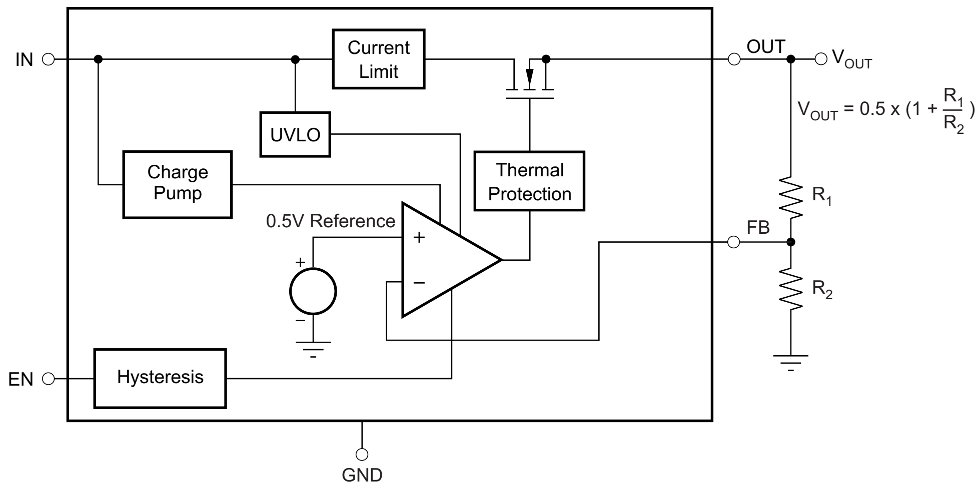
Figure 5. Dropout Voltage vs Output Current

7 Detailed Description

7.1 Overview

The TPS7A7001 offers a high current supply with very low dropout voltage. The TPS7A7001 is designed to minimize the required component count for a simple, small-size, and low-cost solution.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable (EN)

The enable pin (EN) is an active high logic input. When it is logic low, the device turns off and its consumption current is less than 1 µA. When it is logic high, the device turns on. The EN pin is required to be connected to a logic high or logic low level.

When the enable function is not required, connect EN to VIN.

7.3.2 Internal Current Limit

The TPS7A7001 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in a current limit state for extended periods of time.

Powering on the device with the enable pin, or increasing the input voltage above the minimum operating voltage while a low-impedance short exists on the output of the device, may result in a sequence of high-current pulses from the input to the output of the device. The energy consumed by the device is minimal during these events; therefore, there is no failure risk. Additional input capacitance helps to mitigate the load transient requirement of the upstream supply during these events.

7.4 Device Functional Modes

Table 1 provides a quick comparison between the normal, dropout, and disabled modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	EN	I_{OUT}	T_J
Normal	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$
Dropout	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$
Disabled	—	$V_{EN} < V_{EN(LO)}$	—	$T_J > T_{SD}$

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$).
- The enable voltage has previously exceeded the enable rising threshold voltage and not yet decreased below the enable falling threshold.
- The output current is less than the current limit ($I_{OUT} < I_{CL}$).
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$).

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output-voltage deviations.

8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input Capacitor (IN)

Although an input capacitor is not required for stability, it is recommended to connect a 1-µF to 10-µF low equivalent series resistance (ESR) capacitor across IN and GND near the device.

8.1.2 Output Capacitor (OUT)

The TPS7A7001 is stable with standard ceramic capacitors with capacitance values from 4.7 µF to 47 µF without a feedforward capacitor. For output capacitors from 47 µF to 200 µF, a feedforward capacitor of at least 220 pF must be used. The TPS7A7001 is evaluated using an X5R-type, 10-µF ceramic capacitor. X5R- and X7R-type capacitors are recommended because of minimal variation in value and ESR over temperature. Maximum ESR must be less than 1 Ω.

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude, but increases duration of the transient response.

8.1.3 Feedback Resistors (FB)

The voltage on the FB pin sets the output voltage and is determined by the values of R_1 and R_2. The values of R_1 and R_2 can be calculated for any voltage using the formula given in Equation 1:

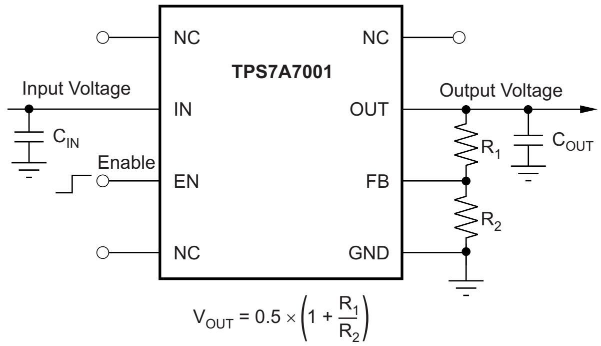
$$V_{OUT} = 0.5 \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

Table 2 shows the recommended resistor values for the best performance of the TPS7A7001. If the values in Table 2 are not used, keep the value of R2 between 27 kΩ and 33 kΩ. In Table 2, E96 series resistors are used. For the actual design, pay attention to any resistor error factors.

Table 2. Sample Resistor Values for Common Output Voltages

V_{OUT}	R_1	R_2
1.0 V	30.1 kΩ	30.1 kΩ
1.2 V	42.2 kΩ	30.1 kΩ
1.5 V	60.4 kΩ	30.1 kΩ
1.8 V	78.7 kΩ	30.1 kΩ
2.5 V	121 kΩ	30.1 kΩ
3.0 V	150 kΩ	30.1 kΩ
3.3 V	169 kΩ	30.1 kΩ
5.0 V	274 kΩ	30.1 kΩ

8.2 Typical Application



$$V_{OUT} = 0.5 \times \left(1 + \frac{R_1}{R_2}\right)$$

Figure 6. Typical Application

8.2.1 Design Requirements

Table 3 lists the design parameters.

Table 3. Design Parameters

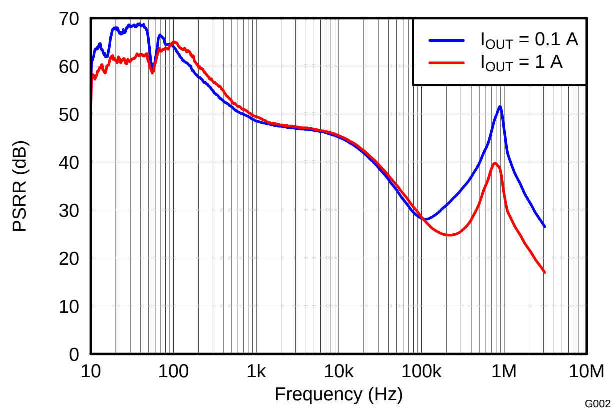
PARAMETER	DESIGN REQUIREMENT
Input voltage	3.3 V
Output voltage	2.5 V
Maximum output current	1.2 A

8.2.2 Detailed Design Procedure

Select the desired device based on the output voltage.

Provide an input supply with adequate headroom to account for dropout and output current to account for the GND terminal current, and power the load.

8.2.3 Application Curve



V_{IN} = 5.0 V, V_{OUT} = 3.3 V

Figure 7. Power-Supply Ripple Rejection vs Frequency

9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range between 1.425 V and 6.5 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply is well regulated and stable. If the input supply is noisy, additional input capacitors with low ESR help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendation to Improve PSRR and Noise Performance

To improve ac measurements like PSRR, output noise, and transient response, use the board design shown in the layout example of Figure 8.

10.2 Layout Example

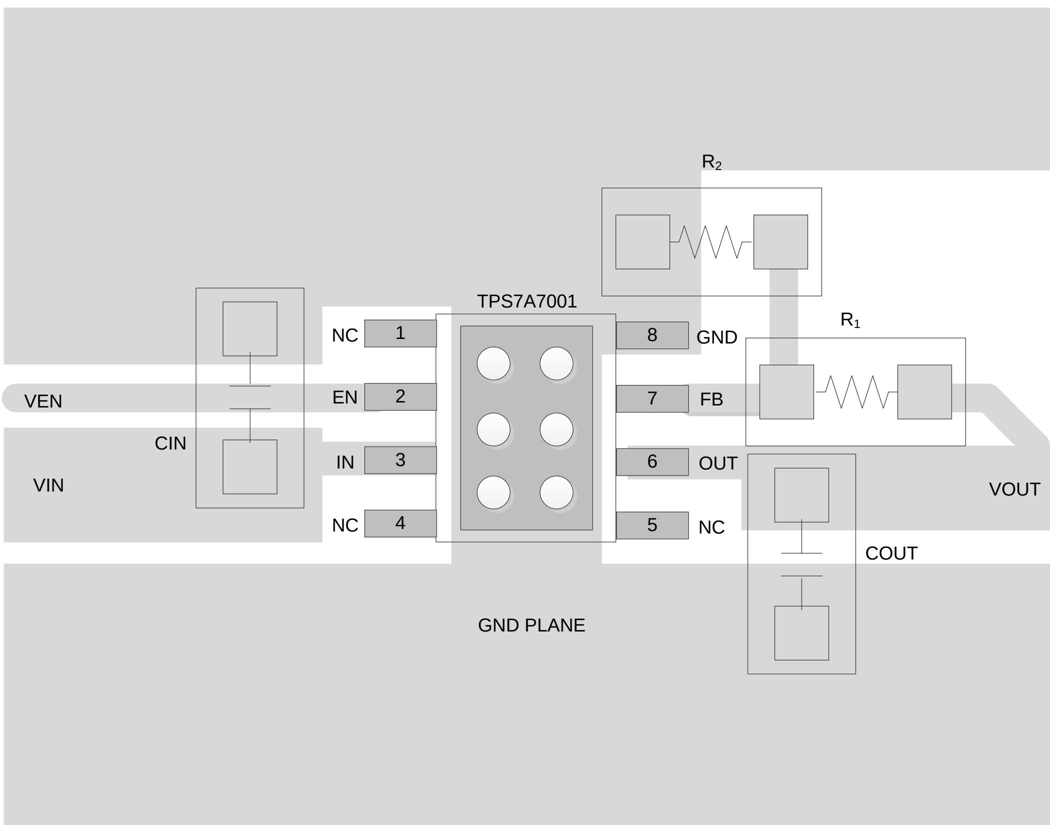


Figure 8. Layout Example

10.3 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is re-enabled.

The internal protection circuitry of the TPS7A7001 is designed to protect against overload conditions. The protection circuitry is not intended to replace proper heat sinking. Continuously running the TPS7A7001 into thermal shutdown degrades device reliability.

10.4 Power Dissipation

Power dissipation (P_D) of the device depends on the input voltage and load conditions and is calculated using Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

In order to minimize power dissipation and achieve greater efficiency, use the lowest possible input voltage necessary to achieve the required output voltage regulation

On the SO (DDA) package, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or left floating; however, attach the pad to an appropriate amount of copper PCB area to prevent the device from overheating. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device, and is calculated using Equation 3:

$$R_{\theta JA} = \left(\frac{+125°C - T_A}{P_D} \right) \quad (3)$$

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 デバイスの項目表記

製品名 (1)	説明
TPS7A7001**yyyz**	YYYはパッケージ指定子です。 Zはパッケージ数量です。

(1) 最新のパッケージおよび注文情報については、このドキュメントの最後にあるパッケージ・オプションの付録を参照するか、www.ti.comのデバイス製品フォルダをご覧ください。

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- *『TI LDOの局所的インデックス』アプリケーション・ノート*
- *『半導体およびICパッケージの熱指標』*

11.3 ドキュメントの更新通知を受け取る方法

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11.6 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A7001DDA	ACTIVE	SO PowerPAD	DDA	8	75	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QVH	Samples
TPS7A7001DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QVH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

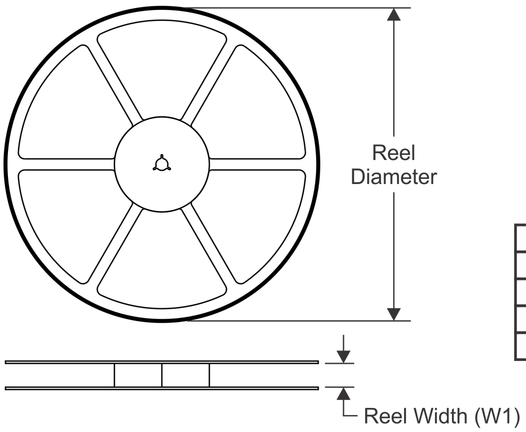
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

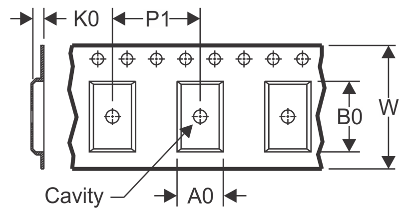
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

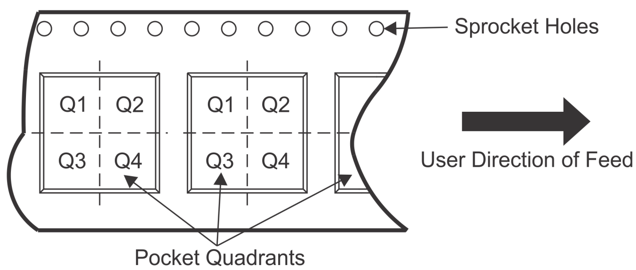


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

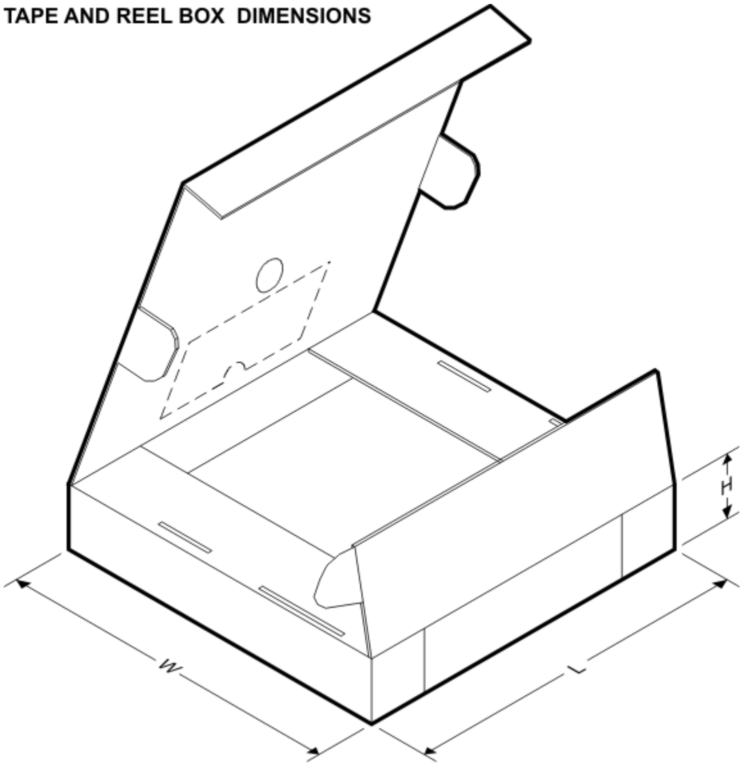
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A7001DDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

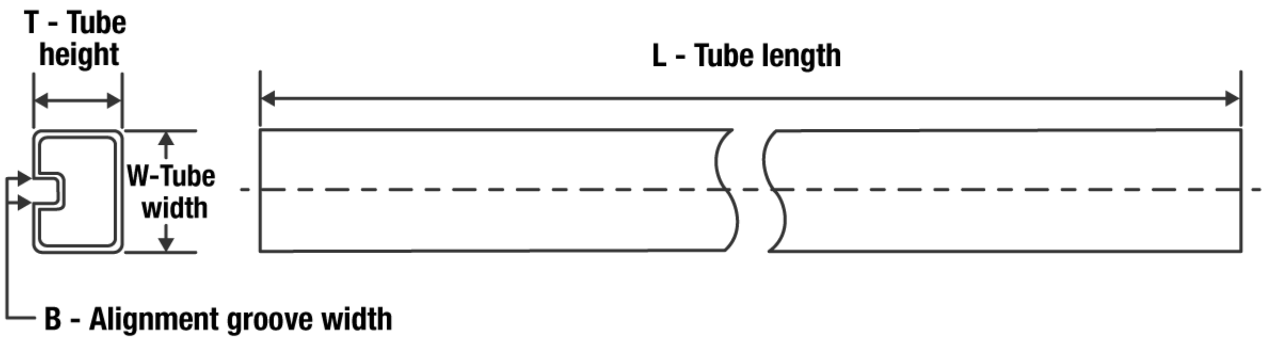
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A7001DDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

TUBE

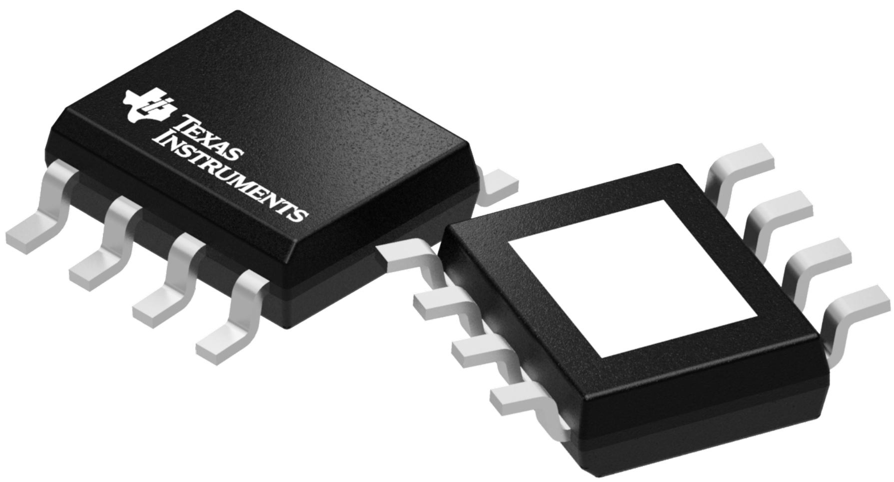


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS7A7001DDA	DDA	HSOIC	8	75	517	7.87	635	4.25

DDA 8 PowerPAD™ SOIC - 1.7 mm max height

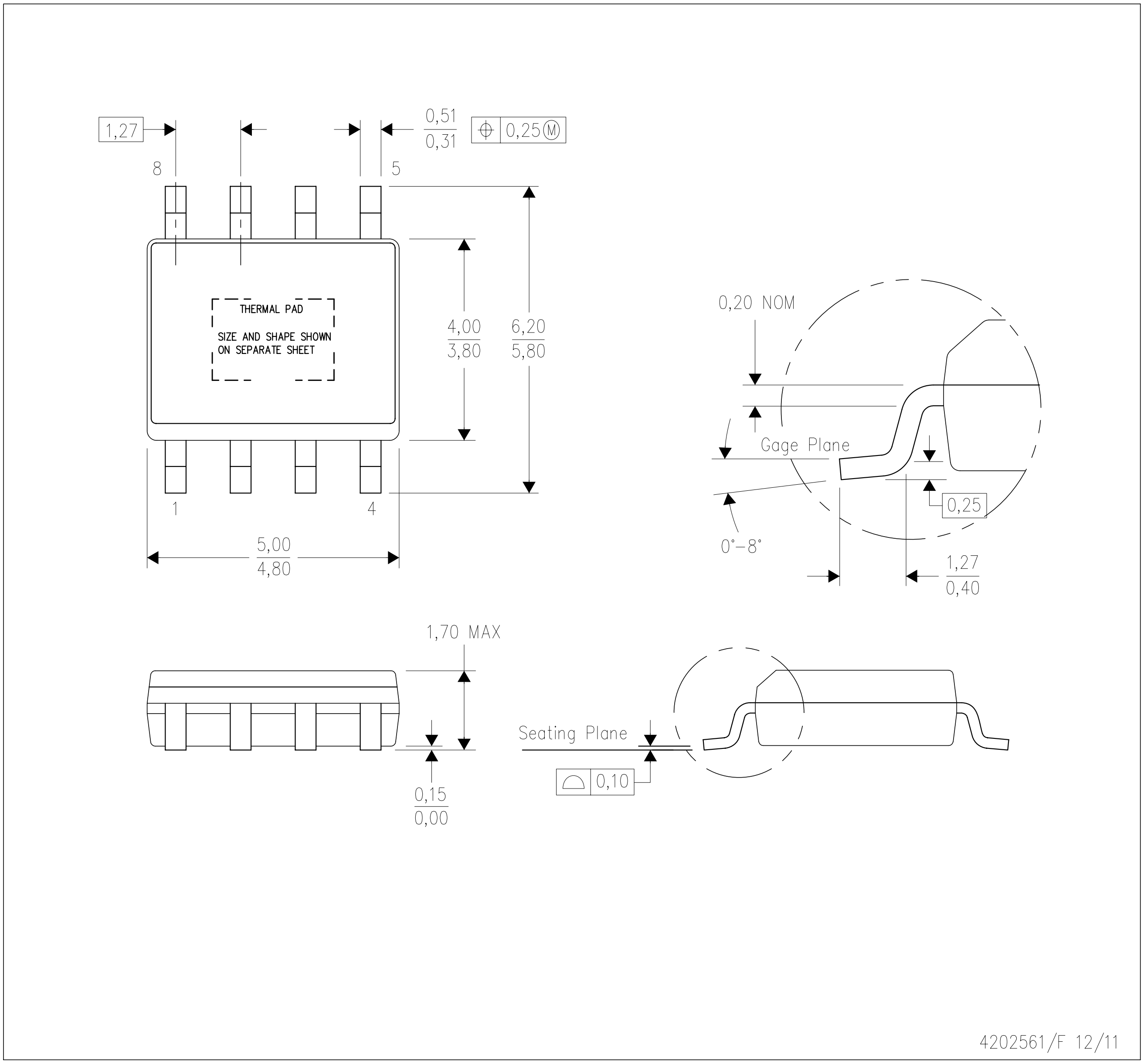
PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4202561/G

DDA (R-PDSO-G8) PowerPAD™ PLASTIC SMALL-OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

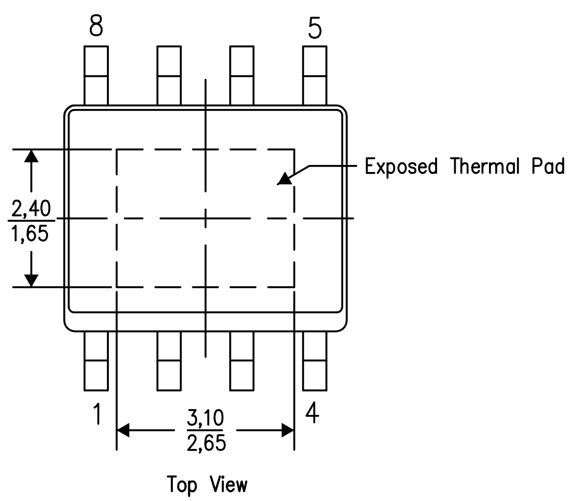
DDA (R-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

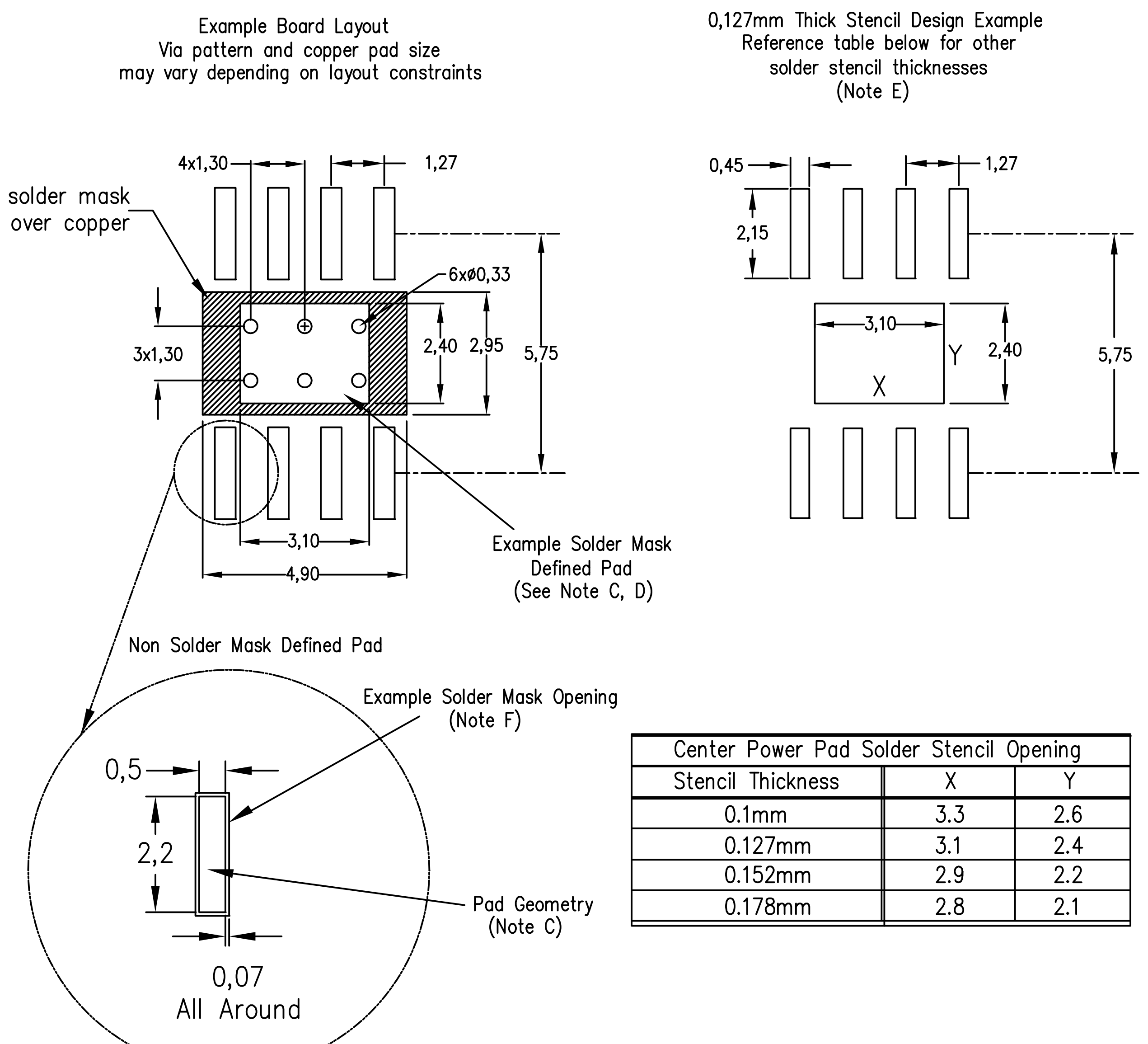


Exposed Thermal Pad Dimensions

4206322-6/L 05/12

NOTE: A. All linear dimensions are in millimeters

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

4208951-6/D 04/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要なお知らせと免責事項

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