TEXAS INSTRUMENTS
TPS7B85-Q1
JAJSIN6A – FEBRUARY 2020 – REVISED NOVEMBER 2020

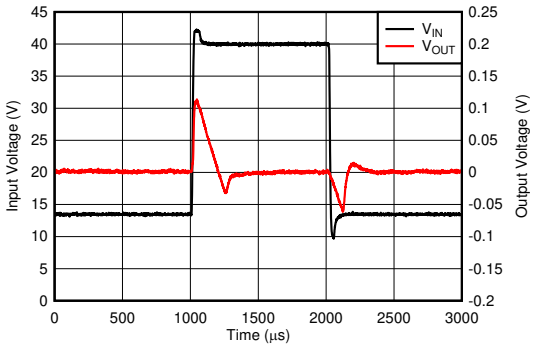
TPS7B85-Q1 150mA、40V、低ドロップアウト・レギュレータ パワー・グッドおよび内蔵電圧監視機能搭載

1 特長

- 車載アプリケーション用に AEC-Q100 認定取得済み
  - 温度グレード 1:-40℃～+125℃、T_A
  - 接合部温度:–40℃～+150℃、T_J
- 入力電圧範囲:3V～40V (最大 42V)
- 出力電圧範囲:3.3V および 5V (固定)
- 出力電流:最大 150mA
- 出力電圧精度:±0.75% (最大値)
- 低いドロップアウト電圧:
  - 150mA で 225mV 以下 (V_{OUT} ≥ 3.3V)
- 低い静止電流:
  - 18µA (標準値)
  - ディセーブル時:4µA 以下
- 優れたライン過渡応答:
  - V_{OUT} の ±2% の偏差 (コールド・クランク時)
  - V_{OUT} の ±2% の偏差 (1V/µs の V_{IN} スルーレート)
- 電圧検出機能を内蔵
- 調整可能なスレッショルドとプログラム可能な遅延時間を備えたパワー・グッド
- 2.2µF 以上のコンデンサで安定
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- パッケージ:サーマル・パッド付きの 10 ピン VSON
  - 低い熱抵抗 ($R_{\theta JA}$):50.3°C/W

2 アプリケーション

- 再構成可能インストルメント・クラスタ
- 車体制御モジュール (BCM)
- 常時オンのバッテリ接続アプリケーション:
  - 車載ゲートウェイ
  - リモート・キーレス・エントリ (RKE)



ライン過渡応答 (3V/µs の V_{IN} スルーレート)

3 概要

TPS7B85-Q1 は、車載用アプリケーションのバッテリに接続するように設計された低ドロップアウト・リニア・レギュレータです。このデバイスの入力電圧範囲は 40V まで拡張されているため、車載用システムで予測される過渡事象 (負荷ダンプなど) にも耐えられます。このデバイスは静止電流がわずか 18µA であることから、スタンバイ・システムのマイクロコントローラや CAN (コントローラ・エリア・ネットワーク) トランシーバなどの常時オンのコンポーネントへの電力供給に最適なソリューションです。

このデバイスは、負荷やラインの変動 (例:コールド・クランク条件時) に出力が素早く応答できる最先端の過渡応答性能を備えています。またこのデバイスは、ドロップアウトからの回復時に出力オーバーシュートを最小限に抑える革新的なアーキテクチャを採用しています。通常動作時は、ライン、負荷、温度の全範囲にわたって誤差 ±0.75% 以下の高い DC 精度を維持します。

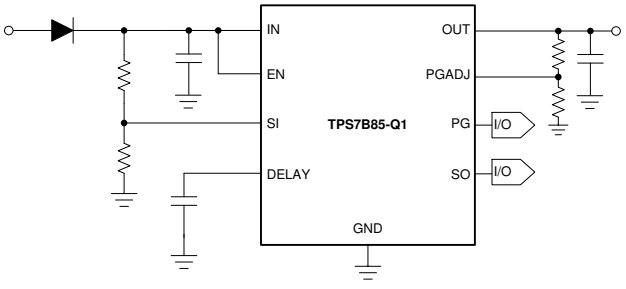
TPS7B85-Q1 はパワー・グッドおよび電圧監視機能を内蔵しています。パワー・グッドの遅延時間と電圧スレッショルドは、外付け部品で調整できます。内蔵電圧検出器を使用して入力電圧を監視し、バッテリ電圧が低下し始めた際に下流の部品 (MCU など) にアラートを発行できます。

このデバイスは、小型 PCB (プリント基板) 設計に適した小型の VSON パッケージで供給されます。熱抵抗が低いため、デバイス全体で大きな発熱があっても持続して動作できます。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
TPS7B85-Q1	VSON (10)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (February 2020) to Revision A (November 2020)	Page
• ドキュメントのステータスを事前情報から量産データに変更	1

5 Pin Configuration and Functions

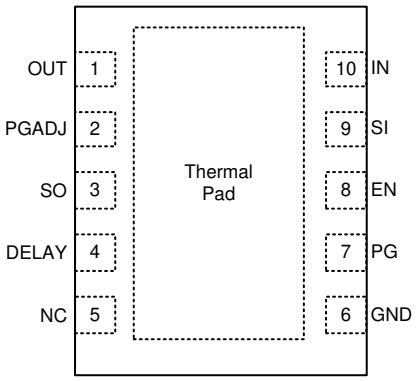


図 5-1. DRC Package, 10-Pin VSON, Top View

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	DRC		
DELAY	4	O	Power-good delay adjustment pin. Connect a capacitor from this pin to GND to set the PG reset delay. Leave this pin floating for a default ($t_{(DLY\_FIX)}$) delay. See the *Power-Good* section for more information. If this functionality is not desired, leave this pin floating because connecting this pin to GND causes a perminant increase in the GND current.
EN	8	I	Enable pin. The device is disabled when the enable pin becomes lower than the enable logic input low level (V_{IL}). To ensure the device is enabled, the EN pin must be driven above the logic high level (V_{IH}). This pin should not be left floating as this pin is high impedance if it is left floating the part may enable or disable.
GND	6	G	Ground pin. Connect this pin to the thermal pad with a low-impedance connection.
NC	5	—	No internal connection. Connect this pin to GND for the best thermal resistance.
PGADJ	2	I	Power-good threshold-adjustment pin. Connect a resistor divider between the PGADJ and OUT pins to set the power-good threshold. Connect this pin to ground to set the threshold to $V_{PG(TH,FALLING)}$. See *Power-Good* for more information.
PG	7	O	Power-good pin. This pin has an internal pullup resistor. Do not connect this pin to V_{OUT} or any other biased voltage rail. V_{PG} is logic level high when V_{OUT} is above the power-good threshold. See *Power-Good* for more information.
SI	9	I	Sense input pin. Connect via an external voltage divider to the supply voltage to be monitored.
SO	3	O	Sense output pin. This pin has an internal pullup resistor. Do not connect this pin to V_{OUT} or any other biased voltage rail. V_{SO} is logic level low when V_{SI} falls below the sense-low threshold.
IN	10	P	Input power-supply voltage pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground as listed in the *Recommended Operating Conditions* table and the *Input Capacitor* section. Place the input capacitor as close to the input of the device as possible.
OUT	1	O	Regulated output voltage pin. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to ground; see the *Recommended Operating Conditions* table and the *Output Capacitor* section. Place the output capacitor as close to the output of the device as possible. If using a high ESR capacitor, decouple the output with a 100-nF ceramic capacitor.
Thermal pad		—	Thermal pad. Connect the pad to GND for the best possible thermal performance. See the *Layout* section for more information.

(1) I = input; O = output; P = power; G = ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
IN	Unregulated input	–0.3	42	V
EN	Enable input	–0.3	42	V
OUT	Regulated output	–0.3	V_{IN} + 0.3(2)	V
FB	Feedback	–0.3	20	V
SI	Sense input	–0.3	42	V
Delay	Reset delay input	–0.3	6	V
SO, PG, PGADJ	Sense output, power-good, power-good adjustable threshold	–0.3	20	V
T_A	Operating ambient temperature	–40	125	°C
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* isnot implied. Exposure to absolute-maximum-rated conditions for extended periods may affect devicereliability.
(2) The absolute maximum rating is V_{IN} + 0.3 V or 20 V, whichever is smaller.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordancewith the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	3		40	V
V_{OUT}	Output voltage	1.2		18	V
I_{OUT}	Output current	0		150	mA
V_{EN}, V_{SI}	High voltage (I/O)	0		40	V
V_{Delay}	Delay pin voltage	0		5.5	V
V_{PG}, V_{SO}, V_{PGADJ}	Low voltage (I/O), power-good adjustable threshold	0		18	V
C_{OUT}	Output capacitor(2)	2.2		220	µF
ESR	Output capacitor ESR requirements(3)	0.001		2	Ω
C_{IN}	Input capacitor(1)	0.1	1		µF
C_{Delay}	Power-good delay capacitor	0		1	uF
T_J	Operating junction temperature	–40		150	°C

(1) For robust EMI performance the minimum input capacitance is 500 nF.
(2) Effective output capacitance of 1 µF minimum required for stability.
(3) If using a large ESR capacitor it is recommended to decouple this with a 100-nF ceramic capacitor to improve transient performance.

6.4 Thermal Information

THERMAL METRIC(1) (2)		TPS7B85-Q1 DRC (VSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(3)	50.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.5	°C/W

(1) The thermal data is based on the JEDEC standard high K profile,JESD 51-7. Two-signal, two-plane, four-layer board with 2-oz. copper. The copper pad is soldered tothe thermal land pattern. Also, correct attachment procedure must be incorporated.
(2) For more information about traditional and new thermal metrics,see the Semiconductor and IC PackageThermal Metrics application report.
(3) The 1s0p $R_{\theta JA}$ is 202.5℃/W for the DRC package.

6.5 Electrical Characteristics

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 0 mA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF, and V_{EN} = 2 V (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OUT}	Regulated output accuracy	V_{IN} = V_{OUT} + 500 mV to 40 V, I_{OUT} = 100 µA to 150 mA (1)	T_J = 25ºC	–0.5		0.5	%
			T_J = –40°C to +150ºC	–0.75		0.75	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	Change in percent of output voltage	V_{IN} = V_{OUT} + 500 mV to 40 V, I_{OUT} = 100 µA			0.2	%
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	Change in percent of output voltage	V_{IN} = V_{OUT} + 500 mV, I_{OUT} = 100 µA to 150 mA			0.2	
ΔV_{OUT}	Load transient response settling time(2) (3)	C_{OUT} = 10 µF	C_{OUT} = 10 µF			100	µs
	Load transient response overshoot, undershoot(3)		I_{OUT} = 45 mA to 105 mA	–2%		10%	%V_{OUT}
			I_{OUT} = 0 mA to 150 mA	–10%			
I_Q	Quiescent current	V_{IN} = V_{OUT} + 500 mV to 40 V, I_{OUT} = 0 mA	T_J = 25ºC		18	21	µA
			T_J = –40°C to +150ºC			26	
		I_{OUT} = 500 µA	T_J = –40°C to +150ºC			35	
$I_{SHUTDOWN}$	Shutdown supply current (I_{GND})	V_{EN} = 0 V	T_J = 25ºC			2.5	µA
			T_J = –40°C to +150ºC			4	
V_{DO}	Dropout voltage	I_{OUT} ≤ 1 mA, V_{OUT} ≥ 3.3 V, V_{IN} = $V_{OUT(NOM)}$ x 0.95				43	mV
		I_{OUT} = 105 mA, V_{OUT} ≥ 3.3 V, V_{IN} = $V_{OUT(NOM)}$			125	175	
		I_{OUT} = 150 mA, V_{OUT} ≥ 3.3 V, V_{IN} = $V_{OUT(NOM)}$			155	225	
$V_{UVLO(RISING)}$	Rising input supply UVLO	V_{IN} rising		2.6	2.7	2.82	V
$V_{UVLO(FALLING)}$	Falling input supply UVLO	V_{IN} falling		2.38	2.5	2.6	V
$V_{UVLO(HYST)}$	V_{UVLO} hysteresis				230		mV
V_{IL}	Enable logic input low level					0.7	V
V_{IH}	Enable logic input high level			2			V
I_{EN}	EN pin current	V_{EN} = V_{IN} = 13.5 V				50	nA

6.5 Electrical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 0 mA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF, and V_{EN} = 2 V (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CL}	Output current limit	V_{IN} = $V_{OUT(nom)}$ + 1 V, V_{OUT} short to 90% x $V_{OUT(NOM)}$	180	220	260	mA
PSRR	Power-supply ripple rejection	V_{IN} - V_{OUT} = 500 mV, frequency = 1 kHz, I_{OUT} = 150 mA		55		dB
V_n	Output noise voltage	V_{OUT} = 3.3 V, BW = 10 Hz to 100 kHz		280		μV_{RMS}
$V_{SI(HIGH)}$	Sense input threshold high	V_{SI} rising	1.17	1.21	1.25	V
$V_{SI(LOW)}$	Sense input threshold low	V_{SI} falling	1.07	1.12	1.15	V
$V_{SI(HYST)}$	Sense input switching hysteresis			90		mV
I_{SI}	Sense input current	V_{SI} = 40 V		0.015	1.5	µA
R_{SO}	Sense output internal pullup resistor		10	30	50	kΩ
$V_{SO(OL)}$	Sense output low voltage	V_{SI} ≤ 1.07 V, V_{IN} ≥ 3 V			0.4	V
R_{PG}	Power-good internal pullup resistor		10	30	50	kΩ
$V_{PG(OL)}$	PG pin low level output voltage	V_{OUT} ≤ 0.83 x V_{OUT}			0.4	V
$V_{PG(TH,RISING)}$	Default power-good threshold	V_{OUT} rising, PGADJpin shorted to ground	85		95	$\%V_{OUT}$
$V_{PG(TH,FALLING)}$		V_{OUT} falling, PGADJ pin shorted to ground	83		93	
$V_{PG(HYST)}$	Power-good hysteresis			2.5		$\%V_{OUT}$
$V_{PGADJ (TH,FALLING)}$	Switching voltage for the power-good adjust pin	V_{OUT} falling, PGADJ falling	0.97	1	1.030	V
$V_{PGADJ(HYST)}$	PGADJ hysteresis		5	35	50	mV
$V_{DLY(TH)}$	Threshold to release power-good high	Voltage at delay pin rising	1.17	1.21	1.25	V
$I_{DLY(CHARGE)}$	Delay capacitor charging current	V_{DLY} = 1 V	1	1.5	2	µA
$T_{SD(SHUTDOWN)}$	Junction shutdown temperature			175		°C
$T_{SD(HYST)}$	Hysteresis of thermal shutdown			20		°C

(1) Power dissipation is limited to 2W for IC production testing purposes. The power dissipation can be higher during normal operation. Please see the thermal dissipation section for more information on how much power the device can dissipate while maintaining a junction temperature below 150°C.
(2) The settling time is measured from when I_{OUT} is stepped from 45mA to 105 mA to when the output voltage recovers to V_{OUT} = $V_{OUT(nom)}$ - 5 mV.
(3) This specification is specified by design.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TIMING FOR SENSE INPUT AND OUTPUT (SI, SO)						
$t_{(PD\_SO\_HL)}$	Sense high reaction time			25		µs
$t_{(PD\_SO\_LH)}$	Sense low reaction time			30		µs
TIMING POWER-GOOD						
$t_{(DLY\_FIX)}$	Power-good propagation delay	No capacitor connected at DELAY pin		100		µs
$t_{(Deglitch)}$	Power-good deglitch time	No capacitor connected at DELAY pin		90		µs
$t_{(DLY)}$	Power-good propagation delay	Delay capacitor value: $C_{(DELAY)}$ = 100 nF		80		ms

6.7 Typical Characteristics

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 100 µA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF, and V_{EN} = 2 V (unless otherwise noted)

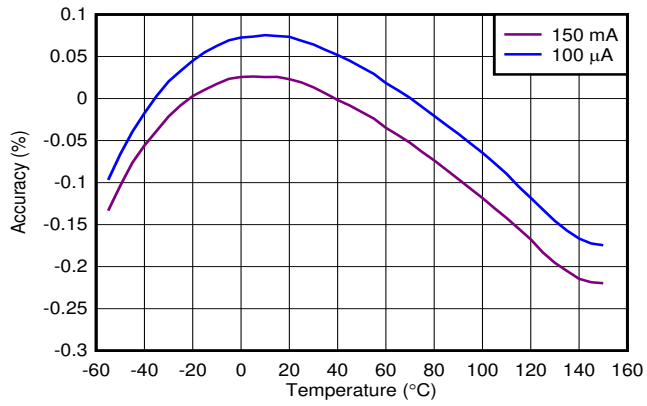
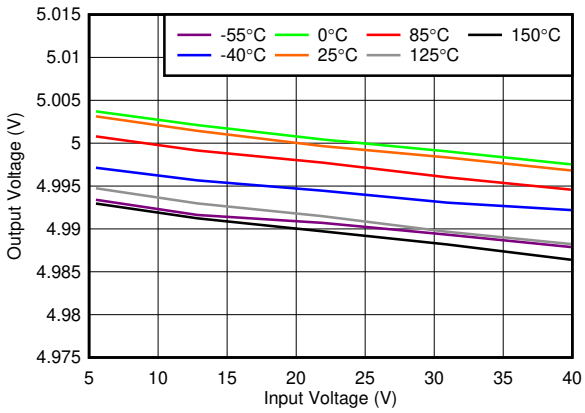
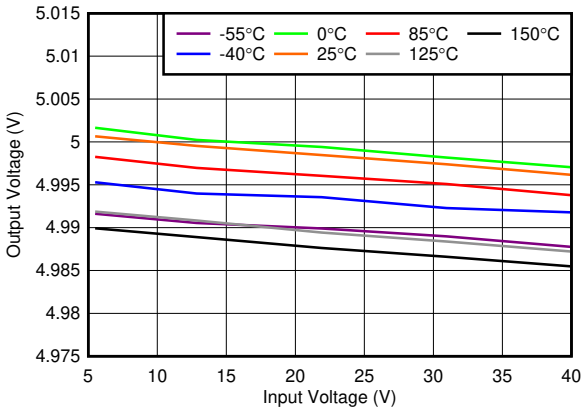


図 6-1. Accuracy vs Temperature



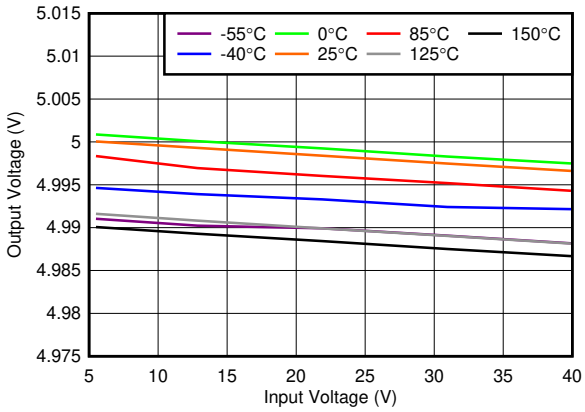
V_{OUT} = 5 V, I_{OUT} = 150 mA

図 6-2. Line Regulation vs V_{IN}



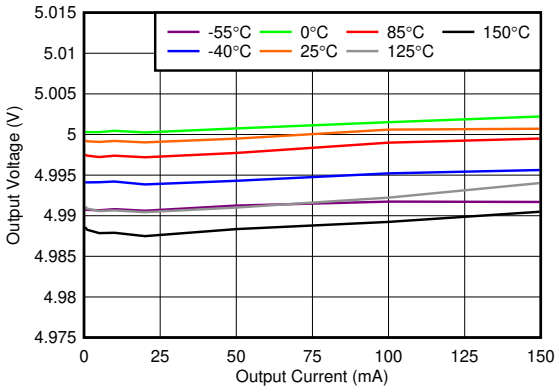
V_{OUT} = 5 V, I_{OUT} = 5 mA

図 6-3. Line Regulation vs V_{IN}



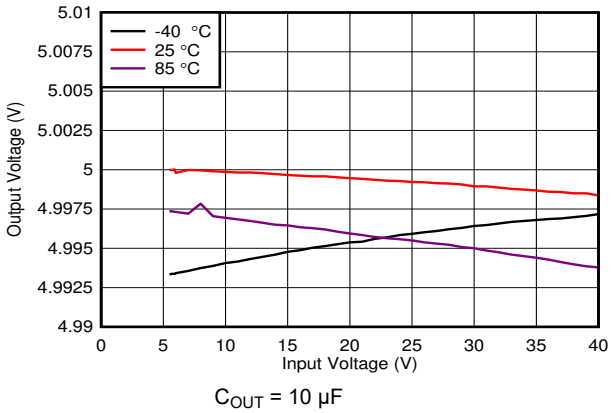
V_{OUT} = 5 V, I_{OUT} = 1 mA

図 6-4. Line Regulation vs V_{IN}



V_{OUT} = 5 V

図 6-5. Load Regulation vs I_{OUT}

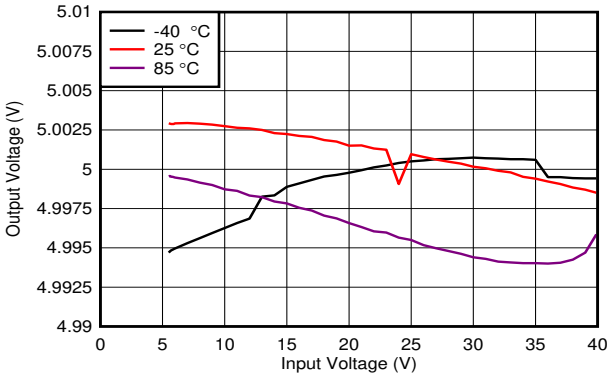


C_{OUT} = 10 µF

図 6-6. Line Regulation at 50 mA

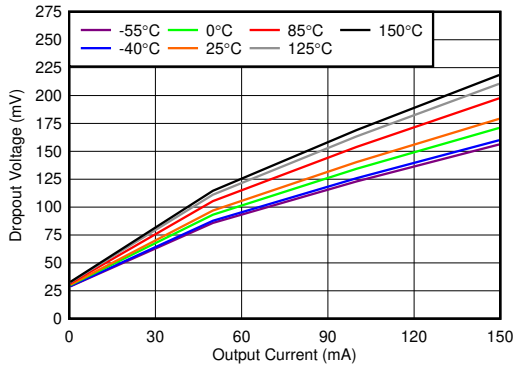
6.7 Typical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 100 µA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF, and V_{EN} = 2 V (unless otherwise noted)



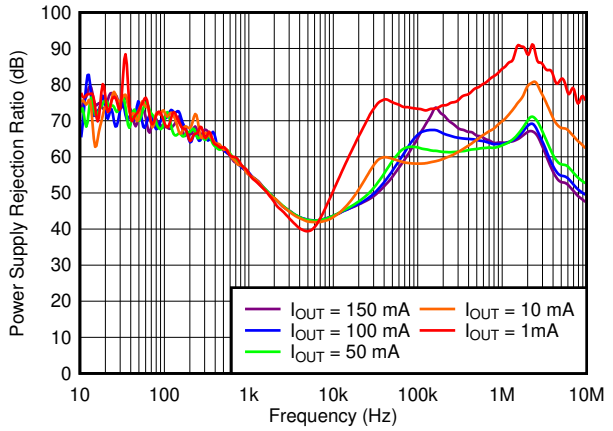
C_{OUT} = 10 µF

図 6-7. Line Regulation at 100 mA



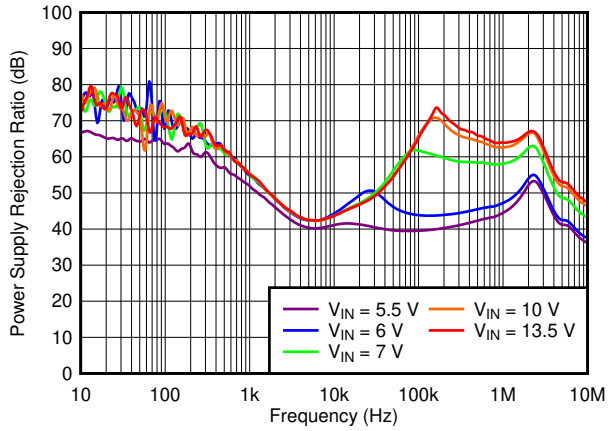
V_{IN} = 3 V

図 6-8. Dropout Voltage (V_{DO}) vs I_{OUT}



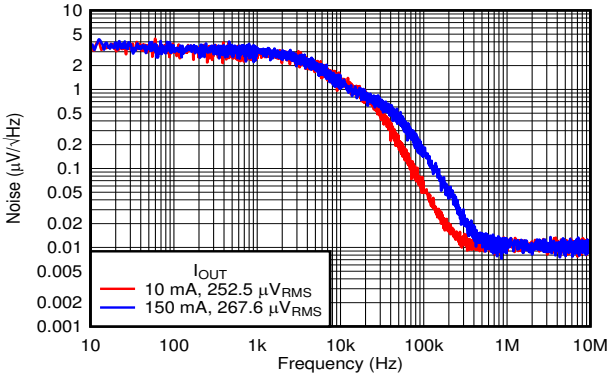
C_{OUT} = 10 µF (X7R 50 V), V_{OUT} = 5 V

図 6-9. PSRR vs Frequency and I_{OUT}



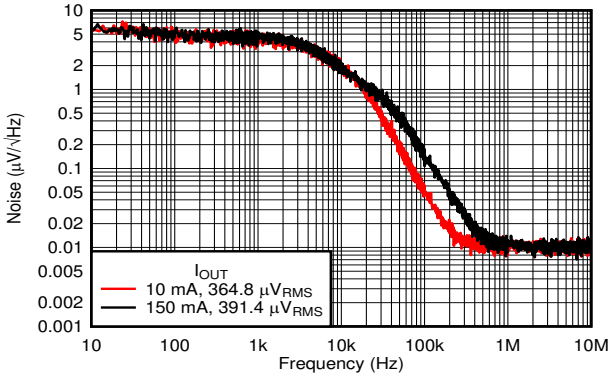
C_{OUT} = 10 µF (X7R 50 V), I_{OUT} = 150 mA, V_{OUT} = 5 V

図 6-10. PSRR vs Frequency and V_{IN}



V_{OUT} = 3.3 V, C_{OUT} = 10 µF

図 6-11. Noise vs Frequency at 3.3 V

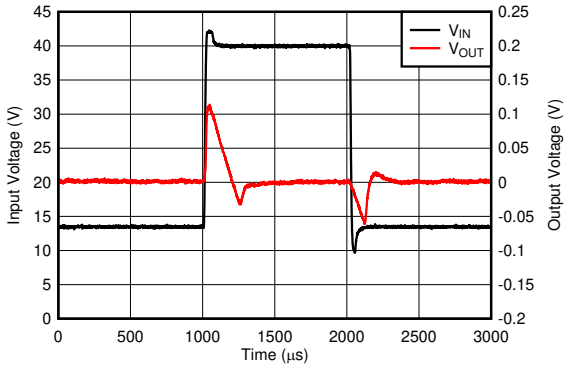


V_{OUT} = 5 V, C_{OUT} = 10 µF

図 6-12. Noise vs Frequency at 5.0 V

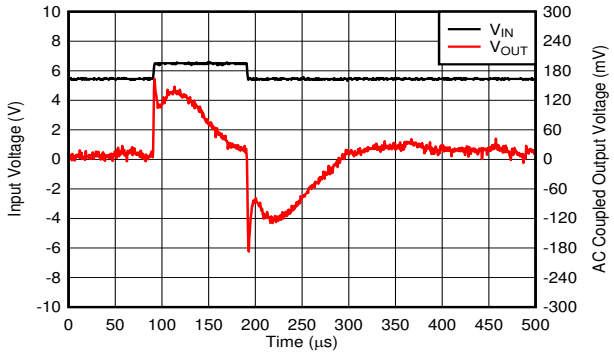
6.7 Typical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 100 µA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF, and V_{EN} = 2 V (unless otherwise noted)



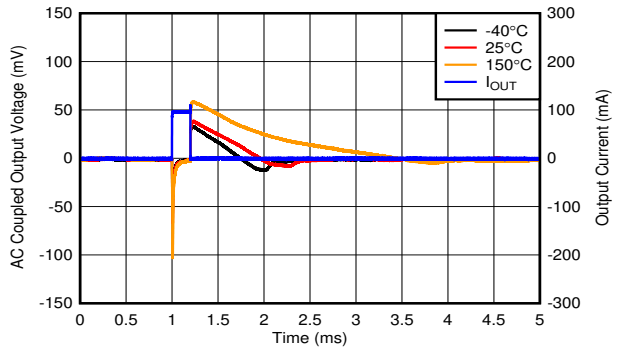
V_{OUT} = 5 V, I_{OUT} = 1 mA, V_{IN} = 13.5 V to 40 V, slew rate = 2.7 V/µs, V_{EN} = 3.3 V, C_{OUT} = 10 µF

図 6-13. Line Transients at 13.5 V to 40 V



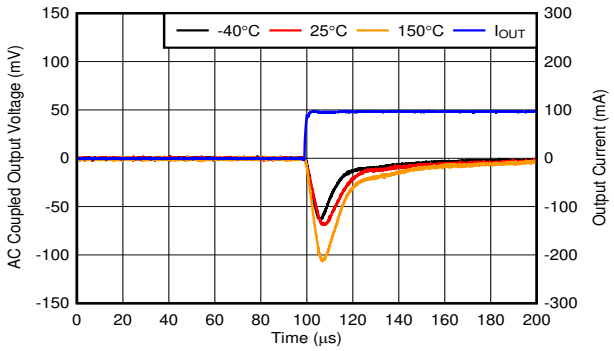
V_{OUT} = 5 V, V_{IN} = 5.5 V to 6.5 V, t_{rise} = 1 µs, C_{OUT} = 10 µF

図 6-14. Line Transients at 5.5 V to 6.5 V



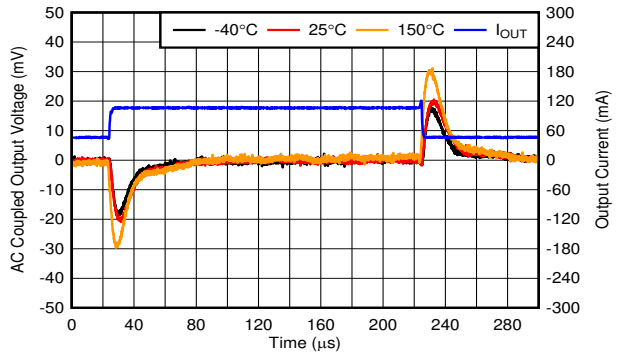
V_{OUT} = 5 V, I_{OUT} = 0 mA to 100 mA, slew rate = 1 A/µs, V_{EN} = 3.3 V, C_{OUT} = 10 µF

図 6-15. Load Transient, No Load to 100 mA



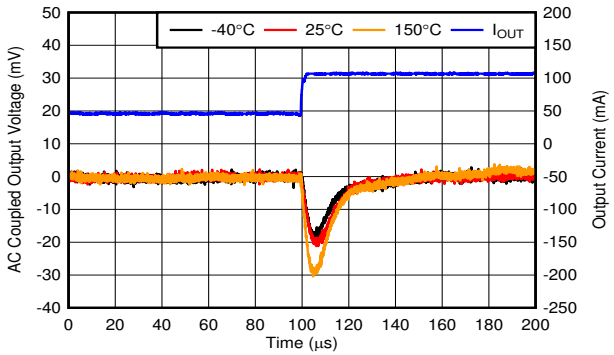
V_{OUT} = 5 V, I_{OUT} = 0 mA to 100 mA, slew rate = 1 A/µs, V_{EN} = 3.3 V, C_{OUT} = 10 µF

図 6-16. Load Transient, No Load to 100-mA Rising Edge



V_{OUT} = 5 V, I_{OUT} = 45 mA to 105 mA, slew rate = 0.1 A/µs, V_{EN} = 3.3 V, C_{OUT} = 10 µF

図 6-17. Load Transient, 45 mA to 105 mA

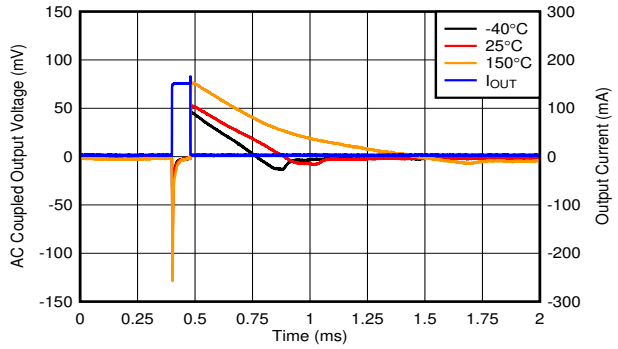


V_{OUT} = 5 V, I_{OUT} = 45 mA to 105 mA, slew rate = 0.1 A/µs, V_{EN} = 3.3 V, C_{OUT} = 10 µF

図 6-18. Load Transient, 45-mA to 105-mA Rising Edge

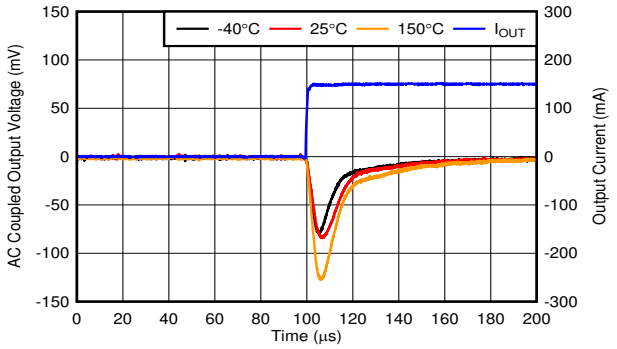
6.7 Typical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 100 µA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF, and V_{EN} = 2 V (unless otherwise noted)



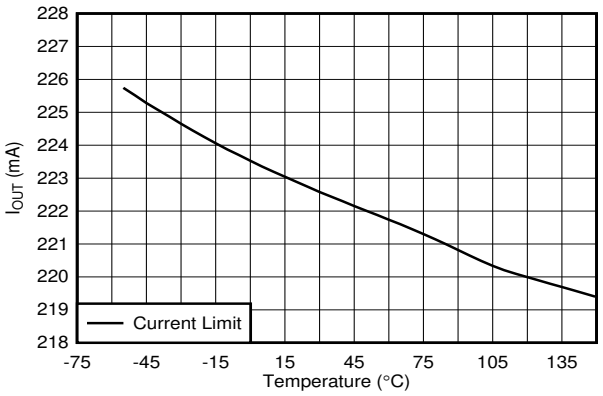
V_{OUT} = 5 V, I_{OUT} = 0 mA to 150 mA, slew rate = 1 A/µs, V_{EN} = 3.3 V, C_{OUT} = 10 µF

図 6-19. Load Transient, No Load to 150 mA



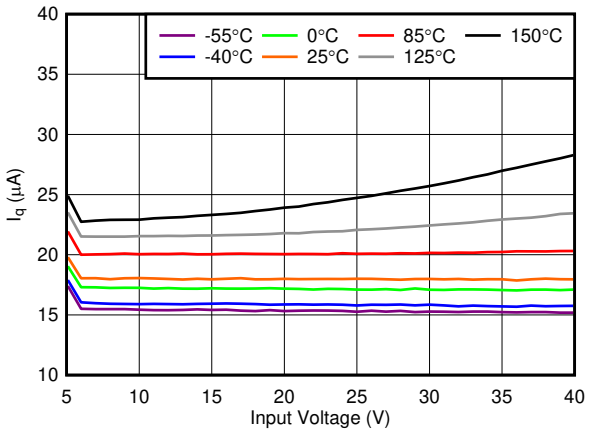
V_{OUT} = 5 V, I_{OUT} = 0 mA to 150 mA, slew rate = 1 A/µs, V_{EN} = 3.3 V, C_{OUT} = 10 µF

図 6-20. Load Transient, No Load to 150-mA Rising Edge



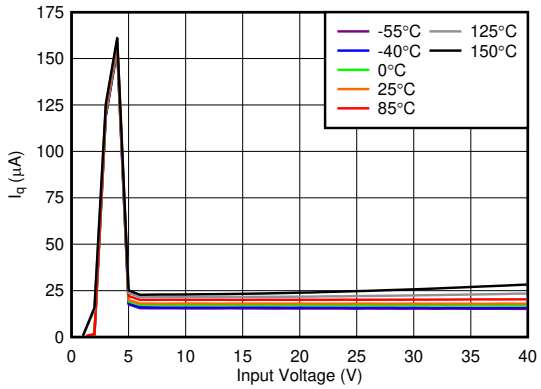
V_{IN} = V_{OUT} + 1 V, V_{OUT} = 90% × $V_{OUT(NOM)}$

図 6-21. Output Current Limit vs Temperature



V_{OUT} = 5 V

図 6-22. Quiescent Current (I_Q) vs V_{IN}



V_{OUT} = 5 V

図 6-23. Quiescent Current (I_Q) vs V_{IN}

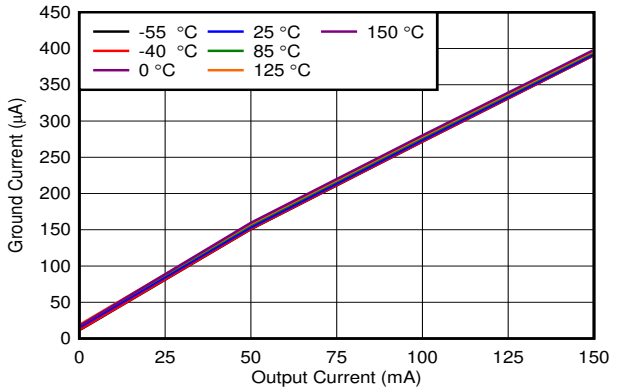
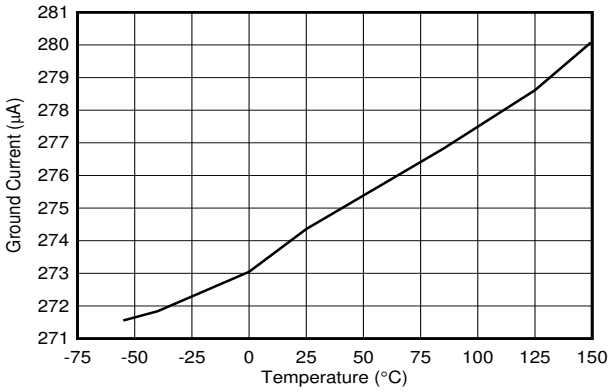


図 6-24. Ground Current (I_{GND}) vs I_{OUT}

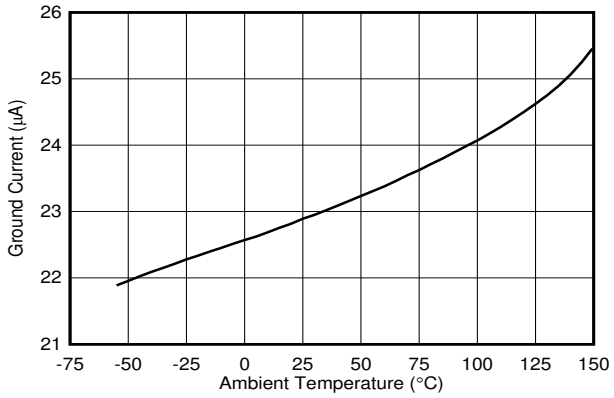
6.7 Typical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 100 µA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF, and V_{EN} = 2 V (unless otherwise noted)



I_{OUT} = 100 mA

図 6-25. Ground Current



I_{OUT} = 500 µA

図 6-26. Ground Current

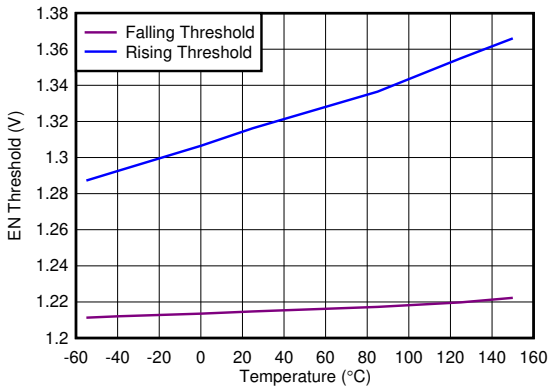


図 6-27. EN Threshold vs Temperature

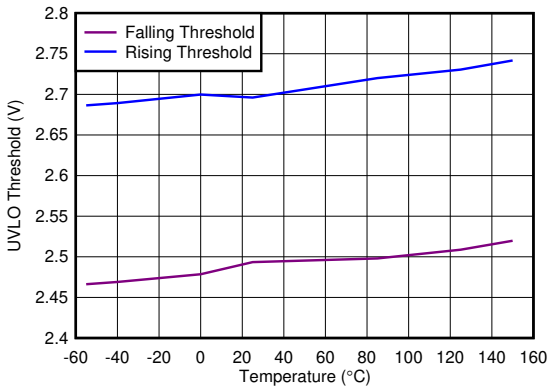


図 6-28. Undervoltage Lockout (UVLO) Threshold vs Temperature

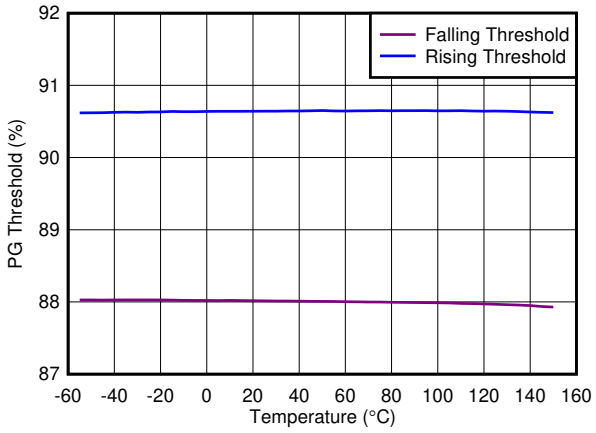


図 6-29. PG Threshold vs Temperature

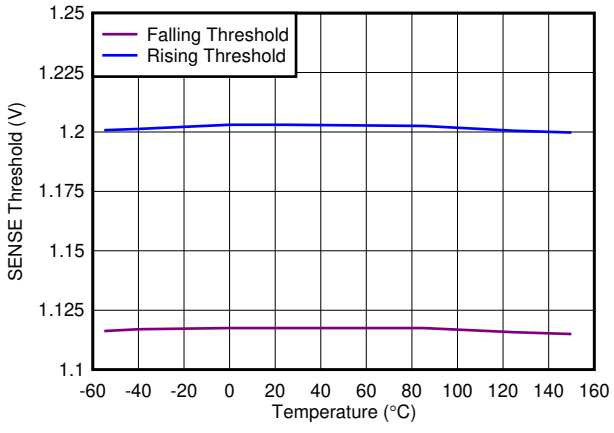


図 6-30. Sense Input Threshold vs Temperature

6.7 Typical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 100 µA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF, and V_{EN} = 2 V (unless otherwise noted)

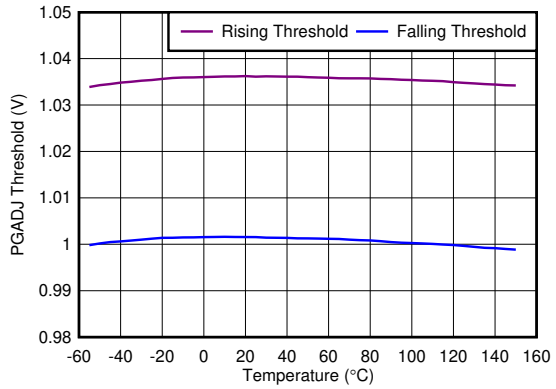
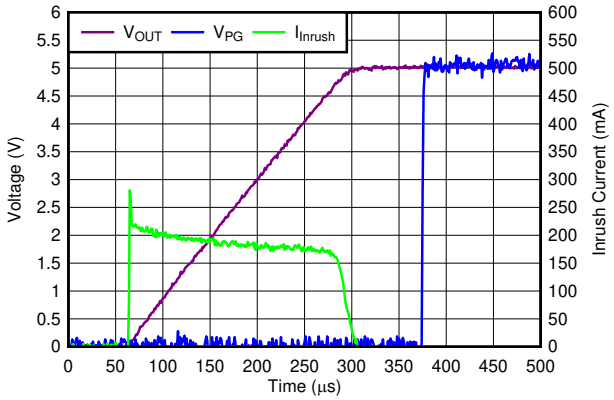
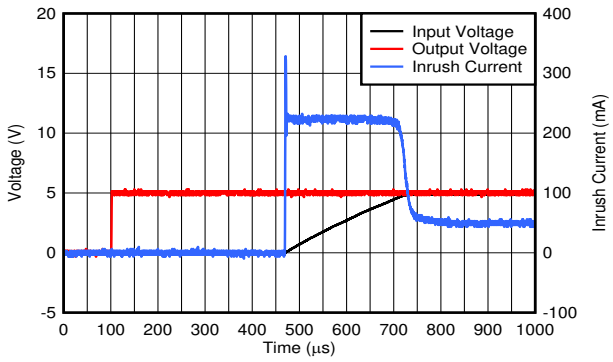


図 6-31. PGADJ Threshold vs Temperature



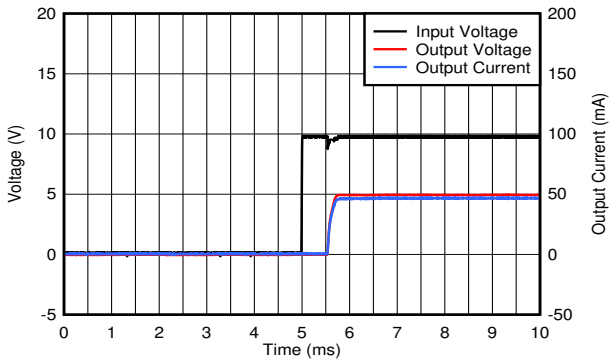
C_{OUT} = 10 µF

図 6-32. Startup Plot Inrush Current



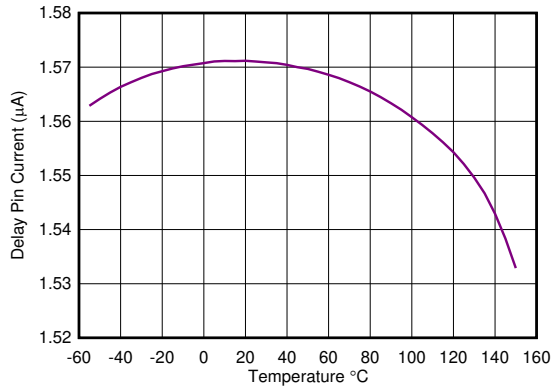
V_{IN} = 13.5 V, C_{OUT} = 10 µF

図 6-33. Startup Plot With EN



C_{OUT} = 10 µF

図 6-34. Startup Plot



V_{DELAY} = 1 V

図 6-35. Delay Pin Current vs Temperature

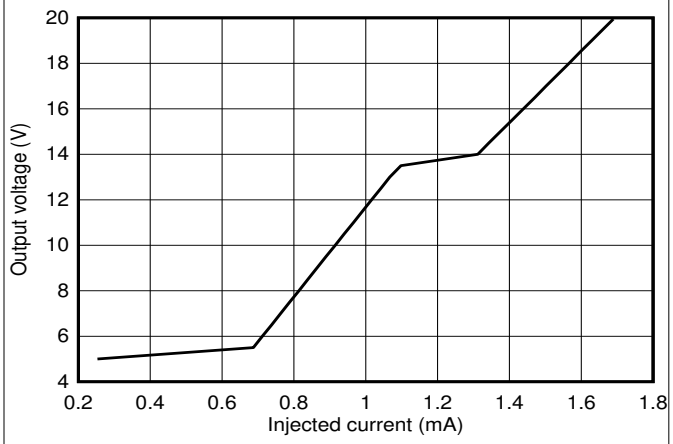


図 6-36. Output Voltage vs Injected Current

6.7 Typical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 100 µA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF, and V_{EN} = 2 V (unless otherwise noted)

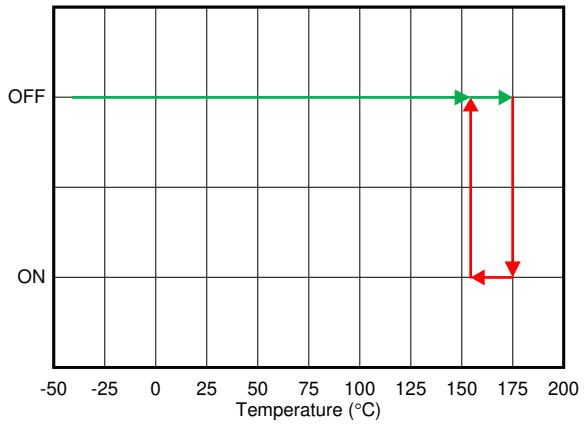


図 6-37. Thermal Shutdown

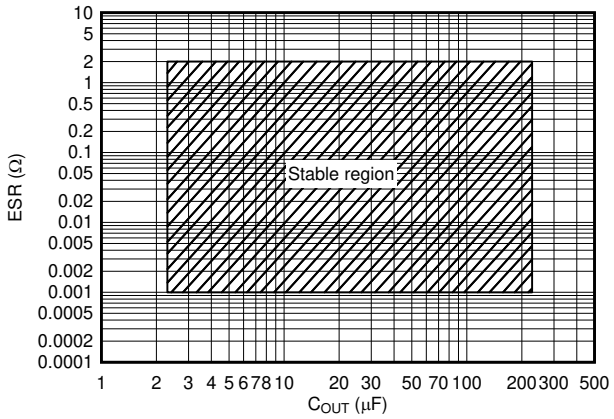


図 6-38. Stability ESR vs C_{OUT}

7 Detailed Description

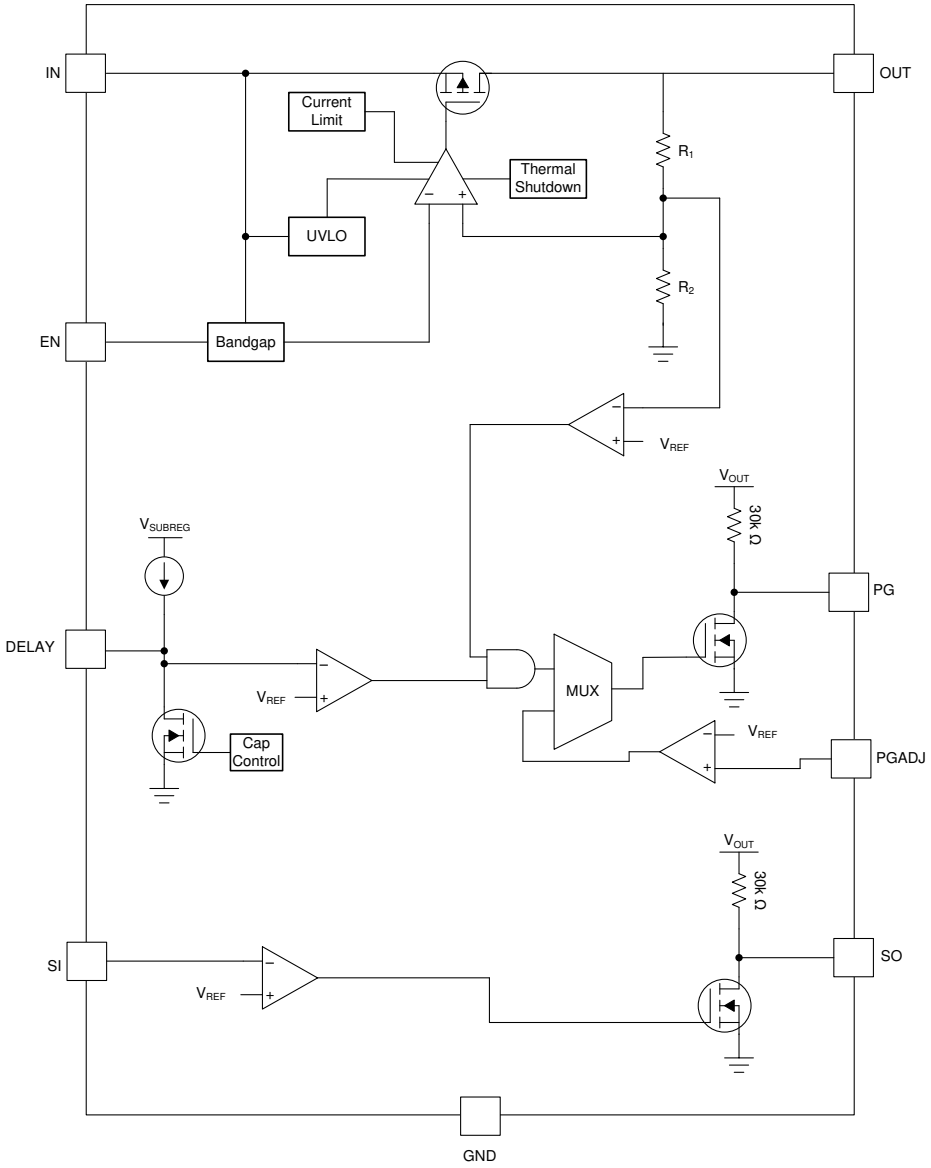
7.1 Overview

The TPS7B85-Q1 is a low-dropout linear regulator (LDO) designed to connect to the battery in automotive applications. The device has an input voltage range extending to 40 V, which allows the device to withstand transients (such as load dumps) that are anticipated in automotive systems. With only a 18-µA quiescent current at light loads, the device is an optimal solution for powering always-on components.

The device has a state-of-the-art transient response that allows the output to quickly react to changes in the load or line (for example, during cold-crank conditions). Additionally, the device has a novel architecture that minimizes output overshoot when recovering from dropout. During normal operation, the device has a tight DC accuracy of ±0.75% over line, load, and temperature.

The TPS7B85-Q1 is equipped with power-good and integrated voltage monitoring. The power-good delay and voltage threshold can be adjusted by external components. The integrated voltage detector can be used to monitor the input voltage and alert downstream components (such as MCUs) when the battery voltage begins to fall.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable (EN)

The enable pin for the device is an active-high pin. The output voltage is enabled when the voltage of the enable pin is greater than the high-level input voltage of the EN pin and disabled with the enable pin voltage is less than the low-level input voltage of the EN pin. If independent control of the output voltage is not needed, connect the enable pin to the input of the device.

7.3.2 Power-Good (PG)

The PG signal provides an easy solution to meet demanding sequencing requirements because PG alerts when the output nears its nominal value. PG can be used to signal other devices in a system when the output voltage is near, at, or above the set output voltage ($V_{OUT(nom)}$). 図 7-1 shows a simplified schematic. The PG signal has an internal pullup resistor to the nominal output voltage and is active high. The PG circuit sets the PG pin into a high-impedance state to indicate that the power is good.

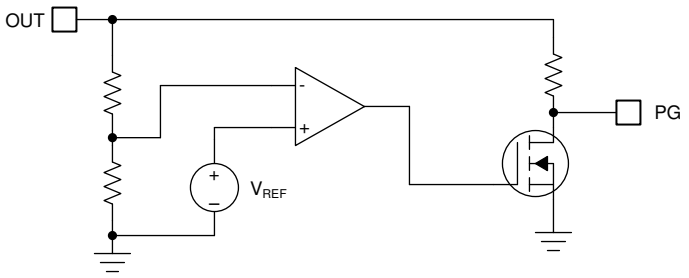


図 7-1. Simplified Power-Good Schematic

7.3.2.1 Adjustable Power-Good (PGADJ)

One unique feature of this LDO, as shown in 図 7-2, is the ability to adjust the power-good threshold through the use of a resistor divider. The adjustable power-good threshold allows the PG threshold to be set to the desired level to further assist in transient detection or sequencing requirements. If this feature is not desired, then tie the PGADJ pin to GND and the default PG threshold is used. For more information on how to calculate the power-good threshold, see the *Setting the Adjustable Power-Good Delay* section.

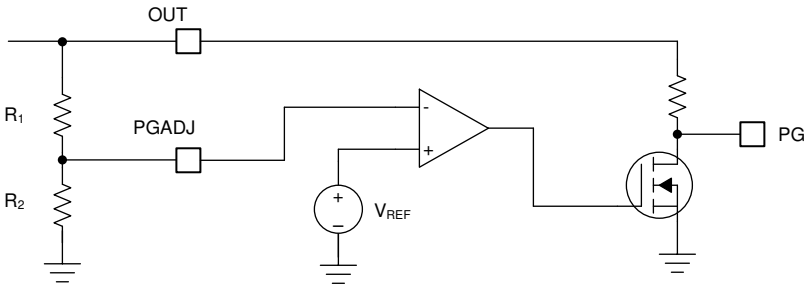
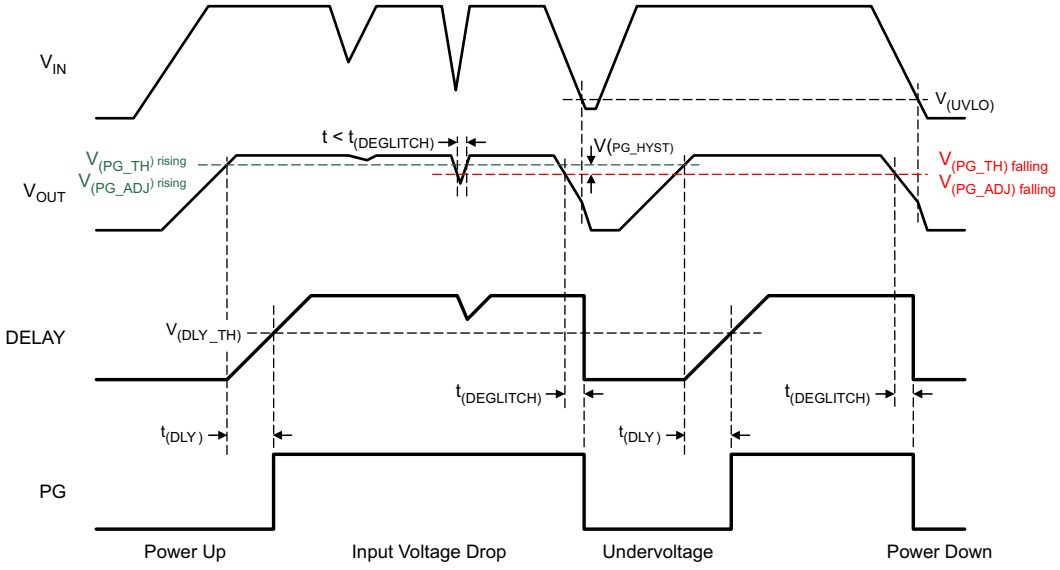


図 7-2. Typical Use of Power-Good Adjust Pin

7.3.3 Adjustable Power-Good Delay Timer (DELAY)

The power-good delay period is a function of the external capacitor on the DELAY pin. The adjustable delay configures the amount of time required before the PG pin becomes high. This delay is configured by connecting an external capacitor from this pin to GND. 図 7-3 illustrates the typical timing diagram for the power-good delay pin. If the DELAY pin is left floating, the power-good delay is $t_{(DLY\_FIX)}$. For more information on how to program the PG delay, see the *Setting the Adjustable Power-Good Delay* section.



$V_{(PG\_TH)\ falling} = V_{(PG\_TH)\ rising} - V_{(PG\_HYST)}$.

図 7-3. Typical Power-Good Timing Diagram

7.3.4 Sense Comparator

The sense comparator compares the input signal with an internal voltage reference of 1.223 V for a rising threshold and 1.123 V for a falling threshold. Using an external voltage divider makes this comparator very flexible in the application.

The device can supervise the input voltage either before or after the protection diode and provides additional information to the microprocessor (such as low-voltage warnings).

7.3.5 Undervoltage Lockout

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

7.3.6 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during startup can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before startup completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed its operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

7.3.7 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brickwall scheme. In a high-load current fault, the brickwall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application report.

図 7-4 shows a diagram of the current limit.

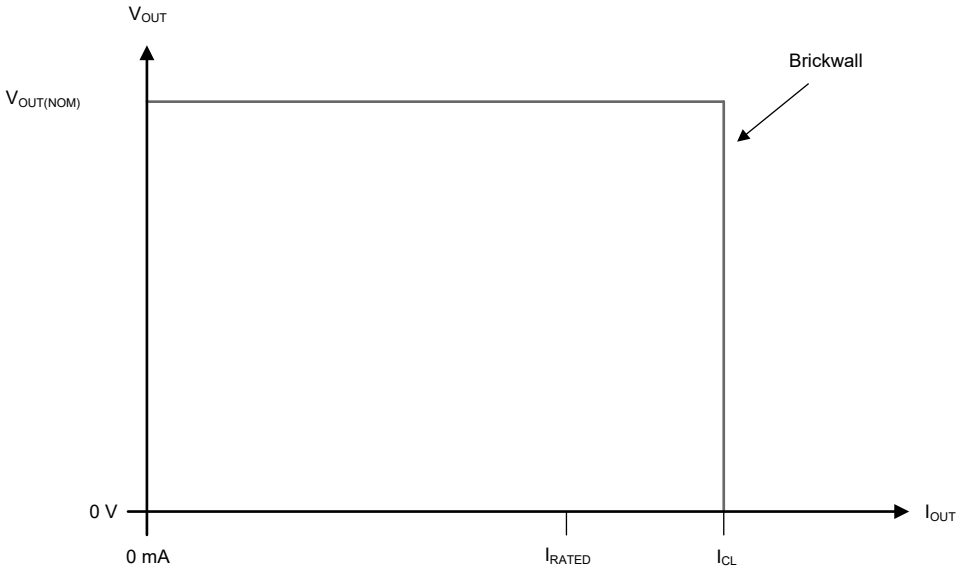


図 7-4. Current Limit

7.4 Device Functional Modes

7.4.1 Device Functional Mode Comparison

The *Device Functional Mode Comparison* table shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

表 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

7.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

8 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

8.1.1 Input and Output Capacitor Selection

The TPS7B85-Q1 requires an output capacitor of 2.2 µF or larger (1 µF or larger capacitance) for stability and an equivalent series resistance (ESR) between 0.001 Ω and 2 Ω. For the best transient performance, use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and ESR over temperature. When choosing a capacitor for a specific application, be mindful of the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitance is 220 µF.

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors can be used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are anticipated, or if the device is located several inches from the input power source.

8.1.2 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} – V_{OUT}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

8.1.3 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \leq V_{IN} + 0.3$ V.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection is recommended to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

8.1.4 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (2)$$

Note

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (3)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

8.1.4.1 Thermal Performance Versus Copper Area

The most used thermal resistance parameter, $R_{\theta JA}$, is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table in the *Specifications* section is determined by the JEDEC standard (see 図 8-1), PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper.

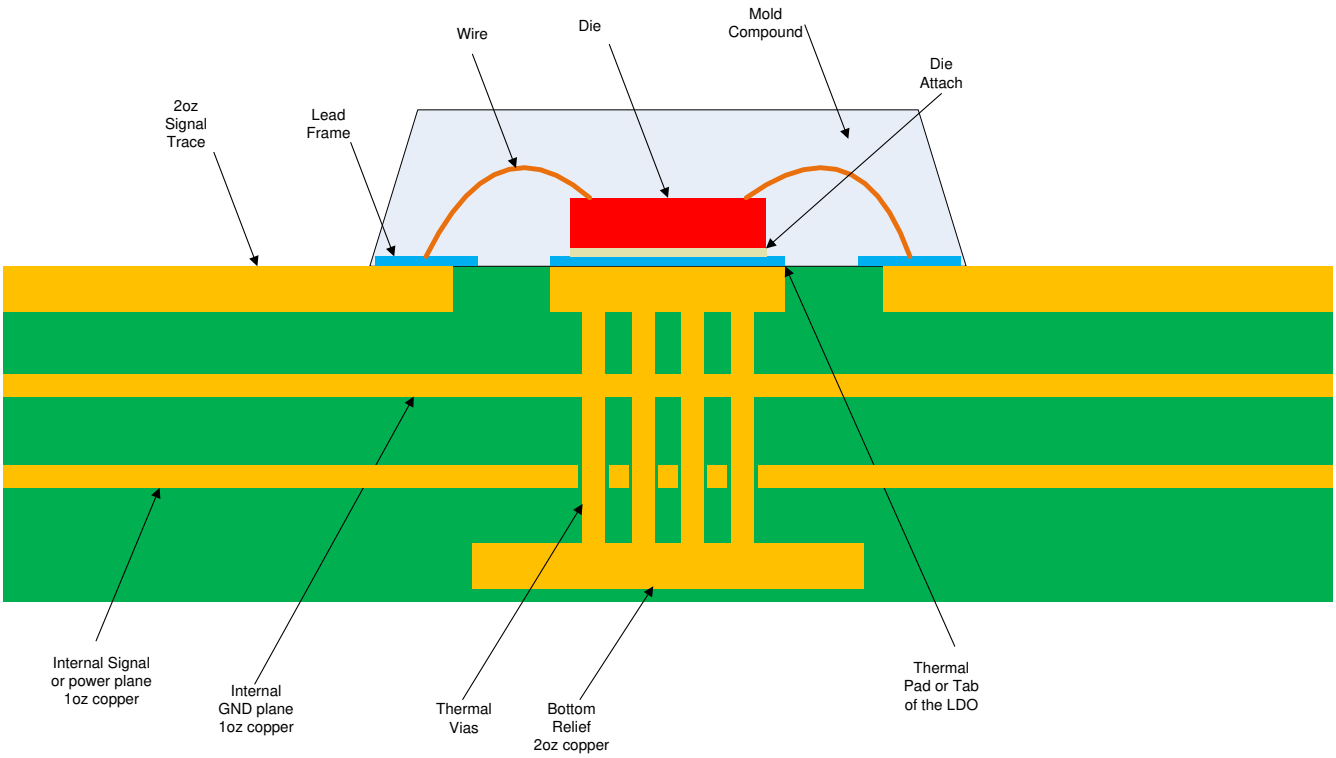


図 8-1. JEDEC Standard 2s2p PCB

図 8-2 and 図 8-3 depict the functions of $R_{\theta JA}$ and ψ_{JB} versus copper area and thickness. These plots are generated with a 101.6-mm x 101.6-mm x 1.6-mm PCB of two and four layers. For the four-layer board, the inner planes use a 1-oz copper thickness. Outer layers are simulated with both a 1-oz and 2-oz copper thickness. A 4 x 4 array of thermal vias of 300-µm drill diameter and 25-µm Cu plating is located beneath the thermal pad of the device. The thermal vias connect the top layer, the bottom layer and, in the case of the 4-layer board, the first inner GND plane. Each of the layers has a copper plane of equal area.

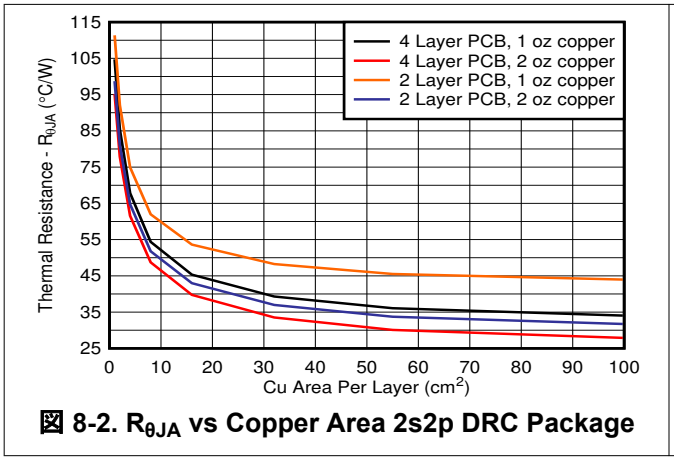


図 8-2. $R_{\theta JA}$ vs Copper Area 2s2p DRC Package

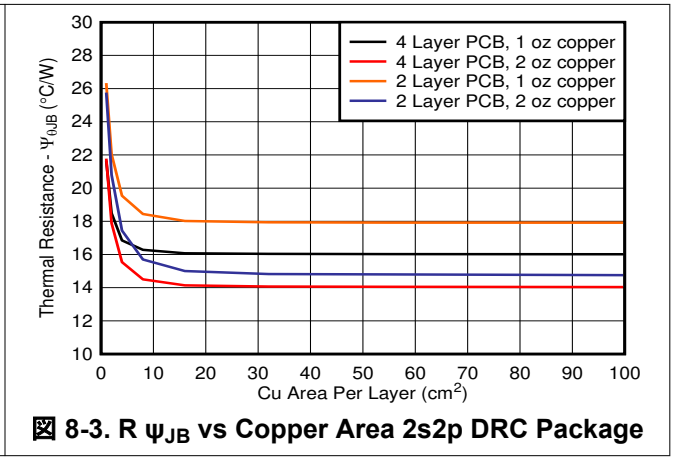


図 8-3. R ψ_{JB} vs Copper Area 2s2p DRC Package

8.1.5 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \tag{4}$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \tag{5}$$

where

- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application report.

8.1.6 SI Pin

8.1.6.1 Calculating the Sense Input (SI) Pin Threshold

To use the SI pin, connect this pin to the rail being monitored through a resistor divider. This input can be configured as an undervoltage supervisor that can monitor voltage rails greater than 1.2 V or used as an overvoltage supervisor with an inverted output. 表 8-1 lists typical 1% resistor values for undervoltage monitoring where the trip point is a 5% threshold. The resistor values can be scaled to decrease the amount of current flowing through the resistor divider, but increasing the resistor values also decreases the accuracy of the resistor divider. General practice is for the current flowing through the resistor divider to be 100 times greater than the current going into the SI pin. This practice ensures the highest possible accuracy. 式 6 can be used to calculate the resistors required in the resistor divider for any desired falling threshold. 図 8-4 depicts the typical timing for this comparator and 図 8-5 illustrates a block diagram for the adjustable operation.

$$V_{mon(falling)} = V_{SI(LOW)} x \left(1 + \frac{R1}{R2}\right) \tag{6}$$

表 8-1. SI Resistor Divider Values

INPUT VOLTAGE (V)	5% THRESHOLD		
	R1 (kΩ)	R2 (kΩ)	THRESHOLD VOLTAGE (V)
3.3	18.2	10	3.13
5	32.4	10	4.71
6	41.2	10	5.68
7	49.9	10	6.65
8	59	10	7.66
9	66.5	10	8.49
10	75.5	10	9.49
11	80.6	10	10.06
12	93.1	10	11.44
13.5	105	10	12.77

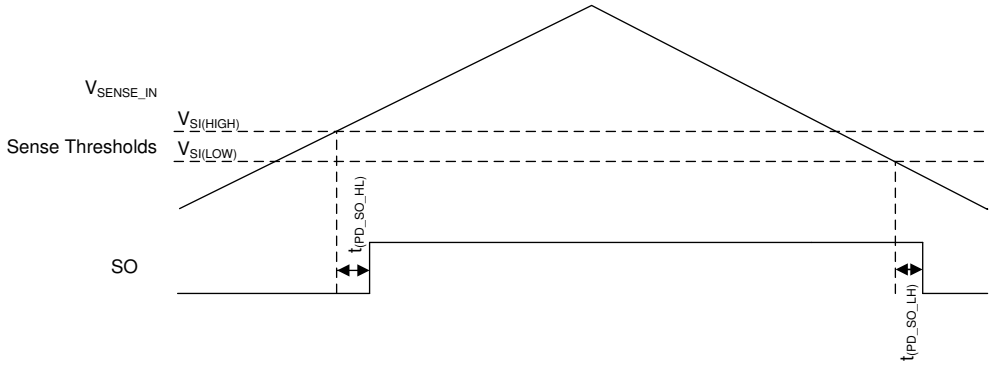


図 8-4. SI Timing Diagram

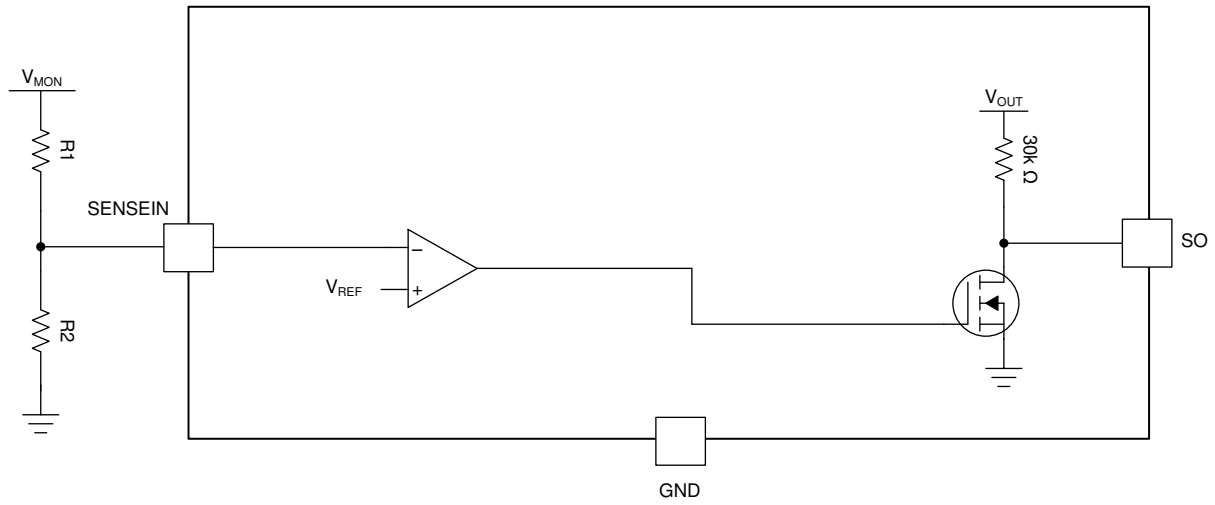


図 8-5. SI Basic Block Diagram

8.1.6.2 Different Uses for the Sense Input Pin

The sense input pin incorporates a comparator with hysteresis into the LDO. The SI pin can help replace a supervisor in the system by connecting the SI pin to rails that need to be monitored. The three most common uses for this supervisor are described in the *Monitoring Input Voltage*, *Creating OV and UV Power-Good*, and *Monitoring a Separate Supply Voltage* sections.

8.1.6.2.1 Monitoring Input Voltage

Monitoring the input voltage of the LDO, as shown in 図 8-6, is the most common way that the SI pin is used. The device has a built-in precision comparator that allows the device to compare a divided-down version of the input to the internal reference of the LDO. When the voltage on the sense pin is below $V_{SI(LOW)}$, the output of the SO pin is low. However, when V_{SI} crosses $V_{SI(HIGH)}$ the voltage on the SO pin gets pulled up to V_{OUT} through a pullup resistor, R_{SO}. This pin also has built-in hysteresis to keep the pin from toggling between the two states from small changes on the SENSE voltage. 図 8-7 shows a typical timing diagram for the SENSE pin.

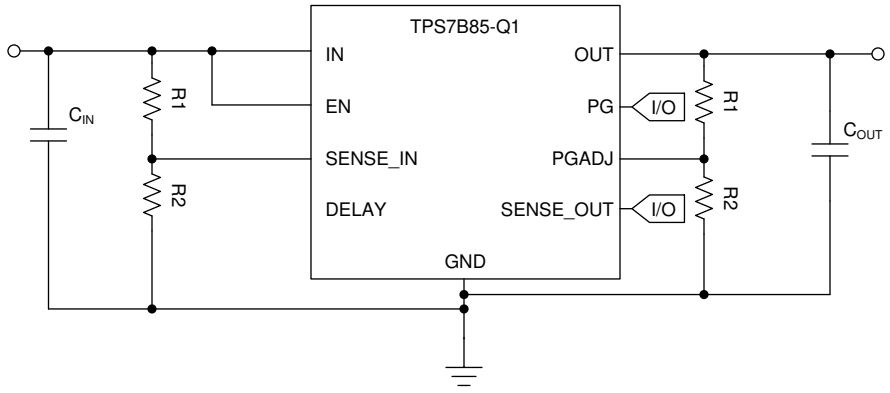


図 8-6. Monitoring the Device Input Voltage

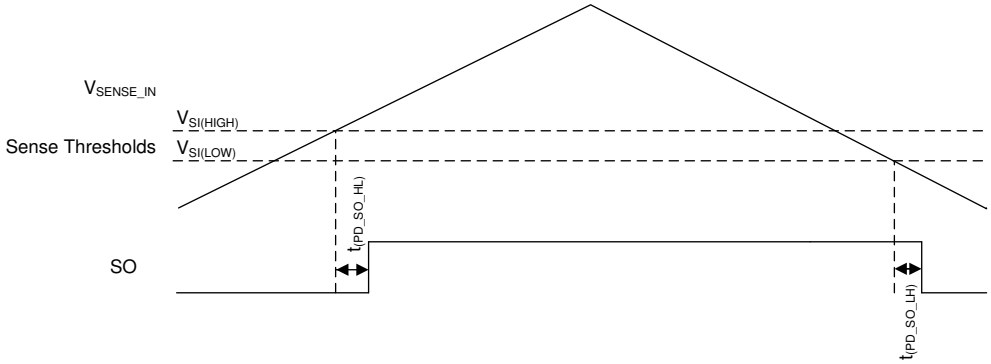


図 8-7. SENSE Pin Timing Diagram

8.1.6.2.2 Creating OV and UV Power-Good

Another feature that is often desired is the ability to monitor the output voltage for overvoltage (OV) or undervoltage (UV) events. Because the integrated power-good pin only detects undervoltage events, a separate solution must be implemented to monitor for overvoltage issues. This monitoring can be done by using the integrated SI pin and connecting this pin to the output through a resistor divider. Then place the rising threshold of the SI pin where the output voltage is going to be flagged as overvoltage. 式 7 depicts how to calculate the resistor divider for this application based on the desired overvoltage threshold. If this method is used for creating an overvoltage detection, the output of the overvoltage signal has inverted logic. 図 8-8 shows the typical configuration for using the device as an overvotlage monitor.

$$V_{mon(rising)} = V_{SI(HIGH)} x \left(1 + \frac{R1}{R2}\right) \quad (7)$$

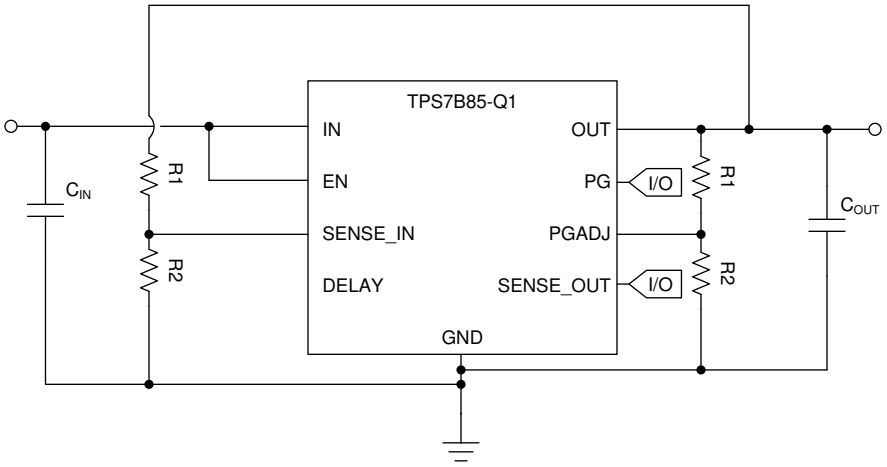


図 8-8. Creating an Overvoltage Detector on the Output

8.1.6.2.3 Monitoring a Separate Supply Voltage

One of the final applications for the SI pin is monitoring a separate supply. This method can be implemented as either an overvoltage detection or undervoltage detection for the externally monitored supply. 式 6 and 式 7 can be used to calculate the resistor dividers required to implement the supervision of the separate power supply. 図 8-9 shows a block diagram for this monitoring application.

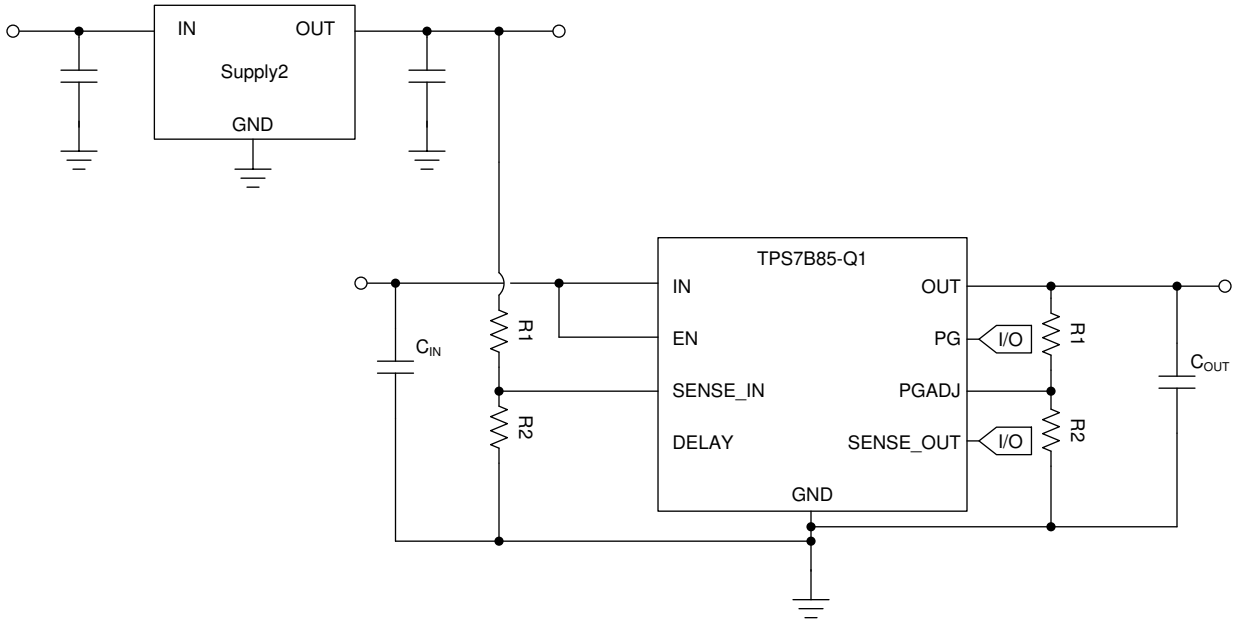


図 8-9. Monitoring a Separate Power Supply

8.1.7 Pulling Up the SO and PG Pins to a Different Voltage

Because the sense out (SO) and power-good (PG) pins are pulled up internally to the output rail, they cannot be pulled up to any voltage or wire AND'd like a typical open-drain PG output can be. If these signals must be pulled up to another logic level then an external circuit can be implemented using a PMOS transistor and a pullup resistor. Implementing the circuit shown in 図 8-10 allows the outputs to be pulled up to any logic rail. This implementation also allows the outputs to be AND'd together like the traditional power-good pins.

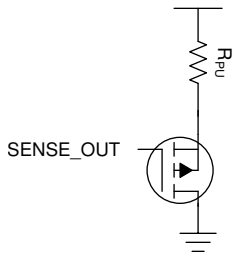


図 8-10. Additional Components for the SO and PG Pins to be Pulled Up to Another Rail

8.1.8 Power-Good

8.1.8.1 Setting the Adjustable Power-Good Threshold

The power-good threshold is also adjustable from 1 V to 18 V with an external resistor divider between PGADJ and OUT. Use 式 8 to calculate this threshold:

$$V_{(PG\_ADJ)falling} = V_{(PGADJ\_TH)falling} x \left(\frac{R_1 + R_2}{R_2} \right)$$
$$V_{(PG\_ADJ)rising} = \left[V_{(PGADJ\_TH)falling} + V_{PGADJ(HYST)} \right] x \left(\frac{R_1 + R_2}{R_2} \right) \quad (8)$$

where

- $V_{(PG\_ADJ)\ rising}$, $V_{(PG\_ADJ)\ falling}$ is the adjustable power-good threshold
- $V_{(PGADJ\_TH)\ falling}$ is the internal comparator reference voltage of the PGADJ pin

By setting the power-good threshold $V_{(PG\_ADJ)\ rising}$, when V_{OUT} exceeds this threshold, the PG output turns high after the power-good delay period has expired. When V_{OUT} falls below $V_{(PG\_ADJ)\ falling}$, the PG output turns low after a short deglitch time. 図 8-11 shows a diagram of the PG threshold.

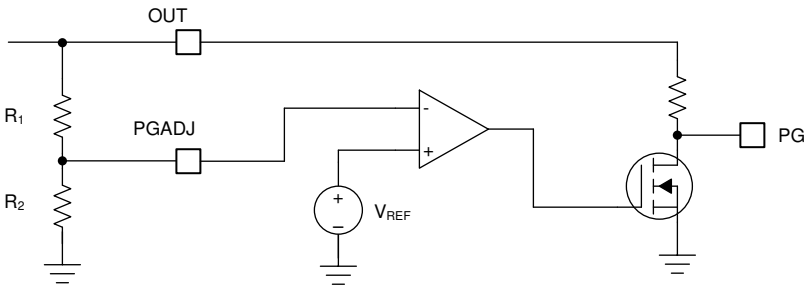


図 8-11. Adjustable Power-Good Threshold

8.1.8.2 Setting the Adjustable Power-Good Delay

The power-good delay time can be set in two ways: either by floating the delay pin or by connecting a capacitor from this pin to GND. When the DELAY pin is floating, the time defaults to $t_{(DLY\_FIX)}$. The delay time is set by 式 9 if a capacitor is connected between the DELAY pin and GND.

$$t = t_{(DLY\_FIX)} + C_{DELAY} \left(\frac{V_{DLY(TH)}}{I_{DLY(CHARGE)}} \right) \quad (9)$$

8.2 Typical Application

図 8-12 shows a typical application circuit for the TPS7B85-Q1. Use different values of external components, depending on the end application. An application may require a larger output capacitor during fast load steps in order to prevent a reset from occurring. TI recommends a low-ESR ceramic capacitor with a dielectric of type X5R or X7R.

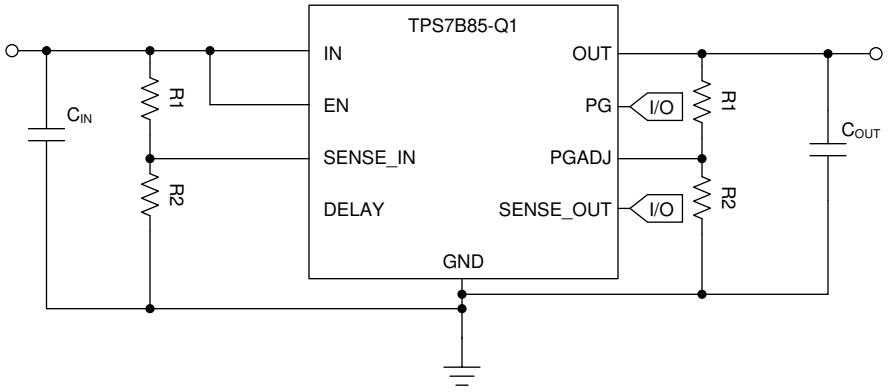


図 8-12. Typical Application Schematic for the TPS7B85-Q1

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-2 as the input parameters.

表 8-2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	6 V to 40 V
Output voltage	5 V
Output current	100 mA
Output capacitor	10 µF
Power-good delay capacitor	100 nF
Sense input trip threshold	5.5 V

8.2.2 Detailed Design Procedure

8.2.2.1 Input Capacitor

The device requires an input decoupling capacitor, the value of which depends on the application. The typical recommended value for the decoupling capacitor is 1 µF. The voltage rating must be greater than the maximum input voltage.

8.2.2.2 Output Capacitor

The device requires an output capacitor to stabilize the output voltage. The capacitor value must be between 2.2 µF and 200 µF and the ESR range must be between 1 mΩ and 2 Ω. For this design a low ESR, 10-µF ceramic capacitor was used to improve transient performance.

8.2.3 Application Curves

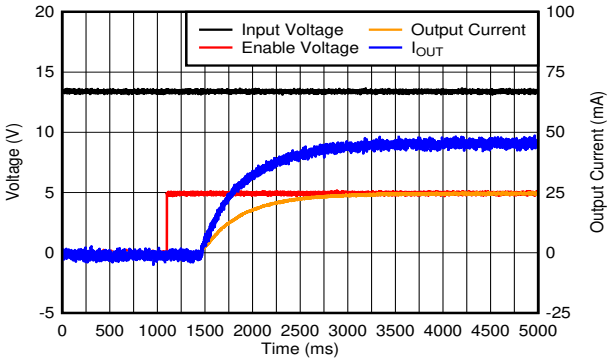


図 8-13. Power-Up Waveform

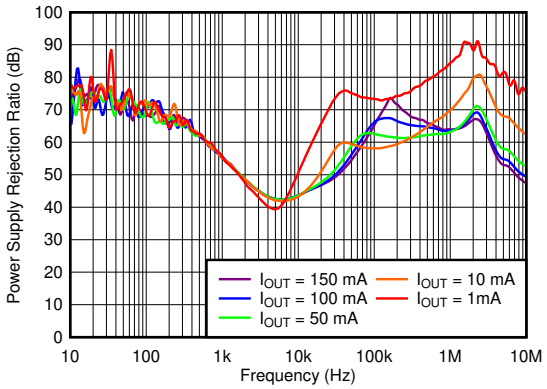


図 8-14. PSRR

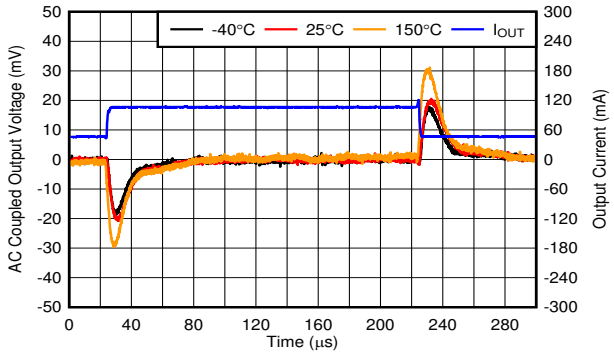


図 8-15. Transient Response

9 Power Supply Recommendations

This device is designed for operation from an input voltage supply with a range between 3 V and 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B85-Q1, add an electrolytic capacitor and a ceramic bypass capacitor at the input.

10 Layout

10.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close as possible to each other, connected by a wide, component-side, copper surface. The use of vias and long traces to the input and output capacitors is strongly discouraged and negatively affects system performance. TI also recommends a ground reference plane either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similarly to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

10.1.1 Package Mounting

Solder pad footprint recommendations for the TPS7B85-Q1 are available at the end of this document and at www.ti.com.

10.1.2 Board Layout Recommendations to Improve PSRR and Noise Performance

As depicted in 図 10-1, place the input and output capacitors close to the device for the layout of the TPS7B85-Q1. In order to enhance the thermal performance, place as many vias as possible around the device. These vias improve the heat transfer between the different GND planes in the PCB.

To improve ac performance such as PSRR, output noise, and transient response, TI recommends a board design with separate ground planes for IN and OUT, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor must connect directly to the GND pin of the device.

Minimize equivalent series inductance (ESL) and ESR in order to maximize performance and ensure stability. Place each capacitor as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. TI strongly discourages the use of vias and long traces to connect the capacitors because these can negatively impact system performance and may even cause instability.

If possible, and to ensure the maximum performance specified in this document, use the same layout pattern used for the TPS7B85-Q1 evaluation board, available at www.ti.com.

10.2 Layout Example

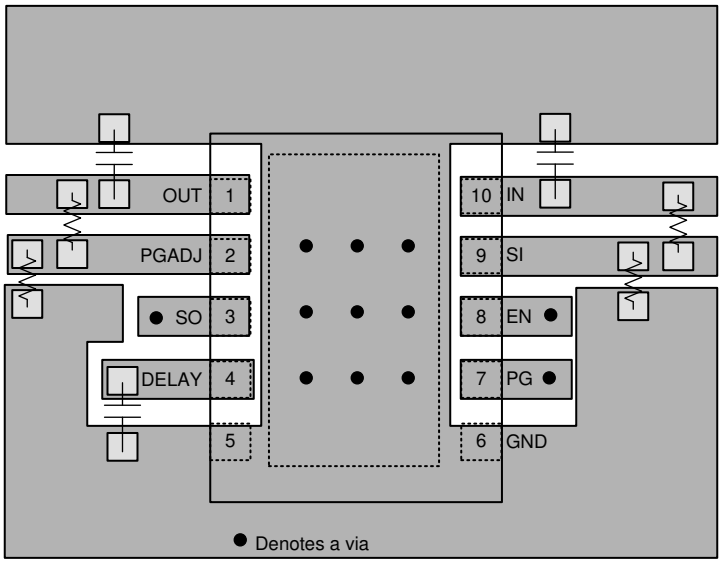


図 10-1. VSON (DRC) Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

表 11-1. Device Nomenclature(1)

PRODUCT	V_{OUT}
TPS7B85**xxQWyyyRQ1**	**xx** is the nominal output voltage (for example, 33 = 3.3 V; 50 = 5.0 V). **Q** indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard. **W** indicates the package has wettable flanks. **yyy** is the package designator. **R** is the package quantity. R is for reel (3000 pieces). **Q1** indicates that this device is an automotive grade (AEC-Q100) device.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。*「更新の通知を受け取る」をクリック*して登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

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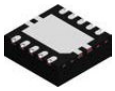
11.6 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

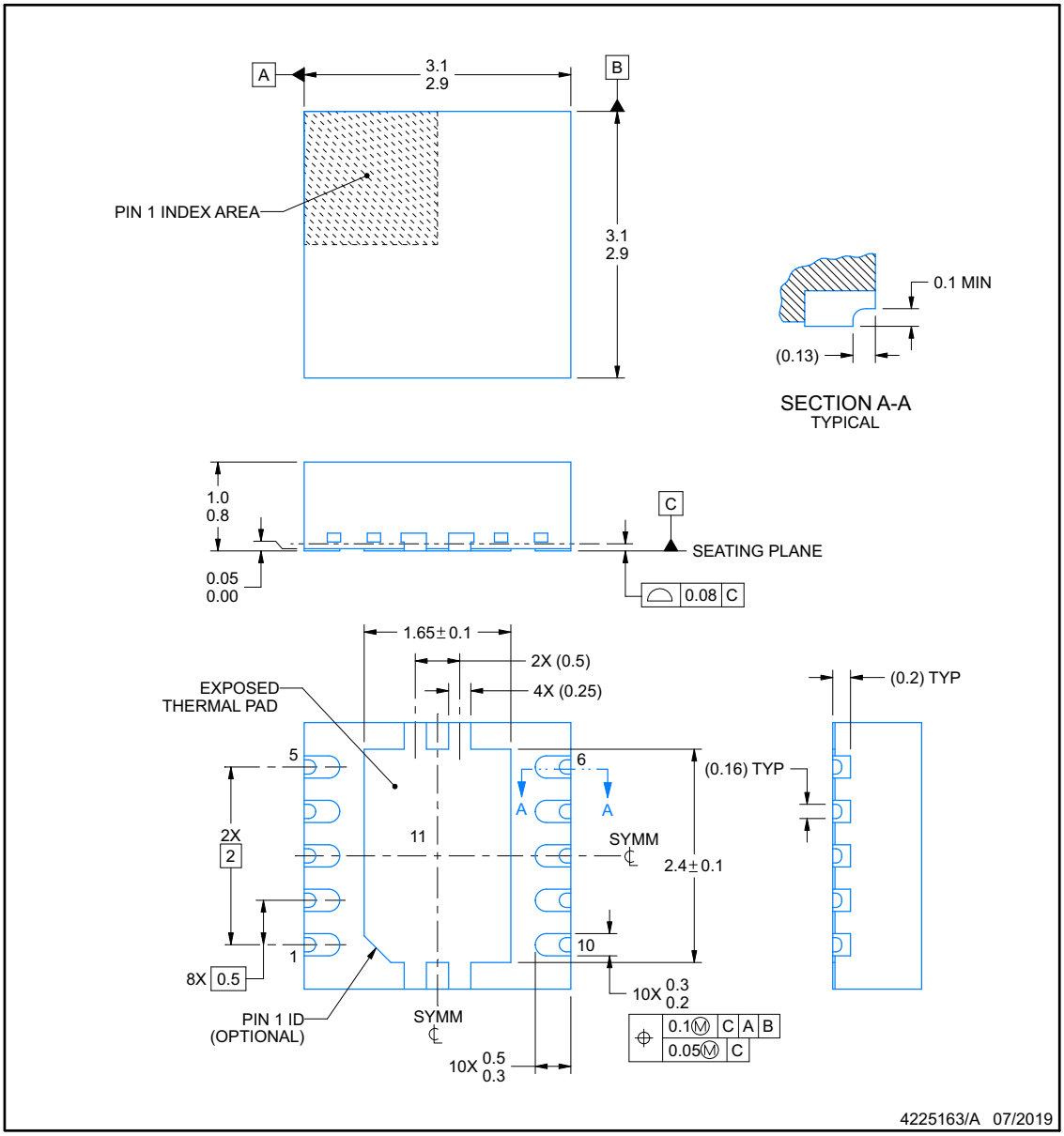


PACKAGE OUTLINE

DRC0010U

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

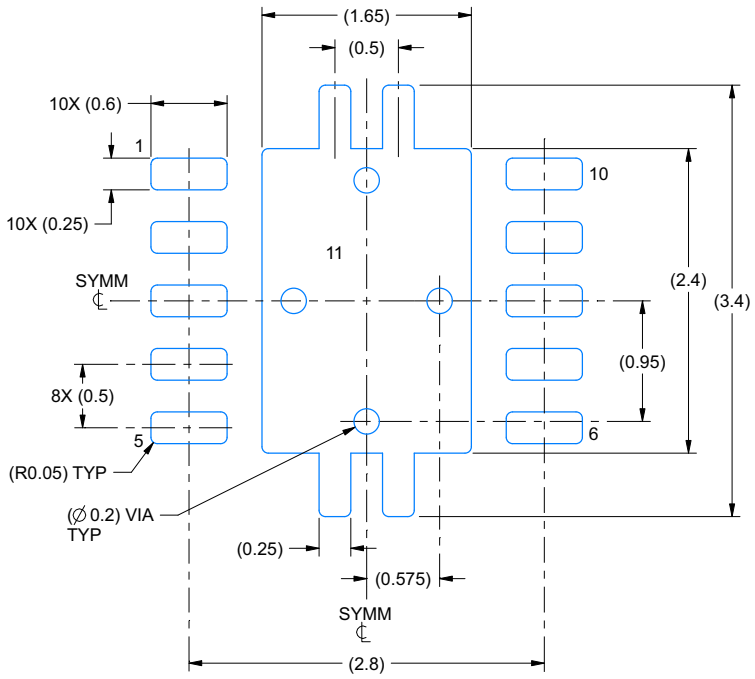
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

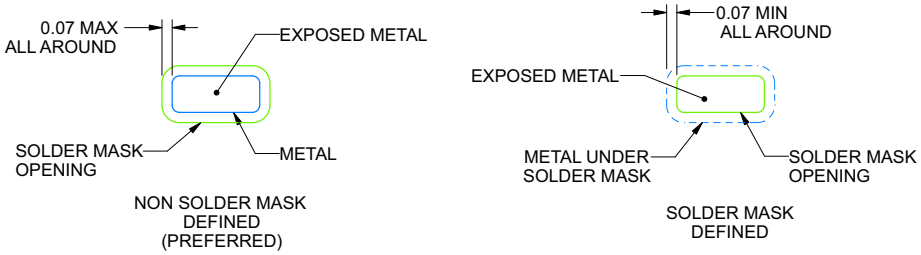
DRC0010U

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

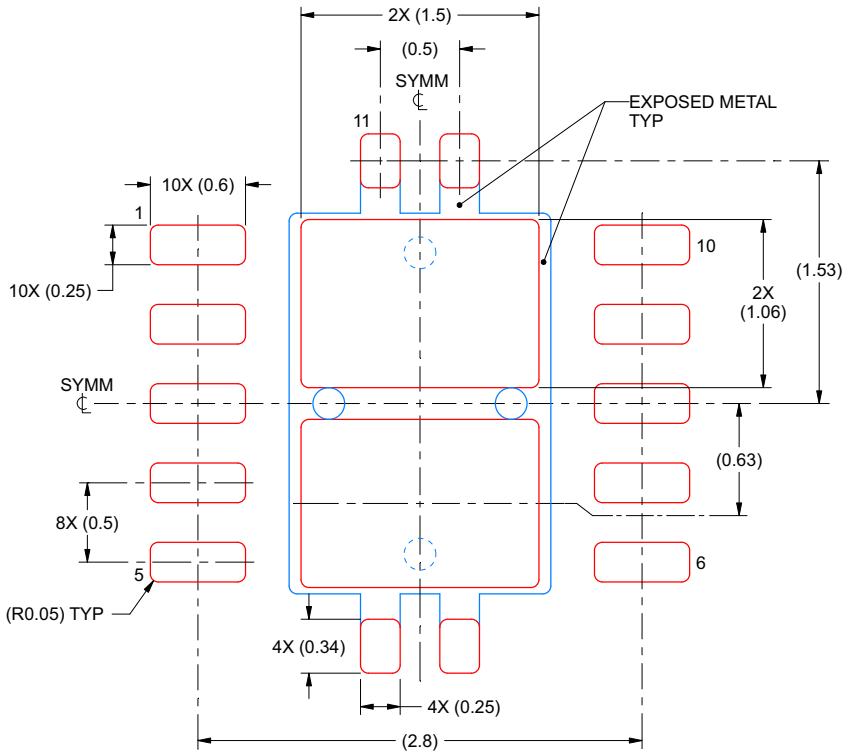
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010U

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7B8533QWDRCRQ1	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	7B8533	Samples
TPS7B8550QWDRCRQ1	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	7B8550	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

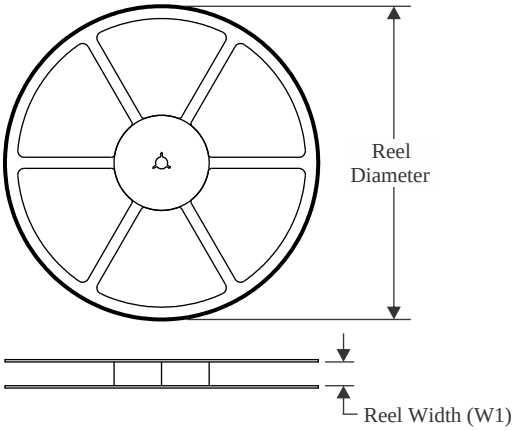
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

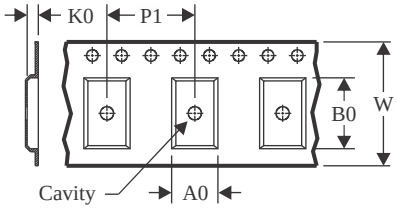
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

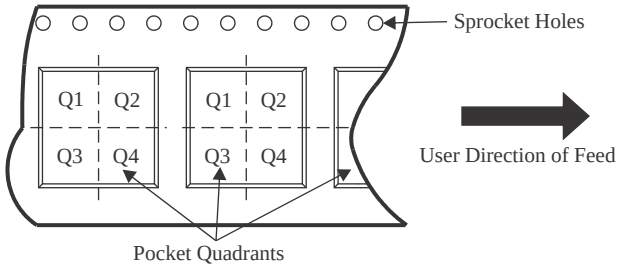


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

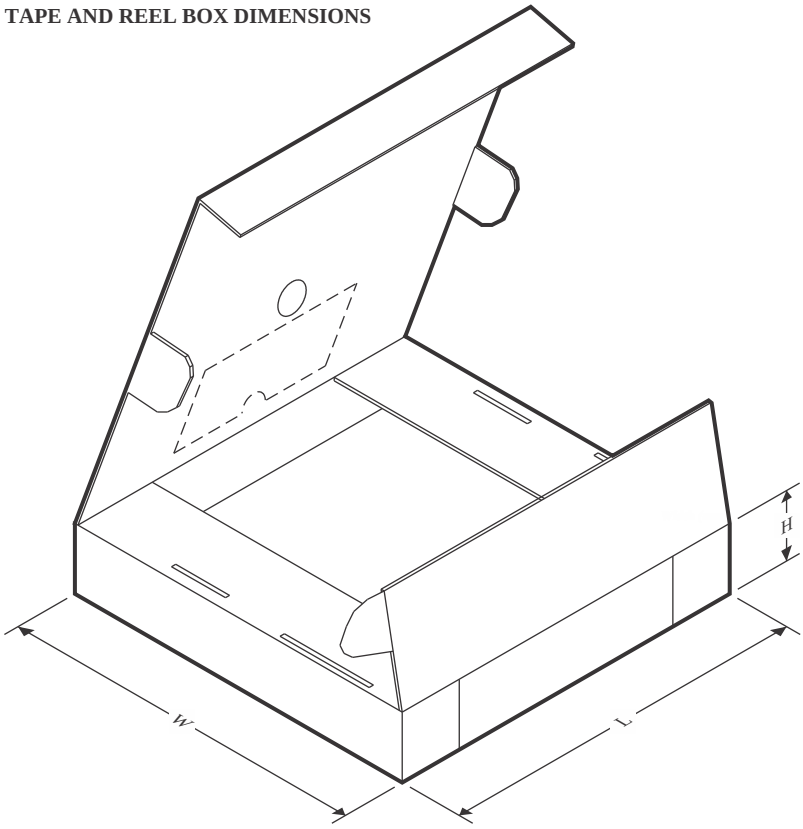
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B8533QWDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS7B8550QWDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B8533QWDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0
TPS7B8550QWDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

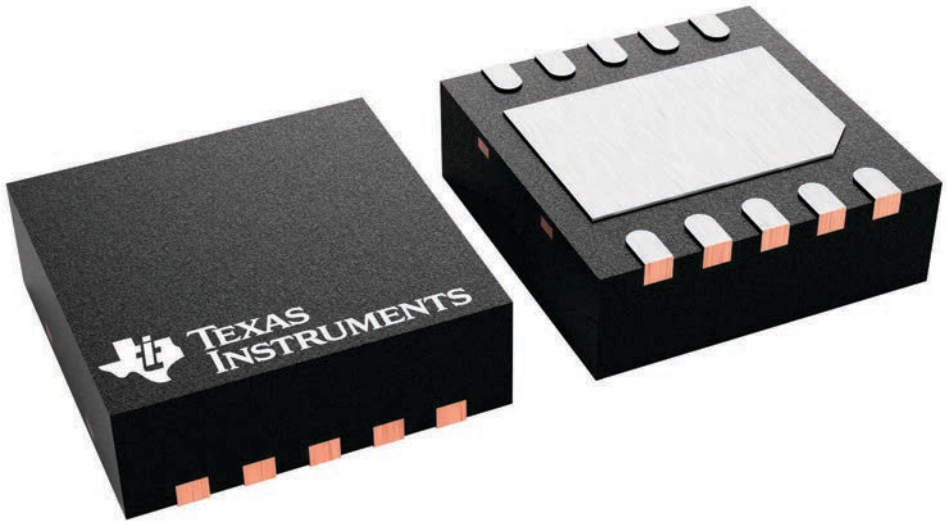
DRC 10

VSON - 1 mm max height

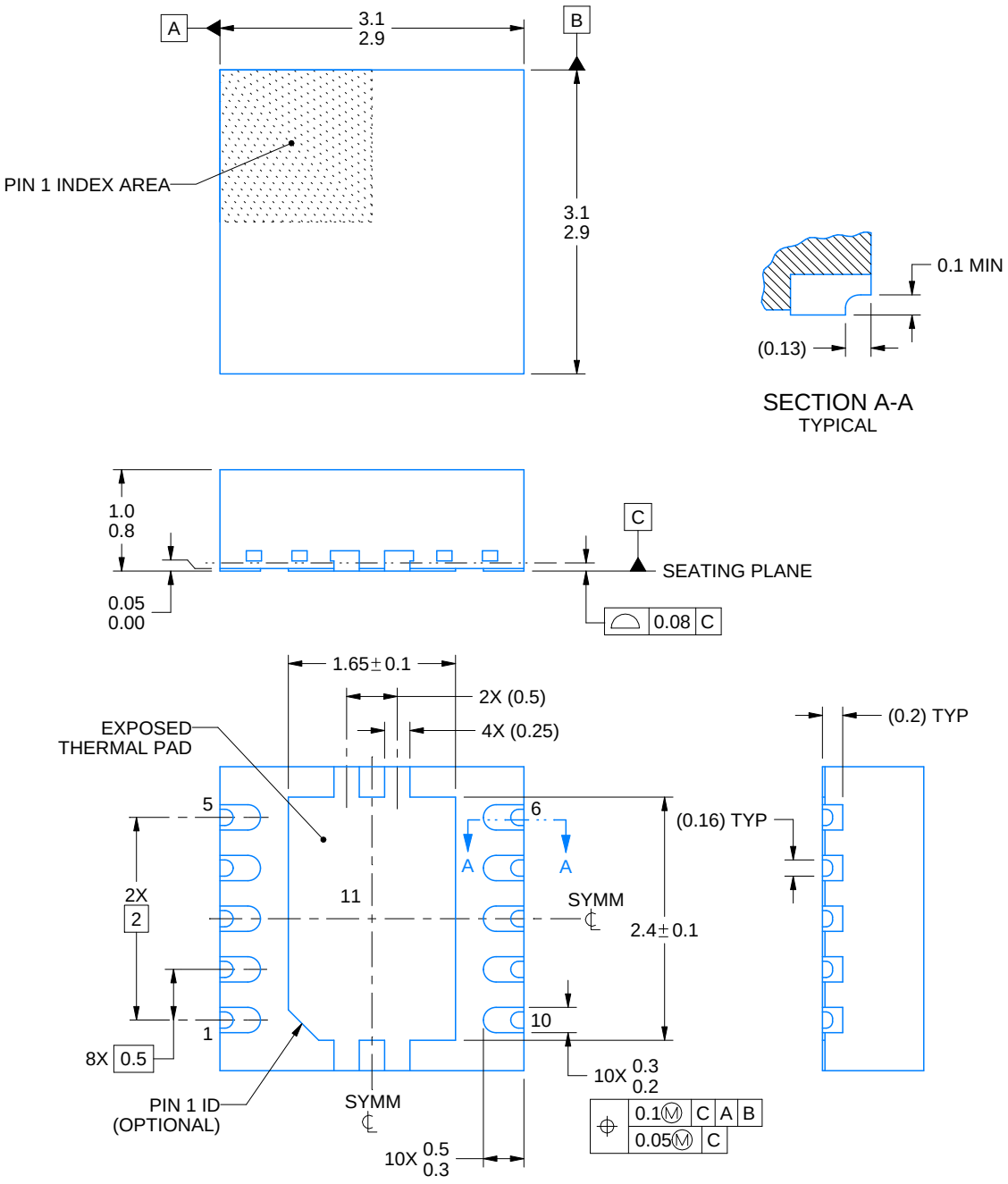
3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226193/A



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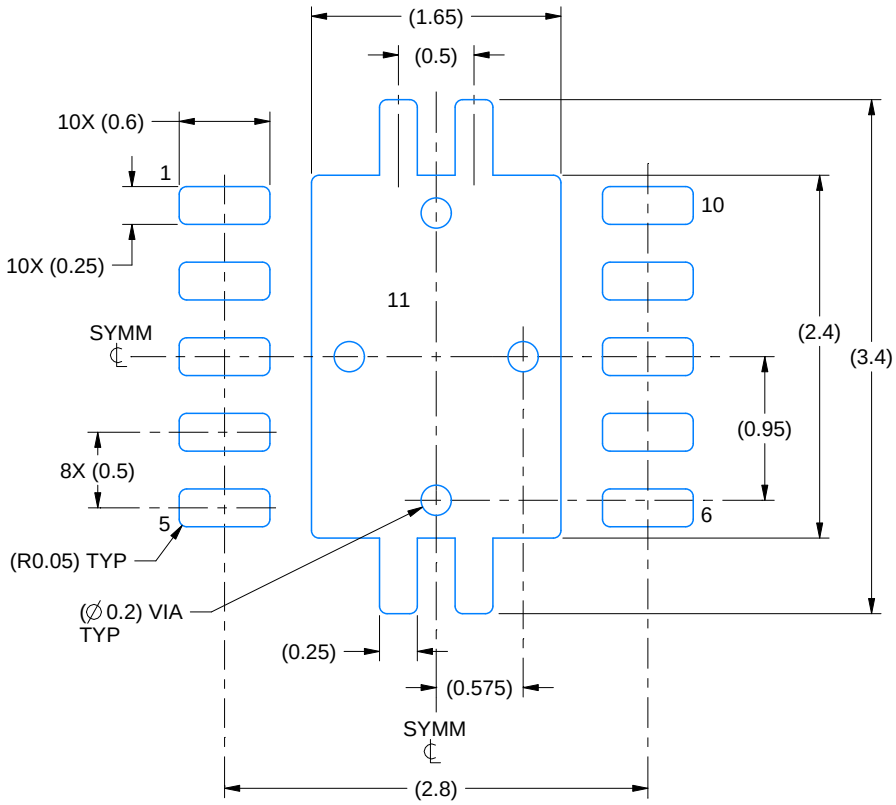
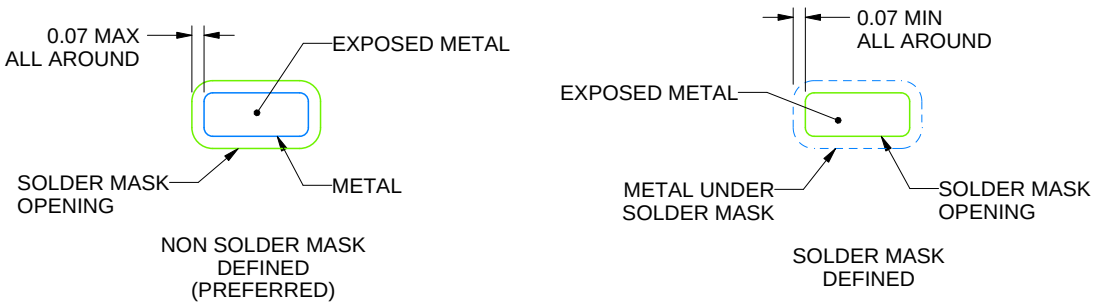


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4225163/A 07/2019

NOTES: (continued)

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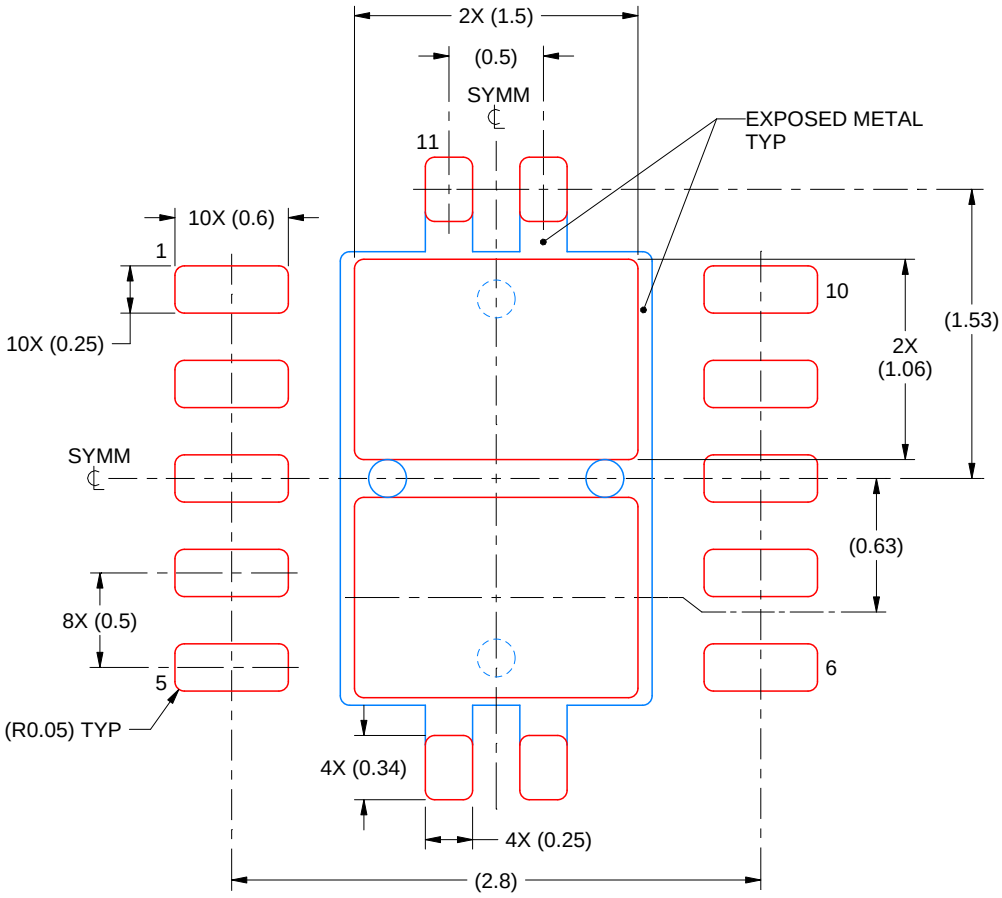

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4225163/A 07/2019

NOTES: (continued)

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