TEXAS INSTRUMENTS
TPS92830-Q1
JAJSE12A – OCTOBER 2017 – REVISED OCTOBER 2017

TPS92830-Q1 3チャネル、大電流のリニアLEDコントローラ

1 特長

- AEC-Q100認定済み
  - デバイス温度グレード1: 動作時周囲温度範囲 –40°C～125°C
  - デバイスHBM ESD分類レベルH2
  - デバイスCDM ESD分類レベルC4B
- **広い入力電圧範囲**: 4.5V～40V
- **3チャネルのハイサイド電流駆動およびセンシング**
  - チャネル独立の電流設定
  - チャネル独立のPWM入力
  - PWM入力および電源の両方によるPWM調光
  - EMCに対して最適化されたスルー・レート
- **高精度のLED駆動**
  - 外部NチャネルMOSFETによる高精度の電流レギュレーション(許容誤差2.5%)
  - 20:1のアナログ調光プロファイルとオフボードのビン抵抗サポート
  - 完全デューティ・サイクル・マスクを持つ高精度PWMジェネレータ(許容誤差2%)
  - オープン・ドレインのPWM出力による同期
- **保護および診断機能**
  - 外付けMOSFETの過熱保護用の可変出力電流ディレーティング
  - LEDストリングの開路または短絡の診断および自動回復機能
  - 診断イネーブルと可変スレッショルドによる低電圧動作
  - 最大15個のデバイスのフォルト・バス、どれか1つに障害が発生すれば全体を障害とするか、障害の発生したチャネルのみをオフにするかを選択可能
  - フォルト・モードでの低い静止電流(デバイスごとに0.75mA未満)
- **動作時の接合部温度範囲**: -40℃～150℃
- TSSOP 28パッケージ(PW)

2 アプリケーション

- **後方ライト - テール・ランプとストップ・ランプ、後方ウインカー、フォッグ・ランプ、バック・ランプ**
- **前方ライト - 位置灯、昼間走行灯、前方ウインカー、ロービーム**

3 概要

ライトの均一性が求められる傾向から、車載用の前方および後方ランプには多くの場合に大電流LEDが、拡散板や導光板とともに使用されます。その一方で、厳格なEMCおよび信頼性の要件に合致するため、リニアLEDドライバが車載用アプリケーションで多く使われています。しかし、リニアLEDドライバ用の大電流を内蔵のパワー・トランジスタで供給するのは困難です。TPS92830-Q1デバイスは、外付けのNチャネルMOSFETを使用して大電流を供給するための、高度な車載グレードのハイサイド定電流リニアLEDコントローラです。このデバイスには、車載用アプリケーション向けの完全な機能セットがあり、広範なNチャネルMOSFETと互換性があります。

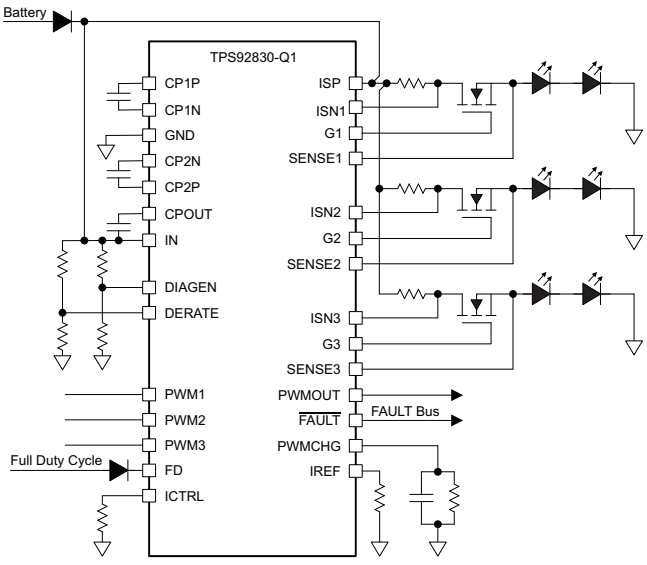
TPS92830-Q1デバイスの各チャネルは、センス抵抗の値により、独立にチャネル電流を設定します。内蔵の高精度定電流レギュレーション・ループは、センス抵抗の両端の電圧によってチャネルの電流を検出し、それに応じてNチャネルMOSFETのゲート電圧を制御します。このデバイスには、低ドロップアウト動作用の2段のチャージ・ポンプも内蔵されています。チャージ・ポンプの電圧は十分に高く、広範なNチャネル MOSFETをサポートできます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS92830-Q1	TSSOP (28)	9.70mm×4.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

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- 「*特長*」セクションで電流レギュレーションとPWMジェネレータの許容誤差を変更 ... 1
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- Changed parameter definitions for $I_{(DRV\_source)}$ and $I_{(DRV\_sink)}$ in the *Electrical Chaaracteristics* table ... 7
- Changed parameter symbols for analog dimming accuracy in the Electrical Characteristics table ... 8
- Changed parameter descriptions for $V_{(OPEN\_th\_rising)}$, $V_{(OPEN\_th\_falling)}$, ... 8
- Changed parameter descriptions for $t_{(SG\_retry\_OFF)}$ and $t_{(OPEN\_retry\_OFF)}$ in the *Timing Requirements* table ... 9
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- Deleted a *Fast Power Down and Slow Power Up* typical characteristic graph ... 12
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- Added resistor and capacitor reference designators ... 19
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- Changed symbol of short-to-ground retry current to $I_{(Retry\_short)}$ ... 26
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- Added an application curve 34
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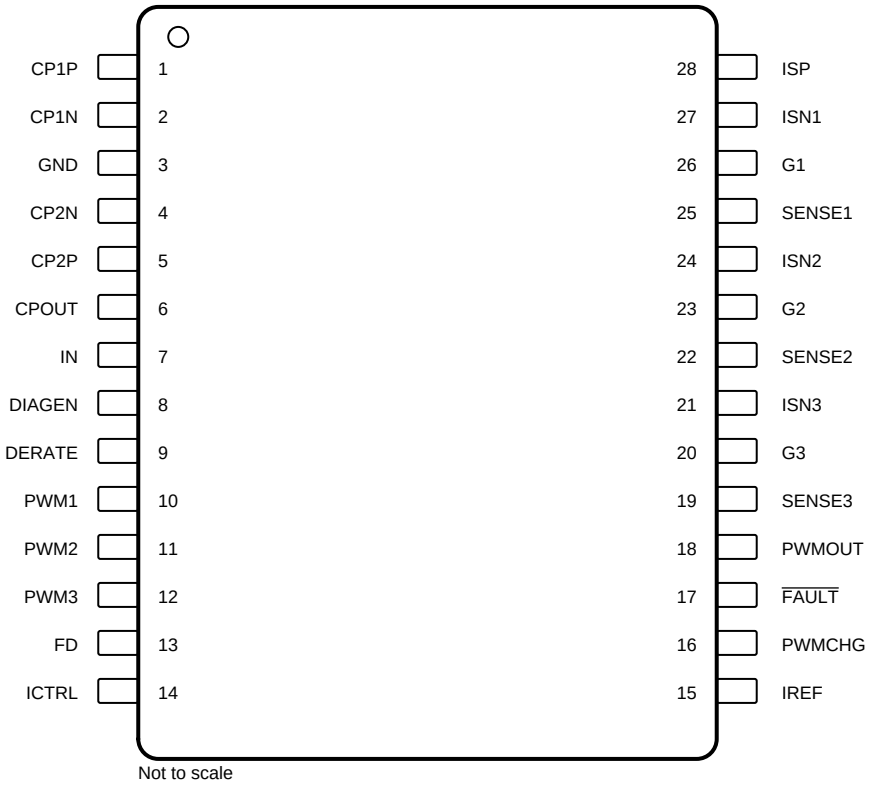
5 概要(続き)

PWM調光により、複数のソースとして内部PWMジェネレータ、外部PWM入力、または電源調光を柔軟に使用できます。車載アプリケーションに特化して設計された、各種の診断および保護機能により、システムはより堅牢で使いやすくなります。どれか1つに障害が発生すれば全体を障害とするフォルト・バスでは、TPS92830-Q1がTPS92630-Q1、TPS92638-Q1、およびTPS9261x-Q1ファミリとともに動作し、各種のフォルト処理要件を満たすことができます。

6 Pin Configuration and Functions

PW Package
28-Pin TSSOP
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CP1N	2	O	Charge pump first-stage flying capacitor negative output, charge pump to provide gate-drive voltage for external MOSFET. Connect a 10-nF flying capacitor between CP1P and CP1N.
CP1P	1	O	Charge pump first-stage flying capacitor positive output
CP2N	4	O	Charge pump second-stage flying capacitor negative output. Connect a 10-nF flying capacitor between CP2P and CP2N.
CP2P	5	O	Charge pump second-stage flying capacitor positive output
CPOUT	6	O	Charge-pump output voltage. Connect a 150-nF storage capacitor between CPOUT and IN.
DERATE	9	I	Voltage input for current derating. Connect to GND to disable the derate feature.
DIAGEN	8	I	Input pin with comparator to enable diagnostics to avoid false open-fault diagnostics when the device works in low-dropout mode. Use a resistor divider to set a threshold according to the LED forward voltage.
$\overline{\text{FAULT}}$	17	I/O	Fault bus pin to support one-fails–all-fail feature. Float: one-fails–all-fail; strong pullup: only-fails-off

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
FD	13	I	Full duty-cycle input, HIGH: 100% PWM; LOW: using external resistor-capacitor network to set PWM duty cycle
G1	26	O	Channel 1 gate driver output, connect to CH 1 N-channel MOSFET gate
G2	23	O	Channel 2 gate driver output, connect to CH 2 N-channel MOSFET gate
G3	20	O	Channel 3 gate driver output, connect to CH 3 N-channel MOSFET gate
GND	3	—	GND
ICTRL	14	I	Analog dimming input, modulates the regulation voltage across the current-sense resistor. Apply a voltage source or connect a resistor between ICTRL and GND to set the analog dimming ratio.
IN	7	I	Power supply for the device. LED current only flows from the external MOSFET to the LED.
ISN1	27	I	Channel 1 current-sense negative input. Connect a current-sense resistor between ISP and ISN1 to set the CH 1 current.
ISN2	24	I	Channel 2 current-sense negative input. Connect a current-sense resistor between ISP and ISN2 to set the CH 2 current.
ISN3	21	I	Channel 3 current-sense negative input. Connect a current-sense resistor between ISP and ISN3 to set the CH 3 current.
IREF	15	O	Internal current reference. Connect an 8-kΩ resistor between IREF and GND,
ISP	28	I	Channel current-sense positive input. Kelvin-sense to LED sense-resistor positive node.
PWM1	10	I	Channel 1 PWM input
PWM2	11	I	Channel 2 PWM input
PWM3	12	I	Channel 3 PWM input
PWMCHG	16	I/O	On-chip PWM generator pin for external R-C. Connect a resistor and a capacitor between PWMCHG and GND to set the PWM duty cycle and frequency.
PWMOUT	18	O	High-voltage PWM open-drain output. Connect a 10-kΩ resistor between IN and PWMOUT
SENSE1	25	I/O	Channel 1 diagnostics pin. Connect to the CH 1 MOSFET source terminal
SENSE2	22	I/O	Channel 2 diagnostics pin. Connect to the CH 2 MOSFET source terminal
SENSE3	19	I/O	Channel 3 diagnostics pin. Connect to the CH 3 MOSFET source terminal

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range T_J= –40°C to 150°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	IN(2)	–0.3	45(3)	V
Input voltage	DERATE, DIAGEN, FD, ICTRL, ISN1, ISN2, ISN3, ISP, PWM1, PWM2, PWM3, PWMOUT, SENSE1, SENSE2, SENSE3(2)	–0.3	$V_{(IN)}$ + 0.3	V
Output voltage	CP1P, CP2P, CPOUT, G1, G2, G3(2)	–0.3	$V_{(IN)}$ + 10	V
Current-sense voltage	$V_{(ISP)} – V_{(ISNx)}$	–0.3	1	V
Gate-source voltage	$V_{(Gx)} – V_{(SENSEx)}$	–1	12	V
I/O	$\overline{FAULT}$(2)	–0.3	22	V
	CP1N, CP2N, IREF, PWMCHG(2)	–0.3	6	V
Storage temperature, T_{stg}		–65	150	°C
Junction temperature, T_J		-40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND.
(3) Absolute maximum voltage 45 V for 200 ms.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	Corner pins (CP1P, ICTRL, IREF, ISP)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating junction temperature range T_J= –40°C to 150°C (unless otherwise noted)

		MIN	MAX	UNIT
Device supply voltage	IN	4.5	40	V
Sense voltage	ISP	0	$V_{(IN)}$	V
PWM inputs	PWMx	0	$V_{(IN)}$	V
Diagnostics enable pin	DIAGEN	0	$V_{(IN)}$	V
Current-sense voltage	$V_{(ISP)} – V_{(ISNx)}$	0	1	V
Fault bus	$\overline{FAULT}$	0	20	V
PWM open-drain output	PWMOUT	0	$V_{(IN)}$	V
Analog dimming input	ICTRL	0	$V_{(IN)}$	V
Current derating input	DERATE	0	$V_{(IN)}$	V
Full duty-cycle input	FD	0	$V_{(IN)}$	V

7.4 Thermal Information

THERMAL METRIC[1]		TPS92830-Q1 PW (TSSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	79.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

7.5 Electrical Characteristics

V_{IN} = 5 V to 40 V, V_{ICTRL} = 3 V, V_{DERATE} = 0 V, T_J = –40°C to 150°C,[1] (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS						
$V_{(POR\_rising)}$	Supply voltage POR, rising threshold				4.5	V
$I_{(Quiescent)}$	Device standby current	PWMx = HIGH, FD = HIGH		3.5		mA
$I_{(FAULT)}$	Device current in fault mode	PWMx = HIGH, $\overline{FAULT}$ = LOW		0.5	0.75	mA
$I_{(IREF)}$	Reference current	$R_{(IREF)}$ = 8 kΩ		99		µA
$C_{(IREF)}$	IREF loading capacitance	$R_{(IREF)}$ = 8 kΩ	0		4.3	nF
CHARGE PUMP						
$V_{(cp\_drv)}$	Charge-pump operating voltage		6.1	8.5	10	V
$f_{(cp\_sw)}$	Charge-pump switching frequency			2.65		MHz
$C_{(cp\_flying)}$	Charge-pump flying capacitor			10		nF
$C_{(cp\_storage)}$	Charge-pump storage capacitor			150		nF
HIGH-PRECISION LOGIC INPUTS (DIAGEN, PWMx, FD)						
$V_{IL(DIAGEN)}$	Input logic-low voltage, DIAGEN		1.105	1.145	1.185	V
$V_{IH(DIAGEN)}$	Input logic-high voltage, DIAGEN		1.193	1.224	1.255	V
$V_{IL(PWMx)}$	Input logic-low voltage, PWMx		1.094	1.128	1.161	V
$V_{IH(PWMx)}$	Input logic-high voltage, PWMx		1.176	1.212	1.248	V
$V_{IL(FD)}$	Input logic-low voltage, FD		1.105	1.133	1.161	V
$V_{IH(FD)}$	Input logic-high voltage, FD		1.186	1.216	1.246	V
CONSTANT-CURRENT EXTERNAL N-CHANNEL MOSFET DRIVER						
$V_{(CS\_REG\_FULL)}$	Current-sense-resistor regulation voltage	$V_{(ICTRL)}$ = 3 V, $V_{(DERATE)}$ = 0 V		295		mV
$\Delta V_{(CS)}$[2][3]	Current-sense-resistor regulation-voltage accuracy	$V_{(ICTRL)}$ = 3 V, $V_{(DERATE)}$ = 0 V, channel accuracy	–1.5%		1.5%	
		$V_{(ICTRL)}$ = 3 V, $V_{(DERATE)}$ = 0 V, device accuracy	–2.5%		2.5%	
$I_{(DRV\_source)}$	Gate-driver current-source capability at Gx		190	230	270	µA

(1) External N-channel MOSFET C_{iss} = 200 pF, C_{oss} = 70 pF, at V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1 MHz, V_{th} = 4 V, compensation capacitor C_{gs} = 4 nF

(2) $$\Delta V_{(CS\_Channel\_CHx)} = 1 - \frac{3 \times V_{(CS\_REG\_x)}}{\left(V_{(CS\_REG\_1)} + V_{(CS\_REG\_2)} + V_{(CS\_REG\_3)}\right)}, x = 1,2,3$$

(3) $$\Delta V_{(CS\_Device\_CHx)} = 1 - \frac{V_{(CS\_REG\_x)}}{0.295}, x = 1,2,3$$

Electrical Characteristics (continued)

V_{IN} = 5 V to 40 V, V_{ICTRL} = 3 V, V_{DERATE} = 0 V, T_J= –40°C to 150°C,(1) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(DRV\_sink)}$	Gate-driver current-sink capability at Gx		190	230	270	µA
$V_{(GS\_clamp\_neg)}$	Gate-source negative clamp voltage		–0.9	–0.7	–0.5	V
$V_{(GS\_clamp\_pos)}$	Gate-source positive clamp voltage		9.8	10.4	11.3	V
$I_{(ISNx\_leakage)}$	Leakage current sink on ISNx pins			1.3	2.3	µA
INTERNAL PWM DIMMING						
$V_{(PWMCHG\_th\_rising)}$	Internal PWM generator, rising threshold		1.45	1.48	1.51	V
$V_{(PWMCHG\_th\_falling)}$	Internal PWM generator, falling threshold		0.78	0.8	0.82	V
$V_{(PWMCHG\_th\_hys)}$	Internal PWM generator hysteresis			0.68		V
$I_{(PWMCHG)}$	PWM generator pullup current	$V_{(PWMCHG)}$ = 0 V, FD = LOW	194	200	206	µA
$V_{OL(PWMOUT)}$	Open-drain PWMOUT pulldown voltage	$V_{(PWMCHG)}$ = 3 V, $I_{(PWMOUT)}$ pullup current = 4 mA			0.4	V
$r_{DS(on)(PWMOUT)}$	Open-drain PWMOUT pulldown MOSFET $r_{DS(on)}$		40	55	90	Ω
ANALOG DIMMING						
$V_{(ICTRL\_FULL)}$	Full-range ICTRL voltage				1.65	V
$V_{(ICTRL\_LIN\_TOP)}$	Upper boundary for linear ICTRL dimming			1.425		V
$V_{(ICTRL\_LIN\_BOT)}$	Lower boundary for linear ICTRL dimming			75		mV
$\Delta V_{(CS\_ICTRL\_H)}$	Analog dimming accuracy	$V_{(ICTRL)}$ = 1.35 V, $V_{(DERATE)}$ = 0 V, accuracy: 1 – ($V_{(CS\_REG\_x)}$ / 0.27), x = 1, 2, 3	–2.5%		2%	
$\Delta V_{(CS\_ICTRL\_M)}$	Analog dimming accuracy	$V_{(ICTRL)}$ = 0.75 V, $V_{(DERATE)}$ = 0 V, accuracy: 1 – ($V_{(CS\_REG\_x)}$ / 0.15), x = 1, 2, 3	–4%		4%	
$\Delta V_{(CS\_ICTRL\_L)}$	Analog dimming accuracy	$V_{(ICTRL)}$ = 0.15 V, $V_{(DERATE)}$ = 0 V, accuracy: 1 –$V_{(CS\_REG\_x)}$ / 0.03, x = 1, 2, 3	–18%		18%	
$I_{(ICTRL\_pullup)}$	ICTRL internal pullup current		0.95	0.985	1.02	mA
CURRENT DERATING						
$V_{(DERATE\_FULL)}$	Full-range DERATE voltage			1.83		V
$V_{(DERATE\_HALF)}$	Half-range DERATE voltage			2.38		V
$K_{(DERATE)}$	Derate dimming ratio	$V_{(DERATE)}$ = 1.966 V	81%	87%	95%	
		$V_{(DERATE)}$ = 2.316 V	51%	58%	65%	
DIAGNOSTICS						
$V_{(OPEN\_th\_rising)}$	LED open rising threshold, device triggers open-circuit diagnostics $V_{(SG\_th\_rising)}$, and $V_{(SG\_th\_falling)}$ in the *Electrical Characteristics* table	$V_{(ISNx)}$ – $V_{(SENSEx)}$, x = 1, 2, 3	100	145	190	mV
$V_{(OPEN\_th\_falling)}$	LED open falling threshold, device releases from open-circuit diagnostics	$V_{(ISNx)}$ – $V_{(SENSEx)}$, x = 1, 2, 3	240	280	320	mV
$V_{(OPEN\_th\_hyst)}$				135		mV
$I_{(Retry\_open)}$	LED-open retry current		8	10	12	mA

Electrical Characteristics (continued)

V_{IN} = 5 V to 40 V, V_{ICTRL} = 3 V, V_{DERATE} = 0 V, T_J= –40°C to 150°C,(1) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SG\_th\_rising)}$	Channel output V_{SENSEx} short-to-ground rising threshold, device triggers short-to-ground diagnostics		0.885	0.92	0.95	V
$V_{(SG\_th\_falling)}$	Channel output V_{SENSEx} short-to-ground falling threshold, device releases from short-to-ground diagnostics		1.17	1.215	1.26	V
$V_{(SG\_th\_hyst)}$	Channel output V_{SENSEx} short-to-ground hysteresis			295		mV
$I_{(Retry\_short)}$	Channel output V_{SENSEx} short-to-ground retry current		0.75	1	1.25	mA
$\overline{FAULT}$						
$V_{IL(FAULT)}$	Logic-input low threshold				0.7	V
$V_{IH(FAULT)}$	Logic-input high threshold		2			V
$V_{OL(FAULT)}$	Logic-output low threshold	With 500-µA external pullup			0.4	V
$V_{OH(FAULT)}$	Logic-output high threshold	With 1-µA external pulldown	2.7		3.4	V
$I_{(FAULT\_pulldown)}$	$\overline{FAULT}$ internal pulldown current		650	750	800	µA
$I_{(FAULT\_pullup)}$	$\overline{FAULT}$ internal pullup current		6.5	7.6	9.5	µA
THERMAL PROTECTION						
$T_{(TSD)}$	Thermal shutdown threshold			176		ºC
$T_{(TSD\_HYS)}$	Thermal shutdown hysteresis			15		ºC

7.6 Timing Requirements

		MIN	NOM	MAX	UNIT
$t_{(OPEN\_deg)}$	LED open-circuit deglitch time, described in LED open-circuit diagnostics section	100	125	150	µs
$t_{(SG\_deg)}$	LED short-to-GND detection deglitch time, described in the LED short-to-GND diagnostics section	100	125	150	µs
$t_{(SG\_retry\_ON)}$	Channel output SENSEx short-to-ground retry on-time, described in the LED short-to-GND auto retry section	100	125	150	µs
$t_{(SG\_retry\_OFF)}$	Channel output SENSEx short-to-ground retry off-time, described in LED short-to-GND auto retry section		10.8		ms
$t_{OPEN\_retry\_ON)}$	Channel output SENSEx open-circuit retry on-time	100	125	150	µs
$t_{(OPEN\_retry\_OFF)}$	Channel output SENSEx open-circuit retry off-time		10.8		ms
$D_{(PWM\_50)}$	PWM generated internally, nominal 50% duty cycle, as measured on output channel; see 図 1	49.6%	50%	50.4%	
$t_{d(DERATE)}$	Derate current-response delay time when DERATE steps from 1.8 V to 2.4 V		25		µs
$t_{(CP\_STARTUP)}$	$V_{(IN)}$ = 14 V, Cs = 150 nF, CPOUT voltage reaches 18 V as shown in *Device Start-Up Delay diagram*		25		µs
$f_{(DRV\_PWM)}$	Recommended PWM driving-frequency range			2000	Hz

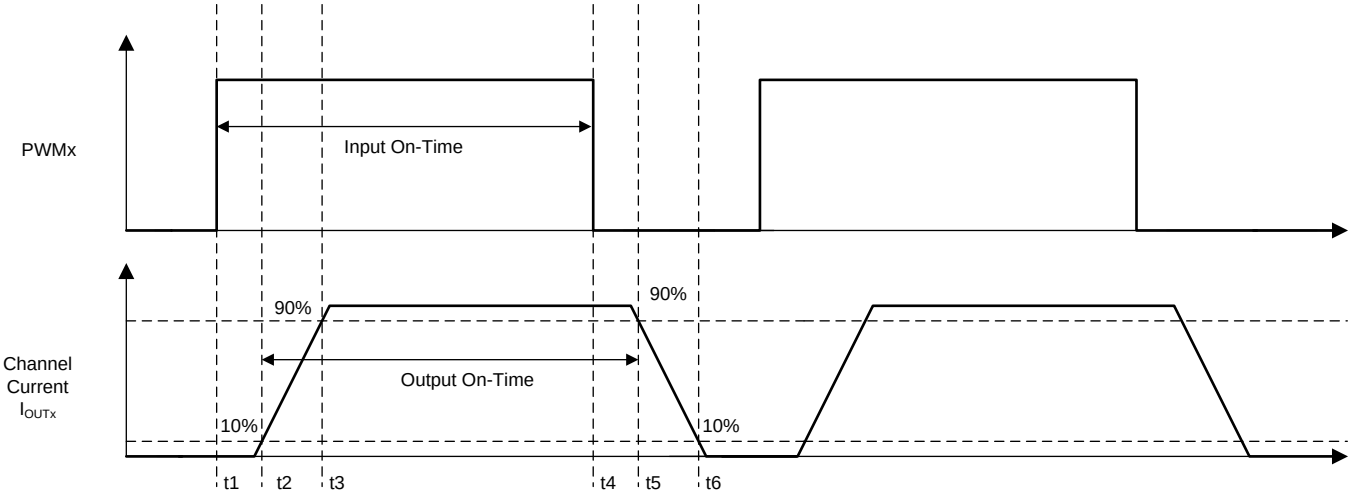
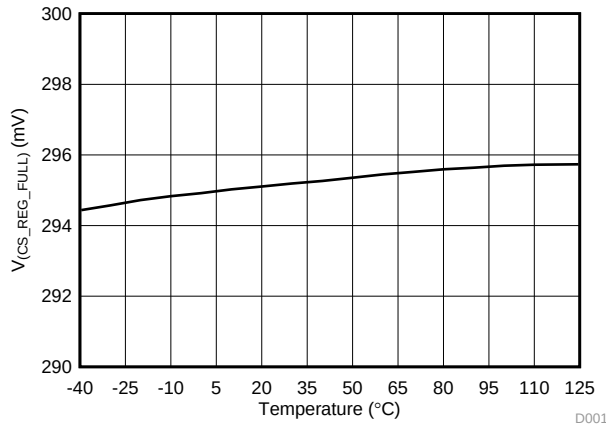


図 1. Channel-Current Output Timing Diagram

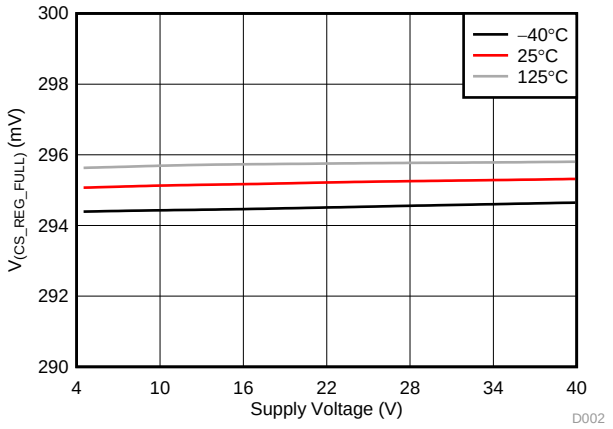
7.7 Typical Characteristics

T_A = 25 ºC unless otherwise noted



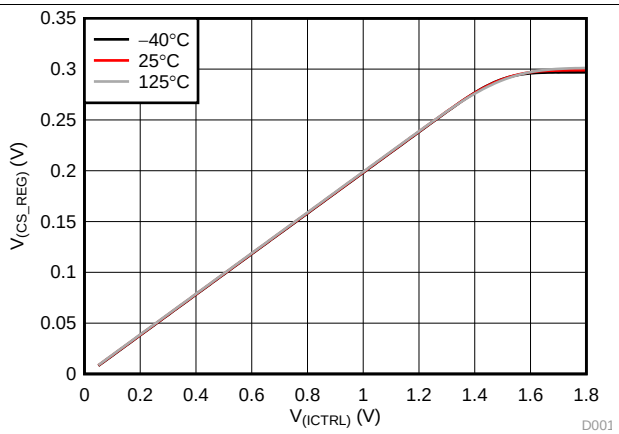
$V_{(IN)}$ = 14 V $V_{(ICTRL)}$ = 1.8 V

図 2. Full-Range Current-Sense Voltage vs Ambient Temperature



$V_{(ICTRL)}$ = 1.8 V

図 3. Full-Range Current-Sense Voltage vs Supply Voltage



$V_{(IN)}$ = 14 V

図 4. Current-Sense Voltage vs ICTRL Input Voltage

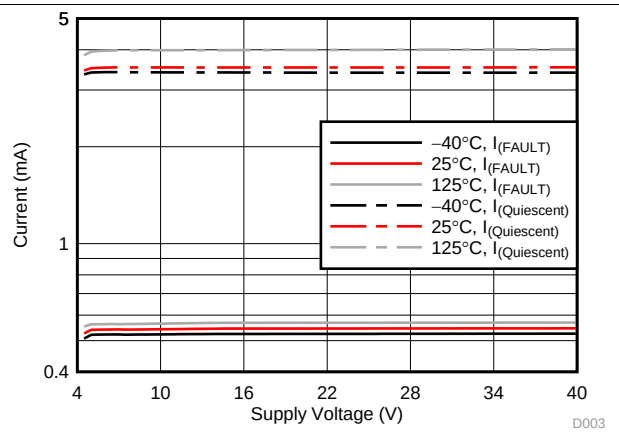
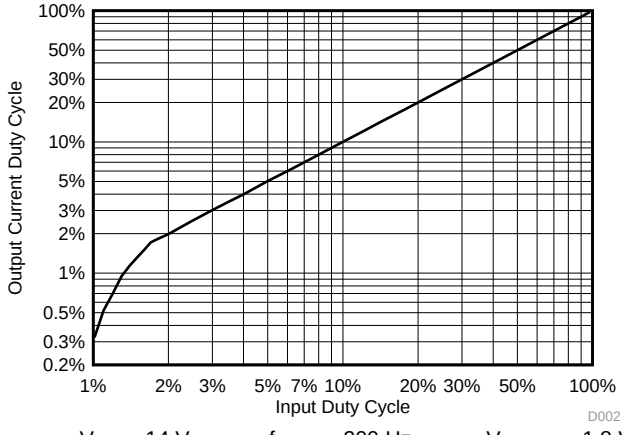
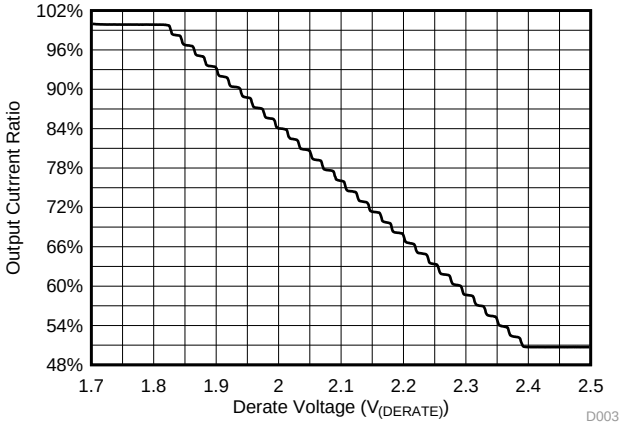


図 5. Device Current vs Supply Voltage



$V_{(IN)}$ = 14 V $f_{(PWM)}$= 200 Hz $V_{(ICTRL)}$ = 1.8 V

図 6. Duty Cycle of PWM Dimming-Current Output vs PWM Input Duty Cycle

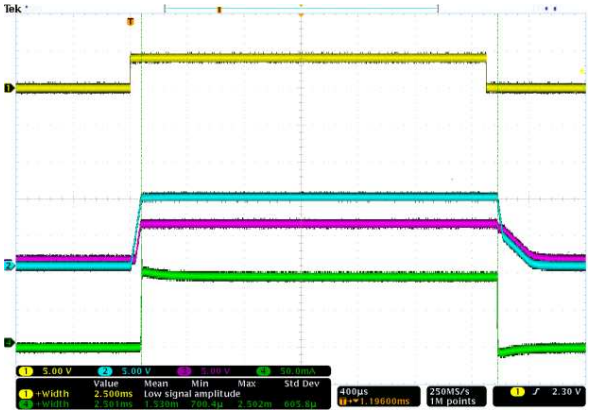


$V_{(IN)}$ = 14 V

図 7. Current-Derating Profile; Output-Current Ratio vs DERATE Voltage

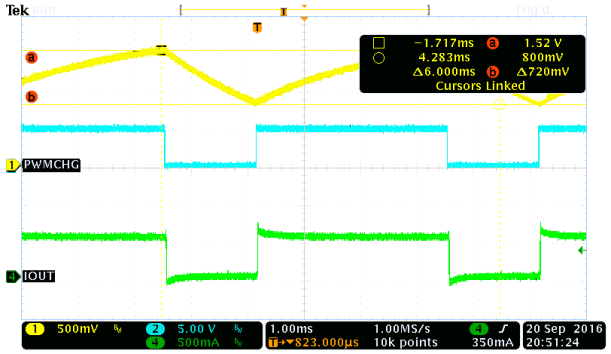
Typical Characteristics (continued)

T_A = 25 ºC unless otherwise noted



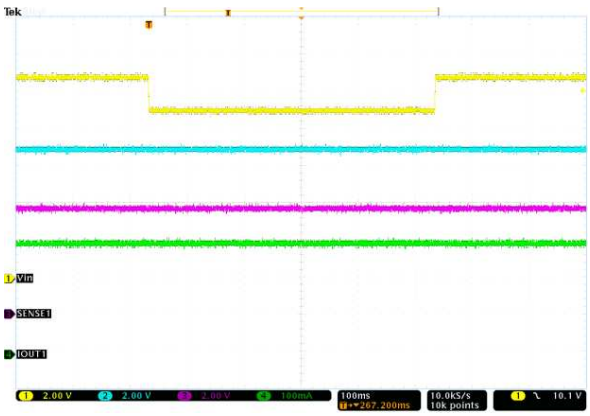
Ch. 1 = PWM1 Ch. 2 = G1 Ch. 3 = SENSE1
Ch. 4 = $I_{(OUT1)}$ $V_{(IN)}$ = 14 V

図 8. PWM Dimming



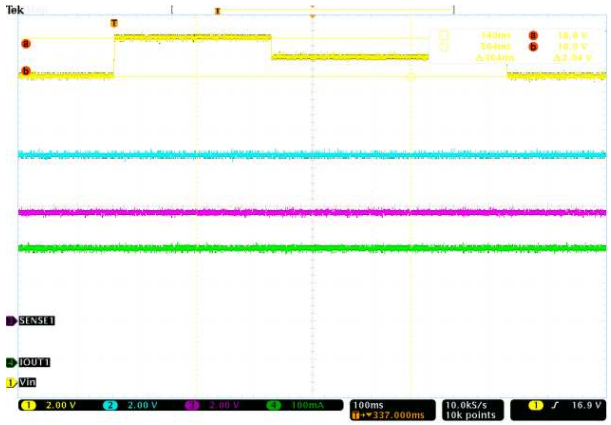
Ch. 1 = PWMCHG Ch. 2 = PWMOUT Ch. 4 = $I_{(OUT1)}$
$V_{(IN)}$ = 14 V

図 9. PWM Generator



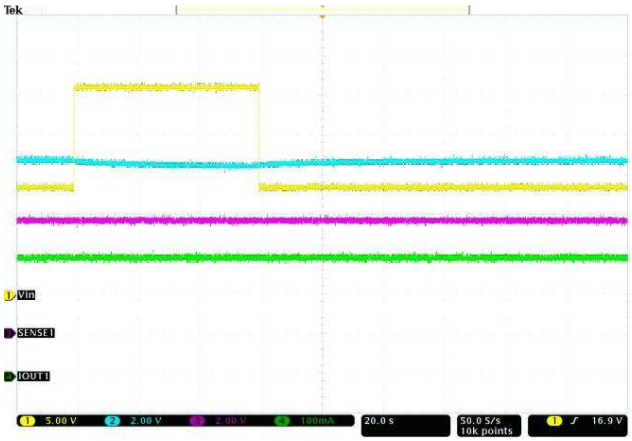
Ch. 1 = $V_{(IN)}$ Ch. 2 = G1 Ch. 3 = SENSE1
Ch. 4 = $I_{(OUT1)}$

図 10. Undervoltage



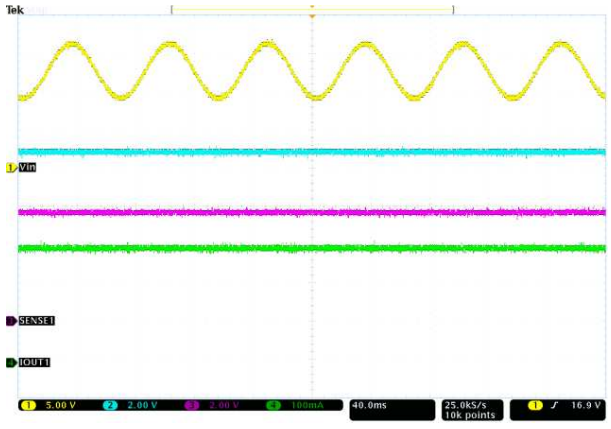
Ch. 1 = $V_{(IN)}$ Ch. 2 = G1 Ch. 3 = SENSE1
Ch. 4 = $I_{(OUT1)}$

図 11. Transient Overvoltage



Ch. 1 = $V_{(IN)}$ Ch. 2 = G1 Ch. 3 = SENSE1
Ch. 4 = $I_{(OUT1)}$

図 12. Jump Start

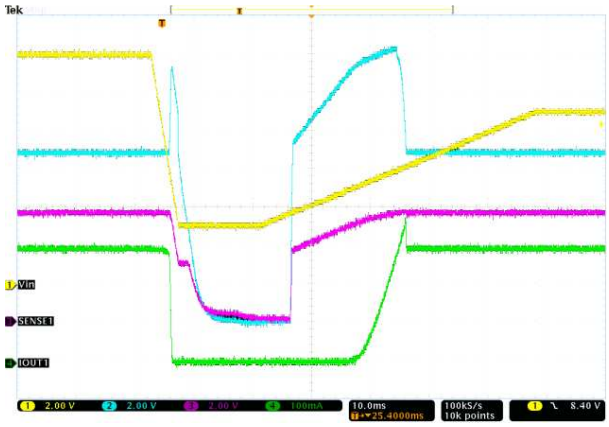


Ch. 1 = $V_{(IN)}$ Ch. 2 = G1 Ch. 3 = SENSE1
Ch. 4 = $I_{(OUT1)}$ f = 15 Hz

図 13. Superimposed Alternating Voltage

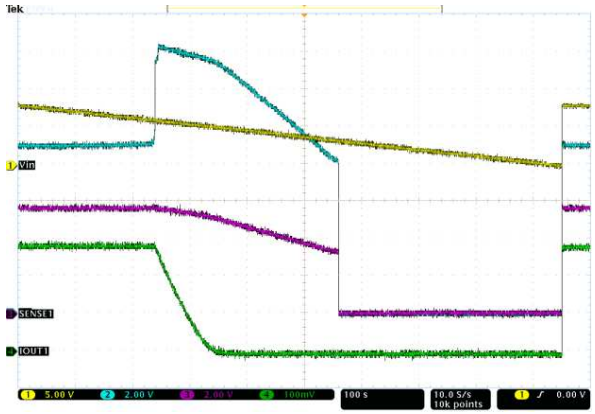
Typical Characteristics (continued)

T_A = 25 ºC unless otherwise noted



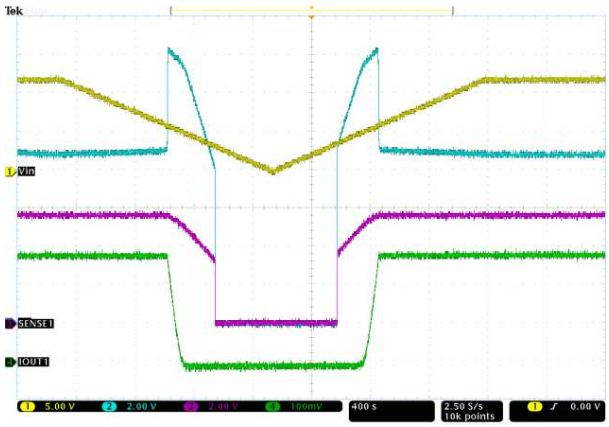
Ch. 1 = $V_{(IN)}$ Ch. 2 = G1 Ch. 3 = SENSE1
Ch. 4 = $I_{(OUT1)}$

図 14. Fast Power Down and Slow Power Up



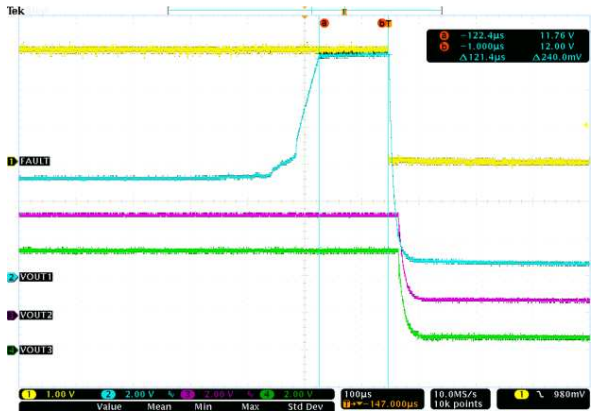
Ch. 1 = $V_{(IN)}$ Ch. 2 = G1 Ch. 3 = SENSE1
Ch. 4 = $I_{(OUT1)}$

図 15. Slow Decrease, Quick Increase of Supply Voltage



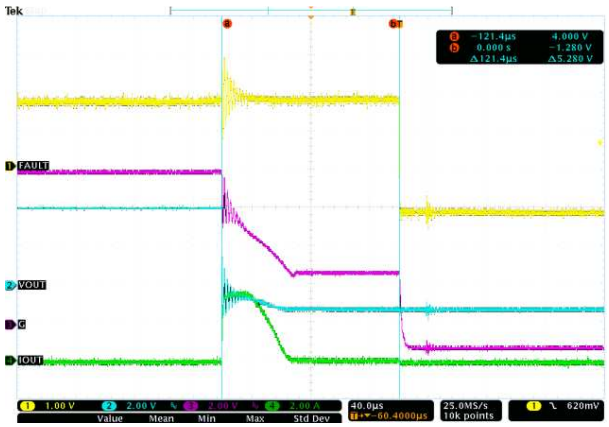
Ch. 1 = $V_{(IN)}$ Ch. 2 = G1 Ch. 3 = SENSE1
Ch. 4 = $I_{(OUT1)}$

図 16. Slow Decrease and Slow Increase of Supply Voltage



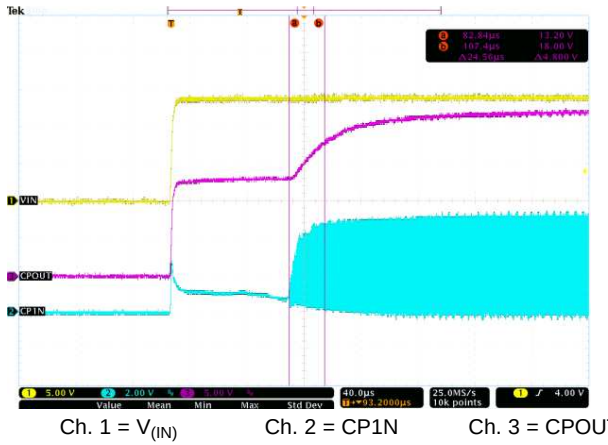
Ch. 1 = FAULT Ch. 2 = SENSE1 Ch. 3 = SENSE2
Ch. 4 = SENSE3 LED open-circuit on SENSE1

図 17. LED Open-Circuit Protection and One-Fails–All-Fail



Ch. 1 = FAULT Ch. 2 = SENSE1 Ch. 3 = G1
Ch. 4 = $I_{(OUT1)}$ LED short-to-ground on SENSE1

図 18. LED Hard Short Protection and One-Fails–All-Fail



Ch. 1 = $V_{(IN)}$ Ch. 2 = CP1N Ch. 3 = CPOUT

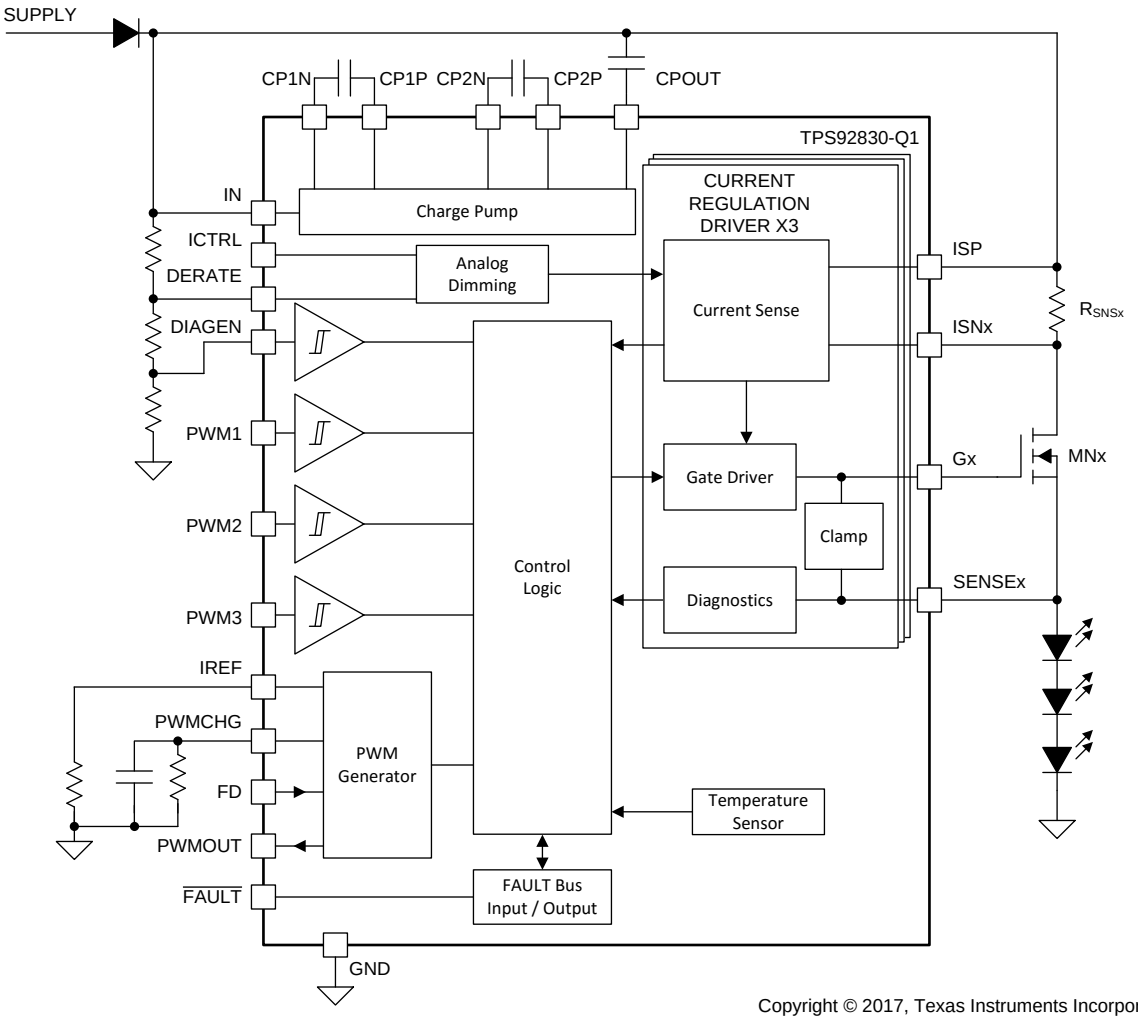
図 19. Device Start-Up Delay

8 Detailed Description

8.1 Overview

The TPS92830-Q1 device is an advanced automotive-grade high-side constant-current linear LED controller for delivering high current using external N-channel MOSFETs. The device has a full set of features for automotive applications. Each channel of the TPS92830-Q1 device sets the channel current independently by the sense-resistor value. An internal precision constant-current regulation loop senses the channel current by the voltage across the sense resistor and controls the gate voltage of the N-channel MOSFET accordingly. The device also integrates a two-stage charge pump for low-dropout operation. The charge-pump voltage is high enough to support a wide selection of N-channel MOSFETs. PWM dimming allows multiple sources for flexibility—internal PWM generator, external PWM inputs, or power-supply dimming. Various diagnostics and protection features specially designed for automotive applications help improve system robustness and ease of use. A one-fails–all-fail fault bus supports TPS92830-Q1 operation together with the TPS92630-Q1, TPS92638-Q1, and TPS9261x-Q1 family to fulfill various fault-handling requirements.

8.2 Functional Block Diagram



8.3 Feature Description

The TPS92830-Q1 device uses IN voltage to generate device bias. A two-stage charge pump provides gate driving voltage above the IN voltage for the high-side N-channel MOSFET. Each channel current is independently set by sense resistors. The analog-dimming ICTRL input supports off-board resistors as bin-setting resistors as well as direct voltage input. An integrated precision PWM generator could be used for PWM dimming locally.

8.3.1 Device Bias

The TPS92830-Q1 device has internal bias-generation and power-on-reset circuits for internal bias.

8.3.1.1 Power-On-Reset (POR)

The TPS92830-Q1 device has an internal power-on-reset (POR) function. When power is applied to IN, the internal POR holds the device in the reset condition until V_{IN} reaches $V_{(POR\_rising)}$.

When the supply rises above POR threshold $V_{(POR\_rising)}$, the charge pump starts working. The maximum gate-drive voltage is determined by the charge-pump voltage between CPOUT and IN.

8.3.1.2 Current Reference (IREF)

The TPS92830-Q1 device has a constant reference-voltage output on the IREF pin and uses current $I_{(IREF)}$ as the internal current reference. The analog-dimming internal-pullup current on ICTRL, and the PWM-generator internal charge current on PWMCHG, use $I_{(IREF)}$ as a reference current. The recommended value of reference resistor $R_{(IREF)}$ for IREF is 8 kΩ.

8.3.1.3 Low-Current Fault Mode

The TPS92830-Q1 device consumes minimal quiescent current when it is in fault mode. If the $\overline{FAULT}$ voltage is pulled low either by internal diagnostics or externally, the device performs as follows:

- The charge pump is shut down.
- All drivers are turned off with their gates internally pulled down.
- The PWM generator and PWMOUT are turned off.
- IREF current is turned off.
- ICTRL current is turned off.

8.3.2 Charge Pump

8.3.2.1 Charge Pump Architecture

The TPS92830-Q1 device uses a two-stage charge pump to generate the high-side gate-drive voltage. The charge pump is a voltage tripler using external flying and storage capacitors.

C_{P1} is the first-stage flying capacitor, connected between CP1P and CP1N, which are the positive and negative nodes, respectively. C_{P2} is the second-stage flying capacitor, connected between CP2P and CP2N, which are the positive and negative nodes, respectively. C_S is the storage capacitor, connected between CPOUT and IN. C_S stores charge for the high-side gate driver.

The charge pump switches at frequency $f_{(cp\_sw)}$ to optimize EMI performance.

Negative nodes CP1N and CP2N are driven by a 5-V driver, thus the maximum voltage on charge-pump output node CPOUT is approximately $V_{(IN)} + V_{(CP\_drv)}$. The charge pump voltage across storage capacitor C_S is not dependent on $V_{(IN)}$.

Feature Description (continued)

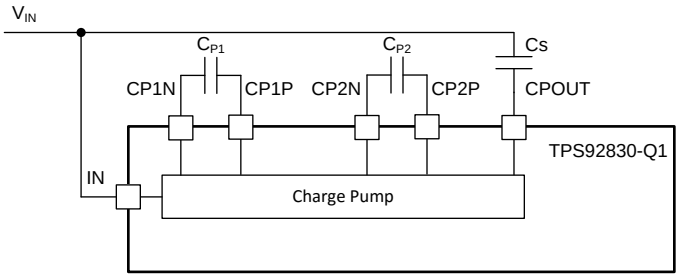


図 20. Charge Pump

8.3.3 Constant-Current Driving

The TPS92830-Q1 device has three independent constant-current driving channels. Each channel sets channel current with an external high-side current-sense resistor, R_{SNSx}. Channel current is set as $V_{(CS\_REG)}$ / R_{SNSx}.

Considering that both ICTRL and DERATE voltages reduce current-sense voltage $V_{(CS\_REG)}$ independently, channel current can be calculated using the following equation. Each of the dimming ratios is described separately in following sections.

$$I_{(CHx)} = \frac{V_{(CS\_REG\_FULL)} \times k_{(ICTRL\_DIM)} \times k_{(DERATE\_DIM)}}{R_{SNSx}} \quad (1)$$

8.3.3.1 High-Side Current Sense

The sense voltage across external current-sense resistor R_{SNSx} feeds back current information to the controller. An internal feedback control loop within the TPS92830-Q1 device regulates the external gate-overdrive voltage of the N-channel MOS transistor to keep the sense voltage at the desired level. By setting the external current-sense resistance value, the output current can be set individually on each channel.

8.3.3.2 High-Side Current Driving

To regulate the output current, the gate-source voltage of the external MOSFET must be regulated accordingly. The constant-current source is used to charge and discharge the N-channel MOSFET gate. During the current-slewing period, constant-current sourcing and sinking ensures the smooth slewing of the output current. The control loop requires sufficient MOSFET gate capacitance to ensure loop stability. In case the MOSFET gate capacitance is insufficient, a capacitor C_{GS} must be added across Gx and SENSEx. TI also recommends always putting a C_{SENSE} of 10 nF from each of the SENSEx pins to GND, and close to the device for EMC.

When a channel is switched on, current source $I_{(DRV\_source)}$ charges the gate of the external N-channel MOSFET. When a channel is switched off, current sink $I_{(DRV\_sink)}$ discharges the gate of the external MOSFET transistor down to ground.

Feature Description (continued)

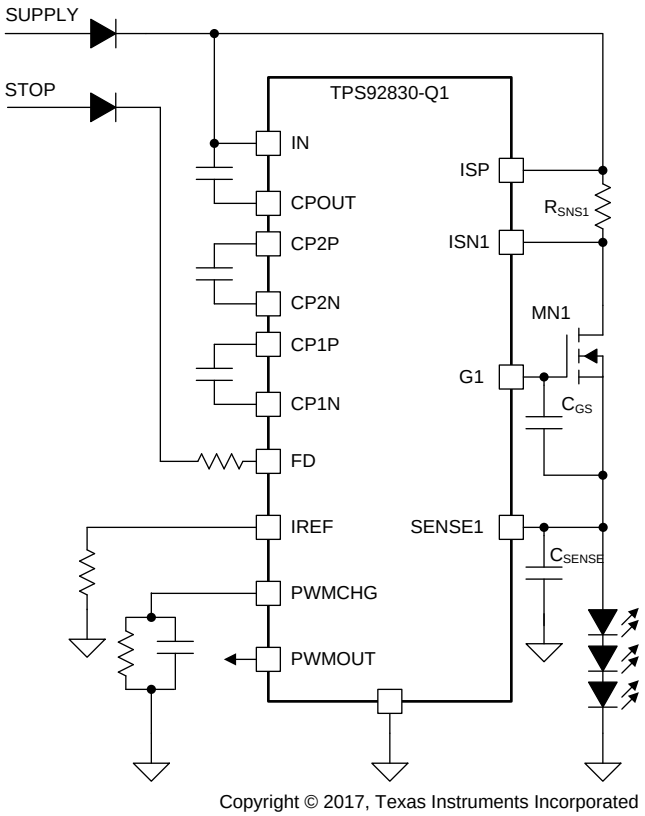


図 21. MOSFET Gate Capacitance Compensation

8.3.3.3 Gate Overdrive Voltage Protection

A bidirectional clamp is used to protect the gate-source path of the external N-channel MOSFETs from overstress conditions. Gate-source voltage $V_{(GS)}$ is clamped between $V_{(GS\_clamp\_neg)}$ and $V_{(GS\_clamp\_pos)}$ for MOSFET protection.

8.3.3.4 High-Precision Current Regulation

The TPS92830-Q1 device has a high-precision current-regulation loop. Its precision is at the maximum when the voltage across the current-sense resistor is set to maximum. The analog-dimming or current-derating function reduces the current-sense voltage, thus decreasing current-regulation accuracy.

8.3.3.5 Parallel MOSFET Driving

The TPS92830-Q1 device is designed to support parallel N-channel MOSFETs driving within the same channel. To balance heat dissipation, multiple MOSFETs could be paralleled together. A ballast resistor for each MOSFET is recommended to balance current distribution among parallel MOSFETs.

Larger variation on threshold mismatches requires larger ballast resistors. $V_{(TH\_MISMATCH)}$ is the threshold for mismatches within the same batch of MOSFETs. $I_{(CH\_MISMATCH)}$ is the allowed mismatch current between the parallel channels. Typically, $I_{(CH\_MISMATCH)}$ can be set to 10% of full-range current. The ballast resistor value is set as calculated in the following equation.

$$R_{(Ballast)} = \frac{V_{(TH\_MISMATCH)}}{I_{(CH\_MISMATCH)}} \quad (2)$$

The ballast resistor typically ranges from hundreds of milliohms to several ohms depending on the channel current and MOSFET threshold-voltage variations.

Feature Description (continued)

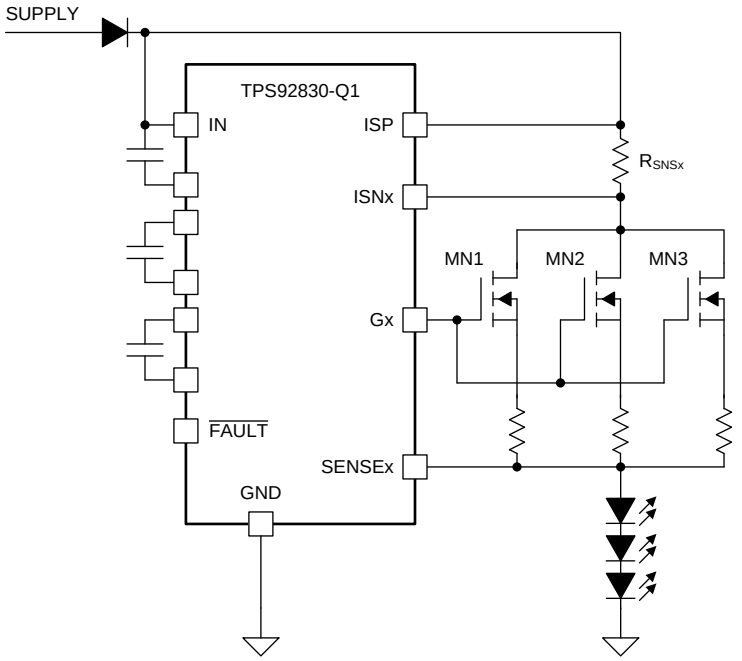


図 22. Parallel MOSFET Driving

8.3.4 PWM Dimming

The TPS92830-Q1 device supports a variety of PWM dimming methods, including PWM supply dimming, external PWM dimming by inputs, and internal PWM dimming by the internal PWM generator. Each PWM cycle should allow enough positive cycle time for gate charging and enough negative cycle time for gate discharging in order to achieve an accurate PWM dimming duty cycle.

8.3.4.1 Supply Dimming

In the case of supply dimming, the supply of the whole LED driver module is PWM dimmed, for example by body-control-module (BCM) high-side switches. The TPS92830-Q1 device supports supply dimming with a short power-on delay. Device supply V_{IN} should be always equal to $V_{(ISP)}$ to ensure that the charge pump voltage is high enough to turn on the MOSFET.

When supply dimming is used, it is recommended to be used together with PWM input, so that the channel is only turned on when the input voltage is above the device UVLO threshold. By keeping enough delay time between device power up and channel turnon, output current spikes can be avoided to ease EMC design.

8.3.4.2 PWM Dimming by Input

Each channel has individual PWM dimming by inputs.

The internal thresholds for PWM1–PWM3 are designed with high precision. With external resistor dividers, each channel threshold can be set flexibly and independently.

8.3.4.3 Internal Precision PWM Generator

The TPS92830-Q1 device has an integrated precision PWM generator for on-chip PWM dimming as shown in . The device supports open-drain PWMOUT for synchronization between devices. Each device can be connected as a master, generating PWM, or as a slave, relying on external PWM sources. An external RC circuit precisely sets the duty cycle of the PWM generator across a wide duty-cycle range. Variation of the capacitor value affects the output frequency but not the duty cycle.

The PWM generator uses reference current 2 × $I_{(IREF)}$ as the internal charge current, $I_{(PWMCHG)}$.

Feature Description (continued)

When $V_{(PWMCHG)}$ increases above rising threshold $V_{(PWMCHG\_th\_rising)}$, the constant-current source is turned off and $V_{(PWMCHG)}$ decays through the external resistor-capacitor circuit. The PWM output is set LOW. The PWMCHG threshold is set to $V_{(PWMCHG\_th\_falling)}$. When $V_{(PWMCHG)}$ decreases below falling threshold $V_{(PWMCHG\_th\_falling)}$, the constant-current source is turned on again to charge up the external capacitor. The PWM output is HIGH and the threshold is set to $V_{(PWMCHG\_th\_rising)}$.

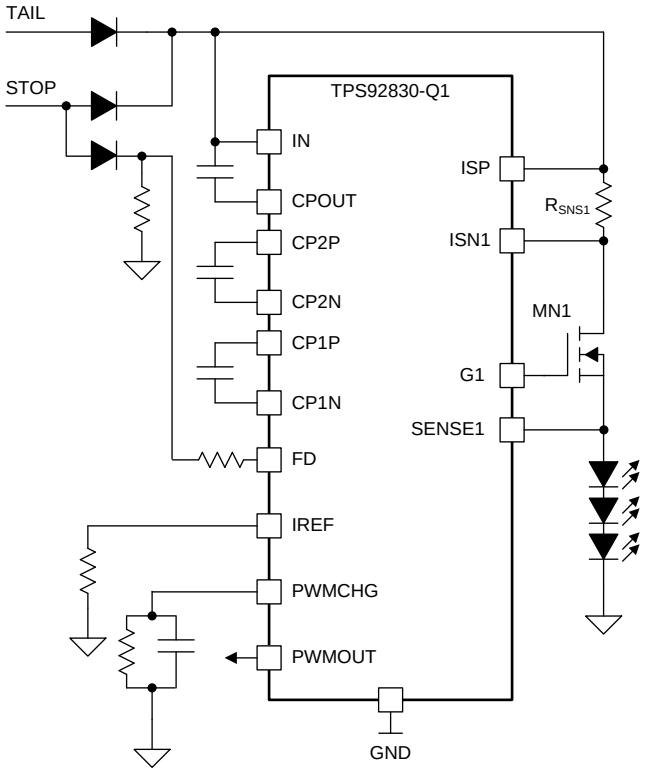


図 23. PWM Generator Dual-Brightness Configuration

An external resistor $R_{(PWMEXT)}$ and capacitor $C_{(PWMEXT)}$ are used to set the PWM cycle time.

$$t_{(PWM\_ON)} = R_{(PWMEXT)} \times C_{(PWMEXT)} \times \ln\left(\frac{V_{(PWMCHG\_th\_falling)} - I_{(PWMCHG)} \times R_{(PWMEXT)}}{V_{(PWMCHG\_th\_rising)} - I_{(PWMCHG)} \times R_{(PWMEXT)}}\right) \quad (3)$$

$$t_{(PWM\_OFF)} = R_{(PWMEXT)} \times C_{(PWMEXT)} \times \ln\left(\frac{V_{(PWMCHG\_th\_rising)}}{V_{(PWMCHG\_th\_falling)}}\right) \quad (4)$$

$$f_{(PWMEXT)} = \frac{1}{R_{(PWMEXT)} \times C_{(PWMEXT)} \times \left[\ln\left(\frac{V_{(PWMCHG\_th\_falling)} - I_{(PWMCHG)} \times R_{(PWMEXT)}}{V_{(PWMCHG\_th\_rising)} - I_{(PWMCHG)} \times R_{(PWMEXT)}}\right) + \ln\left(\frac{V_{(PWMCHG\_th\_rising)}}{V_{(PWMCHG\_th\_falling)}}\right)\right]} \quad (5)$$

$$D_{(PWMEXT)} = \frac{\ln\left(\frac{V_{(PWMCHG\_th\_falling)} - I_{(PWMCHG)} \times R_{(PWMEXT)}}{V_{(PWMCHG\_th\_rising)} - I_{(PWMCHG)} \times R_{(PWMEXT)}}\right)}{\ln\left(\frac{V_{(PWMCHG\_th\_falling)} - I_{(PWMCHG)} \times R_{(PWMEXT)}}{V_{(PWMCHG\_th\_rising)} - I_{(PWMCHG)} \times R_{(PWMEXT)}}\right) + \ln\left(\frac{V_{(PWMCHG\_th\_rising)}}{V_{(PWMCHG\_th\_falling)}}\right)} \quad (6)$$

Feature Description (continued)

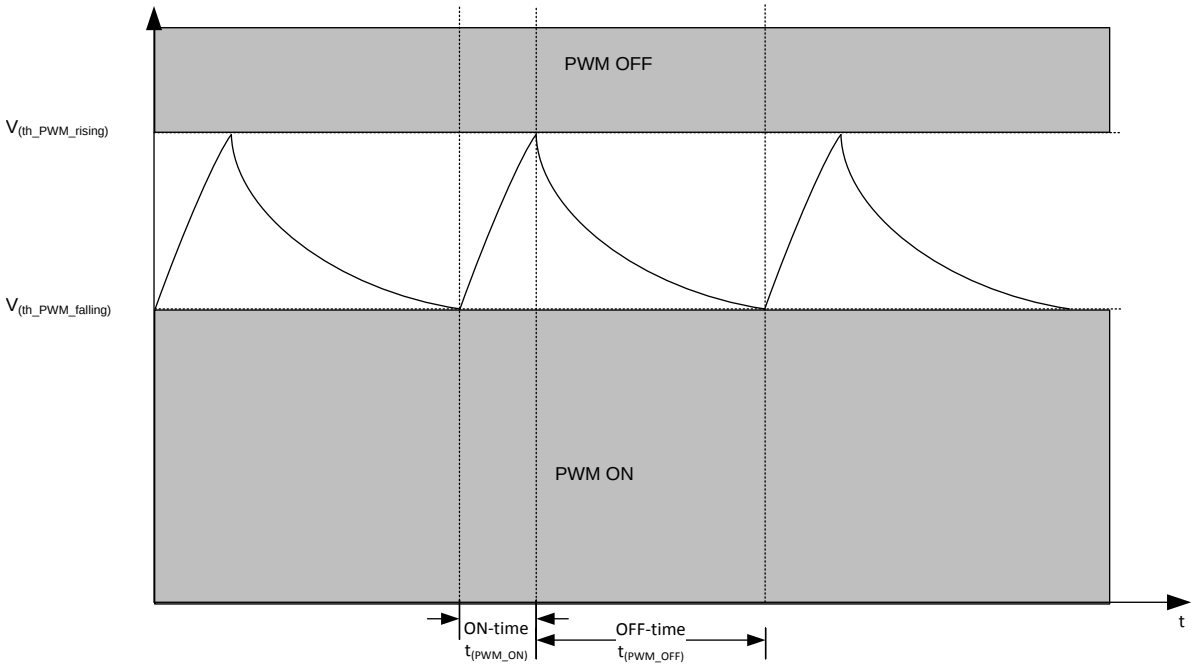


図 24. PWM Dimming Profile

8.3.4.4 Full Duty-Cycle Switch

The TPS92830-Q1 device can flexibly switch between the internal PWM modulation mode and the 100% duty-cycle mode by using the FD input. Once $V_{(FD)}$ is higher than threshold $V_{IH(FD)}$, the internal PWM generator is bypassed and output is merely controlled by the PWM inputs.

If FD is HIGH, the PWMCHG current source is turned off and $V_{(PWMCHG)}$ decays to GND through the external resistor-capacitor circuit. When FD falls below the threshold, $V_{(PWMCHG)}$ increases from GND due to the internal charge current.

If FD is HIGH, PWM generator oscillation stops, and PWMOUT is controlled by PWM1 only.

External PWM inputs and internal PWM inputs are combined together for channel PWM dimming, or external PWM inputs can be used as channel enable inputs.

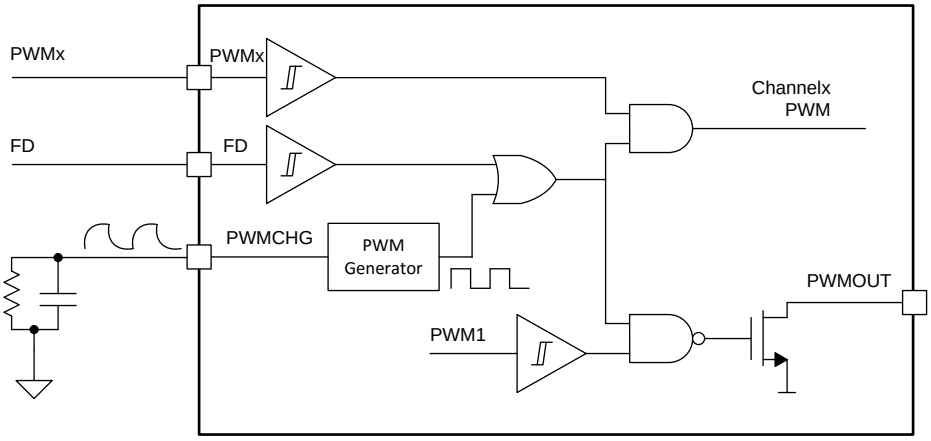


図 25. PWM Dimming Internal Block Diagram

Feature Description (continued)

表 1. Truth Table When Driving With PWM

PWMx	FD	PWMCHG	CHANNELx PWM
LOW	X	X	LOW
HIGH	HIGH	X	HIGH
HIGH	LOW	R-C	PWM generated with RC

表 2. Truth Table When Driving With PWMOUT

PWM1	FD	PWMCHG	PWMOUT
LOW	X	X	LOW
HIGH	HIGH	X	HIGH
HIGH	LOW	R-C	PWM generated with RC

8.3.5 Analog Dimming

The TPS92830-Q1 device has a linear analog input pin, ICTRL, for output-current dimming. Voltage across the sense resistors is linearly reduced if the ICTRL input voltage $V_{(ICTRL)}$ decreases. Analog dimming can be used for brightness control, LED bin brightness correction, and thermal protection with a thermistor. ICTRL also supports off-board connection for LED binning and thermistor connection.

8.3.5.1 Analog Dimming Topology

Voltage at the ICTRL pin, $V_{(ICTRL)}$, is used for analog dimming control. To set $V_{(ICTRL)}$, either a reference input voltage can be applied or a resistor between ICTRL and GND can be used.

When $V_{(ICTRL)}$ is greater than $V_{(ICTRL\_FULL)}$, analog dimming is not enabled; thus the analog dimming ratio is at 100%.

When $V_{(ICTRL)}$ is between $V_{(ICTRL\_LIN\_BOT)}$ and $V_{(ICTRL\_LIN\_TOP)}$, the analog dimming ratio is directly proportional to $V_{(ICTRL)}$. The analog dimming ratio can be calculated using the following equation. $V_{(ICTRL\_LIN\_BOT)}$ and $V_{(ICTRL\_LIN\_TOP)}$ represent the ICTRL voltage boundaries of the linear region.

$$k_{(ICTRL\_DIM)} = \frac{V_{(ICTRL)}}{1.475\,V} \times 100\% \quad (7)$$

When V_{ICTRL} is between $V_{(ICTRL\_LIN\_TOP)}$ and $V_{(ICTRL\_FULL)}$ or between $V_{(ICTRL\_LIN\_BOT)}$ and 0, analog dimming is in a transition region, and linearity is not assured. Thus it is not recommended to use ICTRL in these regions.

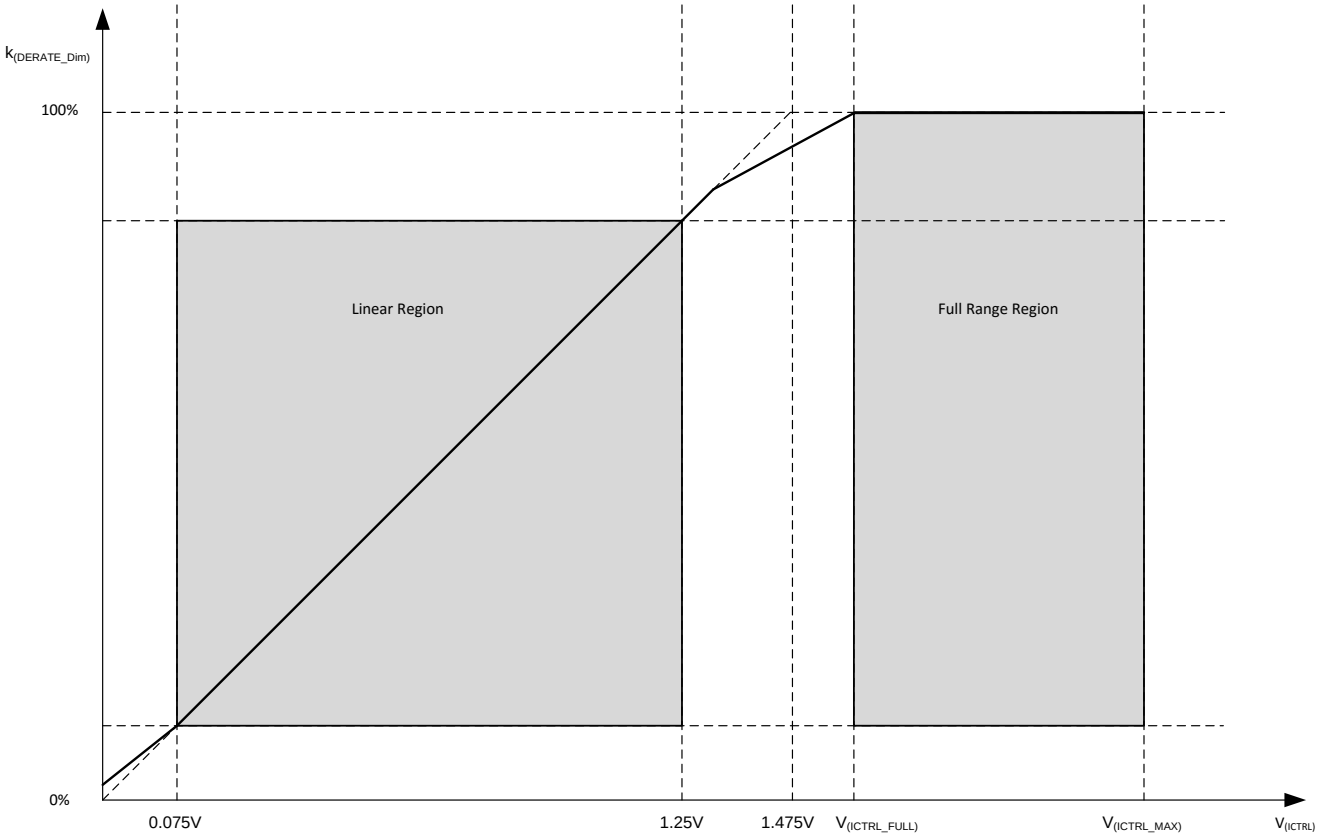


図 26. Analog Dimming Ratio

8.3.5.2 Internal High-Precision Pullup Current Source

An internal precision pullup current $I_{(ICTRL\_pullup)}$ is provided within the device to minimize external component count. $I_{(ICTRL\_pullup)}$ uses current reference $I_{(IREF)}$ as reference. With the internal pullup current source, only an external resistor between the ICTRL pin and GND is needed to set the ICTRL voltage and the analog dimming ratio.

If a voltage source or resistor divider is used, the internal pullup current must be taken into account to set the analog dimming ratio accurately.

The pullup current source pulls the ICTRL pin voltage up to input voltage $V_{(IN)}$ if the ICTRL pin is unconnected. When ICTRL is not used, it is recommended to leave the ICTRL pin floating.

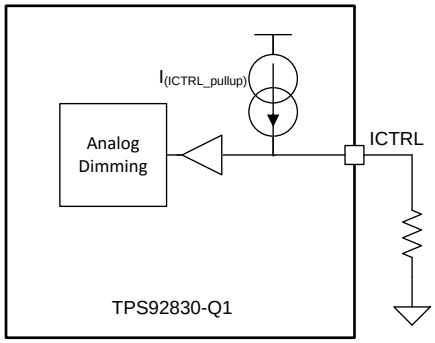


図 27. Internal High-Precision Pullup Current Source

8.3.6 Output Current Derating

The TPS92830-Q1 device has an integrated output-current derating function. Voltage across the sensing resistors is reduced if DERATE input voltage V_{DERATE} increases. The output current derating function can be used for supply overvoltage protection and thermal protection with a thermistor. The DERATE current curves are divided into 32 steps between 100% and 50% with hysteresis.

In the case where DERATE is used for battery voltage sensing, the resistor-divider ratio can be set in a typical application as follows.

- In the normal supply-voltage range, for example, (9 V–16 V), the output-current-derating function is disabled.
- In the overvoltage range, for example, (18 V–24 V), the output current starts to derate and reaches 50% when V_{IN} is at 24 V.
- When the voltage is even higher, for example, (24 V–26 V), the output current is saturated at 50%.

8.3.6.1 Output-Current Derating Topology

Voltage at the DERATE pin, $V_{(DERATE)}$, is used for output-current-derating control. To set the $V_{(DERATE)}$ voltage, a resistor divider on supply voltage V_{IN} is typically used for supply overvoltage protection.

- When V_{DERATE} is lower than $V_{(DERATE\_FULL)}$, output current derating is not enabled; thus, output-current derating ratio $k_{(DERATE\_Dim)}$ is at 100%.
- When V_{DERATE} is higher than $V_{(DERATE\_HALF)}$, output current derating is limited to 50%; thus, output-current derating ratio $k_{(DERATE\_Dim)}$ is at 50%.
- When $V_{(DERATE)}$ is between $V_{(DERATE\_FULL)}$ and $V_{(DERATE\_HALF)}$, the output-current-derating ratio is negatively proportional to $V_{(DERATE)}$ with 32 steps. Current derating is rounded to the next-lower step. The output-current-derating ratio can be calculated using the following equations.

$$V_{(DERATE\_STEP)} = \frac{V_{(DERATE\_HALF)} - V_{(DERATE\_FULL)}}{32} \tag{8}$$

$$k_{(DERATE\_Dim)} = 100\% - \left(\frac{V_{(DERATE)} - V_{(DERATE\_FULL)}}{V_{(DERATE\_STEP)}} \right) \times \frac{50\%}{32} \tag{9}$$

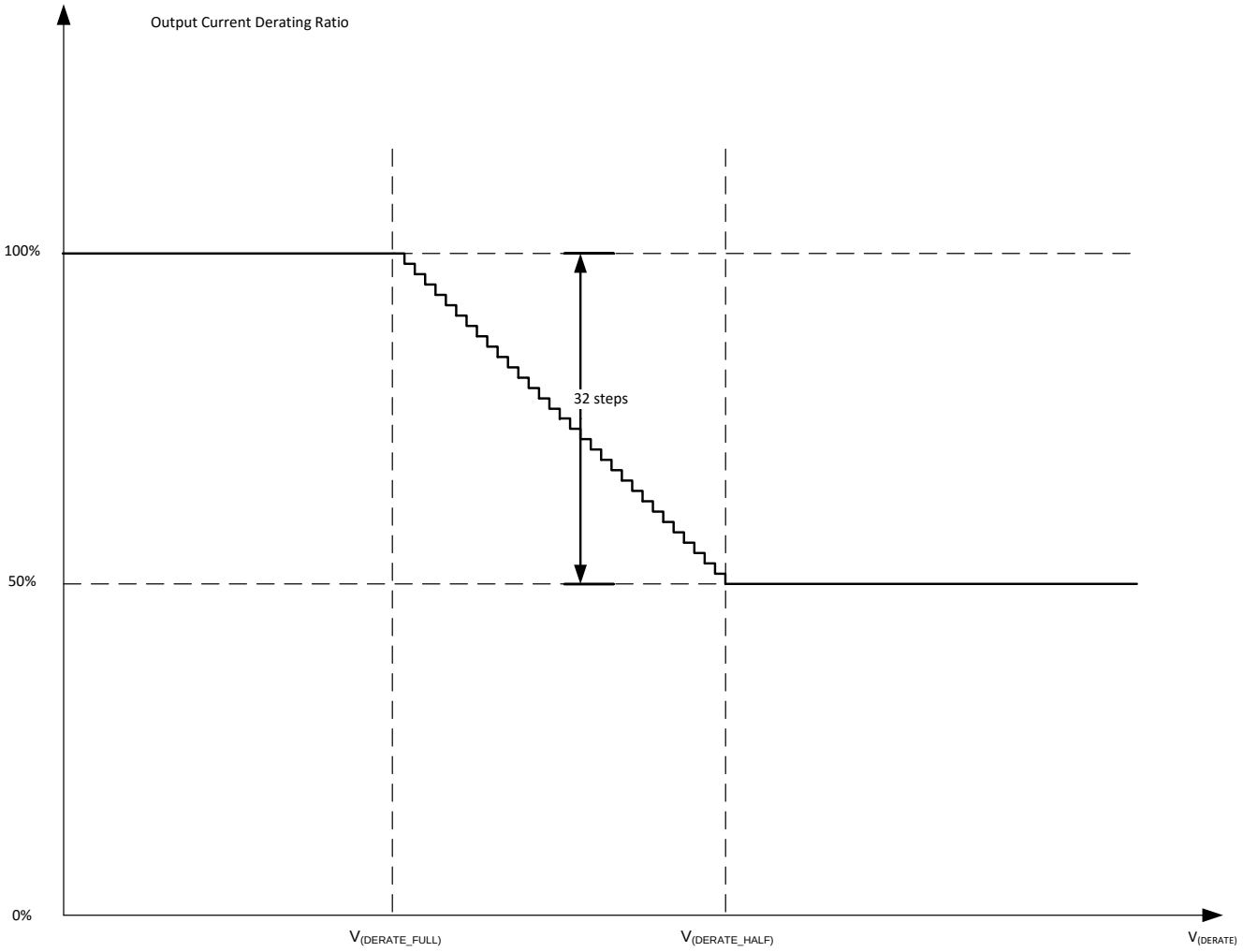


図 28. Output-Current Derating Profile

8.3.7 Diagnostics and Fault

The TPS92830-Q1 device provides advanced diagnostics and fault protection methods for automotive exterior lighting systems. The device is able to detect and protect from LED output short-to-GND as well as from LED output open-circuit scenarios. The device also supports a one-fails–all-fail fault bus that could flexibly fit different legislative requirements.

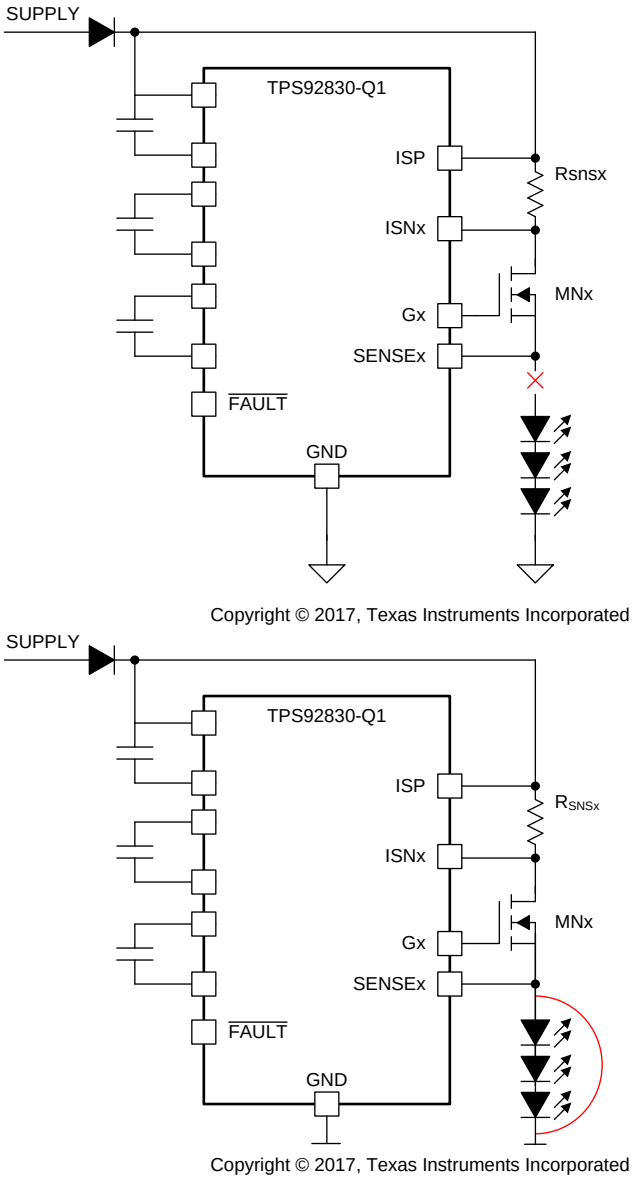


図 29. LED Open and Short Scenarios

8.3.7.1 LED Short-to-GND Detection

The TPS92830-Q1 device has channel-independent LED short-to-GND detection. Short-to-GND detection is only enabled during channel on-time. Once an LED short-to-GND failure is detected, the device turns off the faulty channel and retries automatically. If the auto-retry mechanism detects that the LED short-to-GND fault has been removed, the device resumes normal operation. section

The device monitors voltage $V_{(SENSEx)}$ and compares it with the internal reference voltage to detect short-to-GND failures. If the period during which $V_{(SENSEx)}$ falls below $V_{(SG\_th\_rising)}$ is longer than the deglitch time of $t_{(SG\_deg)}$, the device asserts a short-to-GND fault on this channel. During the deglitch time period, if V_{SENSEx} rises above $V_{(SG\_th\_falling)}$, the timer is reset.

If a fault is detected, a constant-current source pulls the fault bus down. If $\overline{FAULT}$ is low, all devices connected to the fault bus are off in the fault mode.

8.3.7.2 LED Short-to-GND Auto Retry

Once the channel has asserted a short-to-GND fault, it automatically retries periodically. In PWM mode, the device sources $I_{(Retry\_short)}$ through the SENSEx pin to pull up the LED loads with a pulse duration of $t_{(SG\_retry\_ON)}$. The device waits for $t_{(SG\_retry\_OFF)}$ until the next retry pulse. Once auto retry detects that the short-to-GND fault is removed, the device resumes normal operation. During auto retry mode, the device ignores PWM inputs.

8.3.7.3 LED Open-Circuit Detection

The TPS92830-Q1 device has channel-independent LED open-circuit detection. Once an LED open-circuit failure is detected, the device turns off the faulty channel and retries automatically. If the retry mechanism detects that the LED open-circuit fault is removed, the device resumes normal operation.

The device monitors MOSFET dropout voltage differences between the ISNx and SENSEx pins. Voltage difference $V_{(ISNx)} – V_{(SENSEx)}$ is compared with internal reference voltage $V_{(OPEN\_th\_rising)}$ to detect an LED open-circuit failure. If $V_{(ISNx)} – V_{(SENSEx)}$ falls below the $V_{(OPEN\_th\_rising)}$ voltage and it stays there longer than the deglitch time of $t_{(OPEN\_deg)}$, the device asserts an open-load fault on this channel. During the deglitching time period, if $V_{(ISNx)} – V_{(SENSEx)}$ rises above $V_{(OPEN\_th\_falling)}$, the deglitch timer is reset.

In normal operation, the N-channel MOSFET operates in the saturation region with a gate-source voltage close to its threshold voltage. In this case, the drain-source voltage of the N-channel MOSFET is typically much higher than open-circuit threshold $V_{(OPEN\_th\_rising)}$. In the LED open-circuit condition, the N-channel MOSFET operates in the linear region with a gate-source voltage much higher than its threshold voltage. The N-channel MOSFET is fully on.

If a fault is detected, a constant-current source pulls the fault bus down. If the $\overline{FAULT}$ pin is low, all devices connected to the fault bus are off in the fault mode.

8.3.7.4 LED Open-Circuit Auto Retry

Once the channel has asserted an open-circuit fault, it automatically retries periodically. The device sources $I_{(Retry\_open)}$ through the SENSEx pin to pull up the LED loads with a pulse duration of $t_{(OPEN\_retry\_ON)}$. In PWM mode, the device waits for $t_{(OPEN\_retry\_OFF)}$ until the next retry pulse. Once auto retry detects that the open-circuit fault has been removed, the device resumes normal operation. During auto retry mode, the device ignores PWM inputs. In the open-circuit scenario, the retry current cannot find a path to ground; thus, total current consumption does not increase.

8.3.7.5 Dropout-Mode Diagnostics

When the input voltage is not high enough to keep the external N-channel MOSFET in the constant-current saturation region, the TPS92830-Q1 device tries to regulate current by driving the external N-channel MOSFET in the linear region. This state is called the dropout mode, because voltage across the sense resistor is not able to reach the regulation threshold.

In dropout mode, LED open-circuit detection must be disabled via the DIAGEN input. Otherwise, the dropout mode would be treated as an LED open-circuit fault. The DIAGEN pin is used to avoid false diagnostics on an output channel due to low supply voltage.

When the DIAGEN voltage is low, the LED open-circuit detection is ignored. When the DIAGEN voltage is high, LED open-circuit detection resumes normal operation.

In dropout mode, the MOSFET is driven at maximum gate-source voltage to regulate current to the desired value. When the supply voltage increases, the MOSFET gate voltage is pulled down internally by a control loop. If the supply-voltage slew rate is fast, a high-current pulse can be observed on the LED for a short period of time. At the same time, the current-sense voltage may exceed the normal operating range and damage internal circuitry. A parallel diode or a current-limiting resistor less than 1 kΩ is recommended to clamp the voltage across the sensing resistor in the case of a large pulse current.

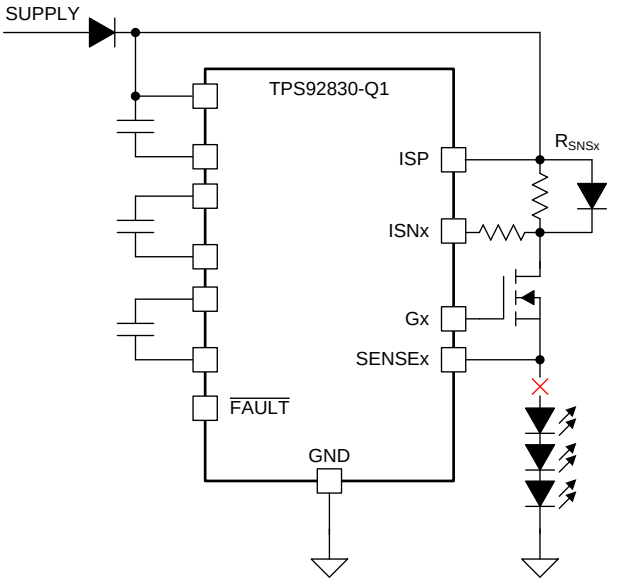


図 30. Resistor and Diode for Sense-Resistor Protection

8.3.7.6 Overtemperature Protection

The TPS92830-Q1 device monitors device junction temperature. When the junction temperature reaches the thermal shutdown threshold $T_{(TSD)}$, all outputs shut down and the charge pump also stops working. Once the junction temperature falls below $T_{(TSD)} - T_{(TSD\_HYS)}$, the device resumes normal operation. During overtemperature protection, the $\overline{FAULT}$ bus is pulled low.

8.3.7.7 $\overline{FAULT}$ Bus Output With One-Fails–All-Fail

The TPS92830-Q1 device has a $\overline{FAULT}$ bus for diagnostics output. It also supports a one-fails–all-fail function with other TPS92830-Q1, TPS9261x-Q1, TPS92630-Q1, or TPS92638-Q1 devices.

In normal operation, $\overline{FAULT}$ is weakly pulled up by internal pullup current source $I_{(FAULT\_pullup)}$ to a voltage higher than $V_{OH(FAULT)}$. If any fault scenario occurs, the $\overline{FAULT}$ bus is strongly pulled low by internal pulldown current source $I_{(FAULT\_pulldown)}$. Once $V_{(FAULT)}$ falls below $V_{IL(FAULT)}$, all outputs are shut down for protection. The faulty channel keeps retrying until the fault condition is removed. The charge pump is shut down, and current consumption is also reduced to $I_{(FAULT)}$ to save quiescent current.

If $\overline{FAULT}$ is externally pulled up with a current higher than $I_{(FAULT\_pulldown)}$, the one-fails–all-fail function is disabled and only the faulty channel is turned off. The charge pump remains operating normally, and the device is in normal operation mode. The $\overline{FAULT}$ bus is able to support up to 15 pieces of TPS92830-Q1, TPS92630-Q1, TPS92638-Q1, or TPS9261x-Q1 devices.

8.3.7.8 Fault Table

表 3. Fault Table With DIAGEN = HIGH

FAULT TYPE	DETECTION MECHANISM	CHANNEL STATE	DEGLITCH TIME	FAULT BUS	FAULT HANDLING ROUTINE	FAULT RECOVERY
$\overline{\text{FAULT}}$ FLOATING						
LED open-circuit	$V_{ISNx} - V_{SENSEx} < V_{(OPEN\_th\_rising)}$	On	$t_{(OPEN\_deg)}$	Constant-current pulldown	All channels turned off. Pulsed pullup retry of faulty channel.	Auto recover
LED short-to-GND	$V_{SENSEx} < V_{(SG\_th\_rising)}$	On	$t_{(SG\_deg)}$		All channels turned off. Pulsed pullup retry of faulty channel.	
LED short-to-battery	$V_{ISNx} - V_{SENSEx} < V_{(OPEN\_th\_rising)}$	On or off	$t_{(OPEN\_deg)}$		All channels turned off. Faulty channel pulsed pullup retry of faulty channel.	
Overtemperature	$T_J > T_{(TSD)}$	On or off			All channels turned off.	
$\overline{\text{FAULT}}$ EXTERNALLY PULLED UP						
LED open-circuit	$V_{ISNx} - V_{SENSEx} < V_{(OPEN\_th\_rising)}$	On	$t_{(OPEN\_deg)}$	Externally pulled up with internal constant-current pulldown	Only faulty channel turned off. Pulsed pullup retry of faulty channel.	Auto recover
LED short-to-GND	$V_{SENSEx} < V_{(SG\_th\_rising)}$	On	$t_{(SG\_deg)}$		Only faulty channel turned off. Pulsed pullup retry of faulty channel.	
LED short-to-battery	$V_{ISNx} - V_{(SENSEx)} < V_{(OPEN\_th\_rising)}$	On or off	$t_{(OPEN\_deg)}$		Only faulty channel turned off. Pulsed pullup retry of faulty channel.	
Overtemperature	$T_J > T_{(TSD)}$	On or off			All channels turned off.	
$\overline{\text{FAULT}}$ EXTERNALLY PULLED DOWN						
All outputs disabled						

表 4. Fault Table With DIAGEN = LOW

FAULT TYPE	DETECTION MECHANISM	CHANNEL STATE	DEGLITCH TIME	FAULT BUS	FAULT HANDLING ROUTINE	FAULT RECOVERY
$\overline{\text{FAULT}}$ FLOATING						
LED open-circuit	Ignored	Ignored	Ignored	Ignored	Ignored	Ignored
LED short-to-GND	$V_{(SENSEx)} < V_{(SG\_th\_rising)}$	On	$t_{(SG\_deg)}$	Constant current pull down	All channels turned off. Pulsed pullup retry of faulty channel.	Auto recover
LED short-to-battery	Ignored	Ignored	Ignored	Ignored	Ignored	Ignored
Overtemperature	$T_J > T_{(TSD)}$	On or off		Constant current pull down	All channels turned off.	Auto recover
$\overline{\text{FAULT}}$ EXTERNALLY PULLED UP						
LED open-circuit	Ignored	Ignored	Ignored	Ignored	Ignored	Ignored
LED short-to-GND	$V_{(SENSEx)} < V_{(SG\_th\_rising)}$	On	$t_{(SG\_deg)}$	Externally pulled up with internal constant current pulled down	Only faulty channel turned off. Pulsed pullup retry of faulty channel.	Auto recover
LED short-to-battery	Ignored	Ignored	Ignored	Ignored	Ignored	Ignored
Overtemperature	$T_J > T_{(TSD)}$	On or off		Externally pulled up with internal constant current pulled down	All channels turned off.	Auto recover
$\overline{\text{FAULT}}$ EXTERNALLY PULLED LOW						
All outputs disabled	All outputs disabled	All outputs disabled	All outputs disabled	All outputs disabled	All outputs disabled	All outputs disabled

8.4 Device Functional Modes

8.4.1 Undervoltage Lockout, $V_{(IN)} < V_{(UVLO)}$

When the device is in undervoltage lockout mode, the TPS92830-Q1 device disables all functions until the supply rises above the UVLO-rising threshold. The device pulls down the Gx outputs. Other outputs are in the high-impedance state.

8.4.2 Normal Operation ($V_{(IN)} \geq 4.5$ V, $V_{(IN)} > V_{(LED)} + 0.5$ V)

The device drives an LED string in normal operation. A 0.5-V minimal dropout voltage is typically more than enough to maintain LED current regulation.

8.4.3 Low-Voltage Dropout

When the device drives an LED string in low-dropout mode, even with the MOSFETs fully turned on the output current may not reach target value. The device reports an LED open-circuit failure if DIAGEN is HIGH.

8.4.4 Fault Mode (Fault Is Detected)

When the device detects an open or shorted LED, the device tries to pull down the $\overline{\text{FAULT}}$ pin with a constant current. If the fault bus is pulled down, the device switches to fault mode and consumes a fault current of $I_{(FAULT)}$.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

In automotive applications, linear LED drivers are preferable for various applications, especially exterior lighting, for their simplicity and electromagnetic compatibility. This section provides a few examples to show the design process for different features.

9.2 Typical Applications

9.2.1 Typical Application for Automotive Exterior Lighting With One-Fails–All-Fail

Various functions of exterior lighting may use the following circuit. Here is a typical application circuit for a turn indicator. A TPS92830-Q1 drives a total of nine LEDs with 3s3p configuration at 300 mA each.

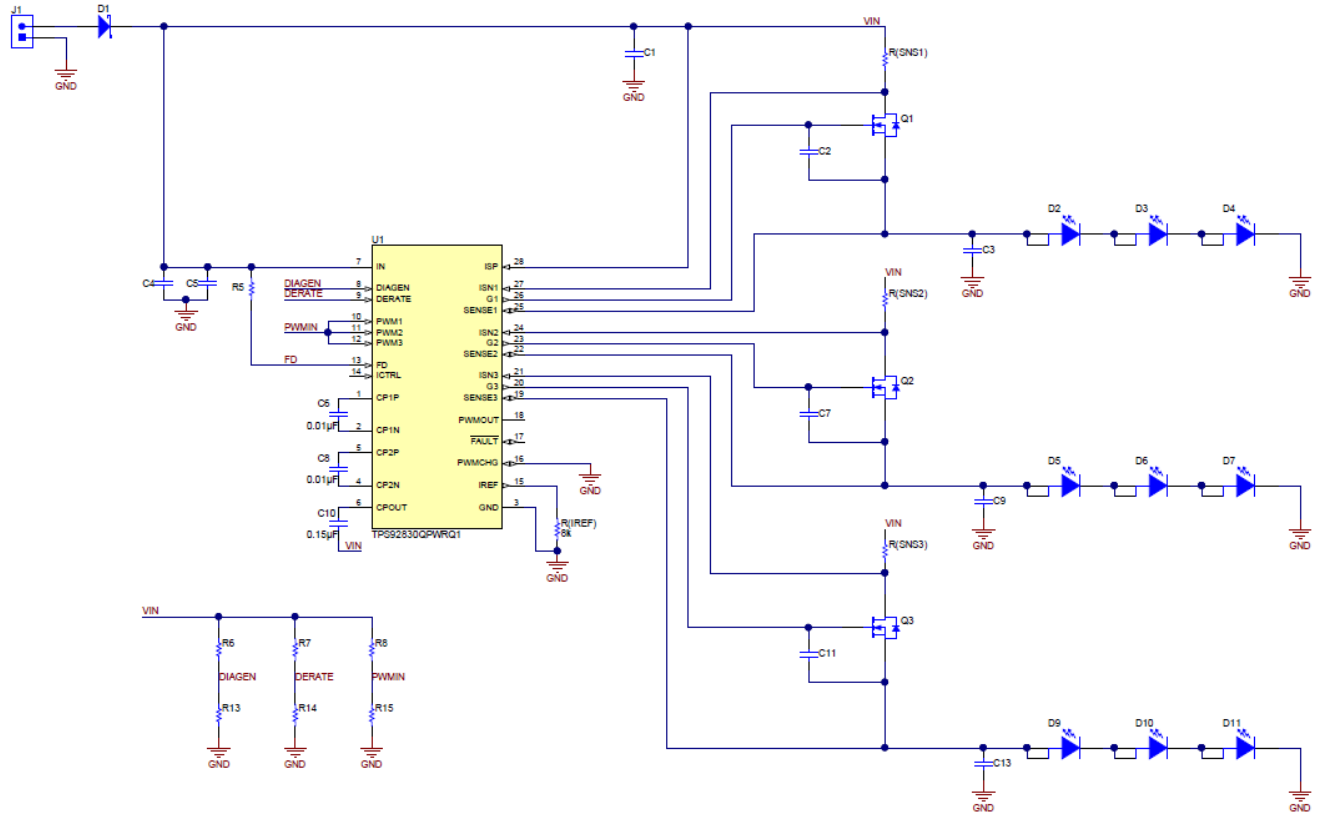


図 31. TPS92830-Q1 Typical Application Circuit For Automotive Exterior Lighting

9.2.1.1 Design Requirements

With the wide range of battery voltages in modern automotive systems, it is a common requirement among car OEMs to turn LEDs off when the battery voltage is below the minimal voltage threshold, for example, 6 V.

When the battery voltage is between 6 V and 9 V, LEDs may not achieve full brightness due to low input voltage. Although a linear LED driver may drive in low-dropout mode, it is required not to treat the low-dropout mode as an open-circuit fault and to report a false error.

Typical Applications (continued)

When battery voltage ranges between 9 V and 16 V, the LED driver works in normal mode with the one-fails–all-fail feature. If any LED strings fail with an open circuit or short circuit, the TPS92830-Q1 device pulls down the fault bus. All devices connected to the same fault bus turn off their outputs.

When the battery voltage is above 18 V, the TPS92830-Q1 device is able to detect the overvoltage and derate the output current to reduce the power dissipation of the MOSFETs and prevent thermal damage.

9.2.1.2 Detailed Design Procedure

Fixed Parameters

- Charge pump flying capacitor C6 = 10 nF
- Charge pump flying capacitor C8 = 10 nF
- $R_{(IREF)}$ = 8 kΩ
- Charge pump storage capacitor C10 = 150 nF

Current Setting

- $I_{(LED)}$ = 300 mA
- $R_{(SNS)}$= $V_{(CS\_REG)}$ / $I_{(LED)}$ = 0.983 Ω

PWM Threshold Setting

- PWM enables when $V_{(IN)}$ > 6 V
- $K_{(RES\_PWM)}$ = $V_{IH(PWMx,\ max)}$ / 6 V
- $K_{(RES\_PWM)}$ = R15 / (R15 + R8)
- Set R15 = 20 kΩ, R8 = 76 kΩ

DiagEN Setting (Enables LED-Open Detection When $V_{(IN)}$ > 9 V

- $K_{(RES\_DiagEN)}$ = $V_{IH(DIAGEN,\ max)}$ / 9 V
- $K_{(RES\_DiagEn)}$ = R13 / (R6 + R13)
- Set R13 = 10 kΩ, R6 = 62 kΩDiagEN setting

DERATE Setting (Reduces Current Output When $V_{(IN)}$ > 18 V

- $K_{(RES\_DERATE)}$ = $V_{(DERATE\_FULL,\ min)}$ / 18 V
- $K_{(RES\_DERATE)}$ = R7 / (R7+ R14)
- Set R7 = 10 kΩ, R14 = 95 kΩ

To deliver 300 mA with a single MOSFET package, the designer must consider the maximum thermal-dissipation condition. The power dissipation of a MOSFET is usually at its peak when input voltage is at 16 V in a full-brightness condition. Assume the minimal LED forward voltage at 300 mA is 6 V.

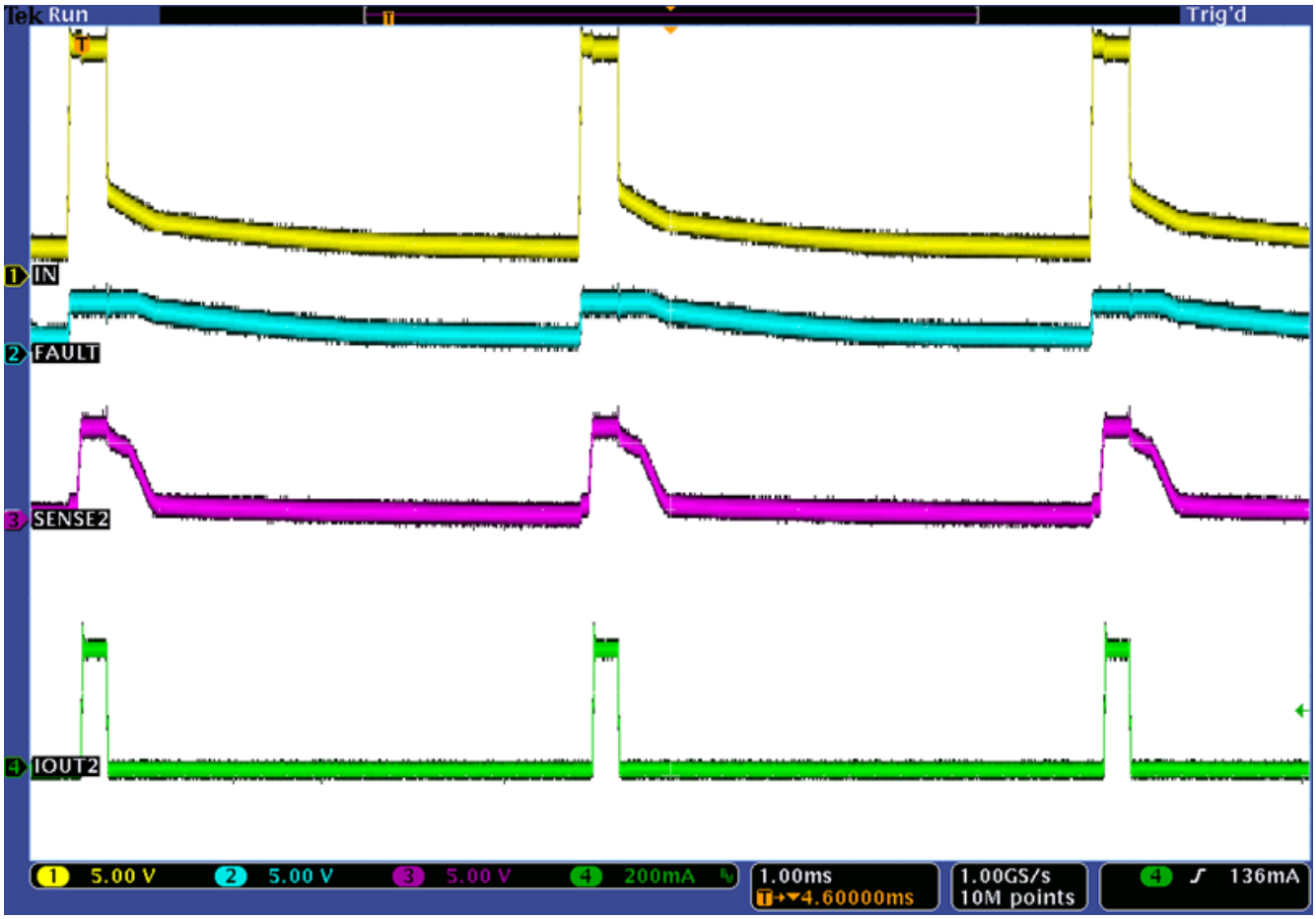
$$P_{(MOSFET)} = I_{(LED)} \times \left(V_{(IN)} - V_{F(Diode)} - V_{F(LED,min)} - V_{(CS\_REG)} \right) = 300mA \times (16 - 0.7 - 6 - 0.295) = 2.702W \quad (10)$$

MOSFET package and layout design must be considered to dissipate 2.702 W at maximum ambient temperature, usually 85°C.

The TPS92830 device can support a variety of N-channel MOSFETs in the markets. Adding a capacitor between the gate and source increases the loop phase margin. The recommended total capacitance at Gx is greater than 4 nF.

Typical Applications (continued)

9.2.1.3 Application Curves



Ch. 1 = $V_{(IN)}$
Ch. 4 = $I_{(OUT2)}$

Ch .2 = $V_{(\overline{FAULT})}$
IN HIGH = 14 V, LOW = 0 V, with reverse blocking diode

Ch. 3 = $V_{(SENSE2)}$
Pulse duration = 300 µs, period = 2 ms

図 32. BCM PWM Dimming Curve

9.2.2 High-Precision Dual-Brightness PWM Generation

9.2.2.1 Dual-Brightness Application

Automotive lighting often reuses the same LEDs for different functions with different brightness, for example, daytime running lights (DRL) and position lights, or stop and tail lights. Analog dimming by changing the constant current may affect LED color temperature. PWM dimming could easily achieve the dimming ratio with the same color temperature.

The TPS92830-Q1 device provides a precision PWM generator with a synchronization PWMOUT output. Its integrated high-precision PWM generator ensures homogeneity across different devices.

Typical Applications (continued)

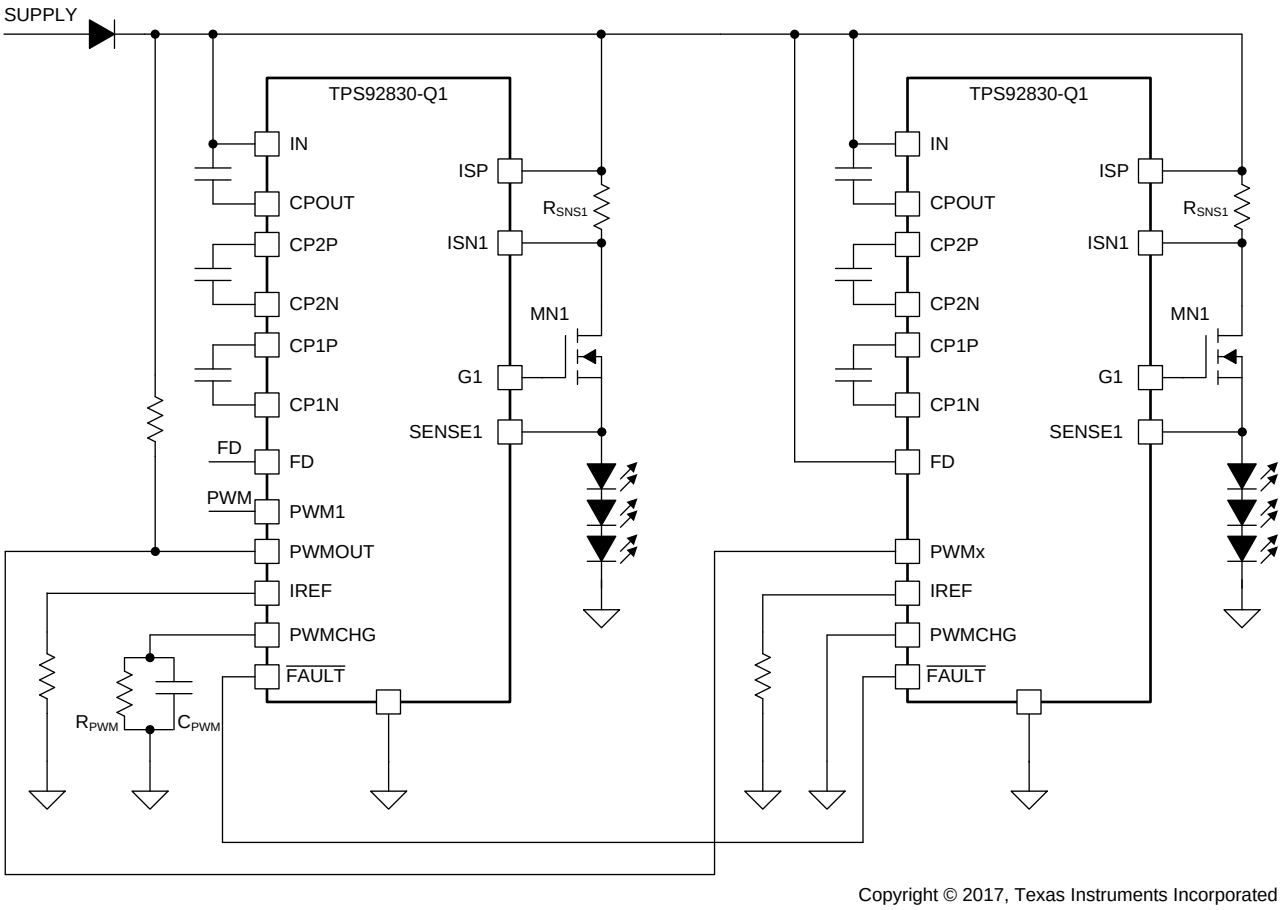


図 33. PWM Generator Master-Slave Configuration

9.2.2.2 Design Requirements

When full duty-cycle (FD) is HIGH, the output is at 100% duty cycle.

When full duty-cycle (FD) is LOW, the output is at 10% duty cycle and 250 Hz.

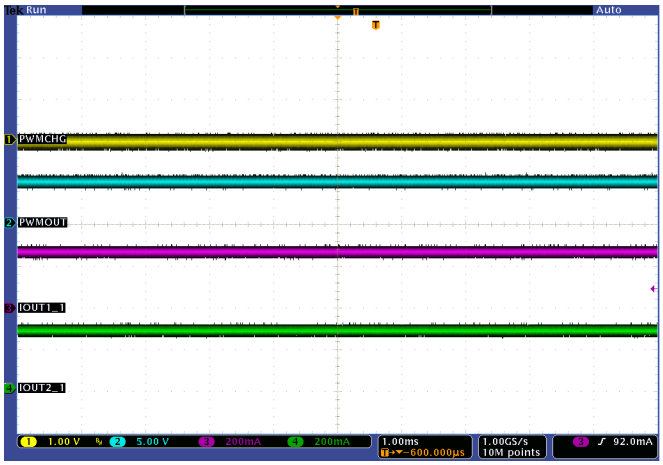
9.2.2.3 Detailed Design Procedure

PWM Equations

- R_{PU} = 10 kΩ
- C_{PWM} = 105.5 nF
- R_{PWM} = 55.5 kΩ

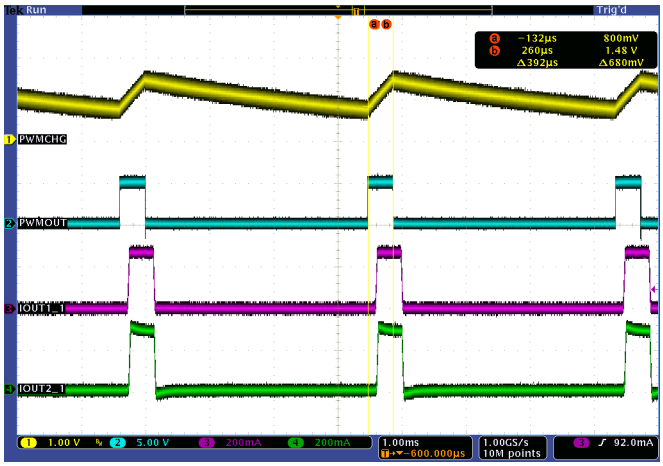
Typical Applications (continued)

9.2.2.4 Application Curve



Ch. 1 = $V_{(PWMCHG)}$ Ch. 2 = $V_{(PWMOUT)}$ Ch. 3 = $I_{(OUT1\_1)}$
Ch. 4 = $I_{(OUT2\_1)}$

図 34. Dual Brightness With Integrated High-Precision PWM Generator at Full Duty-cycle



Ch. 1 = $V_{(PWMCHG)}$ Ch. 2 = $V_{(PWMOUT)}$ Ch. 3 = $I_{(OUT1\_1)}$
Ch. 4 = $I_{(OUT2\_1)}$

図 35. Dual Brightness With Integrated High-Precision PWM Generator at 10% Duty-cycle

9.2.3 Driving High-Current LEDs With Parallel MOSFETs

Thermal performance is one key consideration in automotive exterior driving, especially for a linear LED driver. Due to large variations of automotive battery voltage, a linear LED driver must accommodate thermal dissipation with a worst-case scenario, which is high ambient temperature and high battery voltage.

LED driver thermal dissipation performance merely depends on the package and PCB thermal dissipation area. However, if the thermal dissipation performance of a single MOSFET is not able to support the required LED string current, multiple MOSFETs in parallel are able to dissipate heat for high-current applications.

When a MOSFET is in the saturation region as a current-control device, its current output strongly depends on its threshold. MOSFET threshold V_{th} can vary from one device to another. When MOSFETs are in parallel, even a small threshold mismatch could lead to imbalance of current distribution.

With an integrated charge pump, the TPS92830-Q1 device provides sufficient headroom even when the supply voltage is as low as 5 V. Thus adding ballast resistors between the N-channel MOSFET source and the LED string introduces negative feedback for each parallel MOSFET path to balance the current flows.

表 5. Thermal Measurement of Parallel MOSFETs

	WITHOUT CURRENT BALLAST Resistor	WITH 1-Ω BALLAST RESISTOR	WITH 3-Ω BALLAST RESISTOR
MOSFET1 Temperature (ºC)	105.7	85.3	85.9
MOSFET2 Temperature (ºC)	76.1	82.8	84.2
MOSFET3 Temperature (ºC)	84.8	87.6	85.3

$V_{(IN)}$= 16 V, $I_{(Total)}$ = 964 mA, T_A= 25 ºC.

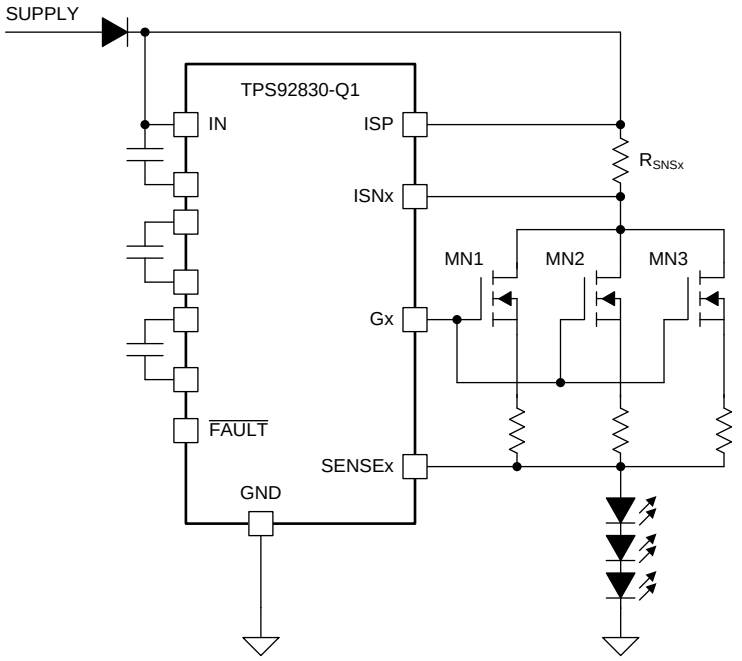
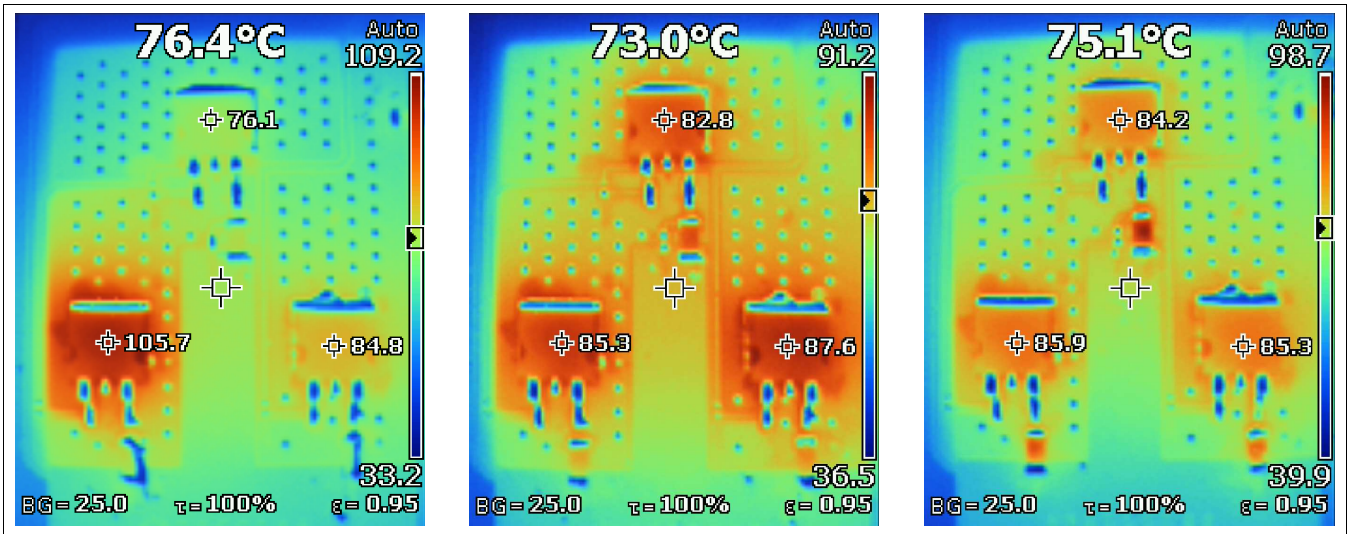


図 36. Parallel MOSFET Driving

9.2.3.1 Application Curves



Without Ballast Resistors | With 1-Ω Ballast Resistors | With 3-Ω Ballast Resistors

図 37. Thermal Images of Parallel MOSFETs With Various Ballast Resistors

10 Layout

10.1 Layout Guidelines

The TPS92830-Q1 device relies on external MOSFETs to dissipate heat for high-current applications. To effectively dissipate heat on MOSFETs and LEDs, TI recommends to use 0.071-mm-thick (2-oz.) copper PCBs or metal-based boards. Make the thermal dissipation area with copper as large as possible. Place thermal vias on the thermal dissipation area to further improve the thermal dissipation capability. The current path starts from IN through the sense-resistors, MOSFETs, and LEDs to GND. Wide traces are helpful to reduce parasitic resistance along the current path as shown in the layout example below.

Place capacitors, especially charge pump capacitors, close to the device to make the current path as short as possible. TI suggests keeping the LED high-current ground path separate from device ground. TI also recommends kelvin-connection to the connector. The following layout example shows the recommended guidelines.

10.2 Layout Example

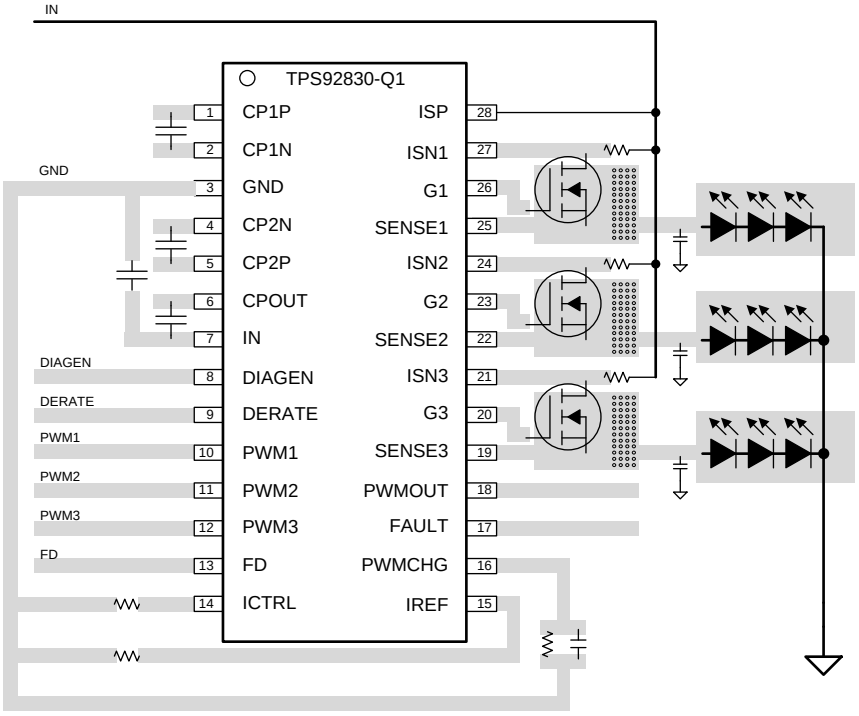


図 38. TPS92830-Q1 Example Layout Diagram

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.2 コミュニティ・リソース

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TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）コミュニティ。*****エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。**

設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

11.3 商標

E2E is a trademark of Texas Instruments.

11.4 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92830QPWRQ1	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS92830	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

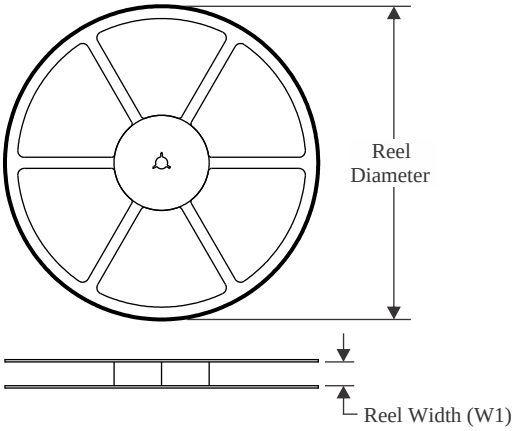
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

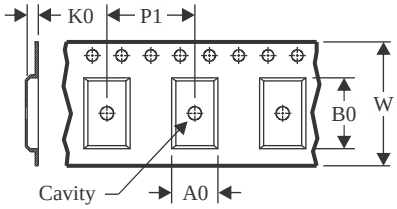
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

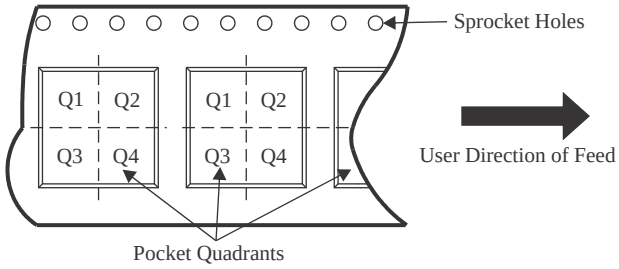


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

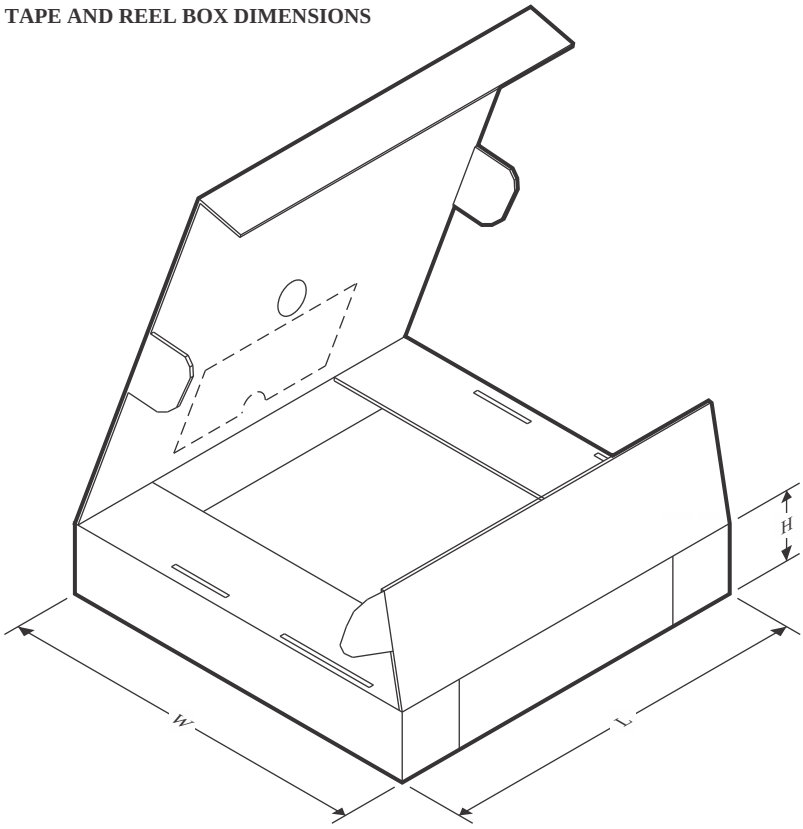
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92830QPWRQ1	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

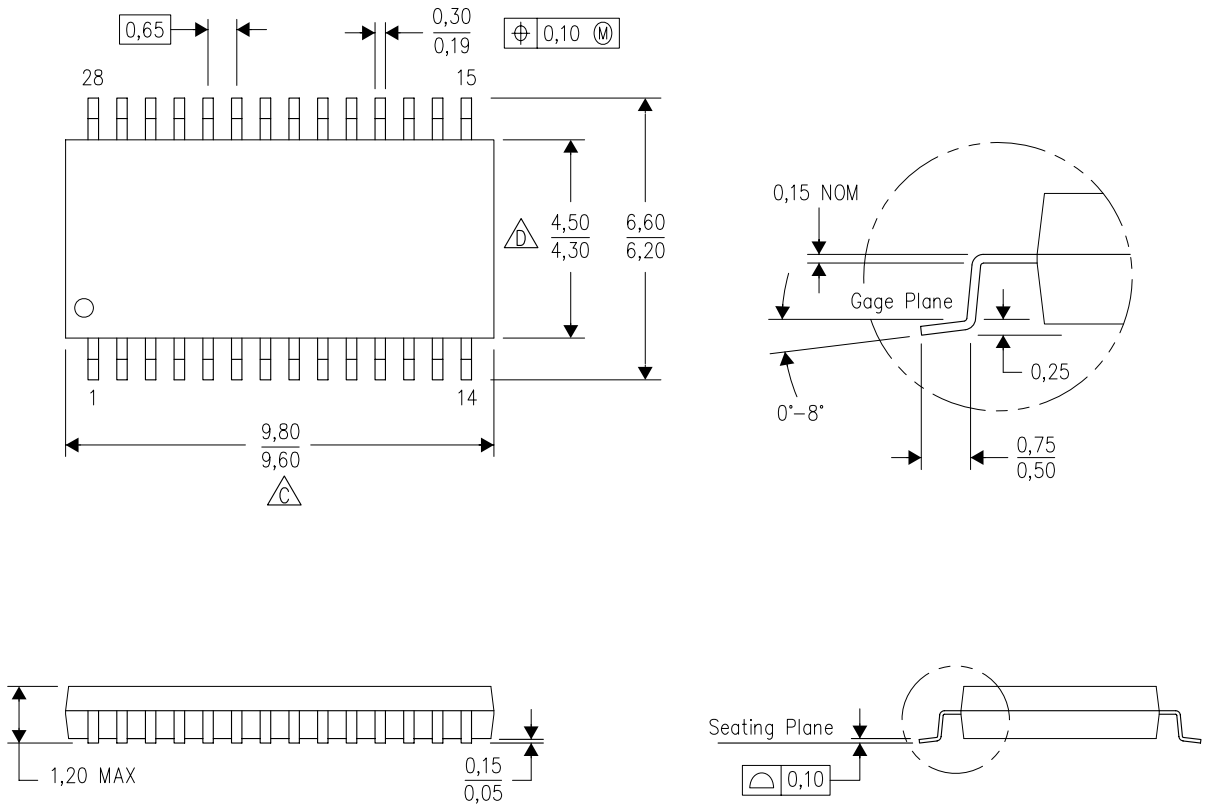
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92830QPWRQ1	TSSOP	PW	28	2000	350.0	350.0	43.0

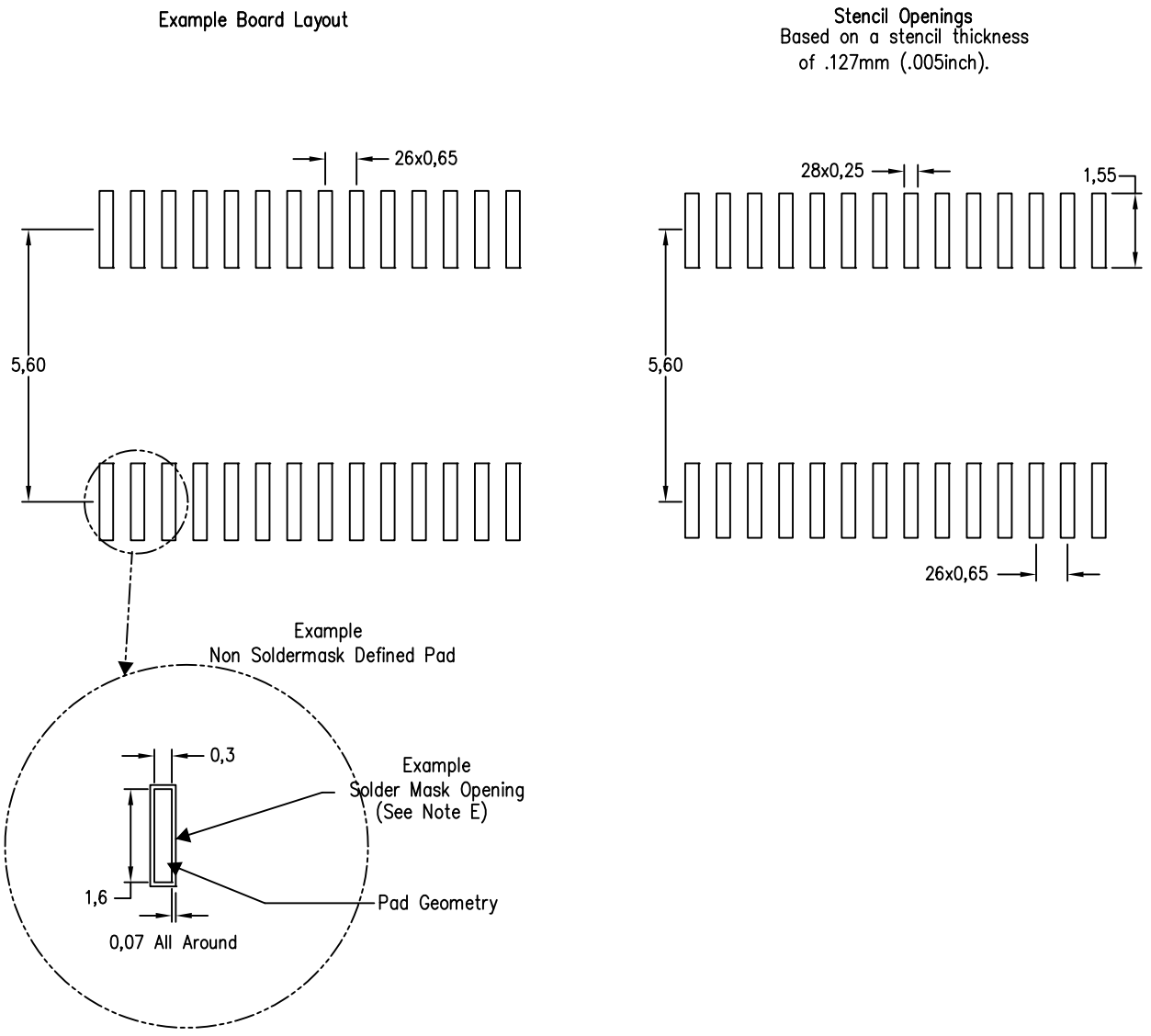
PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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