TEXAS INSTRUMENTS
TPSF12C3-Q1
JAJSNX8A – JANUARY 2023 – REVISED APRIL 2023

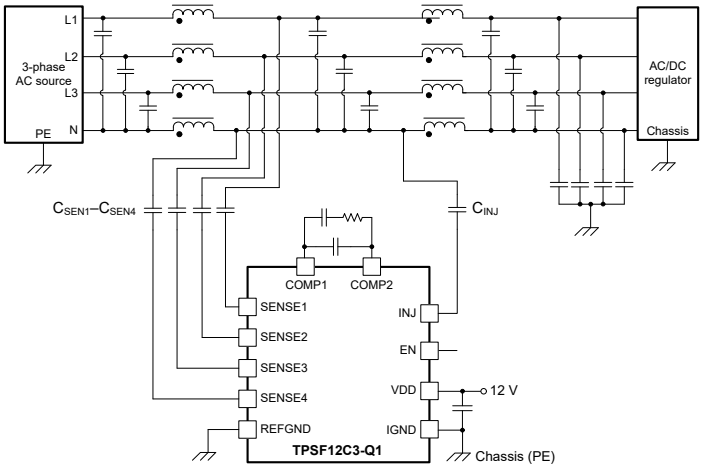
TPSF12C3-Q1 3 相、AC、車載用電源システムの同相ノイズ低減用スタンドアロン、アクティブ、EMI フィルタ

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - デバイス温度グレード 1:動作時周囲温度範囲:-40℃～+125℃
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 電圧センス、電流注入アクティブ EMI フィルタ
  - CISPR 25 Class 5 車載用 EMI 要件に最適化
  - 同相放射に対して低インピーダンス
  - チョーク・サイズ、重量、コストを 50% 以上低減
  - ピーク注入電流 ±80mA (標準値)
- 広い電源電圧範囲:8V～16V
- 接合部温度範囲:-40℃～150℃
- 3 相 AC システムのシンプルな構成
  - センシング・フィルタと加算ネットワークを内蔵
  - ライン周波数での低リーク電流
  - 簡略化された補償ネットワーク
- 堅牢な設計のための本質的な保護機能
  - 最小限の外付け部品で 6kV のサージ (IEC 61000-4-5) に対応
  - イネーブル・ピンによりリモートでオン / オフ制御
  - ヒステリシス付きの VDD 電圧 UVLO 保護
  - ヒステリシス付きのサーマル・シャットダウン保護
- 4.2mm × 2mm SOT-23 14 ピン (DYY) パッケージ

2 アプリケーション

- BEV と PHEV 向けのオンボード・チャージャ
- 車載絶縁型 DC/DC レギュレータ
- HVAC モーター制御、航空宇宙、防衛



簡略回路図

3 概要

TPSF12C3-Q1 は、3 相 AC 電源システムの同相 (CM) 電磁干渉 (EMI) を低減するよう設計されたアクティブ・フィルタ IC です。

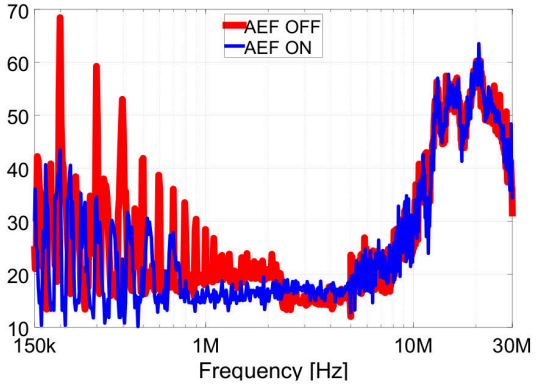
電圧センスと電流注入 (VSCI) を使用して構成されたアクティブ EMI フィルタ (AEF) は、容量性マルチプライヤ回路を使用して、従来型のパッシブ・フィルタ設計で Y コンデンサをエミュレートします。このデバイスは、一連のセンス・コンデンサを使用して各電力線の高周波数ノイズを検出し、注入コンデンサを使用してノイズ・キャンセル電流を電力線に戻します。実効アクティブ容量は、回路のゲインと注入容量によって設定されます。AEF センシングおよび注入インピーダンスは、小さい部品フットプリントで比較的小さい容量値を使用します。このデバイスには、フィルタリング、補償および保護回路、イネーブル入力が内蔵されています。

TPSF12C3-Q1 は、EMI 測定の対象となる周波数範囲で、CM ノイズに対して非常に低いインピーダンス・パスを実現します。仕様の周波数範囲の下限 (150kHz～3MHz など) で最大 30dB の CM ノイズ低減を実現すると、CM フィルタ実装のサイズ、重量、コストを大幅に削減できます。

パッケージ情報

部品番号	パッケージ(1)	本体サイズ (公称)
TPSF12C3-Q1	DYY (SOT-23-THIN、14)	4.20mm × 2.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



EMI 低減結果

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4 Revision History

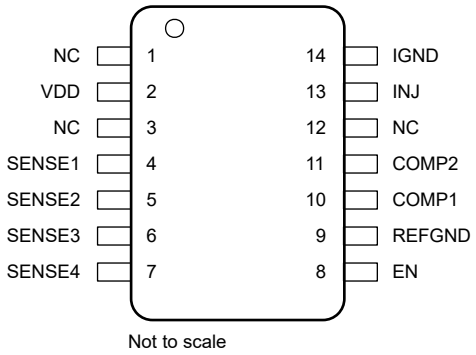
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (January 2023) to Revision A (April 2023)	Page
• ステータスを「事前情報」から「量産データ」に変更	1

5 Device Comparison Table

DEVICE	ORDERABLE PART NUMBER	PHASES	GRADE	JUNCTION TEMPERATURE RANGE
TPSF12C3-Q1	TPSF12C3QDYYRQ1	3	Automotive	–40°C to 150°C
TPSF12C1-Q1	TPSF12C1QDYYRQ1	1	Automotive	–40°C to 150°C
TPSF12C3	TPSF12C3DYYR	3	Commerical	–40°C to 150°C
TPSF12C1	TPSF12C1DYYR	1	Commercial	–40°C to 150°C

6 Pin Configuration and Functions



Not to scale

図 6-1. 14-Pin SOT-23-THIN DYY Package (Top View)

表 6-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1, 3, 12	NC	–	No internal connection. Tie to the GND plane on the PCB.
2	VDD	P	Power supply for IC. Bypass to IGND with a 1-µF X7R ceramic capacitor.
4	SENSE1	I	Sense input (power line 1, 2, 3, or neutral)
5	SENSE2	I	Sense input (power line 1, 2, 3, or neutral)
6	SENSE3	I	Sense input (power line 1, 2, 3, or neutral)
7	SENSE4	I	Sense input (power line 1, 2, 3, or neutral)
8	EN	I	Enable signal to activate noise cancellation
9	REFGND	G	Reference ground (Kelvin connected to IGND)
10	COMP1	I	Connection 1 for external compensation circuit
11	COMP2	I	Connection 2 for external compensation circuit
13	INJ	O	Injection signal output
14	IGND	G	Injection ground

(1) P = Power, G = Ground, I = Input, O = Output

7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Pin voltage	VDD to IGND and REFGND	–0.3	18	V
Pin voltage	SENSE1, SENSE2, SENSE3, SENSE4 to REFGND	–5.5	5.5	V
Pin voltage	COMP1 to IGND and REFGND	–0.3	5.5	V
Pin voltage	COMP2 to IGND and REFGND	–0.3	15	V
Pin voltage	INJ to IGND	–0.3	V_{VDD}	V
Pin voltage	EN to IGND and REFGND	–0.3	18	V
Pin voltage	IGND to REFGND	–0.3	0.3	V
Sink current	INJ		150	mA
Source current	INJ		150	mA
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD classification level 2		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C4B	Corner pins (1, 7, 8, and 14)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{VDD}	VDD voltage range		8	12	16	V
V_{INJ}	Output voltage range		2.5		V_{VDD} – 2	V
V_{SENSE}	Sense voltage range		–5		5	V
V_{EN}	Pin voltage		0		16	V
I_{INJ}	Output current range	Source and sink magnitude			80	mA
T_A	Operating ambient temperature		–40		105	°C

7.4 Thermal Information

THERMAL METRIC[1]		DYY (SOT-23-THIN) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Limits apply over the junction temperature (T_J) range of –40°C to 150°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{VDD} = 12 V[1].

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	VDD quiescent current	SENSE1, SENSE2, SENSE3, and SENSE4 grounded, V_{EN} = 5 V, 8 V ≤ V_{VDD} ≤ 16 V	6.25	13.2	25.5	mA
		SENSE1, SENSE2, SENSE3, and SENSE4 grounded, V_{EN} = 5 V, V_{VDD} = 12 V, T_J = 25°C	11	13.2	15.5	
I_{SD}	VDD shutdown supply current	V_{EN} = 0 V		55		µA
SUPPLY VOLTAGE UVLO						
$V_{VDD-UV-R}$	UVLO rising threshold	V_{VDD} rising	7.35	7.7	7.95	V
$V_{VDD-UV-F}$	UVLO falling threshold	V_{VDD} falling	6.4	6.7	7.0	V
$V_{VDD-UV-HYS}$	UVLO hysteresis			0.97		V
ENABLE						
V_{EN-H}	EN voltage high		2.2			V
V_{EN-L}	EN voltage low				0.8	V
R_{EN}	EN pin pull-up resistance to VDD	V_{EN} = 0 V		850		kΩ
I_{EN-LKG}	EN input leakage current	V_{EN} = 12 V		840		nA
INPUT FILTER NETWORK						
A_{CM}	Gain from shorted power lines through single sense cap, C_{SEN}, to COMP1 vs. REFGND	C_{SEN} = 2 µF[2], 60 Hz		–44		dB
		C_{SEN} = 2 µF[2], 50 kHz		–4		
		C_{SEN} = 2 µF[2], 500 kHz[3]		–2		
		C_{SEN} = 2 µF[2], 1 MHz[3]		–1		

7.5 Electrical Characteristics (continued)

Limits apply over the junction temperature (T_J) range of –40°C to 150°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{VDD} = 12 V(1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
A_{DM}	Gain from differential signal applied to SENSE lines to COMP1 vs. REFGND	SENSE1 shorted to SENSE2, SENSE3 shorted to SENSE4, C_{SEN1} = C_{SEN3} = 1 µF(2), 60 Hz		–71		dB
		SENSE1 shorted to SENSE2, SENSE3 shorted to SENSE4, C_{SEN1} = C_{SEN3} = 1 µF(2), 1 kHz		–59		
		SENSE1 shorted to SENSE2, SENSE3 shorted to SENSE4, C_{SEN1} = C_{SEN3} = 1 µF(2), 500 kHz(3)		–42		
		SENSE1 shorted to SENSE2, SENSE3 shorted to SENSE4, C_{SEN1} = C_{SEN3} = 1 µF(2), 1 MHz(3)		–43		
		SENSE1 shorted to SENSE2, SENSE3 shorted to SENSE4, C_{SEN1} = C_{SEN3} = 1 µF(2), 10 MHz(3)		–35		
AMPLIFIER						
A_{DC}	DC gain		52	58	69	dB
f_{BW}	Unity gain bandwidth(3)			113		MHz
f_{BW40}	40 dB gain frequency			1		MHz
V_{OFST}	COMP1 offset voltage			2		V
$V_{INJ-MAX}$	Maximum output voltage for linear operation(3)	COMP2 to INJ gain > 36 dB	V_{VDD} – 2			V
$V_{INJ-MIN}$	Minimum output voltage for linear operation(3)	COMP2 to INJ gain > 36 dB			2.5	V
$I_{INJ-MAX-OP}$	INJ current at linearity limits(3)	V_{INJ} = V_{VDD} – 2 V	80			mA
		V_{INJ} = V_{IGND} + 2.5 V			–80	mA
PSRR						
$PSRR_{10}$		10 pF in parallel with the series combination of 10 nF and 2 kΩ between COMP1 and COMP2, 10 kHz		0		dB
$PSRR_{100}$		10 pF in parallel with the series combination of 10 nF and 2 kΩ between COMP1 and COMP2, 100 kHz		6		
STARTUP						
t_W	Startup delay(3)	Time from VDD = EN applied until output valid		43		ms
t_{SU}	EN high to valid output			42		ms
t_{SD}	EN low to stop output signal			0.32		µs
THERMAL SHUTDOWN						
T_{J-SHD}	Thermal shutdown threshold(3)	Temperature rising		175		°C
T_{J-HYS}	Thermal shutdown hysteresis(3)			20		°C

(1) MIN and MAX limits are 100% production tested at 25ºC unless otherwise specified. Limits over the operating temperature range verified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Capacitance chosen for effective test only. Do not use this capacitance in applications.
(3) Parameter specified by design, statistical analysis and production testing of correlated parameters.

7.6 System Characteristics

The following specifications apply only to the typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C and V_{VDD} = 12 V only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of T_J = –40°C to 150°C. These specifications are not ensured by production testing.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_{SUPPLY}	Input supply current with INJ loaded			15		mA

7.7 Typical Characteristics

V_{VDD} = V_{EN} = 12 V, unless otherwise specified.

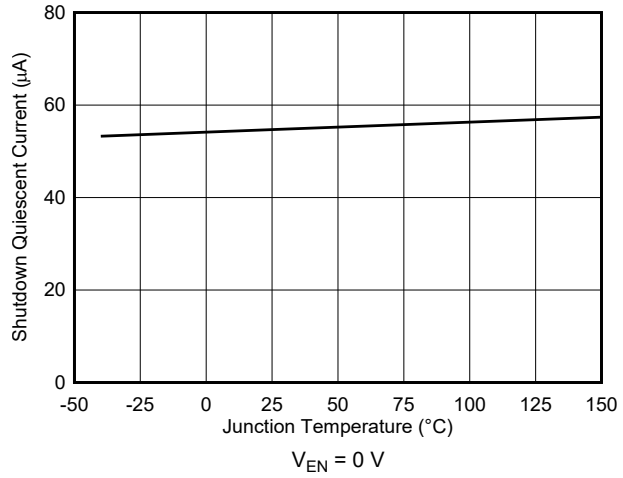


図 7-1. Shutdown Supply Current vs. Temperature

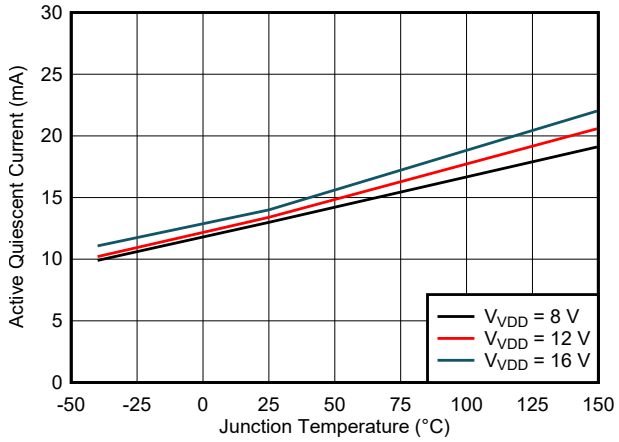


図 7-2. Quiescent Supply Current vs. Temperature

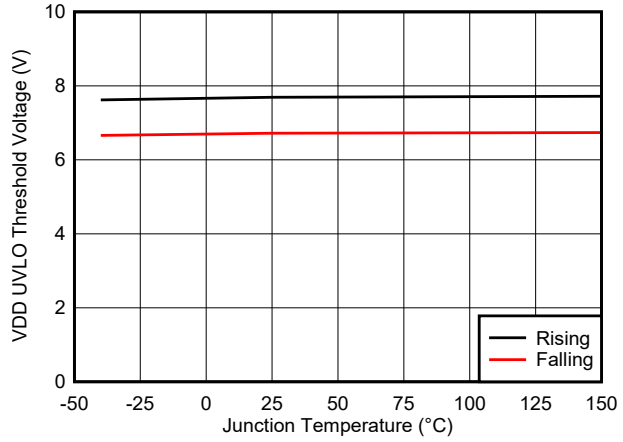


図 7-3. VDD UVLO Thresholds vs. Temperature

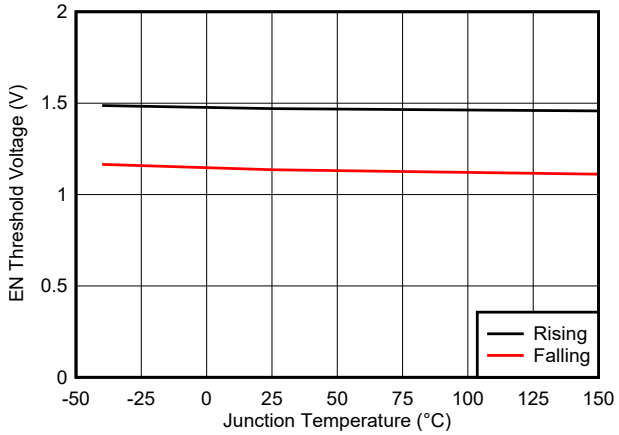


図 7-4. EN Threshold vs. Temperature

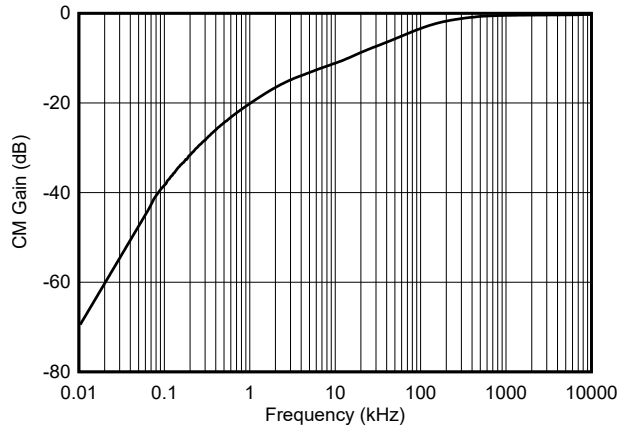


図 7-5. Input Filter Response – Common Mode

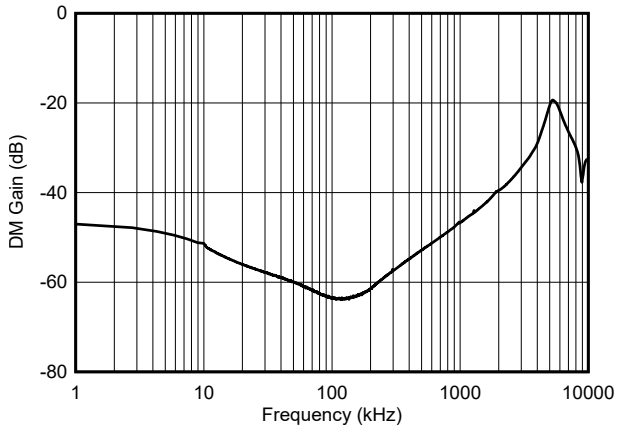


図 7-6. Input Filter Response – Differential Mode

8 Detailed Description

8.1 Overview

The TPSF12C3-Q1 is an active electromagnetic interference (EMI) filter that is designed to reduce common-mode (CM) conducted emissions in off-line power converter systems. Using a VSCI architecture, the device senses the high-frequency noise on each power line using a set of Y-rated capacitors, C_{SEN1-4}, then injects noise-canceling currents back into the power lines using a Y-rated capacitor, C_{INJ}, along with a damping circuit that ensures stability. The device includes integrated filtering, compensation and protection circuitry.

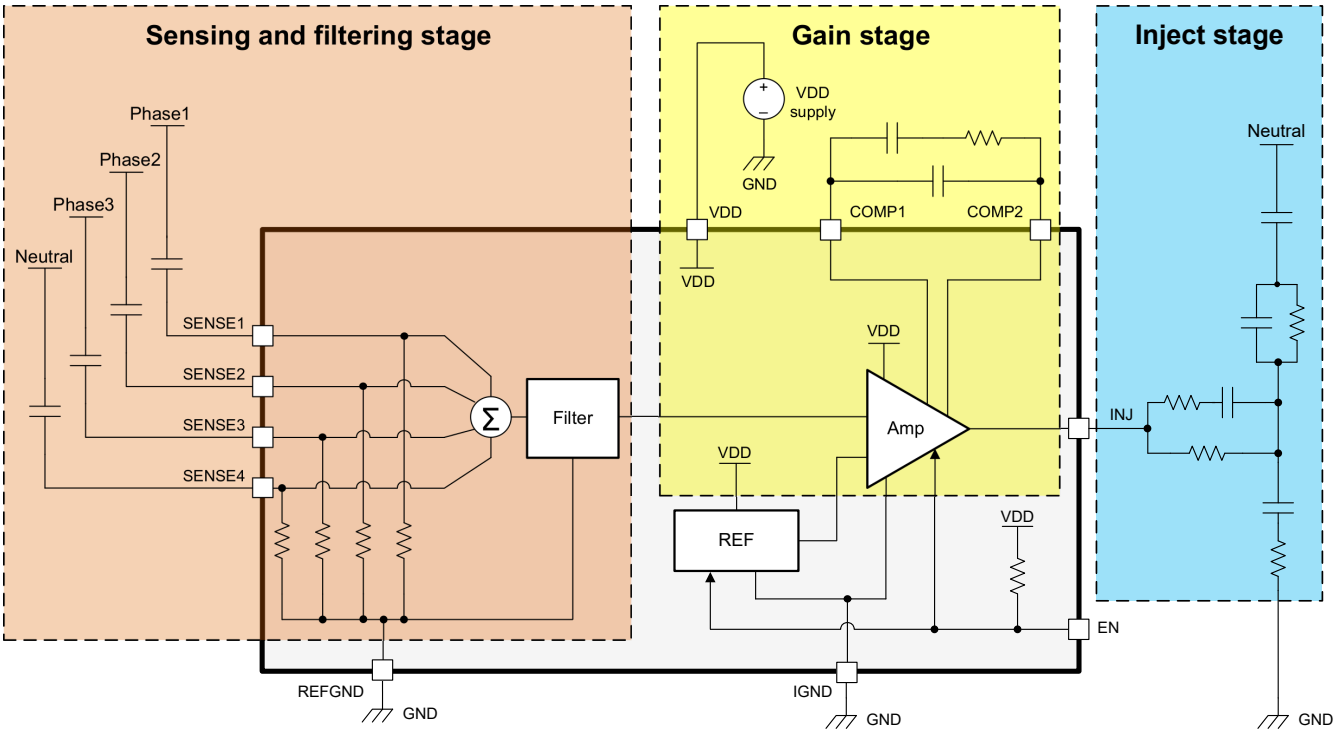
The TPSF12C3-Q1 provides a low-impedance shunt path for CM noise in the frequency range of interest for EMI measurement. This feature can achieve approximately 15 to 30 dB of CM attenuation over the applicable frequency range (for example, 100 kHz to 3 MHz) helping to reduce the size of CM chokes, typically the largest components in the filter.

The TPSF12C3-Q1 operates over a supply voltage range of 8 V to 16 V and can withstand 18 V. The device features include:

- Internal circuitry that simplifies compensation and design
- Built-in supply voltage UVLO to ensure proper operation
- Built-in thermal shutdown protection
- An EN input that allows power saving when the system is idling

The active EMI filter circuit significantly reduces EMI filter cost, size, and weight, while helping to meet CISPR 25 Class 5 limits for conducted emissions. Leveraging a pin arrangement designed for simple layout that requires relatively few external components, the TPSF12C3-Q1 is specified for maximum ambient and junction temperatures of 105°C and 150°C, respectively.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Active EMI Filtering

A compact and efficient design of the input EMI filter is one of the main challenges in high-density switching regulator design and is critical to achieving the full benefits of electrification in highly constrained system

environments such as automotive. For AC-input applications in general, CM chokes and Y-capacitors provide CM filtering, whereas the leakage inductance of the CM chokes and the X-capacitors provide DM filtering. However, CM filters for such applications may have limited Y-capacitance due to touch-current safety requirements and thus require large-sized CM chokes to achieve the requisite attenuation – ultimately resulting in filter designs with bulky, heavy and expensive passive components. Fortunately, the deployment of active filter circuits enable more compact filter solutions for next-generation power conversion systems.

8.3.1.1 Schematics

図 8-1 and 図 8-2 show schematics for conventional two-stage passive EMI filters with and without neutral, respectively, in kilowatt-scale, grid-connected applications. L, N and PE refer to the respective live, neutral and protective earth connections. Multistage filters as shown provide high roll-off and are widely used in high-power AC line applications where CM noise is often more challenging to mitigate than DM noise. The low-order switching harmonics usually dictate the size of the reactive filter components based on the required corner frequency (or multiple corner frequencies in multistage designs).

Also included in 図 8-1 and 図 8-2 are the corresponding active filter designs. The active circuit replaces the bank of Y-capacitors positioned between the CM chokes with a three-phase AEF circuit using the TPSF12C3-Q1 to provide a lower impedance shunt path for CM currents. The sense pins of the TPSF12C3-Q1 interface with the power lines using a set of Y-rated sense capacitors, typically 680 pF, and feed into an internal high-pass filter and signal combiner. The IC rejects both line-frequency (50-Hz or 60-Hz) AC voltage as well as DM disturbances, while amplifying high-frequency CM disturbances and maintaining closed-loop stability using an external tunable damping circuit.

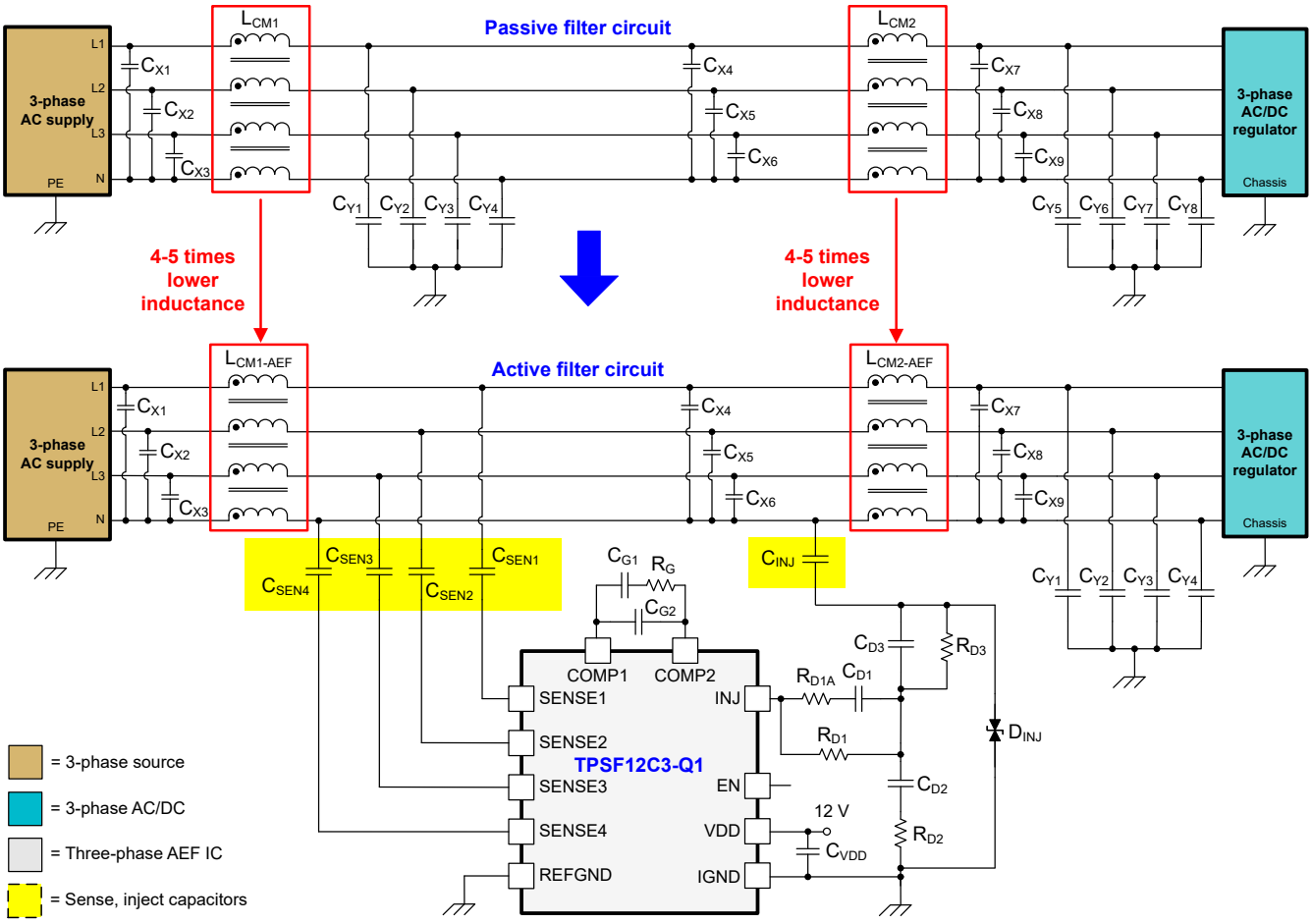


図 8-1. Circuit Schematic of a Three-Phase, Four-Wire Passive Filter and Corresponding Active Filter Solution for CM Attenuation

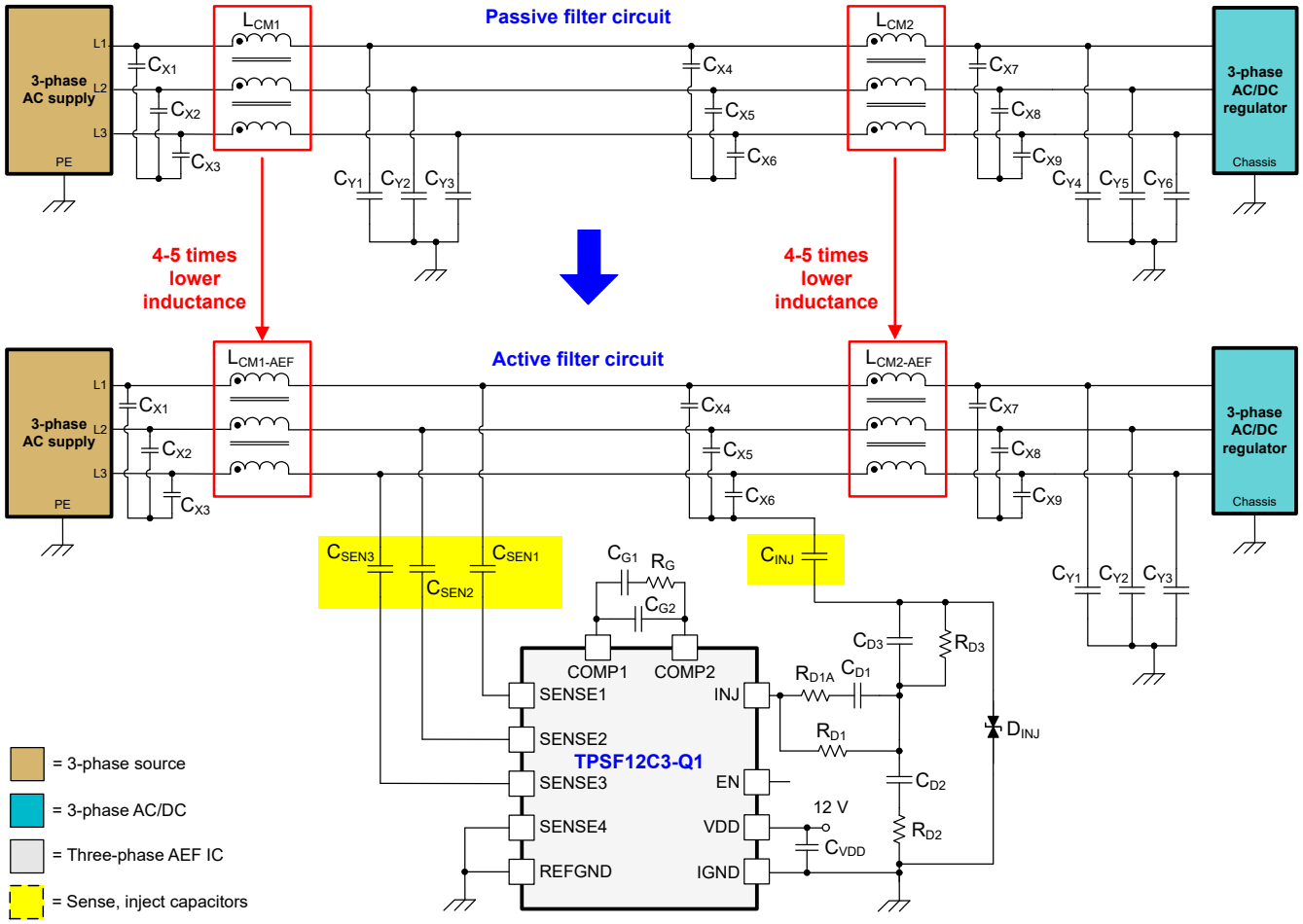


図 8-2. Circuit Schematic of a Three-Phase, Three-Wire Passive Filter and Corresponding Active Filter Solution for CM Attenuation

The X-capacitors placed between the two CM chokes effectively provide a low-impedance path between the power lines from a CM standpoint, typically up to low-MHz frequencies. This allows current injection onto one power line, typically neutral, using only one inject capacitor. If the three-phase filter is a three-wire system without neutral as shown in 図 8-2, the SENSE4 pin of the TPSF12C3-Q1 ties to ground and the inject capacitor couples through a star-point connection of the X-capacitors.

8.3.2 Capacitive Amplification

An AEF circuit for CM noise mitigation fundamentally either amplifies the apparent inductance of a CM choke or the apparent capacitance of a Y-capacitor over the frequency range of interest. A VSCI AEF circuit configured for CM attenuation uses an amplifier stage as a capacitive multiplier of the inject capacitor, C_{INJ}. This higher value of the active capacitance supports lower values for the CM chokes to achieve a target attenuation. More specifically, the amplified Y-capacitance enables a reduction of each CM choke inductance by up to 80% (while keeping the filter corner frequencies effectively unchanged), resulting in lower size, weight, and cost of the CM chokes.

Capacitive multiplication of the inject capacitance occurs over a relevant frequency range for low- and mid-frequency emissions, while not impacting the value at low frequency applicable for touch current measurement. The total capacitance of the sense and inject capacitors (highlighted in yellow in 図 8-1 and 図 8-2) is kept less than or equal to that of the replaced Y-capacitors in the equivalent passive filter, which results in the total line-frequency leakage current remaining effectively unchanged or reduced.

8.3.3 Integrated Line Rejection Filter

The TPSF12C3-Q1 has a built-in input line filter. The high-pass filter stage attenuates the large line-frequency (50 Hz or 60 Hz) components of the power-line voltages, both line-to-line and line-to-earth, thus maximizing the useful voltage range of the low-voltage output at INJ.

The circuit also sums the signals in a CM combiner, rejecting the DM components of the voltages and extracting a signal that represents the CM noise signature without line-frequency components. Combined with the action of the high-pass filter, the net result is that the COMP1 pin voltage represents the sensed high-frequency CM noise that the device attempts to cancel. Because the entire filter is integrated in the device, matching is better than what can be achieved using discrete components.

8.3.4 Compensation

The TPSF12C3-Q1 contains partial internal compensation that, when combined with two capacitors and a resistor between COMP1 and COMP2, forms a lead-lag network. This internal network allows fewer external components to be used.

8.3.5 Remote Enable

The TPSF12C3-Q1 has an enable input, EN, that allows the device to be shut down, drastically reducing power consumption during intervals when EMI mitigation is not required. The typical quiescent current consumption is 13.2 mA and 55 µA when the device is enabled and disabled, respectively. Because many designs may not use this feature, a 850-kΩ pullup resistor connects internally between VDD and EN, allowing the EN pin to be left open.

In addition, INJ is pulled low when the device is disabled to reduce the effective resistance in series with C_{INJ}.

8.3.6 Supply Voltage UVLO Protection

To ensure that the TPSF12C3-Q1 operates safely while VDD is powered on and off as well as during brownout conditions, this device has a built-in UVLO protection to provide predictable behavior while VDD is below its operating voltage. UVLO releases when the VDD voltage exceeds 7.7 V (typical), allowing normal operation. UVLO engages if the VDD voltage falls below approximately 6.7 V (typical). There is approximately 1 V of UVLO hysteresis.

8.3.7 Thermal Shutdown Protection

The TPSF12C3-Q1 provides built-in overtemperature protection that shuts down the device if the junction temperature exceeds approximately 175°C. After the junction temperature decreases by approximately 20°C, the device restarts. This process is repeated until the ambient temperature or power dissipation is reduced. The device has a relatively low thermal time constant and can cycle into and out of thermal shutdown at a high rate during a sustained overtemperature condition.

8.4 Device Functional Modes

8.4.1 Shutdown Mode

The EN pin provides ON and OFF control for the TPSF12C3-Q1. When the EN voltage is below approximately 0.8 V, the device is in shutdown mode. Most internal circuitry is shutdown. The quiescent current in shutdown mode drops to 55 µA (typical). The TPSF12C3-Q1 also employs VDD internal undervoltage protection. If the VDD voltage is below its UVLO threshold, the device remains off. The INJ output pulls to ground while in shutdown mode.

8.4.2 Active Mode

The TPSF12C3-Q1 is in active mode when V_{VDD} is above its UVLO threshold, EN is high, and there is no overtemperature fault. The simplest way to enable operation is to connect EN to VDD, which allows startup when the applied supply voltage exceeds the UVLO threshold voltage. In this mode, the device amplifies signals on COMP2 and outputs the amplified signal on the INJ pin.

9 Applications and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPSF12C3-Q1 common-mode AEF IC helps to improve the CM EMI signature of three-phase AC power systems. The device provides a very low impedance path for CM noise in the frequency range of interest for EMI measurement and helps to meet prescribed limits for EMI standards, such as:

- CISPR 11, EN 55011 – Industrial, Scientific and Medical (ISM) applications
- CISPR 25, EN 55025 – Automotive applications
- CISPR 32, EN 55032 – Multimedia applications

To expedite and streamline the process of designing of a TPSF12C3-Q1-based solution, a comprehensive TPSF12C3-Q1 quickstart calculator is available by download to assist the system designer with component selection for a given application.

9.2 Typical Applications

For the circuit schematic, bill of materials, PCB layout files, and test results of a TPSF12C3-Q1-powered implementation, see the TPSF12C3-Q1 EVM.

9.2.1 Design 1 – AEF Circuit for High-Density On-Board Charger (OBC) in Electric Vehicles (EVs)

図 9-1 shows a schematic diagram of a 22-kW high-density OBC with conventional two-stage passive EMI filter. The CM chokes and Y-capacitors provide CM filtering, whereas the leakage inductance of the CM chokes and the X-capacitors provide DM filtering. The circuit uses a three-phase power-factor correction (PFC) front-end followed by a full-bridge CLLLC topology with active synchronous rectification.

The PFC stage runs at a fixed switching frequency of 100 kHz. The CLLLC isolated DC/DC stage runs at a variable frequency from 200 kHz to 800 kHz (500-kHz nominal) and provides galvanic isolation in addition to battery voltage and current regulation. Even though the use of GaN or SiC power switches enables a high power density, the conventional passive EMI filter typically occupies over 20% of the total solution size.

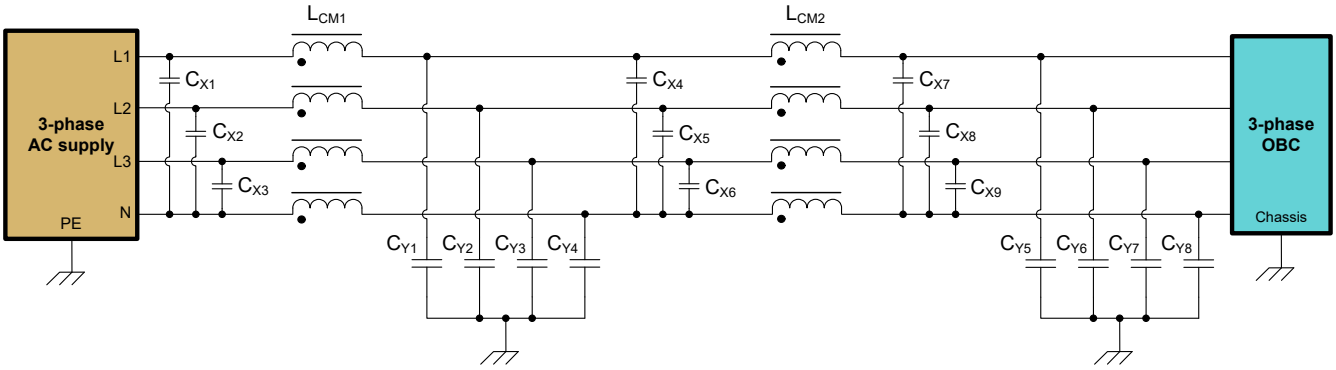


図 9-1. Circuit Schematic of a Three-phase OBC With a Conventional Two-Stage Passive EMI Filter

Note that the DC/DC stage in particular increases the CM EMI signature based on the high dv/dt of the GaN power switches, the transformer interwinding capacitance as well as the various switch-node parasitic capacitances to chassis ground.

This application example replaces the four Y-capacitors, designated as C_{Y1}, C_{Y2}, C_{Y3} and C_{Y4} in 図 9-1, with a three-phase AEF circuit using the TPSF12C3-Q1. See 図 9-2. The AEF circuit effectively provides capacitive multiplication of the inject capacitor, which reduces the CM inductance values to maintain the target LC corner frequencies and thus the size, weight, and cost of the CM chokes, now designated as $L_{CM1\text{-}AEF}$ and $L_{CM2\text{-}AEF}$. The total capacitance of the sense and inject capacitors is kept less than or equal to that of the replaced Y-capacitors, which results in the total line-frequency leakage current remaining effectively unchanged or reduced.

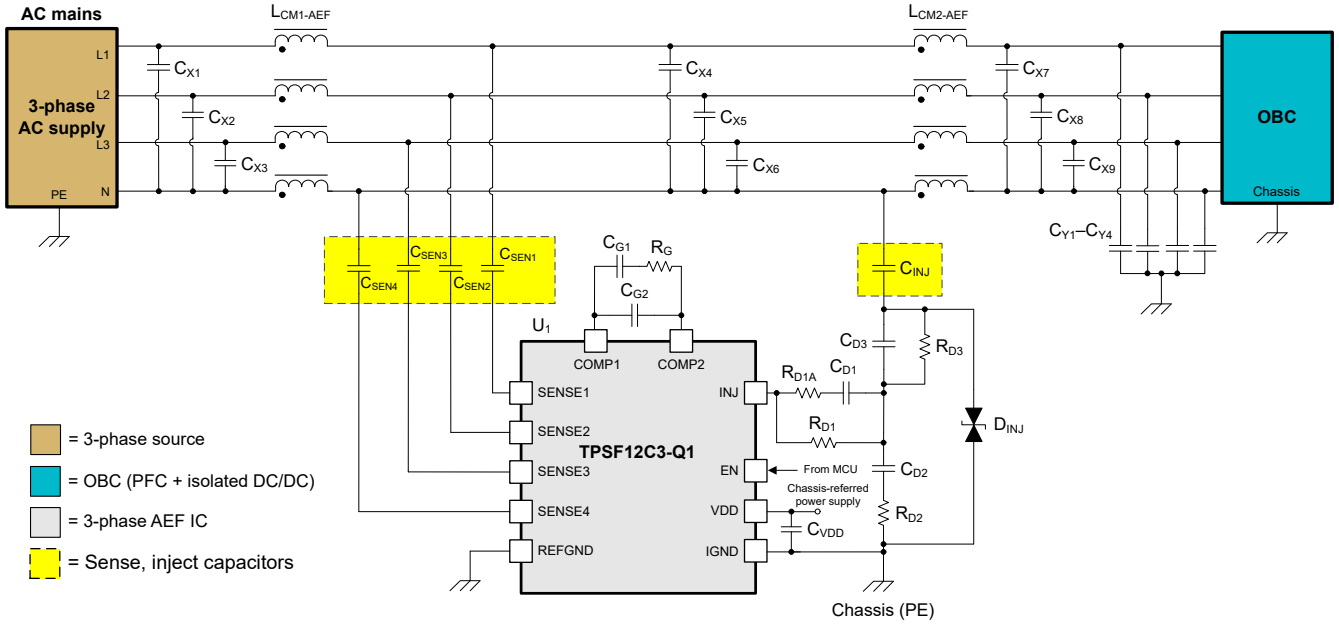


図 9-2. Circuit Schematic of a Three-phase OBC With AEF Circuit Connected

9.2.1.1 Design Requirements

表 9-1 shows the intended operating parameters for this application example. Also included is the total Y-rated filter capacitance that is allowed in order to meet the applicable touch current fault specification.

表 9-1. Design Parameters

DESIGN PARAMETER	VALUE
AC input voltage	230 V L-N or 400 V L-L (RMS)
AC input line frequency	47 Hz to 63 Hz
DC output voltage range	250 V to 450 V
Rated output power	22 kW
Output current (maximum)	60 A
AC/DC stage switching frequency (fixed)	100 kHz
DC/DC stage switching frequency (variable)	200 kHz to 800 kHz
Total Y-rated filter capacitance (maximum)	10 nF

9.2.1.2 Detailed Design Procedure

表 9-2 gives the selected component values, which are the same as those used in the TPSF12C3-Q1 EVM. This design uses a TVS diode placed at the low-voltage side of the inject capacitor for clamping during input surge conditions.

表 9-2. AEF Circuit Components for Application Circuit 1

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER(1)	PART NUMBER
C_{SEN1}, C_{SEN2}, C_{SEN3}, C_{SEN4} (2)	4	Capacitor, ceramic, 680 pF, 300 VAC, Y2	MuRata	DE2B3SA681KN3AX02F
C_{INJ} (2)	1	Capacitor, ceramic, 4.7 nF, 300 VAC, Y2	MuRata	DE2E3SA472MA3BX02F
C_{D1} (2)	1	Capacitor, ceramic, 4.7 nF, 50 V, 0603	Various	–
C_{D2} (2)	1	Capacitor, ceramic, 22 nF, 50 V, 0603	Various	–
C_{D3}	1	Capacitor, ceramic, 4.7 nF, 50 V, 0603	Various	–
C_{G1}	1	Capacitor, ceramic, 10 nF, 50 V, 0603	Various	–
C_{G2}	1	Capacitor, ceramic, 10 pF, 50 V, 0603	Various	–
C_{VDD}	1	Capacitor, ceramic, 1 µF, 25 V, X7R, 0603	Various	–
D_{INJ}	1	TVS diode, bidirectional, 24 V, SOD-323	Eaton	STS321240B301
R_{D1}	1	Resistor, 1 kΩ, 0.1 W, 0603	Various	–
R_{D1A}	1	Resistor, 50 Ω, 0.1 W, 0603	Various	–
R_{D2}	1	Resistor, 200 Ω, 0.1 W, 0603	Various	–
R_{D3}	1	Resistor, 698 Ω, 0.1 W, 0603	Various	–
R_G	1	Resistor, 1.5 kΩ, 0.1 W, 0603	Various	–
U_1	1	TPSF12C3-Q1 common-mode AEF IC for three-phase AC power systems	Texas Instruments	TPSF12C3QDYYRQ1

(1) See the *Third-Party Products Disclaimer*.
(2) Check the effective capacitance value based on the applied voltage and operating temperature.

More generally, the TPSF12C3-Q1 AEF IC is designed to operate with a wide range of passive filter components and system parameters.

9.2.1.2.1 Sense Capacitors

The sense pins of the TPSF12C3-Q1 feed into a high-pass filter and signal combiner within the IC, which rejects the line-frequency and DM components of the power line voltages, extracting the high-frequency CM component.

The sense pins externally interface to the power lines using Y-rated capacitors, designated as C_{SEN1}, C_{SEN2}, C_{SEN3} and C_{SEN4} in Figure 9-2. Choose Y2-rated sense capacitors of 680 pF, 300 VAC in this application to establish voltages at the SENSE pins of less than 1-V peak-to-peak when operating at maximum line voltage.

9.2.1.2.2 Inject Capacitor

The INJ node interfaces to a power line using a Y-rated capacitor, designated as C_{INJ} in Figure 9-2. Choose a Y2-rated inject capacitor of 4.7 nF, 300 VAC in this design to accommodate an AC voltage swing at INJ with at least a 2.5-V margin of headroom from the positive and negative supply rails. The INJ pin biases at half the VDD supply voltage. Assuming a 12-V supply rail and allowing 2.5 V of upper and lower headroom, this implies that a swing of ±3.5 V is available around the DC operating midpoint.

注

Many commercially available Y-rated capacitors yield an effective capacitance that derates significantly with operating temperature. The effective capacitance value can be much lower than the nameplate capacitance, particularly when operating near the boundaries of the rated operating temperature range. Select the dielectric of the sense and inject capacitors to meet the required temperature range. Depending on the implementation, lower than expected sense and inject capacitances can affect the stability performance.

9.2.1.2.3 Compensation Network

The CM noise signal derived from the internal sensing filter and summation network of the TPSF12C3-Q1 is internally inverted and amplified by a gain stage. The components between the COMP1 and COMP2 pins of the IC, designated as as R_G, C_{G1} and C_{G2} in Figure 9-2, set the gain characteristic.

More specifically, resistor R_G establishes a high midband AEF gain at frequencies where EMI filtering is required. Capacitor C_{G1} increases the impedance of that branch at low frequencies, which sets a lower AEF amplifer gain to further reject line-frequency components appearing at the INJ output. Capacitor C_{G2} preserves gain at high frequencies, which extends the AEF bandwidth.

Choose a value for R_G between 1 kΩ and 2 kΩ. A resistance of 1.5 kΩ is a common choice and selected in this example to set a midband gain of 50 dB. Choose capacitances for C_{G1} and C_{G2} of 10 nF and 10 pF, respectively, which establishes a gain rolloff below approximately 10 kHz for line- and low-frequency attenuation.

9.2.1.2.4 Injection Network

The components connected between the INJ pin and inject capacitor establish a damped injection network. Damping is specifically required to manage resonance between the CM choke inductance and inject capacitance, which manifests in the AEF loop gain as a pair of complex zeros.

図 9-3 highlights three specific RC branches: R_{D1}, R_{D1A} and C_{D1} form one branch from the INJ pin; R_{D2} and C_{D2} in series connect to GND; R_{D3} and C_{D3} in parallel connect to the inject capacitor.

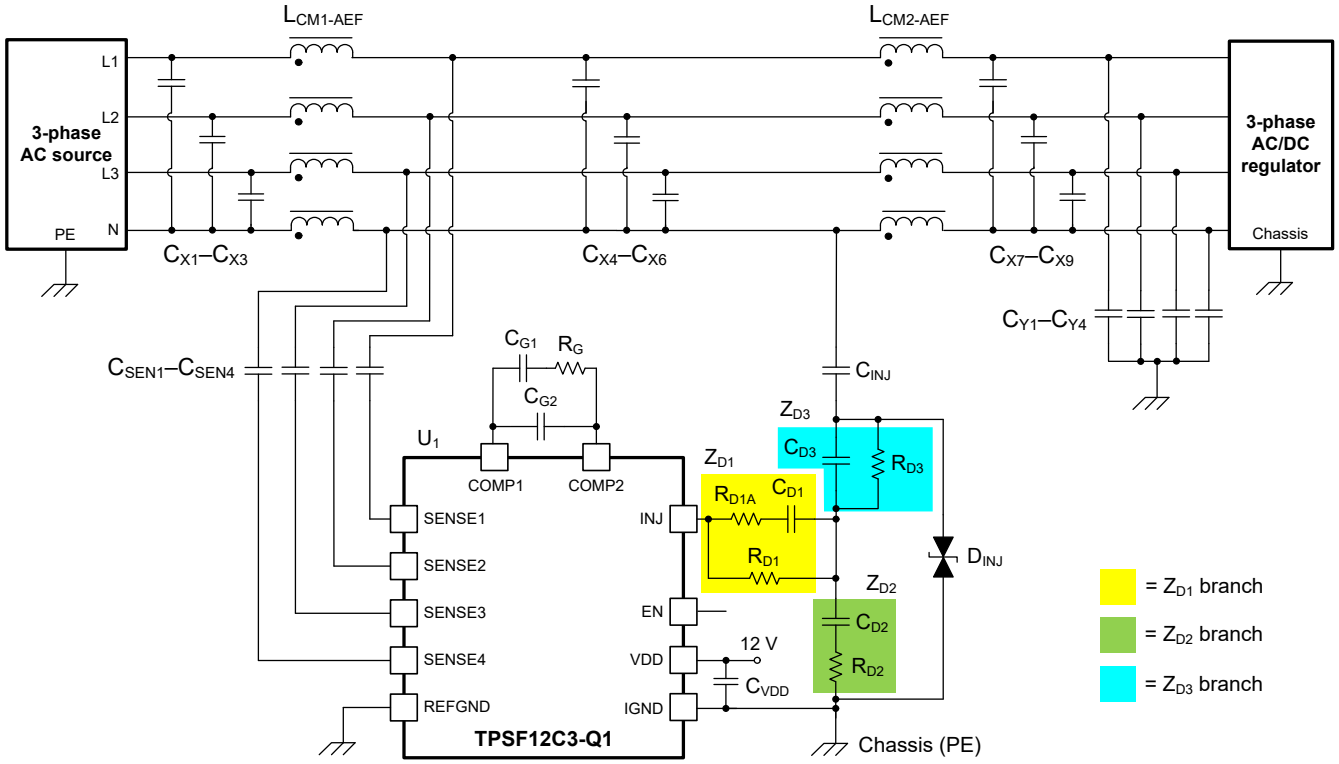


図 9-3. Injection Network

Based on the injection mechanism, the AEF circuit presents a low shunt impedance to CM noise. Given the three damping impedance branches highlighted in 図 9-3, 式 1 approximates the AEF impedance as:

$$Z_{AEF}(s) \approx \frac{Z_{INJ}(s) + Z_{D3}(s) + \left(Z_{D1}(s) \| Z_{D2}(s)\right)}{1 - G_{AEF}(s) \cdot \frac{Z_{D2}(s)}{Z_{D1}(s) + Z_{D2}(s)}} \quad (1)$$

where the term G_{AEF} is the gain from the power lines to the INJ node (see the TPSF12C3-Q1 quickstart calculator for related detail).

式 1 shows that the impedance Z_{INJ} appears in series with Z_{D3} and a parallel combination of Z_{D1} and Z_{D2}. Furthermore, the gain G_{AEF} is reduced by the voltage divider ratio between Z_{D2} and Z_{D1}. These effects combine to increase the effective impedance of the AEF and hence reduce its attenuation performance, thus illustrating a trade-off between performance and stability.

So while an injection network is needed for stability, it also adds impedance in series with the inject capacitor, thus compromising EMI mitigation. As shown below, the user can minimize the impact on performance with careful and appropriate design.

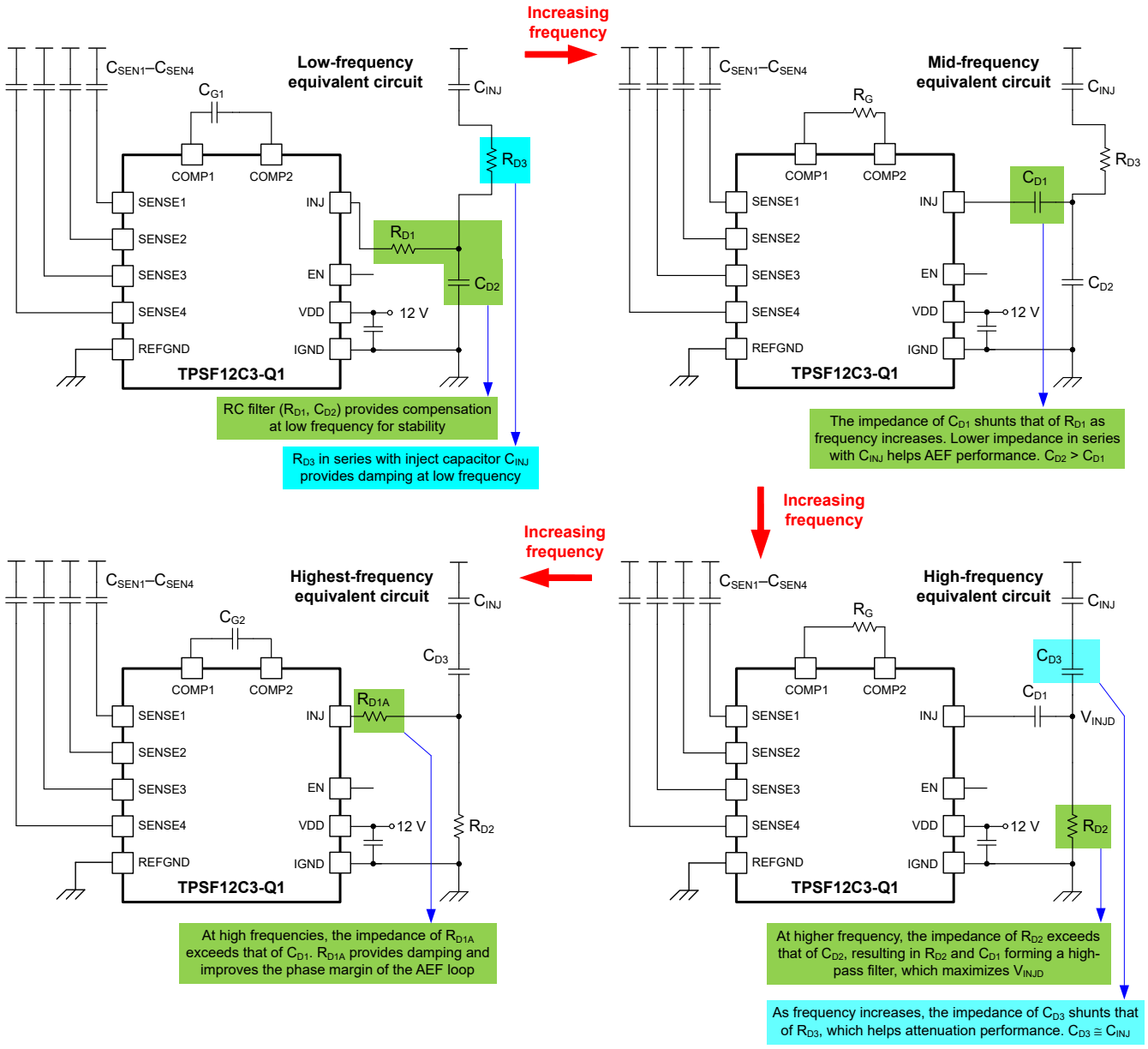


図 9-4. Dominant Components of the Injection Network vs Frequency

Illustrated in 図 9-4, at low frequencies in the range of 5 kHz to 50 kHz, components R_{D1} and C_{D2} provide compensation and R_{D3} damps the effects of LC resonance. At higher frequencies (above 10 kHz), the dominant component impedance of each branch transitions to enable better attenuation performance:

- R_{D1} transitions to C_{D1}
- C_{D2} transitions to R_{D2}
- R_{D3} transitions to C_{D3}

Finally, C_{D1} transitions to R_{D1A} if needed for phase margin of the AEF loop at high frequencies, typically above 100 kHz. When viewed in a clockwise direction, 図 9-4 shows these transitions in sequence as frequency increases.

Below are basic guidelines to select the component values for the injection network:

1. The undamped loop gain characteristic is likely to be unstable within the range of 5 kHz to 50 kHz, which, as mentioned previously, relates to an LC resonance between CM choke inductance and inject capacitance.

Observe from circuit simulation – or by using the TPSF12C3-Q1 quickstart calculator – the frequency, $f_{LFstability}$, at which the phase crosses –180° with positive gain, indicating negative gain margin.

2. Choose a corner frequency with R_{D1} and C_{D2} equal to one fifth of the instability frequency:

$$\frac{1}{2\pi \cdot R_{D1} \cdot C_{D2}} = \frac{f_{LFstability}}{5} \tag{2}$$

Assigning R_{D1} = 1 kΩ and assuming instablity at 35 kHz, use 式 3 to find a value for the capacitance of C_{D2}:

$$C_{D2}\left[nF\right] = \frac{5000}{2\pi \cdot R_{D1}\left[k\Omega\right] \cdot f_{LFstability}\left[kHz\right]} = \frac{5000}{2\pi \cdot 1 \cdot 35} = 22nF \tag{3}$$

3. Select $C_{D1} < C_{D2}$, where a typical choice is $C_{D1} = C_{D2}/5$ = 4.7 nF.
4. Choose the resistance of R_{D2} such that the R_{D2}, C_{D2} corner frequency is equal to that of R_{D1}, C_{D1}:

$$R_{D2}\left[\Omega\right] = \frac{R_{D1}\left[\Omega\right] \cdot C_{D1}\left[nF\right]}{C_{D2}\left[nF\right]} = \frac{R_{D1}\left[\Omega\right]}{5} = \frac{1000}{5} = 200\,\Omega \tag{4}$$

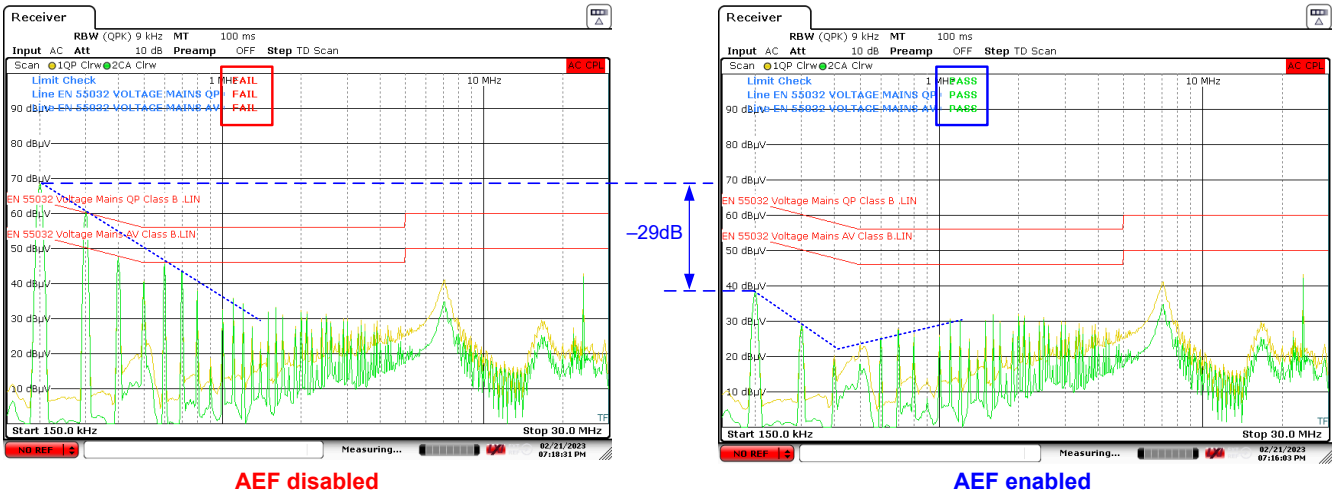
5. Select the resistance of R_{D3} to damp the resonance around the instability frequency, $f_{LFstability}$.
   - A typical choice for R_{D3} is 500 Ω to 1 kΩ.
   - Assign C_{D3} equal to C_{INJ} or a suitable value such that the R_{D3}, C_{D3} corner frequency is less than switching frequency.
   - A lower resistance for R_{D3} results in more damping but at the penalty of reduced high-frequency attenuation (or forces a higher value for C_{D3} to maintain the applicable corner frequency below the switching frequency).
6. Select a resistance for R_{D1A} of 50 Ω to improve the phase margin of the AEF loop (if needed).

9.2.1.2.5 Surge Protection

EMI filter designs, both passive and active, typically use MOVs connected from the power lines to chassis ground to clamp surge voltage transients. While the sense pins of the TPSF12C3-Q1 have internal clamp protection, the higher value of inject capacitance produces larger currents during surge events and thus requires external protection. Place a bidirectional TVS diode on the low-voltage side of the inject capacitor with standoff voltage of 24 V. Using the SOD-323 packaged device given in 表 9-2, clamping occurs at 40 V and 50 V with surge currents of 1 A and 8 A, respectively.

9.2.1.3 Application Curves

Unless otherwise indicated, V_{VDD} = V_{EN} = 12 V.



注

A high DM noise signature may mask improvement in CM noise performance related to AEF. A reduction of CM choke inductance may also reduce leakage inductance, which could impact DM noise attenuation. Install higher X-capacitance or a discrete DM filter inductor to manage DM attenuation as needed. Also, use a DM-CM noise splitter to isolate the CM component of the measured total noise.

図 9-5. EMI Mitigation Result with AEF On and Off (EN Tied High and Low)

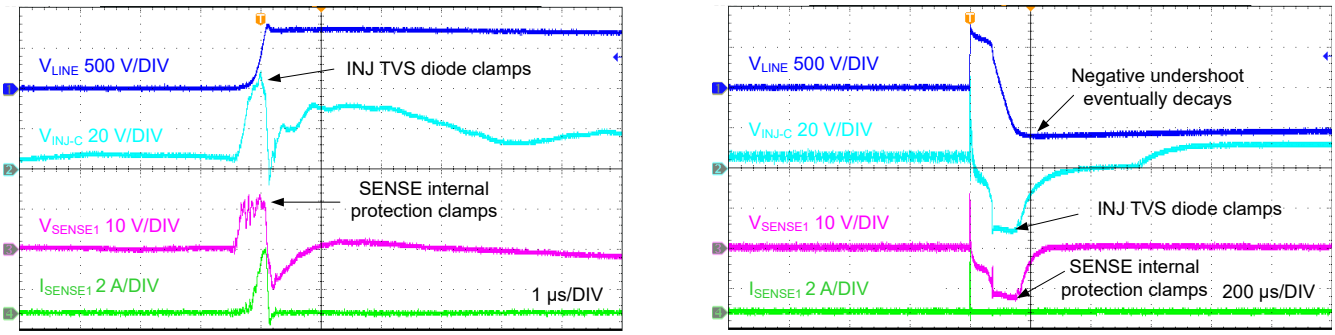
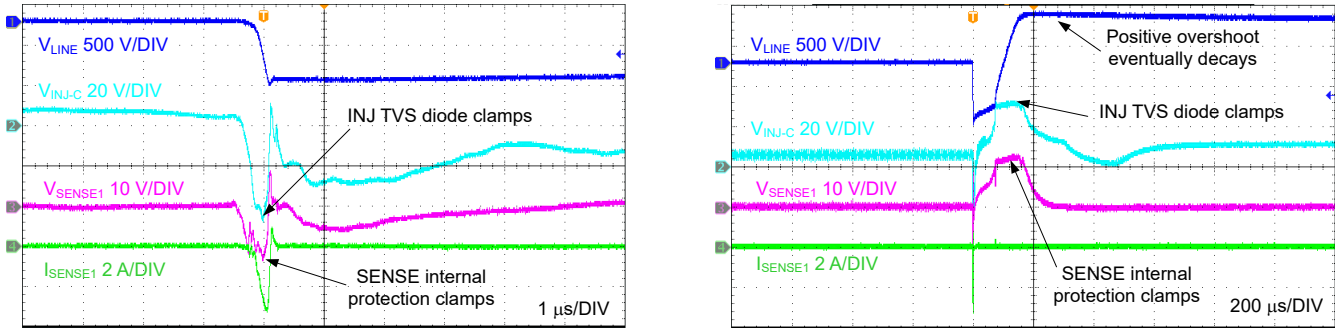
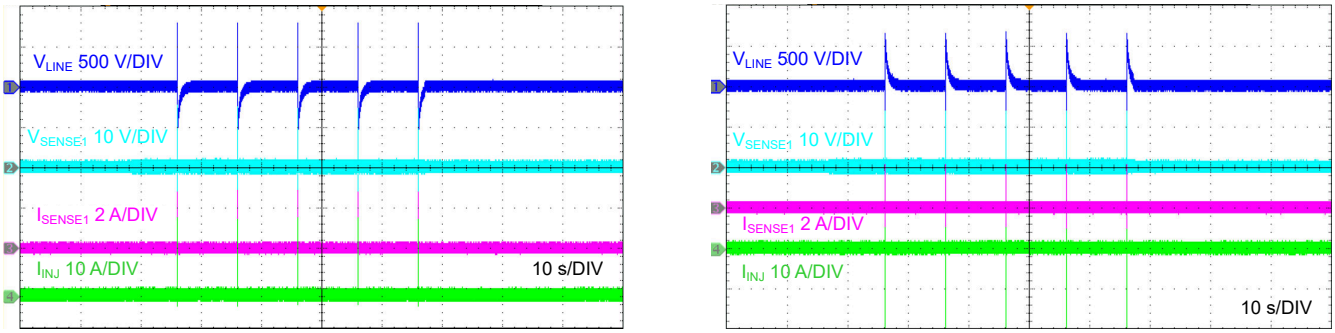


図 9-6. IEC 61000-4-5 Positive Surge, 5-kV Single Strike – 1 µs/div (a), 200 µs/div (b)



(a) (b)

図 9-7. IEC 61000-4-5 Negative Surge, 5-kV Single Strike – 1 µs/div (a), 200 µs/div (b)



(a) (b)

図 9-8. IEC 61000-4-5 Surge, 5-kV Repetitive Strike at 10-Second Intervals – Positive (a), Negative (b)

注

The surge test circuit used MOVs (Littelfuse V20E300P) connected from line and neutral filter inputs to chassis ground. See 図 9-11.

9.3 Power Supply Recommendations

The TPSF12C3-Q1 AEF IC operates over a wide supply voltage range of 8 V to 16 V (typically 12 V) and is referenced to chassis ground of the system. The characteristics of this VDD bias supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* in this data sheet. In addition, the VDD supply must be capable of delivering the required supply current to the loaded AEF circuit.

The supply rail can already be present in the system or can be derived using a low-cost solution with an auxiliary winding from an isolated flyback regulator. Connect a ceramic capacitor of at least 1 µF close to the VDD and IGND pins of the TPSF12C3-Q1. Ensure that the ripple voltage at VDD is less than 20 mV peak-to-peak to avoid low-frequency noise amplification.

9.4 Layout

Proper PCB design and layout is important in active EMI circuits (where high regulator voltage and current slew rates exist) to achieve reliable device operation and design robustness. Furthermore, the EMI performance of the design depends to a large extent on PCB layout.

9.4.1 Layout Guidelines

The following list summarizes the essential guidelines for PCB layout and component placement to optimze AEF performance. 図 9-9 and 図 9-10 show a recommended layout for the TPSF12C3-Q1 circuit specifically with optimized placement and routing of the IC and small-signal components. 図 9-11 shows an example of a three-

phase, four-wire filter board design with CM chokes, X-capacitors, Y-capacitors, protection components (varistors and X-capacitor discharge resistors), and AEF circuit.

- *Position the sense and inject capacitors between the CM chokes near the X-capacitor that couples the injected signal to the other power lines.* Avoid placement close to the CM choke windings that may result in parasitic coupling to the sense and inject capacitors.
- *Maintain adequate clearance spacing between high-voltage and low-voltage traces.* As an example, 図 9-11 has 150 mils (3.8 mm) copper-to-copper spacing from power lines (lives and neutral) to chassis ground.
- *Route the sense lines S1, S2, S3 and S4 away from the INJ line.* Avoid coupling between the sense and inject traces.
- *Use a solid ground connection between the TPSF12C3-Q1 and the filter board.* Minimize parasitic inductance from the AEF circuit return to the chassis ground connections on the board.
- *Place a ceramic capacitor close to VDD and IGND.* Minimize the loop area to the VDD and IGND pins.
- *Place the compensation network copnponents close to the COMP1 and COMP2 pins.* Reduce noise sensitivity of the feedback compensation network path by placing components R_G, C_{G1} and C_{G2} close to the COMP pins. COMP2 is the inverting input to the AEF anplifier and represents a high-impedance node sensitive to noise.
- *Provide enough PCB area for proper heatsinking.* Use sufficient copper area to acheive a low thermal impedance. Provide adequate heatsinking for the TPSF12C3-Q1 to keep the junction temperature below 150°C. A top-side ground plane is an important heat-dissipating area. Use several heat-sinking vias to connect REFGND (pin 9) and IGND (pin 14) to ground copper on other layers.

9.4.2 Layout Example

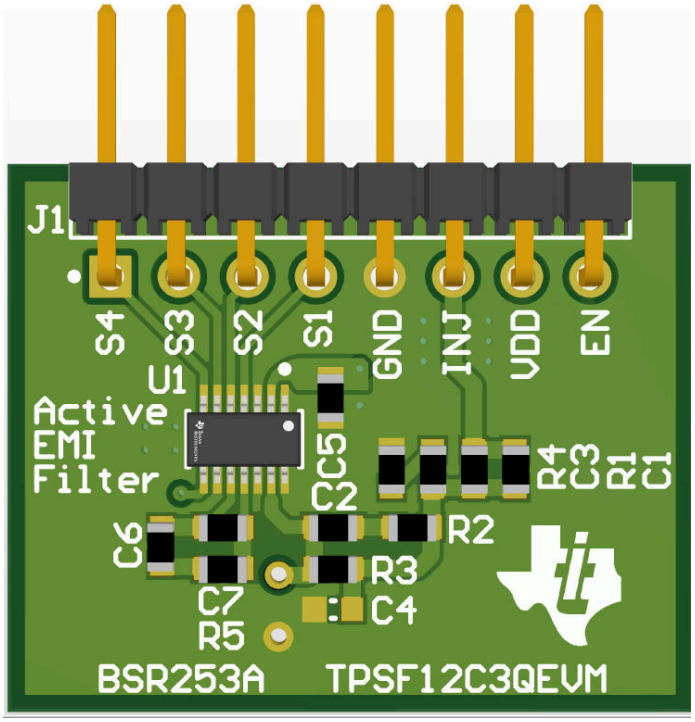


図 9-9. Typical Layout

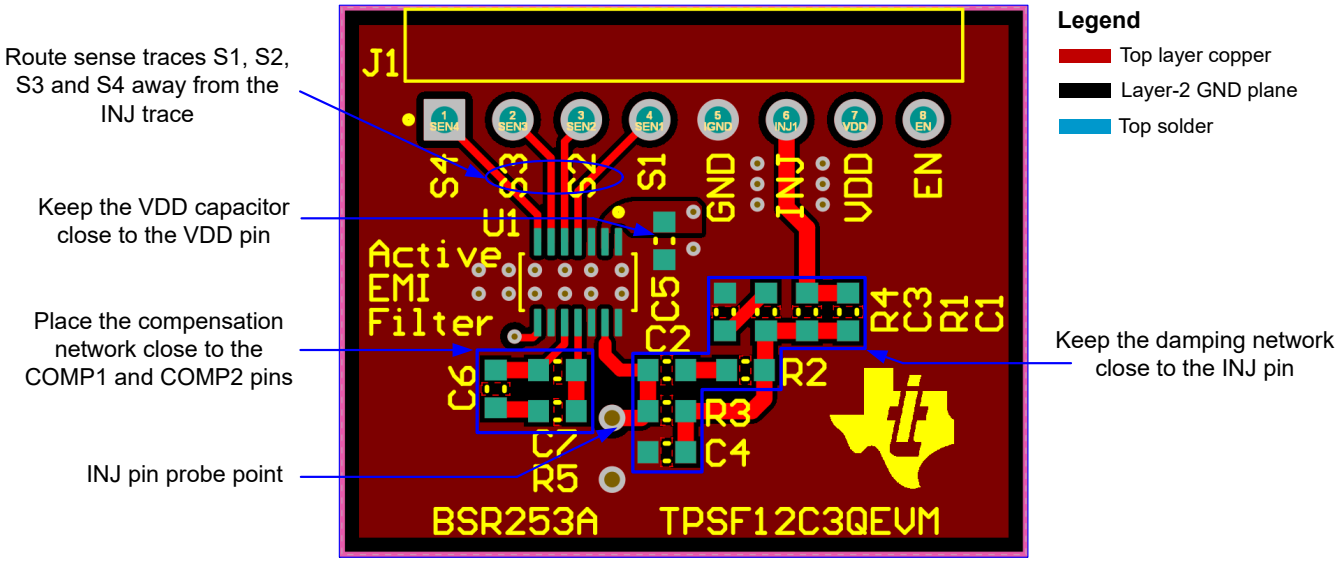


図 9-10. Typical Top-Layer Design

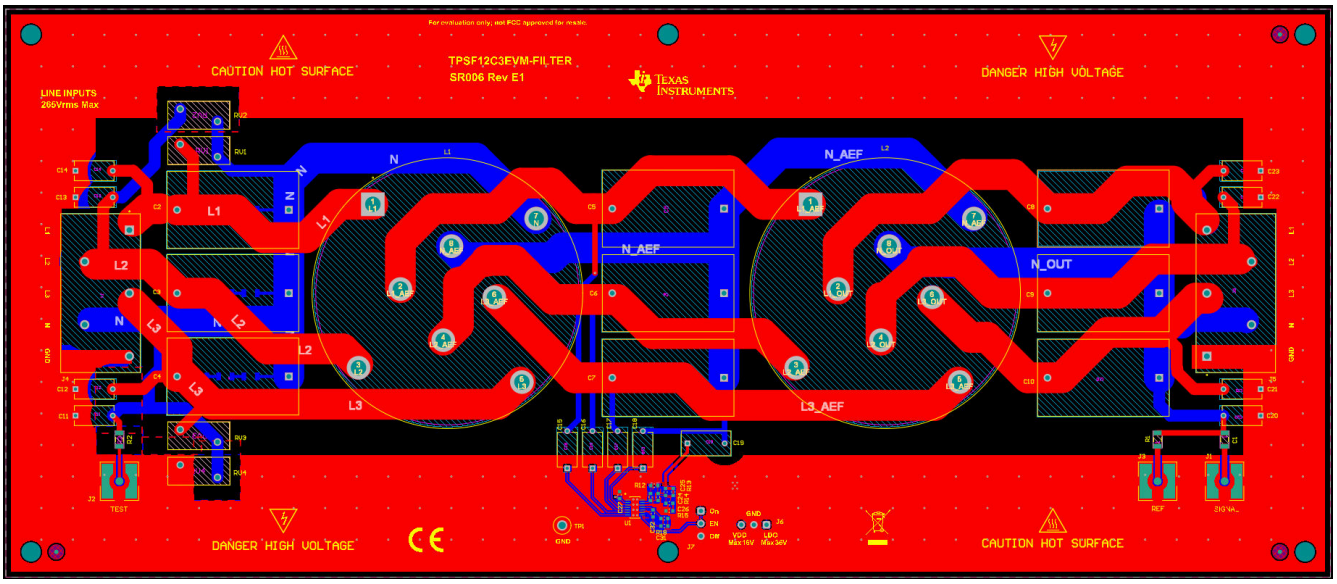


図 9-11. Typical Three-Phase Filter Board Design With AEF

10 Device and Documentation Support

10.1 Device Support

10.1.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

10.1.2 Development Support

All AEF devices from the family shown in 表 10-1 are rated for a maximum junction temperature of 150°C and are functional safety-capable. See the Texas Instruments power-supply filter ICs landing page for more detail.

表 10-1. Common-mode AEF IC Family

DEVICE	ORDERABLE PART NUMBER	PHASES	GRADE	JUNCTION TEMPERATURE RANGE
TPSF12C3-Q1	TPSF12C3QDYYRQ1	3	Automotive	–40°C to 150°C
TPSF12C1-Q1	TPSF12C1QDYYRQ1	1	Automotive	–40°C to 150°C
TPSF12C3	TPSF12C3DYYR	3	Commercial	–40°C to 150°C
TPSF12C1	TPSF12C1DYYR	1	Commercial	–40°C to 150°C

For development support see the following:

- TPSF12C3-Q1 quickstart calculator
- TPSF12C3-Q1 EVM *Altium layout source files*
- TPSF12C3-Q1 PSPICE for TI and SIMPLIS *simulation models*
- TPSF12C3-Q1 *EVM user's guide*
- For TI's reference design library, visit *TI Reference Design library*
- To design a low-EMI power supply, review TI's comprehensive *EMI Training Series*
- TI Reference Designs:
  - *3-kW, 180-W/in3 single-phase totem-pole bridgeless PFC reference design with 16-A max input*
  - *1-kW reference design with CCM totem pole PFC and current-mode LLC realized by C2000™ and GaN*
  - *7.4-kW on-board charger reference design with CCM totem pole PFC and CLLLC DC/DC using C2000™ MCU*
  - *GaN-based, 6.6-kW, bidirectional, onboard charger reference design*
  - *10-kW, bidirectional three-phase three-level (T-type) inverter and PFC reference design*
- Technical Articles:
  - Texas Instruments, *How a stand-alone active EMI filter IC shrinks common-mode filter size*
  - Texas Instruments, *How device-level features and package options can help minimize EMI in automotive designs*
  - Texas Instruments, *How to use slew rate for EMI control*
- White Papers:
  - Texas Instruments, *How Active EMI Filter ICs Mitigate Common-Mode Emissions and Save PCB Space in Single- and Three-Phase Systems*
  - Texas Instruments, *An Overview of Conducted EMI Specifications for Power Supplies*
  - Texas Instruments, *An Overview of Radiated EMI Specifications for Power Supplies*
- Video:
  - Texas Instruments, *Single- and three-phase active EMI filter ICs mitigate common-mode EMI, save space and reduce cost*
- To view a related device of this product, see the TPSF12C1-Q1 single-phase active EMI filter for common-mode noise mitigation or refer to the Texas Instruments power-supply filter ICs landing page

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *TI pioneers the industry's first stand-alone active EMI filter ICs, supporting high-density power supply designs* press release
- Texas Instruments, *An Engineer's Guide To EMI In DC/DC Regulators* e-book
- Texas Instruments, *Reduce Buck Converter EMI and Voltage Stress by Minimizing Inductive Parasitics* ADJ article
- Texas Instruments, *Designing High Performance, Low-EMI, Automotive Power Supplies* application report
- Texas Instruments, *EMI Filter Components And Their Nonidealities For Automotive DC/DC Regulators* technical brief

10.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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10.5 Trademarks

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10.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPSF12C3QDYYRQ1	ACTIVE	SOT-23-THIN	DYY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 150	TPSF12C3Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPSF12C3-Q1 :

- Catalog : TPSF12C3

NOTE: Qualified Version Definitions:

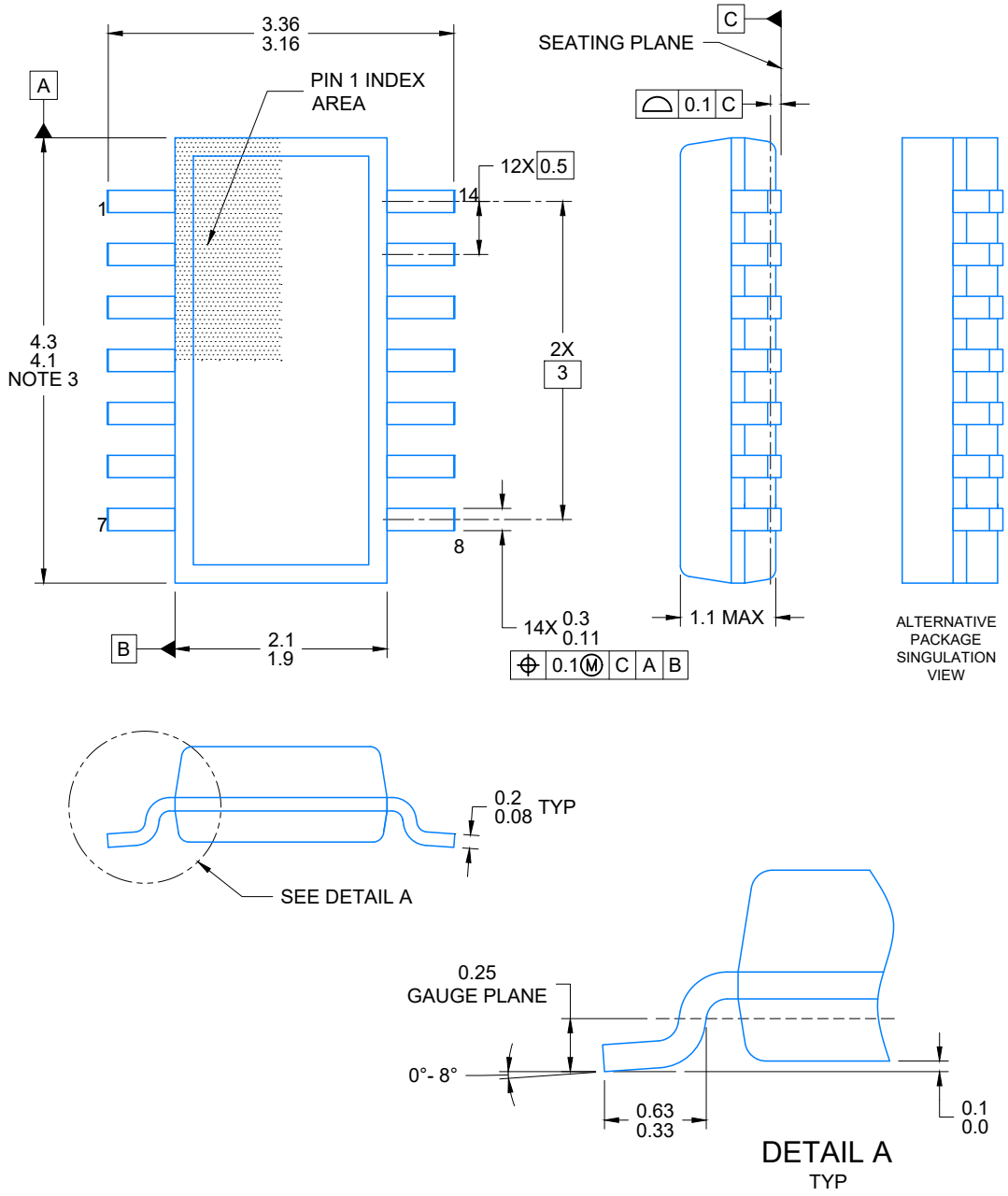
- Catalog - TI's standard catalog product

PACKAGE OUTLINE

DYY0014A

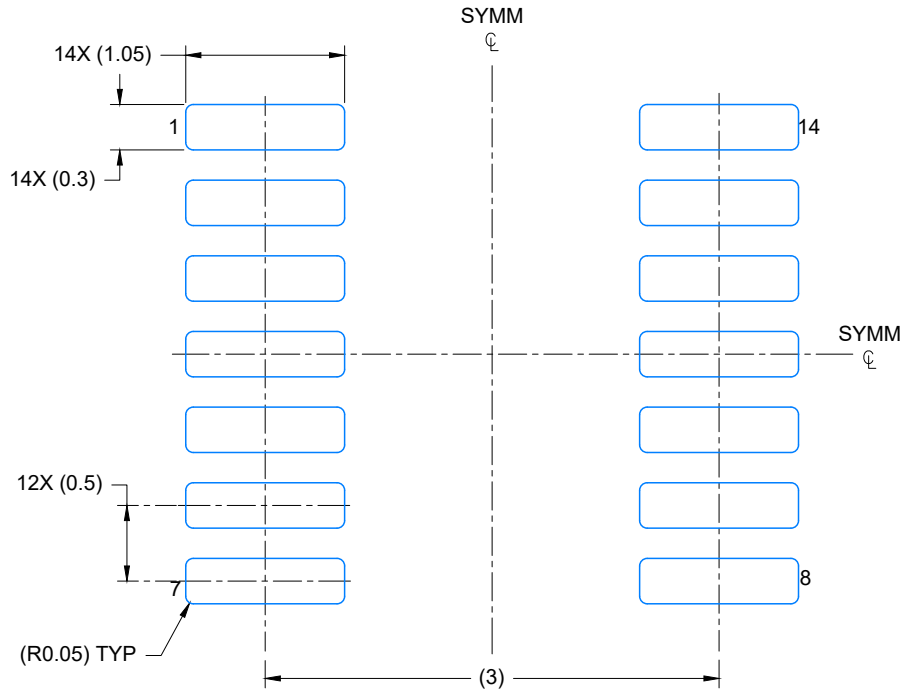
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

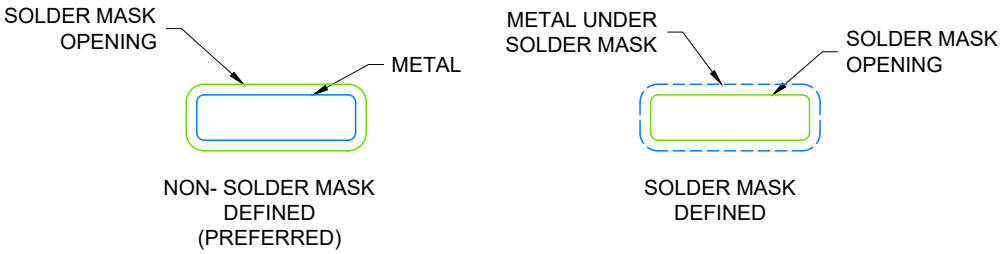


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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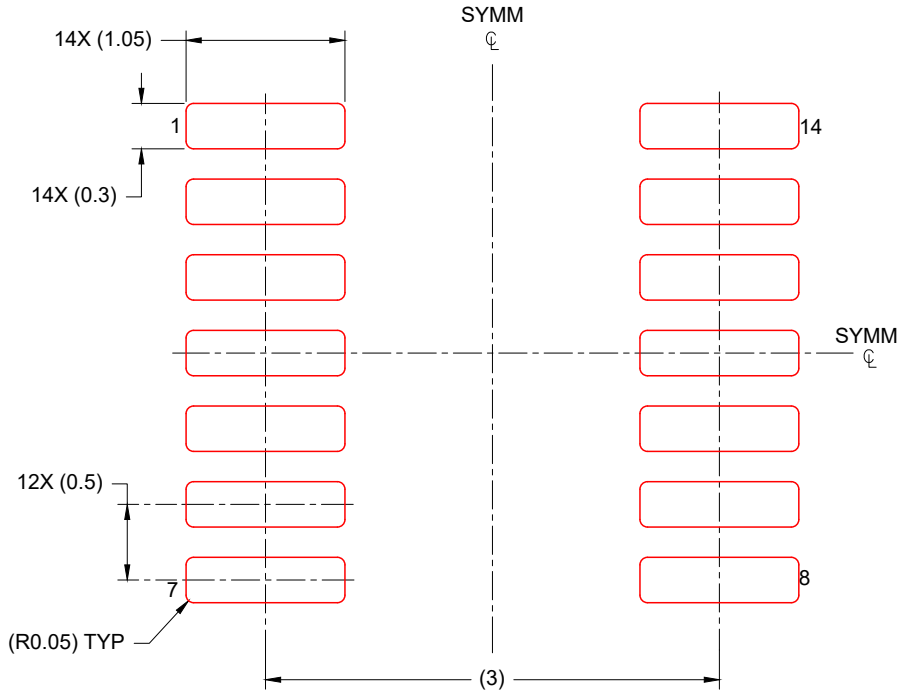
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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