TEXAS INSTRUMENTS
TPSI3100-Q1
JAJSL38 – DECEMBER 2023

TPSI3100-Q1 車載対応、15V ゲート電源とデュアル絶縁型コンパレータ搭載、強化絶縁型スイッチ ドライバ

1 特長

- 外部パワー トランジスタを駆動
- 絶縁型二次電源は不要
- 15.8V ゲート ドライブ、1.5/2.5A ピーク ソース / シンク電流
- 5kV$_{RMS}$ に耐える強化絶縁
- 外部補助回路に対して最大 25mW、5V の電力を供給
- ±1.5% の精度の電圧リファレンスを内蔵したデュアル絶縁型高速コンパレータ
- フォルトおよびアラーム インジケータ用のオープン ドレイン出力
- 車載アプリケーション用に AEC Q-100 認定済み:
  - 温度グレード 1:-40℃～+125℃、T_A
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 安全関連認証
  - 予定:DIN EN IEC 60747-17 (VDE 0884-17) に準拠した強化絶縁耐圧:7070V$_{PK}$
  - 予定:UL 1577 に準拠した絶縁耐圧:5kV$_{RMS}$ (1 分間)

2 アプリケーション

- ソリッド ステート リレー
- バッテリ管理システム
- オンボード チャージャ
- ハイブリッド / 電動パワートレイン システム
- ビル オートメーション
- ファクトリ オートメーション / 制御

3 概要

TPSI3100-Q1 は、統合型の絶縁スイッチ ドライバで、外部パワー スイッチと組み合わせることにより、完全な絶縁型ソリッド ステート リレー ソリューションを形成します。ゲート駆動電圧 15.8V、ピーク ソース / シンク電流 1.5/2.5A という性能を備えているため、さまざまなパワー スイッチを使用して多くのアプリケーションのニーズに対応できます。TPSI3100-Q1 は、1 次側で供給された電源によって独自の 2 次バイアス電源を生成するので、絶縁型の 2 次側電源バイアスは不要です。TPSI3100-Q1 は、電流および電圧監視やリモート温度検出などの各種機能を実行するために補助回路で使用する追加電力を公称 5V のレール (VDDM) 経由で供給します。TPSI3100-Q1 の絶縁は非常に堅牢で、従来の機械式リレーやフォトカプラに比べて高信頼性、低消費電力で、温度範囲が広くなっています。

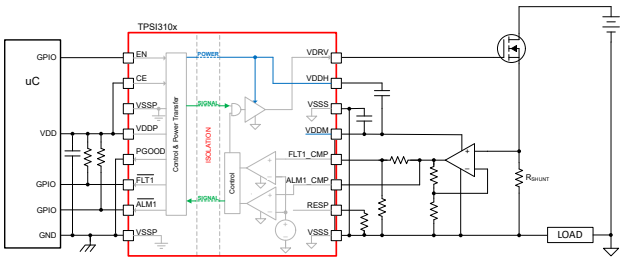
TPSI3100-Q1 には通信バックチャネルが内蔵されており、オープン ドレイン出力の PGOOD (パワー グッド)、$\overline{FLT1}$ (フォルト 1)、$\overline{ALM1}$ (アラーム 1) を通じて 2 次側から 1 次側にステータス情報を転送します。$\overline{FLT1}$ および $\overline{ALM1}$ のアサートには、共有の電圧リファレンスを内蔵したデュアル高速コンパレータが使用されます。コンパレータ入力 FLT1_CMP が電圧リファレンスを超えると、ドライバが即座に Low にアサートされると共に $\overline{FLT1}$ も Low に駆動され、フォルトが発生したことがシステムに示されます。これは、過電流検出などの重大なイベントが発生したときに、短い待ち時間で外部スイッチを無効にするのに便利です。コンパレータ入力 ALM1_CMP が電圧リファレンスを超えると、$\overline{ALM1}$ 信号が Low にアサートされますが、ドライバでは何も行われません。これは、過熱や過電圧のイベントに対するアラームまたは警告インジケータとして役立ちます。

TPSI310xL-Q1 シリーズは、ラッチ ベースのフォルト インジケータを備えています。フォルトが検出されると、ドライバとフォルト インジケータが Low にアサートされ、EN が Low にアサートされるまでラッチされた状態を維持します。TPSI310x-Q1 シリーズには、ラッチなしのフォルト インジケータがあります。フォルト イベントが解消されると、$\overline{FLT1}$ がデアサートされ、ドライバは指定された回復期間の後で EN ピンの状態に従います。それでもフォルト イベントが解消されない場合、フォルト インジケータとドライバの両方が Low にアサートされたままになります。

製品情報

部品番号	REF (2)	コンパレータ(2)	パッケージ (1)
TPSI3100-Q1	0.3V	フォルト 1 / アラーム 1	SSOP (16) DVX
TPSI3103-Q1 (3)	1.2V		
TPSI3100L-Q1	0.3V	ラッチ フォルト 1 / アラーム 1	
TPSI3103L-Q1 (3)	1.2V		

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) Device Comparison Table を参照してください。
(3) 製品プレビュー。



TPSI3100-Q1 の概略回路図

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4 Device Comparison Table

VARIANT	REF	COMPARATORS	LATCHED FAULT
TPSI3100-Q1	0.3 V	1 fault, 1 alarm	No
TPSI3103-Q1 (3)	1.2 V		
TPSI3100L-Q1	0.3 V		Yes
TPSI3103L-Q1 (3)	1.2 V		
TPSI3110-Q1 (3)	0.3 V	2 faults	No
TPSI3113-Q1 (3)	1.2 V		
TPSI3110L-Q1 (3)	0.3 V		Yes
TPSI3113L-Q1 (3)	1.2 V		
TPSI3120-Q1 (3)	0.3 V	2 alarms	N/A(2)
TPSI3123-Q1 (3)	1.2 V		
TPSI3130-Q1 (3)	0.3 V	1 fault(1), 1 alarm	No
TPSI3133-Q1 (3)	1.2 V		

(1) FLT1_CMP input is actively pulled down when EN is low. These devices are useful for over-current detection using DESAT techniques primarily with IGBT power transistors.
(2) Non-applicable.
(3) Product preview.

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5 Pin Configuration and Functions

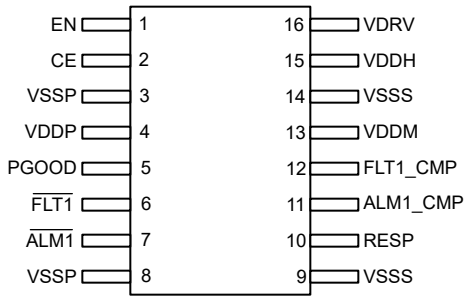

図 5-1. TPSI310x-Q1 and TPSI310xL-Q1 DVX Package, 16-Pin SSOP (Top View)

PIN		I/O	TYPE(1)	DESCRIPTION
NO.	NAME			
1	EN	I	-	Active high driver enable. Internal 500 kΩ pull-down to VSSP.
2	CE	I	-	Active high input. When asserted low, device is disabled. Tie to VDDP when not used. Internal 500 kΩ pull-down to VSSP.
3	VSSP	-	GND	Ground supply for primary side. All VSSP pins must be connected to the primary side ground.
4	VDDP	-	P	Power supply for the primary side.
5	PGOOD	O	-	Power good indicator. Open-drain output. When being used, requires external pull-up to VDDP. Float or tie to VSSP when not used.
6	$\overline{\text{FLT1}}$	O	-	Fault 1 indicator. Open-drain output. When being used, requires external pull-up to VDDP. Float or tie to VSSP when not used.
7	$\overline{\text{ALM1}}$	O	-	Alarm 1 indicator. Open-drain output. When being used, requires external pull-up to VDDP. Float or tie to VSSP when not used.
8	VSSP	-	GND	Ground supply for the primary side. All VSSP must be connected to the primary side ground.
9	VSSS	-	GND	Ground supply for the secondary side. All VSSS pins must be connected to the secondary side ground.
10	RESP	O	-	Used in conjunction with an external resistor connected to VSSS to adjust comparator response time. When not being used, tie to VSSS.
11	ALM1_CMP	I	-	Analog comparator input. When ALM1_CMP voltage exceeds internal reference voltage, $\overline{\text{ALM1}}$ is asserted low within $t_{ALM\_LATENCY}$. Internal 3 MΩ pull-down to VSSS. When not being used, tie to VSSS.
12	FLT1_CMP	I	-	Analog comparator input. When FLT1_CMP voltage exceeds internal reference voltage, VDRV is automatically asserted low regardless of EN state and $\overline{\text{FLT1}}$ asserted low within $t_{FLT\_LATENCY}$. Internal 3 MΩ pull-down to VSSS. When not being used, tie to VSSS.
13	VDDM	-	P	Generated mid-supply, nominal 5 V.
14	VSSS	-	GND	Ground supply for secondary side. All VSSS pins must be connected to the secondary side ground.
15	VDDH	-	P	Generated high supply, nominal 15.8 V.
16	VDRV	O	-	Active high driver output.

(1) P = power, GND = ground, NC = no connect

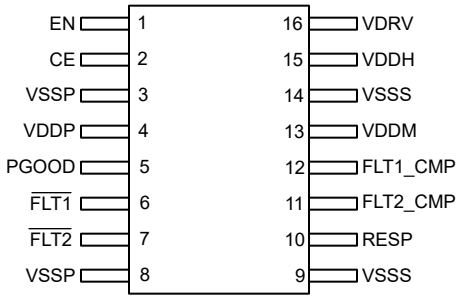

図 5-2. TPSI311x-Q1 and TPSI311xL-Q1 DVX Package, 16-Pin SSOP (Top View)

PIN		I/O	TYPE(1)	DESCRIPTION
NO.	NAME			
1	EN	I	-	Active high driver enable. Internal 500 kΩ pull-down to VSSP.
2	CE	I	-	Active high input. When asserted low, device is disabled. Tie to VDDP when not used. Internal 500 kΩ pull-down to VSSP.
3	VSSP	-	GND	Ground supply for primary side. All VSSP pins must be connected to the primary side ground.
4	VDDP	-	P	Power supply for the primary side.
5	PGOOD	O	-	Power good indicator. Open-drain output. When being used, requires external pull-up to VDDP. Float or tie to VSSP when not used.
6	$\overline{\text{FLT1}}$	O	-	Fault 1 indicator. Open-drain output. When being used, requires external pull-up to VDDP. Float or tie to VSSP when not used.
7	$\overline{\text{FLT2}}$	O	-	Fault 2 indicator. Open-drain output. When being used, requires external pull-up to VDDP. Float or tie to VSSP when not used.
8	VSSP	-	GND	Ground supply for the primary side. All VSSP pins must be connected to the primary side ground.
9	VSSS	-	GND	Ground supply for the secondary side. All VSSS pins must be connected to the secondary side ground.
10	RESP	O	-	Used in conjunction with an external resistor connected to VSSS to adjust comparator response time. When not being used, tie to VSSS.
11	FLT2_CMP	I	-	Analog comparator input. When FLT2_CMP voltage exceeds internal reference voltage, VDRV is automatically asserted low regardless of EN state and $\overline{\text{FLT2}}$ asserted low within $t_{FLT\_LATENCY}$. Internal 3 MΩ pull-down to VSSS. When not being used, tie to VSSS.
12	FLT1_CMP	I	-	Analog comparator input. When FLT1_CMP voltage exceeds internal reference voltage, VDRV is automatically asserted low regardless of EN state and $\overline{\text{FLT1}}$ asserted low within $t_{FLT\_LATENCY}$. Internal 3 MΩ pull-down to VSSS. When not being used, tie to VSSS.
13	VDDM	-	P	Generated mid-supply, nominal 5 V.
14	VSSS	-	GND	Ground supply for secondary side. All VSSS pins must be connected to the secondary side ground.
15	VDDH	-	P	Generated high supply, nominal 15.8 V.
16	VDRV	O	-	Active high driver output.

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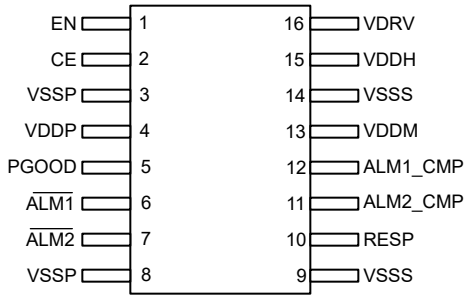

図 5-3. TPSI312x-Q1 DVX Package, 16-Pin SSOP (Top View)

PIN		I/O	TYPE(1)	DESCRIPTION
NO.	NAME			
1	EN	I	-	Active high driver enable. Internal 500 kΩ pull-down to VSSP.
2	CE	I	-	Active high input. When asserted low, device is disabled. Tie to VDDP when not used. Internal 500 kΩ pull-down to VSSP.
3	VSSP	-	GND	Ground supply for primary side. All VSSP pins must be connected to the primary side ground.
4	VDDP	-	P	Power supply for the primary side.
5	PGOOD	O	-	Power good indicator. Open-drain output. When being used, requires external pull-up to VDDP. Float or tie to VSSP when not used.
6	$\overline{\text{ALM1}}$	O	-	Alarm 1 indicator. Open-drain output. When being used, requires external pull-up to VDDP. Float or tie to VSSP when not used.
7	$\overline{\text{ALM2}}$	O	-	Alarm 2 indicator. Open-drain output. When being used, requires external pull-up to VDDP. Float or tie to VSSP when not used.
8	VSSP	-	GND	Ground supply for the primary side. All VSSP pins must be connected to the primary side ground.
9	VSSS	-	GND	Ground supply for the secondary side. All VSSS pins must be connected to the secondary side ground.
10	RESP	O	-	Used in conjunction with an external resistor connected to VSSS to adjust comparator response time. When not being used, tie to VSSS.
11	ALM2_CMP	I	-	Analog comparator input. When ALM2_CMP voltage exceeds internal reference voltage, $\overline{\text{ALM2}}$ is asserted low within $t_{ALM\_LATENCY}$. Internal 3 MΩ pull-down to VSSS. When not being used, tie to VSSS.
12	ALM1_CMP	I	-	Analog comparator input. When ALM1_CMP voltage exceeds internal reference voltage, $\overline{\text{ALM1}}$ is asserted low within $t_{ALM\_LATENCY}$. Internal 3 MΩ pull-down to VSSS. When not being used, tie to VSSS.
13	VDDM	-	P	Generated mid-supply, nominal 5 V.
14	VSSS	-	GND	Ground supply for secondary side. All VSSS pins must be connected to the secondary side ground.
15	VDDH	-	P	Generated high supply, nominal 15.8 V.
16	VDRV	O	-	Active high driver output.

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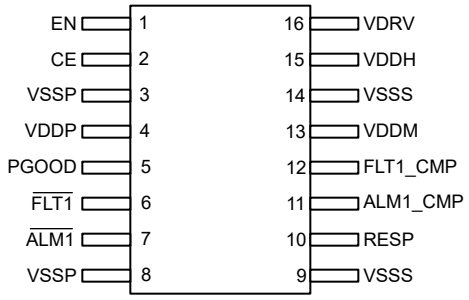

図 5-4. TPSI313x-Q1 DVX Package, 16-Pin SSOP (Top View)

PIN		I/O	TYPE(1)	DESCRIPTION
NO.	NAME			
1	EN	I	-	Active high driver enable. Internal 500 kΩ pull-down to VSSP.
2	CE	I	-	Active high input. When asserted low, device is disabled. Tie to VDDP when not used. Internal 500 kΩ pull-down to VSSP.
3	VSSP	-	GND	Ground supply for primary side. All VSSP pins must be connected to the primary side ground.
4	VDDP	-	P	Power supply for the primary side.
5	PGOOD	O	-	Power good indicator. Open-drain output. When being used, requires external pull-up to VDDP. Float or tie to VSSP when not used.
6	$\overline{\text{FLT1}}$	O	-	Fault 1 indicator. Open-drain output. When being used, requires external pull-up to VDDP. Float or tie to VSSP when not used.
7	$\overline{\text{ALM1}}$	O	-	Alarm 1 indicator. Open-drain output. When being used, requires external pull-up to VDDP. Float or tie to VSSP when not used.
8	VSSP	-	GND	Ground supply for the primary side. All VSSP pins must be connected to the primary side ground.
9	VSSS	-	GND	Ground supply for the secondary side. All VSSS pins must be connected to the secondary side ground.
10	RESP	O	-	Used in conjunction with an external resistor connected to VSSS to adjust comparator response time. When not being used, tie to VSSS.
11	ALM1_CMP	I	-	Analog comparator input. When ALM1_CMP voltage exceeds internal reference voltage, $\overline{\text{ALM1}}$ is asserted low within $t_{ALM\_LATENCY}$. Internal 3 MΩ pull-down to VSSS. When not being used, tie to VSSS.
12	FLT1_CMP	I/O	-	Analog comparator input/output. When EN state is low, FLT1_CMP is actively pulled low. If EN state is high and FLT1_CMP voltage exceeds internal reference voltage, VDRV is automatically asserted low and $\overline{\text{FLT1}}$ asserted low within $t_{FLT\_LATENCY}$. Internal 3 MΩ pull-down to VSSS. When not being used, tie to VSSS.
13	VDDM	-	P	Generated mid-supply, nominal 5 V.
14	VSSS	-	GND	Ground supply for secondary side. All VSSS pins must be connected to the secondary side ground.
15	VDDH	-	P	Generated high supply, nominal 15.8 V.
16	VDRV	O	-	Active high driver output.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER(1)		MIN	MAX	UNIT
Primary side supply(2)	VDDP, EN, CE, PGOOD, $\overline{FLT1}$ (TPSI310x, TPSI311x, TPSI313x), $\overline{FLT2}$ (TPSI311x), $\overline{ALM1}$ (TPSI310x, TPSI312x, TPSI313x), $\overline{ALM2}$ (TPSI312x)	–0.3	6	V
Secondary side supply(3)	FLT1_CMP (TPSI310x, TPSI311x, TPSI313x), FLT2_CMP (TPSI311x), ALM1_CMP (TPSI310x, TPSI312x, TPSI313x), ALM2_CMP (TPSI312x)	–3	6	V
	VDRV	–0.3	18	V
	VDDH	–0.3	18	V
	VDDM	–0.3	6	V
	VDDH-VDDM	–0.3	12	V
	RESP	–0.3	6	V
Junction temperature, T_J	Junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute MaximumRatings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to VSSP. Not all signals listed may be present pending device variant.
(3) All voltage values are with respect to VSSS. Not all signals listed may be present pending device variant.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD classification level 2		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C4B	Corner pins (1, 8, 9, and 16)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDDP	Primary side supply voltage(1)	4.5		5.5	V
EN	Enable VDRV(1)	0		5.5	V
CE	Chip enable(1)	0		5.5	V
PGOOD	Power good indicator(4) (1)	0		5.5	V
$\overline{FLTn}$	Fault indicator(s).(4) (1) $\overline{FLT1}$ (TPSI310x, TPSI311x, TPSI313x) $\overline{FLT2}$ (TPSI311x)	0		5.5	V
$\overline{ALMn}$	Alarm indicator(s).(4) (1) $\overline{ALM1}$ (TPSI310x, TPSI311x, TPSI313x) $\overline{ALM2}$ (TPSI312x)	0		5.5	V

6.3 Recommended Operating Conditions (続き)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
C_{VDDP}	Decoupling capacitance on VDDP and VSSP(3)	1		20	µF
C_{DIV1} (2)	Decoupling capacitance across VDDH and VDDM(3)	0.003		15	µF
C_{DIV2} (2)	Decoupling capacitance across VDDM and VSSS(3)	0.1		40	µF
R_{RESP}	Comparator response resistor from RESP to VSSS.	0		1000	kΩ
I_{AUX}	Auxiliary current sourced from VDDM.	0		5	mA
T_A	Ambient operating temperature	–40		125	°C
T_J	Operating junction temperature	–40		150	°C

(1) All voltage values are with respect to VSSP.
(2) C_{DIV1} and C_{DIV2} should be of same type and tolerance. C_{DIV2} capacitance value should be at least three times the capacitance value of C_{DIV1} i.e. $C_{DIV2} \geq 3 \times C_{DIV1}$.
(3) All capacitance values are absolute. Derating should be applied where necessary.
(4) Open-drain fail-safe output. When being used, an external pull-up resistor greater than 20 kΩ to VDDP is recommended. When not being used, float pin or connect to VSSP.

6.4 Thermal Information

THERMAL METRIC(1)		DEVICE	UNIT
		DVX (SSOP)	
		16 PINS	
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	82.5	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	39.3	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	42.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	41.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation, VDDP.	T_A = 25°C, V_{VDDP} = 5.0 V, f_{EN} = 1 kHz square wave, C_{VDRV} = 1 nF			250	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
CREEPAGE AND TRACKING				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	≥ 8	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	≥ 8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 120	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	

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6.6 Insulation Specifications (続き)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
DIN EN IEC 60747-17 (VDE 0884-17)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1697	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave)	1200	V_{RMS}
		DC voltage	1697	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$; t = 60 s (qualification test)	7070	V_{PK}
		$V_{TEST} = 1.2 \times V_{IOTM}$; t = 1 s (100% production test)	8484	V_{PK}
V_{IMP}	Maximum impulse voltage(2)	Tested in air; 1.2/50-µs waveform per IEC 62638-1	9230	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	Tested in oil (qualification test); 1.2/50-µs waveform per IEC 62638-1	12000	V_{PK}
q_{pd}	Apparent charge(4)	Method a: After input-output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM} = 2036\ V_{PK}$, t_m = 10 s.	≤ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM} = 2715\ V_{PK}$, t_m = 10 s.	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM} = 3139\ V_{PK}$, t_m = 1 s.	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1 MHz	3	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S =150°C	> 10^{9}	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5000\ V_{RMS}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 6000\ V_{RMS}$, t = 1 s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed-circuit board are used to help increase these specifications.
(2) Testing is carried out in air to determine the intrinsic surge immunity of the package.
(3) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.

6.7 Safety-Related Certifications

VDE	UL
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify under UL 1577 Component Recognition Program
Reinforced insulation; Maximum transient isolation voltage, 7070 V_{PK}; Maximum repetitive peak isolation voltage, 1697 V_{PK}; Maximum surge isolation voltage, 12000 V_{PK}	Single protection, 5000 V_{RMS}
Certificate planned	Certificate planned

6.8 Safety Limiting Values

PARAMETER(1) (2)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 82.5°C/W, V_{VDDP} = 5.5 V, T_J = 150°C, T_A = 25°C			275	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ =82.5°C/W, T_J = 150°C, T_A = 25°C			1.52	W
T_S	Maximum safety temperature				150	°C

(1) Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

(2) The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the セクション 6.4 table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

6.9 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25 °C. C_{VDDP} = 1 µF, C_{DIV1} = 47 nF, C_{DIV2} = 220 nF, C_{VDRV} = 1 nF, I_{AUX} = 0 mA. 50 kΩ pull-ups from $\overline{FLT1}$, $\overline{ALM1}$, PGOOD to VDDP. R_{RESP} = 100 kΩ to VSSS.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON						
CMTI	Common-mode transient immunity, static.	$\|V_{CM}\|$ = 1000 V, V_{EN} = 0 V or V_{EN} = 5 V.	100			V/ns
TSD	Temperature shutdown	V_{VDDP} = 5 V		173		℃
TSDH	Temperature shutdown hysteresis	V_{VDDP} = 5 V		32		℃
SUPPLY						
I_{VDDP_STBY}	VDDP current in standby	V_{VDDP} = 5 V, EN = 0 V, CE = 0 V. Measure average current.		30	40	µA
I_{VDDP_LOW}	VDDP average current in steady state	V_{VDDP} = 5 V, EN = CE = 5 V. Fault and alarm inputs tied to VSSP (device specific). I_{AUX} = 0 mA. Lowest power regulation. V_{VDDH} in steady state, measure I_{VDDP}.		5.3		mA
I_{VDDP_HIGH}	VDDP average current in steady state	V_{VDDP} = 5 V, EN = CE = 5 V. Fault and alarm inputs tied to VSSS (device specific). Highest power regulation. V_{VDDH} in steady state, measure I_{VDDP}.		35		mA
V_{VDDH}	VDDH output voltage	V_{VDDP} = 5 V, EN = CE = 5 V. Fault and alarm inputs tied to VSSS (device specific).	14.7	15.8	17.1	V
V_{VDDM}	Average VDDM voltage when not sourcing current.	V_{VDDP} = 5 V, EN = CE = 5 V. Fault and alarm inputs tied to VSSS (device specific).	4.8	5.0	5.2	V
I_{VDDH_STBY}	Average standby current of VDDH supply.	V_{VDDP} = 5 V, EN = 0 V, CE = 5 V. Fault and alarm inputs tied to VSSS (device specific).		48		µA
I_{VDDM_STBY}	Average standby current of VDDM supply.	V_{VDDP} = 5 V, EN = 0 V, CE = 5 V. Fault and alarm inputs tied to VSSS (device specific).		115		µA

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6.9 Electrical Characteristics (続き)

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25 °C. C_{VDDP} = 1 µF, C_{DIV1} = 47 nF, C_{DIV2} = 220 nF, C_{VDRV} = 1 nF, I_{AUX} = 0 mA. 50 kΩ pull-ups from $\overline{FLT1}$, $\overline{ALM1}$, PGOOD to VDDP. R_{RESP} = 100 kΩ to VSSS.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VDDM_IAUX}	Average VDDM voltage when sourcing external current.	V_{VDDP} = 5 V, EN = 0 V, steady state. Fault and alarm inputs tied to VSSS (device specific). Source I_{AUX} = 5 mA from VDDM, measure V_{VDDM}. C_{DIV2} = 1 µF	4.7		5.5	V
SUPERVISORY						
$V_{VDDP\_UV\_R}$	VDDP under-voltage threshold rising	VDDP rising.	3.9	4.1	4.35	V
$V_{VDDP\_UV\_F}$	VDDP under-voltage threshold falling	VDDP falling	3.8	3.9	4.25	V
$V_{VDDP\_UV\_HYS}$	VDDP under-voltage threshold hysteresis			170		mV
$V_{VDDH\_UV\_R}$	VDDH under-voltage threshold rising	VDDH rising.	12.4	13	13.5	V
$V_{VDDH\_UV\_F}$	VDDH under-voltage threshold falling.	VDDH falling.	9.9	10.4	10.9	V
$V_{VDDH\_UV\_HYS}$	VDDH under-voltage threshold hysteresis.			2.5		V
$V_{VDDM\_UV\_R}$	VDDM under-voltage threshold rising	VDDM rising.	3.4	3.7	3.9	V
$V_{VDDM\_UV\_F}$	VDDM under-voltage threshold falling.	VDDM falling.	3.1	3.4	3.7	V
$V_{VDDM\_UV\_HYS}$	VDDM under-voltage threshold hysteresis.			0.3		V
DRIVER						
V_{VDRV_H}	VDRV output voltage driven high	V_{VDDP} = 5 V, EN = 5 V. V_{VDDH} in steady state, no DC loading. Fault and alarm inputs tied to VSSS (device specific).	14.7	15.8	17.1	V
V_{VDRV_L}	VDRV output voltage driven low	V_{VDDP} = 5 V, EN = 0 V, V_{VDDH} in steady state, VDRV sinking 10 mA. Fault and alarm inputs tied to VSSS (device specific).			0.1	V
I_{VDRV_PEAK}	VDRV peak output current during rise	V_{VDDP} = 5 V, EN = 0 V → 5 V, V_{VDDH} in steady state, measure peak current. Fault and alarm inputs tied to VSSS (device specific).		1.5		A
	VDRV peak output current during fall	V_{VDDP} = 5 V, EN = 5 V → 0 V, V_{VDDH} in steady state, measure peak current. Fault and alarm inputs tied to VSSS (device specific).		2.5		A

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6.9 Electrical Characteristics (続き)

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25 °C. C_{VDDP} = 1 µF, C_{DIV1} = 47 nF, C_{DIV2} = 220 nF, C_{VDRV} = 1 nF, I_{AUX} = 0 mA. 50 kΩ pull-ups from $\overline{FLT1}$, $\overline{ALM1}$, PGOOD to VDDP. R_{RESP} = 100 kΩ to VSSS.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{DSON_VDRV}	Driver on resistance in low state.	Force V_{VDDH} = 15 V, sink I_{VDRV} = 50 mA. Fault and alarm inputs tied to VSSS (device specific).		1.8		Ω
	Driver on resistance in high state.	Force V_{VDDH} = 15 V, source I_{VDRV} = 50 mA. Fault and alarm inputs tied to VSSS (device specific).		3.6		Ω
DIGITAL INPUT/OUTPUT						
$V_{IT\_+(EN)}$	Input threshold voltage rising on EN.	V_{VDDP} = 5 V	2.2	2.4	2.6	V
$V_{IT\_-(EN)}$	Input threshold voltage falling on EN.	V_{VDDP} = 5 V	1.7	1.9	2.0	V
$V_{IT\_HYS(EN)}$	Input threshold voltage hysteresis on EN.	V_{VDDP} = 5 V		0.5		V
$V_{IT\_+(CE)}$	Input threshold voltage rising on CE.	V_{VDDP} = 5 V	2.2	2.4	2.6	V
$V_{IT\_-(CE)}$	Input threshold voltage falling on CE.	V_{VDDP} = 5 V	1.7	1.9	2.0	V
$V_{IT\_HYS(CE)}$	Input threshold voltage hysteresis on CE.	V_{VDDP} = 5 V		0.5		V
V_{OL}	Low level output voltage. PGOOD $\overline{FLT1}$ (TPSI310x, TPSI312x, TPSI313x) $\overline{FLT2}$ (TPSI312x) $\overline{ALM1}$ (TPSI310x, TPSI311x, TPSI313x) $\overline{ALM2}$ (TPSI311x)	V_{VDDP} = 4.5 V to 5.5 V, I_{OL} = 2 mA. Outputs enabled.			0.4	V
I_{OL}	Low level output current. PGOOD $\overline{FLT1}$ (TPSI310x, TPSI312x, TPSI313x) $\overline{FLT2}$ (TPSI312x) $\overline{ALM1}$ (TPSI310x, TPSI311x, TPSI313x) $\overline{ALM2}$ (TPSI311x)	V_{VDDP} = 4.5 V to 5.5 V, V_{OL} = 0.4 V. Outputs enabled.	-2			mA
$V_{OL\_FLT\_CMP}$	Open-drain output, low level output voltage. FLT_CMP1 (TPSI313x)	V_{VDDP} = 4.5 V to 5.5 V, I_{OL} = 2 mA, CE = 1, EN = 0.			0.1	V
$I_{OL\_FLT\_CMP}$	Open-drain output, low level output current. FLT_CMP1 (TPSI313x)	V_{VDDP} = 4.5 V to 5.5 V, V_{OL} = 0.4 V, CE = 1, EN = 0.	-2			mA
I_{LKG}	Leakage current. PGOOD $\overline{FLT1}$ (TPSI310x, TPSI312x, TPSI313x) $\overline{FLT2}$ (TPSI312x) $\overline{ALM1}$ (TPSI310x, TPSI311x, TPSI313x) $\overline{ALM2}$ (TPSI311x)	V_{VDDP} = 4.5 V to 5.5 V, Outputs disabled.			2	µA
$R_{EN\_PULLDOWN}$	Internal resistor pull-down on EN.	V_{VDDP} = 5 V	400	500	600	kΩ
$R_{CE\_PULLDOWN}$	Internal resistor pull-down on CE.	V_{VDDP} = 5 V	400	500	600	kΩ

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6.9 Electrical Characteristics (続き)

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25 °C. C_{VDDP} = 1 µF, C_{DIV1} = 47 nF, C_{DIV2} = 220 nF, C_{VDRV} = 1 nF, I_{AUX} = 0 mA. 50 kΩ pull-ups from $\overline{FLT1}$, $\overline{ALM1}$, PGOOD to VDDP. R_{RESP} = 100 kΩ to VSSS.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE						
V_{REF}	Internal reference voltage. TPSI3100, TPSI3110, TPSI3120, TPSI3130 devices.	T_A = 25°C		0.31		V
	Internal reference voltage. TPSI3103, TPSI3113, TPSI3123, TPSI3133 devices.	T_A = 25°C		1.2		V
V_{REF_TOL}	Internal reference voltage tolerance.		-1.5		1.5	%
COMPARATORS						
$R_{CMP\_PULLDOWN}$	Internal resistor pull-down. FLT1_CMP, ALM1_CMP (TPSI310x, TPS313x) FLT1_CMP, FLT2_CMP (TPSI311x) ALM1_CMP. ALM1_CMP (TPSI312x)		1.9	3	3.6	MΩ

6.10 Switching Characteristics

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25 °C. C_{VDDP} = 1 µF, C_{DIV1} = 47 nF, C_{DIV2} = 220 nF, C_{VDRV} = 1 nF. 50 kΩ pull-ups from $\overline{FLT1}$, $\overline{ALM1}$, PGOOD to VDDP. R_{RESP} = 100 kΩ to VSSS.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER and DRIVER						
t_{LO_EN}	Low time of EN.	V_{VDDH} = steady state.	5			µs
t_{HI_EN}	High time of EN.	V_{VDDH} = steady state.	5			µs
t_{PER_EN}	Period of EN.	V_{VDDH} = steady state.	10			µs
t_{LH_VDDH}	Propagation delay time from VDDP rising to VDDH at 50% level.	EN = 0 V, V_{VDDP} = 0 V → 5 V at 1 V/µs, V_{VDDH} = 7.5 V.		145		µs
t_{LH_VDRV}	Propagation delay time from EN rising to VDRV at 90% level	V_{VDDP} = 5 V, V_{VDDH} steady state, EN = 0 V → 5 V, V_{VDRV} = 13.5 V.		3	4.5	µs
t_{HL_VDRV}	Propagation delay time from EN falling to VDRV at 10% level	V_{VDDP} = 5 V, V_{VDDH} steady state, EN = 5 V → 0 V, V_{VDRV} = 1.5 V.		2.5	3.0	µs
$t_{HL\_VDRV\_PD}$	Propagation delay time from VDDP falling to VDRV at 10% level. Timeout mechanism due to loss of power on primary supply.	EN = 5 V, V_{VDDP} = 5 V → 0 V at -1 V/µs, V_{VDRV} = 1.5 V.		140	160	µs
$t_{HL\_VDRV\_CE}$	Propagation delay time from CE falling to VDRV at 10% level	V_{VDDP} = 5 V, V_{VDDH} steady state, EN = 5 V, CE= 5 V → 0 V, V_{VDRV} = 1.5 V.		3	4	µs
t_{R_VDRV}	VDRV rise time from EN rising to VDRV from 15% to 85% level	V_{VDDP} = 5 V, V_{VDDH} steady state, EN = 0 V → 5 V, V_{VDRV} = 2.25 V to 12.75 V.		10		ns

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6.10 Switching Characteristics (続き)

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25 °C. C_{VDDP} = 1 µF, C_{DIV1} = 47 nF, C_{DIV2} = 220 nF, C_{VDRV} = 1 nF. 50 kΩ pull-ups from $\overline{FLT1}$, $\overline{ALM1}$, PGOOD to VDDP. R_{RESP} = 100 kΩ to VSSS.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{F_VDRV}	VDRV fall time from EN falling to VDRV from 85% to 15% level	V_{VDDP} = x V, V_{VDDH} steady state, EN = x V → 0 V, V_{VDRV} = 12.75 V to 2.25 V.		10		ns
t_{REC_VDRV} (1)	Time VDRV remains low upon detection of a fault condition.	V_{VDDP} = 5 V, V_{VDDH} and V_{VDRV} in steady state, EN = 5 V, FLTn_CMP positive-pulse of 3V, 50 µs pulse-width. Measure from FLTn_CMP going low (1.5 V) to V_{VDRV} = 7.5 V.		215	270	µs
COMPARATORS						
$t_{PD\_CMP\_VDRV\_DIS}$	Propagation delay time, fault comparator output rising to VDRV asserted low.	EN = CE = VDDP R_{RESP} ≤ 10 kΩ V_{UD} = 100 mV V_{OD} = 30 mV Measure V_{FLT_CMP} crossing VREF to 50% V_{VDRV}.	340	400	460	ns
		EN = CE = VDDP R_{RESP} = 100 kΩ. V_{UD} = 100 mV V_{OD} = 30 mV Measure V_{FLT_CMP} crossing VREF to 50% V_{VDRV}.	660	735	830	ns
		EN = CE = VDDP R_{RESP} = 300 kΩ. V_{UD} = 100 mV V_{OD} = 30 mV Measure V_{FLT_CMP} crossing VREF to 50% V_{VDRV}.	1090	1395	1785	ns
		EN = CE = VDDP R_{RESP} = 500 kΩ. V_{UD} = 100 mV V_{OD} = 30 mV Measure V_{FLT_CMP} crossing VREF to 50% V_{VDRV}.	1270	2130	2880	ns
$t_{DEGLITCH\_CMP\_F}$	Fault comparator falling output de-glitch.		4.2	5.7	8	µs
$t_{FLT\_LATENCY}$	Delay from rising or falling event detected by fault comparator and indicated on $\overline{FLT1}$ output.	EN = CE = VDDP R_{RESP} = 500 kΩ. V_{UD} = 100 mV V_{OD} = 30 mV Measure V_{FLT1_CMP} rising or falling and crossing VREF to 50% $\overline{FLT1}$.			30	µs
$t_{ALM\_LATENCY}$	Delay from rising or falling event detected by alarm comparator and indicated on $\overline{ALM1}$ output.	EN = CE = VDDP R_{RESP} = 500 kΩ. V_{UD} = 100 mV V_{OD} = 30 mV Measure V_{ALM1_CMP} rising or falling and crossing VREF to 50% $\overline{ALM1}$.			30	µs

(1) On latched based devices, recovery timer is still in effect even though VDRV is latched low. If the fault condition is removed and EN is asserted low and then high to clear the fault, VDRV will remain asserted low until the recovery timer has elapsed.

ADVANCE INFORMATION

6.11 Insulation Characteristic Curves

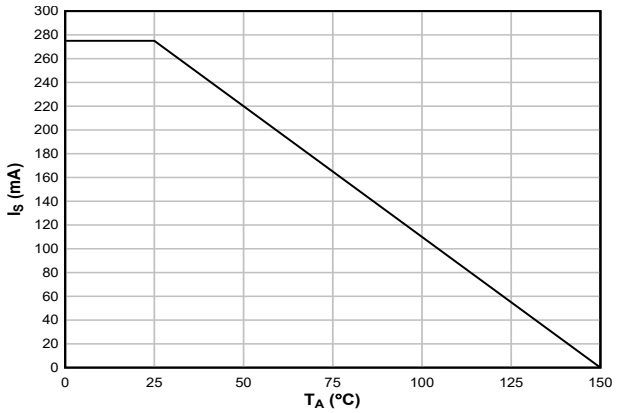


図 6-1. Thermal Derating Curve for Limiting Current per VDE and IEC

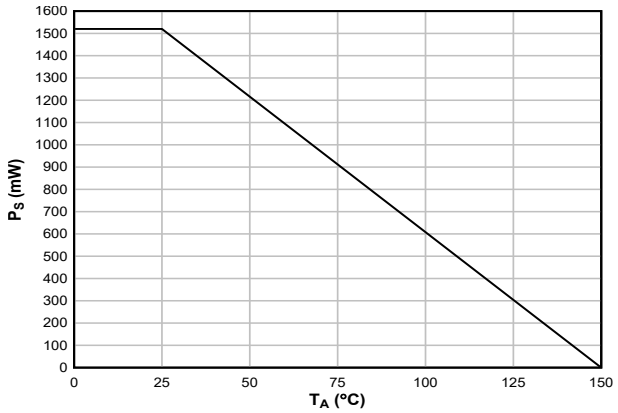
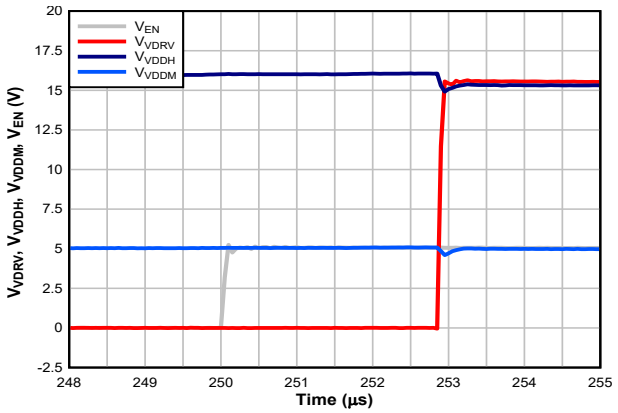


図 6-2. Thermal Derating Curve for Limiting Power per VDE and IEC

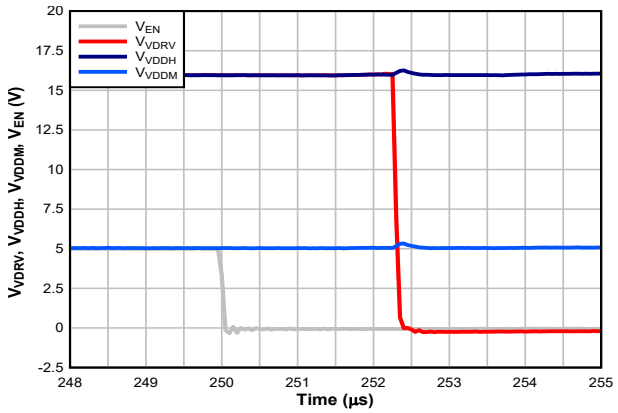
ADVANCE INFORMATION

6.12 Typical Characteristics



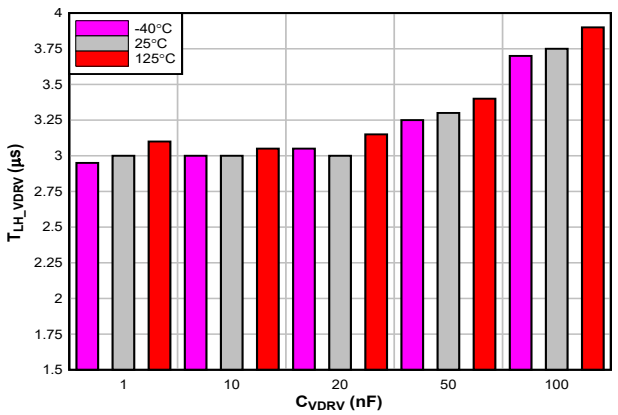
VDDP = 5.0 V T_A = 25°C
C_{DIV1} = 47 nF C_{DIV2} = 220 nF C_{VDRV} = 1 nF

図 6-3. t_{LH_VDRV}



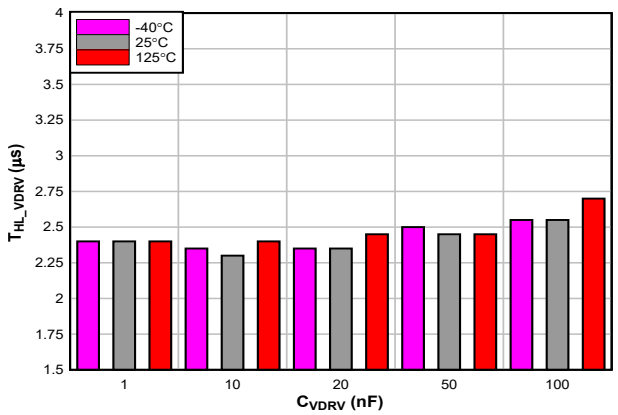
VDDP = 5.0 V T_A = 25°C
C_{DIV1} = 47 nF C_{DIV2} = 220 nF C_{VDRV} = 1 nF

図 6-4. t_{HL_VDRV}



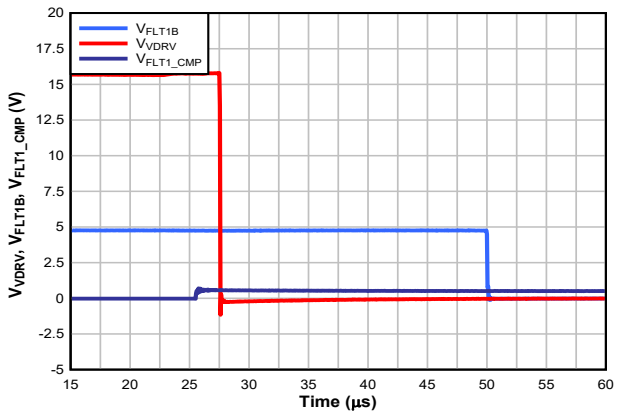
VDDP = 5.0 V
C_{DIV1} = 3.3 µF C_{DIV2} = 10 µF

図 6-5. t_{LH_VDRV} versus C_{VDRV}



VDDP = 5.0 V
C_{DIV1} = 3.3 µF C_{DIV2} = 10 µF

図 6-6. t_{HL_VDRV} versus C_{VDRV}



VDDP = 5.0 V T_A = 25°C R_{RESP} = 500 kΩ
C_{DIV1} = 47 nF C_{DIV2} = 220 nF C_{VDRV} = 1 nF

図 6-7. $t_{PD\_CMP\_VDRV\_DIS}$, $t_{FLT\_LATENCY}$

ADVANCE INFORMATION

7 Parameter Measurement Information

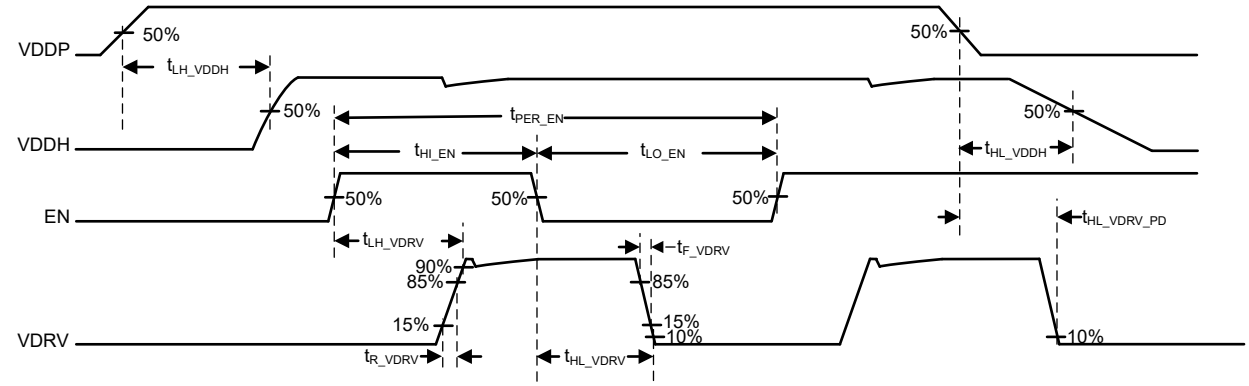


図 7-1. VDRV Timing, (CE = 1 or CE = VDDP, FLTn_CMP = ALMn_CMP = 0)

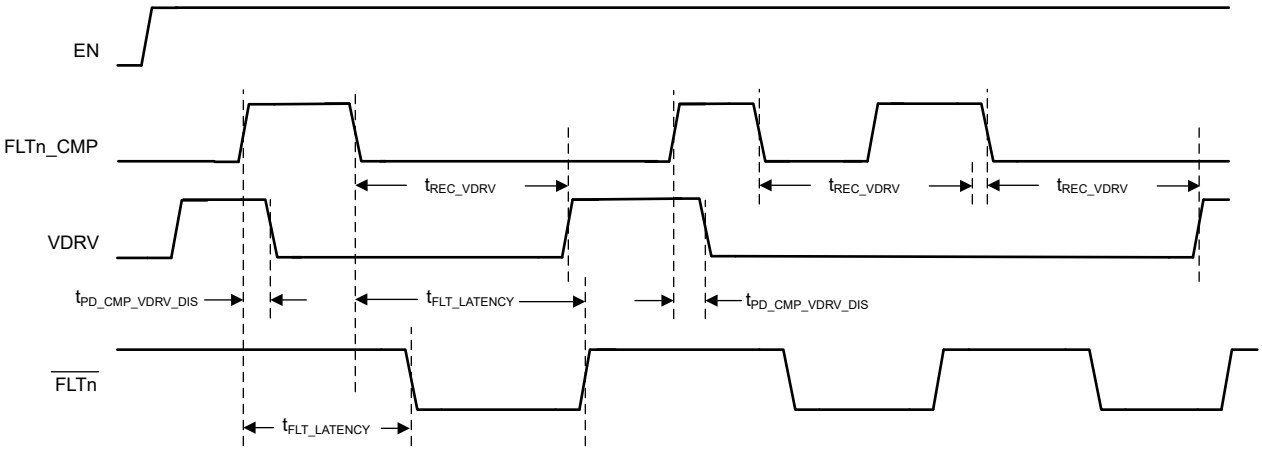


図 7-2. VDRV Auto-Recovery Timing (CE = 1 or CE = VDDP)

ADVANCE INFORMATION

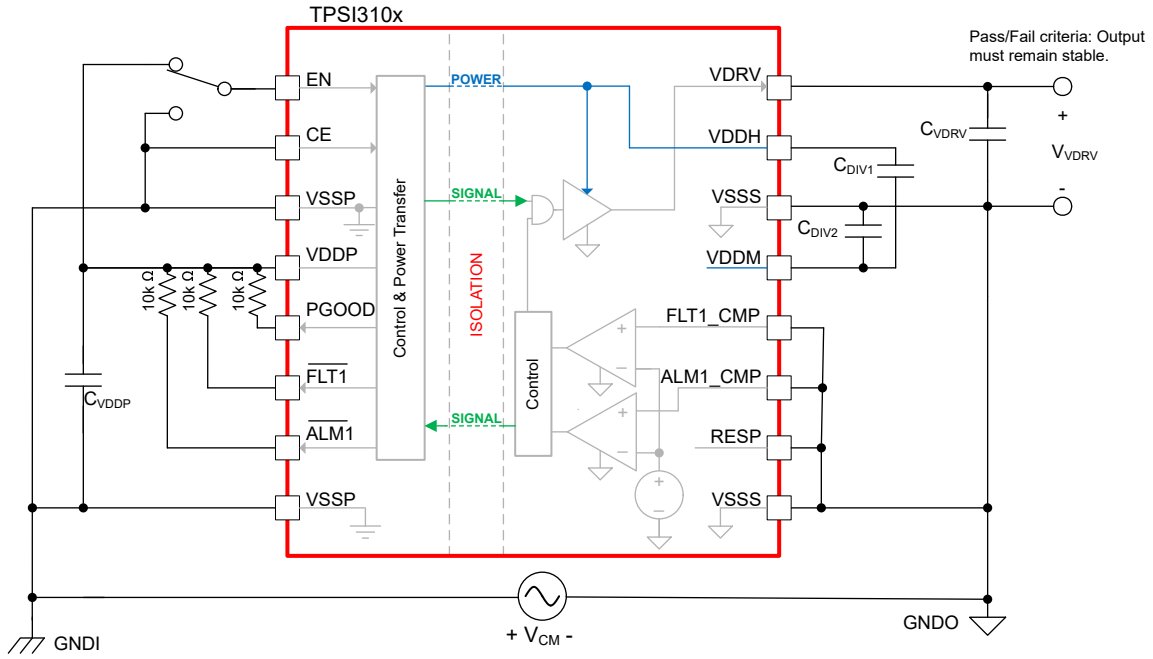


図 7-3. Common-Mode Transient Immunity Test Circuit

ADVANCE INFORMATION

8 Detailed Description

8.1 Overview

The TPSI3100-Q1 is a fully integrated isolated switch driver, which when combined with an external power switch, forms a complete isolated solid state relay solution. With a gate drive voltage of 15.8-V with 1.5/2.5-A peak source/sink current, a large availability of power switches can be used to meet many application needs. The TPSI3100-Q1 generates its own secondary bias supply from power received on its primary side, so no isolated secondary supply bias is required. The TPSI3100-Q1 provides additional power via the nominal 5-V rail (VDDM) for use by auxiliary circuits to perform various function such as current and voltage monitoring or remote temperature detection. The TPSI3100-Q1 isolation is extremely robust with much higher reliability, lower power consumption, and increased temperature ranges than those found using traditional mechanical relays and optocouplers.

The TPSI3100-Q1 integrates a communication back-channel that transfers status information from the secondary side to the primary side via open-drain outputs, PGOOD (Power Good), $\overline{\text{FLT1}}$ (Fault 1), and $\overline{\text{ALM1}}$ (Alarm 1). Dual high-speed comparators with an integrated shared voltage reference are used to assert $\overline{\text{FLT1}}$ and $\overline{\text{ALM1}}$. When the comparator input, FLT1_CMP, exceeds the voltage reference, the driver is immediately asserted low and $\overline{\text{FLT1}}$ is also driven low, indicating to the system that a fault has occurred. This is useful for disabling the external switch with low latency on critical events, such as over-current detection. When the comparator input, ALM1_CMP, exceeds the voltage reference, $\overline{\text{ALM1}}$ signal is asserted low, but no action is taken by the driver. This may be useful as an alarm or warning indicator for over-temperature or over-voltage events.

The TPSI310xL-Q1 series offers a latch based fault indicator. When a fault is detected, the driver and the fault indicator are asserted low and remain latched, until EN is asserted low. The TPSI310x-Q1 series has a non-latched fault indicator. If the fault event is no longer present, $\overline{\text{FLT1}}$ deasserts and the driver, after a specified recovery period, follows the state of the EN pin. If the fault event still remains, both the fault indicator and the driver remain asserted low.

The TPSI310x-Q1 and TPSI310xL-Q1 device family has two voltage options for the integrated reference to meet a wide range of application needs.

The Functional Block Diagram shows the primary side includes a transmitter that drives an alternating current into the primary winding of an integrated transformer which transfers power from the primary side to the secondary side. The transmitter operates at high frequency (80 MHz, nominal) to optimally drive the transformer to its peak efficiency. In addition, the transmitter utilizes spread spectrum techniques to greatly improve EMI performance allowing many applications to achieve CISPR 25 - Class 5. During transmission, data information is transferred to the secondary side alongside with the power. On the secondary side, the voltage induced on the secondary winding of the transformer, is rectified and multiplied, and is regulated to the voltage level of VDDH. Lastly, the demodulator decodes the received data information and drives VDRV high or low, respective of the logic state of the EN pin.

During each transfer of power from the primary side to the secondary side, back-channel state information is automatically sampled, encoded, and sent from the secondary side back to the primary side where it is decoded.

8.2 Functional Block Diagram

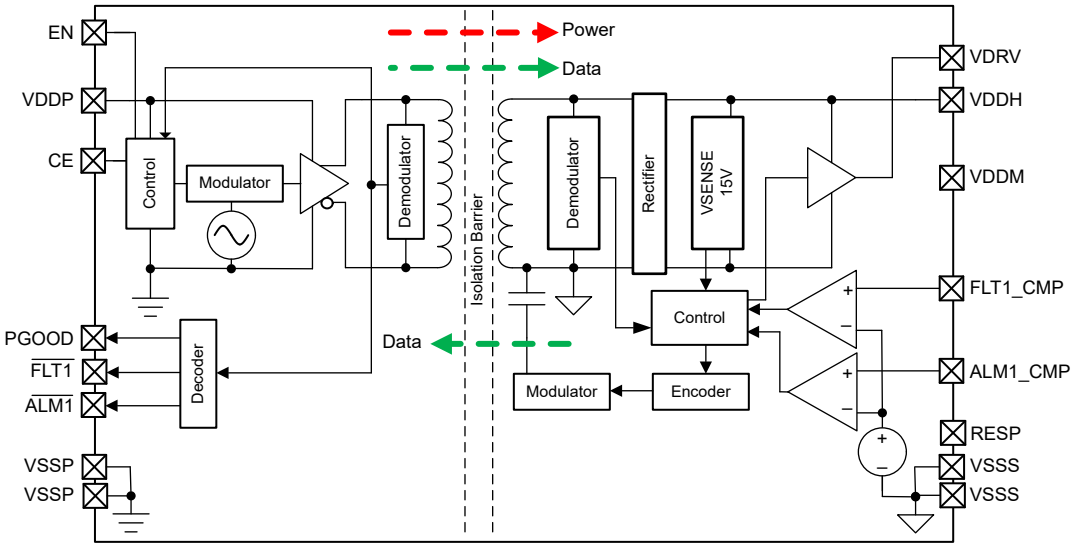


図 8-1. TPSI310x-Q1, TPSI310xL-Q1

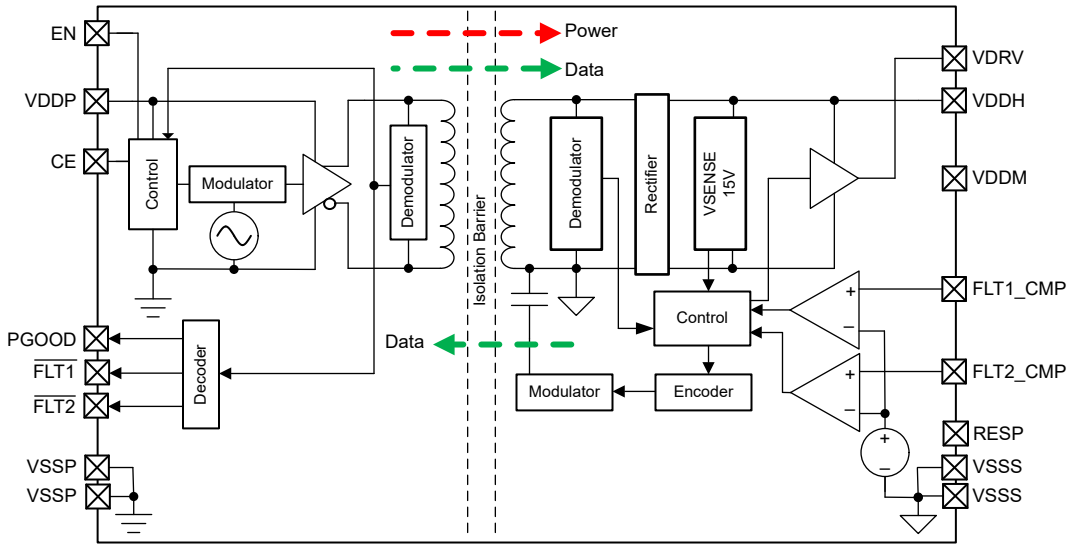


図 8-2. TPSI311x-Q1, TPSI311xL-Q1

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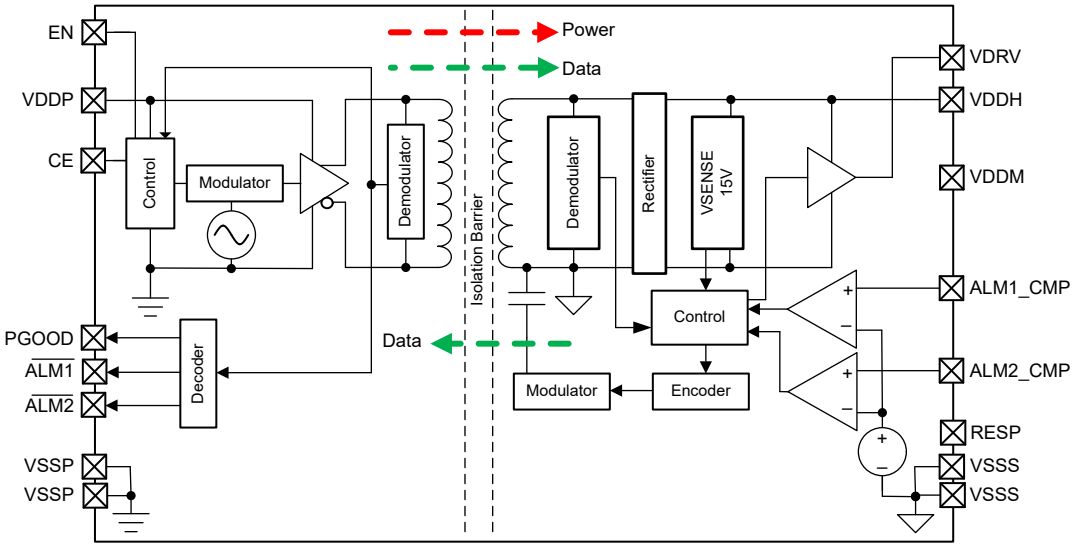

図 8-3. TPSI312x-Q1

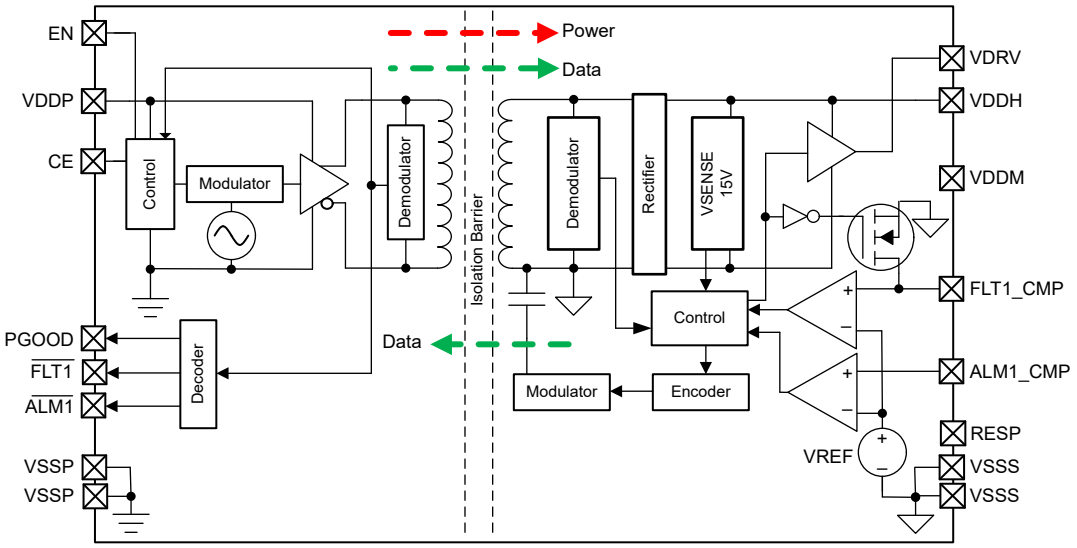

図 8-4. TPSI313x-Q1

8.3 Feature Description

8.3.1 Transmission of the Enable State

The TPSI310x-Q1, TPSI311x-Q1, TPSI312x-Q1, and TPSI313x-Q1 family uses a modulation scheme to transmit the switch enable (EN) state information across the isolation barrier. The transmitter modulates the EN signal with an internally generated, high frequency carrier, and differentially drives the primary winding of the isolation transformer. The receiver on the secondary side demodulates the received signal and asserts VDRV high or low based on the state information received.

8.3.2 Power Transmission

The TPSI310x-Q1, TPSI311x-Q1, TPSI312x-Q1, and TPSI313x-Q1 family does not utilize a secondary side isolated bias supply for its power. The secondary side power is obtained by the transferring of the primary side input power from VDDP across the isolation transformer. The modulation scheme uses spread spectrum techniques to improve EMI performance assisting applications in meeting the CISPR 25 Class 5 standards.

8.3.3 Gate Driver

The TPSI310x-Q1, TPSI311x-Q1, TPSI312x-Q1, and TPSI313x-Q1 family has an integrated gate driver that provides a nominal 15.8-V with 1.5/2.5-A peak source and sink current sufficient for driving many power transistors. When driving external power transistors, TI recommends bypass capacitors ($C_{DIV2} \geq 3 * C_{DIV1}$) from VDDH to VDDM and VDDM to VSSS with an equivalent series capacitance of minimum of 30 times the equivalent gate capacitance. If optional auxiliary circuitry requires power, additional capacitance may be required.

8.3.4 Chip Enable (CE)

The TPSI310x-Q1, TPSI311x-Q1, TPSI312x-Q1, and TPSI313x-Q1 family has an active high chip enable, CE. When CE is asserted high and VDDP is present, the device enters its active mode of operation and power transfer occurs from the primary side to the secondary side. When CE is asserted low while VDDP is present, the device enters standby and no power transfer occurs from primary side to the secondary side and VDRV will be asserted low. Over time, VDDH and VDDM fully discharges depending on the amount of loading present on these rails.

8.3.5 Comparators

The TPSI310x-Q1, TPSI311x-Q1, TPSI312x-Q1, and TPSI313x-Q1 family devices include two identical isolated comparators. A simplified block diagram is shown in 図 8-5. The function of the comparator, fault or alarm, depends on the device orderable in the family. The positive inputs (FLTn_CMP or ALMn_CMP) of each comparator monitor the voltage on these inputs referenced to VSSS. Both comparators share a single integrated voltage reference, VREF, with an accuracy of ±1.5% over voltage and temperature and is connected internally to the negative inputs of each comparator. The reference voltage is internal to the device and not available externally. The reference voltage level depends on the device orderable in the family.

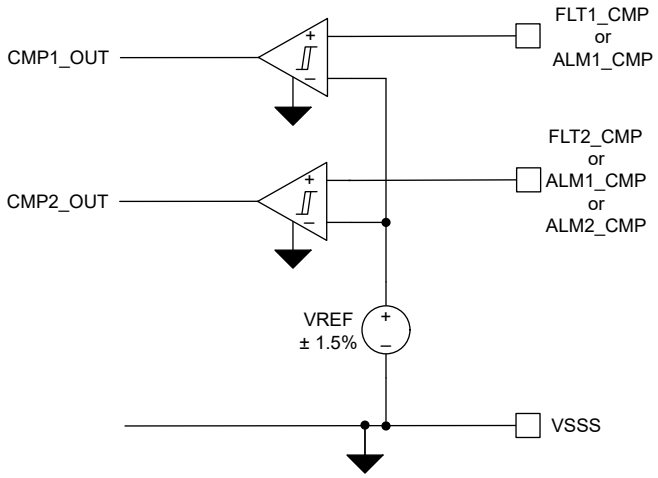

図 8-5. Comparator Block Diagram

8.3.5.1 Fault Comparator

The TPSI310x-Q1 and TPSI313x-Q1 devices include one fault comparator that is used to quickly assert the output driver, VDRV, low to allow for the fastest disable time of the external power switch. This is useful for critical events such as over-current protection (OCP) to protect the external power switch and downstream circuitry. The block diagram of the fault comparator is shown in 図 8-6. The TPSI311x-Q1 devices have two fault comparators. This can be useful for applications such as bi-directional OCP or whenever there are two independent critical events required to protect the external power switch. The TPSI312x-Q1 device does not support any fault comparators, only alarm comparators.

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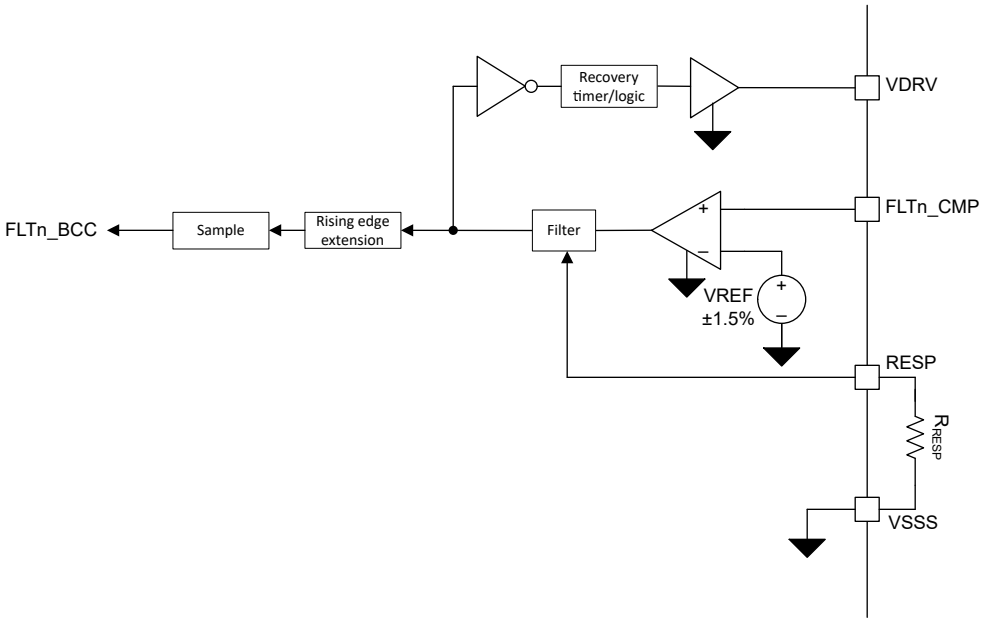

図 8-6. Fault Comparator Block Diagram

If the input voltage of the fault comparator, FLTn_CMP, exceeds the internal reference voltage, VREF, the comparator output asserts high. The comparator output is filtered and is adjustable via an external 1% resistor, R_{RESP}, connected from RESP to VSSS. The filtering of low-to-high transitions of the comparator output is adjustable by the external resistor. High-to-low transitions of the comparator output are filtered at a fixed setting. Filtering the comparator output allows for flexibility and application tradeoffs to help minimize false trigger events while still providing adequate protection. The filtered comparator output is then fed into the driver logic. If the comparator output low-to-high event passes through the filter, VDRV is immediately asserted low regardless of the state of EN. The TPSI310x-Q1, TPSI311x-Q1, and TPSI313x-Q1 fault comparators are not latched. If a fault condition is removed (FLTn_CMP voltage falls below the internal reference voltage and passes through the filter), VDRV is held low until the recovery timer has elapsed. Once the recovery timer has elapsed, VDRV follows the state of EN. If a fault condition occurs before the recovery timer has elapsed, the recovery timer is restarted.

The comparator output information is transferred to the primary side of the device via back-channel communication (BCC) over the isolation barrier. As shown in 図 8-6, any low-to-high transition of the comparator output (fault event) that passes through the filter is extended to make sure the event is captured by the sample logic. Any high-to-low transition of the comparator output (recovery event) that passes through the filter are not extended. A recovery event can be missed by the sample logic if the event does not last longer than the sample period. Therefore, priority is given to fault events over recovery events. $\overline{\text{FLTn}}$ open-drain output is asserted low upon the fault event. If a recovery event occurs and is captured by the sample logic, $\overline{\text{FLTn}}$ open-drain output is set to high-impedance, but VDRV remains asserted low until the recovery timer elapses.

The TPSI310xL-Q1, TPSI311xL-Q1, and TPSI313xL-Q1 devices have latched fault comparators as shown in 図 8-7. Fault events are latched and held until EN is asserted low. Upon a fault event, VDRV asserts low and is held until EN is asserted low and the recovery timer elapses. $\overline{\text{FLTn}}$ is also asserted low and held until EN is asserted low. If the fault event has recovered, $\overline{\text{FLTn}}$ is asserted high even if the recovery timer has not elapsed.

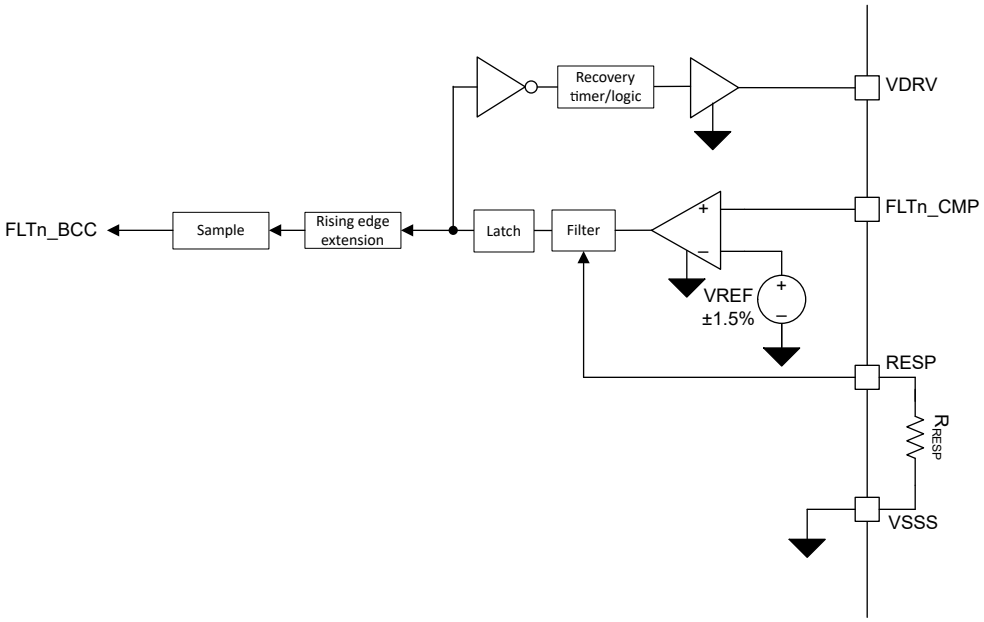

図 8-7. Latched Fault Comparator Block Diagram

8.3.5.2 Alarm Comparator

The TPSI310x-Q1 and TPSI313x-Q1 devices include one alarm comparator. The TPSI312x-Q1 devices include two alarm comparators. An alarm comparator differs from the fault comparator in that the output state of the comparator has no direct control of the VDRV output driver. The block diagram of the alarm comparator is shown in 図 8-8.

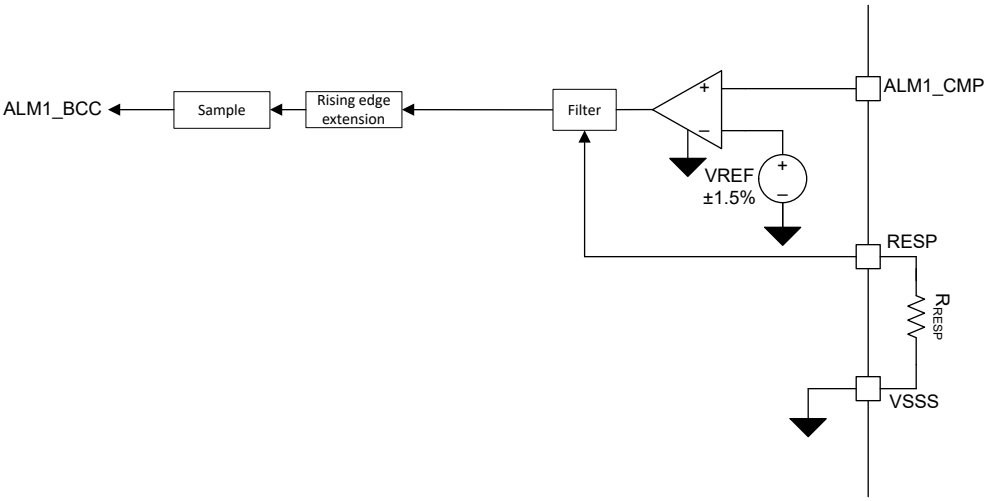

図 8-8. Alarm Comparator Block Diagram

If the input voltage of the alarm comparator, ALM1_CMP, exceeds the internal reference voltage, VREF, the comparator output asserts high. The comparator output is filtered and is adjustable via an external 1% resistor, R_{RESP}, connected from RESP to VSSS. The filtering of low-to-high transitions of the comparator output is adjustable by the external resistor. High-to-low transitions of the comparator output are filtered at a fixed setting. The filter setting is shared by both the fault and alarm comparators and cannot be set independently. In addition, the alarm comparator is not latched.

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Similar to the fault comparator, the alarm comparator output information is transferred to the primary side of the device via back-channel communication (BCC) over the isolation barrier. As shown in 図 8-8, any low-to-high transition of the comparator output (alarm event) that passes through the filter is extended to make sure the event is captured by the sample logic. Any high-to-low transition of the comparator output (recovery event) that passes through the filter are not extended. A recovery event can be missed by the sample logic if the event does not last longer than the sample period. Therefore, priority is given to alarm events over recovery events. $\overline{\text{ALM1}}$ open-drain output is asserted low upon the alarm event. If a recovery event occurs and is captured by the sample logic, $\overline{\text{ALM1}}$ open-drain output is set to high-impedance.

8.3.5.3 Comparator De-glitch

For many applications, there is a tradeoff between detecting critical events and the false triggering of a non-critical events. The RESP pin allows for adjustment of the response time of the comparator based on the application needs. Selection of a 1% resistor from the RESP pin to VSSS allows for filtering of the comparator response. The amount of typical de-glitch, $t_{DEGLITCH\_CMP\_R}$, on the comparator output high assertion is estimated using 式 1, where $t_{DEGLITCH\_CMP\_R}$ units is nanoseconds and R_{RESP} units is kilo-ohm.

$$t_{DEGLITCH\_CMP\_R} = 3.56 \times R_{RESP} + 52.7 \quad (1)$$

If the comparator output high assertion exceeds the duration of $t_{DEGLITCH\_R}$, the comparator output is propagated. Comparator output low assertions are filtered at a fixed setting, $t_{DEGLITCH\_CMP\_F}$.

8.3.6 VDDP, VDDH, and VDDM Under-voltage Lockout (UVLO)

The TPSI310x-Q1, TPSI311x-Q1, TPSI312x-Q1, and TPSI313x-Q1 family implements an internal UVLO protection feature for both input (VDDP) and output power supplies (VDDM and VDDH). The device remains disabled until VDDP exceeds its rising UVLO threshold. When the VDDP supply voltage falls below its falling threshold voltage, the device attempts to send data information to quickly assert VDRV low, regardless of the state of EN. This depends on the rate of VDDP loss. If VDDP collapses too fast to send the information, a timeout mechanism ensures VDRV is asserted low within $t_{HL\_VDRV\_PD}$. A VDDP ULVO event causes PGOOD, $\overline{\text{FLT1}}$, and $\overline{\text{ALM1}}$ to assert low.

The VDDH and VDDM UVLO circuits monitor the voltage on VDDH and VDDM, respectively. VDRV is only asserted high if both the VDDH and VDDM UVLO rising thresholds are surpassed. If either VDDH or VDDM fall below their respective UVLO falling thresholds, VDRV is immediately asserted low. The UVLO protection blocks feature hysteresis, which helps to improve the noise immunity of the power supply. During turn on and turn off, the driver sources and sinks a peak transient current, which can result in voltage drop of the VDDH and VDDM power supplies. The UVLO protection circuits ignores the associated noise during these normal switching transients.

8.3.7 Thermal Shutdown

The TPSI310x-Q1, TPSI311x-Q1, TPSI312x-Q1, and TPSI313x-Q1 family has an integrated temperature sensor. The sensor monitors its local temperature. When the sensor reaches its threshold, it automatically disables power transfer from the primary side to the secondary side, and sends data information to disable the driver, VDRV. The power transfer and driver are disabled until the local temperature reduces enough to re-engage.

8.4 Device Operation

VDDP must be supplied independently by a low impedance external supply that can deliver the required power. When VDDP power is present and CE is a logic high, power transfers from the primary side to the secondary side. Setting the EN pin logic high or low asserts or deasserts VDRV, thereby enabling or disabling the external switch, respectively. 図 8-9 shows the basic set-up required for proper operation which requires EN, VDDP, and VSSP signals. EN may be driven up to 5.5-V which is normally driven from circuitry on the same rail as VDDP. In this example, the TPSI310x-Q1 is being used to drive back-to-back MOSFETs in a common-source configuration. Driving back-to-back MOSFETs is required for AC switching applications or DC switching where reverse blocking is required. C_{VDDP} provides the required decoupling capacitance for the VDDP supply. C_{DIV1}

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and C_{DIV2} provide the required decoupling capacitance of the VDDH/VDDM supply rails to provide peak current to drive the external MOSFETs.

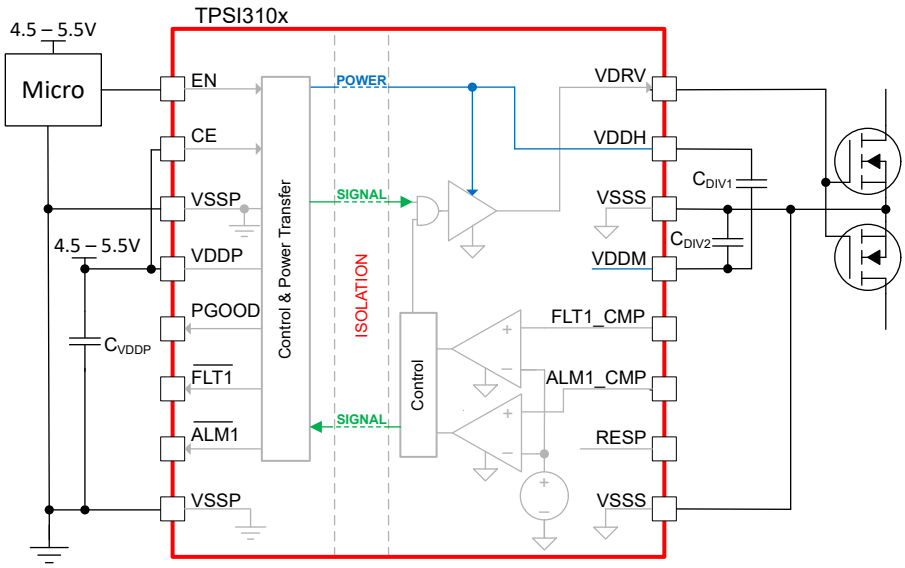

図 8-9. Simplified Schematic

図 8-10 shows the basic operation from start up to steady state conditions.

- At T1: VDDP powers up the device. $\overline{\text{FLTn}}$, $\overline{\text{ALMn}}$, and PGOOD are asserted low.
- At T2 and T3: TPSI310x-Q1 begins to transfer power from VDDP to the secondary side for a fixed burst period (25 µs typical), which begins to charge up the VDDH and VDDM secondary side rails. Power transfer continues as long as VDDP is present (and CE remains high). The time required to fully charge VDDH depends on several factors including the values of VDDP, C_{DIV1}, C_{DIV2}, the amount of auxiliary load drawn from VDDM, and the overall power transfer efficiency.
- At T4, T5, and T6: After four burst periods, the $\overline{\text{FLTn}}$, $\overline{\text{ALMn}}$, and PGOOD are released and begin to reflect their respective status. PGOOD asserts high if VDDM and VDDH are both above their UVLO thresholds, otherwise remains asserted low. $\overline{\text{FLTn}}$ and $\overline{\text{ALMn}}$ indicate the status of their comparator outputs. In this example, since FLTn_CMP and ALMn_CMP are tied to VSSS, $\overline{\text{FLTn}}$ and $\overline{\text{ALMn}}$ assert high. The status indicators are always transferred sequentially in the order of $\overline{\text{FLTn}}$, $\overline{\text{ALMn}}$, and PGOOD with a delay of approximately 400 ns between each indicator.
- At T7 and T8: EN is asserted high and VDRV asserts high. Note that VDRV will not assert high until VDDH and VDDM are both above their UVLO thresholds. Due to latency of the $\overline{\text{FLTn}}$, $\overline{\text{ALMn}}$, and PGOOD indicators, it is possible that VDRV asserts high prior to PGOOD asserting high.

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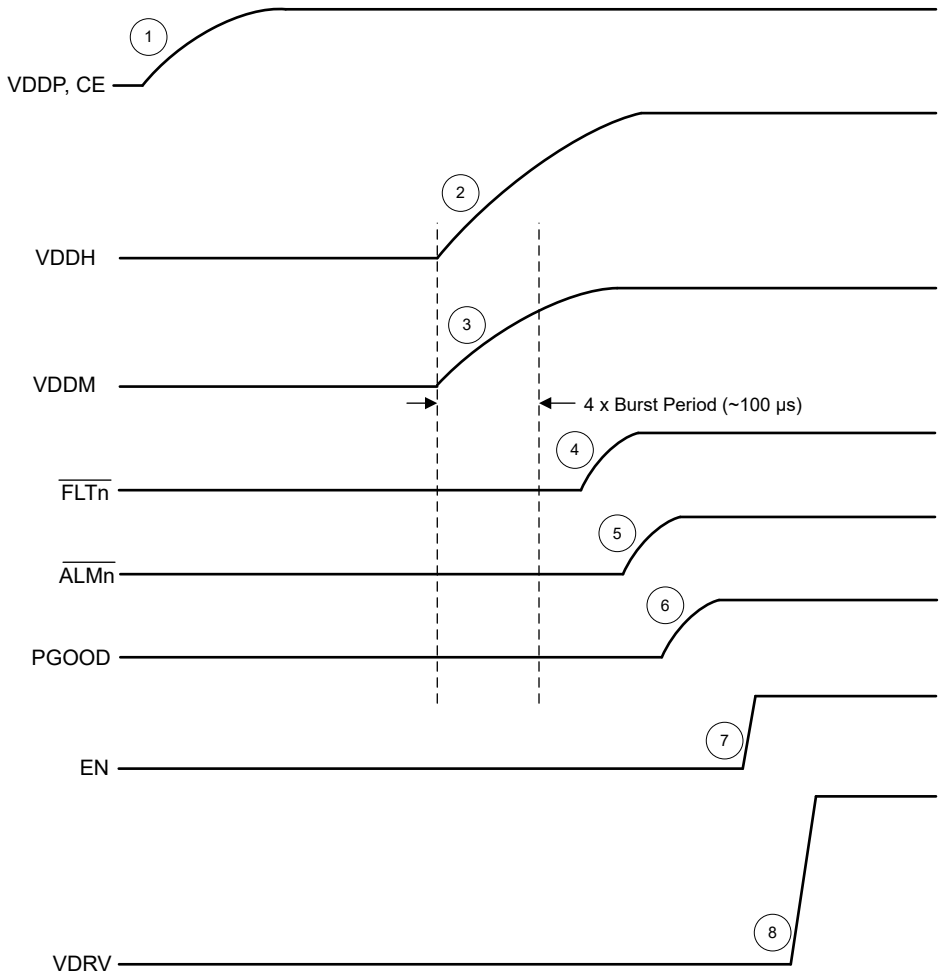

図 8-10. TPSI310x-Q1 Typical Start-up (CE = VDDP, FLTn_CMP = 0, ALMn_CMP = 0)

図 8-11 shows start up sequence where VDDP, CE, and EN signals are tied together.

- At T1: VDDP powers up the device. $\overline{\text{FLTn}}$, $\overline{\text{ALMn}}$, and PGOOD are asserted low.
- At T2 and T3: TPSI310x-Q1 begins to transfer power from VDDP to the secondary side for a fixed burst period (25 µs typical), which begins to charge up the VDDH and VDDM secondary side rails.
- At T4: VDRV asserts high when both VDDH and VDDM are above their UVLO thresholds.
- At T5, T6, and T7: After four burst periods, the $\overline{\text{FLTn}}$, $\overline{\text{ALMn}}$, and PGOOD are released and begin to reflect their respective status. In this specific example, it is assumed that VDDH and VDDM rails have charged up beyond their UVLO thresholds under the four burst periods (100 µs). In this case, due to the PGOOD latency, PGOOD is asserted high after VDRV is asserted high.

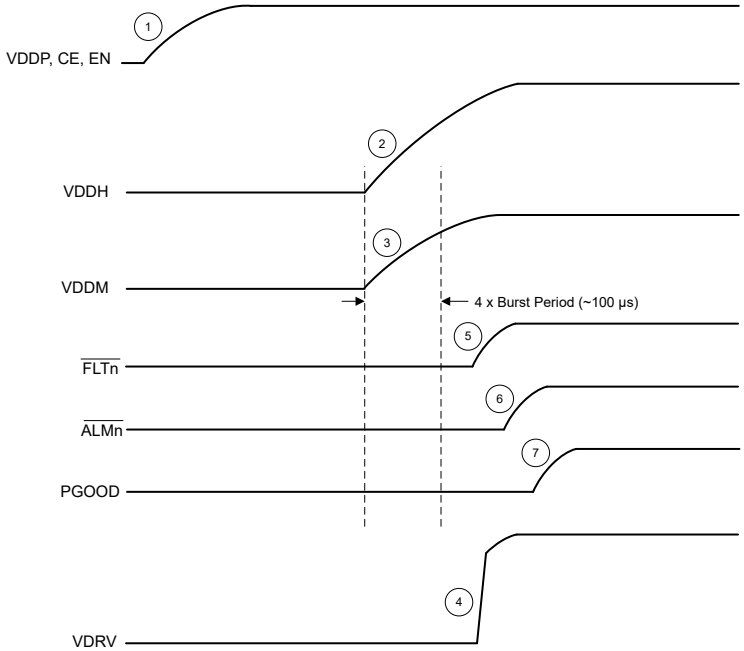

図 8-11. TPSI310x-Q1 Typical Start-up (CE = EN = VDDP, FLTn_CMP = 0, ALMn_CMP = 0)

To reduce average power, the TPSI310x-Q1 transfers power from the primary side to the secondary side in a burst fashion. The period of the burst is fixed while the burst on time is determined internally by the control loop regulating the VDDM voltage. The burst on time is automatically adjusted based upon the status of the VDDM voltage thereby optimizing power transfer for a given load condition. During power up, the device operates at the highest power setting. This helps to quickly charge up the VDDM and VDDH rails.

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8.5 Device Functional Modes

表 8-1 summarizes the functional modes for the TPSI310x-Q1 and TPSI310xL-Q1.

表 8-1. TPSI310x-Q1, TPSI311x-Q1, TPSI312x-Q1, and TPSI313x-Q1 family, Functional Modes(1)(2)

CE	VDDP	VDDH, VDDM	EN	VDRV	PGOOD	COMMENTS
X	Powered Down(4)	Powered Down(6)	X	L	L	Powered Down: VDRV output disabled, keep off circuitry applied.
L	Powered Up(3)	Powered Down(6)	X	L	L	Disabled Operation: When CE is asserted low, power transfer to the secondary ceases. VDDH and VDDM rails discharge pending loading. VDRV output disabled, keep off circuitry applied.
H	Powered Up(3)	Powered Up(5)	L	L	H	Normal Operation: VDRV output state follows logic state of EN logic state.
			H	H	H	
X	Powered Down(4)	Powered Up(5)	X	L	L	Disabled Operation: When VDDP is powered down, output driver is disabled automatically. If sufficient VDDP power is available, VDRV is disabled within the propagation delay, otherwise after the timeout duration. Keep off circuitry applied.

(1) No alarm or fault conditions present (FLTn_CMP = ALMn_CMP = 0).
(2) X: do-not-care.
(3) V_{VDDP} ≥ VDDP_UVLO threshold.
(4) V_{VDDP} < VDDP_UVLO threshold.
(5) V_{VDDH} ≥ VDDH_UVLO threshold and V_{VDDM} ≥ VDDM_UVLO threshold.
(6) V_{VDDH} <VDDH_UVLO threshold or V_{VDDM} < VDDM_UVLO threshold.

表 8-2 summarizes fault and comparator functional behavior.

表 8-2. $\overline{\text{FLTn}}$, $\overline{\text{ALMn}}$ Functional Behavior(1)

CE(2)	FLTn_CMP(3)	ALMn_CMP(4)	$\overline{\text{FLTn}}$ (5)	$\overline{\text{ALMn}}$ (5)	COMMENTS
L	X	X	L	L	VDRV output disabled, keep off circuitry applied.
H	L	L	Hi-Z	Hi-Z	VDRV output follows state of EN pin.
H	L	H	Hi-Z	L	Fault detected. VDRV output asserted low until recovery timer elapses. On latched fault devices, VDRV asserts low and remains low until EN asserts low then high and recovery timer elapses.
H	H	L	L	Hi-Z	Alarm detected. VDRV output unchanged.
H	H	H	L	L	Fault and alarm detected. VDRV output asserted low until recovery timer elapses. On latched fault devices, VDRV asserts low and remains low until EN asserts low then high and recovery timer elapses.

(1) Assumes V_{VDDP} ≥ VDDP_UVLO threshold and device is fully powered in steady state conditions.
(2) L: $V_{CE} < V_{IT\_-(CE)}$, H: $V_{CE} \geq V_{IT\_+(CE)}$.
(3) L: $V_{FLTn\_CMP} < V_{REF}$, H: $V_{FLTn\_CMP} \geq V_{REF}$.
(4) L: $V_{ALMn\_CMP} < V_{REF}$, H: $V_{ALMn\_CMP} \geq V_{REF}$.
(5) Hi-Z: Open-drain output disabled, L: Open-drain output enabled.

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9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The TPSI310x-Q1 is a fully integrated, isolated switch driver with integrated bias, which when combined with an external power switch, forms a complete isolated solid state relay solution. With a nominal gate drive voltage of 15.8-V with 1.5/3.0-A peak source and sink current, a large variety of external power switches such as MOSFETs, IGBTs, or SCRs can be chosen to meet a wide range of applications. The TPSI310x-Q1 generates its own secondary bias supply from the power received from its primary side, so no isolated secondary supply bias is required.

The secondary side provides a regulated, floating supply rail of 15.8-V for driving a large variety of power switches with no need for a secondary bias supply. The TPSI310x-Q1 can support driving single power switch, dual back-to-back, parallel power switches for a variety of AC or DC applications. The TPSI310x-Q1 integrated isolation protection is extremely robust with much higher reliability, lower power consumption, and increased temperature ranges than those found using traditional mechanical relays and optocouplers.

The TPSI310x-Q1 integrates a communication back-channel that transfers various status information from the secondary side to the primary side via open-drain outputs, PGOOD (Power Good), $\overline{\text{FLT1}}$ (Fault 1), and $\overline{\text{ALM1}}$ (Alarm 1). Two high-speed comparators with an integrated shared voltage reference are used to assert $\overline{\text{FLT1}}$ and $\overline{\text{ALM1}}$. When the comparator input, FLT1_CMP, exceeds the voltage reference, the driver is immediately asserted low and $\overline{\text{FLT1}}$ on the primary side is driven low after some latency, indicating a fault has occurred. This is useful for directly disabling the external switch from the secondary on critical events with low latency, such as short circuit detection. When the comparator input, ALM1_CMP, exceeds the voltage reference, $\overline{\text{ALM1}}$ signal is asserted low on the primary side, but no action is taken by the driver. This may be useful as an alarm or warning indicator.

9.2 Typical Application

The simplified circuit diagram shown in 図 9-1 is a typical over-current protection application using the TPSI3103-Q1. The TPSI3103-Q1 interfaces to the INA181 current sense amplifier. The TPSI3103-Q1 provides power to the current sense amplifier and supporting circuitry via its VDDM power rail. The current sense amplifier is used to amplify the voltage formed across the shunt resistor, R_{SHUNT}, during load conditions. Although the INA181 was chosen for this example, any current sense amplifier may be used that meets the design criteria.

The circuit uses the alarm comparator to signal a warning to the system via the $\overline{\text{ALM1}}$ status indicator. $\overline{\text{ALM1}}$ asserts low when the alarm threshold is exceeded. The fault comparator is used to detect an over-current event and disables the driver at the set over-current threshold. The system is notified via the $\overline{\text{FLT1}}$ status indicator asserting low.

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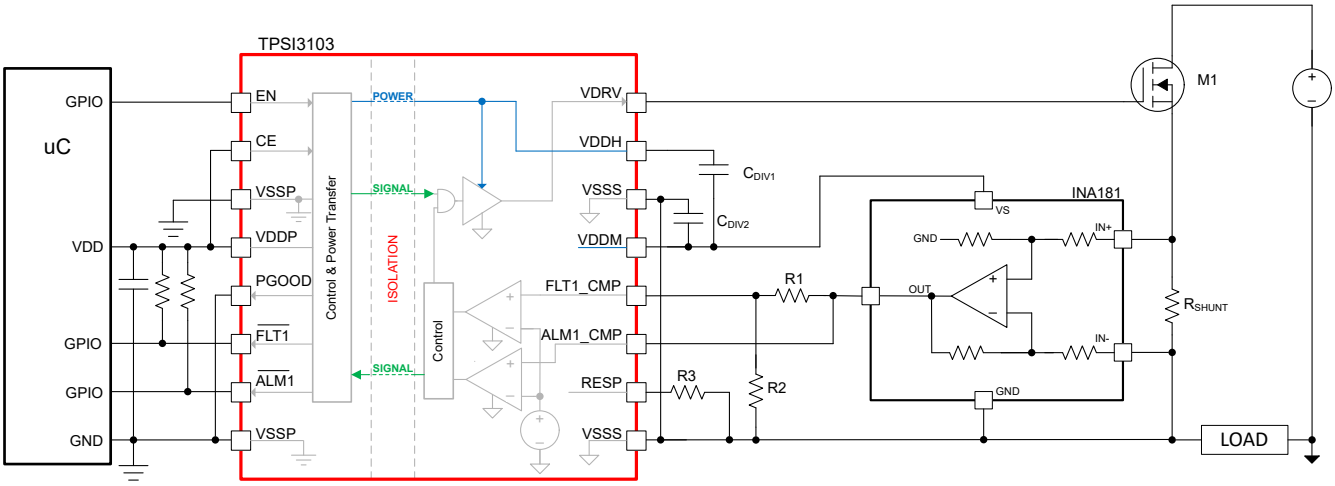

図 9-1. Typical Over-current Protection Application

9.2.1 Design Requirements

表 9-1 lists the design requirements of the TPSI310x-Q1 gate driver. The application requires driving external FETs. It includes circuitry for a two-level over-current protection that is powered by the TPSI310x-Q1. The TPSI3100-Q1 used in this example includes a 0.3-V voltage reference.

表 9-1. TPSI310x-Q1 Design Requirements

DESIGN PARAMETERS	
Total gate capacitance	120 nC
FET turn-off time upon fault detection	< 0.5 µs
Switching frequency	2 kHz
Supply voltage (VDDP)	5 V ±5%
Over-current fault	10 A ±10%
Over-current alarm	5 A ±10%
Shunt resistor power	0.5 W
Shunt resistor tolerance	±1%

9.2.2 Detailed Design Procedure

9.2.2.1 C_{DIV1}, C_{DIV2} Capacitance

The C_{DIV1} and C_{DIV2} capacitors required depends on the amount of drop that can be tolerated on the VDDH rail during switching of the external load. The charge stored on the C_{DIV1} and C_{DIV2} capacitors is used to provide the current to the load during switching. During switching, charge sharing occurs and the voltage on VDDH drops. At a minimum, TI recommends that the total capacitance formed by the series combination of C_{DIV1} and C_{DIV2} be sized to be at least 30 times the total gate capacitance to be switched. This sizing results in an approximate 0.5-V drop of the VDDH supply rail that is used to supply power to the VDRV signal. 式 2 and 式 3 can be to used to calculate the amount of capacitance required for a specified voltage drop.

C_{DIV1} and C_{DIV2} must be of the same type and tolerance.

$$C_{DIV1} = \left(\frac{n+1}{n}\right) \times \frac{Q_{LOAD}}{\Delta V},\ n \geq 3.0 \quad (2)$$

$$C_{DIV2} = n \times C_{DIV1},\ n \geq 3.0 \quad (3)$$

where

- n is a real number greater than or equal to 3.0.

- C_{DIV1} is the external capacitor from VDDH to VDDM.
- C_{DIV2} is the external capacitor from VDDM to VSSS.
- Q_{LOAD} is the total charge of the load from VDRV to VSSS.
- ΔV is the voltage drop on VDDH when switching the load.

注

C_{DIV1} and C_{DIV2} represent absolute capacitor and components selected must be adjusted for tolerances and any derating necessary to achieve the required capacitance.

Larger values of ΔV can be used in the application, but excessive droop can cause the VDDH under-voltage lockout falling threshold ($V_{VDDH\_UVLO\_F}$) to be reached and cause VDRV to be asserted low. Note that as the series combination of C_{DIV1} and C_{DIV2} capacitance increases relative to Q_{LOAD}, the VDDH supply voltage drop decreases, but the initial charging of the VDDH supply voltage during power up increases.

For this design, assuming n = 3 and ΔV = 0.5 V, then

$$C_{DIV1} = \left(\frac{3+1}{3}\right) \times \frac{120\ nC}{0.5\ V} = 320\ nF \tag{4}$$

$$C_{DIV2} = 3 \times 320\ nF = 960\ nF \tag{5}$$

9.2.2.2 Start-up Time and Recovery Time

As described in the 式 3 section, the start-up time of the fully discharged VDDH and VDDM rails depends on the amount of capacitance present on the VDDH and VDDM pins, as well as, power being used from VDDM for any auxiliary circuitry. The rate at which this capacitance is charged depends on the amount of power transferred from the primary side to the secondary side. At start up, the power regulation loop transfers more power until the VDDH and VDDM rails reach their steady state values.

9.2.2.3 R_{SHUNT}, R1, and R2 Selection

The TPSI3100-Q1 has an internal nominal voltage reference (V_{REF}) of 0.3 V. This reference is shared by the fault and alarm comparator negative inputs. To minimize the R_{SHUNT} resistance value and hence its associated power dissipation, a current sense amplifier is used that has a gain (G_{CSA}) of 20 V/V.

The alarm event should be detected when the load current, I_{LOAD}, reaches 5 A nominal. This corresponds to a voltage input to the current sense amplifier (V_{SENSE_ALM}) of:

$$V_{SENSE\_ALM} = \frac{V_{REF}}{G_{CSA}} = \frac{0.3V}{20} = 15\ mV \tag{6}$$

From this, the nominal shunt resistance, R_{SHUNT} may be calculated:

$$R_{SHUNT} = \frac{V_{SENSE\_ALM}}{I_{LOAD}} = \frac{15mV}{5A} = 3\ m\Omega \tag{7}$$

The corresponding power prior to an over-current condition due to the shunt resistor may be calculated:

$$P_{SHUNT} = {I_{OCP}}^2 \times R_{SHUNT} = (10\ A)^2 \times 3\ m\Omega = 300\ mW \tag{8}$$

The power dissipated in the shunt resistor is below the design requirement of 0.5 W.

The fault event should be detected when the load current, I_{LOAD}, reaches 10 A nominal. This corresponds to a voltage input to the current sense amplifier (V_{SENSE_FLT}) of:

$$V_{SENSE\_FLT} = R_{SHUNT} \times I_{LOAD} = 3\ m\Omega \times 10A = 30\ mV \tag{9}$$

The resulting output of the current sense amplifier (V_{CSA_FLT}) is:

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$$V_{CSA\_FLT} = V_{SENSE\_FLT} \times G_{CSA} = 30\,mV \times 20 = 0.6\,V \quad (10)$$

Since the fault comparator threshold of the TPSI3100-Q1 is 0.3 V, a resistor divider is required to scale the current sense amplifier output voltage (V_{CSA_FLT}) to the comparator input threshold (V_{REF}). The divider ratio (DIV) required can be calculated from:

$$DIV = \frac{V_{REF}}{R_{SHUNT} \times I_{LOAD} \times G_{CSA}} = \frac{V_{REF}}{V_{CSA\_FLT}} = 0.5 \quad (11)$$

$$DIV = \frac{R2}{R1 + R2} \quad (12)$$

9.2.2.4 Over-current Fault Error

There are several sources of error that contribute to total error in the over-current detection accuracy. These include:

1. Voltage reference tolerance (includes comparator offset)
2. Current sense amplifier gain error
3. Current sense amplifier offset
4. Shunt resistor tolerance
5. Divider resistor tolerances

For this design, an over-current protection accuracy of ± 10% is required. The comparator offset and voltage reference tolerance of the TPSI3100-Q1 can be found in the *Electrical Characteristics* section of the data sheet.

The error contribution due to the current sense amplifier offset can be estimated as follows:

$$\%Err_{CSA\_offset} = 100\% \times \frac{V_{CSA\_OFFSET}}{I_{OCP} \times R_{SHUNT}} = 100\% \times \frac{0.5mV}{10\,A \times 3\,m\Omega} = \pm 1.7\,\% \quad (13)$$

The resistor tolerances of the resistor divider are chosen as 1%. The current sense amplifier gain error is 1%. The reference voltage tolerance is ± 1.5%. Lastly, the selected shunt resistor tolerance is ± 1%

It is assumed that all error contributors are independent variables, so that the total expected error adds in a root mean squared fashion as follows:

$$\%\mathrm{Err}_{\mathrm{OCP\_TOTAL}} = \left[\%\mathrm{Err}_{\mathrm{CSA\_offset}}{}^2 + \%\mathrm{Err}_{\mathrm{VREF}}{}^2 + \%\mathrm{Err}_{\mathrm{R1}}{}^2 + \%\mathrm{Err}_{\mathrm{R2}}{}^2 + \%\mathrm{Err}_{\mathrm{RSHUNT}}{}^2 + \%\mathrm{Err}_{\mathrm{GAIN}}{}^2\right]^{0.5} \quad (14)$$

$$\%\mathrm{Err}_{\mathrm{OCP\_TOTAL}} = \left[(1.7\%)^2 + (1.5\%)^2 + (1\%)^2 + (1\%)^2 + (1\%)^2 + (1\%)^2\right]^{0.5} = 3.0\,\% \quad (15)$$

9.2.2.5 Over-current Alarm Error

The total error for the alarm or warning indicator is similar to the over-current protection total error except the error contribution due to the resistor divider does not affect the total error.

$$\%Err_{CSA\_offset} = 100\% \times \frac{V_{CSA\_OFFSET}}{I_{ALM} \times R_{SHUNT}} = 100\% \times \frac{0.5mV}{5\,A \times 3\,m\Omega} = \pm 3.3\,\% \quad (16)$$

The error contribution due to the current sense amplifier offset is increased since the load current being detected is reduced.

As before, it is assumed that all error contributors are independent variables, so that the total expected error adds in a root mean squared fashion as follows:

$$\%Err_{ALM\_TOTAL} = \left[\%Err_{CSA\_offset}{}^2 + \%Err_{VREF}{}^2 + \%Err_{RSHUNT}{}^2 + \%Err_{GAIN}{}^2\right]^{0.5} \quad (17)$$

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$$\%Err_{ALM\_TOTAL} = \left[(3.3\%)^2 + (1.5\%)^2 + (1\%)^2 + (1\%)^2\right]^{0.5} = 3.9\% \quad (18)$$

9.2.2.6 VDDP Capacitance, C_{VDDP}

For this design, 1 µF in parallel with 100 nF is used.

9.2.3 Application Curves

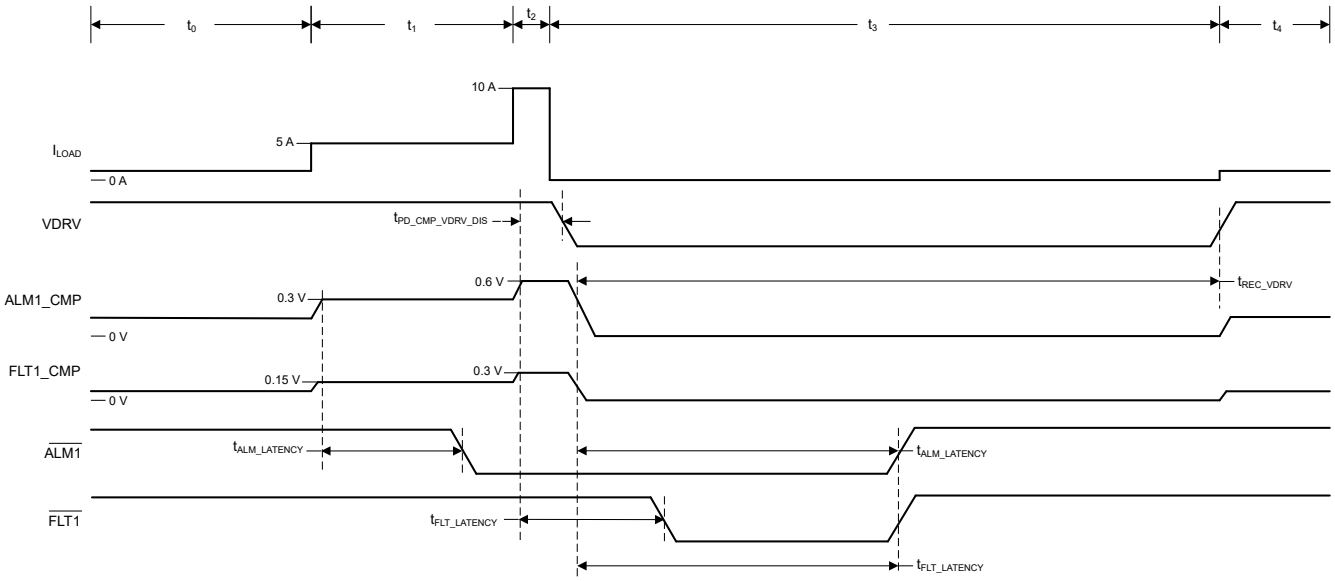

図 9-2. Over-current protection typical timing and behavior

- At t_0: VDRV is asserted high and the external FETs are supplying load current, I_{LOAD}. I_{LOAD} is in its normal operating range and is below the alarm level setting of 5 A, nominal. ALM1_CMP and FLT1_CMP comparator input voltages are below the comparator threshold set by VREF of the TPSI3100-Q1 of 0.3 V,nominal). $\overline{ALM1}$ and $\overline{FLT1}$ faults are asserted high pulled-up by external resistor pull-ups to VDDP.
- At t_1: I_{LOAD} current increases and reaches the alarm level setting of 5 A, nominal. ALM1_CMP comparator input voltage reaches its threshold of 0.3 V and $\overline{ALM1}$ asserts low within $t_{ALM\_LATENCY}$. VDRV remains asserted high since the FLT1_CMP comparator input threshold has not been reached. $\overline{FLT1}$ remains asserted high pulled-up by the external resistor pull-up to VDDP.
- At t_2: I_{LOAD} current continues to increases and reaches the fault level setting of 10 A, nominal. FLT1_CMP comparator input voltage reaches its threshold of 0.3 V and VDRV is quickly asserted low to disable the external FETs. $\overline{FLT1}$ asserts low within $t_{FLT\_LATENCY}$. $\overline{ALM1}$ remains asserted low since the ALM1_CMP comparator input exceeds its threshold.
- At t_3: Since the FETs have been turned off, I_{LOAD}, is removed. FLT1_CMP and ALM1_CMP comparator inputs drop below their thresholds, settling to VSSS. VDRV remains asserted low keeping the external FETs off for t_{REC_VDRV}. $\overline{FLT1}$ and $\overline{ALM1}$ assert high within $t_{FLT\_LATENCY}$ and $t_{ALM\_LATENCY}$, respectively indicating to the system that fault and alarm conditions have been removed.
- At t_4: VDRV asserts high again since EN remains high, t_{REC_VDRV} time has elapsed, and the fault condition is no longer present. The external FETs are enabled and supply I_{LOAD} in its normal operating range.

9.3 Power Supply Recommendations

To help ensure a reliable supply voltage, TI recommends that the C_{VDDP} capacitance from VDDP to VSSP consists of a 0.1-µF bypass capacitor for high frequency decoupling in parallel with a 1-µF for low frequency decoupling. Low-ESR and low-ESL capacitors must be connected close to the device between the VDDP and VSSP pins.

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9.4 Layout

9.4.1 Layout Guidelines

Designers must pay close attention to PCB layout to achieve optimum performance for the TPSI310x-Q1, TPSI311x-Q1, TPSI312x-Q1, and TPSI313x-Q1 family. Some key guidelines are:

- Component placement:
  - Place the driver as close as possible to the power semiconductor to reduce the parasitic inductance of the gate loop on the PCB traces.
  - Connect low-ESR and low-ESL capacitors close to the device between the VDDH and VDDM pins and the VDDM and VSSS pins to bypass noise and to support high peak currents when turning on the external power transistor.
  - Connect low-ESR and low-ESL capacitors close to the device between the VDDP and VSSP pins.
  - Minimize parasitic capacitance on the RESP pin.
- Grounding considerations:
  - Limit the high peak currents that charge and discharge the transistor gates to a minimal physical area. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. Place the gate driver as close as possible to the transistors.
  - Connect the driver VSSS to the Kelvin connection of MOSFET source or IGBT emitter. If the power device does not have a split Kelvin source or emitter, connect the VSSS pin as close as possible to the source or emitter terminal of the power device package to separate the gate loop from the high power switching loop.
- EMI considerations:

  The TPSI310x-Q1, TPSI311x-Q1, TPSI312x-Q1, and TPSI313x-Q1 family employs spread spectrum modulation (SSM), and in some systems, no additional system design considerations are required to meet the EMI performance needs. However, the system designer may choose to take additional measures to minimize EMI depending on the system requirements and safety preferences of the system designer. The measures listed below reduce emissions by providing a capacitive return path from the secondary side to the primary side or by increasing the common mode loop impedance with an inductive component on the primary side.

  - Inductive components: A pair of ferrite beads or a common mode choke with a high frequency impedance on the order of TBD kΩ can be placed in series with VDDP supply and VSSP ground.
  - Capacitive components: Most system designs already employ discrete Y capacitors or contain an amount of parasitic Y capacitance between the high voltage and low voltage domains. If this Y capacitance is located on the same board as the TPSI310x-Q1, TPSI311x-Q1, TPSI312x-Q1, and TPSI313x-Q1 family, they act as a capacitive return path.
- High-voltage considerations:
  - To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. TI recommends a PCB cutout or groove to prevent contamination that can compromise the isolation performance.
- Thermal considerations:
  - Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction-to-board thermal impedance (θ_{JB}).
  - If the system has multiple layers, TI also recommends connecting the VDDH and VSSS pins to internal ground or power planes through multiple vias of adequate size. These vias must be located close to the IC pins to maximize thermal conductivity. However, keep in mind that no traces or coppers from different high voltage planes are overlapping.

9.4.2 Layout Example

図 9-3 shows a PCB layout example with the signals and key components labeled.

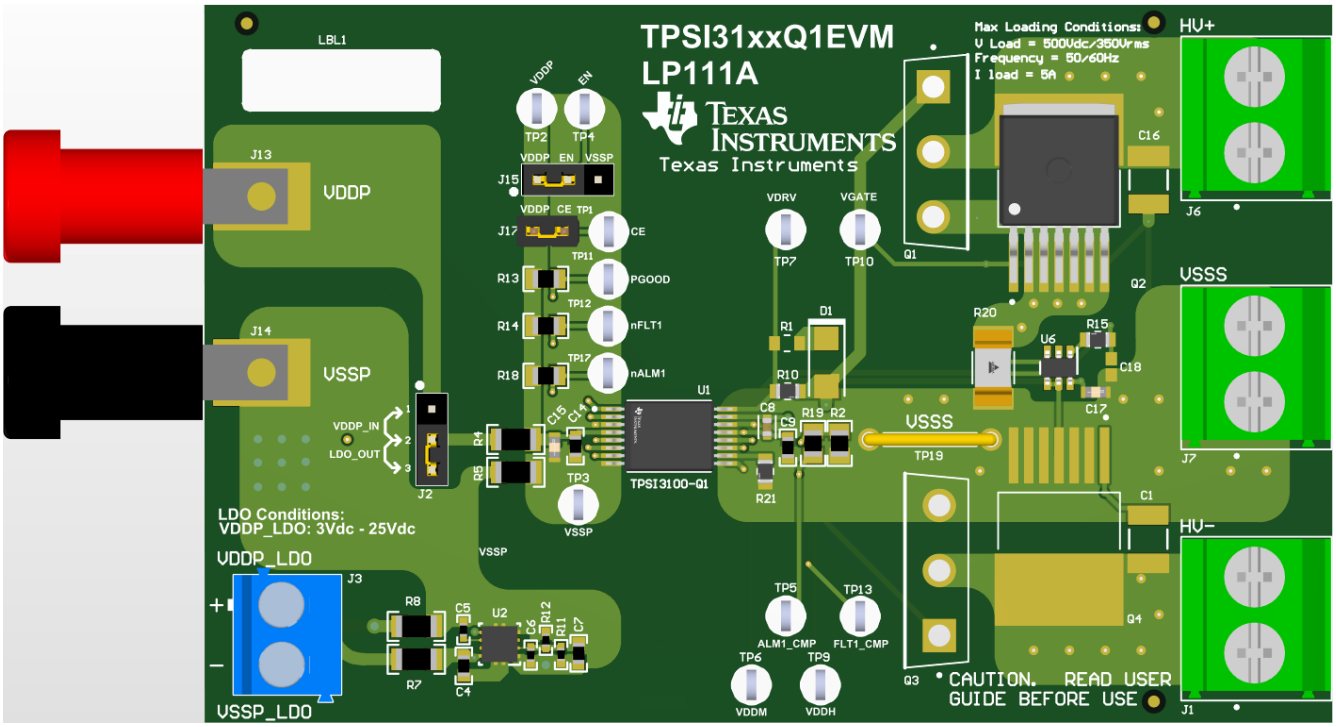


図 9-3. 3-D PCB View

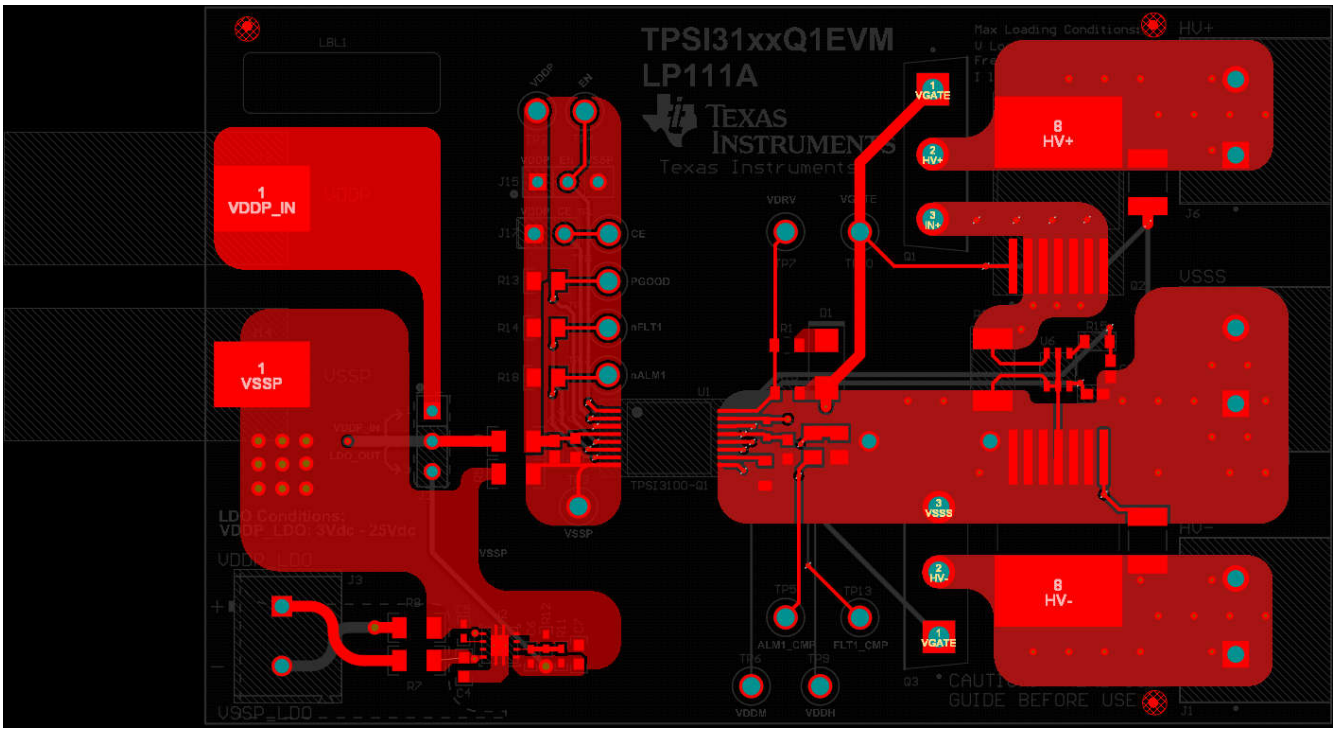


図 9-4. Top Layer

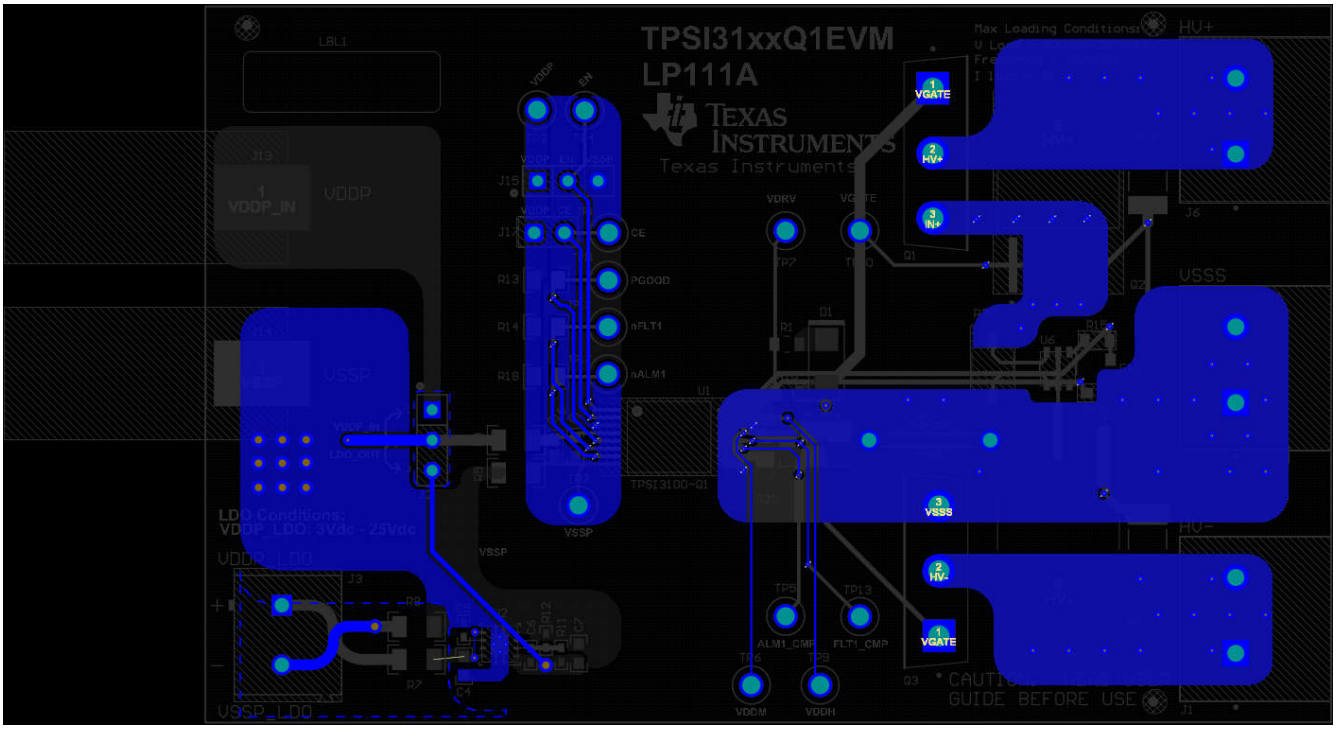


図 9-5. Bottom Layer

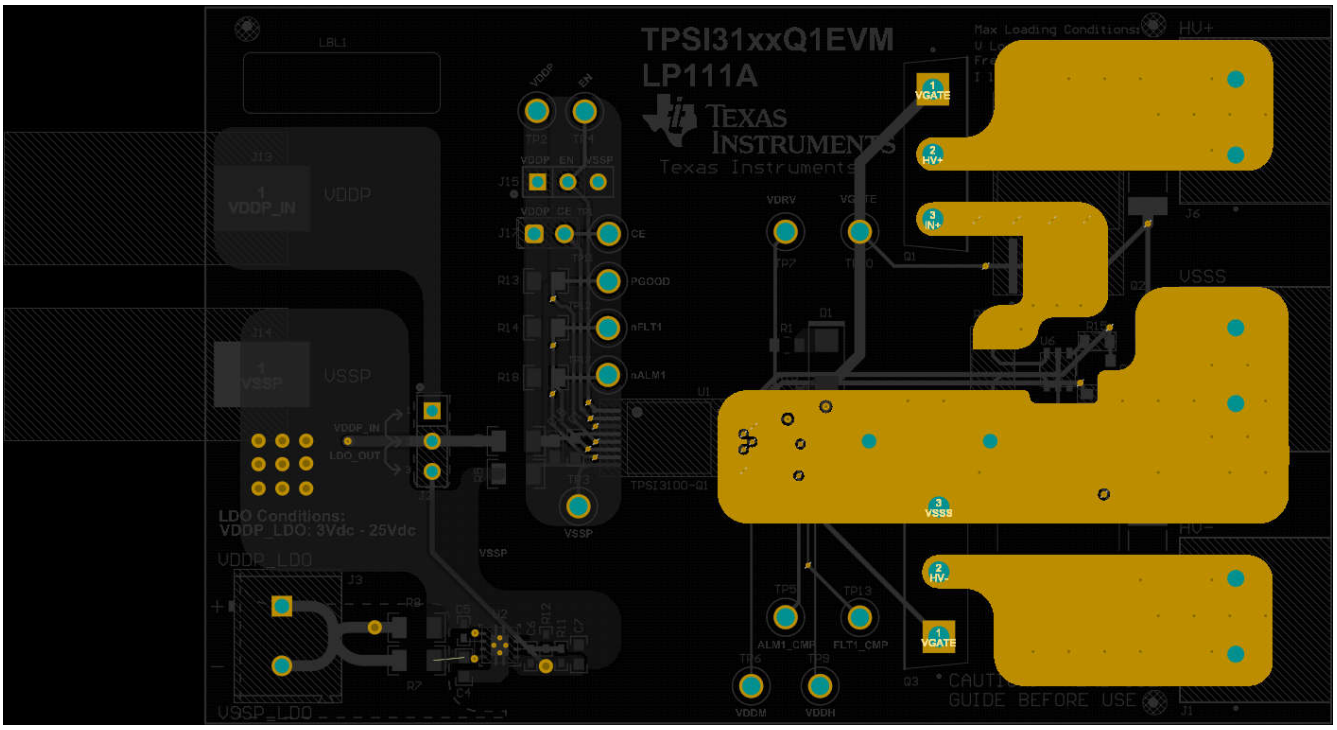


図 9-6. Signal Layer 1

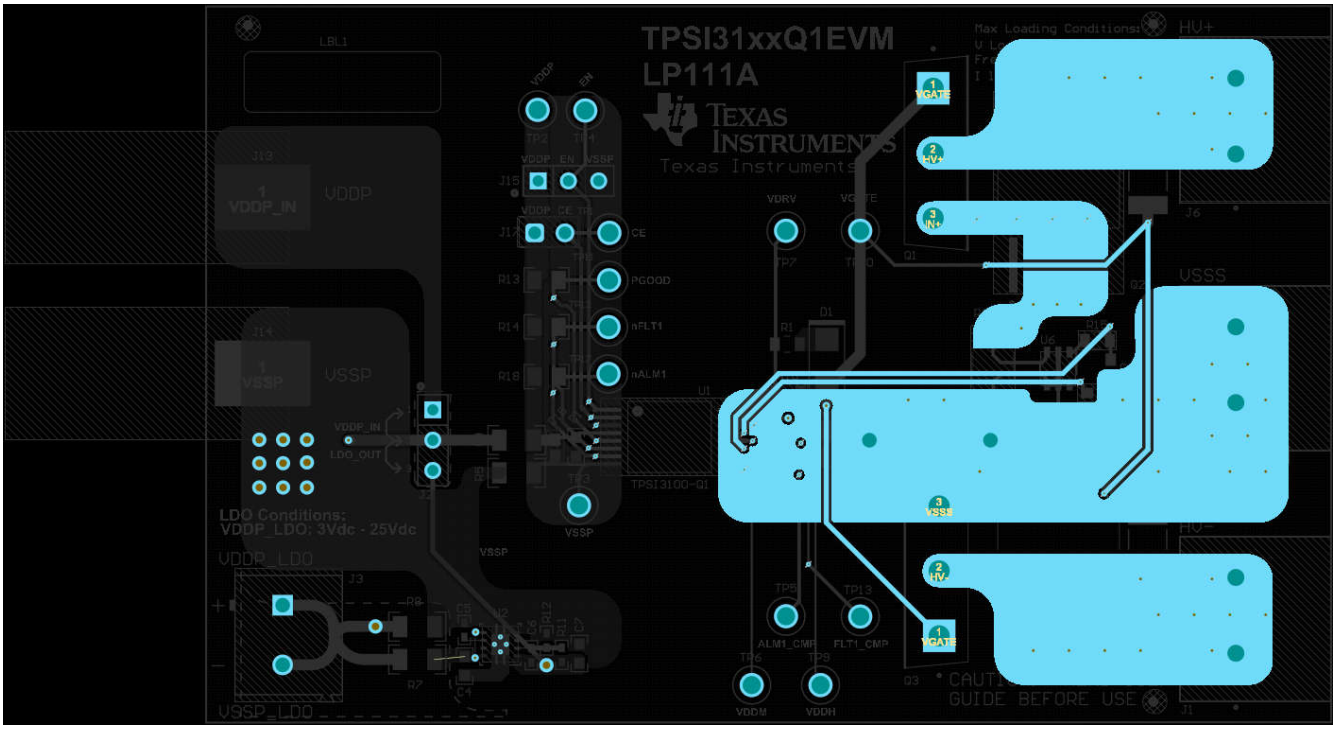


図 9-7. Signal Layer 2

ADVANCE INFORMATION

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Isolation Glossary*

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

10.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

10.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
December 2023	*	Initial Release

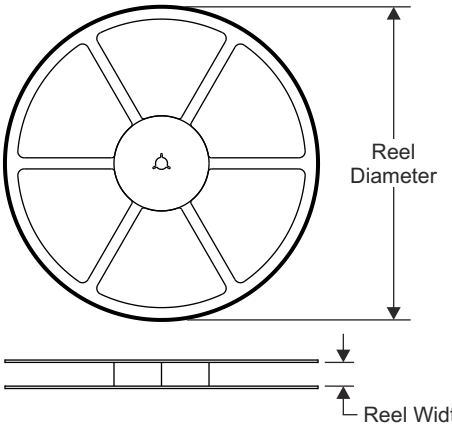
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

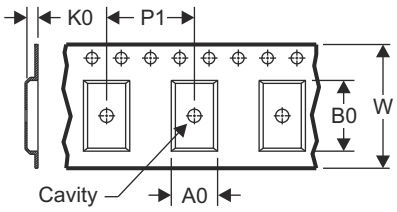
ADVANCE INFORMATION

12.1 Tape and Reel Information

REEL DIMENSIONS

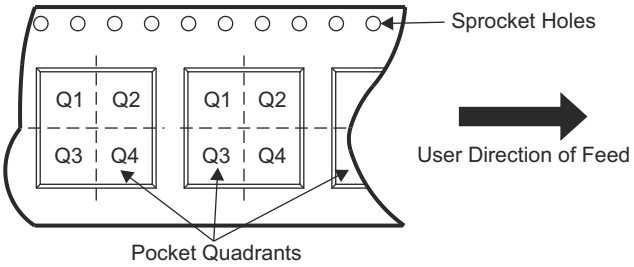


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

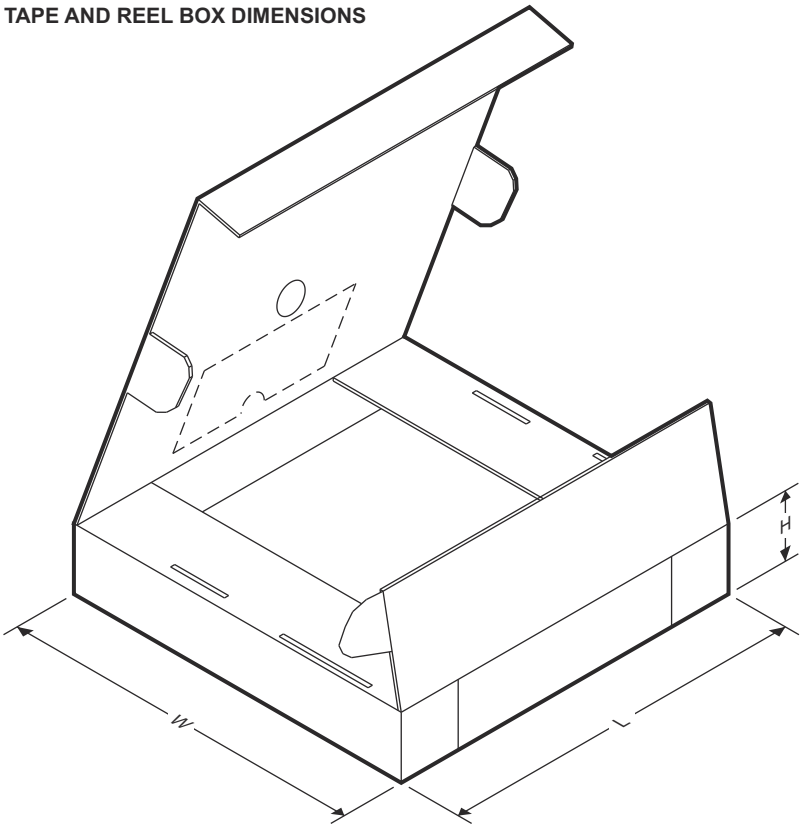


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTPSI3100QDVXRQ1	SSOP	DVX	16	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
PTPSI3100LQDVXRQ1	SSOP	DVX	16	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



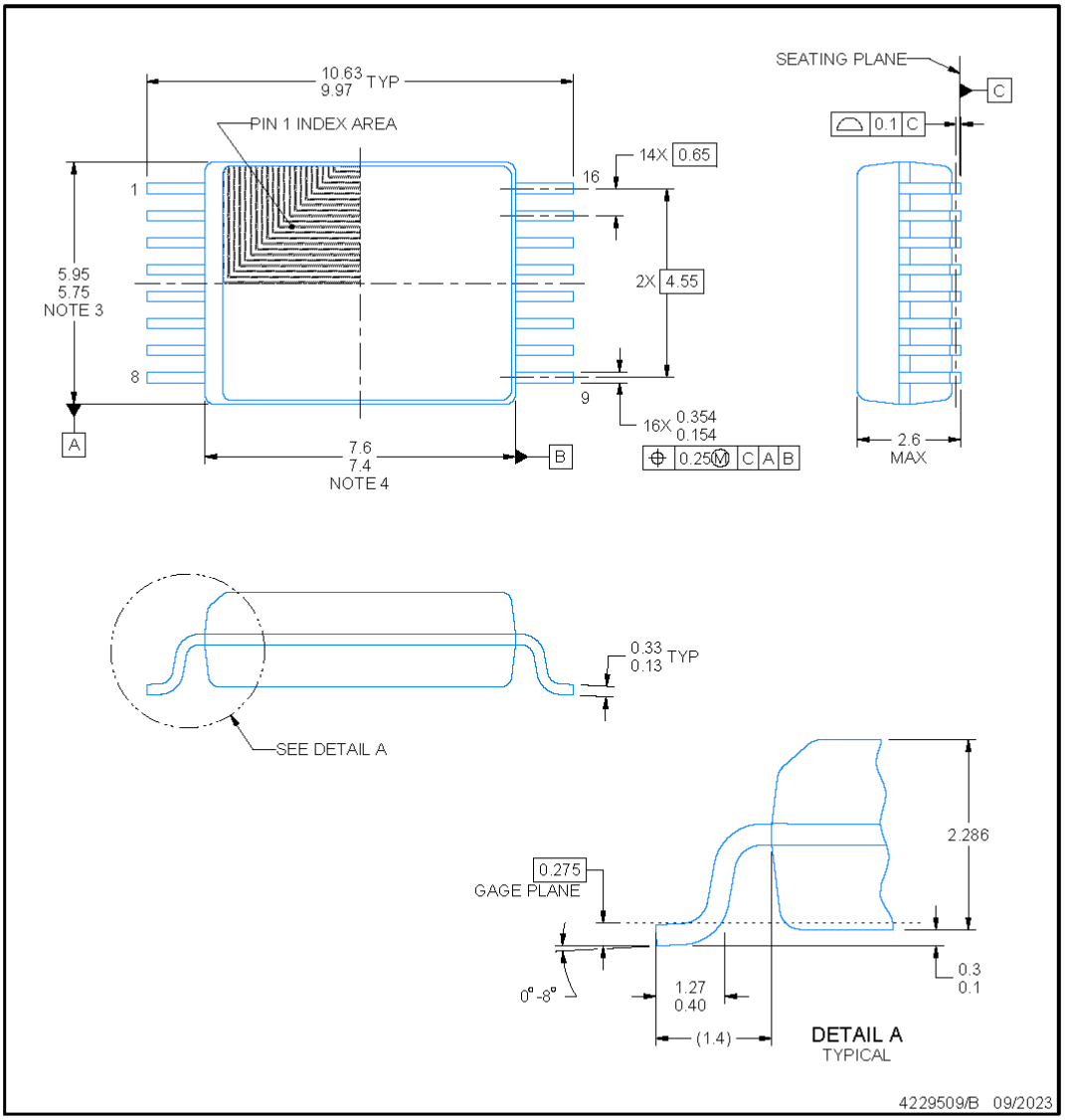
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTPSI3100QDVXRQ1	SSOP	DVX	16	1000	350.0	350.0	43.0
PTPSI3100LQDVXRQ1	SSOP	DVX	16	1000	350.0	350.0	43.0

PACKAGE OUTLINE

DVX0016A

SSOP - 2.6 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

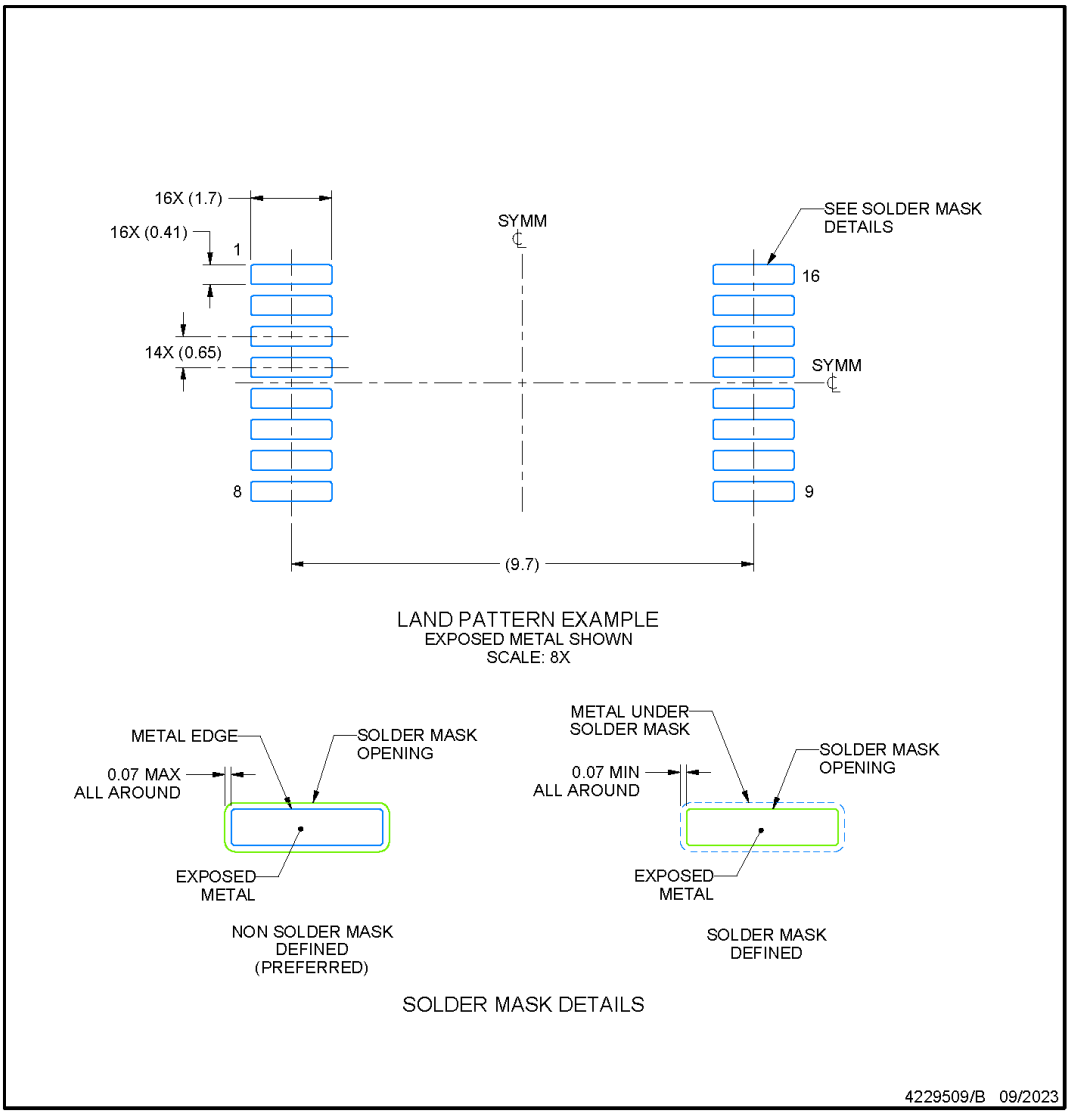
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

DVX0016A

SSOP - 2.6 mm max height

SMALL OUTLINE PACKAGE



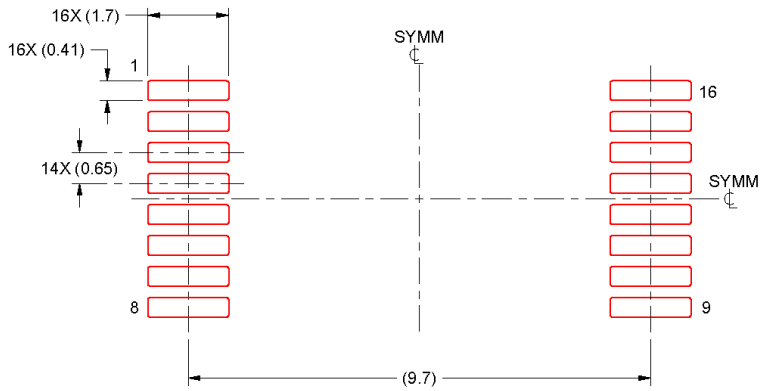
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DVX0016A — **SSOP - 2.6 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

DWG_NO:3/REV:3 MM_YYYY:3

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPSI3100LQDVXRQ1	ACTIVE	SO-MOD	DVX	16	1000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPSI3100QDVXRQ1	ACTIVE	SO-MOD	DVX	16	1000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPSI3100-Q1 :

- Catalog : TPSI3100

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

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