TEXAS INSTRUMENTS
TPSM63606
JAJSLR7B – OCTOBER 2021 – REVISED APRIL 2022

TPSM63606 高密度、3V～36V 入力、1V～16V 出力、6A 同期整流式降圧 DC/DC パワー・モジュール、Enhanced HotRod™ QFN パッケージ

1 特長

- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 用途の広い 36V_{IN}、6A_{OUT} 同期整流式降圧モジュール
  - MOSFET、インダクタ、コントローラを内蔵
  - 出力電圧を調整可能 1V～16V
  - 5.0mm × 5.5mm × 4mm のオーバーモールド・パッケージ
  - –40℃～125℃の接合部温度範囲
  - 200kHz～2.2MHz の範囲で周波数を調整可能
  - 負電圧出力に対応可能
- 全負荷範囲にわたって極めて高い効率を実現
  - 95% 以上のピーク効率
  - 外部バイアス・オプションによる効率向上
  - シャットダウン時静止電流:0.6µA (標準値)
- 非常に小さい伝導および放射 EMI シグネチャ
  - デュアル入力パスと内蔵コンデンサを備えた低ノイズ・パッケージにより、スイッチのリンギングが減少
  - スペクトラム拡散変調 (S サフィックス)
  - 抵抗により調整可能なスイッチ・ノードのスルーレート
  - CISPR 11 および 32 Class B の放射規格に準拠
- スケーラブルな電源に好適
  - TPSM63604 (36V、4A) とピン互換
- 堅牢な設計のための本質的な保護機能
  - 高精度のイネーブル入力とオープン・ドレインの PGOOD インジケータによるシーケンシング、制御、V_{IN} UVLO
  - 過電流およびサーマル・シャットダウン保護機能
- WEBENCH® Power Designer により、TPSM63606 を使用するカスタム設計を作成

2 アプリケーション

- 試験および測定、航空宇宙および防衛
- ファクトリ・オートメーション / 制御
- 降圧および反転型の昇降圧電源

3 概要

同期整流式降圧モジュール・ファミリから派生した TPSM63606 は、パワー MOSFET、シールド付きインダクタ、受動部品を Enhanced HotRod™ QFN パッケージに実装した高集積 36V、6A DC/DC ソリューションです。このモジュールは、VIN および VOUT ピンをパッケージの角に配置し、入力および出力コンデンサの配置を最適化しています。モジュールの下面には大きな 4 つのサーマル・パッドがあるため、単純なレイアウトが可能で、製造時の扱いも容易です。

出力電圧が 1V～16V であるため、TPSM63606 は小さな PCB フットプリントで低 EMI の設計を迅速かつ容易に実装できるよう設計されています。このトータル・ソリューションを使用すると、外付け部品はわずか 4 個で済み、設計プロセスで磁気および補償のための部品選択も不要です。

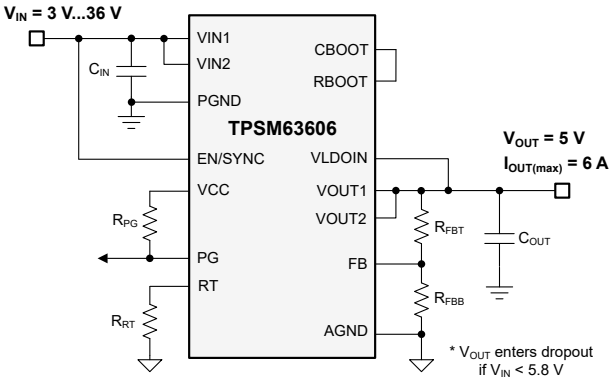
TPSM63606 モジュールは、スペースが制約される用途での小型化と簡素化をめざして設計されているだけでなく、堅牢性の高い性能を実現するためのさまざまな機能を備えています。その例としては、可変入力電圧 UVLO 用のヒステリシス付き高精度イネーブル、抵抗を使ってプログラム可能なスイッチ・ノードのスルーレートおよび拡散スペクトラム・オプションによる EMI 改善、内蔵 VCC、ブートストラップおよび入力コンデンサによる信頼性向上と高密度化、全負荷電流範囲にわたって一定のスイッチング周波数、シーケンシング、障害保護、出力電圧監視用の PGOOD インジケータがあります。

製品情報

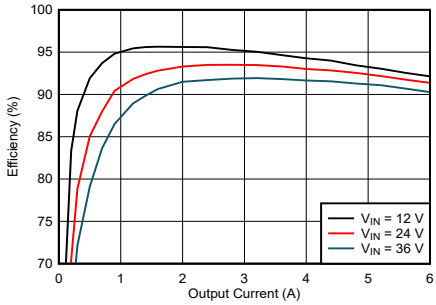
部品番号	パッケージ(1)	本体サイズ (公称)
TPSM63606	B3QFN (20)	5.0mm × 5.5mm
TPSM63606S		

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。



代表的な回路図



代表的な効率 (V_{OUT} = 5V、f_{SW} = 1MHz)

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Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Revision History ... 3
5 Device Comparison Table ... 4
6 Pin Configuration and Functions ... 4
7 Specifications ... 6
7.1 Absolute Maximum Ratings ... 6
7.2 ESD Ratings ... 6
7.3 Recommended Operating Conditions ... 7
7.4 Thermal Information ... 7
7.5 Electrical Characteristics ... 8
7.6 System Characteristics ... 10
7.7 Typical Characteristics ... 11
7.8 Typical Characteristics (V_{IN} = 12 V) ... 13
7.9 Typical Characteristics (V_{IN} = 24 V) ... 14
8 Detailed Description ... 15
8.1 Overview ... 15
8.2 Functional Block Diagram ... 15
8.3 Feature Description ... 16
8.4 Device Functional Modes ... 22
9 Applications and Implementation ... 23
9.1 Application Information ... 23
9.2 Typical Applications ... 23
10 Power Supply Recommendations ... 31
11 Layout ... 32
11.1 Layout Guidelines ... 32
11.2 Layout Example ... 33
12 Device and Documentation Support ... 35
12.1 Device Support ... 35
12.2 Documentation Support ... 36
12.3 Receiving Notification of Documentation Updates ... 36
12.4 サポート・リソース ... 36
12.5 Trademarks ... 36
12.6 Electrostatic Discharge Caution ... 36
12.7 Glossary ... 36
13 Mechanical, Packaging, and Orderable Information ... 37

4 Revision History

Changes from Revision A (December 2021) to Revision B (April 2022) — **Page**

- TPSM6360x モジュール・ファミリへのリンクを追加 ... 1
- Increased peak reflow case temperature to 250°C ... 6
- Removed reference to the external capacitor in セクション 8.3.11 ... 21
- Added module weight ... 34

Changes from Revision * (October 2021) to Revision A (December 2021) — **Page**

- ドキュメントのステータスを「事前情報」から「量産データ」に変更 ... 1

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5 Device Comparison Table

Device	Orderable Part Number	Rated Output Current	Junction Temperature Range	Spread Spectrum	Slew-Rate Control	External Sync
TPSM63602	TPSM63602RDHR	2 A	–40°C to 125°C	No	Yes	Yes
TPSM63603	TPSM63603RDHR	3 A	–40°C to 125°C	No	Yes	Yes
TPSM63603S	TPSM63603SRDHR	3 A	–40°C to 125°C	Yes	Yes	Yes
TPSM63603E	TPSM63603EXTRDHR	3 A	–55°C to 125°C	Yes	Yes	Yes
TPSM63604	TPSM63604RDLR	4 A	–40°C to 125°C	No	Yes	Yes
TPSM63606	TPSM63606RDLR	6 A	–40°C to 125°C	No	Yes	Yes
TPSM63606S	TPSM63606SRDLR	6 A	–40°C to 125°C	Yes	Yes	Yes
TPSM63606E	TPSM63606EXTRDLR	6 A	–55°C to 125°C	Yes	Yes	Yes

6 Pin Configuration and Functions

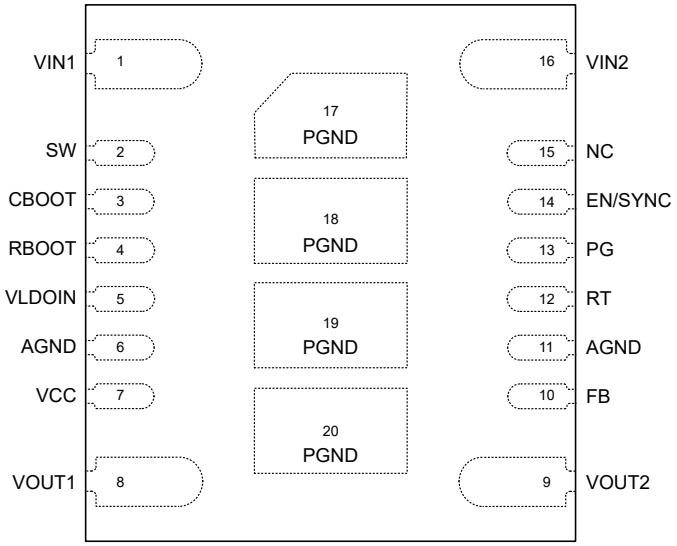

図 6-1. 20-Pin QFN RDL Package (Top View)

表 6-1. Pin Functions

Pin		Type(1)	Description
Name	NO.		
VIN1, VIN2	1, 16	P	Input supply voltage. Connect the input supply to these pins. Connect input capacitors between these pins and PGND in close proximity to the device.
SW	2	O	Switch node. Do not place any external component on this pin or connect to any signal. The amount of copper placed on this pin must be kept to a minimum to prevent issues with noise and EMI.
CBOOT	3	I/O	Bootstrap pin for the internal high-side gate driver. A 100-nF bootstrap capacitor is internally connected from this pin to SW within the module to provide the bootstrap voltage. CBOOT is brought out to use in conjunction with RBOOT to effectively lower the value of the internal series bootstrap resistance to adjust the switch-node slew rate, if necessary.
RBOOT	4	I/O	External bootstrap resistor connection. Internal to the device, a 100-Ω bootstrap resistor is connected between RBOOT and CBOOT. RBOOT is brought out to use in conjunction with CBOOT to effectively lower the value of the internal series bootstrap resistance to adjust the switch-node slew rate, if necessary.
VLDOIN	5	P	Input bias voltage. Input to the internal LDO that supplies the internal control circuits. Connect to an output voltage point to improve efficiency. Connect an optional high-quality 0.1-µF to 1-µF capacitor from this pin to ground for improved noise immunity. If the output voltage is above 12 V, connect this pin to ground.

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表 6-1. Pin Functions (continued)

Pin		Type(1)	Description
Name	NO.		
AGND	6, 11	G	Analog ground. Zero-voltage reference for internal references and logic. All electrical parameters are measured with respect to this pin. *These pins must be connected to PGND*. See セクション 11.2 for a recommended layout.
VCC	7	O	Internal LDO output. Used as a supply to the internal control circuits. Do not connect to any external loads. A 1-µF capacitor internally connects from VCC to AGND.
VOUT1, VOUT2	8, 9	P	Output voltage. These pins are connected to the internal buck inductor. Connect these pins to the output load and connect external output capacitors between these pins and PGND.
FB	10	I	Feedback input. Connect the midpoint of the feedback resistor divider to this pin. Connect the upper resistor (R_{FBT}) of the feedback divider to V_{OUT} at the desired point of regulation. Connect the lower resistor (R_{FBB}) of the feedback divider to AGND. Do not leave open or connect to ground.
RT	12	I	Frequency setting pin used to set the switching frequency between 200 kHz and 2.2 MHz by placing an external resistor from RT to AGND. Do not leave open or connect to ground.
PG	13	O	Open-drain power-good monitor output that asserts low if the FB voltage is not within the specified window thresholds. A 10-kΩ to 100-kΩ pullup resistor to a suitable voltage is required. If not used, PG can be left open or connected to GND.
EN/SYNC	14	I	Precision enable input pin. High = on, Low = off. Can be connected to VIN. Precision enable allows the pin to be used as an adjustable input voltage UVLO. It also functions as the synchronization input pin. Used to synchronize the device switching frequency to a system clock. Triggers on the rising edge of an external clock. A capacitor can be used to AC couple the synchronization signal to this pin. The module can be turned off by using an open-drain/collector device to connect this pin to AGND. Connect an external resistor divider between this pin, VIN and AGND to create an external UVLO.
NC	15	—	No connection. Tie to GND or leave open.
PGND	17, 18, 19, 20	G	Power ground. This is the return current path for the power stage of the device. Connect these pads to the input supply return, the load return, and the capacitors associated with the VIN and VOUT pins. See セクション 11.2 for a recommended layout.

(1) P = Power, G = Ground, I = Input, O = Output

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7 Specifications

7.1 Absolute Maximum Ratings

Limits apply over T_J = –40°C to 150°C (unless otherwise noted). (1)

		MIN	MAX	UNIT
Input voltage	VIN1, VIN2 to AGND, PGND	–0.3	42	V
	RBOOT to SW	–0.3	5.5	V
	CBOOT to SW	–0.3	5.5	V
	VLDOIN to AGND, PGND	–0.3	min (V_{VIN} + 0.3, 16)	V
	EN/SYNC to AGND, PGND	–0.3	42	V
	RT to AGND, PGND	–0.3	5.5	V
	FB to AGND, PGND	–0.3	16	V
	PG to AGND, PGND	0	20	V
	PGND to AGND	–1	2	V
Output voltage	VCC to AGND, PGND	–0.3	5.5	V
	SW to AGND, PGND(2)	–0.3	42	V
	VOUT1, VOUT2 to AGND, PGND	–0.3	16	V
Input current	PG		10	mA
T_J	Junction temperature	–40	150	°C
T_A	Ambient temperature	–40	125	°C
T_{stg}	Storage temperature	–55	150	°C
Peak reflow case temperature			250	°C
Maximum number of reflows allowed			3	
Mechanical vibration	MIL-STD-883D, Method 2007.2, 20 Hz to 2 kHz		20	G
Mechanical shock	MIL-STD-883D, Method 2002.3, 1 ms, 1/2 sine, mounted		500	G

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) A voltage of 2 V below PGND and 2 V above VIN can appear on this pin for ≤ 200 ns with a duty cycle of ≤ 0.01%.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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7.3 Recommended Operating Conditions

Limits apply over T_J = –40°C to 125°C (unless otherwise noted).

		MIN	NOM	MAX	UNIT
Input voltage	VIN (input voltage range after start-up)	3		36	V
Input voltage	VLDOIN			min (V_{VIN}, 12)	V
Output voltage	VOUT(1)	1		16	V
Output current	IOUT(2)	0		6	A
Frequency	F_{SW} set by RT or SYNC	200		2200	kHz
Input current	PG			2	mA
Output voltage	PG			16	V
T_J	Operating junction temperature	–40		125	°C
T_A	Operating ambient temperature	–40		105	°C

(1) Under no conditions should the output voltage be allowed to fall below zero volts.
(2) Maximum continuous DC current may be derated when operating with high switching frequency and/or high ambient temperature. Refer to the *Typical Characteristics* section for details.

7.4 Thermal Information

THERMAL METRIC(1)		TPSM63606 RDL (QFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (TPSM63606 EVM)	22.6	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	33.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter (3)	1	°C/W
ψ_{JB}	Junction-to-board characterization parameter (4)	12.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The junction-to-ambient thermal resistance, $R_{\theta JA}$, applies to devices soldered directly to a 75 mm × 75 mm four-layer PCB with 2 oz. copper and natural convection cooling. Additional airflow and PCB copper area reduces $R_{\theta JA}$.
(3) The junction-to-top board characterization parameter, ψ_{JT}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (section 6 and 7). $T_J = \psi_{JT} \times P_{DIS} + T_T$; where P_{DIS} is the power dissipated in the device and T_T is the temperature of the top of the device.
(4) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} \times P_{DIS} + T_B$; where P_{DIS} is the power dissipated in the device and T_B is the temperature of the board 1mm from the device.

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7.5 Electrical Characteristics

Limits apply over T_J = –40°C to 125°C, V_{IN} = 24 V, V_{OUT} = 3.3 V, V_{LDOIN} = 5 V, F_{SW} = 800 kHz (unless otherwise noted). Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Input operating voltage range	Needed to start up (over the I_{OUT} range)	3.95		36	V
		Once operating (over the I_{OUT} range)	3		36	V
V_{IN_HYS}	Hysteresis(1)			1		V
I_{Q_VIN}	Input operating quiescent current (non-switching)	T_A = 25°C, $V_{EN/SYNC}$ = 3.3 V, V_{FB} = 1.5 V		7		µA
I_{SDN_VIN}	VIN shutdown quiescent current	$V_{EN/SYNC}$ = 0 V, T_A = 25°C		1		µA
ENABLE						
V_{EN_RISE}	EN voltage rising threshold		1.161	1.263	1.365	V
V_{EN_FALL}	EN voltage falling threshold			0.91		V
V_{EN_HYS}	EN voltage hysteresis		0.303	0.353	0.404	V
V_{EN_WAKE}	EN wake-up threshold		0.4			V
I_{EN}	Input current into EN/SYNC (non-switching)	$V_{EN/SYNC}$ = 3.3 V, V_{FB} = 1.5 V		10		nA
t_{EN}	EN high to start of switching delay(1)			0.7		ms
VCC INTERNAL LDO						
V_{CC}	Internal LDO VCC voltage	3.4 V ≤ V_{VLDOIN} ≤ 12.5 V		3.3		V
		V_{VLDOIN} = 3.1 V, non-switching		3.1		V
V_{CC_UVLO}	VCC UVLO rising threshold	V_{VLDOIN} < 3.1 V(1)		3.6		V
		V_{IN} < 3.6 V(2)		3.6		V
$V_{CC_UVLO_HYS}$	VCC UVLO hysteresis(2)	Hysteresis below V_{CC_UVLO}		1.1		V
I_{VLDOIN}	Input current into VLDOIN pin (non-switching)(3)	$V_{EN/SYNC}$ = 3.3 V, V_{FB} = 1.5 V		25	31	µA
FEEDBACK						
V_{OUT}	Adjustable output voltage range	Over the I_{OUT} range	1		16	V
V_{FB}	Feedback voltage	T_A = 25°C, I_{OUT} = 0 A		1.0		V
V_{FB_ACC}	Feedback voltage accuracy	Over the V_{IN} range, V_{OUT} = 1 V, I_{OUT} = 0 A, F_{SW} = 200 kHz	–1%		+1%	
V_{FB}	Load regulation	T_A = 25°C, 0 A ≤ I_{OUT} ≤ 6 A		0.1%		
V_{FB}	Line regulation	T_A = 25°C, I_{OUT} = 0 A, 4 V ≤ V_{IN} ≤ 36 V		0.1%		
I_{FB}	Input current into FB	V_{FB} = 1 V		10		nA
CURRENT						
I_{OUT}	Output current	T_A = 25°C	0		6	A
I_{OCL}	Output overcurrent (DC) limit threshold			8.3		A
I_{L_HS}	High-side switch current limit	Duty cycle approaches 0%	8.3	9.3	10.3	A
I_{L_LS}	Low-side switch current limit		6.5	7.1	7.7	A
I_{L_NEG}	Negative current limit			–3		A
V_{HICCUP}	Ratio of FB voltage to in-regulation FB voltage to enter hiccup	Not during soft start		40%		
t_W	Short circuit wait time ("hiccup" time before soft start) (1)			80		ms
SOFT START						
t_{SS}	Time from first SW pulse to V_{FB} at 90%	V_{IN} ≥ 4.2 V	3.5	5	7	ms
t_{SS2}	Time from first SW pulse to release of FPWM lockout if output not in regulation(1)	V_{IN} ≥ 4.2 V	9.5	13	17	ms
POWER GOOD						
PG_{OV}	PG upper threshold – rising	% of V_{OUT} setting	105%	107%	110%	
PG_{UV}	PG lower threshold – falling	% of V_{OUT} setting	92%	94%	96.5%	
PG_{HYS}	PG threshold hysteresis (rising & falling)	% of V_{OUT} setting		1.3%		
$V_{IN_PG_VALID}$	Input voltage for valid PG output	46 µA pull-up, $V_{EN/SYNC}$ = 0 V	1.0			V
V_{PG_LOW}	PG low-level output voltage	2 mA pullup to PG pin, $V_{EN/SYNC}$ = 3.3 V			0.4	V

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Limits apply over T_J = –40°C to 125°C, V_{IN} = 24 V, V_{OUT} = 3.3 V, V_{LDOIN} = 5 V, F_{SW} = 800 kHz (unless otherwise noted). Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{PG}	Input current into PG pin when open drain output is high	V_{PG} = 3.3 V		10		nA
I_{OV}	Pulldown current at the SW node during an overvoltage condition			0.5		mA
$t_{PG_FLT_RISE}$	Delay time to PG high signal		1.5	2.0	2.5	ms
$t_{PG_FLT_FALL}$	Glitch filter time constant for PG function			120		µs
SWITCHING FREQUENCY						
f_{SW_RANGE}	Switching frequency range by RT or SYNC		200		2200	kHz
f_{SW_RT1}	Default switching frequency by R_{RT}	R_{RT} = 66.5 kΩ	180	200	220	kHz
f_{SW_RT2}	Default switching frequency by R_{RT}	R_{RT} = 5.76 kΩ	1980	2200	2420	kHz
f_{S_SS}	Frequency span of spread spectrum operation – largest deviation from center frequency	Spread spectrum active (TPSM63606S)		2%		
f_{PSS}	Spread spectrum pattern frequency(1)	Spread spectrum active, f_{SW} = 2.1 MHz			1.5	Hz
SYNCHRONIZATION						
V_{EN_SYNC}	Minimum edge amplitude to sync using EN/SYNC	Rise/fall time < 30 ns			2.4	V
t_B	Blanking of EN after rising or falling edges(1)		4		28	µs
t_{SYNC_EDGE}	EN/SYNC signal hold time after edge for edge recognition(1)		100			ns
POWER STAGE						
V_{BOOT_UVLO}	Voltage on CBOOT pin relative to SW that turns off the high-side switch			2.1		V
$t_{ON(min)}$	Minimum ON pulse width(1)	V_{OUT} = 1 V, I_{OUT} = 1 A, RBOOT shorted to CBOOT		55	70	ns
$t_{ON(max)}$	Maximum ON pulse width(1)			9		µs
$t_{OFF(min)}$	Minimum OFF pulse width	V_{IN} = 4 V, I_{OUT} = 1 A, RBOOT shorted to CBOOT		65	85	ns
THERMAL SHUTDOWN						
T_{SHD}	Thermal shutdown threshold (1)	Temperature rising	158	168	180	°C
$T_{SHD-HYS}$	Thermal shutdown hysteresis (1)			10		°C

(1) Parameter specified by design, statistical analysis and production testing of correlated parameters. Not production tested.
(2) Production tested with V_{IN} = 3 V.
(3) This is the current used by the device while not switching, open loop, with FB pulled to +5% of nominal. It does not represent the total input current to the system while regulating.

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7.6 System Characteristics

The following specifications apply only to the typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C only. These specifications are not ensured by production testing.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_{IN}	Input supply current when in regulation	V_{IN} = $V_{EN/SYNC}$ = 24 V, V_{OUT} = V_{VLDOIN} = 3.3 V, F_{SW} = 750 kHz, I_{OUT} = 0 A		15		mA
OUTPUT VOLTAGE						
ΔV_{OUT1}	Load regulation	V_{IN} = 24 V, V_{OUT} = 3.3 V, I_{OUT} = 0.1 A to 6 A		1		mV
ΔV_{OUT2}	Line regulation	V_{IN} = 4 V to 36 V, V_{OUT} = 3.3 V, I_{OUT} = 6 A		1		mV
ΔV_{OUT3}	Load transient	V_{IN} = 24 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A to 4 A at 1 A/µs, $C_{OUT(derated)}$ = 50 µF		100		mV
EFFICIENCY						
η	Efficiency	V_{IN} = 12 V, V_{OUT} = V_{VLDOIN} = 3.3 V, I_{OUT} = 5 A, F_{SW} = 750 kHz		91%		
		V_{IN} = 24 V, V_{OUT} = V_{VLDOIN} = 3.3 V, I_{OUT} = 5 A, F_{SW} = 750 kHz		90%		
		V_{IN} = 12 V, V_{OUT} = V_{VLDOIN} = 5 V, I_{OUT} = 5 A, F_{SW} = 1 MHz		93.2%		
		V_{IN} = 24 V, V_{OUT} = V_{VLDOIN} = 5 V, I_{OUT} = 5 A, F_{SW} = 1 MHz		92.2%		
		V_{IN} = 24 V, V_{OUT} = V_{VLDOIN} = 12 V, I_{OUT} = 4 A, F_{SW} = 2 MHz		95.6%		

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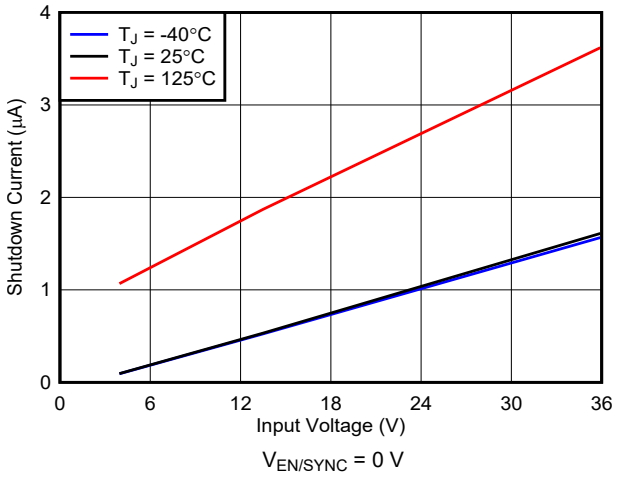
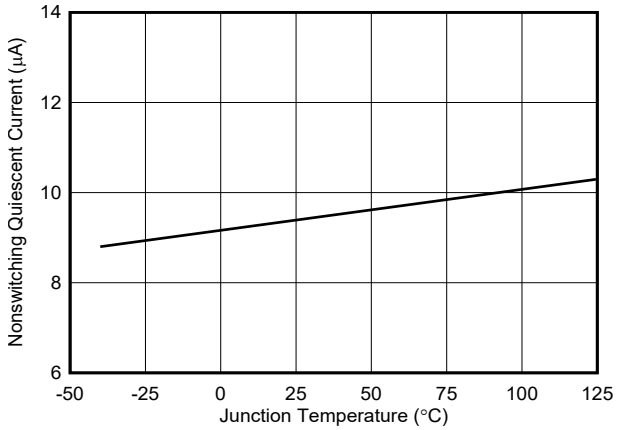
7.7 Typical Characteristics

V_{IN} = 24 V, unless otherwise specified



$V_{EN/SYNC}$ = 0 V

図 7-1. Shutdown Supply Current



V_{LDOIN} = 5 V

図 7-2. Nonswitching Input Supply Current

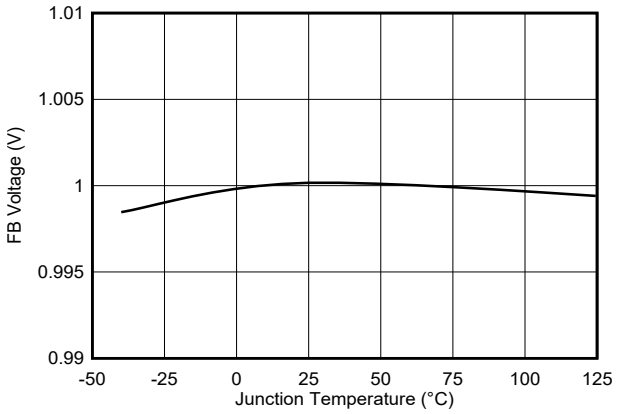


図 7-3. Feedback Voltage

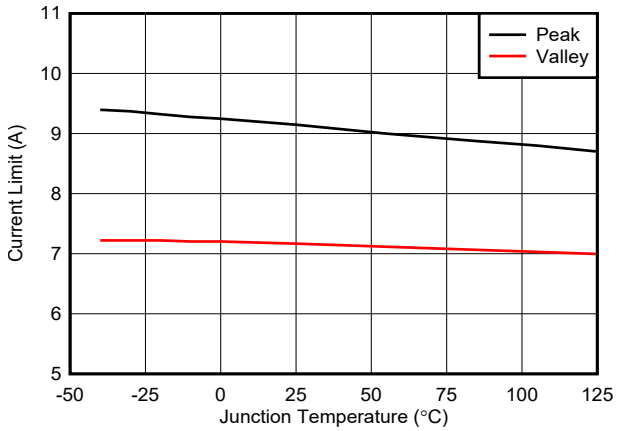


図 7-4. High-Side (Peak) and Low-Side (Valley) Current Limits

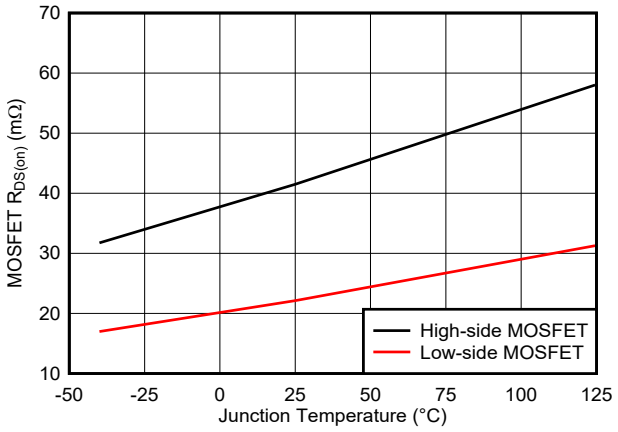


図 7-5. High-Side and Low-Side MOSFET $R_{DS(on)}$

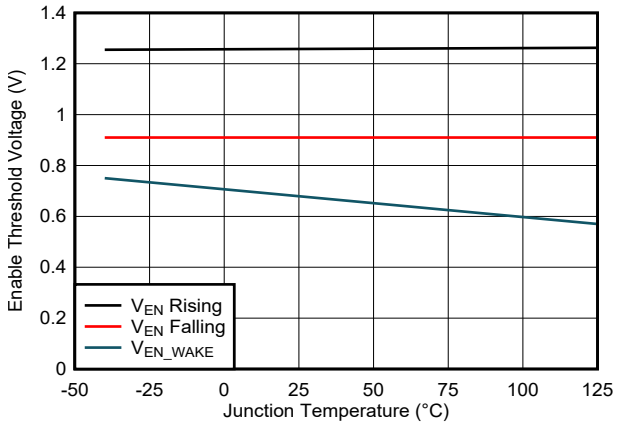


図 7-6. Enable Thresholds

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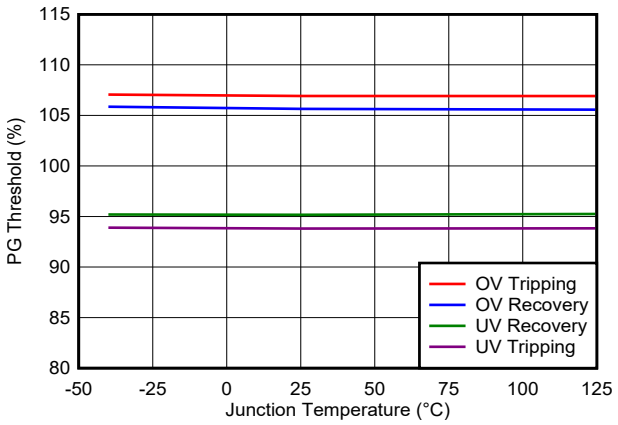

図 7-7. Power Good (PG) Thresholds

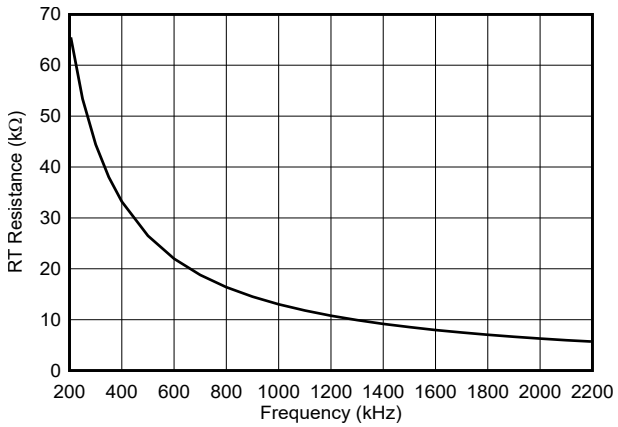

図 7-8. Switching Frequency Set by RT Resistor

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7.8 Typical Characteristics (V_{IN} = 12 V)

Unless otherwise indicated, T_A = 25°C, VLDOIN is tied to VOUT (except for V_{OUT} = 2.5 V), and the module is soldered to a 76-mm × 63-mm, 4-layer PCB. The SOA curves are taken with $T_{J(max)}$ = 125°C and $T_{A(max)}$ = 105°C. Refer to セクション 9.2 for circuit designs.

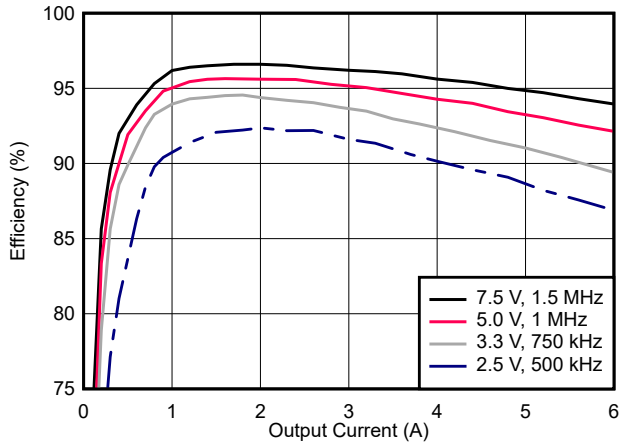

図 7-9. Efficiency

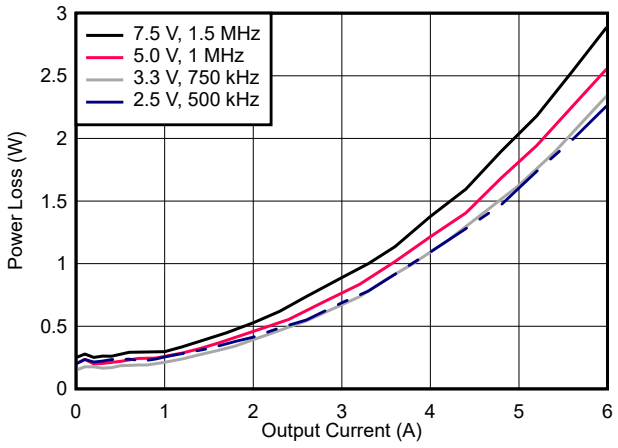

図 7-10. Power Dissipation

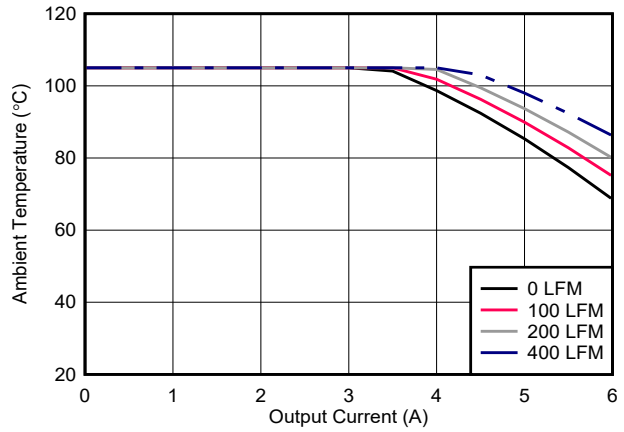

図 7-11. Safe Operating Area
(V_{OUT} = 2.5 V, F_{SW} = 500 kHz)

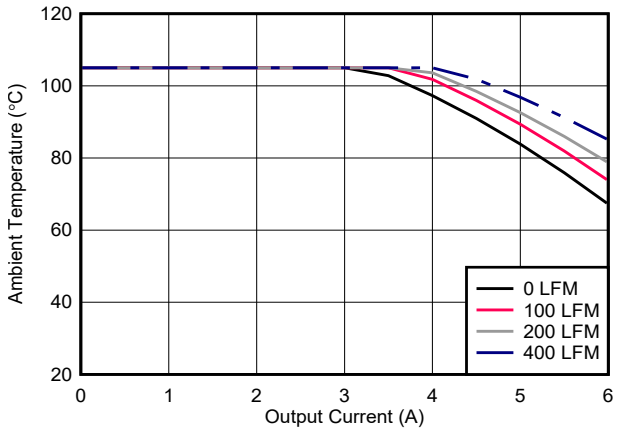

図 7-12. Safe Operating Area
(V_{OUT} = 3.3 V, F_{SW} = 750 kHz)

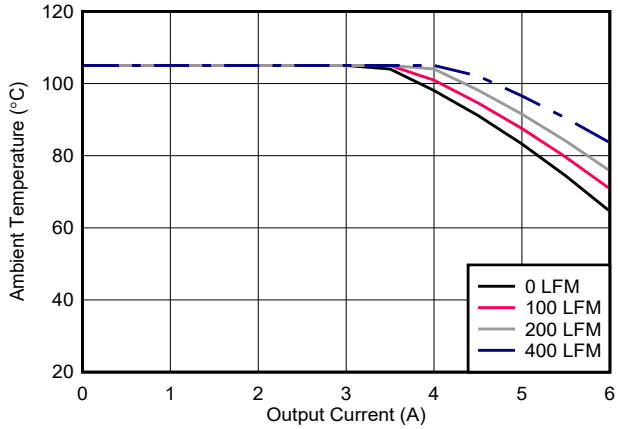

図 7-13. Safe Operating Area
(V_{OUT} = 5 V, F_{SW} = 1 MHz)

7.9 Typical Characteristics (V_{IN} = 24 V)

Unless otherwise indicated, T_A = 25°C, VLDOIN is tied to VOUT (except for V_{OUT} = 2.5 V), and the module is soldered to a 76-mm × 63-mm, 4-layer PCB. The SOA curves are taken with $T_{J(max)}$ = 125°C and $T_{A(max)}$ = 105°C. Refer to セクション 9.2 for circuit designs.

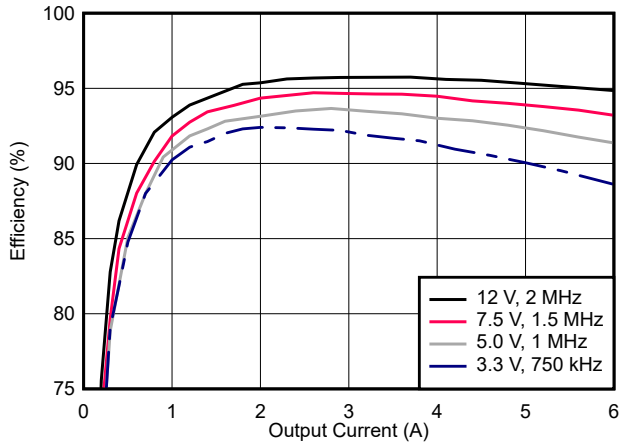

図 7-14. Efficiency

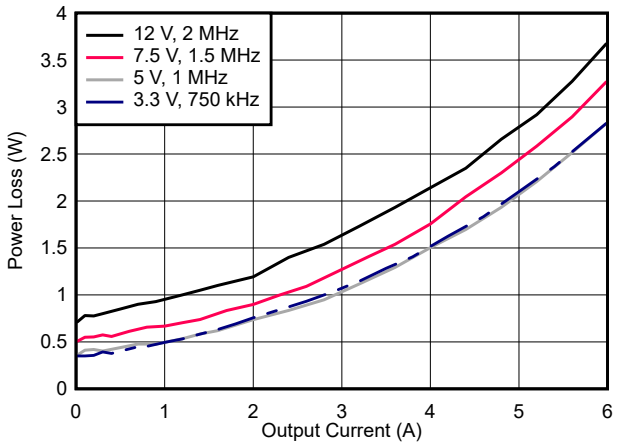

図 7-15. Power Dissipation

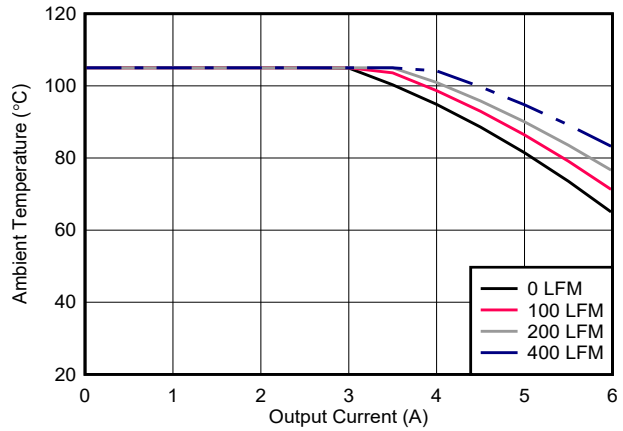

図 7-16. Safe Operating Area
(V_{OUT} = 2.5 V, F_{SW} = 500 kHz)

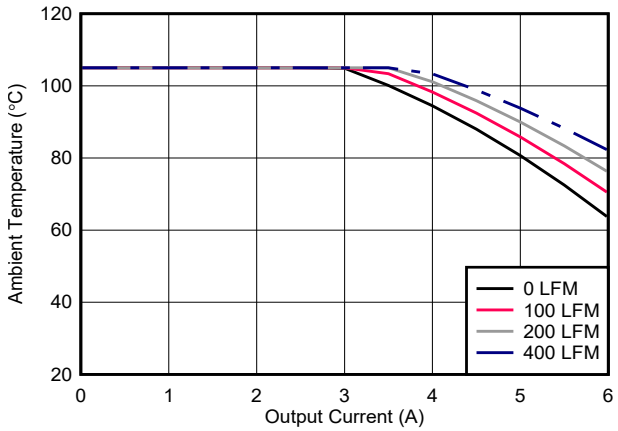

図 7-17. Safe Operating Area
(V_{OUT} = 3.3 V, F_{SW} = 750 kHz)

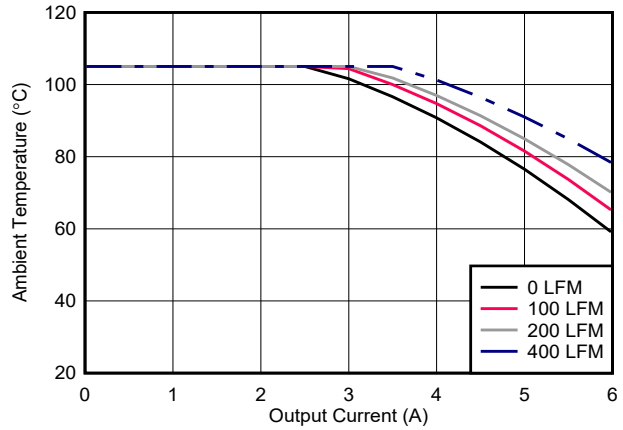

図 7-18. Safe Operating Area
(V_{OUT} = 5 V, F_{SW} = 1 MHz)

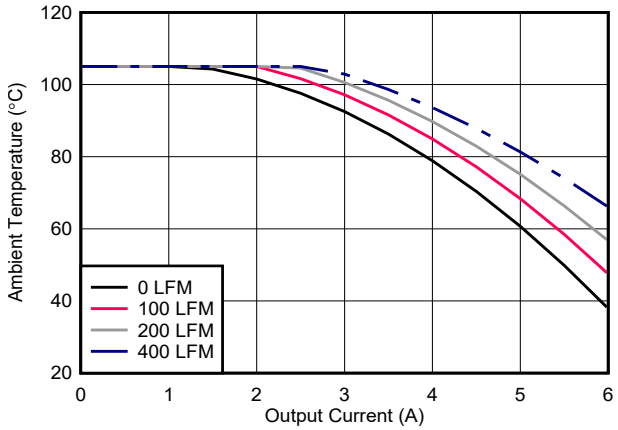

図 7-19. Safe Operating Area
(V_{OUT} = 12 V, F_{SW} = 2 MHz)

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8 Detailed Description

8.1 Overview

The TPSM63606 is an easy-to-use, synchronous buck DC/DC power module designed for a wide variety of applications where reliability, small solution size, and low EMI signature are of paramount importance. With integrated power MOSFETs, a buck inductor, and PWM controller, the TPSM63606 operates over an input voltage range of 3 V to 36 V with transients as high as 42 V. The module delivers up to 6-A DC load current with high conversion efficiency and ultra-low input quiescent current in a very small solution footprint. Control loop compensation is not required, reducing design time and external component count.

With a programmable switching frequency from 200 kHz to 2.2 MHz using its RT pin or an external clock signal, the TPSM63606 incorporates specific features to improve EMI performance in noise-sensitive applications:

- An optimized package and pinout design enables a shielded switch-node layout that mitigates radiated EMI.
- Parallel input and output paths with symmetrical capacitor layouts minimize parasitic inductance, switch-voltage ringing, and radiated field coupling
- Pseudo-random spread spectrum (PRSS) modulation in the TPSM63606S reduces peak emissions
- Clock synchronization and FPWM mode enable constant switching frequency across the load current range.
- Integrated power MOSFETs with enhanced gate drive control enable low-noise PWM switching.

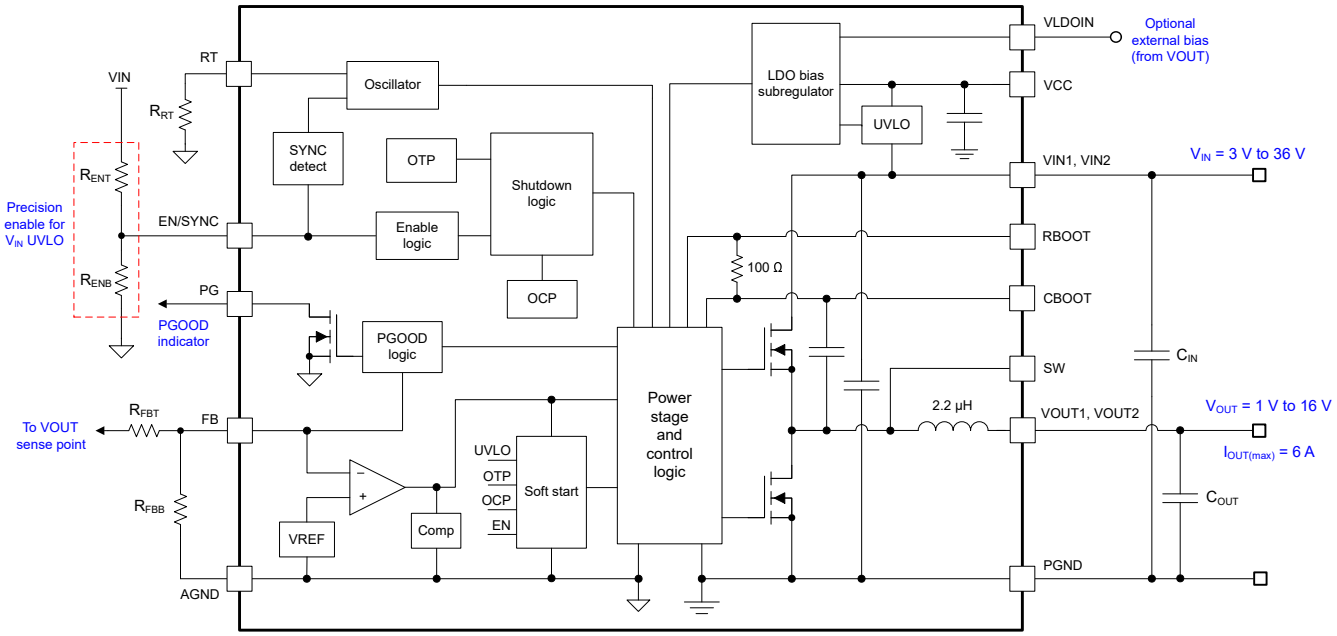
Together, these features significantly reduce EMI filtering requirements, while helping to meet CISPR 11 and CISPR 32 Class B EMI limits for conducted and radiated emissions.

The TPSM63606 module also includes inherent protection features for robust system requirements:

- An open-drain PGOOD indicator for power-rail sequencing and fault reporting
- Precision enable input with hysteresis, providing:
  - Programmable line undervoltage lockout (UVLO)
  - Remote ON/OFF capability
- Internally fixed output-voltage soft start with monotonic start-up into prebiased loads
- Hiccup-mode overcurrent protection with cycle-by-cycle peak and valley current limits
- Thermal shutdown with automatic recovery.

Leveraging a pin arrangement designed for simple layout that requires only a few external components, the TPSM63606 is specified to maximum ambient and junction temperatures of 105°C and 125°C, respectively.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Voltage Range (VIN1, VIN2)

With a steady-state input voltage range from 3 V to 36 V, the TPSM63606 module is intended for step-down conversions from typical 12-V, 24-V, and 28-V input supply rails. The schematic circuit in 図 8-1 shows all the necessary components to implement a TPSM63606-based buck regulator using a single input supply.

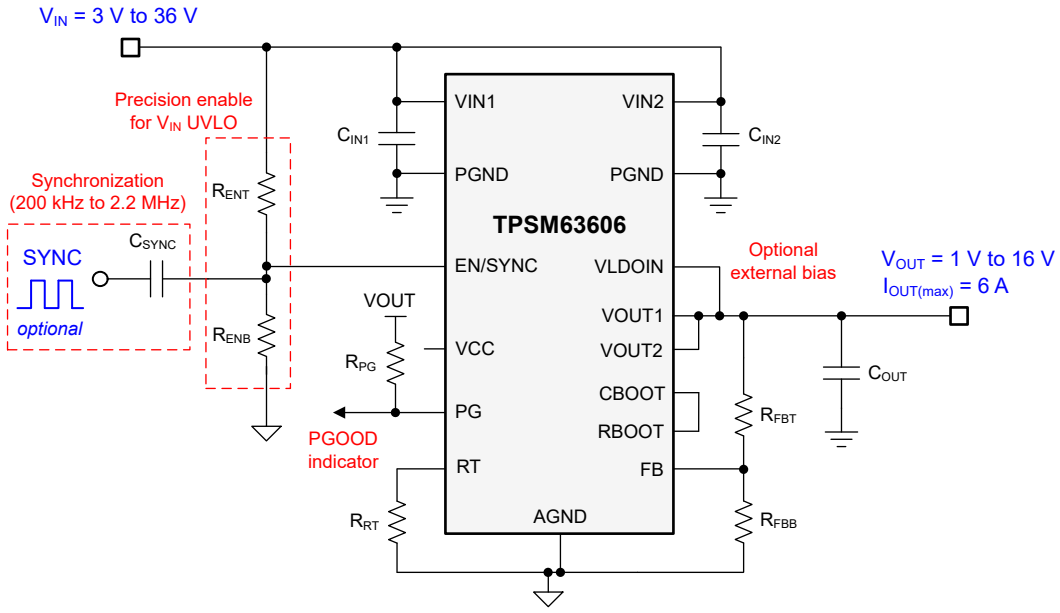


図 8-1. TPSM63606 Schematic Diagram with Input Voltage Operating Range of 3 V to 36 V

The minimum input voltage required for start-up is 3.95 V. Take extra care to make sure that the voltage at the VIN pins of the module (VIN1 and VIN2) does not exceed the absolute maximum voltage rating of 42 V during line or load transient events. Voltage ringing at the VIN pins that exceeds the absolute maximum ratings can damage the IC.

8.3.2 Adjustable Output Voltage (FB)

The TPSM63606 has an adjustable output voltage range from 1 V up to a maximum of 16 V or slightly less than V_{IN}, whichever is lower. Setting the output voltage requires two feedback resistors, designated as R_{FBT} and R_{FBB} in 図 8-1. The reference voltage at the FB pin is set at 1 V with a feedback system accuracy over the full junction temperature range of ±1%. The junction temperature range for the device is –40°C to 125°C.

Calculate the value for R_{FBT} using 式 1 based on a recommended value for R_{FBB} of 10 kΩ.

$$R_{FBT}\left[k\Omega\right] = R_{FBB}\left[k\Omega\right] \cdot \left(\frac{V_{OUT}\left[V\right]}{1V} - 1 \right) \tag{1}$$

表 8-1 lists the standard resistor values for several output voltages and the recommended switching frequency range to maintain reasonable peak-to-peak inductor ripple current. This table also includes the minimum required output capacitance for each output voltage setting to maintain stability. The capacitances as listed represent *effective* values for ceramic capacitors derated for DC bias voltage and temperature. Furthermore, place a feedforward capacitor, C_{FF}, in parallel with R_{FBT} to increase the phase margin when the output capacitance is close to the minimum recommended value.

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表 8-1. Standard R_{FBT} Values, Recommended F_{SW} Range and Minimum C_{OUT}

V_{OUT} (V)	R_{FBT} (kΩ) (1)	Suggested F_{SW} Range (kHz)	$C_{OUT(min)}$ (µF) (Effective)	C_{FF} (pF)		V_{OUT} (V)	R_{FBT} (kΩ) (1)	Suggested F_{SW} Range (MHz)	$C_{OUT(min)}$ (µF) (Effective)	C_{FF} (pF)
1	Short	300 to 500	300	—		5	40.2	0.8 to 1.2	30	22
1.2	2	400 to 600	200	—		7.5	64.9	1.2 to 1.6	25	15
1.8	8.06	500 to 700	120	100		10	90.9	1.6 to 2.0	18	—
2.5	15	650 to 900	70	68		12	110	1.7 to 2.2	12	—
3.3	23.2	700 to 950	50	47		15	140	1.8 to 2.2	10	—

(1) R_{FBB} = 10 kΩ

Note that higher feedback resistances consume less DC current. However, an upper R_{FBT} resistor value higher than 1 MΩ renders the feedback path more susceptible to noise. Higher feedback resistances generally require more careful layout of the feedback path. It is important to locate the feedback resistors close to the FB and AGND pins, keeping the feedback trace as short as possible (and away from noisy areas of the PCB). See セクション 11.2 guidelines for more detail.

8.3.3 Input Capacitors

Input capacitors are necessary to limit the input ripple voltage to the module due to switching frequency AC currents. TI recommends using ceramic capacitors to provide low impedance and high RMS current rating over a wide temperature range. 式 2 gives the input capacitor RMS current. The highest input capacitor RMS current occurs at D = 0.5, at which point, the RMS current rating of the capacitors should be greater than half the output current.

$$I_{CIN,rms} = \sqrt{D \cdot \left({I_{OUT}}^2 \cdot (1-D) + \frac{\Delta I_L^2}{12} \right)} \tag{2}$$

where

- $D = V_{OUT} / V_{IN}$ is the module duty cycle.

Ideally, the DC and AC components of input current to the buck stage are provided by the input voltage source and the input capacitors, respectively. Neglecting inductor ripple current, the input capacitors source current of amplitude ($I_{OUT} – I_{IN}$) during the D interval and sink I_{IN} during the 1 – D interval. Thus, the input capacitors conduct a square-wave current of peak-to-peak amplitude equal to the output current. The resultant capacitive component of AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, 式 3 gives the peak-to-peak ripple voltage amplitude:

$$\Delta V_{IN} = \frac{I_{OUT} \cdot D \cdot (1-D)}{F_{SW} \cdot C_{IN}} + I_{OUT} \cdot R_{ESR} \tag{3}$$

式 4 gives the input capacitance required for a particular load current:

$$C_{IN} \geq \frac{D \cdot (1-D) \cdot I_{OUT}}{F_{SW} \cdot (\Delta V_{IN} - R_{ESR} \cdot I_{OUT})} \tag{4}$$

where

- ΔV_{IN} is the input voltage ripple specification.

The TPSM63606 requires a minimum of two 10-µF ceramic input capacitors, preferably with X7R or X7S dielectric and in 1206 or 1210 footprint. Additional capacitance can be required for applications to meet conducted EMI specifications, such as CISPR 11 or CISPR 32.

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表 8-2 includes a preferred list of capacitors by vendor. To minimize the parasitic inductance in the switching loops, position the ceramic input capacitors in a symmetrical layout close to the VIN1 and VIN2 pins and connect the capacitor return terminals to the PGND pins using a copper ground plane under the module.

表 8-2. Recommended Ceramic Input Capacitors

Vendor(1)	Dielectric	Part Number	Case Size	Capacitance (µF)(2)	Rated Voltage (V)
TDK	X7R	C3216X7R1H106K160AC	1206	10	50
Murata	X7S	GCM32EC71H106KA03K	1210	10	50
AVX	X7R	12105C106MAT2A	1210	10	50
Murata	X7R	GRM32ER71H106KA12L	1210	10	50

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table. See the *Third-Party Products Disclaimer*.
(2) Nameplate capacitance values (the effective values are lower based on the applied DC voltage and temperature).

As discussed in セクション 10, an electrolytic bulk capacitance (68 µF to 100 µF) provides low-frequency filtering and parallel damping to mitigate the effects of input parasitic inductance resonating with the low-ESR, high-Q ceramic input capacitors.

8.3.4 Output Capacitors

表 8-1 lists the TPSM63606 minimum amount of required output capacitance. The effects of DC bias and temperature variation must be considered when using ceramic capacitance. For ceramic capacitors in particular, the package size, voltage rating, and dielectric material contribute to differences between the standard rated value and the actual effective value of the capacitance.

When including additional capacitance above $C_{OUT(min)}$, the capacitance can be ceramic type, low-ESR polymer type, or a combination of the two. See 表 8-3 for a preferred list of output capacitors by vendor.

表 8-3. Recommended Ceramic Output Capacitors

Vendor(1)	Dielectric	Part Number	Case Size	Capacitance (µF)(2)	Voltage (V)
Murata	X7R	GRM31CZ71C226ME15L	1206	22	16
TDK	X7R	C3225X7R1C226M250AC	1210	22	16
Murata	X7R	GRM32ER71C226KEA8K	1210	22	16
TDK	X6S	C3216X6S1E226M160AC	1206	22	25
AVX	X7R	12103C226KAT4A	1210	22	25
Murata	X7R	GRM32ER71E226ME15L	1210	22	25
AVX	X7R	1210ZC476MAT2A	1210	47	10
Murata	X7R	GRM32ER71A476ME15L	1210	47	10
Murata	X6S	GRM32EC81C476ME15L	1210	47	16
TDK	X6S	C3216X6S0G107M160AC	1206	100	4
Murata	X6T	GRM31CD80J107MEA8L	1206	100	6.3
Murata	X7S	GRM32EC70J107ME15L	1210	100	6.3

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in the table. See the *Third-Party Products Disclaimer*.
(2) Nameplate capacitance values (the effective values are lower based on the applied DC voltage and temperature)

8.3.5 Switching Frequency (RT)

Connect a resistor, designated as R_{RT} in 図 8-1, between RT and AGND to set the swiching frequency within the range of 200 kHz to 2.2 MHz. Use 式 5 or refer to 図 7-8 to calculate R_{RT} for a desired frequency.

$$R_{RT}\left[k\Omega\right] = \frac{13.46}{F_{SW}\left[MHz\right]} - 0.44 \tag{5}$$

Refer to 表 8-1 or use the simplified expression in 式 6 to find a switching frequency that sets an inductor ripple current of 25% to 40% of the 6-A module current rating at nominal input voltage:

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$$F_{SW}\left[MHz\right] \simeq 0.25 \cdot V_{OUT}\left[V\right] \cdot \left(1 - V_{OUT}\left[V\right] / V_{IN(nom)}\left[V\right]\right) \quad (6)$$

where

- $V_{IN(nom)}$ and V_{OUT} are the nominal input voltage (typically 12 V or 24 V) and output voltage of the application, respectively.

Note that a resistor value outside of the recommended range can cause the module to shut down. This prevents unintended operation if the RT pin is shorted to ground or left open. Do not apply a pulsed signal to this pin to force synchronization. Refer to セクション 8.3.7 if clock synchronization is required.

8.3.6 Precision Enable and Input Voltage UVLO (EN/SYNC)

The EN/SYNC pin provides precision ON and OFF control for the TPSM63606. Once the EN/SYNC pin voltage exceeds the rising threshold and V_{IN} is above its minimum turn-on threshold, the device starts operation. The simplest way to enable the TPSM63606 is to connect EN/SYNC directly to VIN. This allows the TPSM63606 to start up when V_{IN} is within its valid operating range. However, many applications benefit from the use of an enable divider network as shown in 図 8-1, which establishes a precision input undervoltage lockout (UVLO). This can be used for sequencing, to prevent re-triggering the device when used with long input cables, or to reduce the occurrence of deep discharge of a battery power source. An external logic signal can also be used to drive the enable input to toggle the output on and off and for system sequencing or protection.

Calculate R_{ENB} using 式 7:

$$R_{ENB}\left[k\Omega\right] = R_{ENT}\left[k\Omega\right] \cdot \left(\frac{V_{EN_RISE}\left[V\right]}{V_{IN(on)}\left[V\right] - V_{EN_RISE}\left[V\right]} \right) \quad (7)$$

where

- A typical value for R_{ENT} is 100 kΩ.
- V_{EN_RISE} is enable rising threshold voltage of 1.263 V (typical).
- $V_{IN(on)}$ is the desired start-up input voltage.

Note

The EN/SYNC pin can also be used as an external clock synchronization input. See セクション 8.3.7 for additonal information. A blanking time of 4 µs to 28 µs is applied to the enable logic after a clock edge is detected. To effectively disable the output, the EN/SYNC input must stay low for longer than 28 µs. Any logic change within the blanking time is ignored. A blanking time is not applied when the device is in shutdown mode.

8.3.7 Frequency Synchronization (EN/SYNC)

Synchronize the internal oscillator of the TPSM63606 by AC coupling a positive clock edge to EN/SYNC, as shown in 図 8-1. The synchronization frequency range is 200 kHz to 2.2 MHz.

It is recommended to keep the parallel combination value of R_{ENT} and R_{ENB} in the 100-kΩ range. R_{ENT} is required for synchronization, but R_{ENB} can be left open. The external clock must be off before start-up to allow proper start-up sequencing. After a valid synchronization signal is applied for 2048 cycles, the clock frequency changes to that of the applied signal.

Referring to 図 8-2, the AC-coupled voltage edge at the EN/SYNC pin must exceed the SYNC amplitude threshold, V_{EN_SYNC}, of 2.4 V to trip the internal synchronization pulse detector. In addition, the minimum EN/SYNC rising and falling pulse durations must be longer than the SYNC signal hold time, t_{SYNC_EDGE}, of 100 ns and shorter than the minimum blanking time, t_B. Use a 3.3-V or higher amplitude pulse signal coupled through a 1-nF capacitor, designated as C_{SYNC} in 図 8-1.

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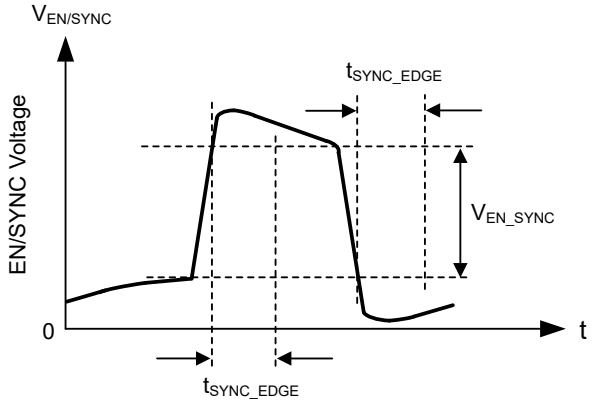

図 8-2. Typical SYNC Waveform

8.3.8 Spread Spectrum

The TPSM63606S includes pseudo-random spread spectrum (PRSS) modulation that provides a ±2% spread of the switching frequency and its harmonics. PRSS spreads the switching energy smoothly across higher-frequency bands, improving both conducted and radiated EMI performance, but is low enough to limit unwanted subharmonic emissions below the switching frequency.

The TPSM63606S uses a cycle-to-cycle frequency hopping method based on a linear feedback shift register (LFSR). This intelligent pseudo-random generator limits cycle-to-cycle frequency changes to optimize output ripple. The pseudo-random pattern repeats at less than 1.5 Hz, which is below the audio band. Spread spectrum is disabled when the module is synchronized to an external clock or when the switching frequency decreases to maintain regulation when operating in or close to dropout.

8.3.9 Power Good Monitor (PG)

The TPSM63606 provides a power-good status signal to indicate when the output voltage is within a regulation window of 94% to 107%. The PG voltage goes low when the feedback (FB) voltage is outside of the specified PGOOD thresholds (see 図 7-7). This can occur during current limit and thermal shutdown, as well as when disabled and during start-up.

PG is an open-drain output, requiring an external pullup resistor to a DC supply, such as VCC or V_{OUT}. To limit current supplied by VCC, the recommended range of pullup resistance is 20 kΩ to 100 kΩ. A 120-µs deglitch filter prevents false flag operation for short excursions of the output voltage, such as during line and load transients. When EN/SYNC is pulled low, PG is forced low and remains remains valid as long as the input voltage is above 1 V (typical). Use the PG signal for start-up sequencing of downstream regulators, as shown in 図 8-3, or for fault protection and output monitoring.

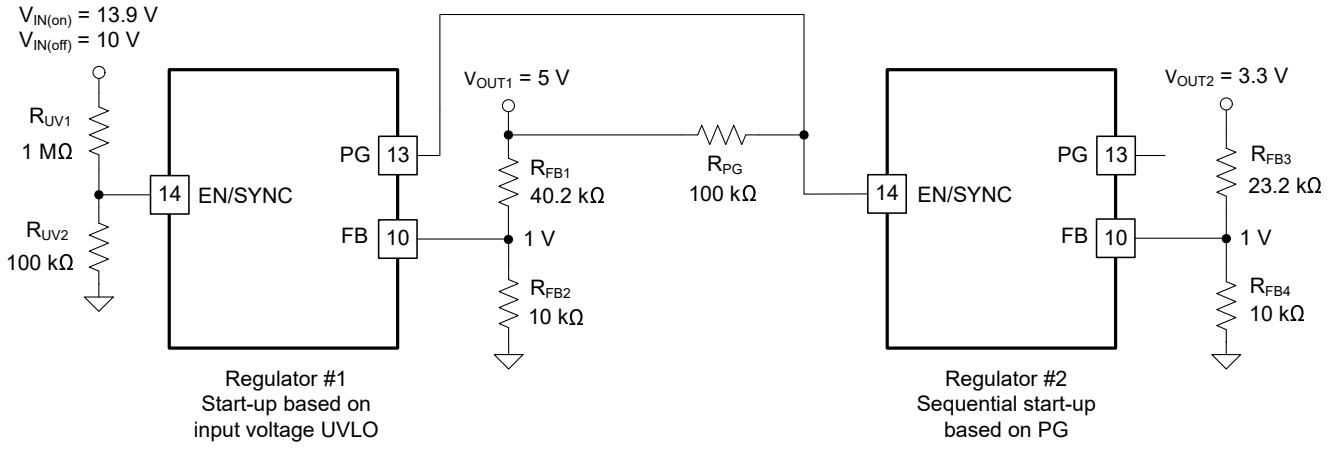

図 8-3. TPSM63606 Sequencing Implementation Using PG and EN/SYNC

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8.3.10 Adjustable Switch-Node Slew Rate (RBOOT, CBOOT)

Adjust the switch-node slew rate of the TPSM63606 to slow the switch-node voltage rise time and improve EMI performance at high frequencies. However, slowing the rise time decreases efficiency. Care must be taken to balance the improved EMI versus the decreased efficiency.

Internal to the module, a 100-Ω bootstrap resistor connects between the RBOOT and CBOOT pins as shown in 図 8-4. Leaving these pins open incorporates the 100-Ω resistor in the bootstrap circuit, slowing the switch voltage slew rate and optimizing EMI. However, if improved EMI is not required, connect RBOOT to CBOOT to short the internal resistor, thus resulting in the highest efficiency. Place a resistor across RBOOT and CBOOT to allow adjustment of the internal resistance to balance EMI and efficiency performance.

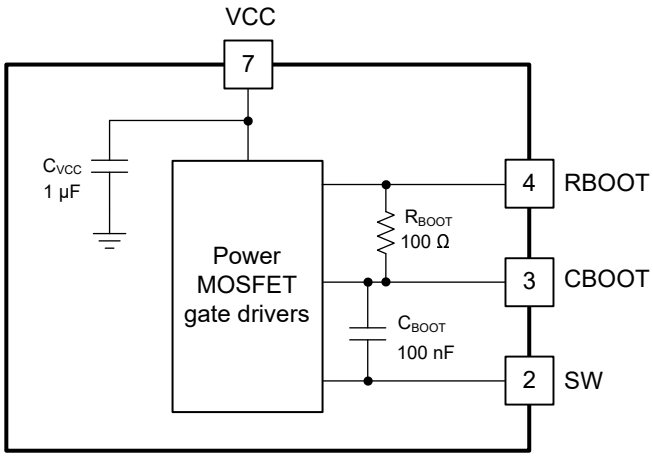

図 8-4. Internal BOOT Resistor

8.3.11 Bias Supply Regulator (VCC, VLDOIN)

VCC is the output of the internal LDO subregulator used to supply the control circuits of the TPSM63606. The nominal VCC voltage is 3.3 V. The VLDOIN pin is the input to the internal LDO. Connect this input to V_{OUT} to provide the lowest possible input supply current. If the VLDOIN voltage is less than 3.1 V, VIN1 and VIN2 directly power the internal LDO.

To prevent unsafe operation, VCC has UVLO protection that prevents switching if the internal voltage is too low. See V_{CC_UVLO} and $V_{CC_UVLO_HYS}$ in the *Electrical Characteristics*.

VCC must not be used to power external circuitry. Do not load VCC or short it to ground. VLDOIN is an optional input to the internal LDO. Connect an optional high quality 0.1-µF to 1-µF capacitor from VLDOIN to AGND for improved noise immunity.

The LDO provides the VCC voltage from one of two inputs: V_{IN} or VLDOIN. When VLDOIN is tied to ground or below 3.1 V, the LDO derives power from V_{IN}. The LDO input becomes VLDOIN when VLDOIN is tied to a voltage above 3.1 V. The VLDOIN voltage must not exceed both V_{IN} and 12 V.

式 8 specifies the LDO power loss reduction as:

$$P_{LDO\text{-}LOSS} = I_{LDO} \times (V_{IN\text{-}LDO} - V_{VCC}) \quad (8)$$

The VLDOIN input provides an option to supply the LDO with a lower voltage than V_{IN}, thus minimizing the LDO input voltage relative to VCC and reducing power loss. For example, if the LDO current is 10 mA at 1 MHz with V_{IN} = 24 V and V_{OUT} = 5 V, the LDO power loss with VLDOIN tied to ground is 10 mA × (24 V – 3.3 V) = 207 mW, while the loss with VLDOIN tied to V_{OUT} is equal to 10 mA × (5 V – 3.3 V) = 17 mW – a reduction of 190 mW.

図 8-5 and 図 8-6 show typical efficiency plots with and without VLDOIN connected to VOUT.

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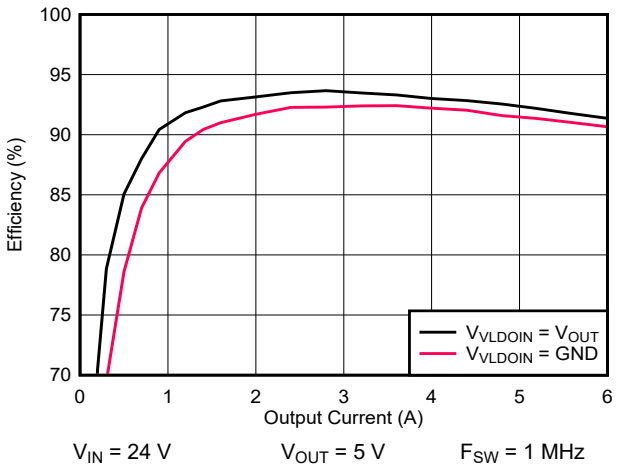

図 8-5. Efficiency Increase With External Bias

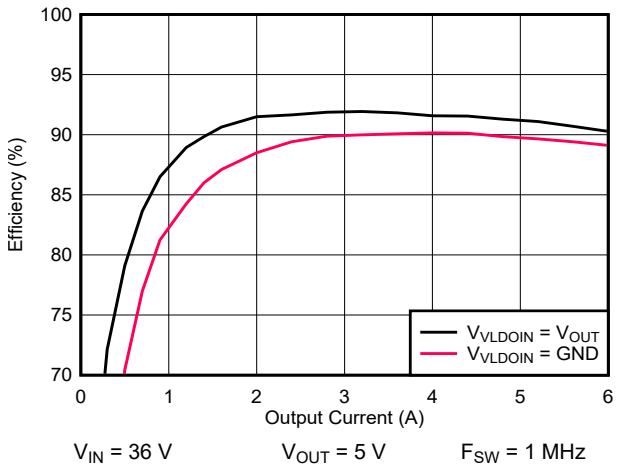

図 8-6. Efficiency Increase With External Bias

8.3.12 Overcurrent Protection (OCP)

The TPSM63606 is protected from overcurrent conditions using cycle-by-cycle current limiting of the peak inductor current. The current is compared every switching cycle to the current limit threshold. During an overcurrent condition, the output voltage decreases.

The TPSM63606 employs hiccup overcurrent protection if there is an extreme overload. In hiccup mode, the TPSM63606 module is shut down and kept off for 80 ms (typical) before a restart is attempted. If an overcurrent or short-circuit fault condition still exists, hiccup repeats until the fault condition is removed. Hiccup mode reduces power dissipation under severe overcurrent conditions, thus preventing overheating and potential damage to the device. Once the fault is removed, the module automatically recovers and returns to normal operation.

8.3.13 Thermal Shutdown

Thermal shutdown is an integrated self-protection used to limit junction temperature and prevent damage related to overheating. Thermal shutdown turns off the device when the junction temperature exceeds 168°C (typical) to prevent further power dissipation and temperature rise. Junction temperature decreases after shutdown, and the TPSM63606 attempts to restart when the junction temperature falls to 158°C (typical).

8.4 Device Functional Modes

8.4.1 Shutdown Mode

The EN/SYNC pin provides ON and OFF control for the TPSM63606. When $V_{EN/SYNC}$ is below approximately 0.4 V, the device is in shutdown mode. Both the internal LDO and the switching regulator are off. The quiescent current in shutdown mode drops to 0.6 µA (typical). The TPSM63606 also employs internal undervoltage protection. If the input voltage is below its UV threshold, the regulator remains off.

8.4.2 Standby Mode

The internal LDO for the VCC bias supply has a lower enable threshold than the regulator itself. When $V_{EN/SYNC}$ is above 1.1 V (maximum) and below the precision enable threshold of 1.263 V (typical), the internal LDO is on and regulating. The precision enable circuitry is turned on once the internal V_{CC} is above its UVLO threshold. The switching action and voltage regulation are not enabled until $V_{EN/SYNC}$ rises above the precision enable threshold.

8.4.3 Active Mode

The TPSM63606 is in active mode when V_{VCC} and $V_{EN/SYNC}$ are above their relevant thresholds and no fault conditions are present. The simplest way to enable operation is to connect EN/SYNC to V_{IN}, which allows self start-up when the applied input voltage exceeds the minimum start-up voltage.

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9 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPSM63606 synchronous buck module requires only a few external components to convert from a wide range of supply voltages to a fixed output voltage at an output current up to 6 A. To expedite and streamline the process of designing of a TPSM63606-based regulator, a comprehensive TPSM63606 quickstart calculator is available by download to assist the system designer with component selection for a given application.

9.2 Typical Applications

For the circuit schematic, bill of materials, PCB layout files, and test results of a TPSM63606-powered implementation, see the TPSM63606 EVM.

9.2.1 Design 1 – High-Efficiency 6-A Synchronous Buck Regulator for Industrial Applications

図 9-1 shows the schematic diagram of a 5-V, 6-A buck regulator with a switching frequency of 1 MHz. In this example, the target half-load and full-load efficiencies are 93.5% and 91.4%, respectively, based on a nominal input voltage of 24 V that ranges from 9 V to 36 V. A resistor R_{RT} of 13 kΩ sets the free-running switching frequency at 1 MHz. An optional SYNC input signal allows adjustment of the switching frequency from 700 kHz to 1.4 MHz for this specific application.

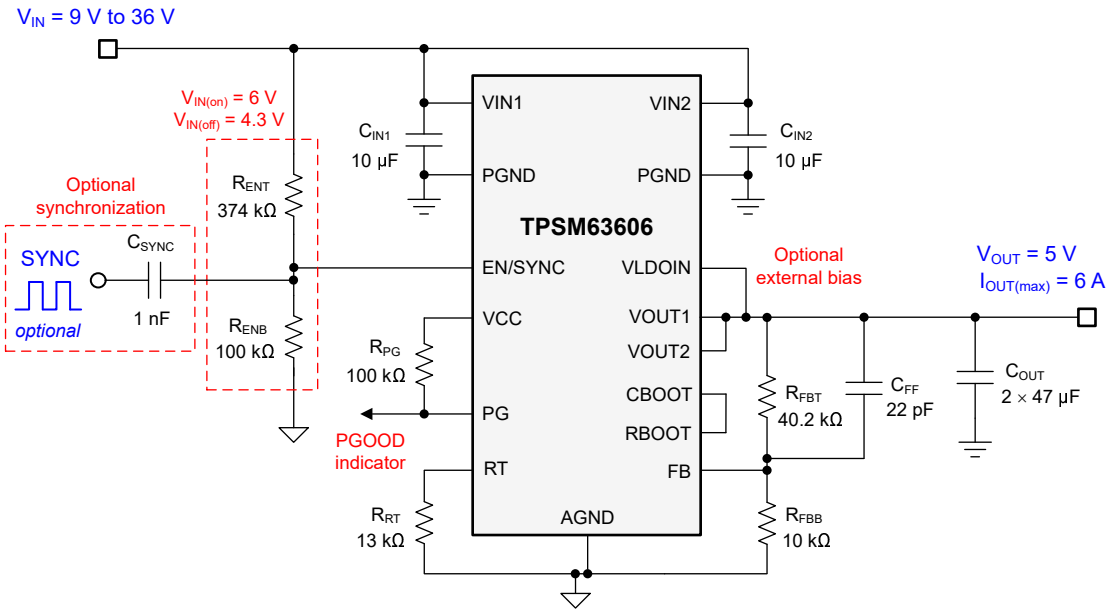

図 9-1. Circuit Schematic

9.2.1.1 Design Requirements

表 9-1 shows the intended input, output, and performance parameters for this application example. Note that if the input voltage decreases below approximately 5.8 V, the regulator operates in dropout with the output voltage below its 5-V setpoint.

表 9-1. Design Parameters

Design Parameter	Value
Input voltage range	9 V to 36 V
Input voltage UVLO turn on, off	6 V, 4.3 V
Output voltage	5 V
Maximum output current	6 A
Switching frequency	1 MHz
Output voltage regulation	±1%
Module shutdown current	< 1 µA

表 9-2 gives the selected buck module power-stage components with availability from multiple vendors. This design uses an all-ceramic output capacitor implementation.

表 9-2. List of Materials for Application Circuit 1

Reference Designator	Qty	Specification	Manufacturer(1)	Part Number
C_{IN1}, C_{IN2}	2	10 µF, 50 V, X7R, 1210, ceramic	Taiyo Yuden	UMJ325KB7106KMHT
			TDK	CNA6P1X7R1H106K
		10 µF, 50 V, X7S, 1210, ceramic	Murata	GCM32EC71H106KA03
			TDK	CGA6P3X7S1H106M
C_{OUT1}, C_{OUT2}	2	47 µF, 6.3 V, X7R, 1210, ceramic	Murata	GRM32ER70J476ME20K
			AVX	12106C476MAT2A
		47 µF, 10 V, X7R, 1210, ceramic	Murata	GRM32ER71A476ME15L
			AVX	1210ZC476MAT2A
		100 µF, 6.3 V, X7S, 1210, ceramic	Murata	GRM32EC70J107ME15L
U_1	1	TPSM63606 36-V, 6-A synchronous buck module	Texas Instruments	TPSM63606RDLR

(1) See the *Third-Party Products Disclaimer*.

More generally, the TPSM63606 module is designed to operate with a wide range of external components and system parameters. However, the integrated loop compensation is optimized for a certain range of output capacitance.

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM63606 module with WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

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9.2.1.2.2 Output Voltage Setpoint

The output voltage of a TPSM63606 module is externally adjustable using a resistor divider. A recommended value for R_{FBB} of 10 kΩ establishes a divider current of 0.1 mA. Select the value for R_{FBT} from 表 8-1 or calculate using 式 9:

$$R_{FBT}\left[k\Omega\right] = R_{FBB}\left[k\Omega\right] \cdot \left(\frac{V_{OUT}\left[V\right]}{1V} - 1 \right) = 10k\Omega \cdot \left(\frac{5V}{1V} - 1 \right) = 40k\Omega \quad (9)$$

Choose the closest standard value of 40.2 kΩ for R_{FBT}.

9.2.1.2.3 Switching Frequency Selection

Connect a 13-kΩ resistor from RT to AGND to set a switching frequency of 1 MHz, which is ideal for an output of 5 V as it establishes an inductor peak-to-peak ripple current in the range of 20% to 40% of the 6-A rated output current at a nominal input voltage of 24 V.

9.2.1.2.4 Input Capacitor Selection

The TPSM63606 requires a minimum input capacitance of 2 × 10-µF ceramic, preferably with X7R dielectric. The voltage rating of input capacitors must be greater than the maximum input voltage. For this design, select two 10-µF, X7R, 50-V, 1210 case size, ceramic capacitors connected from VIN1 and VIN2 to PGND as close as possible to the module. See 図 11-2 for recommneded layout placement.

9.2.1.2.5 Output Capacitor Selection

From 表 8-1, the TPSM63606 requires a minimum of 25 µF of effective output capacitance for proper operation at an output voltage of 5 V. Use high-quality ceramic type capacitors with sufficient voltage and temperature rating. If needed, connect additional output capacitance to reduce ripple voltage or for applications with specific load transient requirements.

For this design example, use two 47-µF, 6.3-V or 10-V, X7R, 1210, ceramic capacitors connected close to the module from the VOUT1 and VOUT2 pins to PGND. The total effective capacitance at 5 V is approximately 52 µF and 38 µF at 25°C and –40°C, respectively.

9.2.1.2.6 Other Connections

Short RBOOT to CBOOT and connect VLDOIN to the 5-V output for best efficiency. To increase phase margin when using an output capacitance close to the minimum recommended in 表 8-1, use a feedforward capacitor, designated as C_{FF} in 図 9-1, across the upper feedback resistor. Based on the feedback resistor values in this application, a capacitor of 22 pF sets a zero-pole pair at 180 kHz and 900 kHz, respectively.

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9.2.1.3 Application Curves

Unless otherwise indicated, V_{IN} = 24 V, V_{OUT} = 5 V, I_{OUT} = 6 A (0.83-Ω resistive load), and F_{SW} = 1 MHz.

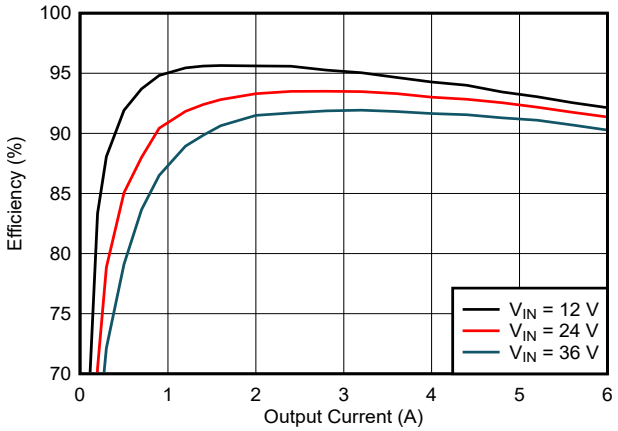

図 9-2. Efficiency

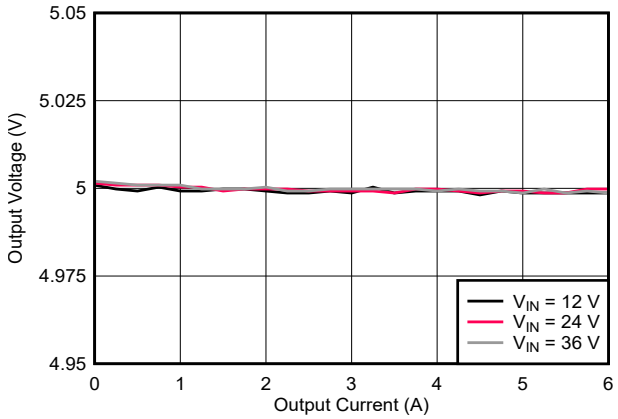

図 9-3. Load Regulation

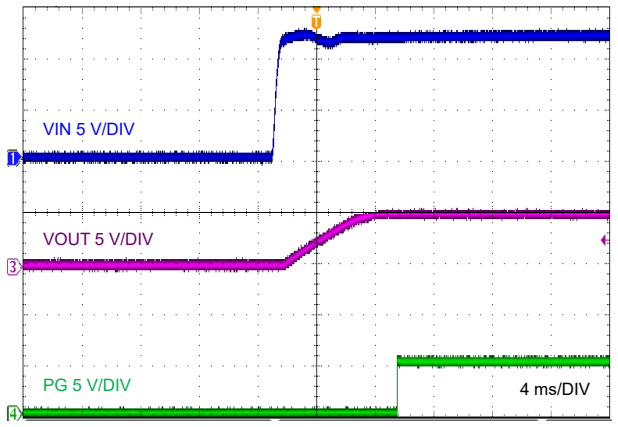

図 9-4. Start-Up, V_{IN} Stepped to 12 V

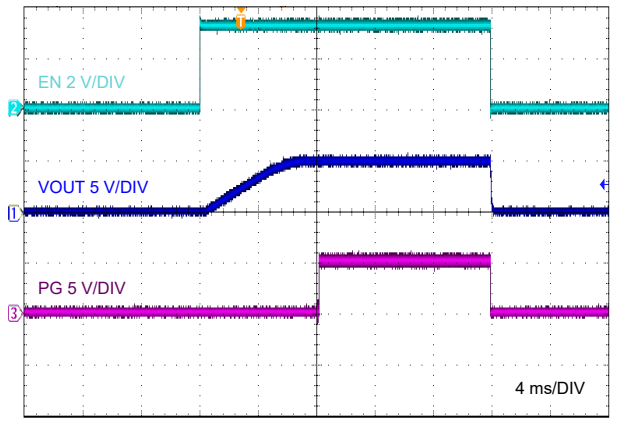

図 9-5. Enable ON and OFF, V_{IN} = 12 V

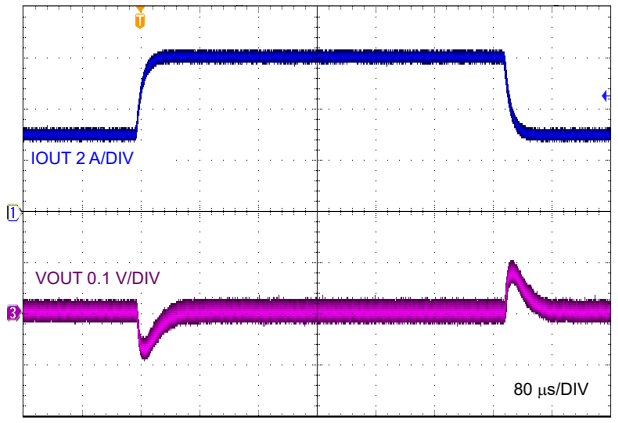

図 9-6. Load Transient, 3 A to 6 A, 1 A/µs

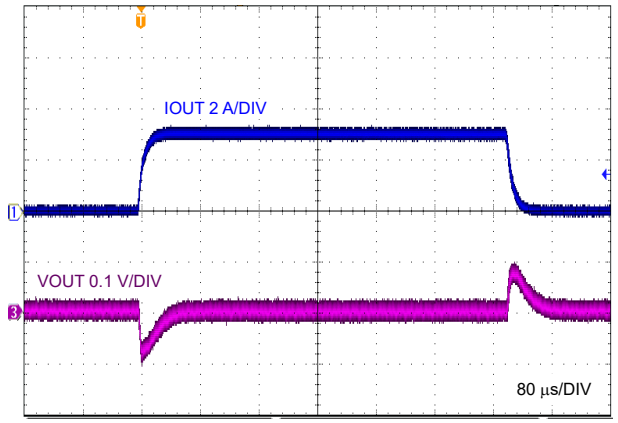

図 9-7. Load Transient, 0 A to 3 A, 1 A/µs

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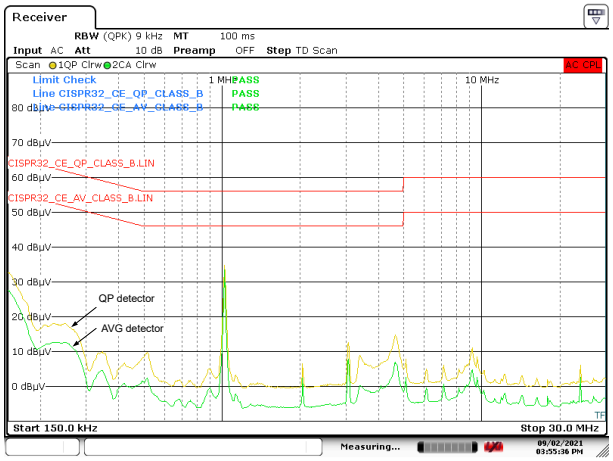

図 9-8. CISPR 32 Class B Conducted Emissions: V_{IN} = 12 V

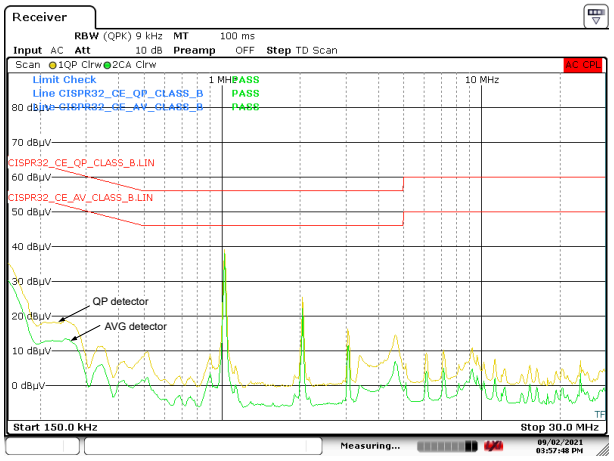

図 9-9. CISPR 32 Class B Conducted Emissions: V_{IN} = 24 V

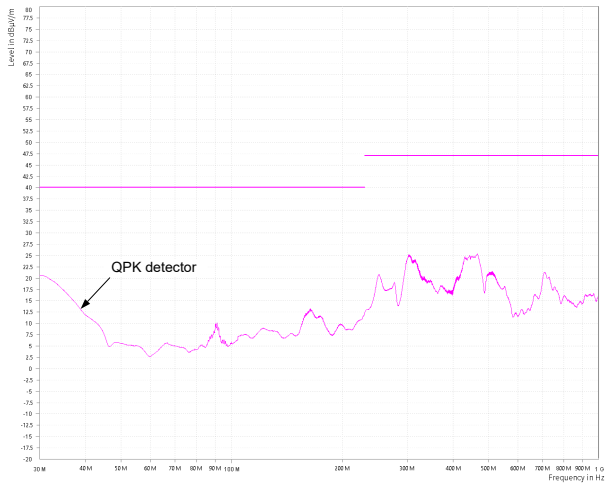

図 9-10. CISPR 32 Class B Radiated Emissions: Horizontal Polarization

図 9-11. CISPR 32 Class B Radiated Emissions: Vertical Polarization

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9.2.2 Design 2 – Inverting Buck-Boost Regulator with Negative Output Voltage

図 9-12 shows the schematic diagram of an inverting buck-boost (IBB) regulator with an output of –12 V at –2.5 A and a switching frequency of 2 MHz. In this example, the target half-load and full-load efficiencies are 91.5% and 90.5%, respectively, based on a nominal input voltage of 12 V that ranges from 9 V to 24 V.

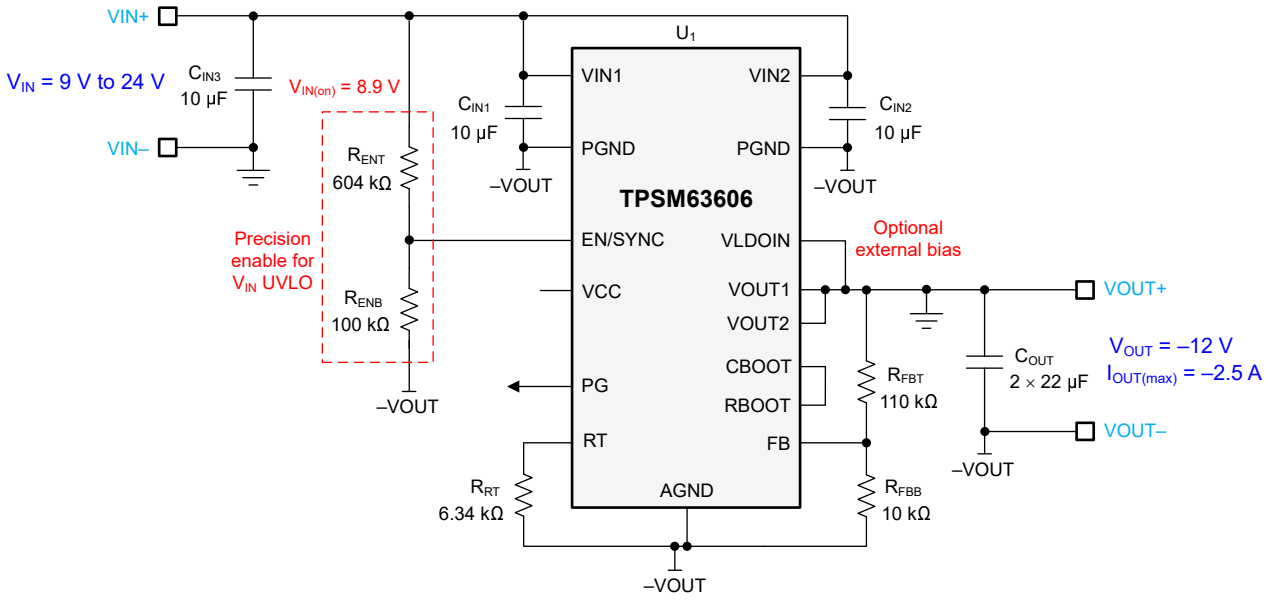

図 9-12. Circuit Schematic

9.2.2.1 Design Requirements

表 9-3 shows the intended input, output, and performance parameters for this application example. With an IBB topology, the module sees a total current of $I_{IN} + |–I_{OUT}|$, which is highest at minimum input voltage.

表 9-3. Design Parameters

Design Parameter	Value
Input voltage range	9 V to 24 V
Input voltage UVLO turn on	8.9 V
Output voltage	–12 V
Full-load current	–2.5 A
Switching frequency	2 MHz
Output voltage regulation	±1%

表 9-4 gives the selected buck module power-stage components with availability from multiple vendors. This design uses an all-ceramic output capacitor implementation.

表 9-4. List of Materials for Application Circuit 2

Ref Des	Qty	Specification	Manufacturer(1)	Part Number
C_{IN1}, C_{IN2}, C_{IN3}	3	10 µF, 50 V, X7R, 1210, ceramic	Kemet	C1210C106K5RACTU
			TDK	CNA6P1X7R1H106K
C_{OUT1}, C_{OUT2}	2	22 µF, 16 V, X7R, 1206, ceramic	Murata	GRM31CZ71C226ME15L
		22 µF, 25 V, X7R, 1210, ceramic	Murata	GRM32ER71E226ME15L
			AVX	12103C226KAT4A
		47 µF, 16 V, X6S, 1210, ceramic	Murata	GRM32EC81C476ME15L
U_1	1	TPSM63606 36-V, 6-A synchronous buck module	Texas Instruments	TPSM63606RDLR

(1) See the *Third-Party Products Disclaimer*.

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9.2.2.2 Detailed Design Procedure

9.2.2.2.1 Output Voltage Setpoint

For an output voltage of –12 V, choose upper and lower feedback resistance of 110 kΩ and 10 kΩ, respectively, using 式 1.

9.2.2.2.2 IBB Maximum Output Current

The achievable output current with an *IBB topology* using the TPSM63606 is $I_{OUT(max)} = I_{LDC(max)} \times (1 - D)$, where $I_{LDC(max)}$ = 6 A is the rated current of the module and $D = |V_{OUT}| / (V_{IN} + |V_{OUT}|)$ is the IBB duty cycle. 図 9-13 provides the maximum output current capability as a function of input voltage for output voltage setpoints of –3.3 V, –5 V, and –12 V.

9.2.2.2.3 Switching Frequency Selection

Connect a 6.34-kΩ resistor from RT to AGND to set a switching frequency of 2 MHz, which is ideal for an output of –12 V as it establishes an inductor peak-to-peak ripple current of approximately 40% of the 6-A rated module current at the nominal input voltage of 12 V.

9.2.2.2.4 Input Capacitor Selection

Use two 10-µF, 50-V, X7R-dielectric ceramic capacitors in 1210 case size connected symmetrically from the VIN1 and VIN2 pins to PGND as close as possible to the module. More specifically, these capacitors appear from the drain of the internal high-side MOSFET to the source of the low-side MOSFET, effectively connecting from the positive input voltage to the negative output voltage terminals.

The sum of the input and output voltages, $V_{IN} + |–V_{OUT}|$, is the effective applied voltage across the capacitors. The total effective capacitance at 25°C and input voltages of 12 V and 24 V (corresponding to applied voltages of 24 V and 36 V) is approximately 12 µF and 8 µF, respectively. Check the capacitance versus voltage derating curve in the capacitor data sheet.

Use an additional 10-µF, 50-V capacitor directly across the input. This capacitor is designated as C_{IN3} and connects across the VIN+ and VIN– terminals as shown in 図 9-12.

9.2.2.2.5 Output Capacitor Selection

For this IBB design example, use two 22-µF, 25-V, X7R-dielectric ceramic capacitors in 1210 case size connected symmetrically close to the module from the VOUT1 and VOUT2 pins to PGND. The total effective capacitance is approximately 16 µF with DC bias of 12 V.

9.2.2.2.6 Other Considerations

Short RBOOT to CBOOT and connect VLDOIN to the power stage GND terminal (corresponding to VOUT1, VOUT2 of the module) for best efficiency.

The right-half-plane zero of an IBB topology is at its lowest freqeuncy at minimum input voltage and highest load current. Using the TPSM63606 quickstart calculator, select the output capacitance to set that the loop crossover freqeuncy at less than one third of the lowest right-half-plane zero frequency for a given application.

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9.2.2.3 Application Curves

Unless otherwise indicated, V_{IN} = 12 V, V_{OUT} = –12 V, I_{OUT} = –2.5 A (4.8-Ω resistive load), and F_{SW} = 2 MHz.

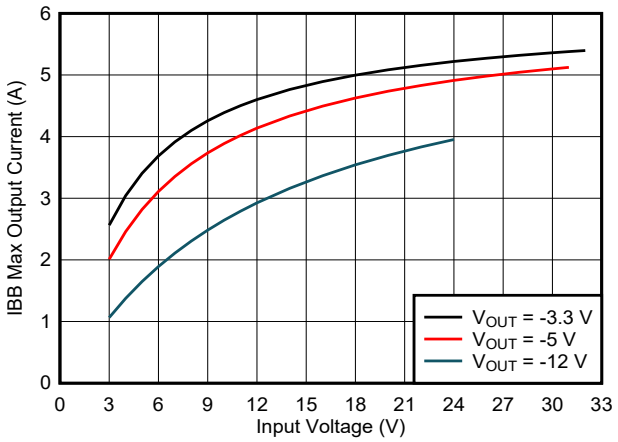

図 9-13. IBB Maximum Output Current

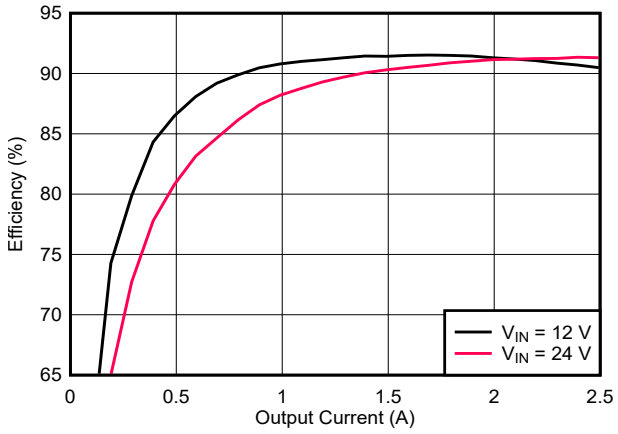

図 9-14. Efficiency

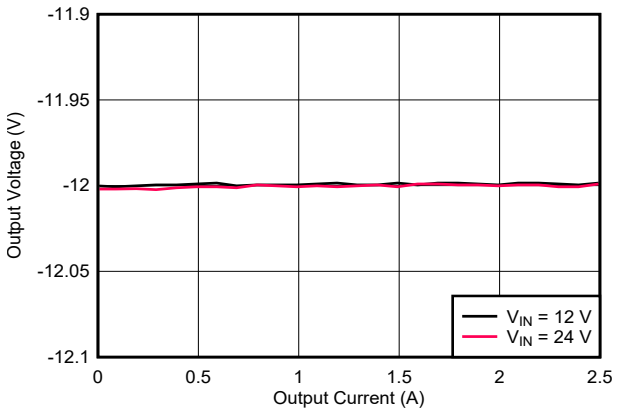

図 9-15. Load Regulation

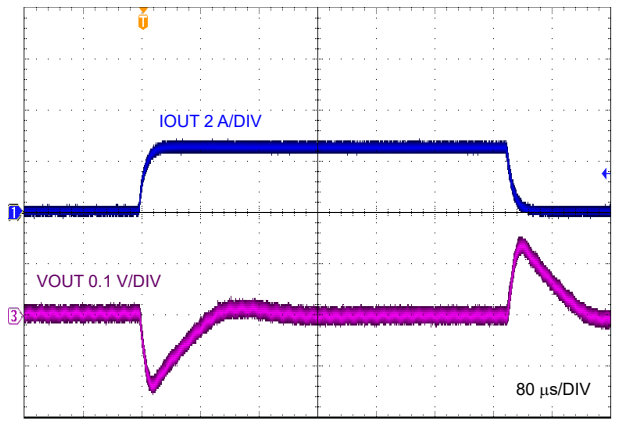

図 9-16. Load Transient, 0 A to 2.5 A

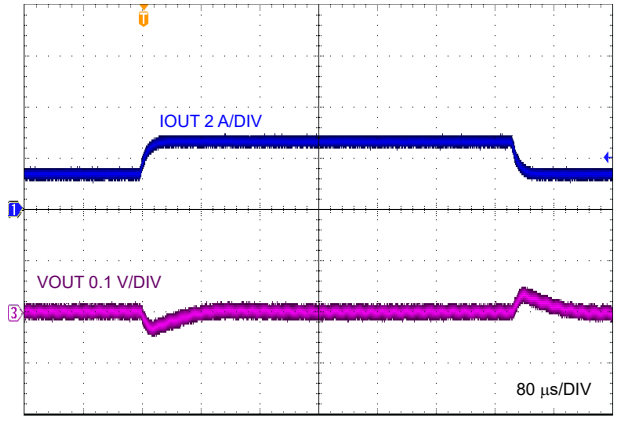

図 9-17. Load Transient, 1.25 A to 2.5 A

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10 Power Supply Recommendations

The TPSM63606 buck module is designed to operate over a wide input voltage range of 3 V to 36 V. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator circuit. Estimate the average input current with 式 10.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \tag{10}$$

where

- η is the efficiency.

If the module is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse affect on module operation. More specifically, the parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit, possibly resulting in instability, voltage transients, or both, each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. If the module is operating close to the minimum input voltage, this dip can cause false UVLO triggering and a system reset.

The best way to solve such issues is to reduce the distance from the input supply to the module and use an electrolytic input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitor helps damp the input resonant circuit and reduce any overshoot or undershoot at the input. A capacitance in the range of 47 µF to 100 µF is usually sufficient to provide input parallel damping and helps hold the input voltage steady during large load transients. A typical ESR of 0.1 Ω to 0.4 Ω provides enough damping for most input circuit configurations.

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11 Layout

Proper PCB design and layout is important in high-current, fast-switching module circuits (with high internal voltage and current slew rates) to achieve reliable device operation and design robustness. Furthermore, the EMI performance of the module depends to a large extent on PCB layout.

11.1 Layout Guidelines

The following list summarizes the essential guidelines for PCB layout and component placement to optimze DC/DC module performance, including thermals and EMI signature. 図 11-1 and 図 11-2 show a recommended PCB layout for the TPSM63606 with optimized placement and routing of the power-stage and small-signal components.

- *Place input capacitors as close as possible to the VIN pins.* Note the dual and symmetrical arrangement of the input capacitors based on the VIN1 and VIN2 pins located on each side of the module package. The high-frequency currents are split in two and effectively flow in opposing directions such that the related magnetic fields contributions cancel each other, leading to improved EMI performance.
  - Use low-ESR 1206 or 1210 ceramic capacitors with X7R or X7S dielectric. The module has integrated dual 0402 input capacitors for high-frequency bypass.
  - Ground return paths for the input capacitors should consist of localized top-side planes that connect to the PGND pads under the module.
  - Even though the VIN pins are connected internally, use a wide polygon plane on a lower PCB layer to connect these pins together and to the input supply.
- *Place output capacitors as close as possible to the VOUT pins.* A similar dual and symmetrical arrangement of the output capacitors enables magnetic field cancellation and EMI mitigation.
  - Ground return paths for the output capacitors should consist of localized top-side planes that connect to the PGND pads under the module.
  - Even though the VOUT pins are connected internally, use a wide polygon plane on a lower PCB layer to connect these pins together and to the load, thus reducing conduction loss and thermal stress.
- *Keep the FB trace as short as possible by placing the feedback resistors close to the FB pin.* Reduce noise sensitivity of the output voltage feedback path by placing the resistor divider close to the FB pin, rather than close to the load. FB is the input to the voltage-loop error anplifier and represents a high-impedance node sensitive to noise. Route a trace from the upper feedback resistor to the required point of output voltage regulation.
- *Use a solid ground plane on the PCB layer directly below the top layer with the module.* This plane acts as a noise shield by minimizing the magnetic fields associated with the currents in the switching loops. Connect AGND pins 6 and 11 directly to PGND pin 19 under the module.
- *Provide enough PCB area for proper heatsinking.* Use sufficient copper area to acheive a low thermal impedance commensurate with the maximum load current and ambient temperature conditions. Provide adequate heatsinking for the TPSM63606 to keep the junction temperature below 150°C. For operation at full rated load, the top-side ground plane is an important heat-dissipating area. Use an array of heat-sinking vias to connect the exposed pads (PGND) of the package to the PCB ground plane. If the PCB has multiple copper layers, connect these thermal vias to inner-layer ground planes. Make the top and bottom PCB layers preferably with two-ounce copper thickness (and no less than one ounce).

11.1.1 Thermal Design and Layout

For a DC/DC module to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The TPSM63606 module is available in a small 5.5-mm × 5-mm 20-pin QFN (RDL) package to cover a range of application requirements. The *Thermal Information* table summarizes the thermal metrics of this package with related detail provided by the *Semiconductor and IC Package Thermal Metrics Application Report*.

The 20-pin QFN package offers a means of removing heat through the exposed thermal pads at the base of the package. This allows a significant improvement in heatsinking, and it becomes imperative that the PCB is designed with thermal lands, thermal vias, and one or more ground planes to complete the heat removal subsystem. The exposed pads of the TPSM63606 are soldered to the ground-connected copper lands on the PCB directly underneath the device package, reducing the thermal resistance to a very low value.

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Preferably, use a four-layer board with 2-oz copper thickness for all layers to provide low impedance, proper shielding and lower thermal resistance. Numerous vias with a 0.3-mm diameter connected from the thermal lands to the internal and solder-side ground planes are vital to promote heat transfer. In a multi-layer PCB stack-up, a solid ground plane is typically placed on the PCB layer below the power-stage components. Not only does this provide a plane for the power-stage currents to flow, but it also represents a thermally conductive path away from the heat-generating device.

11.2 Layout Example

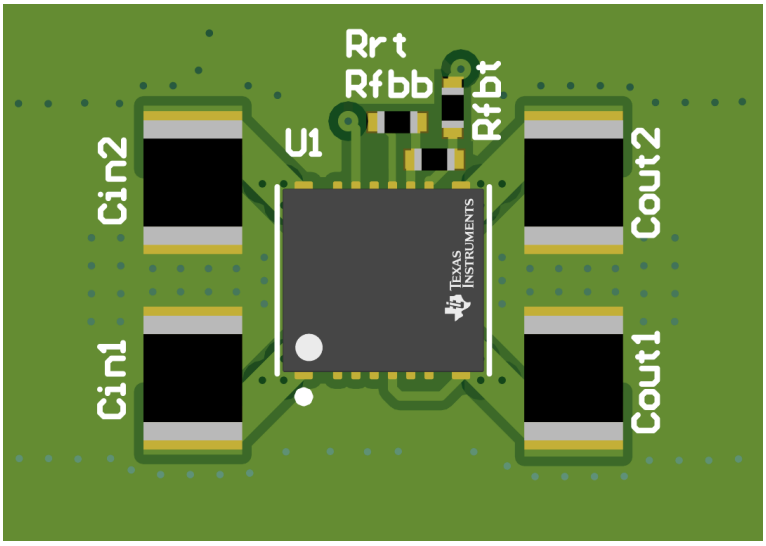

図 11-1. Typical Layout

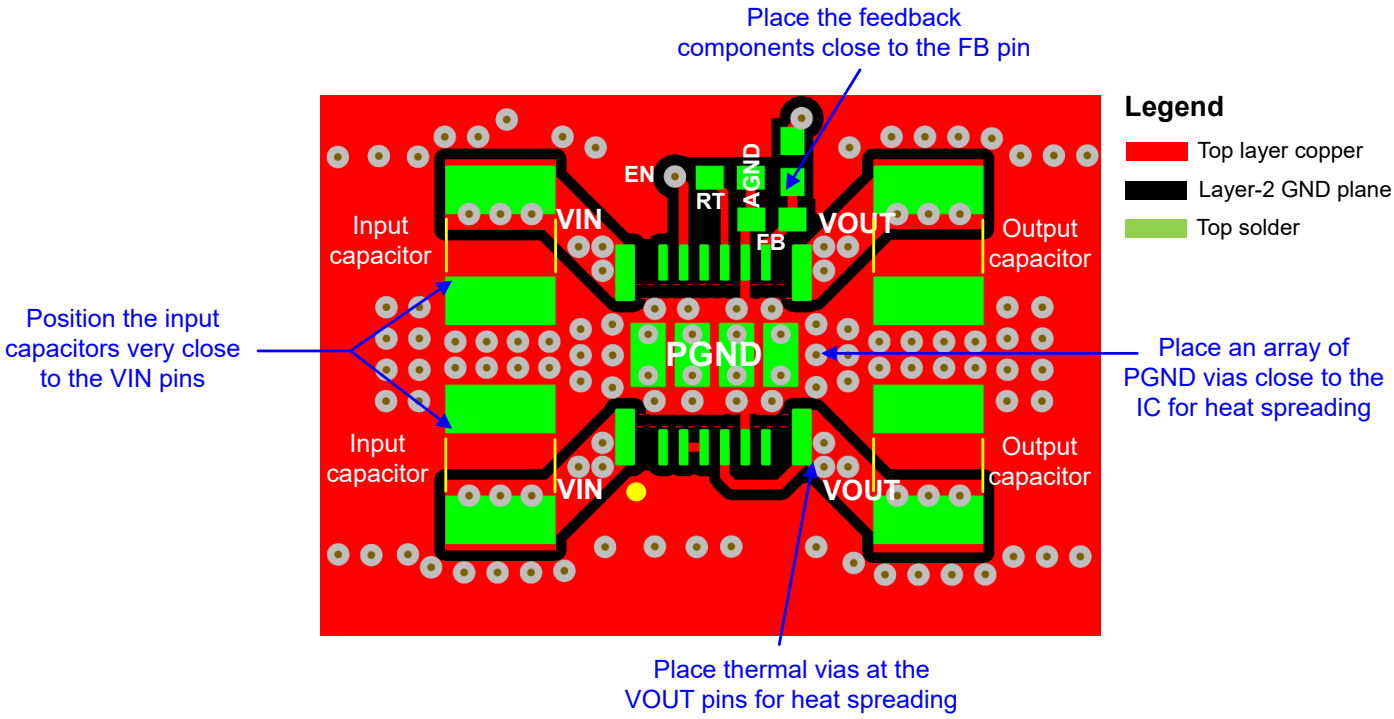

図 11-2. Typical Top Layer Design

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11.2.1 Package Specifications

表 11-1. Package Specifications Table

TPSM63606		VALUE	UNIT
Weight		748	mg
Flammability	Meets UL 94 V-0		
MTBF calculated reliability	Per Bellcore TR-332, 50% stress, T_A = 40°C, ground benign	2580	MHrs

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.1.2 Development Support

With an input operating voltage from 3 V to 36 V and rated output current from 2 A to 6 A, the TPSM63602/3/4/6 family of synchronous buck power modules specified in 表 12-1 provides flexibility, scalability and optimized solution size for a range of applications. These modules enable DC/DC solutions with high density, low EMI and increased flexibility. Available EMI mitigation features include pseudo-random spread spectrum (PRSS), RBOOT-configured switch-node slew rate control, and integrated input bypass capacitors. All modules are rated for an ambient temperature up to 105°C.

表 12-1. Synchronous Buck DC/DC Power Module Family

DC/DC Module	Rated I_{OUT}	Package	Dimensions	Features	EMI Mitigation
TPSM63602	2 A	B0QFN (30)	6.0 × 4.0 × 1.8 mm	RT adjustable F_{SW}, external synchronization	PRSS, RBOOT, integrated input, VCC, and BOOT capacitors
TPSM63603	3 A				
TPSM63604	4 A	B3QFN (20)	5.5 × 5.0 × 4.0 mm		
TPSM63606	6 A				

For development support see the following:

- TPSM63606 *Quickstart Calculator*
- TPSM63606 *Simulation Models*
- *TPSM63606 and TPSM63606S EVM User's Guide*
- *TPSM63606 EVM Layout Files (Altium)*
- For TI's reference design library, visit the *TI Reference Design library*.
- For TI's WEBENCH Design Environment, visit the *WEBENCH® Design Center*.
- To design a low-EMI power supply, review TI's comprehensive *EMI Training Series*.
- To design an inverting buck-boost (IBB) regulator, visit *DC/DC inverting buck-boost modules*.
- TI Reference Designs:
  - *Multiple Output Power Solution For Kintex 7 Application*
  - *Arria V Power Reference Design*
  - *Altera Cyclone V SoC Power Supply Reference Design*
  - *Space-optimized DC/DC Inverting Power Module Reference Design With Minimal BOM Count*
  - *3- To 11.5-V_{IN}, –5-V_{OUT}, 1.5-A Inverting Power Module Reference Design For Small, Low-noise Systems*
- Technical Articles:
  - *Powering Medical Imaging Applications With DC/DC Buck Converters*
  - *How To Create A Programmable Output Inverting Buck-boost Regulator*
- To view a related device of this product, see the LM61460 36-V, 6-A synchronous buck converter.

12.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM63606 module with WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

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In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Innovative DC/DC Power Modules* selection guide
- Texas Instruments, *Enabling Small, Cool and Quiet Power Modules with Enhanced HotRod™ QFN Package Technology* white paper
- Texas Instruments, *Benefits and Trade-offs of Various Power-Module Package Options* white paper
- Texas Instruments, *Simplify Low EMI Design with Power Modules* white paper
- Texas Instruments, *Power Modules for Lab Instrumentation* white paper
- Texas Instruments, *An Engineer's Guide To EMI In DC/DC Regulators* e-book
- Texas Instruments, *Soldering Considerations for Power Modules* application report
- Texas Instruments, *Practical Thermal Design With DC/DC Power Modules* application report
- Texas Instruments, *Using New Thermal Metrics* application report
- Texas Instruments, *AN-2020 Thermal Design By Insight, Not Hindsight* application report
- Texas Instruments, *Using the TPSM53602/3/4 for Negative Output Inverting Buck-Boost Applications* application report

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 サポート・リソース

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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPSM63606RDLR	ACTIVE	B3QFN	RDL	20	1000	RoHS Exempt & Green	NIPDAU	Level-3-250C-168 HR	-40 to 125	TPS63606 B1	Samples
TPSM63606SRDLR	ACTIVE	B3QFN	RDL	20	1000	RoHS Exempt & Green	NIPDAU	Level-3-250C-168 HR	-40 to 125	TPS63606S B1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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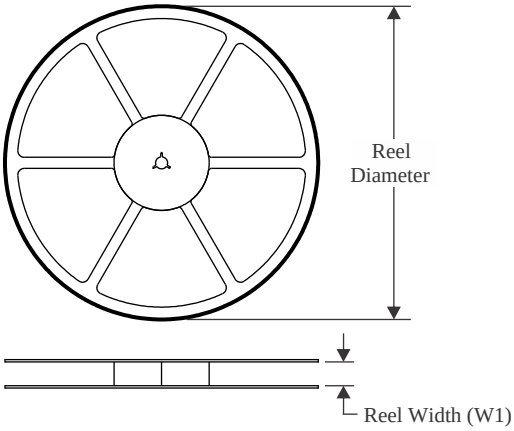
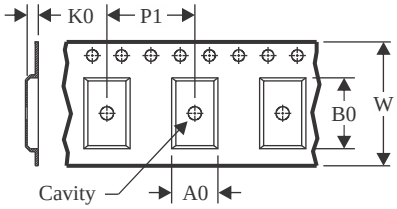
TAPE AND REEL INFORMATION

REEL DIMENSIONS

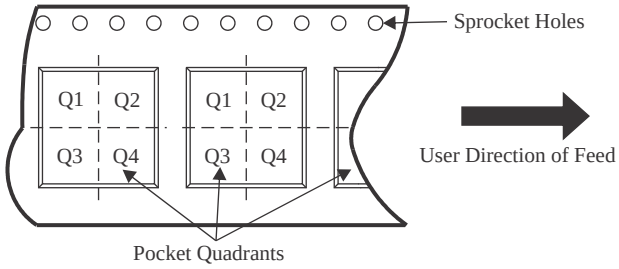


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

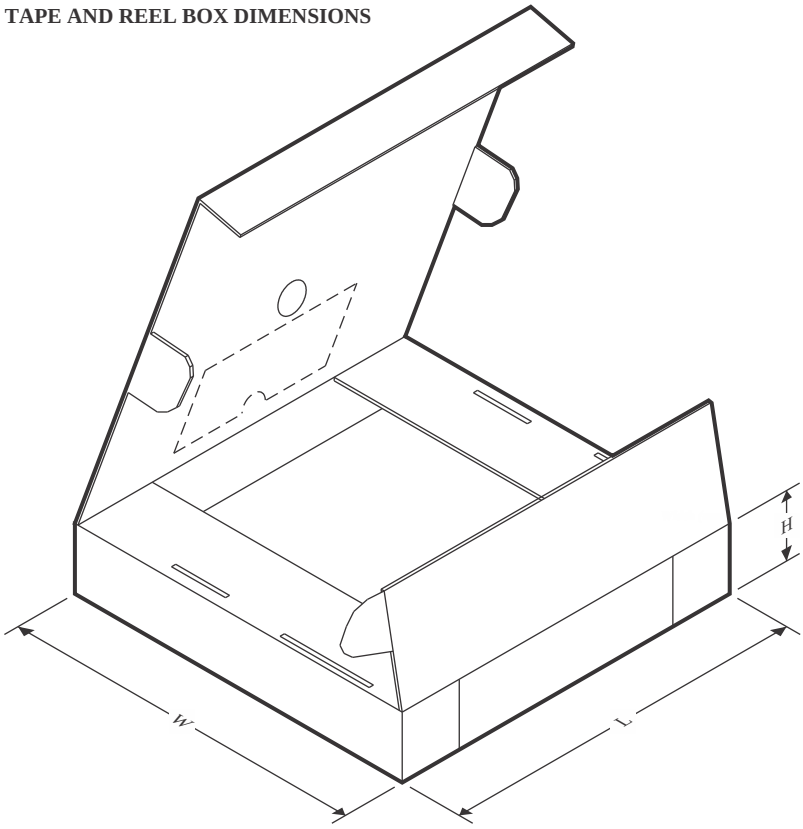
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM63606RDLR	B3QFN	RDL	20	1000	330.0	16.4	5.28	5.78	4.28	8.0	16.0	Q1
TPSM63606SRDLR	B3QFN	RDL	20	1000	330.0	16.4	5.28	5.78	4.28	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

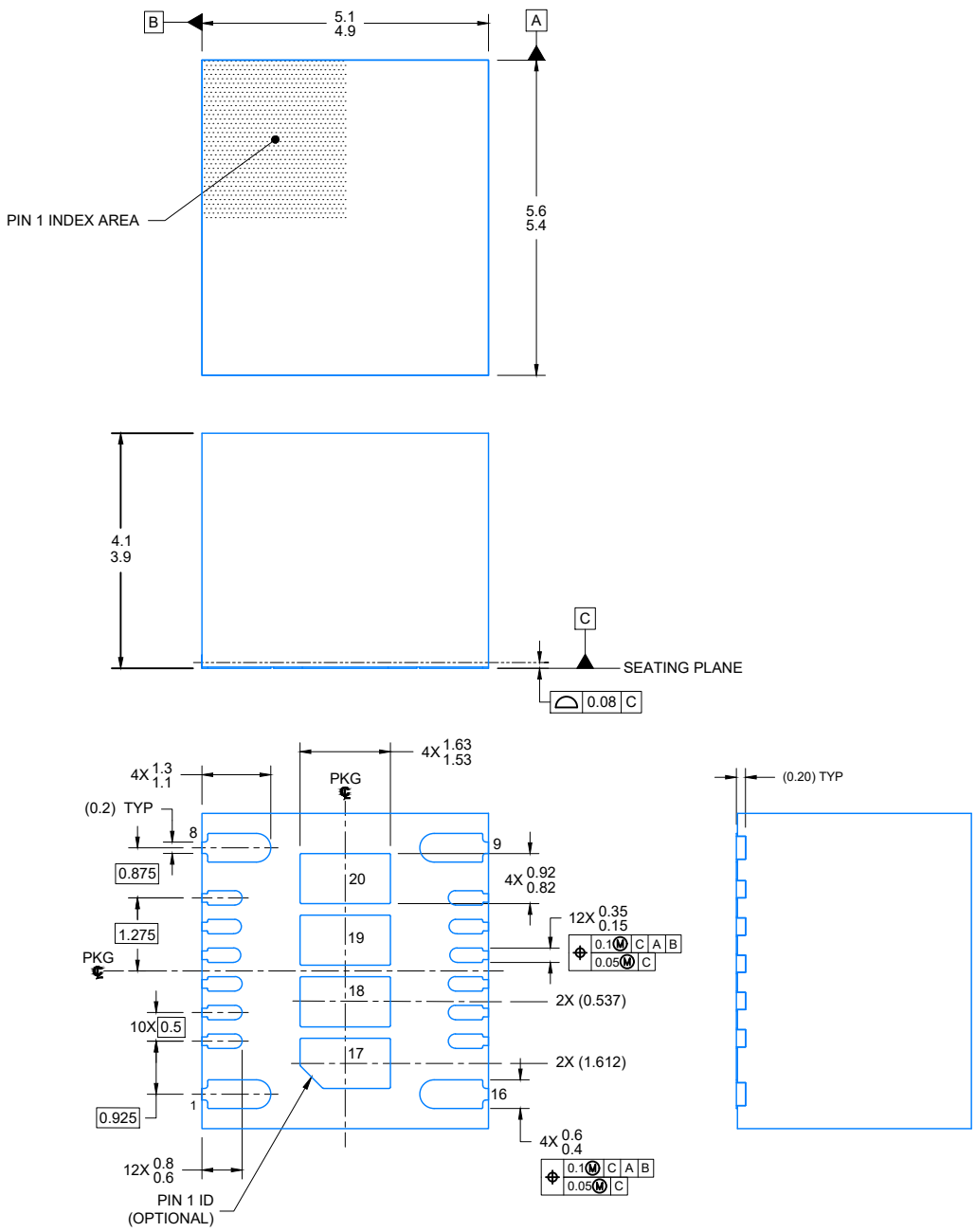
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM63606RDLR	B3QFN	RDL	20	1000	336.0	336.0	48.0
TPSM63606SRDLR	B3QFN	RDL	20	1000	336.0	336.0	48.0

PACKAGE OUTLINE

RDL0020A

B3QFN - 4.1 mm max height

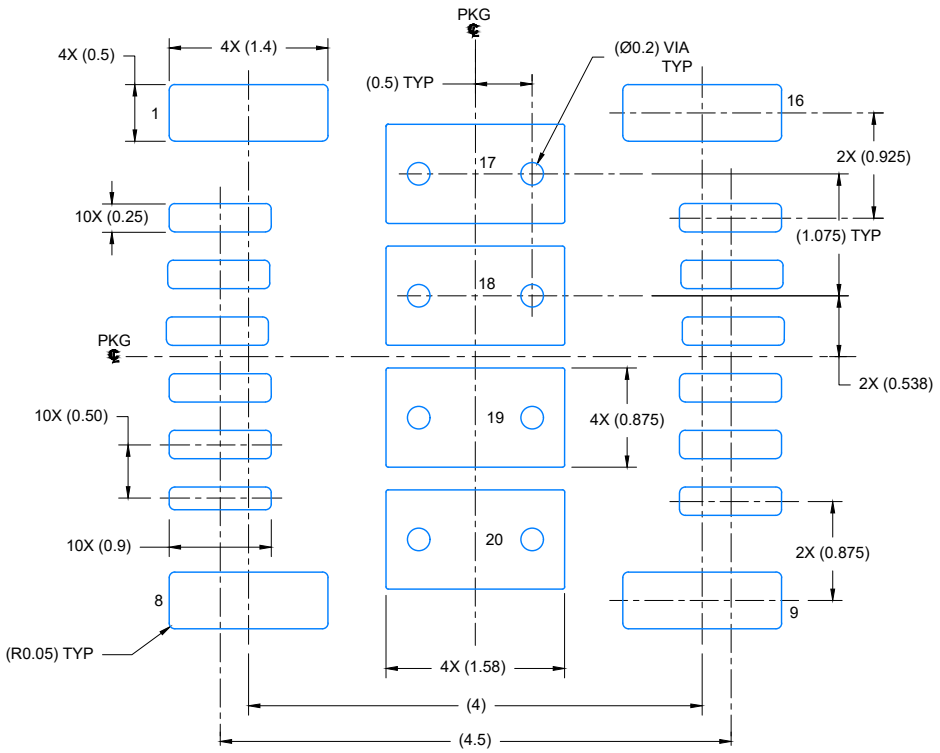
PLASTIC QUAD FLAT PACK- NO LEAD



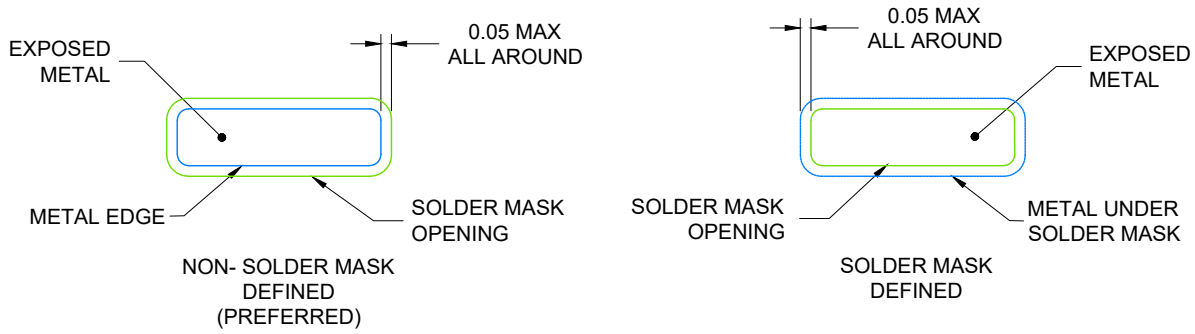
4226416/B 04/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

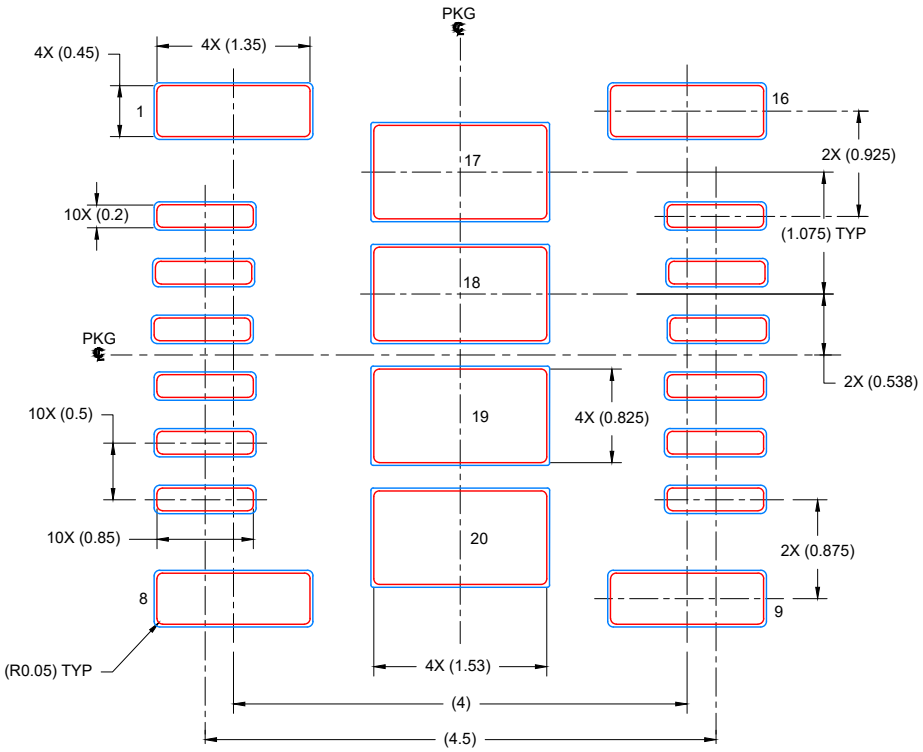


SOLDER MASK DETAILS

4226416/B 04/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17,18, 19 & 20 :
91% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

4226416/B 04/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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