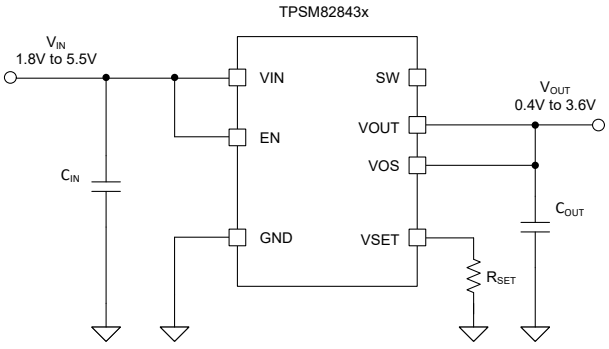
TPSM82843x インダクタ内蔵、QFN パッケージ封止、1.8V～5.5V、600mA、超低 I_Q 275nA、高効率降圧コンバータ

1 特長

- 入力電圧範囲:1.8V～5.5V
- 出力電圧範囲:0.4V ～ 3.6V
- 275nA の静止電流 (代表値)、4nA シャットダウン
- 内蔵出力分圧器からのゼロ フィードバック誤差
- 1.2V ロジック対応の EN (イネーブル) ピン
- 600mA 出力電流および出力放電
- VSET ピンの単一抵抗で、1% 精度の電圧選択
  - TPSM828436:0.4V～0.8V
  - TPSM828437:0.8V～1.8V
  - TPSM828438:1.8V～3.6V
- コストとサイズを最適化した受動部品
  - 最小 4.7µF の C_{IN} および C_{OUT}
  - 0402 および 0201 コンデンサをサポート
- パワー セーブ モードでは小さい出力電圧リップル
- RF フレンドリで高速過渡の DCS-Control
- リップルなし 100% モードへの自動遷移
- 2.45mm × 2.70mm × 1.29mm の小型 QFN パッケージ

2 アプリケーション

- Bluetooth® Low Energy BLE (BTLE) リモート コントロール、ワイヤレス センサ、ビーコン
- IoT Wi-Fi® バッテリ動作ノード
- スマート メーター、暖房メーター、遠隔測定
- データロガー、予測可能なメンテナンス
- プログラマブル ロジック コントローラ (PLC) ポイント オブ ロード
- ウェアラブル電子機器
- ヘッドセット、ヘッドホン、小型イヤホン
- 補聴器



代表的なアプリケーション

3 概要

高効率の TPSM82843x 降圧コンバータ ファミリは、動作時の静止電流 I_Q が 275nA (標準値) と非常に小さく、また、シャットダウン電流はわずか 4nA (標準値) です。インダクタは QFN パッケージに内蔵されているため、使いやすさが向上し、部品表 (BOM) をわずか 3 個の受動部品に減らすことができます。

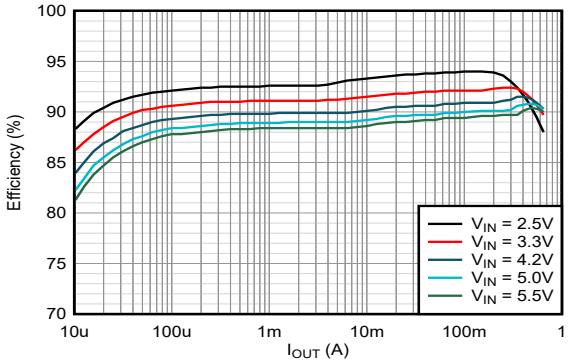
この RF フレンドリなデバイスは、低い出力電圧リップルを備えた DCS-Control を使用しています。このデバイスは、Wi-Fi や Bluetooth などのワイヤレス アプリケーションの電力供給用に設計されています。このデバイスは 1.5MHz でスイッチングを行い、軽負荷電流が最小 10µA のときも高い効率を実現し、バッテリ寿命を延長することができ、熱管理が簡単です。内蔵帰還分圧器により、湿度、温度、振動は出力電圧の精度に影響を与えません。このため、このデバイスは産業用のポイント オブ ロード アプリケーションにも最適です。

部品番号ごとに 18 の事前定義された出力電圧 (VSET ピンにおいて標準 E48 (2%) または E96 (1%) 抵抗により 1% の精度で選択) により、幅広いアプリケーションに対応できます。

製品情報

部品番号 (3)	V_{OUT} 範囲	パッケージ (1)	パッケージ サイズ(2)
TPSM828436	0.4V～0.8V	VCF (QFN-FCMOD、7)	2.45mm × 2.7mm
TPSM828437	0.8V～1.8V		
TPSM828438	1.8V～3.6V		

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
(3) デバイス比較表を参照してください。



1.8V_{OUT} での出力電流と効率の関係

Table of Contents

1 特長.....1
2 アプリケーション.....1
3 概要.....1
4 Device Comparison Table.....3
5 Pin Configuration and Functions.....3
6 Specifications.....4
6.1 Absolute Maximum Ratings.....4
6.2 ESD Ratings.....4
6.3 Recommended Operating Conditions.....4
6.4 Thermal Information.....5
6.5 Electrical Characteristics.....5
6.6 Typical Characteristics.....7
7 Detailed Description.....8
7.1 Overview.....8
7.2 Functional Block Diagram.....8
7.3 Feature Description.....9
7.4 Device Functional Modes.....11
8 Application and Implementation.....12
8.1 Application Information.....12
8.2 Typical Application.....12
8.3 Power Supply Recommendations.....18
8.4 Layout.....18
9 Device and Documentation Support.....19
9.1 Device Support.....19
9.2 ドキュメントの更新通知を受け取る方法.....19
9.3 サポート・リソース.....19
9.4 Trademarks.....19
9.5 静電気放電に関する注意事項.....19
9.6 用語集.....19
10 Revision History.....19
11 Mechanical, Packaging, and Orderable Information.....20

4 Device Comparison Table

Device	Fixed V_{OUT} VSET = GND	Selectable Output Voltages	f_{SW} [MHz]	Soft Start t_{SS}
TPSM828436VCFR	1.0V	0.4V – 0.8V in 25mV steps	1.5	0.45ms
TPSM828437VCFR	1.8V	0.8V – 1.6V in 50mV steps	1.5	1ms
TPSM828438VCFR	3.6V	1.8V – 3.4V in 100mV steps	1.5	0.7ms

5 Pin Configuration and Functions

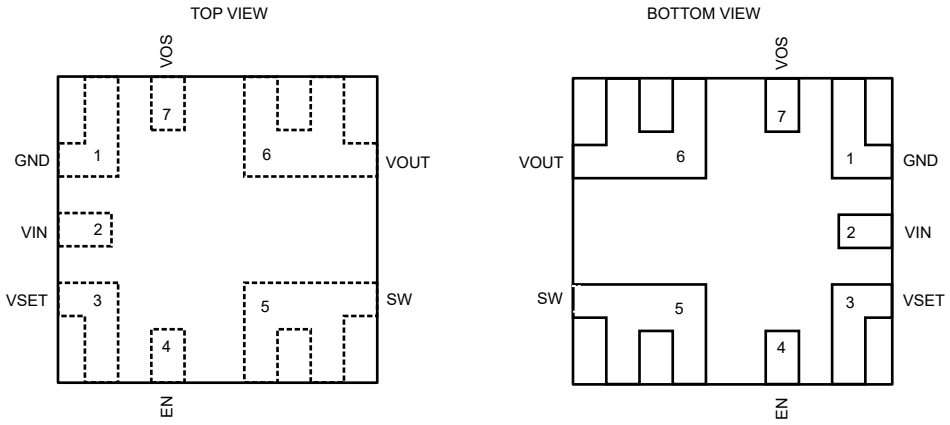


図 5-1. VCF, 7-Pin QFN-FCMOD Package

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
GND	1	PWR	GND supply pin. Connect this pin close to the GND terminal of the input and output capacitor.
VIN	2	PWR	V_{IN} power supply pin. Connect the input capacitor close to this pin for best noise and voltage spike suppression. A ceramic capacitor is required.
VOUT	6	PWR	Output voltage of the module. Connect this pin to the output capacitor.
VSET	3	I	Connecting a resistor to GND selects a pre-defined output voltage.
VOS	7	I	Output voltage sense pin for the internal feedback divider network and regulation loop. This pin also discharges V_{OUT} by an internal MOSFET when the converter is disabled. Connect this pin directly to the output capacitor with a short trace.
SW	5	O	This pin is the switch pin of the converter. This pin connects to the internal power MOSFET and the inductor. Avoid connecting this pin to larger traces as this action can increase EMI. This pin can stay unconnected or be soldered to a small pad for thermal improvement.
EN	4	I	A high level enables the devices and a low level turns the device off. The pin features an internal pulldown resistor, which is disabled after the device has started up.

(1) I = input, O = output, PWR = power

6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage	VIN	–0.3	6	V
Pin voltage	SW, VOUT at DC condition	–0.3	V_{IN} + 0.3V	V
Pin voltage	SW, transient < 10ns, while switching	–2.5	9	V
Pin voltage	EN, VSET	–0.3	6	V
Pin voltage	VOS	–0.3	5	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage V_{IN}	1.8		5.5	V
I_{OUT}	Output current			0.6	A
C_{OUT}	Effective output capacitance	4		25	µF
C_{IN}	Effective input capacitance	0.5	4.7		µF
C_{VSET}	External parasitic capacitance at VSET pin			30	pF
R_{SET}	Resistance range for external resistor at VSET pin (E96 1% resistor values)	10		249	kΩ
	External resistor tolerance E96 series at VSET pin			1%	
	E96 resistor series temperature coefficient (TCR)	–200		+200	ppm/°C
T_J	Operating junction temperature range	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPSM82843x VCF (QFN-FCMOD) 7 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	72.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	(–4.2)[2]	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) Case top temperature can be higher than temperature of active circuit because of inductor power dissipation. This results in a negative Junction-to-top characterization parameter.

6.5 Electrical Characteristics

T_J = –40°C to +125°C, V_{IN} = 1.8V to 5.5V. Typical values are at T_J = 25°C, V_{IN} = 3.6V and V_{OUT} = 0.7V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Operating quiescent current in PFM mode while output voltage > set output voltage	Non-switching, V_{EN} = V_{IN}, I_{OUT} = 0µA, T_J = –40°C to 85°C		275	1500	nA
I_{SD}	Shutdown current	V_{EN} = 0 V, VSET = GND, T_J = –40°C to 85°C		4	850	nA
UVLO						
$V_{UVLO(R)}$	Undervoltage lockout rising threshold	V_{IN} rising, I_{OUT} = 0µA		1.75	1.8	V
$V_{UVLO(F)}$	Undervoltage lockout falling threshold	V_{IN} falling, I_{OUT} = 0µA		1.65	1.7	V
$V_{UVLO(H)}$	Undervoltage lockout hysteresis			100		mV
VSET PIN						
$V_{SET(LKG)}$	VSET input leakage current	T_J = –40°C to 85°C		10	800	nA
$V_{SET(H)}$	VSET high-level detection	Voltage at VSET during startup	1.0			V
R_{SET}	RSET accuracy	T_J = –20°C to 125°C	–4		4	%
R_{SET}	RSET accuracy	T_J = –40°C to 125°C	–3.5		3.5	%
ENABLE						
$V_{EN(R)}$	EN voltage rising threshold	EN rising, enable switching	0.8			V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching			0.4	V
$V_{EN(LKG)}$	EN input leakage current	V_{EN} > 0.8V, T_J = –40°C to 85°C		1	25	nA
$R_{EN;PD}$	EN internal pull-down resistance	EN pin to GND	425	500		kΩ
VOUT VOLTAGE						
V_{OUT}	DC output voltage accuracy	PWM operation, T_J = –20°C to 125°C	–1		+1	%
V_{OUT}	DC output voltage accuracy	PWM operation, T_J = –40°C to 125°C	–1.5		+1.5	%
V_{OUT}	TPSM828436		0.4		0.8	V
	TPSM828437		0.8		1.8	V
	TPSM828438		1.8		3.6	V
$I_{VOS(LKG)}$	VOS input leakage current	TPSM828436, V_{EN} = V_{IN}, V_{VOS} = 0.7V, T_J = –40°C to 85°C			100	nA
		TPSM828437, V_{EN} = V_{IN}, V_{VOS} = 1.2V, T_J = –40°C to 85°C		100	250	nA
		TPSM828438, V_{EN} = V_{IN}, V_{VOS} = 3.3V, T_J = –40°C to 85°C		275	450	nA

6.5 Electrical Characteristics (続き)

T_J = –40°C to +125°C, V_{IN} = 1.8V to 5.5V. Typical values are at T_J = 25°C, V_{IN} = 3.6V and V_{OUT} = 0.7V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SW}		I_{OUT} = 400mA		1.5		MHz
STARTUP						
t_{SS}	TPSM828436 soft-start time	From V_{OUT} = 0% to V_{OUT} = 95% of V_{OUT} nominal		0.45	0.6	ms
	TPSM828438 soft-start time			1.0	1.4	
	TPSM828437 soft-start time			0.7	1.0	
$t_{Startup\_delay}$	EN HIGH to start of switching delay	R2D = GND		330	560	µs
POWER STAGE						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	V_{IN} = 3.6V, I_{OUT} = 300mA		170	260	mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	V_{IN} = 3.6V, I_{OUT} = 300mA		70	115	mΩ
$R_{DROPOUT}$	Dropout resistance high-side MOSFET R_{DSON} + L_{DCR}	V_{IN} = 3.6V, I_{OUT} = 300mA, typ at 25°C		280		mΩ
I_{LKG_SW}	Leakage current into SW-Pin	V_{SW} = 0.7V, T_J = –40°C to 85°C		0	35	nA
I_{LKG_SW}	Leakage current into SW-Pin	V_{SW} = 1.2V, T_J = –40°C to 85°C		0	45	nA
I_{LKG_SW}	Leakage current into SW-Pin	$V_{VIN} > V_{SW}$, V_{SW} = 3.3V, T_J = –40°C to 85°C		0	45	nA
OVERCURRENT PROTECTION						
$I_{HS(OC)}$	High-side peak current limit	$V_{IN} \geqq$ 2.2V	0.9	1.1	1.3	A
$I_{LS(OC)}$	Low-side valley current limit	$V_{IN} \geqq$ 2.2V	0.79	1.0	1.11	A
OUTPUT DISCHARGE						
R_{DSCH_VOS}	Output discharge resistor on VOS pin	V_{EN} = GND, I(VOS) = –10mA		7	22	Ω
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold	Temperature rising		160		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis			20		°C

6.6 Typical Characteristics

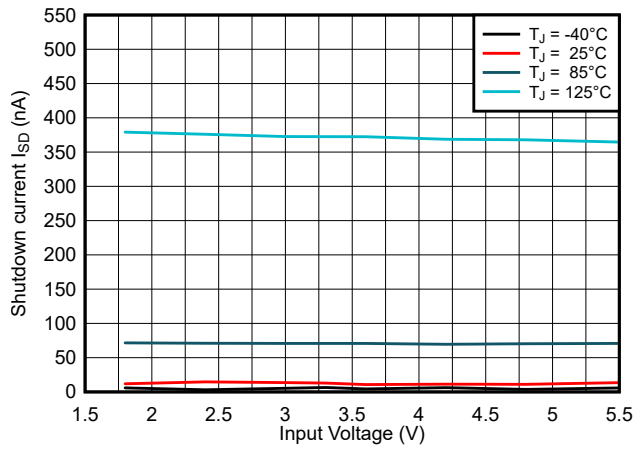


図 6-1. Shutdown Current I_{SD}

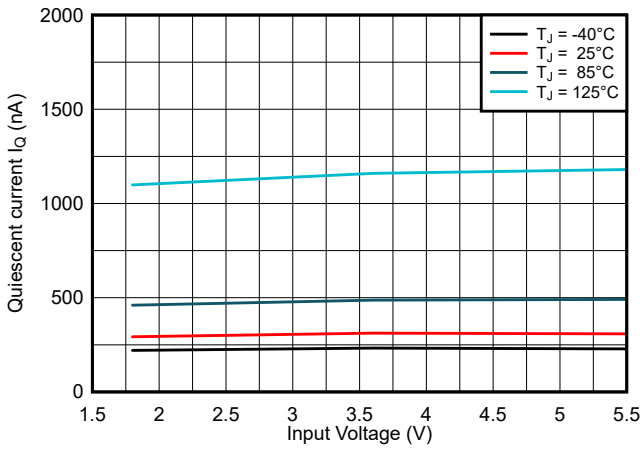


図 6-2. Quiescent Current I_Q

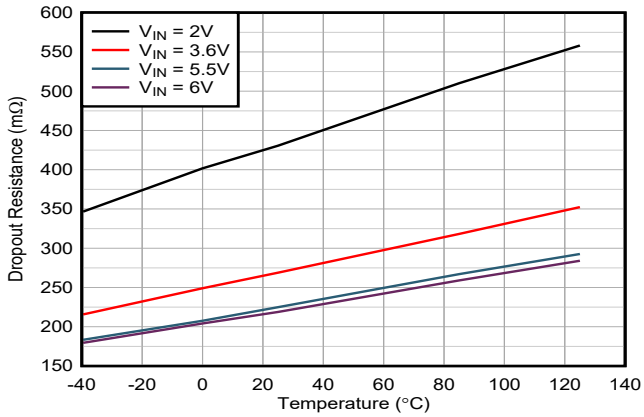


図 6-3. Dropout Resistance $R_{DS(ON)}$

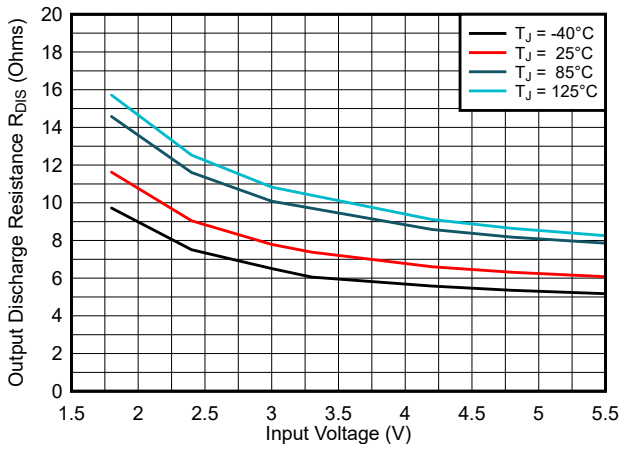


図 6-4. VOS Discharge Switch Drain Source Resistance R_{DIS}

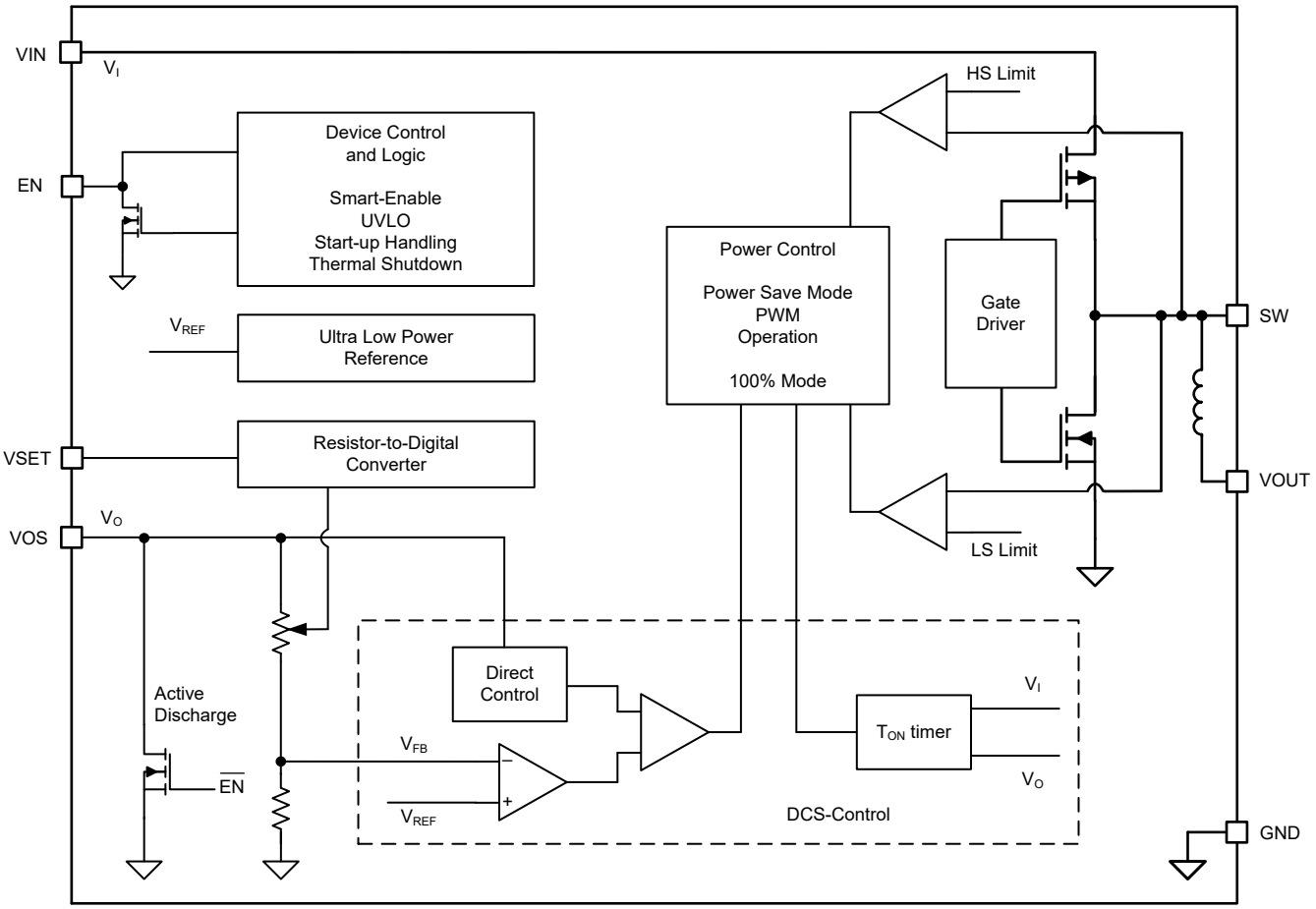
7 Detailed Description

7.1 Overview

The TPSM82843 is a high-frequency, synchronous step-down converter with integrated inductor and ultra-low quiescent current of typically 275nA. The device operates with a 4.7µF input capacitor and 10µF output capacitor over the entire recommended operation range to provide very small design size.

Using TI's DCS-Control topology, the device extends the high efficiency operation area down to microamperes of load current during power saving in Pulse Frequency Modulation (PFM) mode. TI's DCS-Control (Direct Control with Seamless Transition into PFM mode) is an advanced regulation topology that combines the advantages of hysteretic and voltage mode control. Characteristics of DCS-Control are excellent AC load regulation and transient response, low output ripple voltage, and a seamless transition between PFM and Pulse Width Modulation (PWM) mode operation. DCS-Control includes an AC loop that senses the output voltage (VOS pin) and directly feeds the information to a fast comparator stage. This comparator sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To achieve accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low-ESR capacitors.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Smart Enable and Shutdown (EN)

An internal 500kΩ resistor pulls the EN pin to GND and avoids floating the pin. This action prevents an uncontrolled start-up of the device in case the EN pin cannot be driven to low level safely. With EN low, the device is in shutdown mode. The device is turned on with EN set to a high level. The pulldown control circuit disconnects the pulldown resistor on the EN pin after the internal control logic and the reference have been powered up. With EN set to a low level, the device enters shutdown mode and the pulldown resistor is activated again.

7.3.2 Soft Start

After the device has been enabled with EN high, the device initializes and powers up the internal circuits. This action occurs during the regulator start-up delay time, $t_{Startup\_delay}$. After $t_{Startup\_delay}$ expires, the internal soft-start circuitry ramps up the output voltage within the soft-start time, t_{ss}. See 図 7-1.

The start-up delay time, $t_{Startup\_delay}$, varies depending on the selected VSET value. The start-up delay is shortest with VSET = 0 and longest with VSET = 16.

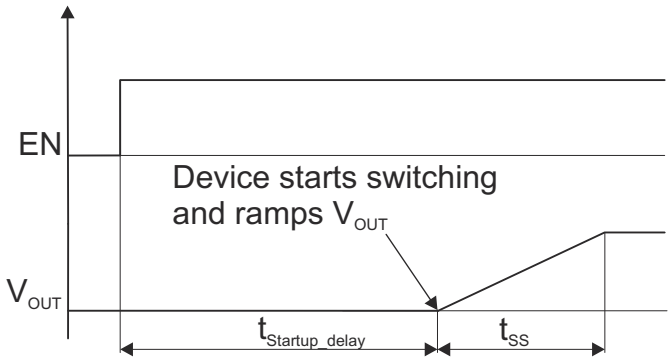


図 7-1. Device Start-Up

7.3.3 VSET Pin: Output Voltage Selection

The output voltage is set with a single external resistor connected between the VSET pin and GND. After the device has been enabled and the control logic as well as the internal reference have been powered up, a R2D (resistor-to-digital) conversion is started to detect the external resistor, R_{SET}, within the regulator start-up delay time, $t_{Startup\_delay}$. An internal current source applies current through the external resistor and an internal ADC reads back the resulting voltage level. Depending on the level, an internal feedback divider network is selected to set the correct output voltage. After this R2D conversion is finished, the current source is turned off to avoid current flow through the external resistor. The circuit can detect resistive values, high-level, low-level, and a pin-open.

For a proper reading, make sure that there is no additional current path or capacitance greater than 30pF total to GND during R2D conversion. Otherwise, the additional current to GND is interpreted as a lower resistor value and a false output voltage is set. 表 7-1 lists the correct resistor values for R_{SET} to set the appropriate output voltages. The R2D converter is designed to operate with resistor values out of the E96 table and requires 1% resistor value accuracy. The external resistor R_{SET} is not a part of the regulator feedback loop and has therefore no impact on the output voltage accuracy. Make sure that there is no other leakage path than the R_{SET} resistor at the VSET pin during an undervoltage lockout event. Otherwise, a false output voltage is set.

表 7-1. Output Voltage Setting

VSET	Output Voltage Setting [V]			R_{SET} [Ω]
	TPSM828436	TPSM828437	TPSM828438	
1	0.400	0.80	1.8	10.0 k
2	0.425	0.85	1.9	12.1 k
3	0.450	0.90	2.0	15.4 k
4	0.475	0.95	2.1	18.7 k
5	0.500	1.00	2.2	23.7 k
6	0.525	1.05	2.3	28.7 k
7	0.550	1.10	2.4	36.5 k
8	0.575	1.15	2.5	44.2 k
9	0.600	1.20	2.6	56.2 k
10	0.625	1.25	2.7	68.1 k
11	0.650	1.30	2.8	86.6 k
12	0.675	1.35	2.9	105.0 k
13	0.700	1.40	3.0	133.0 k
14	0.725	1.45	3.1	162.0 k
15	0.750	1.50	3.2	205.0 k
16	0.775	1.55	3.3	249.0 k or larger
17	0.8	1.6	3.4	VIN
0	1.0	1.8	3.6	GND

7.3.4 Undervoltage Lockout (UVLO)

To avoid misoperation of the device at low input voltages, an undervoltage lockout (UVLO) comparator monitors the supply voltage. The UVLO comparator shuts down the device at an input voltage of 1.7V (maximum) with falling V_{IN}. The device starts at an input voltage of 1.8V (maximum) rising V_{IN}. After the device re-enters operation out of an undervoltage lockout condition, the device behaves like being enabled. The internal control logic is powered up and the external resistor at the VSET pin is read out.

7.3.5 Switch Current Limit, Short-Circuit Protection

The TPSM82843 integrates a current limit on the high-side and low-side MOSFETs to protect the device against overload or short circuit conditions. The current in the switches is monitored cycle by cycle. If the high-side MOSFET current limit, I_{LIMF} trips, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. After the inductor current through the low-side switch decreases beneath the low-side MOSFET current limit, I_{LIMF}, the low-side MOSFET is turned off and the high-side MOSFET turns on again.

7.3.6 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds the thermal shutdown temperature, T_{SD}, of 160°C (typical), the device enters thermal shutdown. Both the high-side and low-side power FETs are turned off. When T_J decreases below the hysteresis amount of typically 20°C, the converter resumes operation, beginning with a soft start to the originally set V_{OUT} (there is no R2D conversion of R_{SET}). The thermal shutdown is not active in power save mode.

7.3.7 Output Voltage Discharge

The purpose of the output discharge function is to make sure of a defined down-ramp of the output voltage when the device is disabled and to keep the output voltage close to 0V.

The internal discharge resistor is connected to the VOS pin. The discharge function is enabled as soon as the device is disabled. The minimum supply voltage required to keep the discharge function active is V_{IN} > V_{TH_UVLO-}.

7.4 Device Functional Modes

7.4.1 Power Save Mode Operation

The DCS-Control topology supports power save mode operation. At light loads, the device operates in PFM (pulse frequency modulation) mode that generates a single switching pulse to ramp up the inductor current and recharge the output capacitor, followed by a sleep period where most of the internal circuits are shut down to achieve the lowest operating quiescent current. During this time, the load current is supported by the output capacitor. The duration of the sleep period depends on the load current and the inductor peak current. During the sleep periods, the current consumption is reduced to typically 275nA. This low quiescent current consumption is achieved by an ultra-low power voltage reference, an integrated high impedance feedback divider network, and an optimized power save mode operation.

In PFM mode, the switching frequency varies linearly with the load current. At medium and high load conditions, the device enters automatically PWM (pulse width modulation) mode and operates in continuous conduction mode with a nominal switch frequency f_{sw} of typically 1.5MHz. The switching frequency in PWM mode is controlled and depends on V_{IN} and V_{OUT}. The boundary between PWM and PFM mode is when the inductor current becomes discontinuous.

If the load current decreases, the converter seamlessly enters PFM mode to maintain high efficiency down to very light loads. Because DCS-Control supports both operation modes within one single building block, the transition from PWM to PFM mode is seamless with minimum output voltage ripple.

7.4.2 100% Mode Operation

The duty cycle of the buck converter operating in PWM mode is given as $D = V_{OUT}/V_{IN}$. The duty cycle increases as the input voltage comes close to the output voltage. In 100% duty cycle mode, the device keeps the high-side switch on continuously. The high-side switch stays turned on as long as the output voltage is below the internal set point. This action allows the conversion of small input to output voltage differences.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The following sections discuss the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

8.2 Typical Application

The following schematics show the typical application circuit for minimal footprint. The TPSM82843 has been designed to accommodate output capacitance values from 4µF (effective) to 25µF (effective). The output capacitance has influence on the application curves, especially light load efficiency and load step. A smaller output capacitance causes a higher switching frequency and lower efficiency at equal light load. This outcome can help however keeping the switching frequency out of the audio band. This outcome also results in a larger voltage change during load transients while a larger capacitance reduces the voltage change. The application curves have been taken with 10µF output capacitor which is equivalent to an effective capacitance of 8µF at V_{OUT} of 1.2V with the output capacitor type in the BOM table.

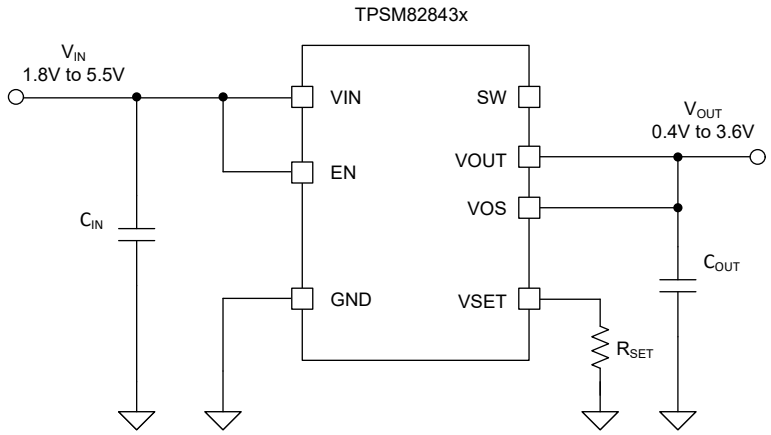


図 8-1. TPSM82843 Typical Application Circuit

8.2.1 Design Requirements

The following table shows the list of components for the application circuit and the characteristic application curves.

表 8-1. Components for Application Characteristic Curves

Reference	Description	Value	Size Code Inch [Metric L × W × T]	Manufacturer
TPSM828436, TPSM828437, TPSM828438	275nA-I_Q buck converter module		[2.45mm × 2.7mm × 1.29mm]	TI
C_{IN}	Ceramic capacitor GRM155R60J475ME47D	4.7µF	0402 [1.0mm × 0.5mm × 0.5mm]	Murata
C_{OUT}	Ceramic capacitor GRM155R60J106ME15D	10µF	0402 [1.0mm × 0.5mm × 0.5mm]	Murata
R_{SET}	See voltage setting table		0402 [1.0mm × 0.5mm × 0.5mm]	

8.2.2 Detailed Design Procedure

Follow the passive component selection per the typical application circuit.

8.2.3 Application Curves

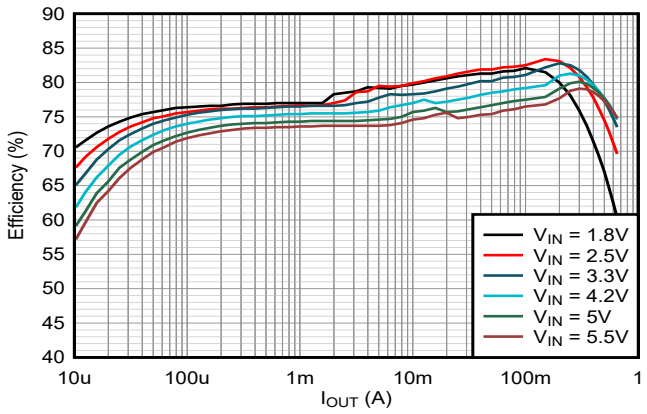


図 8-2. Efficiency at 0.4 V_{OUT} and 25°C

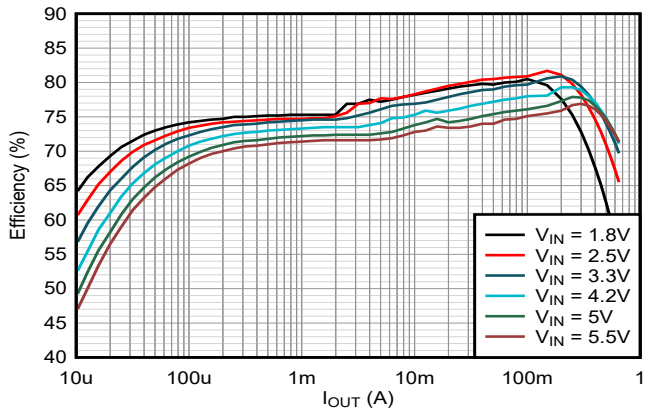


図 8-3. Efficiency at 0.4 V_{OUT} and 85°C

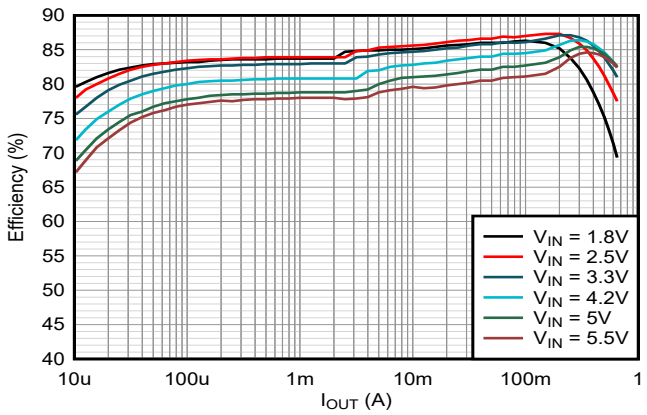


図 8-4. Efficiency at 0.7 V_{OUT} and 25°C

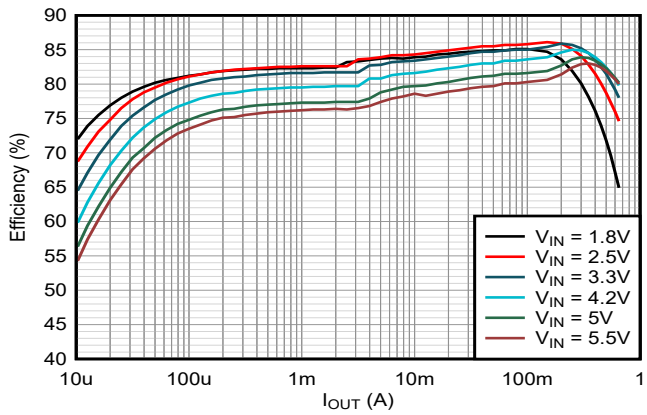


図 8-5. Efficiency at 0.7 V_{OUT} and 85°C

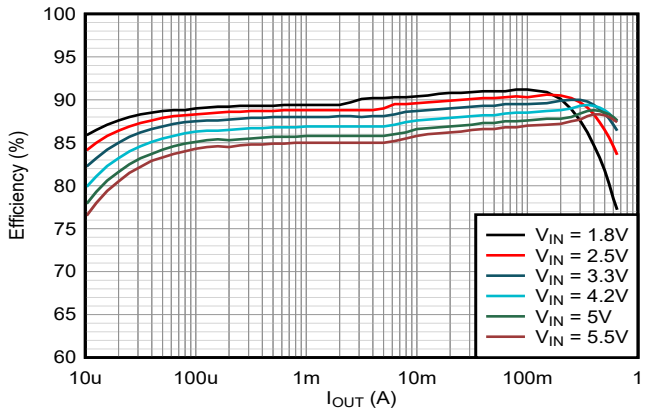


図 8-6. Efficiency at 1.2 V_{OUT} and 25°C

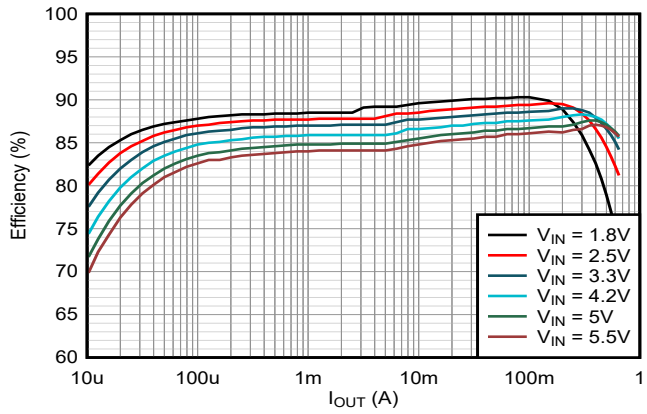


図 8-7. Efficiency at 1.2 V_{OUT} and 85°C

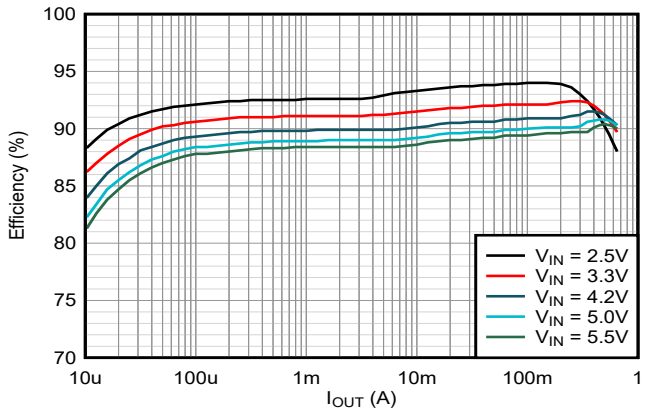


図 8-8. Efficiency at 1.8 V_{OUT} and 25°C

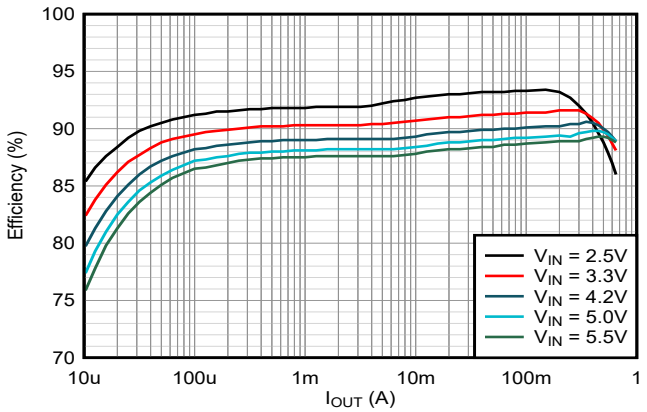


図 8-9. Efficiency at 1.8 V_{OUT} and 85°C

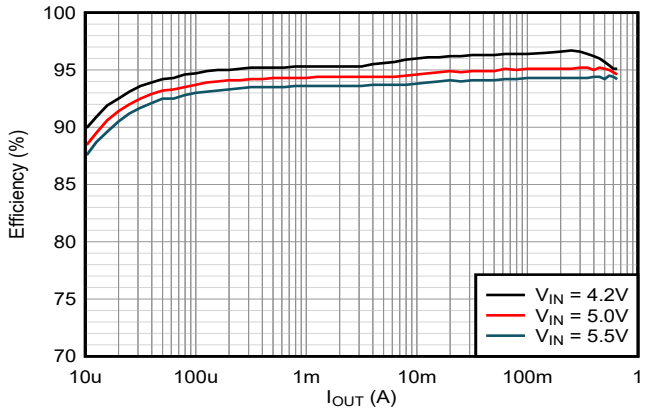


図 8-10. Efficiency at 3.6 V_{OUT} and 25°C

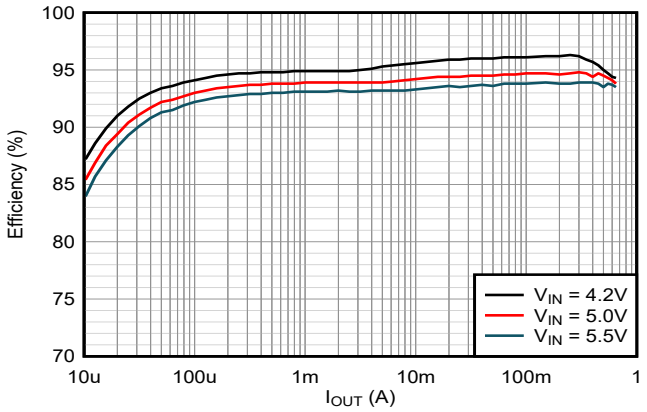


図 8-11. Efficiency at 3.6 V_{OUT} and 85°C

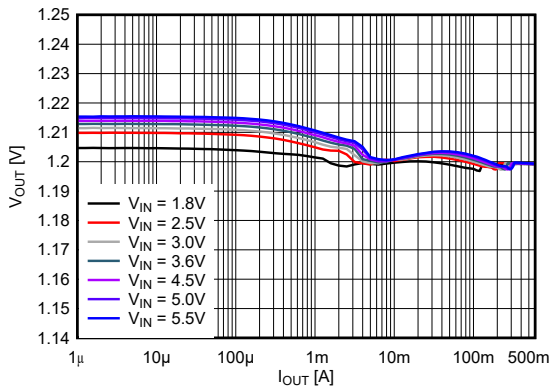


図 8-12. Output Voltage vs Output Current at 1.2 V_{OUT}

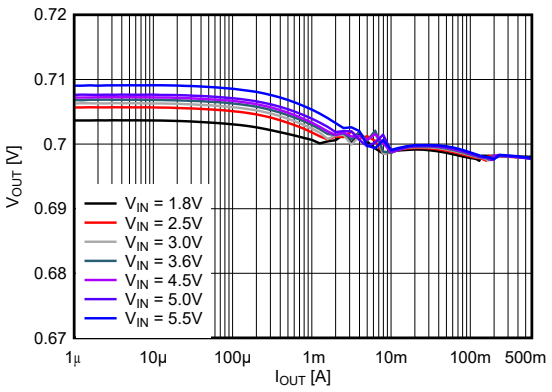


図 8-13. Output Voltage vs Output Current at 0.7 V_{OUT}

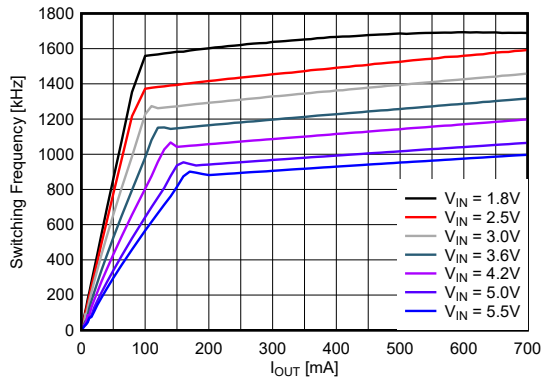


図 8-14. Switching Frequency vs Output Current at 0.4 V_{OUT}

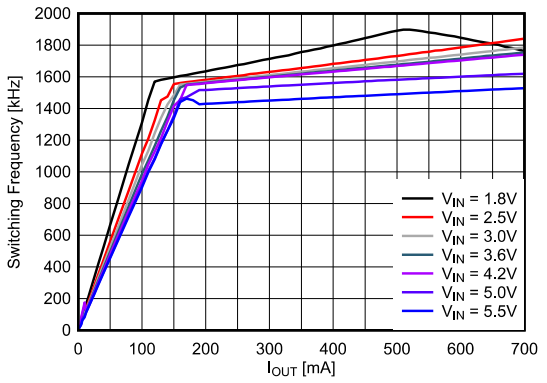


図 8-15. Switching Frequency vs Output Current at 0.7 V_{OUT}

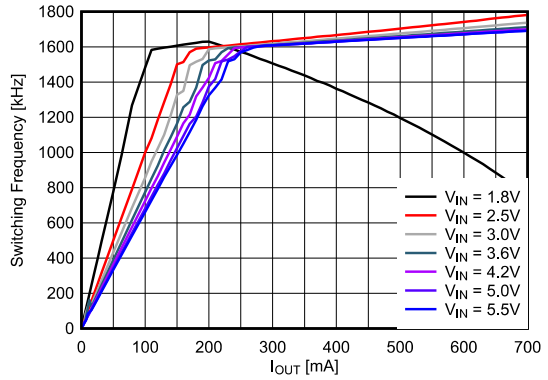


図 8-16. Switching Frequency vs Output Current at 1.2 V_{OUT}

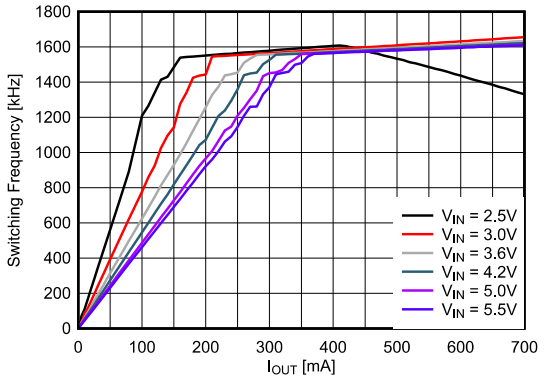


図 8-17. Switching Frequency vs Output Current at 1.8 V_{OUT}

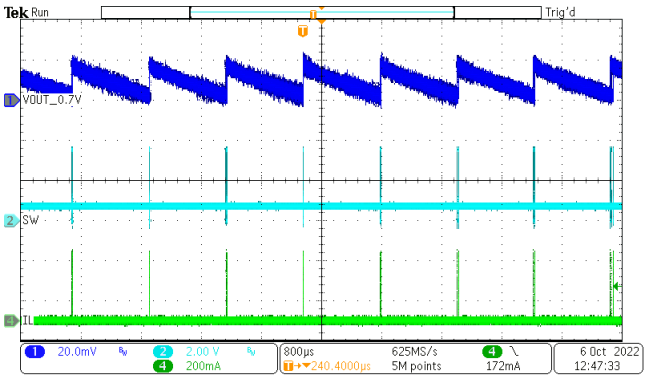


図 8-18. Typical Operation at 0.7 V_{OUT}, 100 µA I_{OUT}

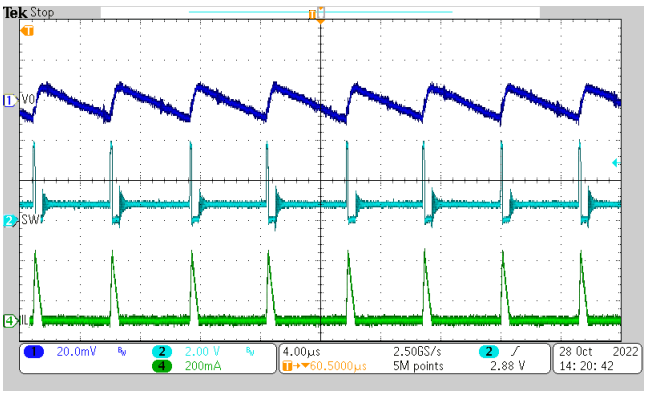


図 8-19. Typical Operation at 0.7 V_{OUT}, 20 mA I_{OUT}

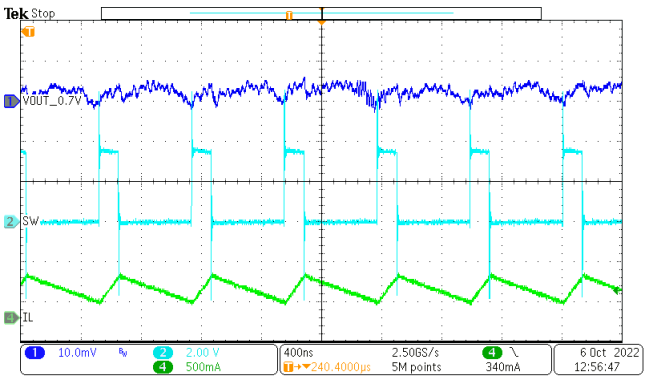


図 8-20. Typical Operation at 0.7 V_{OUT}, 400 mA I_{OUT}

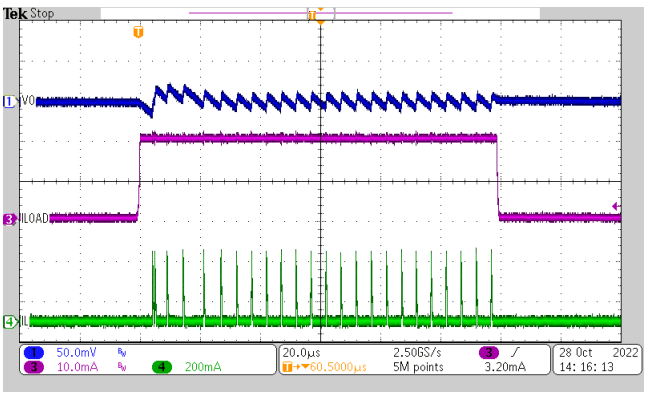


図 8-21. Load Transient at 0.7 V_{OUT}, I_{OUT} = 100µA to 20mA

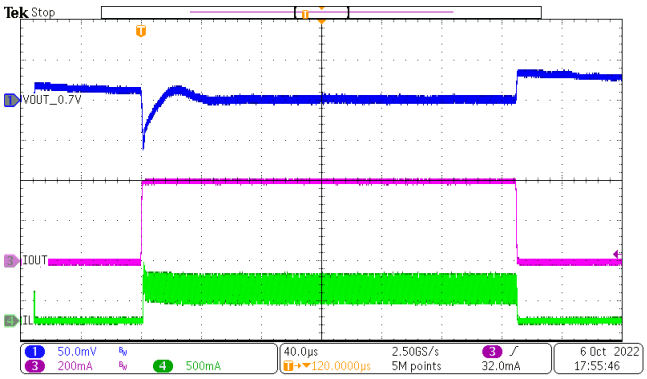


図 8-22. Load Transient at 0.7 V_{OUT}, I_{OUT} = 100µA to 400mA

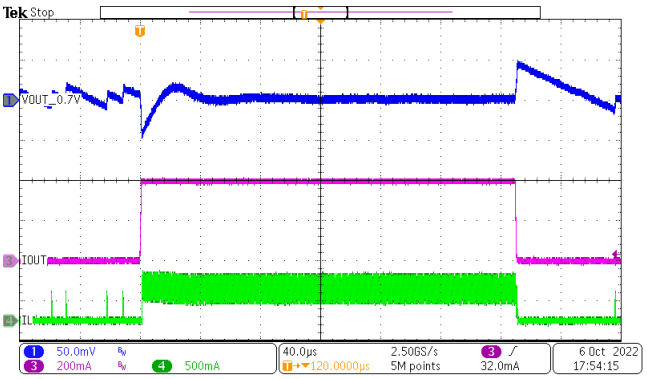


図 8-23. Load Transient at 0.7 V_{OUT}, I_{OUT} = 5mA to 400mA

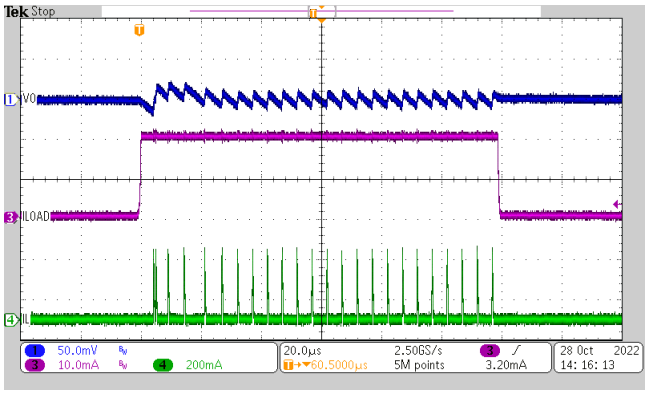


図 8-24. Load Transient at 1.2 V_{OUT}, I_{OUT} = 100µA to 20mA

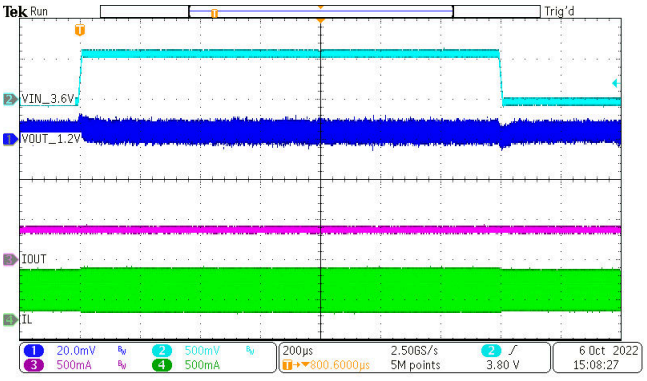


図 8-25. Load Transient at 1.2 V_{OUT}, I_{OUT} = 100µA to 400mA

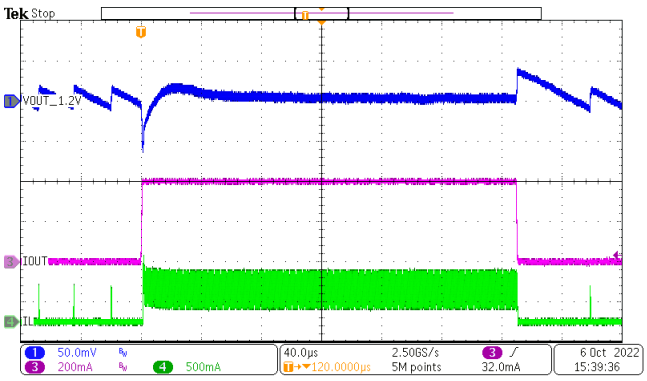


図 8-26. Load Transient at 1.2 V_{OUT}, I_{OUT} = 5mA to 400mA

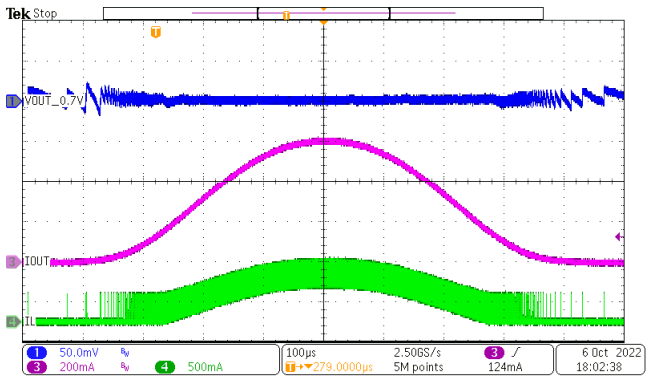


図 8-27. AC Load Sweep at 0.7 V_{OUT}, I_{OUT} = 1mA to 600mA

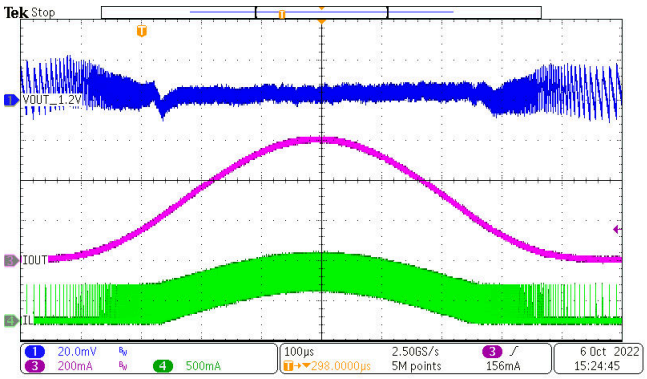


図 8-28. AC Load Sweep at 1.2 V_{OUT}, I_{OUT} = 1mA to 600mA

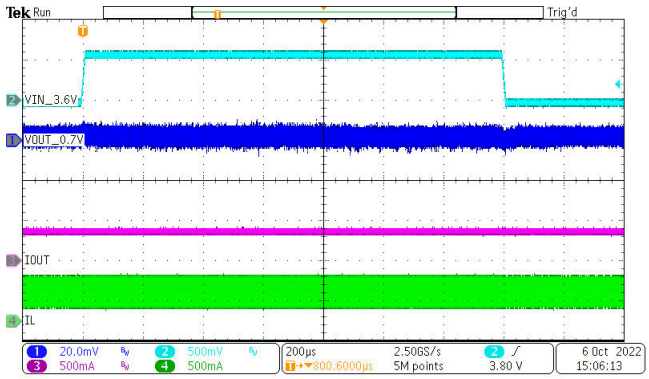


図 8-29. Line Transient at 0.7 V_{OUT}, I_{OUT} = 400mA, V_{IN} = 3.6V to 4.2V

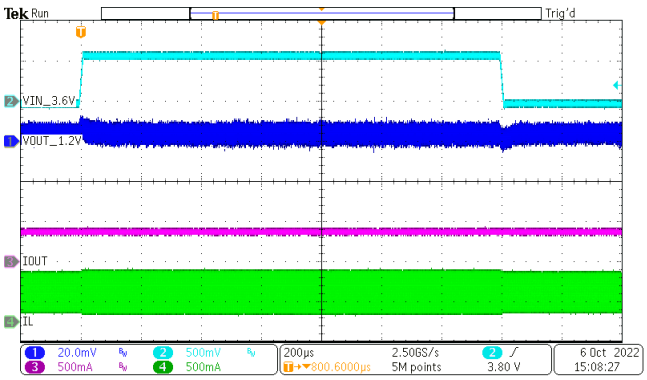


図 8-30. Line Transient at 1.2 V_{OUT}, I_{OUT} = 400mA, V_{IN} = 3.6V to 4.2V

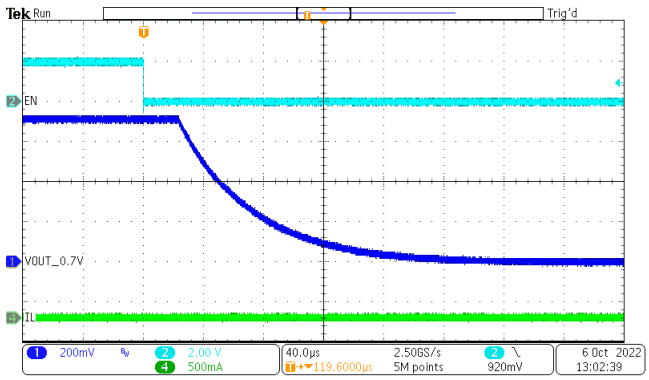


図 8-31. Shutdown, Output Discharge at 0.7 V_{OUT}

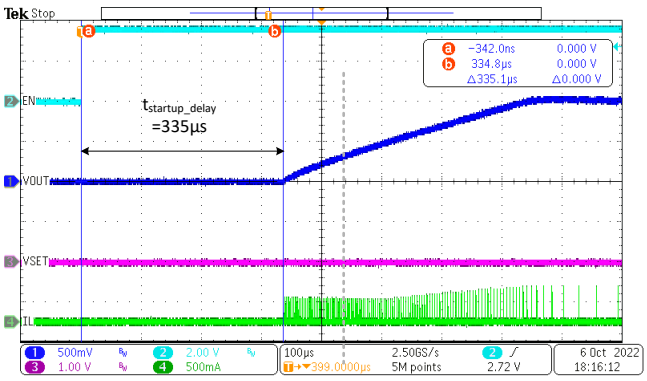


図 8-32. Start-Up Delay Time, VSET = GND

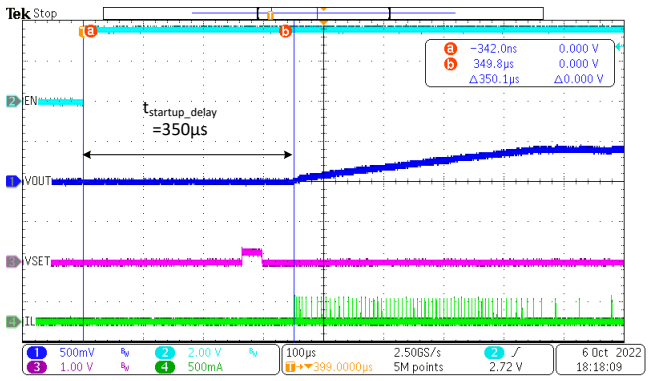


図 8-33. Start-Up Delay Time, VSET = 10kohms

8.3 Power Supply Recommendations

The power supply must provide a current rating according to the supply voltage, output voltage, and output current of the TPSM82843.

8.4 Layout

8.4.1 Layout Guidelines

The pinout of TPSM82843 has been designed to enable a single top layer PCB routing of the IC and the critical passive components such as CIN, COUT, and VSET resistor. Furthermore, this pinout allows the user to connect tiny components such as 0201 (0603 metric) size capacitors and resistors. As for all switching power supplies, the layout is an important step in the design. Care must be taken in board layout to get the specified performance. Providing a low inductance, low impedance ground path is critical. Therefore, use wide and short traces for the main current paths. Place the input capacitor as close as possible to the VIN of the IC and GND pins. This placement is the most critical component placement. Then place the output capacitor without via as close as possible to the VOUT and GND pin as shown in the following layout diagram. The VOS line is a sensitive, high impedance input and must be connected to the output capacitor with a direct trace from the output capacitor solder pad to the device pin. The VOS line must stay away from noisy components and traces (for example, the SW line) or other noise sources. For bode measurements in the evaluation board, a via is placed on the trace to allow connection of a 10Ohm resistor between the capacitor pad and VOS on the bottom side of the PCB. The connection between capacitor pad and via must be cut for this measurement. For the final circuit, no vias can be present and all capacitors must be placed on the top layer.

8.4.2 Layout Example

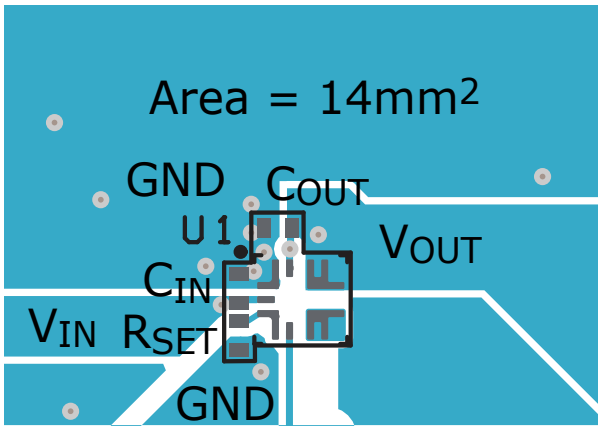


図 8-34. Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

9.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
Bluetooth® is a registered trademark of Bluetooth Special Interest Group (SIG).
Wi-Fi® is a registered trademark of Wi-Fi Alliance.
すべての商標は、それぞれの所有者に帰属します。

9.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (September 2024) to Revision A (November 2024)	Page
• ドキュメントのステータスを「事前情報」から「量産データ」に変更	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPSM828436VCFR	ACTIVE	QFN-FCMOD	VCF	7	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	88436	Samples
TPSM828437VCFR	ACTIVE	QFN-FCMOD	VCF	7	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	88437	Samples
TPSM828438VCFR	ACTIVE	QFN-FCMOD	VCF	7	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	88438	Samples
XPSM828437VCFR	ACTIVE	QFN-FCMOD	VCF	7	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

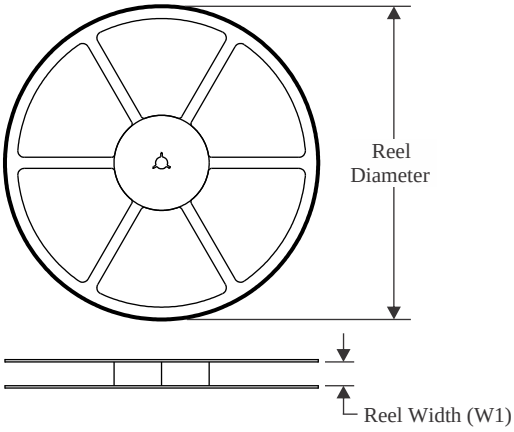
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

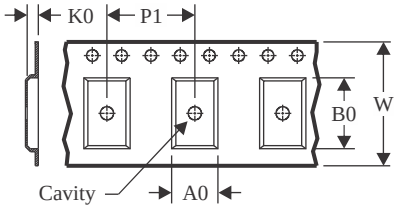
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

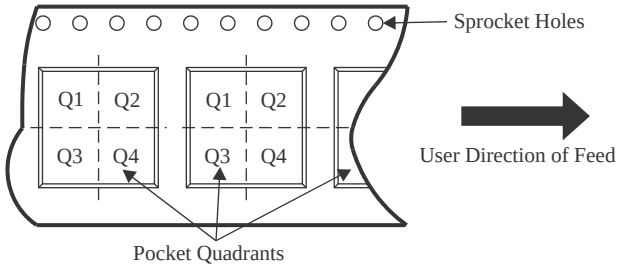


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

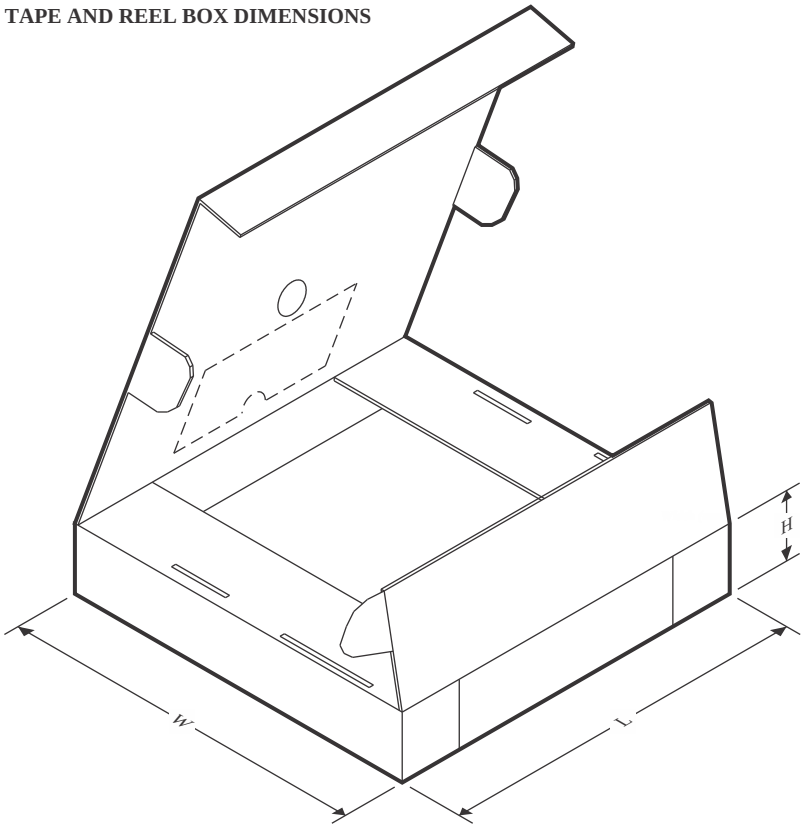
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM828436VCFR	QFN-FCMOD	VCF	7	3000	330.0	12.4	2.75	3.0	1.5	8.0	12.0	Q1
TPSM828437VCFR	QFN-FCMOD	VCF	7	3000	330.0	12.4	2.75	3.0	1.5	8.0	12.0	Q1
TPSM828438VCFR	QFN-FCMOD	VCF	7	3000	330.0	12.4	2.75	3.0	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

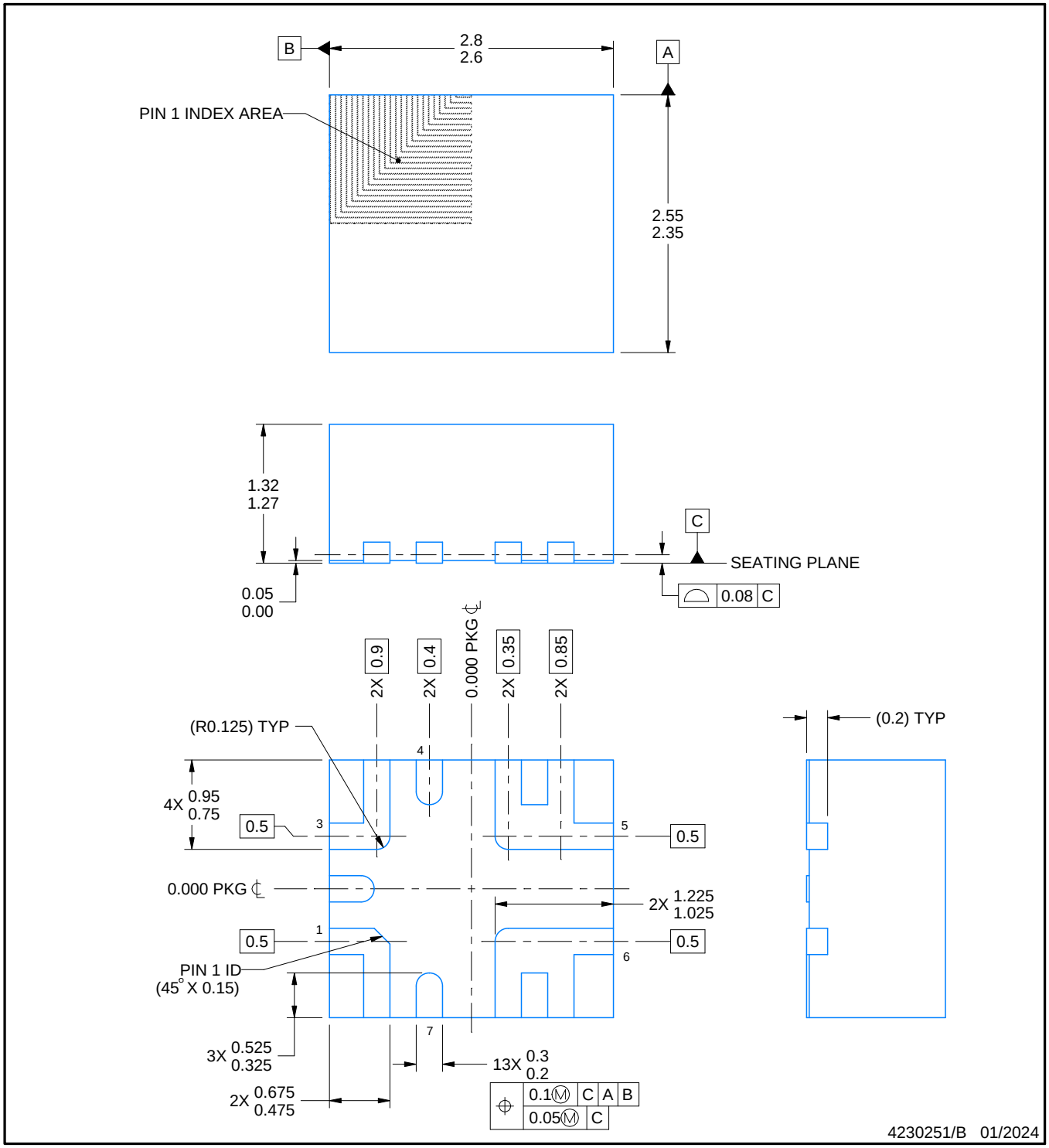
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM828436VCFR	QFN-FCMOD	VCF	7	3000	367.0	367.0	38.0
TPSM828437VCFR	QFN-FCMOD	VCF	7	3000	367.0	367.0	38.0
TPSM828438VCFR	QFN-FCMOD	VCF	7	3000	367.0	367.0	38.0

PACKAGE OUTLINE

VCF0007A

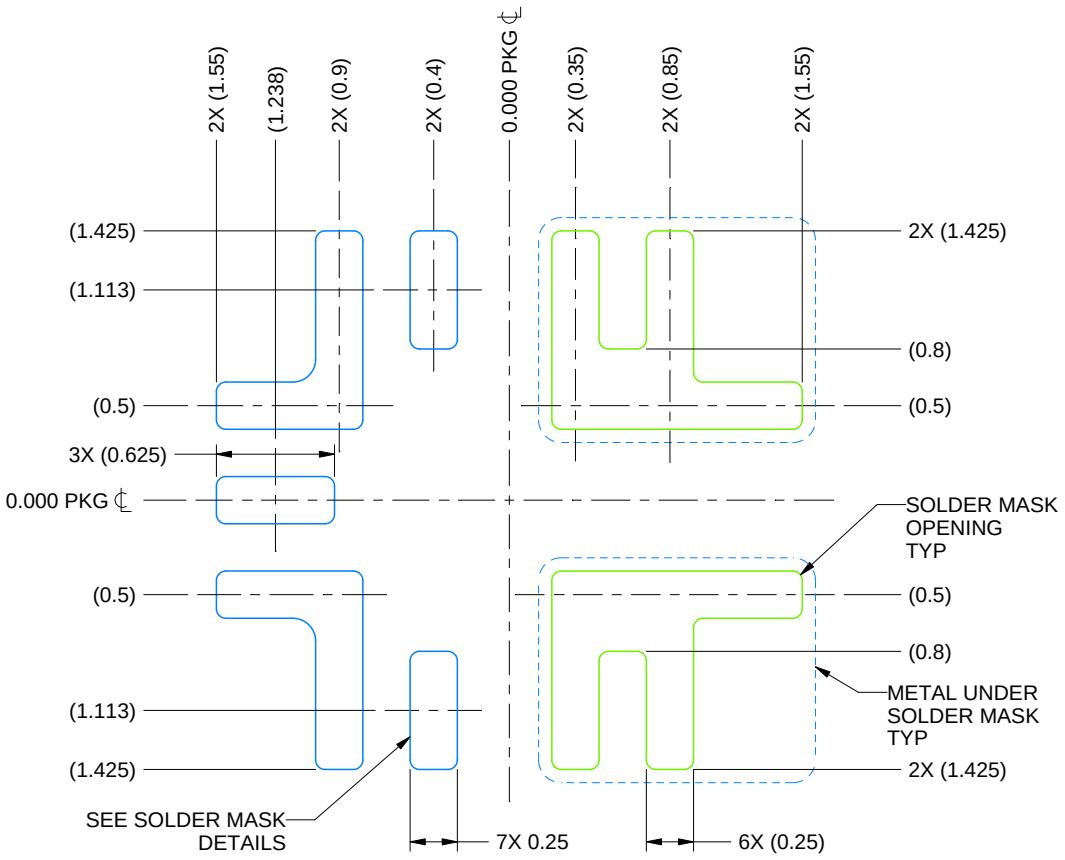
QFN-FCMOD - 1.32 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

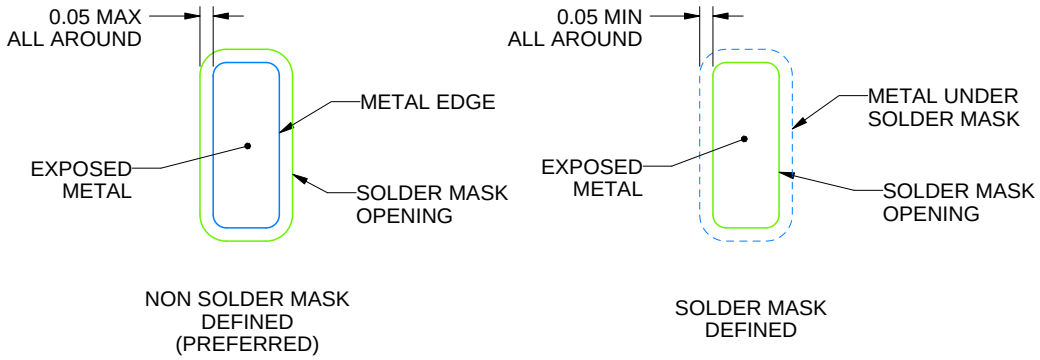


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE: 25X



SOLDER MASK DETAILS

4230251/B 01/2024

NOTES: (continued)

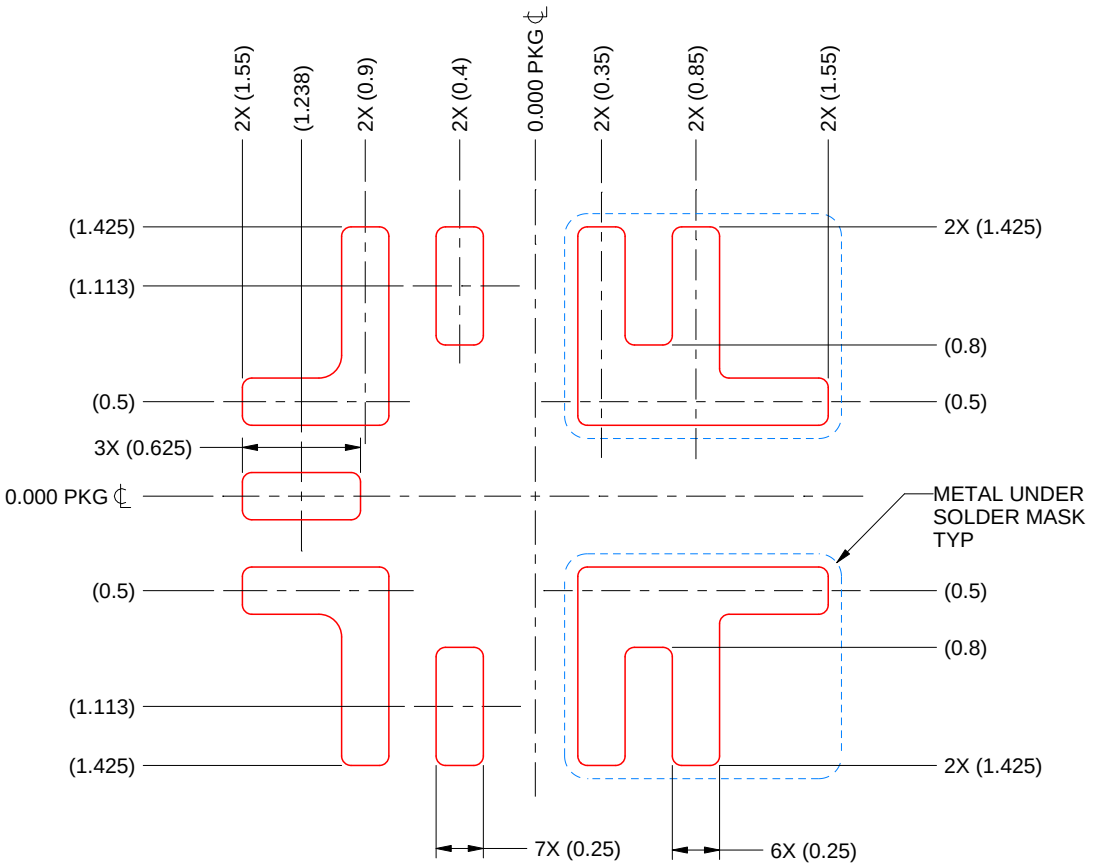
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

VCF0007A

QFN-FCMOD - 1.32 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE 25.000

4230251/B 01/2024

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265