TPSM8287A1xM 2.7V～6V 入力、12A および 15A、並列接続可能な降圧パワー モジュール、I²C インターフェイスとリモート センス機能搭載、-55°C動作可能

1 特長

- –55°C～125°Cの動作温度範囲
- ±1.0% の出力電圧精度
- 差動リモート センシング
- マルチフェーズ動作向けの並列接続が可能
- スタートアップ時の出力電圧は、VSETx ピンにより 0.40V～3.35V の範囲で 50mV 刻みで選択可能、また、I²C により 1.25mV 刻みで調整可能
- VSETx ピンを介して 5 つの I²C アドレスを選択可能
- 可変外部補償により、広い出力コンデンサ範囲と最適化された過渡応答を実現
- 低 EMI 要件向けの設計
  - ボンド ワイヤ パッケージなし
  - 内部入力コンデンサ
  - 並列入力パスによるレイアウトの簡略化
  - 外部クロックへの同期またはスペクトラム拡散動作を選択可能
- パワー セーブ モードまたは強制 PWM 動作
- 高精度のイネーブル入力スレッショルド
- ウィンドウ コンパレータによるパワー グッド出力
- アクティブ出力放電
- 優れた放熱対策
- 4.5mm × 6.8mm、0.5mm ピッチの小型 QFN パッケージ
- 77mm² の設計サイズ

2 アプリケーション

- 航空機の電源
- 防衛無線
- 追尾フロント エンド
- レーダー
- 鉄道輸送

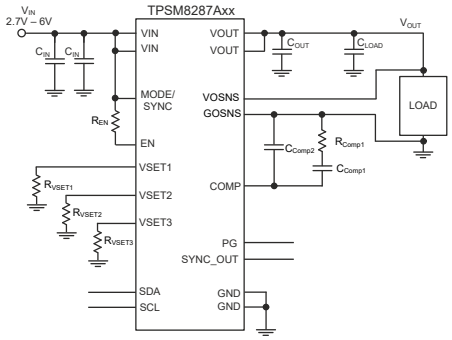
3 概要

TPSM8287A1xM は、差動リモート センシングと I²C インターフェイスを搭載したピン互換の降圧 DC/DC パワー モジュールのファミリです。この電源モジュールには同期整流降圧コンバータ、インダクタ、入力コンデンサが組み込まれているため、設計の簡素化、外付け部品の低減、PCB 面積の削減が可能です。薄く小型に設計されているので、標準的な表面実装機による組み立てが可能です。TPSM8287A1xM ファミリは、高速過渡をサポートする拡張制御方式を実装しています。TPSM8287A1xM は、固定周波数モードまたはパワー セーブ モードで動作可能です。リモート センシング機能により、ポイント オブ ロードでの電圧レギュレーションが最適化され、デバイスは温度範囲全体にわたって ±1.0% の DC 電圧精度を達成します。これらのデバイスをスタック モードまたは並列モードで動作させることで、大出力電流を供給することや、電力散逸を複数のデバイスに分散することが可能です。I²C 互換インターフェイスにより、複数の制御、監視、警告機能を備えています。VSETx ピンによりスタートアップ電圧を選択できるため、アクティブな I²C 通信がなくても起動できます。

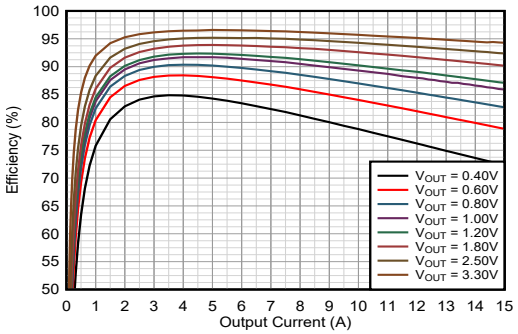
製品情報

部品番号(1)	電流定格	パッケージ(2)	パッケージの高さ
TPSM8287A12BAM	12A	RDV (B0QFN、39)	1.8mm
TPSM8287A12BBM	12A		
TPSM8287A15BAM	15A	RDW (B3QFN、39)	4.0mm
TPSM8287A15BBM	15A		

(1) 「デバイスのオプション」表を参照してください。
(2) 詳細については、セクション 12 を参照してください。



TPSM8287A1xM の概略回路図



効率性 TPSM8287A15BAM (V_{IN} = 5.0V、FPWM)

Table of Contents

4 Device Options

表 4-1. Devices With I²C Interface

ORDERABLE PART NUMBER(1)	OUTPUT CURRENT	NOMINAL INDUCTANCE	OPERATING FREQUENCY	PACKAGE HEIGHT
TPSM8287A12BAMRDVT	12A	100nH ± 20%	1.5MHz	1.8mm
TPSM8287A12BBMRDVT	12A	100nH ± 20%	2.25MHz	
TPSM8287A15BAMRDWT	15A	150nH ± 20%	1.5MHz	4.0mm
TPSM8287A15BBMRDWT	15A	150nH ± 20%	2.25MHz	

(1) For all available packages, see the orderable addendum at the end of the data sheet.

5 Pin Configuration and Functions

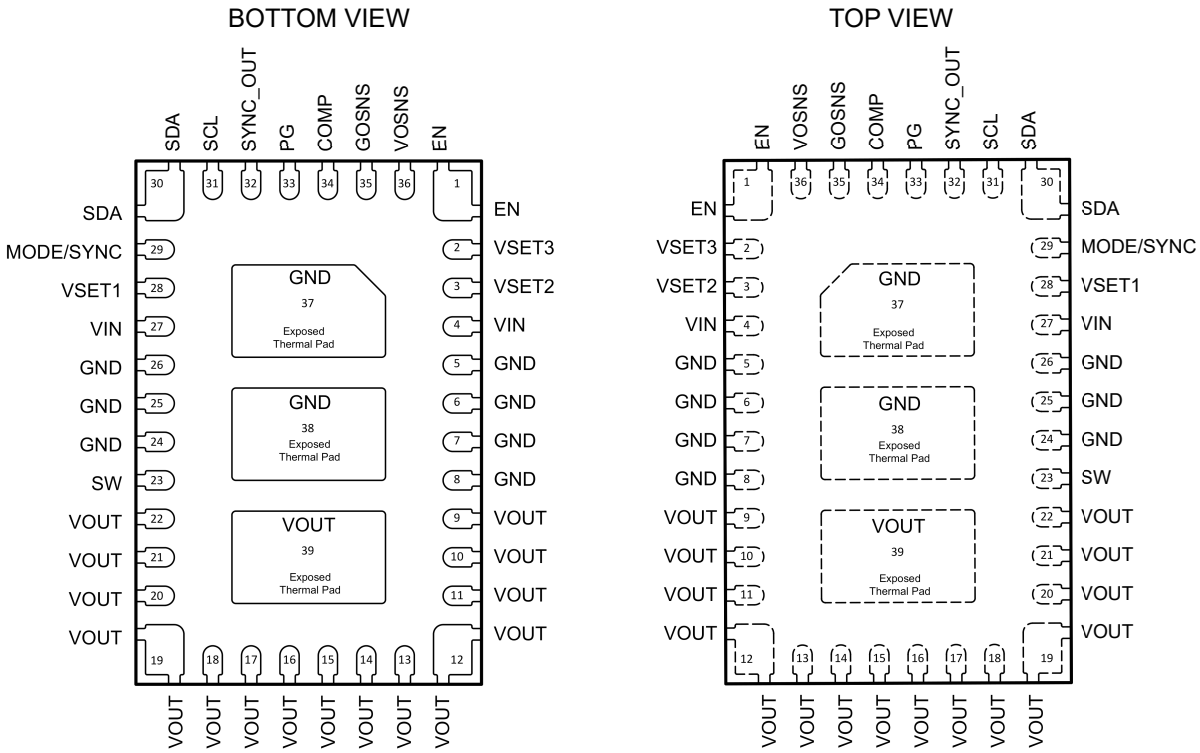


図 5-1. TPSM8287A1xM RDV and RDW Package, B0QFN 39 Pin

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
35	GOSNS	I	Output ground sense (differential output voltage sensing). Connect at the load.
36	VOSNS	I	Output voltage sense (differential output voltage sensing). Connect at the load.
1	EN	I	This pin is the enable pin of the device. The user must connect to this pin using a series resistor of at least 15kΩ. A low logic level on this pin disables the device, and a high logic level on this pin enables the device. Do not leave this pin unconnected. For stacked operation, connect the EN pins of all stacked devices together with a resistor to the supply voltage or a GPIO of a processor. See *Stacked Operation* for a detailed description.
4, 27	VIN	P	Power supply input. Connect an input capacitor as close as possible between each VIN and GND (on both sides of the package).
5, 6, 7, 8, 24, 25, 26	GND	GND	Ground pin
9 - 22	VOUT	P	Output voltage pin
23	SW	O	This pin is the switch pin of the converter and is connected to the internal Power MOSFETs. This pin can be left floating.

表 5-1. Pin Functions (続き)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
33	PG	I/O	Open-drain power-good output with window comparator. This pin is pulled to GND while VOUT is outside the power-good threshold. This pin can be left open or tied to GND if not used in single device operation. A pullup resistor can be connected to any voltage not larger than 6.5V. In stacked operation, connect the PG pins of all stacked devices together. Only the PG pin of the primary converter in stacked operation is an open drain output. For devices that are defined as secondary converters in stacked mode, the pin is an input pin. See *Stacked Operation* for a detailed description.
29	MODE/SYNC	I	The device runs in power save mode when this pin is pulled low. If the pin is pulled high, the device runs in forced-PWM mode. If unused, this pin can be left floating and an internal pulldown resistor pulls the pin low. The pin can also be used to synchronize the device to an external clock. See *セクション 7.3.8* for a detailed description.
30	SDA	I/O	I^2C serial data pin. Do not leave floating. Connect a pullup resistor to a logic high level. For secondary devices in stacked operation, or if the I^2C interface is not used, connect the pin to GND.
31	SCL	I	I^2C serial clock pin. Do not leave this pin floating. Connect a pullup resistor to a logic high level. For secondary devices in stacked operation, or if the I^2C interface is not used, connect the pin to GND.
32	SYNC_OUT	I/O	Internal clock output pin for synchronization in stacked mode. Leave this pin floating for single device operation. Connect this pin to the MODE/SYNC pin of the next device in the daisy-chain in stacked operation. *Do not use this pin to connect to a non-TPSM8287A1xM device.* During start-up, this pin is used to identify if a device must operate as a secondary converter in stacked operation. Connect a 47kΩ resistor from this pin to GND to define a secondary converter in stacked operation. See *Stacked Operation* for a detailed description.
28	VSET1	I/O	Start-up output voltage and I^2C address selection pin. A resistor or short circuit to GND or V_{IN} defines the selected output voltage and I^2C address. See 表 7-2.
3	VSET2	I/O	
2	VSET3	I/O	
34	COMP	I/O	Device compensation input. A resistor and capacitor from this pin to GOSNS define the compensation of the control loop. In stacked operation, connect the COMP pins of all stacked devices together and connect a resistor and capacitor between the common COMP node and GOSNS.
37, 38	GND Exposed Thermal Pad	—	The thermal pad must be soldered to GND to achieve an appropriate thermal resistance and for mechanical stability.
39	VOUT Exposed Thermal Pad	—	The thermal pad must be soldered to VOUT to achieve an appropriate thermal resistance and for mechanical stability.

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	VIN, VSET1, VSET2, VSET3, PG, EN, MODE/SYNC	–0.3	6.5	V
	SW (DC), VOUT	–0.3	V_{IN} + 0.3	
	SW (AC, less than 10ns)(3)	–3	10	
	COMP	–0.3	V_{IN}	
	VOSNS	–0.3	3.8	
	GOSNS	–0.3	0.3	
	SCL, SDA	–0.3	5.5	
	SYNC_OUT	–0.3	2	
Current	SYNC_OUT, COMP	–1	1	mA
	SDA		9	
	EN		0.5	
	PG		10	
T_J	Junction temperature	–55	125	°C
T_{stg}	Storage temperature	–55	125	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the GND pin.
(3) While switching.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	VIN	2.7		6	V
		SDA, SCL	0		5	
V_{OUT}	Output voltage	VOUT	0.4		3.35V or (V_{IN} – 1.4V)(1)	V
I_{OUT}	Output current(3)	TPSM8287A12BAM, TPSM8287A12BBM			12	A
		TPSM8287A15BAM, TPSM8287A15BBM			15	
I_{SINK_PG}	Sink current at PG pin				10	mA
C_{IN}	Input capacitance (per pin)(2)	VIN	5	10		µF
C_{OUT}	Output capacitance(2)	TPSM8287A12BAM, TPSM8287A15BAM	60		(4)	
C_{OUT}	Output capacitance(2)	TPSM8287A12BBM, TPSM8287A15BBM	40		(4)	
R_{VSET}	Resistor value	VSET1, VSET2, VSET3	37.6	47	56.4	kΩ
R_{SYNC_OUT}	Resistor value	SYNC_OUT	37.6	47	56.4	kΩ
C_{PAR}	Parasitic capacitance	VSET1, VSET2, VSET3			100	pF
		SYNC_OUT			20	

6.3 Recommended Operating Conditions (続き)

			MIN	NOM	MAX	UNIT
T_J	Operating junction temperature		–55		125	°C

(1) Whichever value is lower.
(2) *Effective* capacitance.
(3) In stacked operation, the maximum output current per phase can be reduced. See Stacked Operation for details.
(4) The maximum recommended output capacitance depends on the specific operating conditions of an application. Output capacitance values up to a few mF are typically possible, however.

6.4 Thermal Information

THERMAL METRIC(1)		TPSM8287AxxM				UNIT
		39 PINS				
		RDV JEDEC 51-5	RDW JEDEC 51-5	RDV EVM	RDW EVM	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.6	30.4	19.5	20.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.7	52.3	n/a(2)	n/a(2)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.1	9.8	n/a(2)	n/a(2)	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5.1	6.1	3.1	6.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	10.0	9.6	8.8	9.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.3	6.2	n/a(2)	n/a(2)	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) Not applicable to an EVM.

6.5 Electrical Characteristics

T_J = –55°C to 125°C, and V_{IN} = 2.7V to 6V. Typical values at V_{IN} = 3.3V and T_J = 25°C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_{Q_VIN}	Quiescent current (VIN)	EN = high, I_{OUT} = 0mA, $V_{(SW)}$ = 0V, SINGLE=1, MODE/SYNC = low, device not switching, T_J = 25°C		1.5	3	mA
I_{SD}	Shutdown current (VIN)	EN = low, $V_{(SW)}$ = 0V, T_J = 25°C		16.5	40	µA
$V_{IT+(UVLO)}$	Positive-going UVLO threshold voltage (VIN)		2.5	2.6	2.7	V
$V_{IT–(UVLO)}$	Negative-going UVLO threshold voltage (VIN)		2.4	2.5	2.6	V
$V_{hys(UVLO)}$	UVLO hysteresis voltage (VIN)		90			mV
$V_{IT+(OVLO)}$	Positive-going OVLO threshold voltage (VIN)		6.1	6.3	6.5	V
$V_{IT–(OVLO)}$	Negative-going OVLO threshold voltage (VIN)		6.0	6.2	6.4	V
$V_{hys(OVLO)}$	OVLO hysteresis voltage (VIN)		85			mV
$V_{POR–}$	Negative-going power-on reset (POR) threshold (VIN)		1.4			V
T_{SD}	Thermal shutdown threshold temperature	T_J rising		170		°C
	Thermal shutdown hysteresis			20		°C
T_W	Thermal warning threshold temperature	T_J rising		150		°C
	Thermal warning hysteresis			20		°C
CONTROL and INTERFACE						

6.5 Electrical Characteristics (続き)

T_J = –55°C to 125°C, and V_{IN} = 2.7V to 6V. Typical values at V_{IN} = 3.3V and T_J = 25°C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage (EN)		0.97	1.0	1.03	V
$V_{IT–}$	Negative-going input threshold voltage (EN)		0.87	0.9	0.93	V
V_{hys}	Hysteresis voltage (EN)		95			mV
I_{IH}	High-level input current (EN)	V_{EN} = V_{IN}, internal pulldown resistor disabled			200	nA
I_{IL}	Low-level input current (EN)	V_{EN} = 0V, internal pulldown resistor disabled	–200			nA
V_{IH}	High-level input voltage (SDA, SCL, MODE/SYNC)		0.8			V
V_{IL}	Low-level input voltage (SDA, SCL, MODE/SYNC)				0.4	V
V_{OL}	Low-level output voltage (SDA)	I_{OL} = 9mA			0.4	V
		I_{OL} = 5mA			0.2	V
I_{LKG}	Input leakage current into SDA, SCL	V_{OH} = 3.3V			200	nA
I_{IL}	Low-level input current (MODE/SYNC)	$V_{MODE/SYNC}$ = 0V	–150		150	nA
I_{IH}	High-level input current (MODE/SYNC)	$V_{MODE/SYNC}$ = V_{IN}			3	µA
$t_{d(EN)1}$	Enable delay time when EN tied to V_{IN}	Measured from when EN goes high to when device starts switching SR_{VIN} = 1V/µs		210	535	µs
$t_{d(EN)2}$	Enable delay time when V_{IN} already applied	Measured from when EN goes high to when device starts switching		40	100	µs
$t_{d(RAMP)}$	Output voltage ramp time	Measured from when device starts switching to rising edge of PG. Selectable with I^2C. See Table 8-5.	0.46	0.54	0.62	ms
			0.88	1.04	1.20	ms
			1.73	2.04	2.35	ms
			3.43	4.04	4.65	ms
T_{SYNC_LOCK}	Time to lock external frequency			50		µs
$f_{(SYNC)}$	Synchronization clock frequency range (MODE/SYNC)	TPSM8287A12BAM, TPSM8287A15BAM	1.3		2.0	MHz
$f_{(SYNC)}$	Synchronization clock frequency range (MODE/SYNC)	TPSM8287A12BBM, TPSM8287A15BBM	1.8		2.7	MHz
$D_{(SYNC)}$	Synchronization clock duty cycle range (MODE/SYNC)		45		55	
$V_{T+(UVP)}$	Positive-going power good threshold voltage (output undervoltage)		94	96	98	$\%V_{OUT}$
$V_{T–(UVP)}$	Negative-going power good threshold voltage (output undervoltage)		92	94	96	$\%V_{OUT}$
$V_{T+(OVP)}$	Positive-going power good threshold voltage (output overvoltage)		104	106	108	$\%V_{OUT}$
$V_{T–(OVP)}$	Negative-going power good threshold voltage (output overvoltage)		102	104	106	$\%V_{OUT}$
V_{OL}	Low-level output voltage (PG)	I_{OL} = 10mA			0.3	V
I_{LKG}	Input leakage current into PG	V_{OH} = 3.3V			200	nA
V_{IH}	High-level input voltage (PG)	Device configured as a secondary device in stacked operation	0.8			V
V_{IL}	Low-level input voltage (PG)	Device configured as a secondary device in stacked operation			0.4	V

6.5 Electrical Characteristics (続き)

T_J = –55°C to 125°C, and V_{IN} = 2.7V to 6V. Typical values at V_{IN} = 3.3V and T_J = 25°C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level input current (PG)	Device configured as a secondary device in stacked operation			1	µA
I_{IL}	Low-level input current (PG)	Device configured as a secondary device in stacked operation	–1			µA
$t_{d(PG)}$	Deglitch time (PG)	High-to-low or low-to-high transition on the PG pin	34	40	46	µs
OUTPUT						
V_{OUT}	Output voltage accuracy	$V_{IN} \geq V_{OUT}$ + 1.4V	–1.0		1.0	%
V_{ICR}	Input common-mode range (VOSNS)		–100		$V_{O(nom)}$ + 100	mV
V_{ICR}	Input common-mode range (GOSNS)		–100		100	mV
f_{SW}	Switching frequency (SW)	f_{SW} = 1.5MHz, PWM operation, V_{IN} = 3.3V, V_{OUT} = 0.75V	1.35	1.5	1.65	MHz
		f_{SW} = 2.25MHz, PWM operation, V_{IN} = 3.3V, V_{OUT} = 0.75V	2.025	2.25	2.475	
f_{mod}	Frequency of the spread-spectrum sweep			f_{sw}/2048		kHz
Δf_{SW}	Switching frequency variation during spread-spectrum operation			±10%		
τ	Emulated current time constant			12.5		µs
g_m	Error amplifier transconductance			1.5		mS
I_{LIM}	High-side FET forward switch current limit, DC	TPSM8287A12BAM, TPSM8287A12BBM	15	19	21	A
		TPSM8287A15BAM, TPSM8287A15BBM	18	23	25	
	Low-side FET negative current limit, DC		7.5		12	A

6.6 I²C Interface Timing Characteristics

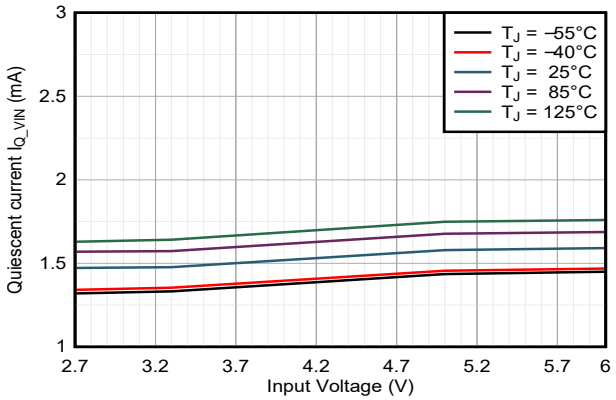
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard mode		100	kHz
		Fast mode		400	
		Fast mode plus		1000	
$t_{HD;}$ t_{STA}	Hold time (repeated) START condition	Standard mode	4		µs
		Fast mode	0.6		
		Fast mode plus	0.26		
t_{LOW}	LOW period of the SCL clock	Standard mode	4.7		µs
		Fast mode	1.3		
		Fast mode plus	0.5		
t_{HIGH}	HIGH period of the SCL clock	Standard mode	4		µs
		Fast mode	0.6		
		Fast mode plus	0.26		
$t_{SU;}$ t_{STA}	Setup time for a repeated START condition	Standard mode	4.7		µs
		Fast mode	0.6		
		Fast mode plus	0.26		
$t_{HD;}$ t_{DAT}	Data hold time	Standard mode	0	3.45	µs
		Fast mode	0	0.9	
		Fast mode plus	0		

6.6 I²C Interface Timing Characteristics (続き)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{SU;}$ t_{DAT}	Data setup time	Standard mode	250		ns
		Fast mode	100		
		Fast mode plus	50		
t_r	Rise time of both SDA and SCL signals	Standard mode		1000	ns
		Fast mode	20	300	
		Fast mode plus		120	
t_f	Fall time of both SDA and SCL signals	Standard mode		300	ns
		Fast mode	20 × V_{DD} / 5.5V (1)	300	
		Fast mode plus	20 × V_{DD} / 5.5V (1)	120	
$t_{SU;}$ t_{STO}	Setup time for STOP condition	Standard mode	4		µs
		Fast mode	0.6		
		Fast mode plus	0.26		
t_{BUF}	Bus free time between a STOP and START condition	Standard mode	4.7		µs
		Fast mode	1.3		
		Fast mode plus	0.5		
C_b	Capacitive load for each bus line	Standard mode		400	pF
		Fast mode		400	
		Fast mode plus		550	

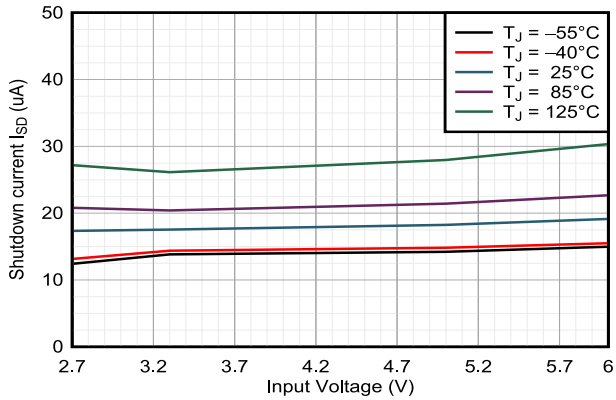
(1) V_{DD} is the pullup voltage of SDA and SCL

6.7 Typical Characteristics



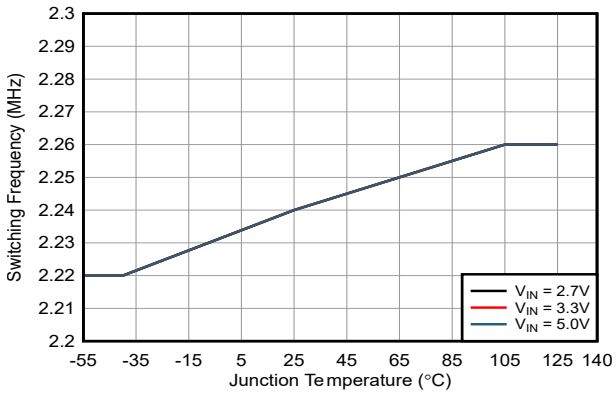
I_{OUT} = 0µA SINGLE = 1 MODE/SYNC = Low

図 6-1. Operating Supply Current (Power-Save Mode)



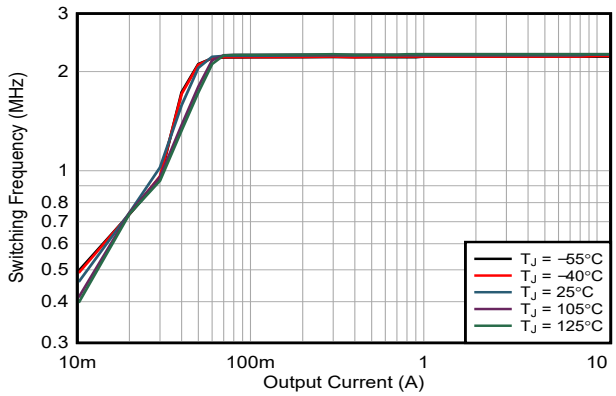
V_{SW} = 0.0V EN = Low

図 6-2. Shutdown Current



I_{OUT} = 6A V_{OUT} = 0.9V MODE/SYNC = High

図 6-3. TPSM8287A12BBM Switching Frequency vs T_J



V_{IN} = 3.3V V_{OUT} = 0.9V MODE/SYNC = Low

図 6-4. TPSM8287A12BBM Switching Frequency vs I_{OUT}

7 Detailed Description

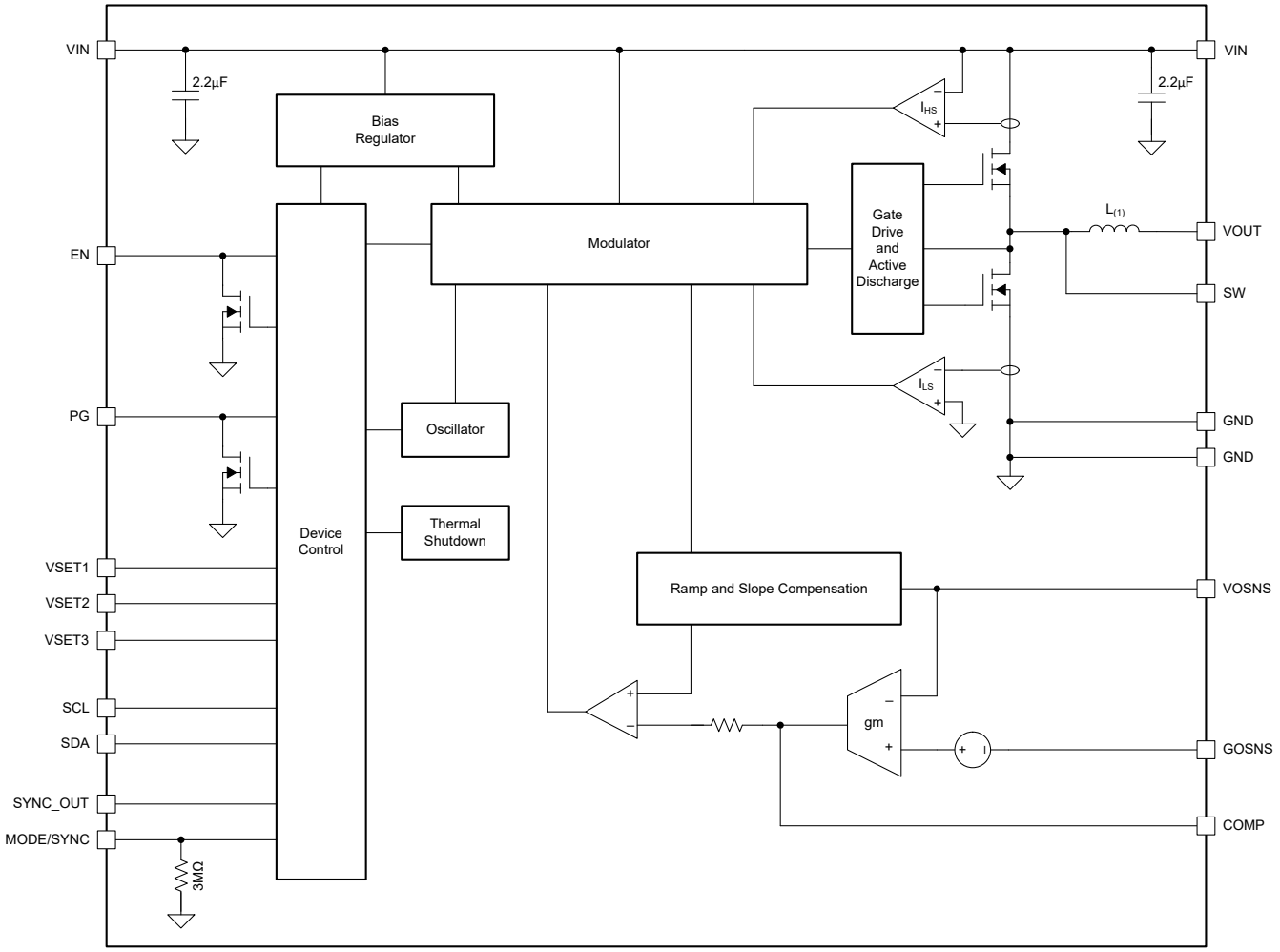
7.1 Overview

The TPSM8287A1xM synchronous, step-down converter power modules use a fixed-frequency DCS-Control topology to achieve fast transient response during a load step while switching with a fixed frequency during normal operation. This control topology, together with the low output voltage ripple, high DC accuracy, and differential remote sense, makes them designed for supplying the cores of modern high-performance processors or other voltage rails with tight regulation requirements.

As the load current decreases, the converter can enter power save mode based on the MODE/SYNC pin, reducing the switching frequency and entering DCM to achieve high efficiency over the entire load current range.

This pin-to-pin compatible family of modules includes 12A and 15A variants. To further increase the output current capability, combine multiple devices in a “stack”. For example, paralleling four 15A devices can provide up to 60A of current.

7.2 Functional Block Diagram



(1) For inductance values, please refer to 表 4-1.

7.3 Feature Description

7.3.1 Fixed-Frequency DCS-Control Topology

図 7-1 shows a simplified block diagram of the fixed-frequency DCS-control topology used in the TPSM8287A1xM devices. This topology comprises an inner emulated current loop, a middle direct feedback loop, and an outer voltage-regulating loop. The differential remote sense allows for precise voltage regulation at the load. The external compensation allows fine tuning the load transient response for a wide range of output capacitance and load transient requirements.

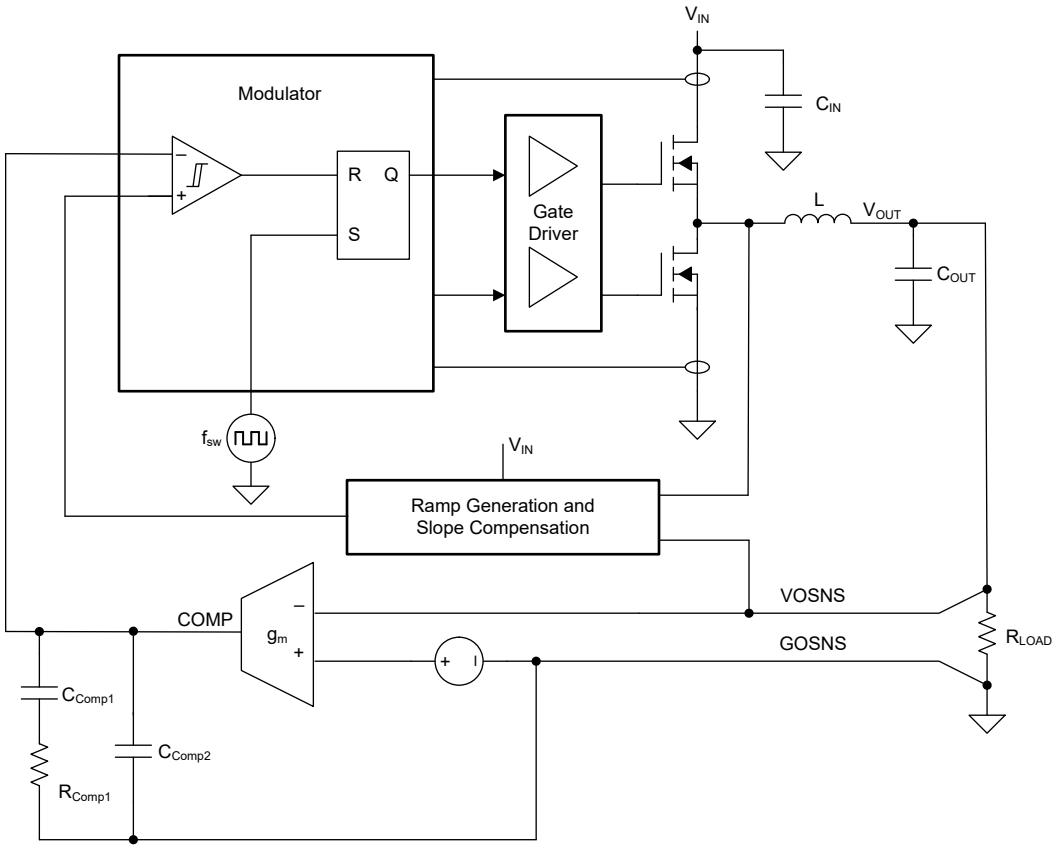


図 7-1. Fixed-Frequency DCS-Control Topology (Simplified)

7.3.2 Forced-PWM and Power Save Modes

The device can control the inductor current in three different ways to regulate the output:

- Pulse-width modulation with continuous inductor current (PWM-CCM)
- Pulse-width modulation with discontinuous inductor current (PWM-DCM)
- Pulse-frequency modulation with discontinuous inductor current and pulse skipping (PFM-DCM)

The on-time in PWM-CCM is set by 式 1. For very small output voltages, a minimum on time of approximately 50ns (t_{ON_min}) reduces the switching frequency from the set value. Even when the minimum on-time is reached, the device maintains proper output voltage regulation by extending the off-time.

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \quad (1)$$

During PWM-CCM operation, the device switches at a constant frequency and the inductor current is continuous (see 図 7-2). PWM operation achieves the lowest output voltage ripple and the best transient performance.

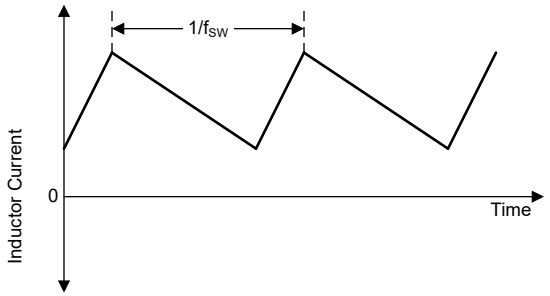


図 7-2. Continuous Conduction Mode (PWM-CCM) Current Waveform

During PWM-DCM operation the device switches at a constant frequency and the inductor current is discontinuous (see 図 7-3). In this mode the device controls the peak inductor current to maintain the selected switching frequency while still being able to regulate the output.

式 2 is used to calculate the output current threshold at which the device changes from PWM-CCM to PWM-DCM:

$$I_{OUT(\mathrm{CCM-DCM})} = \frac{V_{IN} \times t_{ON}}{2} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L} \quad (2)$$

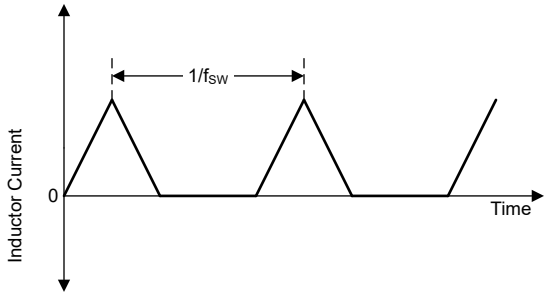


図 7-3. Discontinuous Conduction Mode (PWM-DCM) Current Waveform

During PFM-DCM operation the device keeps the peak inductor current constant (at a level corresponding to an approximately 20ns on-time of the converter) and skips pulses to regulate the output (see 図 7-4). The switching pulses that occur during PFM-DCM operation are synchronized to the internal clock.

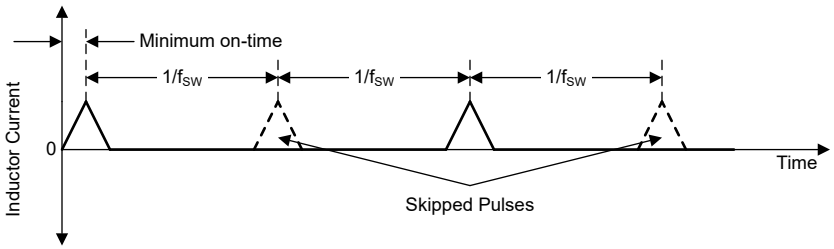
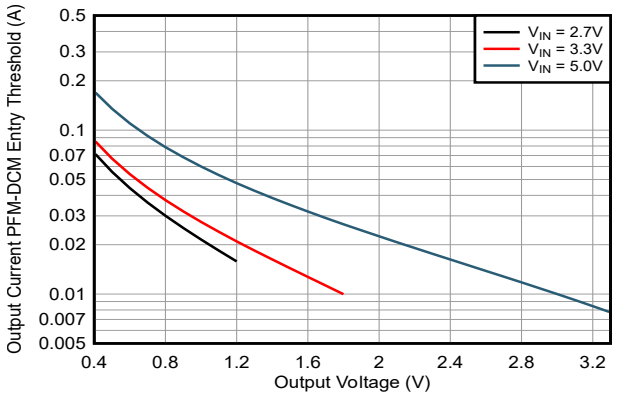


図 7-4. Discontinuous Conduction Mode (PFM-DCM) Current Waveform

式 3 is used to calculate the output current threshold at which the device changes from PWM-DCM to PFM-DCM:

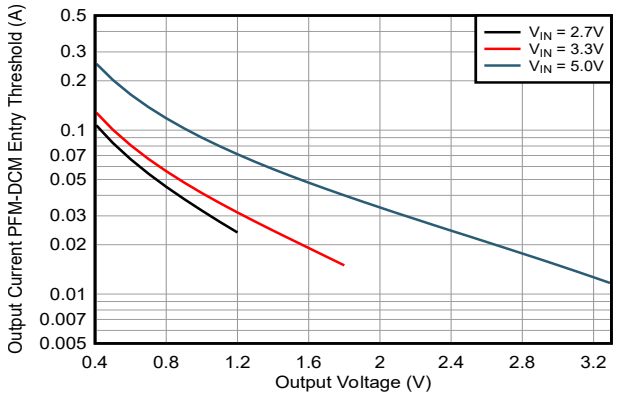
$$I_{OUT(PFM-entry)} = \frac{V_{IN} \times 20\ \mathrm{ns}}{2} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L} \quad (3)$$

図 7-5 through 図 7-8 show how the PWM-DCM to PFM-DCM threshold typically varies with V_{IN} and V_{OUT}.



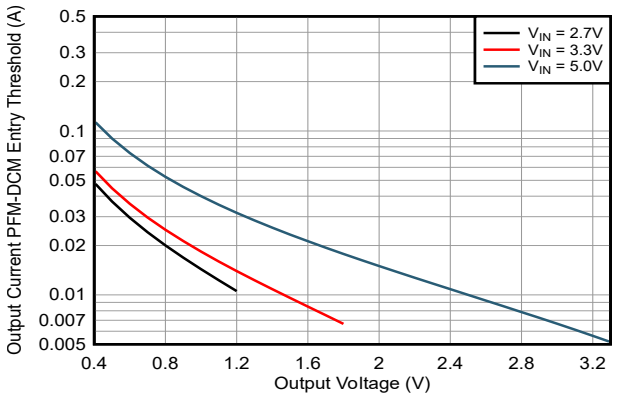
MODE/SYNC = Low

図 7-5. PFM-DCM Entry Threshold TPSM8287A12BAM



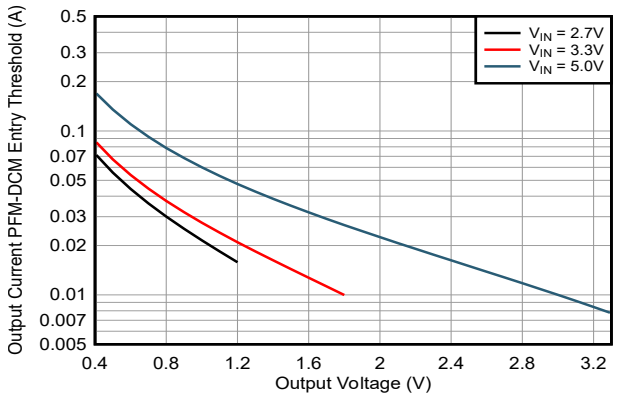
MODE/SYNC = Low

図 7-6. PFM-DCM Entry Threshold TPSM8287A12BBM



MODE/SYNC = Low

図 7-7. PFM-DCM Entry Threshold TPSM8287A15BAM



MODE/SYNC = Low

図 7-8. PFM-DCM Entry Threshold TPSM8287A15BBM

Configure the device to use either Forced-PWM Mode (FPWM) or Power Save Mode (PSM):

- In Forced-PWM mode, the device uses PWM-CCM at all times
- In power save mode, the device uses PWM-CCM at medium and high loads, PWM-DCM at light loads, and PFM-DCM at very light loads. Transitions between the different operating modes are seamless.

表 7-1 shows the function table of the MODE/SYNC pin and the FPWMEN bit in the CONTROL1 register, which controls the operating mode of the device.

表 7-1. FPWM Mode and Power Save Mode Selection

SSCEN Bit	FPWMEN Bit	MODE/SYNC Pin	OPERATING MODE	REMARK
0	0	Low	PSM	Do not use in a stacked configuration
1	0	Low	PSM	
0	1	X	FPWM	
0	X	High	FPWM	
X	X	Sync Clock	FPWM	See セクション 7.3.8
1	1	X	FPWM	See セクション 7.3.9
1	X	High	FPWM	

7.3.3 Precise Enable

The Enable (EN) pin is bidirectional and has two functions. See 図 7-9:

- As an input, the pin enables and disables the DC/DC converter in the device
- In a stacked configuration, the pin is an output and provides a SYSTEM_READY signal to other devices.

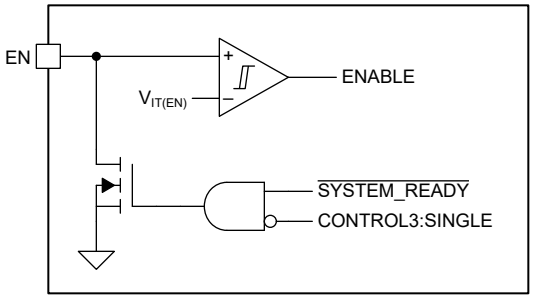


図 7-9. Enable Functional Block Diagram

Because there is an internal open-drain transistor connected to the EN pin, do not drive this pin directly from a low-impedance source. Instead, use a > 15kOhm resistor to limit the current flowing into the EN pin.

When power is first applied to the VIN pin, the device pulls the EN pin low until the pin loads the default register settings from nonvolatile memory and reads the state of the VSETx and SYNC_OUT pins. The device also pulls EN low if a fault, such as thermal shutdown or overvoltage lockout, occurs. In a stacked configuration, all devices share a common enable signal, which means that the DC/DC converters in the stack cannot start to switch until *all* devices in the stack have completed the initialization. Similarly, a fault in one or more devices in the stack disables *all* converters in the stack (see セクション 7.3.17).

In standalone (non-stacked) applications, set SINGLE = 1 in the CONTROL3 register to disable the active pulldown of the EN pin. Fault conditions have no effect on the EN pin when SINGLE = 1. (Note that the EN pin is *always* pulled down during device initialization.) In stacked applications, make sure that SINGLE = 0. Setting SINGLE = 1 also disables the SYNC_OUT pin.

When the internal $\overline{\text{SYSTEM\_READY}}$ signal is low (that is, initialization is complete and there are no fault conditions), the internal open-drain transistor is high impedance and the EN pin functions like a standard input: a high level on the EN pin enables the DC/DC converter in the device and a low level disables the DC/DC converter. The I^2C interface is enabled as soon as the device has completed the initialization and is not affected by the state of the internal ENABLE or $\overline{\text{SYSTEM\_READY}}$ signals.

A low level on the EN pin forces the device into shutdown. During shutdown, the MOSFETs in the power stage are off, the internal control circuitry is disabled, and the device consumes less than 20µA (typical). Do not leave the EN pin floating.

The Precise Enable input provides a user-programmable undervoltage lockout by adding a resistor divider to the input of the EN pin. The Precise Enable input also allows the user to drive the pin by a slowly changing voltage and enables the use of an external RC network to achieve a precise power-up delay. See *Achieving a clean startup by using a DC/DC converter with a precise enable-pin threshold* analog design journal for more details.

7.3.4 Start-Up

When the voltage on the VIN pin exceeds the positive-going UVLO threshold, the device initializes as follows:

- The device pulls the EN pin low
- The device the internal reference voltage
- The device reads the state of the VSETx and SYNC_OUT pins
- The device loads the default values into the device registers

When initialization is complete, the device enables I^2C communication and releases the EN pin. The external circuitry controlling the EN pin now determines the behavior of the device:

- If the EN pin is low, the device is disabled:
  - The user can write to and read from the device registers
  - The power stage does not operate (high-impedance).
- If the EN pin is high, the device is enabled:
  - The user can write to and read from the device registers
  - After a short delay, the power stage starts switching
  - The converter ramps up the output voltage

図 7-10 shows the start-up sequence when the EN pin is pulled up to V_{IN} through a resistor.

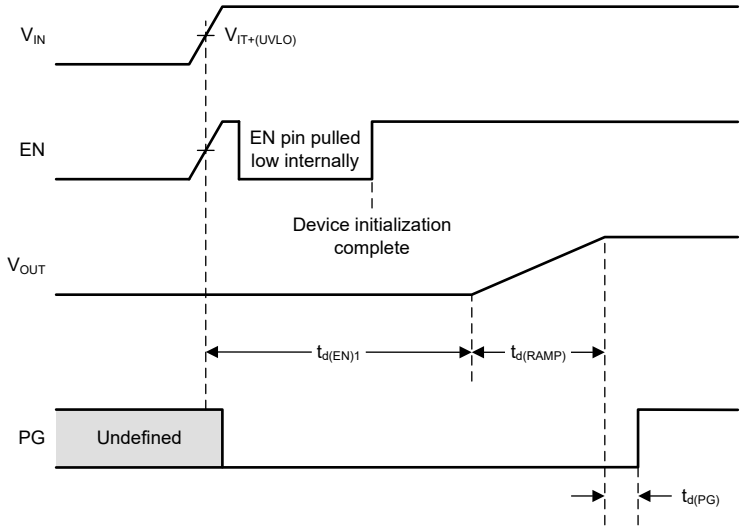


図 7-10. Start-Up Timing When EN is Pulled Up to V_{IN}

図 7-11 shows the start-up sequence when an external signal is connected to the EN pin.

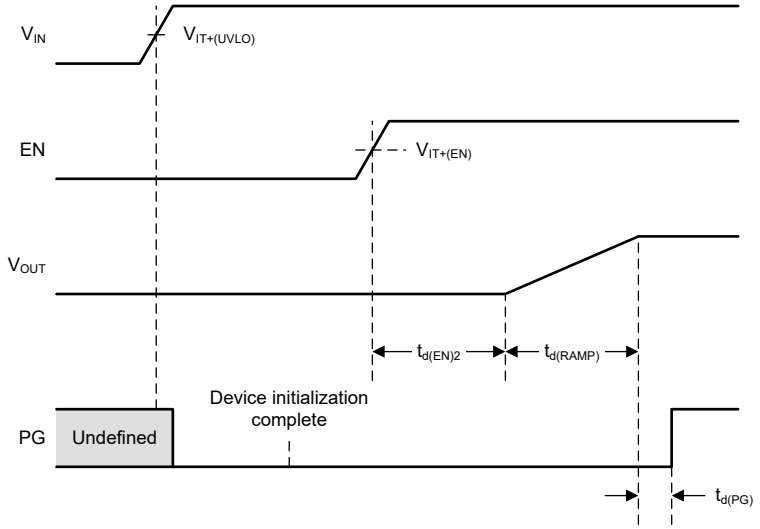


図 7-11. Start-Up Timing When an External Signal is Connected to the EN Pin

The SSTIME[1:0] bits in the CONTROL2 register select the duration of the soft-start ramp:

- $t_{d(RAMP)}$ = 500µs
- $t_{d(RAMP)}$ = 1ms (default)

- $t_{d(RAMP)}$ = 2ms
- $t_{d(RAMP)}$ = 4ms

The device ignores new values during the soft-start sequence for the following parameters:

- Output voltage setpoint (VOUT[7:0])
- Output voltage range (VRANGE[1:0])
- Soft-start time (SSTIME[1:0])

If the user changes the value of VSET[7:0] during soft start, the device first ramps to the value that VSET[7:0] had when the soft-start sequence began. When soft start is complete, the device ramps up or down to the new value.

During start-up, the device does not sink current to make sure that the output voltage follows the configured ramp rate to the target output voltage. With this, the device can start up into a prebiased output. In this case, only a portion of the internal voltage ramp is seen externally (see 図 7-12).

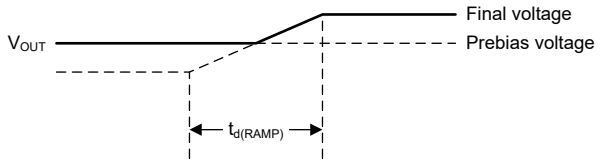


図 7-12. Start-Up into a Prebiased Output

7.3.5 Switching Frequency Selection

The TPSM8287A1xM module family consists of device variants with different switching frequencies. For available options see 表 4-1. The different switching frequencies allows the selection of the device which provides the best efficiency by optimizing the power losses for a given use case.

A lower switching frequency version does not necessarily offer a higher efficiency across the entire load, Vin or Vout range. The lower switching frequency does reduce the switching losses in the power stage, but at the same time leads to a higher ripple current in the inductor which leads to higher inductor losses, higher output voltage ripple, and a lower maximum output current (see セクション 7.3.13). Because of this, TI recommends to compare the efficiency when picking a certain device variant.

図 7-13 and 図 7-14 provide an efficiency comparison between the 1.5MHz TPSM8287A12BAM and 2.25MHz TPSM8287A12BBM. For output voltages ≥ 1.2V, the efficiency between the 2.25MHz and 1.5MHz device is almost the same for high load currents, whereas the 2.25MHz version gives higher efficiency at load currents below 3A. The 1.5MHz device generally gives higher efficiency for the other operating points, especially for lower output voltages. For output voltages >= 1.2V, TI recommends the 2.25MHz device for most applications due to the comparable efficiency, lower output voltage ripple, and higher maximum output current.

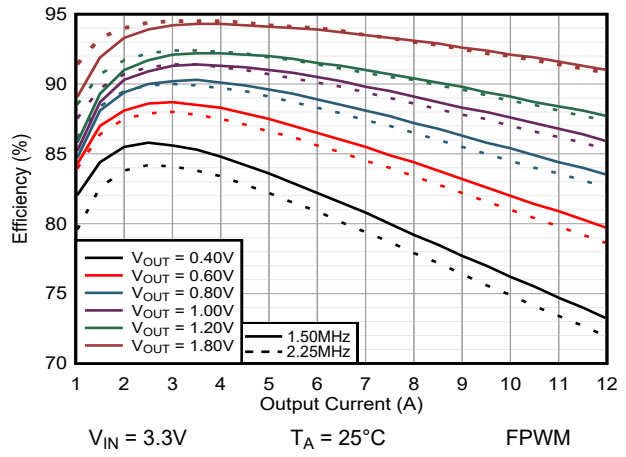


図 7-13. Efficiency Comparison TPSM8287A12BAM vs TPSM8287A12BBM

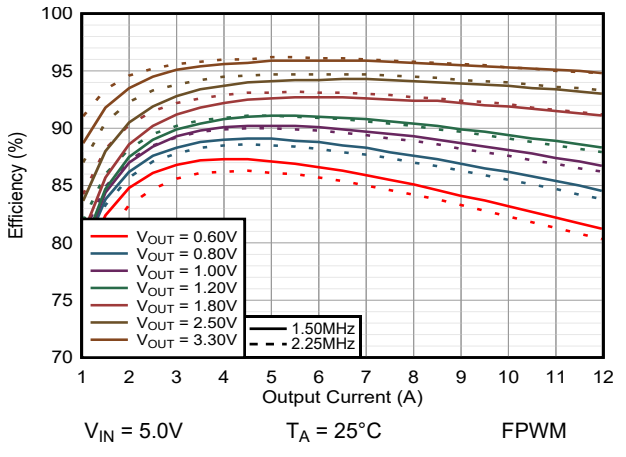


図 7-14. Efficiency Comparison TPSM8287A12BAM vs TPSM8287A12BBM

7.3.6 Output Voltage Setting

7.3.6.1 Output Voltage Setpoint

During initialization, the device reads the state of the VSETx pins and selects the default output voltage according to 表 7-2. Note that the VSETx pins also select the I²C target address of the device and the setting of the VRANGE bits located in register CONTROL2. The VSETx pins are only read during a power cycle of VIN or by setting RESET = 1 through the I²C interface. Changing the configuration after VIN is present does not affect the content of the registers or the I²C address. Make sure that there is no stray current path connected to the VSETx pins and that the parasitic capacitance between the VSETx pins and GND is less than 100pF. For proper operation, the input voltage must be at least 1.4V above the selected output voltage.

表 7-2. Start-Up Output Voltage and I²C Address

VSET3	VSET2	VSET1	I²C ADDRESS	VRANGE [1:0]	VOUT VOLTAGE
GND	GND	VIN	0x40	0b10	0.45V
GND	VIN	GND	0x40	0b10	0.50V
GND	VIN	VIN	0x40	0b10	0.55V
VIN	GND	GND	0x40	0b10	0.60V
VIN	GND	VIN	0x40	0b10	0.65V
VIN	VIN	GND	0x40	0b10	0.70V
VIN	VIN	VIN	0x40 (1)	0b10	0.75V
47kΩ to GND	GND	GND	0x41 (1)	0b11	0.80V
47kΩ to GND	GND	VIN	0x41	0b11	0.85V
47kΩ to GND	VIN	GND	0x41	0b11	0.90V
47kΩ to GND	VIN	VIN	0x41	0b11	0.95V
47kΩ to VIN	GND	GND	0x41	0b11	1.00V
47kΩ to VIN	GND	VIN	0x41 (1)	0b11	1.05V
47kΩ to VIN	VIN	GND	0x41 (1)	0b11	1.10V
47kΩ to VIN	VIN	VIN	0x41	0b11	1.15V
GND	47kΩ to GND	GND	0x42 (1)	0b11	1.20V
GND	47kΩ to GND	VIN	0x42	0b11	1.25V

表 7-2. Start-Up Output Voltage and I²C Address (続き)

VSET3	VSET2	VSET1	I²C ADDRESS	VRANGE [1:0]	VOUT VOLTAGE
GND	47kΩ to VIN	GND	0x42	0b11	1.30V
GND	47kΩ to VIN	VIN	0x42	0b11	1.35V
VIN	47kΩ to GND	GND	0x42	0b11	1.40V
VIN	47kΩ to GND	VIN	0x42	0b11	1.45V
VIN	47kΩ to VIN	GND	0x42	0b11	1.50V
VIN	47kΩ to VIN	VIN	0x42	0b11	1.55V
GND	GND	47kΩ to GND	0x43	0b11	1.60V
GND	GND	47kΩ to VIN	0x43	0b11	1.65V
GND	VIN	47kΩ to GND	0x43	0b11	1.70V
GND	VIN	47kΩ to VIN	0x43	0b11	1.75V
VIN	GND	47kΩ to GND	0x43	0b11	1.80V
VIN	GND	47kΩ to VIN	0x43	0b11	1.85V
VIN	VIN	47kΩ to GND	0x43	0b11	1.90V
VIN	VIN	47kΩ to VIN	0x43	0b11	1.95V
47kΩ to GND	47kΩ to GND	GND	0x40	0b11	2.00V
47kΩ to GND	47kΩ to GND	VIN	0x40	0b11	2.05V
47kΩ to GND	47kΩ to VIN	GND	0x40	0b11	2.10V
47kΩ to GND	47kΩ to VIN	VIN	0x40	0b11	2.15V
47kΩ to VIN	47kΩ to GND	GND	0x40	0b11	2.20V
47kΩ to VIN	47kΩ to GND	VIN	0x40	0b11	2.25V
47kΩ to VIN	47kΩ to VIN	GND	0x40	0b11	2.30V
47kΩ to VIN	47kΩ to VIN	VIN	0x40	0b11	2.35V
47kΩ to GND	GND	47kΩ to GND	0x41	0b11	2.40V
47kΩ to GND	GND	47kΩ to VIN	0x41	0b11	2.45V
47kΩ to GND	VIN	47kΩ to GND	0x41	0b11	2.50V
47kΩ to GND	VIN	47kΩ to VIN	0x41	0b11	2.55V
47kΩ to VIN	GND	47kΩ to GND	0x41	0b11	2.60V
47kΩ to VIN	GND	47kΩ to VIN	0x41	0b11	2.65V
47kΩ to VIN	VIN	47kΩ to GND	0x41	0b11	2.70V
47kΩ to VIN	VIN	47kΩ to VIN	0x41	0b11	2.75V
GND	47kΩ to GND	47kΩ to GND	0x42	0b11	2.80V
GND	47kΩ to GND	47kΩ to VIN	0x42	0b11	2.85V
GND	47kΩ to VIN	47kΩ to GND	0x42	0b11	2.90V
GND	47kΩ to VIN	47kΩ to VIN	0x42	0b11	2.95V
VIN	47kΩ to GND	47kΩ to GND	0x42	0b11	3.00V
VIN	47kΩ to GND	47kΩ to VIN	0x42	0b11	3.05V
VIN	47kΩ to VIN	47kΩ to GND	0x42	0b11	3.10V
VIN	47kΩ to VIN	47kΩ to VIN	0x42	0b11	3.15V

表 7-2. Start-Up Output Voltage and I²C Address (続き)

VSET3	VSET2	VSET1	I²C ADDRESS	VRANGE [1:0]	VOUT VOLTAGE
47kΩ to GND	47kΩ to GND	47kΩ to GND	0x43	0b11	3.20V
47kΩ to GND	47kΩ to GND	47kΩ to VIN	0x43	0b11	3.25V
47kΩ to GND	47kΩ to VIN	47kΩ to GND	0x43	0b11	3.30V
47kΩ to GND	47kΩ to VIN	47kΩ to VIN	0x43	0b11	3.35V
47kΩ to VIN	47kΩ to GND	47kΩ to GND	0x44	0b10	0.75V
GND	GND	GND	0x40	0b11	0.80V
47kΩ to VIN	47kΩ to GND	47kΩ to VIN	0x44	0b11	1.05V
47kΩ to VIN	47kΩ to VIN	47kΩ to GND	0x44	0b11	1.10V
47kΩ to VIN	47kΩ to VIN	47kΩ to VIN	0x44	0b11	1.20V

(1) A second I²C address for the same output voltage is found at the bottom of this table

During start-up, the output voltage ramps up to the target value set by the VSETx pins before ramping up or down to any new value programmed to the device over the I²C interface. If the user programs new output voltage setpoints (VOUT[7:0]), output voltage range (VRANGE[1:0]), or soft-start time (SSTIME[1:0]) settings when the device has already begun the soft-start sequence, the device ignores the new values until the soft-start sequence is complete. When changing VOUT[7:0], VRAMP[1:0], or SSTIME[1:0] while EN is low, the device uses the new values the next time the device is enabled.

7.3.6.2 Output Voltage Range

The device has four different output voltage ranges. The VRANGE[1:0] bits in the CONTROL2 register control which range is active (see 表 7-3). The default output voltage range is determined by the VSETx pins.

表 7-3. Voltage Ranges

VRANGE[1:0]	Voltage Range
0b00	0.4V to 0.71875V in 1.25mV steps
0b01	0.4V to 1.0375V in 2.5mV steps
0b10	0.4V to 1.675V in 5mV steps
0b11	0.8V to 3.35V in 10mV steps

Every change to the VRANGE[1:0] bits must be followed by a write to the VSET register – even if the value of the VSET[7:0] bits does not change. This sequence is necessary for the device to start to use the new voltage range.

When switching to or from the 0.8V to 3.35V range, the device switches the internal reference between 0.4V and 0.8V. To avoid any output voltage over or undershoot that can occur during the change, the VRANGE change must be done at an output voltage that occurs in both the new range and old range and the VSET[7:0] bits must set the same output voltage in both the new range and old range.

7.3.6.3 Non-Default Output Voltage Setpoint

If none of the output voltage setpoints in 表 7-2 are designed for the application, the user can change the output voltage through I²C *before enabling* the device. After the EN pin is pulled high, the device starts up and ramps to the desired output voltage set in the VSET register. A change of the device settings through I²C while the device is ramping are only be performed after the initial ramp is completed.

7.3.6.4 Dynamic Voltage Scaling (DVS)

If the user changes the output voltage setpoint while the device is operating, the device ramps up or down to the new voltage setting in a controlled way.

The VRAMP[1:0] bits in the CONTROL1 register set the slew rate when the device ramps from one voltage to another during DVS (see 表 7-4). The ramp rate is independent of the setting of the VRANGE[1:0] bits.

表 7-4. Dynamic Voltage Scaling Slew Rate

VRAMP[1:0]	DVS Slew Rate
0b00	10mV/µs
0b01	5mV/µs
0b10 (default)	1.25mV/µs
0b11	0.5mV/µs

If the MODE/SYNC pin is low and FPWMEN = 0, the slew rate can be less at low output currents because the device does not actively transfer energy back from the output capacitor to the input. At higher load currents the device controls the slew rate by transferring energy to the output.

Note that ramping the output to a higher voltage requires additional output current, so that during DVS the converter must generate a total output current given by:

$$I_{OUT} = I_{OUT\,(DC)} + C_{OUT} \frac{dV_{OUT}}{dt} \quad (4)$$

where:

- I_{OUT} is the total current the converter must generate while ramping to a higher voltage
- $I_{OUT(DC)}$ is the DC load current
- C_{OUT} is the total output capacitance
- dV_{OUT}/dt is the slew rate of the output voltage (programmable in the range 0.5mV/µs to 10mV/µs)

For correct operation, make sure that the total output current during DVS does not exceed the rated current of the device.

7.3.7 Compensation (COMP)

The COMP pin is the connection point for an external compensation network. A series-connected resistor and capacitor to GOSNS is sufficient for typical applications and provides enough scope to optimize the loop response for a wide range of operating conditions.

When using multiple devices in a stacked configuration, all devices share a common compensation network, and the COMP pin makes sure equal current sharing between them (see セクション 7.3.17).

7.3.8 Mode Selection / Clock Synchronization (MODE/SYNC)

A high level on the MODE/SYNC pin selects forced-PWM operation. A low level on the MODE/SYNC pin selects power-save operation, in which the device automatically transitions between PWM and PFM according to the load conditions.

If applying a valid clock signal to the MODE/SYNC pin, the device synchronizes the switching cycles to the external clock and automatically selects forced-PWM operation. When applying a frequency modulated clock to the MODE/SYNC pin, the device also follows this. This action can be useful in applications where the converter must follow an external Spread Spectrum Modulation.

The MODE/SYNC pin is logically ORed with the FPWMEN bit in the CONTROL1 register. Setting either high enables FPWM (see セクション 7.3.2).

When multiple devices are used in a stacked / parallel configuration to increase the output current, the clock signal from the primary device must cascade through all devices in a daisy chain configuration. The SYNC_OUT pin of the previous device must connect to the MODE/SYNC pin of the next device in the chain (see セクション 7.3.17).

7.3.9 Spread Spectrum Clocking (SSC)

The device has a spread spectrum clocking function which can reduce electromagnetic interference (EMI). When the SSC function is active, the device modulates the switching frequency to approximately ±10% around the nominal value. The frequency modulation has a triangular characteristic (see 図 7-15).

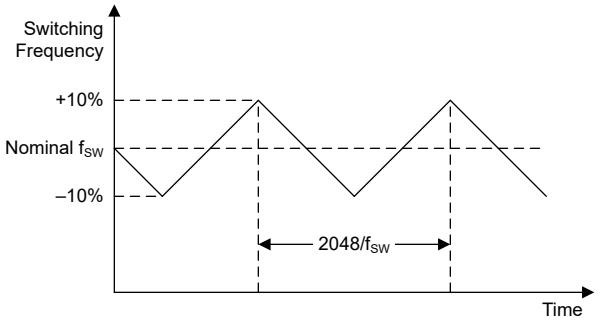


図 7-15. Spread Spectrum Clocking Behavior

To use the SSC function, make sure that:

- SSCEN = 1 in the CONTROL1 register
- The device is not synchronized to an external clock

TI recommends to use FPWM operation when using SSC, but SSC is available with PSM operation. To disable the SSC function, make sure that SCCEN = 0 in the CONTROL1 register.

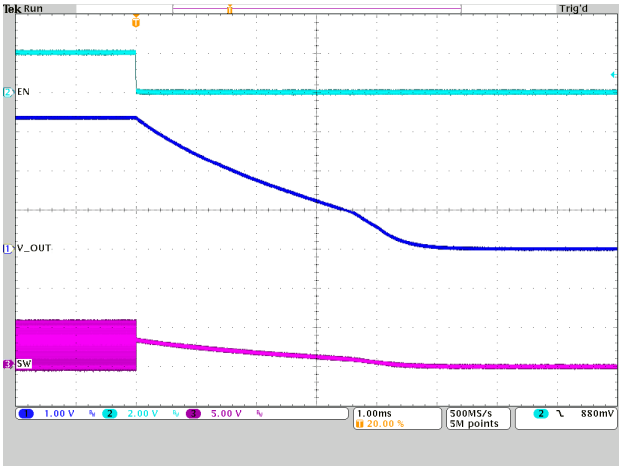
7.3.10 Output Discharge

The device has an output discharge function which makes sure a defined ramp down of the output voltage when the device is disabled. The discharge stays on after the output is discharged. The output discharge function is enabled when DISCHEN = 1 in the CONTROL1 register.

If output discharge is enabled, the device discharges the output under the following conditions:

- A low level is applied to the EN pin
- SWEN = 0 in the CONTROL1 register
- A thermal shutdown event occurs
- An UVLO event occurs
- An OVLO event occurs

When the output voltage is above 900mV (typical), the discharge is about 115mA. Below 900mV, the discharge is about 3.5Ohm. 図 7-16 shows an example of the typical discharge behavior.



V_{IN} = 5.0V　　I_{OUT} = 0mA　　VOUT = 3.3V discharge to 0V

図 7-16. Output Discharge

The output discharge function is not available until the device has been enabled at least once after applying VIN. The output discharge functions until VIN drops to around 1.8V.

In a stacked configuration, the discharge is always active in the secondary devices. Please refer to 表 7-6.

7.3.11 Undervoltage Lockout (UVLO)

The device has an undervoltage lockout function which disables the device if the supply voltage is too low for correct operation. The negative-going threshold of the UVLO function is 2.5V (typical). If the supply voltage decreases below this value, the device stops switching and, if DISCHEN = 1 in the CONTROL1 register, turns on the output discharge. In addition, the EN pin is pulled low, which disables all other devices in the stack.

The device automatically starts switching again – begins a new soft-start sequence – when the supply voltage is higher than 2.6V (typical).

7.3.12 Overvoltage Lockout (OVLO)

The device has an overvoltage lockout function that disables the DC/DC converter if the supply voltage is too high for correct operation. The positive-going threshold of the OVLO function is 6.3V (typical). If the supply voltage increases above this value, the device stops switching and, if DISCHEN = 1 in the CONTROL1 register, turns on the output discharge. In addition, the EN pin is pulled low, which disables all other devices in the stack.

The device automatically starts switching again – begins a new soft-start sequence – when the supply voltage falls below 6.2V (typical).

7.3.13 Overcurrent Protection

7.3.13.1 Cycle-by-Cycle Current Limiting

The TPSM8287A1xM module is protected against overload and short-circuit events. If the inductor current exceeds the high-side current limit, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. The high-side MOSFET turns on again only if the current in the low-side MOSFET has decreased below the low-side current limit. These current limits are designed to prevent the inductor of going into saturation. 図 7-17 shows the typical input current in current limit.

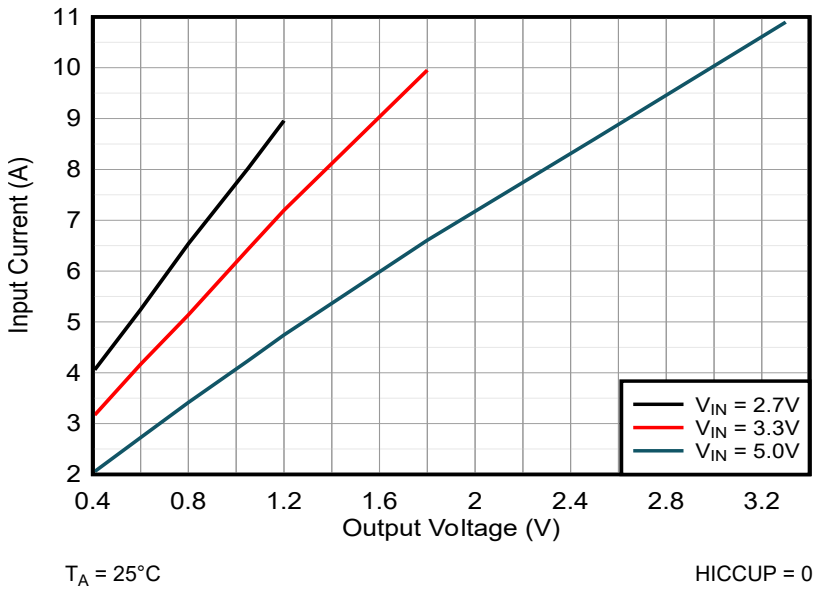


図 7-17. TPSM8287A12BBM Typical Input Current in Current Limit

The low-side MOSFET also contains a negative current limit to prevent excessive current from flowing back through the inductor to the input. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off. In this scenario, both MOSFETs are off until the start of the next cycle. The negative current limit is only active in forced-PWM mode.

7.3.13.2 Hiccup Mode

Hiccup mode reduces the power dissipation during an overload event. To enable hiccup operation, make sure that HICCUPEN = 1 in the CONTROL1 register. If hiccup operation is enabled and the high-side switch current hits the high-side current limit threshold on 32 consecutive switching cycles, the device:

- Stops switching for 128µs, after which the device automatically starts switching again (the device starts a new soft-start sequence)
- Sets the HICCUP bit in the STATUS register
- Pulls the PG pin low. The PG pin stays low until the overload condition goes away and the device can start up and regulate the output voltage.

Hiccup operation continues – in a repeating sequence of 32 cycles in current limit, followed by a pause of 128µs, followed by a soft-start attempt – for as long as the output overload condition exists.

The device clears the HICCUP bit if reading the STATUS register when the overload condition no longer exists. 図 7-18 shows 2 cycles of hiccup operation, at which point the over load is removed and the part continues in normal operation.

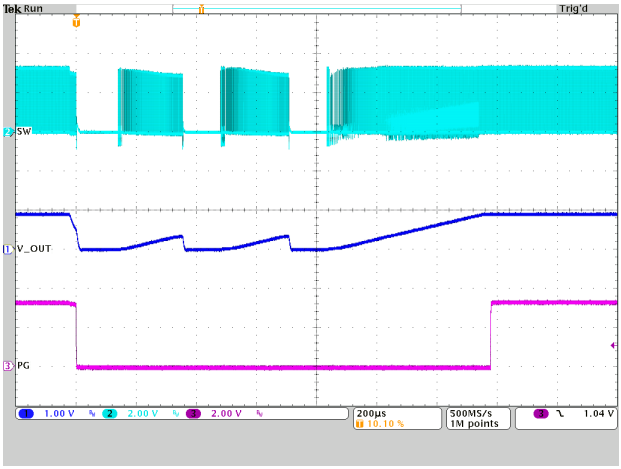


図 7-18. Hiccup Current Limit

7.3.13.3 Current-Limit Mode

To enable current-limit mode, make sure that HICCUPEN = 0 in the CONTROL1 register.

When current limit operation is enabled, the device limits the high-side switch current cycle-by-cycle for as long as the overload condition exists. If the device limits the high-side switch current for four or more consecutive switching cycles, the device sets ILIM = 1 in the STATUS register.

The device clears the ILIM bit if the user reads the STATUS register after the overload condition no longer exits.

7.3.14 Power Good (PG)

The Power-Good (PG) pin is bidirectional and has two functions:

- In a standalone configuration, and in the primary device of a stacked configuration, the PG pin is an open-drain output that indicates the status of the converter or stack.
- In a secondary device of a stacked configuration, the PG pin is an input that detects when the soft-start sequence is complete.

7.3.14.1 Power-Good Standalone, Primary Device Behavior

The primary purpose of the PG pin is to indicate if the output voltage is in regulation, but the PG pin also indicates if the device is in thermal shutdown or disabled. 表 7-5 summarizes the behavior of the PG pin in a stand-alone or primary device.

表 7-5. Power-Good Function Table

V_{IN}	EN	V_{OUT}	Soft Start	PGBLNKDVS	T_J	PG
V_{IN} < 2V	X	X	X	X	X	Undefined
$V_{IT-(UVLO)} \geq V_{IN} \geq 2V$	X	X	X	X	X	Low
$V_{IT-(OVLO)} > V_{IN} > V_{IT+(UVLO)}$	L	X	X	X	X	Low
	H	X	Active	X	X	Low
		$V_{OUT} > V_{T+(OVP)}$ or $V_{OUT} < V_{T-(UVP)}$	Inactive	0	X	Low
				1 (DVS inactive)	X	Low
		X		1 (DVS active)	$T_J < T_{SD}$	Hi-Z
		$V_{T-(OVP)} > V_{OUT} > V_{T+(UVP)}$		X		Hi-Z
		X	X	X	$T_J > T_{SD}$	Low
$V_{IN} > V_{IT+(OVLO)}$	X	X	X	X	X	Low

図 7-20 shows a functional block diagram of the power-good function in a stand-alone or primary device. A window comparator monitors the output voltage, and the output of the comparator goes high if the output voltage is either less than 94% (typical) or greater than 106% (typical) of the nominal output voltage. The output of the window comparator is deglitched – the typical deglitch time is 40µs (see 図 7-19) – and then used to drive the open-drain PG pin.

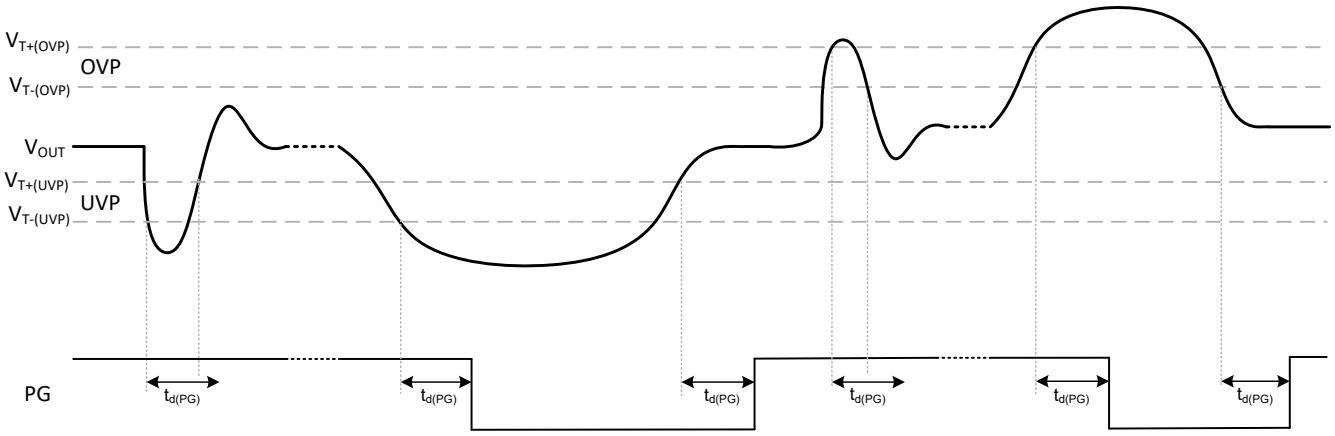


図 7-19. Power-Good Transient and Delay Behavior

If an output under or overvoltage event occurs, the device sets the PBUV or PBOV bits in the STATUS register, respectively. The device clears the PBOV and PBUV bits if the user reads the STATUS register after the power-bad condition no longer exists.

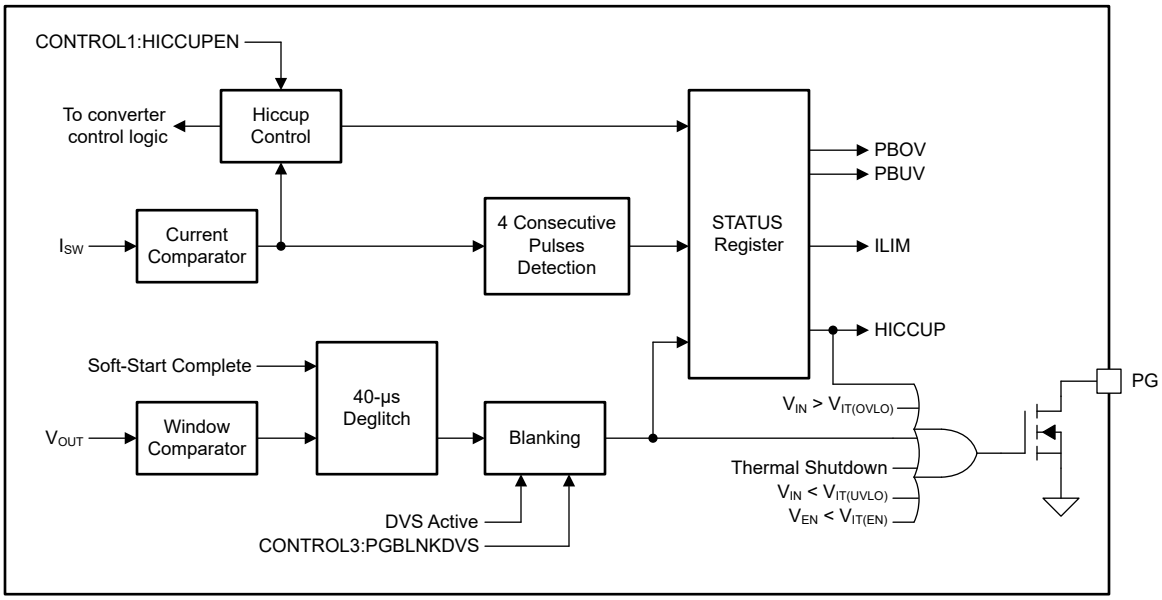


図 7-20. Power-Good Functional Block Diagram (Standalone, Primary Device)

During DVS activity, when the device transitions from one output voltage setting to another, the output voltage can temporarily exceed the limits of the window comparator and pull the PG pin low. The device has a feature to disable this behavior: if PGBLNKDVS = 1 in the CONTROL3 register, the device ignores the output of the power-good window comparator while DVS is active.

Note that the PG pin is always low – regardless of the output of the window comparator – when:

- The device is in thermal shutdown

- The device is in hiccup mode
- The device is disabled
- The device is in undervoltage or overvoltage lockout (UVLO or OVLO)
- The device is in soft start

7.3.14.2 Power-Good Secondary Device Behavior

In a stacked, parallel configuration, the PG signal is used to communicate between the devices. During device initialization, all devices in the stack pull the PG signal low. After each device completes the initialization, only the primary device controls the PG signal and holds the PG signal low until soft start is completed.

The Secondary devices monitor the voltage level of the PG signal. When the PG signal is low, the secondary devices can not sink current until the primary device releases the PG signal. The external pullup resistor pulls PG high and the secondary devices operate in FPWM from that point onwards.

In case of a fault condition, the secondary device does not drive the PG signal but uses the EN pin to deactivate the whole stack. In this case, the Primary converter pulls the PG signal low. For details, see 表 7-6.

7.3.15 Remote Sense

The device has two pins, VOSNS and GOSNS, to remotely sense the output voltage. Remote sensing lets the converter sense the output voltage directly at the point-of-load and increases the accuracy of the output voltage regulation. These sense lines must be routed in parallel and away from noisy signals. Connect them to the lowest impedance point on the output bus, which must be the center of the output capacitor bank closest to the load.

In a stacked configuration, VOSNS and GOSNS of the primary and all secondary devices must be connected. For further details, please see セクション 7.3.17.

7.3.16 Thermal Warning and Shutdown

The device has a two-level overtemperature detection function.

If the junction temperature rises above the thermal warning threshold of 150°C (typical), the device sets the TWARN bit in the STATUS register. The device clears the TWARN bit if the STATUS register is read after the junction temperature fell below the TWARN threshold of 130°C (typical).

If the junction temperature rises above the thermal shutdown threshold of 170°C (typical), the device:

- Stops switching
- Pulls down the EN pin (if SINGLE = 0 in the CONTROL3 register)
- Enables the output discharge (if DISCHEN = 1 in the CONTROL1 register)
- Sets the TSHUT bit in the STATUS register
- Pulls the PG pin low

If the junction temperature then falls below the thermal shutdown threshold of 150°C (typical), the device:

- Starts switching again, starting with a new soft-start sequence
- Releases the EN pin (high impedance)
- Releases the PG pin (high-impedance)

The device clears the TSHUT bit if the user reads the STATUS register after the junction temperature fell below the TSHUT threshold of 150°C (typical).

In a stacked configuration, in which all devices share a common enable signal, a thermal shutdown condition in one device disables the entire stack. When the hot device cools down, the whole stack automatically starts switching again.

7.3.17 Stacked Operation

The user can connect multiple devices in parallel in what is known as a "stack" to increase output current capability, to reduce device junction temperature or the output voltage ripple. For example, paralleling four 15A

devices can provide up to 60A of current. More devices can be stacked, as long as the PCB layout maintains the integrity of the shared signals between the modules.

A stack comprises one *primary* device and one or more *secondary* devices. During initialization, each device monitors the SYNC_OUT pin to determine if the SYNC_OUT pin must operate as a primary device or a secondary device:

- If there is a 47kΩ resistor between the SYNC_OUT pin and ground, the device operates as a secondary device.
- If the SYNC_OUT pin is high impedance, the device operates as a primary device.

図 7-21 shows the recommended interconnections in a stack of two TPSM8287A1xM devices.

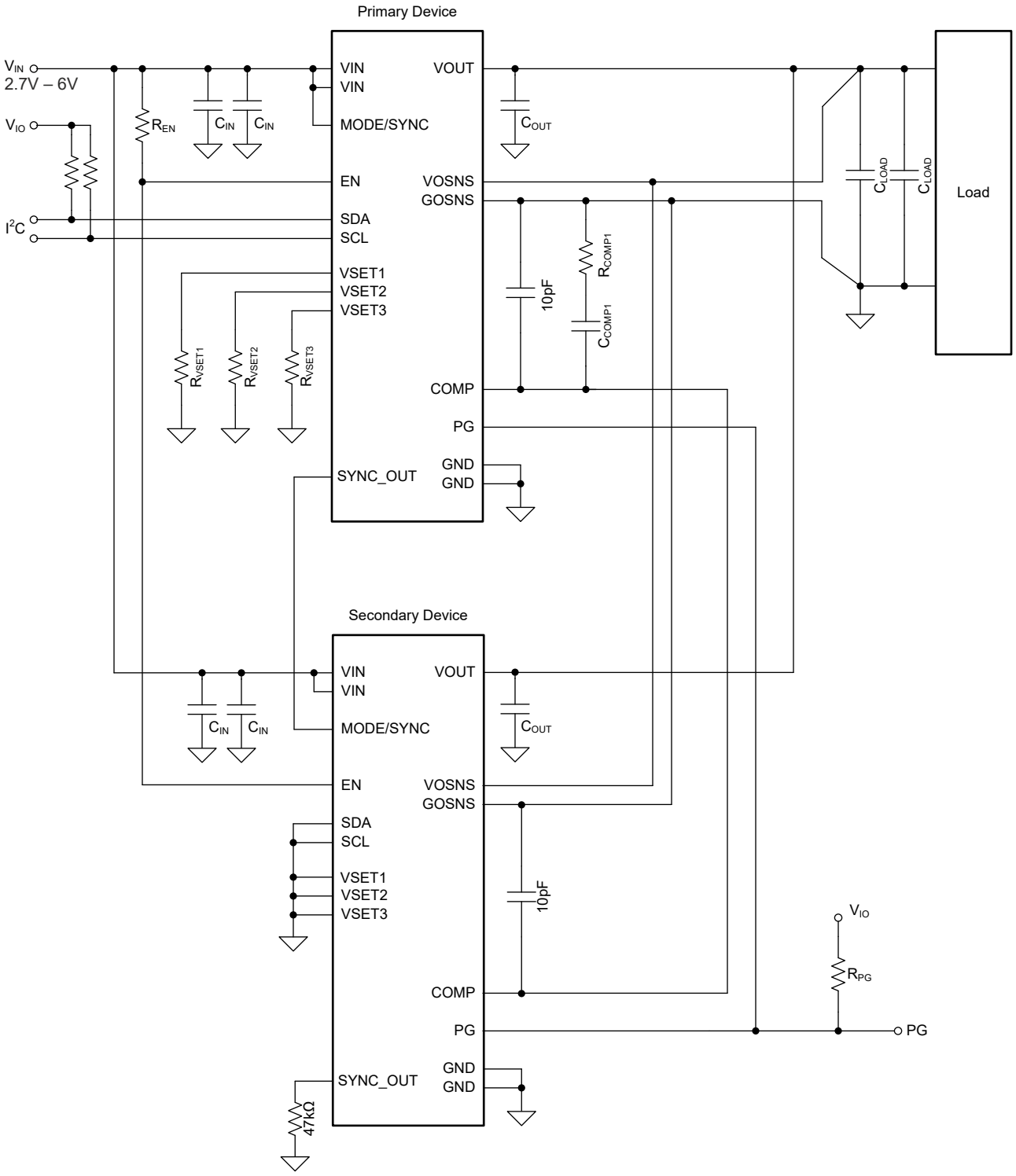


図 7-21. Two TPSM8287A1xM Devices in a Stacked Configuration

The key points to note are:

- All the devices in the stack share a common enable signal, which must be pulled up with a resistance of at least 15kΩ.
- All secondary devices must connect a 47kΩ resistor between the SYNC_OUT pin and ground.

- All the devices in the stack share a common power-good signal, which must be pulled up with a resistor to a logic high level.
- All the devices in the stack share a common compensation signal.
- The remote sense pins (VOSNS and GOSNS) *of each device* must be connected (do not leave these pins floating).
- The same device part number (with the same frequency and output current) must be used for all devices in the stack.
- The primary device must be configured for forced-PWM operation (secondary devices are automatically configured for forced-PWM operation).
- A stacked configuration can support synchronization to an external clock or spread-spectrum clocking.
- Only the VSETx pins of the primary device are used to set the default output voltage. The VSETx pins of secondary devices are not used and must be connected to ground.
- The SDA and SCL pins of secondary devices are not used and must be connected to ground.
- A stacked configuration uses a daisy-chained clocking signal, in which each device switches with a phase offset of approximately 140° relative to the previous device in the daisy-chain. To daisy-chain the clocking signal, connect the SYNC_OUT pin of the primary device to the MODE/SYNC pin of the first secondary device. Connect the SYNC_OUT pin of the first secondary device to the MODE/SYNC pin of the second secondary device. Continue this connection scheme for all devices in the stack to daisy-chain them together.
- Hiccup overcurrent protection must not be used in a stacked configuration.
- For output voltages >=1.2V, reduce the maximum output current per phase by 1A to account for current balancing inaccuracy.

In a stacked configuration, the common enable signal also acts as a SYSTEM_READY signal (see セクション 7.3.3). Each device in the stack can pull the EN pin low during device start-up or when a fault occurs. Thus, the stack is only enabled when all devices have completed the start-up sequence and are fault-free. A fault in any one device disables the whole stack for as long as the fault condition exists.

During start-up, the primary converter pulls the COMP pin low for as long as the enable signal (SYSTEM_READY) is low. When the enable signal goes high, the primary device actively controls the COMP pin and all converters in the stack follow the COMP voltage. During start-up, each device in the stack pulls the PG pin low while he device initializes. When initialization is complete, each secondary device in the stack sets the PG pin to high impedance and the primary device alone controls the state of the PG signal. The PG pin goes high when the stack has completed the start-up ramp and the output voltage is within the power good window. The secondary converters in the stack detect the rising edge of the power-good signal and switch to FPWM operation. After the stack has successfully started up, the primary device controls the power-good signal in the normal way. In a stacked configuration, there are some faults that only affect individual devices, and other faults that affect all devices. For example, if one device enters current limit, only that device is affected. But a thermal shutdown or undervoltage lockout event in one device disables all devices through the shared enable (SYSTEM_READY) signal. For details refer to 表 7-7.

Functionality During Stacked Operation

Some device features are not available during stacked operation, or are only available in the primary converter. 表 7-6 summarizes the available functionality during stacked operation.

表 7-6. Functionality During Stacked Operation

Function	Primary Device	Secondary Device	Remark
UVLO	Yes	Yes	Common enable signal
OVLO	Yes	Yes	Common enable signal
OCP – current limit	Yes	Yes	Individual device
OCP – hiccup OCP	No	No	Do not use during stacked operation
Thermal shutdown	Yes	Yes	Common enable signal
Power Good (Window Comparator)	Yes	No	Primary device only

表 7-6. Functionality During Stacked Operation (続き)

Function	Primary Device	Secondary Device	Remark
I²C interface	Yes	No	Primary device only
DVS	Through I²C	No	Voltage loop controlled by primary device only
SSC	Through I²C	Yes, through primary device	Daisy-chained from primary device to secondary devices
SYNC	Yes	Yes, through primary device	Synchronization clock applied to primary device and daisy-chained from primary device to secondary devices
Precise enable	No	No	Only binary enable
Output discharge	Through I²C	Yes	Always enabled in secondary devices

Fault Handling During Stacked Operation

In a stacked configuration, there are some faults that only affect individual devices, and other faults that affect all devices. For example, if one device enters current limit, only that device is affected. But a thermal shutdown or undervoltage lockout event in one device disables all devices through the shared enable (SYSTEM_READY) signal. 表 7-7 summarizes the fault handling during stacked operation.

表 7-7. Fault Handling During Stacked Operation

Fault Condition	Device Response	System Response
UVLO	Enable signal pulled low	New soft start
OVLO		
Thermal shutdown		
Current limit	Enable signal remains high	Error amplifier clamped

7.4 Device Functional Modes

7.4.1 Power-On Reset (POR)

The device operates in POR mode when the supply voltage is less than the POR threshold (V_{POR-}).

In POR mode, no functions are available and the device resets the registers to the default values.

The device leaves POR mode and enters UVLO mode when the supply voltage increases above the POR threshold.

7.4.2 Undervoltage Lockout

The device operates in UVLO mode when the supply voltage is between the POR and UVLO thresholds.

If the device enters UVLO mode from POR mode, no functions are available. If the device enters UVLO mode from Standby mode, the output discharge function is available. The I²C interface is not available in UVLO mode.

The device leaves UVLO mode and enters POR mode when the supply voltage decreases below the POR threshold. The device leaves UVLO mode and enters Standby mode when the supply voltage increases above the UVLO threshold.

7.4.3 Standby

The device operates in standby mode when the supply voltage is greater than the UVLO threshold and any of the following conditions is true:

- A low level is applied to the EN pin
- SWEN = 0 in the CONTROL1 register

- The device junction temperature is greater than the thermal shutdown threshold
- The supply voltage is greater than the OVLO threshold
- The device is initializing

The following functions are available in standby mode:

- I^2C interface
- Output discharge
- Power good

The device leaves standby mode and enters UVLO mode when the supply voltage decreases below the UVLO threshold. The device leaves standby mode and enters on mode when all of the following conditions are true:

- A high-level is applied to the EN pin
- SWEN = 1 in the CONTROL1 register
- The device junction temperature is below the thermal shutdown threshold
- The supply voltage is below the OVLO threshold

7.4.4 On

The device operates in on mode when the supply voltage is greater than the UVLO threshold and all of the following conditions are true:

- A high-level is applied to the EN pin
- SWEN = 1 in the CONTROL1 register
- The device junction temperature is below the thermal shutdown threshold
- The supply voltage is below the OVLO threshold

All functions are available in on mode.

The device leaves on mode and enters UVLO mode when the supply voltage decreases below the UVLO threshold. The device leaves on mode and enters the standby mode when any of the following conditions is true:

- A low level is applied to the EN pin
- SWEN = 0 in the CONTROL1 register
- The device junction temperature is greater than the thermal shutdown threshold
- The supply voltage is greater than the OVLO threshold

7.5 Programming

7.5.1 Serial Interface Description

I^2C is a 2-wire serial interface developed by Philips Semiconductor, now NXP Semiconductors (see I^2C-Bus Specification and User Manual, Revision 6, 4 April 2014). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All I^2C-compatible devices connect to the I^2C bus through open drain I/O pins, SDA and SCL. A *controller*, usually a microcontroller or a digital signal processor, controls the bus. The controller is responsible for generating the SCL signal and device addresses. The controller also generates specific conditions that indicate the START and STOP of data transfer. A *target* receives and transmits data on the bus under control of the controller.

The TPSM8287A1xM device operates as a target and supports the following data transfer *modes*, as defined in the I^2C-Bus Specification: standard mode (100kbps), fast mode (400kbps), and fast mode plus (1Mbps). The interface adds flexibility to the power supply design, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as the input voltage remains above V_{POR-}.

The data transfer protocol for standard and fast modes is exactly the same, therefore the modes are referred to as F/S mode in this document. The device supports 7-bit addressing; general call addresses are not supported.

The state of the VSETx pins during power-up defines the I^2C target address of the device (see 表 7-2).

TI recommends that the I^2C controller initiates a STOP condition on the I^2C bus after the initial power up of the SDA and SCL pullup voltages to make sure a reset of the I^2C engine.

7.5.2 Standard-, Fast-, Fast-Mode Plus Protocol

The controller initiates a data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in 図 7-22. All I²C-compatible devices must recognize a start condition.

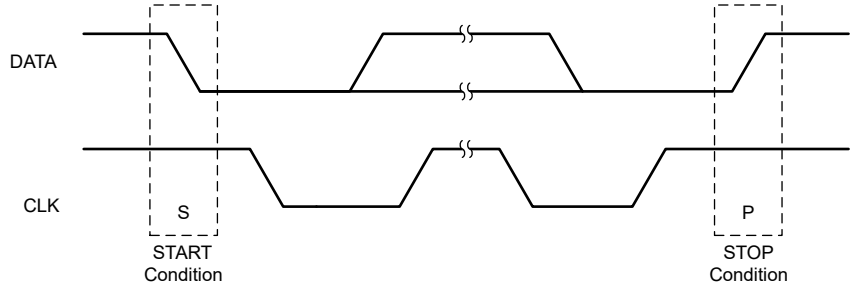


図 7-22. START and STOP Conditions

The controller then generates the SCL pulses, and transmits the 7 bit address and the read/write direction bit R/$\overline{W}$ on the SDA line. During all transmissions, the controller makes sure that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see 図 7-23). All devices recognize the address sent by the controller and compare the address to the internal fixed addresses. Only the target with a matching address generates an acknowledge (see 図 7-24) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the controller knows that communication link with a target has been established.

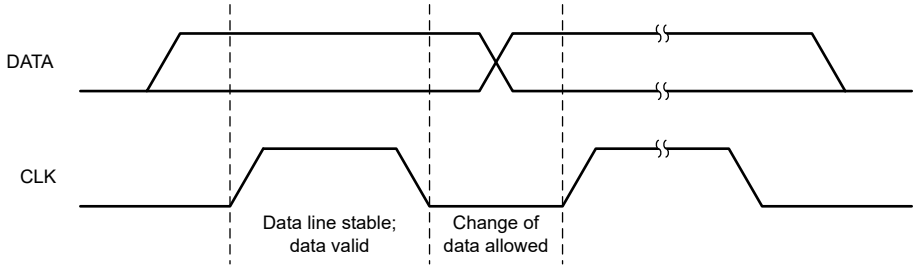


図 7-23. Bit Transfer on the Serial Interface

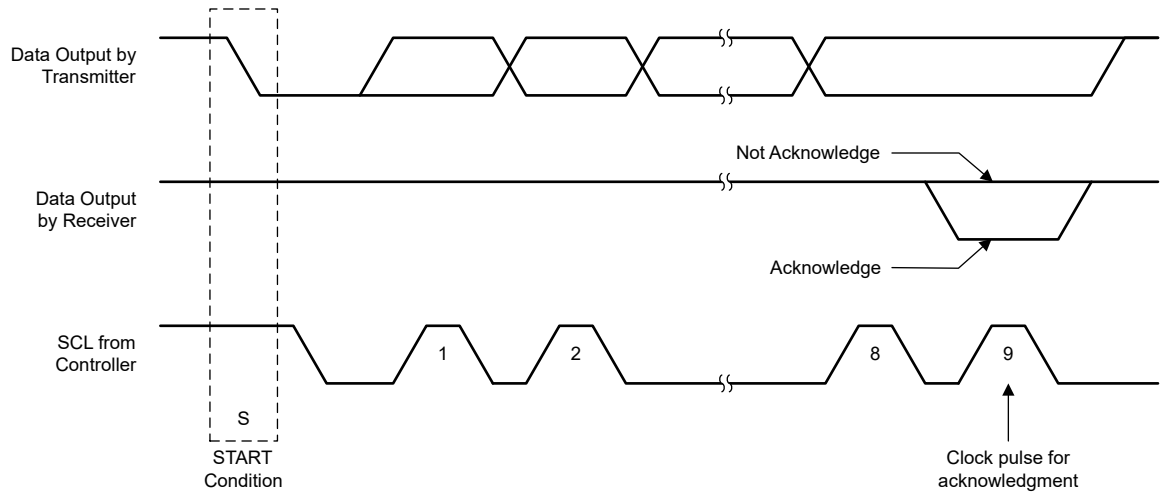


図 7-24. Acknowledge on the I²C Bus

The controller generates further SCL cycles to either transmit data to the target (R/$\overline{W}$ bit 0) or receive data from the target (R/$\overline{W}$ bit 1). In either case, the target must acknowledge the data sent by the controller. So an acknowledge signal can either be generated by the controller or by the target, depending on which one is the receiver. 9bit valid data sequences consisting of 8bit data and 1bit acknowledge can continue as long as necessary (see 図 7-25).

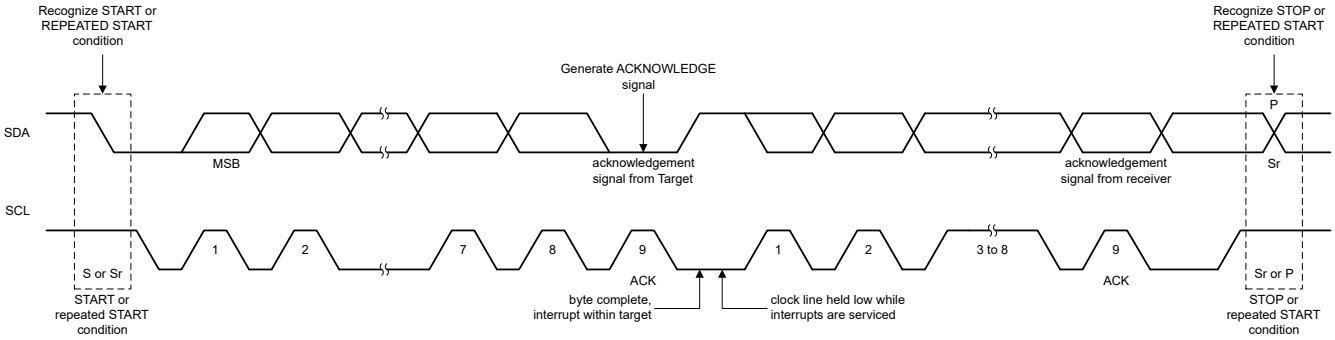


図 7-25. Bus Protocol

To signal the end of the data transfer, the controller generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see 図 7-22). This action releases the bus and stops the communication link with the addressed target. All I^2C-compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and the devices wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section results in 0x00 being read out.

7.5.3 I^2C Update Sequence

A start condition, a valid I^2C address, a register address byte, and a data byte are required for a single update. After the receipt of each byte, the receiving device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I^2C address selects the target. The target performs an update on the falling edge of the acknowledge signal that follows the LSB byte.

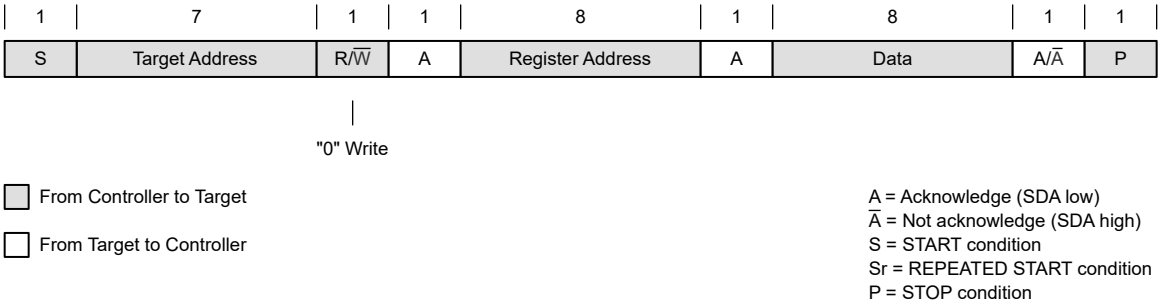


図 7-26. “Write” Data Transfer Format in Standard-, Fast, Fast-Plus Modes

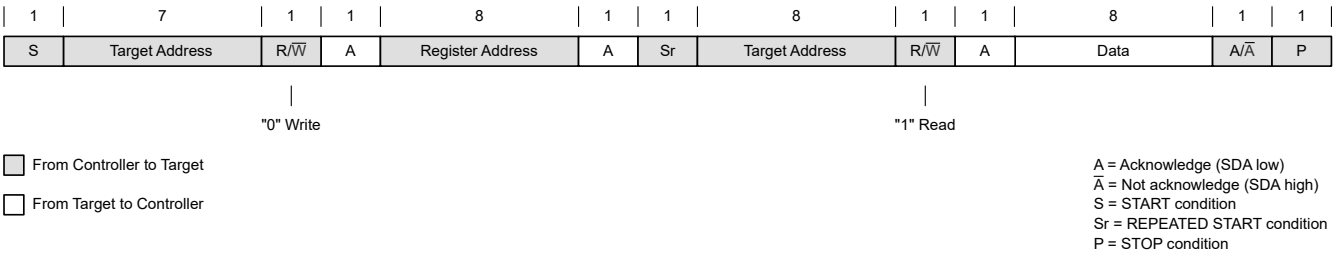


図 7-27. “Read” Data Transfer Format in Standard-, Fast, Fast-Plus Modes

7.5.4 I²C Register Reset

The I²C registers can be reset by:

- Pulling the input voltage below V_{POR-} (see セクション 7.4.1).
- Setting the RESET bit in the CONTROL register. When RESET = 1, all registers are reset to the default values and a new start-up begins immediately. After $t_{d(EN)2}$, all I²C registers can be accessed again.

8 Device Registers

表 8-1 lists the Device registers. All register addresses not listed in 表 8-1 must be considered as reserved locations and the register contents must not be modified.

表 8-1. Device Registers

Address	Acronym	Register Name	Section
0h	VSET	Output Voltage Setpoint	Go
1h	CONTROL1	Control 1	Go
2h	CONTROL2	Control 2	Go
3h	CONTROL3	Control 3	Go
4h	STATUS	Status	Go

Complex bit access types are encoded to fit into small table cells. 表 8-2 shows the codes that are used for access types in this section.

表 8-2. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
- *n*		Value after reset or the default value

8.1 VSET Register (Address = 0h) [Reset = X]

VSET is shown in 図 8-1 and described in 表 8-3.

Return to the Summary Table.

This register controls the output voltage setpoint

図 8-1. VSET Register

7	6	5	4	3	2	1	0
VSET							
R/W-X							

表 8-3. VSET Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VSET	R/W	X	Output voltage setpoint (see also the range-setting bits in the CONTROL2 register). Range 1: Output voltage setpoint = 0.4V + VSET[7:0] × 1.25mV Range 2: Output voltage setpoint = 0.4V + VSET[7:0] × 2.5mV Range 3: Output voltage setpoint = 0.4V + VSET[7:0] × 5mV Range 4: Output voltage setpoint = 0.8V + VSET[7:0] × 10mV The state of the VSETx pins during power up determines the reset value. (See 表 7-2).

8.2 CONTROL1 Register (Address = 1h) [Reset = 2Ah]

CONTROL1 is shown in 図 8-2 and described in 表 8-4.

Return to the Summary Table.

This register controls various device configuration options

図 8-2. CONTROL1 Register

7	6	5	4	3	2	1	0
RESET	SSCEN	SWEN	FPWMEN	DISCHEN	HICCUPEN	VRAMP	
R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-1b	R/W-0b	R/W-10b	

表 8-4. CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESET	R/W	0b	Reset device. 0b = No effect 1b = Resets all registers to the default values. The device then performs another initialization. Reading this bit always returns 0.
6	SSCEN	R/W	0b	Spread spectrum clocking enable. 0b = SSC operation disabled 1b = SSC operation enabled
5	SWEN	R/W	1b	Software enable. 0b = Switching disabled (register values retained) 1b = Switching enabled (without the enable delay $t_{d(EN)1}$)
4	FPWMEN	R/W	0b	Forced-PWM enable. 0b = Power-save operation enabled 1b = Forced-PWM operation enabled This bit is logically ORed with the MODE/SYNC pin: If a high level or a synchronization clock is applied to the the MODE/SYNC pin, the device operates in Forced-PWM, regardless of the state of this bit.
3	DISCHEN	R/W	1b	Output discharge enable. 0b = Output discharge disabled. 1b = Output discharge enabled.
2	HICCUPEN	R/W	0b	Hiccup operation enable. 0b = Hiccup operation disabled 1b = Hiccup operation enabled. Do not enable Hiccup operation during stacked operation
1-0	VRAMP	R/W	10b	Output voltage ramp speed when changing from one output voltage setting to another. 00b = 10mV/µs 01b = 5mV/µs 10b = 1.25mV/µs 11b = 0.5mV/µs

8.3 CONTROL2 Register (Address = 2h) [Reset = X]

CONTROL2 is shown in 図 8-3 and described in 表 8-5.

Return to the Summary Table.

This register controls various device configuration options

図 8-3. CONTROL2 Register

7	6	5	4	3	2	1	0
RESERVED				VRANGE		SSTIME	
R-0000b				R/W-X		R/W-01b	

表 8-5. CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000b	Reserved for future use. To make sure compatibility with future device variants, program these bits to 0.
3-2	VRANGE	R/W	X	Output voltage range. 00b = 0.4V to 0.71875V in 1.25mV steps 01b = 0.4V to 1.0375V in 2.5mV steps 10b = 0.4V to 1.675V in 5mV steps 11b = 0.8V to 3.35V in 10mV steps. The state of the VSETx pins during power up determines the reset value. See 表 7-2.
1-0	SSTIME	R/W	01b	Soft-start ramp time. 00b = 0.5ms 01b = 1ms 10b = 2ms 11b = 4ms

8.4 CONTROL3 Register (Address = 3h) [Reset = 0h]

CONTROL3 is shown in 図 8-4 and described in 表 8-6.

Return to the Summary Table.

This register controls various device configuration options

図 8-4. CONTROL3 Register

7	6	5	4	3	2	1	0
RESERVED						SINGLE	PGBLNKDVS
R-000000b						R/W-0b	R/W-0b

表 8-6. CONTROL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000b	Reserved for future use. To make sure compatibility with future device variants, program these bits to 0.
1	SINGLE	R/W	0b	Single operation. This bit controls the internal EN pulldown and SYNC_OUT functions. 0b = EN pin pulldown and SYNC_OUT enabled. 1b = EN pin pulldown and SYNC_OUT disabled. Do not use during stacked operation. In standalone operation, increases I_{Q_VIN} by 200µA typical.
0	PGBLNKDVS	R/W	0b	Power-good blanking during DVS. 0b = PG pin reflects the output of the window comparator 1b = PG pin is high impedance during DVS

8.5 STATUS Register (Address = 4h) [Reset = 2h]

STATUS is shown in 図 8-5 and described in 表 8-7.

Return to the Summary Table.

This register returns the device status flags

図 8-5. STATUS Register

7	6	5	4	3	2	1	0
RESERVED		HICCUP	ILIM	TWARN	TSHUT	PBUV	PBOV
R-00b		R-0b	R-0b	R-0b	R-0b	R-1b	R-0b

表 8-7. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved for future use. To make sure compatibility with future device variants, ignore these bits.
5	HICCUP	R	0b	Hiccup. This bit reports whether a hiccup event occurred since the last time the STATUS register was read. 0b = No hiccup event occurred 1b = A hiccup event occurred
4	ILIM	R	0b	Current limit. This bit reports whether a current limit event occurred since the last time the STATUS register was read. 0b = No current limit event occurred 1b = A current limit event occurred
3	TWARN	R	0b	Thermal warning. This bit reports whether a thermal warning event occurred since the last time the STATUS register was read. 0b = No thermal warning event occurred 1b = A thermal warning event occurred
2	TSHUT	R	0b	Thermal shutdown. This bit reports whether a thermal shutdown event occurred since the last time the STATUS register was read. 0b = No thermal shutdown event occurred 1b = A thermal shutdown event occurred
1	PBUV	R	1b	Power-bad undervoltage. This bit reports whether a power-bad event (output voltage too low) occurred since the last time the STATUS register was read. 0b = No power-bad undervoltage event occurred 1b = A power-bad undervoltage event occurred
0	PBOV	R	0b	Power-bad overvoltage. This bit reports whether a power-bad event (output voltage too high) occurred since the last time the STATUS register was read. 0b = No power-bad overvoltage event occurred 1b = A power-bad overvoltage event occurred

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The following section discusses selection of the external components to complete the power supply design for typical a application.

The required power inductor is integrated inside the TPSM8287A1xM, as shown in the block diagram. The integrated shielded inductor inductance and tolerance are found in 表 4-1. All TPSM8287A1xM versions are pin-to-pin compatible, though the inductance and frequency is different between the versions. Check the values for the specific device before starting the design procedure below.

9.2 Typical Application

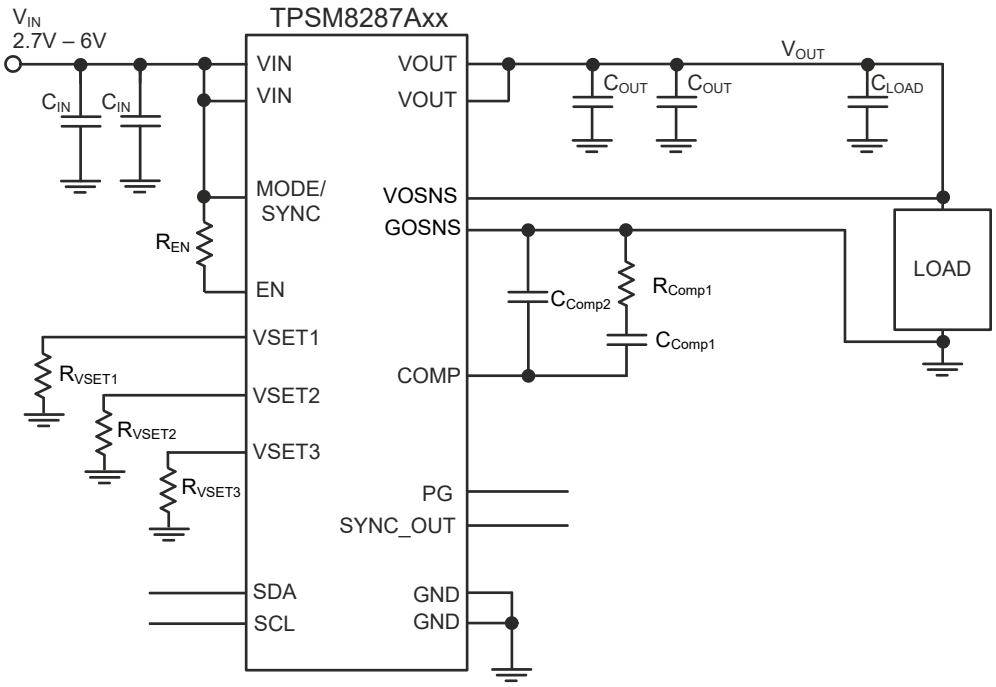


図 9-1. Typical Application Schematic

表 9-1. List of Components

REFERENCE	VALUE	DESCRIPTION	PART NUMBER	MANUFACTURER [1]
C_{Comp1}	6800pF	Ceramic Capacitor, X7R	Std	Std
C_{Comp2}	10pF	Ceramic Capacitor, C0G/NP0	Std	Std
C_{OUT}	2 × 47µF	Ceramic Capacitor, 6.3V, X6S, size 0805	GRM21BC80J476ME01L	Murata
C_{LOAD}	220µF	Ceramic Capacitor, 4V, X6S, size 1210	GRM32EC80G227ME05L	Murata
C_{IN}	2 × 22µF	Ceramic Capacitor, 10V, X7R, size 0805	GRM21BZ71A226ME15L	Murata
R_{Comp1}	806Ω	Resistor 1%, 0.1W	Std	Std
R_{VSET1}, R_{VSET2}, R_{VSET3}	set per 表 7-2	Resistor 5%, 0.1W	Std	Std

表 9-1. List of Components (続き)

REFERENCE	VALUE	DESCRIPTION	PART NUMBER	MANUFACTURER (1)
R_{EN}	15kΩ	Resistor 5%, 0.1W	Std	Std

(1) See the *Third-Party Products Disclaimer*

9.2.1 Design Requirements

表 9-2 lists the operating parameters for this application example with the TPSM8287A12BBM device.

表 9-2. Design Parameters

SYMBOL	PARAMETER	VALUE
V_{IN}	Input voltage	2.7V – 6.0V
V_{OUT}	Output voltage	0.90V
TOL_{VOUT}	Output voltage tolerance allowed by the application	±4.0%
TOL_{DC}	Output voltage tolerance of the TPSM8287A12BBM (DC accuracy)	±1.0%
$\Delta I_{OUT(step)}$	Output current load step	±8.0A
t_t	Load step transition time	1µs
f_{SW}	Switching frequency	2.25MHz
L	Integrated inductor	100nH
TOL_{IND}	Integrated inductor tolerance	±20%
g_m	Error amplifier transconductance	1.5mS
τ	Emulated current time constant	12.5µs
TOL_τ	Tolerance of the emulated current time constant	±30%
BW_τ	Target loop bandwidth	300kHz
N_Φ	Number of paralleled devices (phases)	1

Preliminary Calculations

The maximum allowable deviation of the power supply is ±4.0%. The DC accuracy of the TPSM8287A1xM is specified as ±1.0%, and therefore the maximum output voltage variation during a transient is given by:

$$\Delta V_{OUT} = \pm V_{OUT} \times (TOL_{VOUT} - TOL_{DC}) \quad (5)$$

$$\Delta V_{OUT} = \pm V_{OUT} \times (4.0\% - 1.0\%) = \pm 27mV \quad (6)$$

式 7 computes the peak-to-peak inductor current ripple, which is the greatest at the maximum input voltage:

$$I_{L(PP)} = \frac{V_{OUT}}{V_{IN(max)}}\left(\frac{V_{IN(max)} - V_{OUT}}{L \times f_{sw}}\right) \quad (7)$$

$$I_{L(PP)} = \frac{0.9}{6.0}\left(\frac{6.0 - 0.9}{100 \times 10^{-9} \times 2.25 \times 10^{6}}\right) = 3.4A \quad (8)$$

The maximum load step occurs when the load step from the application occurs at exactly the same time as the peak (or trough) of the inductor ripple current, and is given by:

$$\Delta I_{OUT(max)} = \Delta I_{OUT(step)} + \frac{\Delta I_{L(PP)}}{2 \times N\Phi} \quad (9)$$

$$\Delta I_{OUT(max)} = 8.0 + \frac{3.4}{2 \times 1} = 9.7A \quad (10)$$

9.2.2 Detailed Design Procedure

The following subsections describe how to calculate the external components required to meet the specified transient requirements of a given application. The calculations include the worst-case variation of components and use the RMS method to combine the variation of uncorrelated parameters.

See *TPSM8287A-COMPONENT-CALCULATOR* for a spreadsheet component calculator with the following calculations.

9.2.2.1 Selecting the Input Capacitors

The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. TI recommends a X7R multilayer ceramic capacitor (MLCC) for best filtering and must be placed between both VIN and GND pins, as close as possible to those pins. For applications with ambient temperatures below 85°C, a capacitor with X5R dielectric can be used. Ceramic capacitors have a DC-Bias effect, which has a strong influence on the final effective capacitance. Choose the right capacitor carefully in combination with considering the package size and voltage rating. The two high frequency input capacitors are placed inside the module to reduce EMI, shrink the overall design size and to simplify the board layout. As those integrated capacitors target high frequencies, additional external capacitors with a minimum of 5µF are required per VIN pin.

The TPSM8287A1xM devices feature a *butterfly* or parallel layout with two pairs of VIN and GND pins on opposite sides of the package. This feature allows the input capacitors to be placed symmetrically on the PCB so that the electromagnetic fields cancel each other out, thereby reducing EMI. In addition, the parasitic loop inductance between the input capacitors and the IC is reduced through this pinout.

The duty cycle of the converter is given by:

$$D = \frac{V_{OUT}}{\eta \times V_{IN}} \tag{11}$$

where:

- V_{IN} is the input voltage
- V_{OUT} is the output voltage
- η is the efficiency

$$D = \frac{0.90}{0.83 \times 2.7} = 0.402 \tag{12}$$

The value of input capacitance needed to meet any system-level input voltage ripple requirement is given by 式 13. For this example, the lowest input voltage and highest load current are used to generate a worst case input voltage ripple of 100mV.

$$C_{IN} = \frac{D \times (1 - D) \times I_{OUT}}{V_{IN(PP)} \times f_{sw}} \tag{13}$$

where:

- D is the duty cycle
- f_{sw} is the switching frequency
- L is the inductance
- I_{OUT} is the output current

$$C_{IN} = \frac{0.402 \times (1 - 0.402) \times 12.0}{0.1 \times 2.25 \times 10^{6}} = 12.8\mu F \tag{14}$$

The value of C_{IN} calculated with 式 13 is the *effective* capacitance after all derating, tolerance, and aging effects have been considered.

9.2.2.2 Selecting the Target Loop Bandwidth

The control loop bandwidth measures how quickly the device responds to a change in output voltage. With the TPSM8287A1xM external compensation, the loop bandwidth is adjustable to balance the tradeoff of a fast response versus stability and ringing. The R_{Comp1} resistor and output capacitance are the primary means of adjusting the loop bandwidth.

TI recommends setting the target loop bandwidth to 200kHz for a simple design. If strong load transients are expected in the application, the target bandwidth can be set as high as ¼ of the switching frequency. A target bandwidth of 300kHz is used for this example design.

9.2.2.3 Selecting the Compensation Resistor

Use 式 15 to calculate the recommended value of compensation resistor, R_{Comp1}:

$$R_{Comp1} = \frac{1}{g_m}\left(\frac{\pi \times \Delta I_{OUT(step)} \times L}{4 \times \tau \times \Delta V_{OUT} \times N\Phi} - 1\right)\left(1 + \sqrt{TOL_{IND}^2 + TOL_{\tau}^2}\right) \quad (15)$$

$$R_{Comp1} = \frac{1}{1.5 \times 10^{-3}}\left(\frac{\pi \times 8.0 \times 100 \times 10^{-9}}{4 \times 12.5 \times 10^{-6} \times 27 \times 10^{-3} \times 1} - 1\right)\left(1 + \sqrt{20\%^2 + 30\%^2}\right) = 781.6\Omega \quad (16)$$

Picking a standard component above the calculated value, a 806Ω resistor is chosen in this example. The selected value must be used for the further calculations.

9.2.2.4 Selecting the Output Capacitors

In practice, the total output capacitance is typically comprised of a combination of different capacitors, in which larger capacitors provide the load current at lower frequencies and smaller capacitors provide the load current at higher frequencies to satisfy the load impedance requirements. The value, type, and location of the output capacitors are typically defined by the load. TI recommends X7R multilayer ceramic capacitors (MLCCs) for best filtering and must be placed between both VOUT and GND pins, as close as possible to those pins. For applications with ambient temperatures below 85°C, capacitors with an X5R dielectric can be used. Ceramic capacitors have a DC-Bias effect, which has a strong influence on the final effective capacitance. Choose the right capacitors carefully in combination with considering the package size and voltage rating. The below calculations use the effective value of the total output capacitance.

The TPSM8287A1xM devices feature a *butterfly* or *parallel* layout with VOUT and GND pins on opposite sides of the package. This feature allows the output capacitors to be placed symmetrically on the PCB such that the electromagnetic fields cancel each other out, thereby reducing EMI.

The TPSM8287A1xM device is optimized to support harsh load transients. The device external loop compensation tunes the loop response to the desired response with a given output capacitance. The below calculations create designs that meet the load step specified in 表 9-2. These calculations typically result in total output capacitances of several hundred µF.

Best output voltage regulation is achieved when the TPSM8287A1xM device, the output capacitors, and load are placed very close to each other, keeping the distance and added inductance between the device and load to the absolute minimum.

In case this placement can not be achieved, then the majority of the total capacitance must be located at the load, with just two capacitors located at the TPSM8287A1xM device. TI recommends that the capacitance located at the load be at least twice the amount of the capacitance located at the device.

If the application does not contain harsh load transients, then smaller values of output capacitances are possible. Do not use output capacitances below the minimum values in *Recommended Operating Conditions*.

The transient response of the converter is defined by one of two criteria:

- The slew rate of the current through the inductor, in which case the feedback loop of the converter saturates.
- The loop bandwidth, in which the converter stays in regulation, and the loop does not saturate ($BW_T < f_{SW} / 4$)

Which of the above criteria applies in any given application depends on the operating conditions and component values used. Calculate the output capacitance for both cases and select the higher of the two values.

If the converter remains in regulation, the minimum required output capacitance is given by:

$$C_{OUT(min)(reg)} = \left(\frac{\tau \times \left(1 + g_m \times R_{Comp1}\right)}{2 \times \pi \times \frac{L}{N\Phi} \times BW_\tau}\right)\left(1 + \sqrt{TOL_\tau{}^2 + TOL_{IND}{}^2 + TOL_{fSW}{}^2}\right) \quad (17)$$

$$C_{OUT(min)(reg)} = \left(\frac{12.5 \times 10^{-6} \times \left(1 + 1.5 \times 10^{-3} \times 806\right)}{2 \times \pi \times \frac{100 \times 10^{-9}}{1} \times 300 \times 10^{3}}\right)\left(1 + \sqrt{30\%^2 + 20\%^2 + 10\%^2}\right) = 201.3\mu F \quad (18)$$

If the converter loop saturates, the minimum output capacitance is given by:

$$C_{OUT(min)(sat)} = \frac{1}{\Delta V_{OUT}}\left(\frac{L \times \Delta I_{OUT(max)}{}^2}{2 \times V_{OUT} \times N\Phi} - \frac{\Delta I_{OUT(step)} \times t_t}{2}\right)(1 + TOL_{IND}) \quad (19)$$

$$C_{OUT(min)(sat)} = \frac{1}{27 \times 10^{-3}}\left(\frac{100 \times 10^{-9} \times 9.7^2}{2 \times 0.9 \times 1} - \frac{8.0 \times 1 \times 10^{-6}}{2}\right)(1 + 20\%) = 54.5\mu F \quad (20)$$

In this case, choose $C_{OUT(min)}$ = 201.3µF as the larger of the two values for the output capacitance.

表 9-1 lists the three output capacitors chosen. 2 × 47µF capacitors are placed close to the IC, giving a minimum effective capacitance of about 27µF each. A single 220µF capacitor is placed near the load to approximate the total decoupling capacitance required by a typical load. This 220µF capacitor yields about 138µF of effective capacitance. Together, the 192µF of effective capacitance is very close to the required minimum value calculated above. For further calculations, use C_{OUT} = 192µF.

式 21 checks that most of the output capacitance is placed at the load. If the ratio is less than 1, increase the capacitance at the load or place the device, output capacitance, and load next to each other such that there is no separation between the output capacitances.

$$\frac{C_{LOAD}}{2 \times C_{OUT}} > 1 \quad (21)$$

$$\frac{138 \times 10^{-6}}{2 \times \left(2 \times 27 \times 10^{-6}\right)} > 1 = \text{True} \quad (22)$$

式 23 calculates the output voltage ripple, based on the effective output capacitance value.

$$V_{OUT(p-p)} = \frac{I_{L(PP)}}{8 \times C_{OUT} \times f_{sw}} \quad (23)$$

$$V_{OUT(p-p)} = \frac{3.4}{8 \times 192 \times 10^{-6} \times 2.25 \times 10^{6}} = 0.984 \ mV \quad (24)$$

The ripple is slightly higher in the application, due to the ESR and ESL in the output capacitors and the application board parasitics.

9.2.2.5 Selecting the Compensation Capacitor, C_{Comp1}

First, use 式 25 to calculate the bandwidth of the inner loop:

$$BW_{INNER} = \frac{\tau}{2\pi \times \frac{L}{N\Phi} \times C_{OUT}} \quad (25)$$

$$BW_{INNER} = \frac{12.5 \times 10^{-6}}{2\pi \times \frac{100 \times 10^{-9}}{1} \times 192 \times 10^{-6}} = 104kHz \quad (26)$$

Next, calculate the product of $g_m R_{Comp1}$:

$$g_m \times R_{Comp1} = 1.5 \times 10^{-3} \times 806 = 1.21 \quad (27)$$

If $g_m R_{Comp1}$ > than 1, use 式 28 to calculate the recommended value of C_{Comp1}, which sets a zero in the control loop. If $g_m R_{Comp1}$ < 1, use 式 30 to calculate the recommended value of C_{Comp1}.

$$C_{Comp1} = \frac{2}{\pi \times BW_{INNER} \times g_m \times {R_{Comp1}}^2} \quad (28)$$

$$C_{Comp1} = \frac{2}{\pi \times 104 \times 10^3 \times 1.5 \times 10^{-3} \times (806)^2} = 6.31nF \quad (29)$$

The closest standard value is 6.8nF.

$$C_{Comp1} = \frac{2 \times g_m}{\pi \times BW_{INNER}} \quad (30)$$

式 31 approximates the loop bandwidth.

$$BW = BW_{INNER} \times 2 \times \left(1 + R_{Comp1} \times g_m\right) \quad (31)$$

$$BW = 104 \times 10^3 \times 2 \times \left(1 + 806 \times 1.5 \times 10^{-3}\right) = 458kHz \quad (32)$$

9.2.2.6 Selecting the Compensation Capacitor, C_{Comp2}

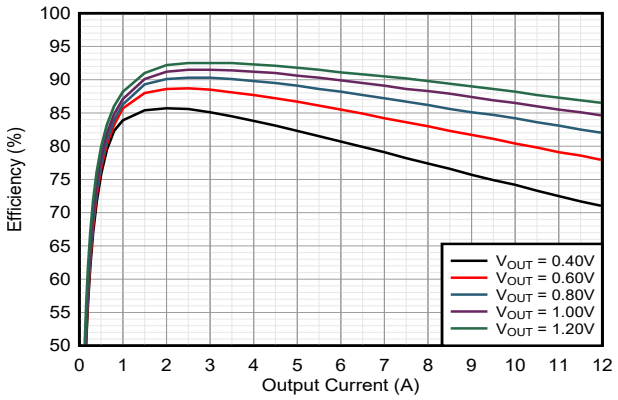
The compensation capacitor, C_{Comp2}, is an optional capacitor that TI recommends the user include to bypass high-frequency noise away from the COMP pin. The value of this capacitor is not critical; 10pF or 22pF capacitors are designed for typical applications.

This capacitor can be made larger to suppress high-frequency zeros or resonances that occur in the system output voltage routing and decoupling network. 式 33 calculates the pole created by C_{Comp2}.

$$f_{pole} = \frac{1}{2 \times \pi \times R_{Comp1} \times C_{Comp2}} \quad (33)$$

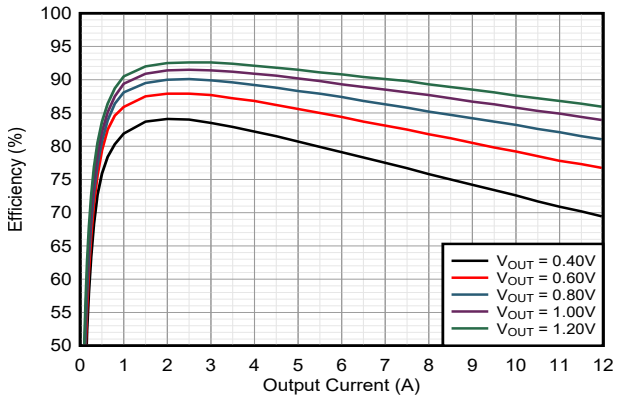
9.2.3 Application Curves

V_{IN} = 5.0V, V_{OUT} = 0.9V, T_A = 25°C, BOM = 表 9-1, unless otherwise noted.



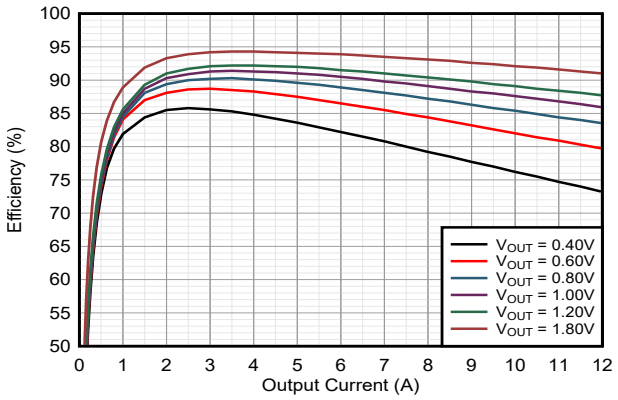
V_{IN} = 2.7V F_{SW} = 1.5MHz FPWM

図 9-2. Efficiency TPSM8287A12BAM



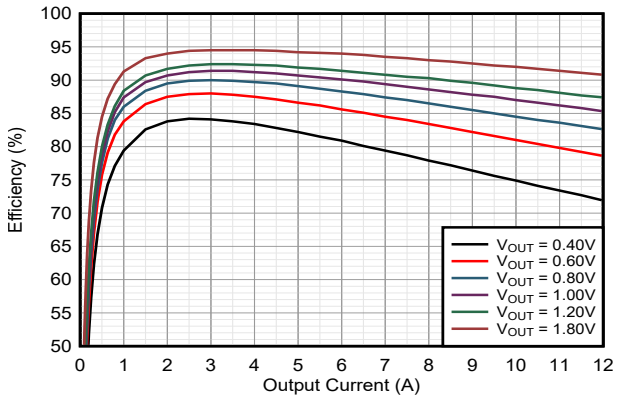
V_{IN} = 2.7V F_{SW} = 2.25MHz FPWM

図 9-3. Efficiency TPSM8287A12BBM



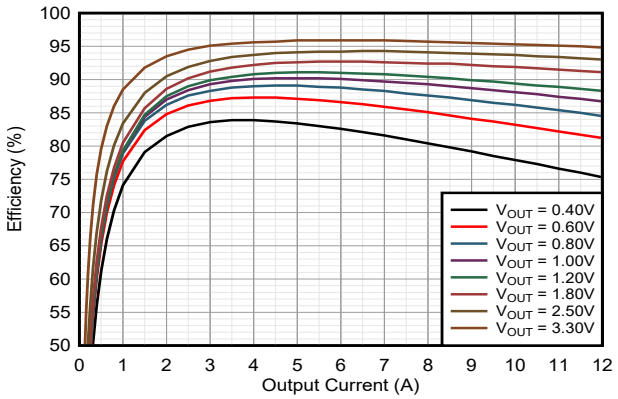
V_{IN} = 3.3V F_{SW} = 1.5MHz FPWM

図 9-4. Efficiency TPSM8287A12BAM



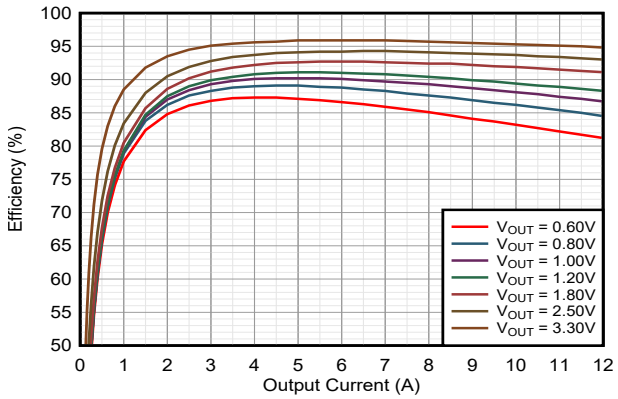
V_{IN} = 3.3V F_{SW} = 2.25MHz FPWM

図 9-5. Efficiency TPSM8287A12BBM



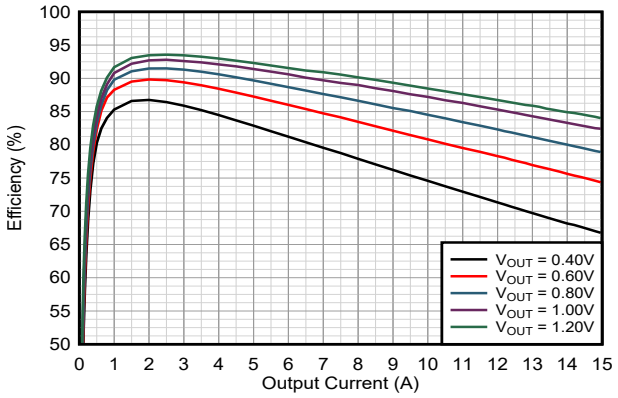
V_{IN} = 5.0V F_{SW} = 1.5MHz FPWM

図 9-6. Efficiency TPSM8287A12BAM



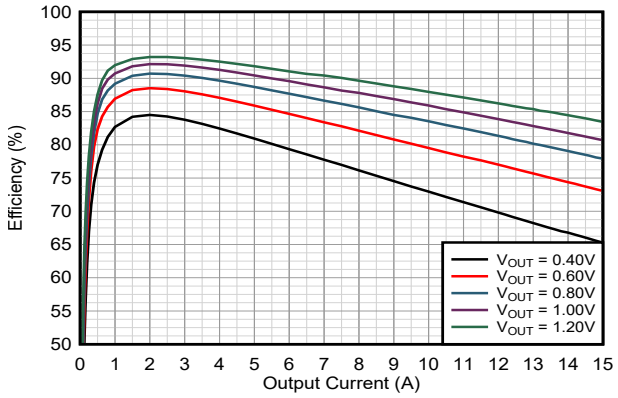
V_{IN} = 5.0V F_{SW} = 2.25MHz FPWM

図 9-7. Efficiency TPSM8287A12BBM



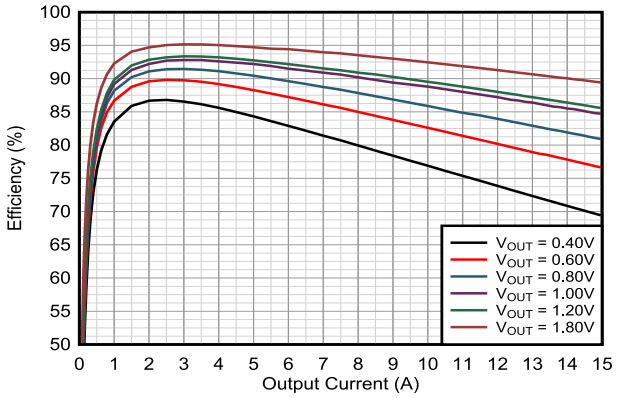
V_{IN} = 2.7V F_{SW} = 1.5MHz FPWM

図 9-8. Efficiency TPSM8287A15BAM



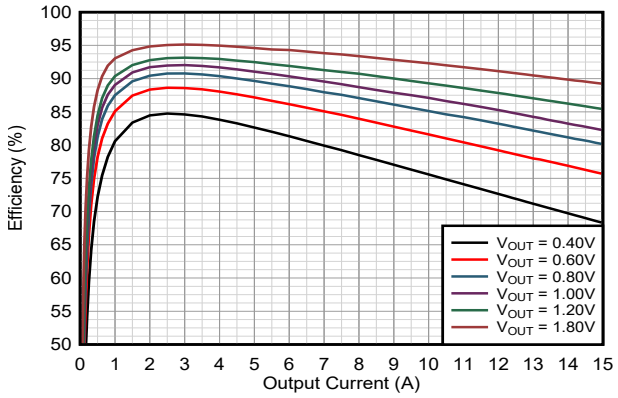
V_{IN} = 2.7V F_{SW} = 2.25MHz FPWM

図 9-9. Efficiency TPSM8287A15BBM



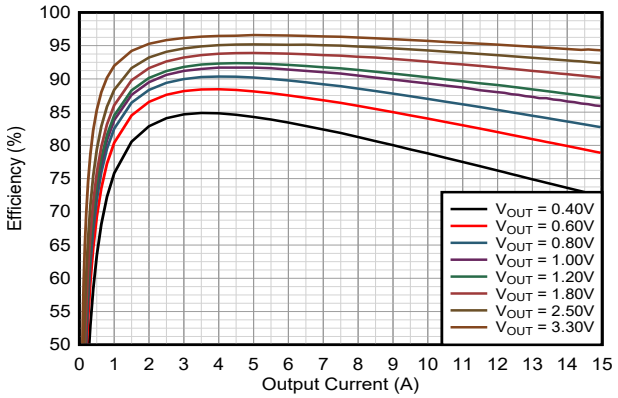
V_{IN} = 3.3V F_{SW} = 1.5MHz FPWM

図 9-10. Efficiency TPSM8287A15BAM



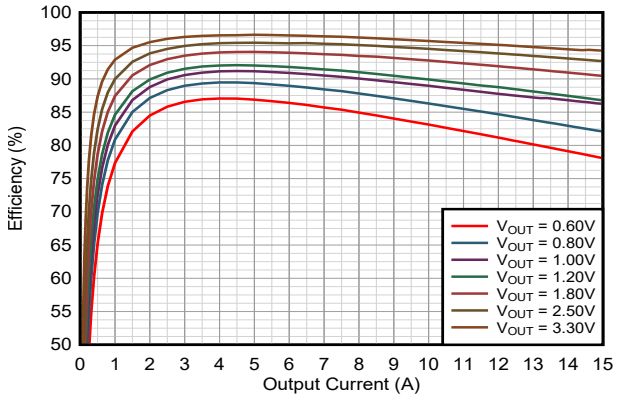
V_{IN} = 3.3V F_{SW} = 2.25MHz FPWM

図 9-11. Efficiency TPSM8287A15BBM



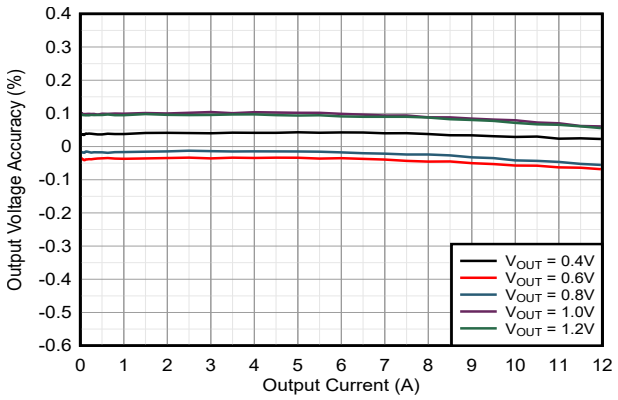
V_{IN} = 5.0V F_{SW} = 1.5MHz FPWM

図 9-12. Efficiency TPSM8287A15BAM



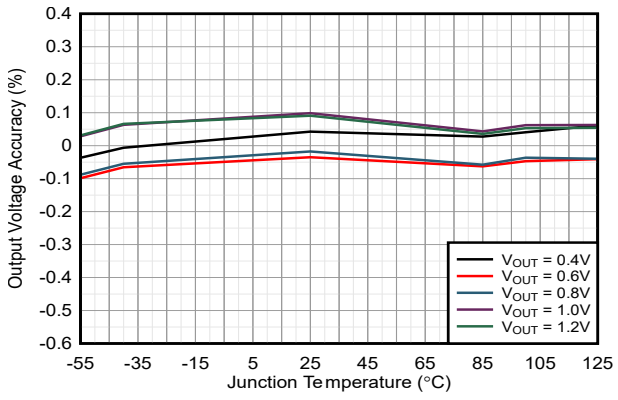
V_{IN} = 5.0V F_{SW} = 2.25MHz FPWM

図 9-13. Efficiency TPSM8287A15BBM



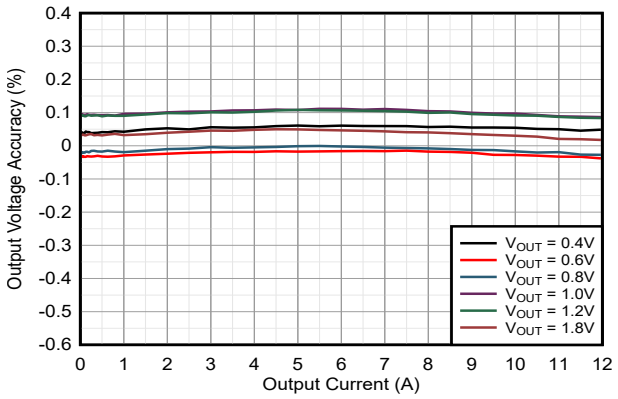
V_{IN} = 2.7V T_J = 25°C FPWM

図 9-14. Load Regulation TPSM8287A12BAM



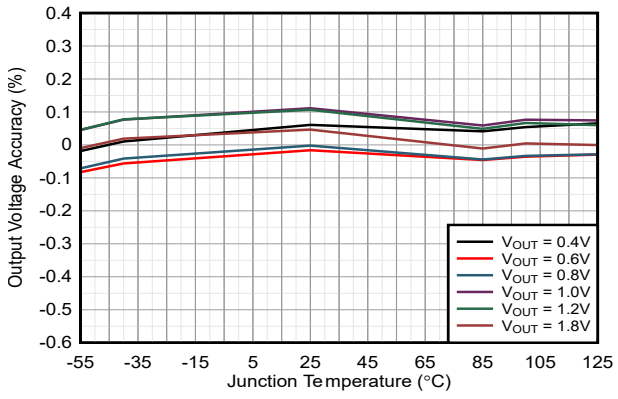
V_{IN} = 2.7V I_{OUT} = 6A FPWM

図 9-15. Vout Accuracy vs Temperature TPSM8287A12BAM



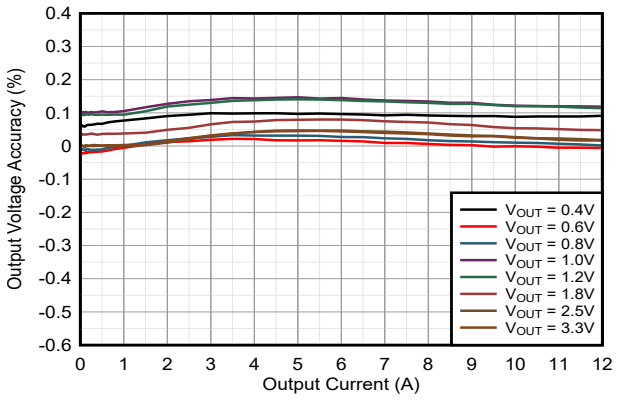
V_{IN} = 3.3V T_J = 25°C FPWM

図 9-16. Load Regulation TPSM8287A12BAM



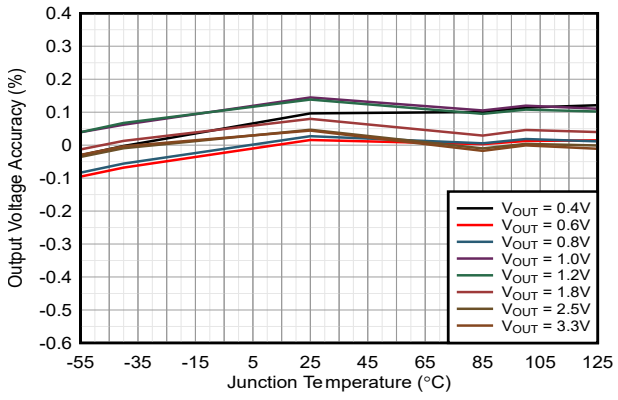
V_{IN} = 3.3V I_{OUT} =6A FPWM

図 9-17. Vout Accuracy vs Temperature TPSM8287A12BAM



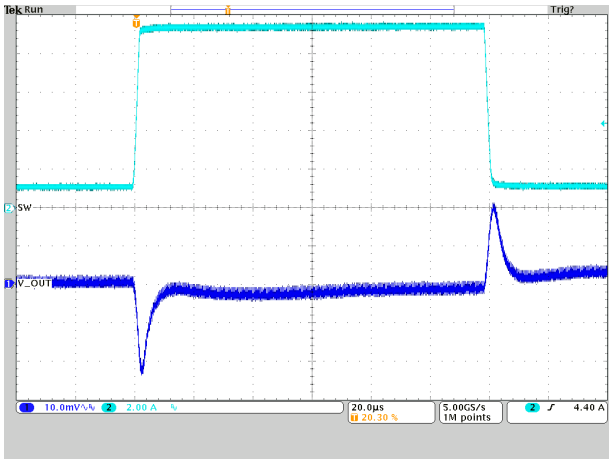
V_{IN} = 5.0V T_J = 25°C FPWM

図 9-18. Load Regulation TPSM8287A12BAM



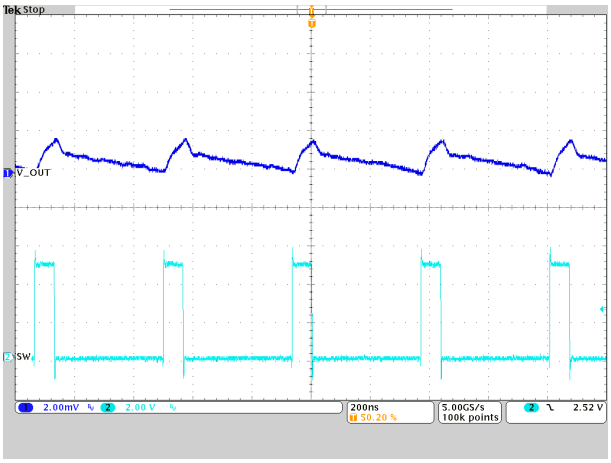
V_{IN} = 5.0V I_{OUT} = 6A FPWM

図 9-19. Vout Accuracy vs Temperature TPSM8287A12BAM



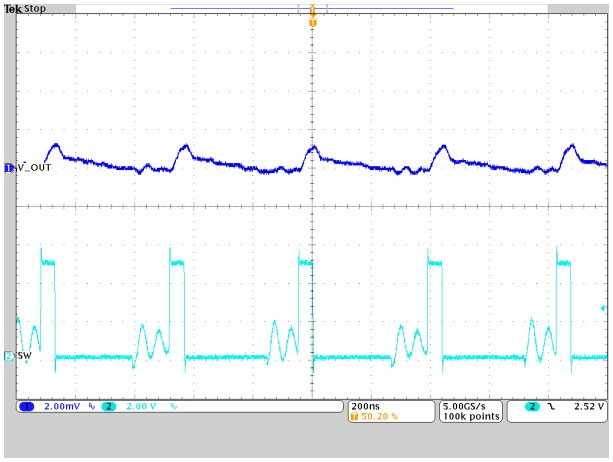
Vout = 0.9V　　Iout = 1A → 9A → 1A

図 9-20. Load Transient Response TPSM8287A12BBM



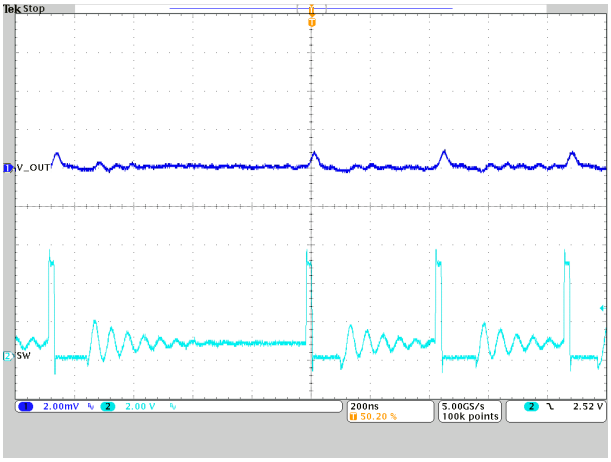
Vout = 0.9V　　I_{OUT} = 2A

図 9-21. PWM-CCM Operation TPSM8287A12BBM



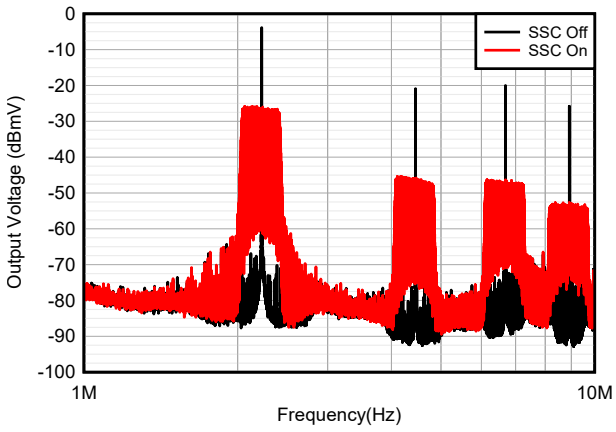
Vout = 0.9V　　I_{OUT} = 1A

図 9-22. PWM-DCM Operation TPSM8287A12BBM



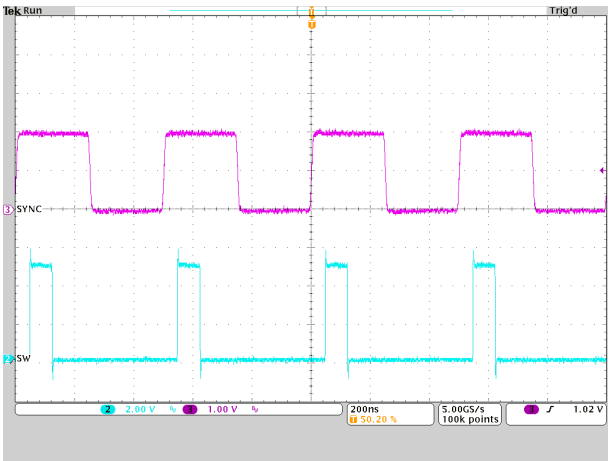
Vout = 0.9V　　I_{OUT} = 100mA

図 9-23. PFM-DCM Operation TPSM8287A12BBM



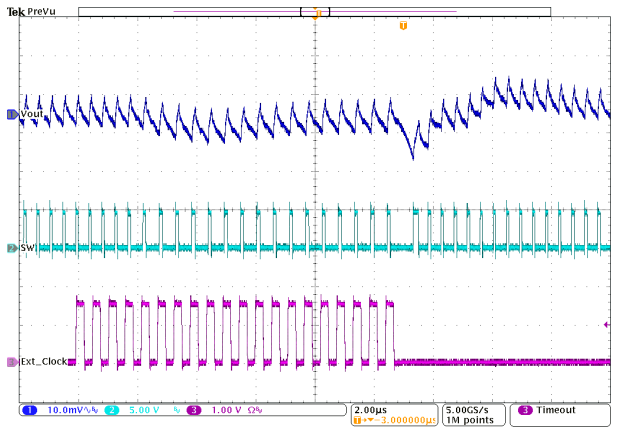
V_{IN} = 3.3V　　V_{OUT} = 0.75V　　I_{OUT} = 6A

図 9-24. Output Noise over Frequency TPSM8287A12BBM



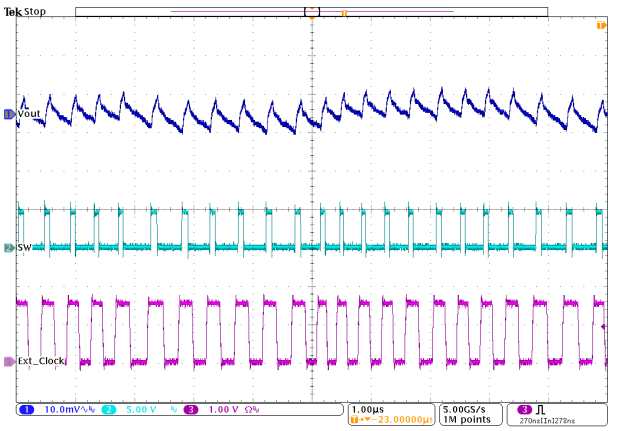
I_{OUT} = 1A　　$f_{(SYNC)}$ = 2MHz

図 9-25. Synchronization to an External Clock



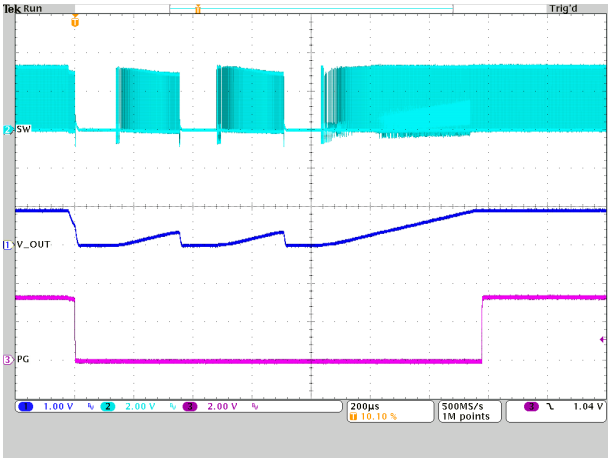
I_{OUT} = 10A V_{OUT} = 0.9V $f_{(SYNC)}$ = 1.8MHz

図 9-26. Adding and Removing an External Clock



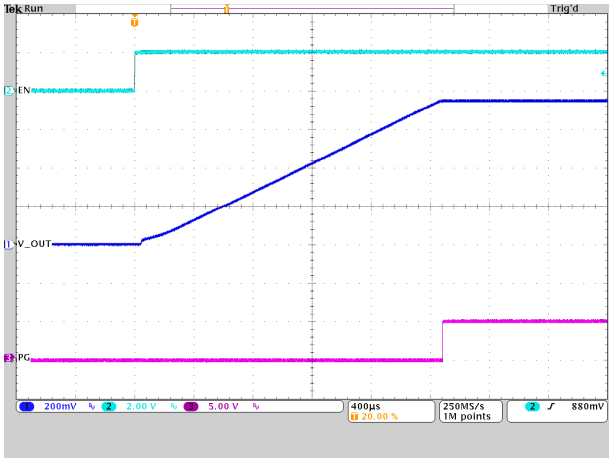
I_{OUT} = 10A V_{OUT} = 0.9V $f_{(SYNC)}$ = 2 to 2.5MHz (random)

図 9-27. Synchronization to a Random External Clock



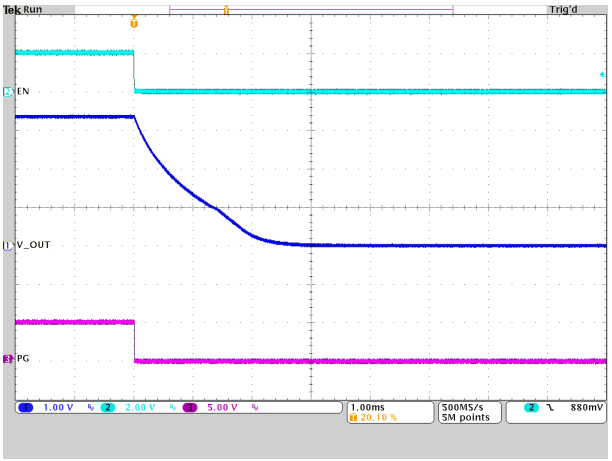
V_{IN} = 3.3V

図 9-28. Current Limit (Hiccup)



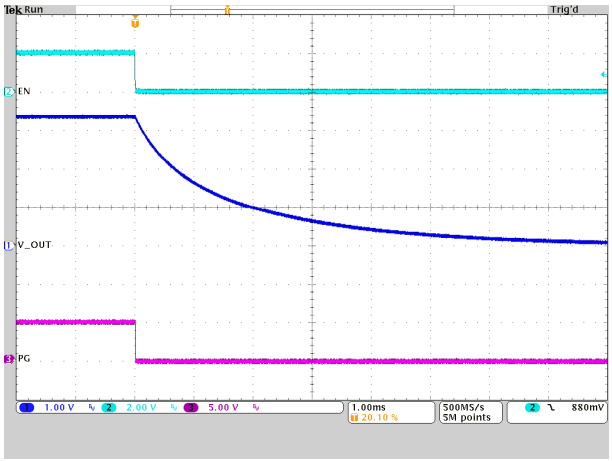
V_{OUT} = 0.75V

図 9-29. Start-Up Using EN Pin



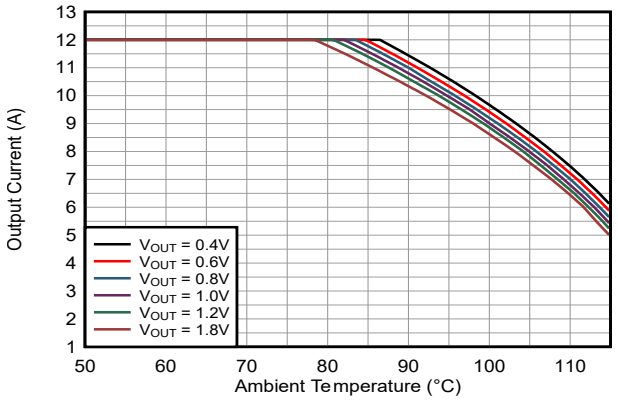
V_{OUT} = 3.3V Load = 7.5Ω

図 9-30. Shutdown Using EN Pin (Discharge Enabled)



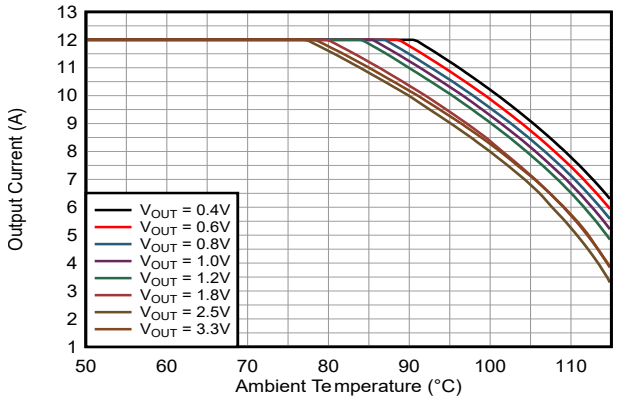
V_{OUT} = 3.3V Load = 7.5Ω

図 9-31. Shutdown Using EN Pin (Discharge Disabled)



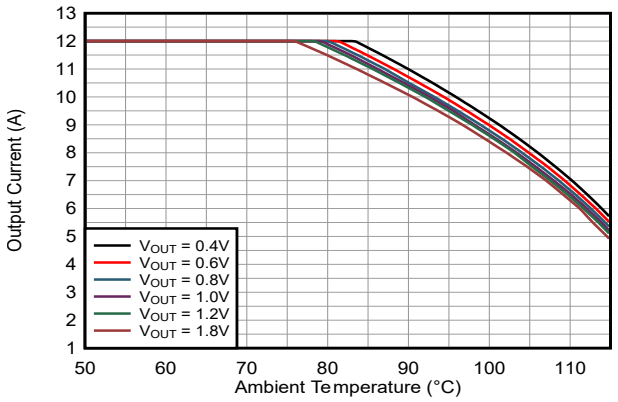
$R_{\Theta JA}$ = 19.5°C/W nat. convection $T_{J,max}$ = 125°C

図 9-32. Safe Operating Area TPSM8287A12BAM V_{IN} = 3.3V



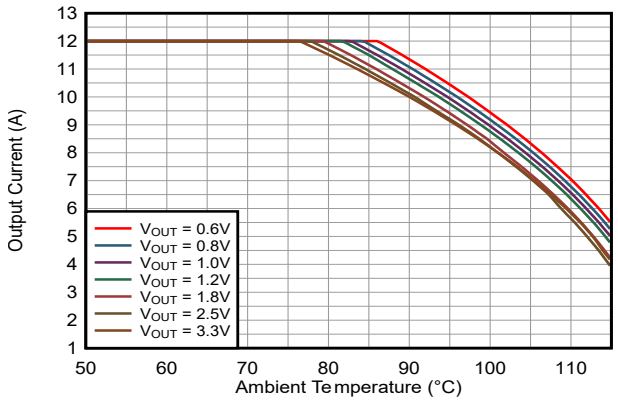
$R_{\Theta JA}$ = 19.5°C/W nat. convection $T_{J,max}$ = 125°C

図 9-33. Safe Operating Area TPSM8287A12BAM V_{IN} = 5.0V



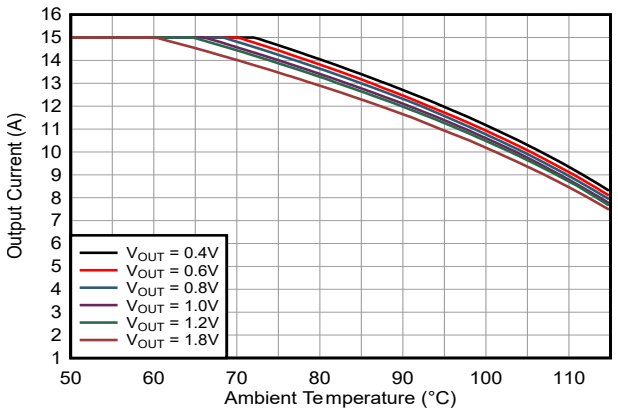
$R_{\Theta JA}$ = 19.5°C/W nat. convection $T_{J,max}$ = 125°C

図 9-34. Safe Operating Area TPSM8287A12BBM V_{IN} = 3.3V



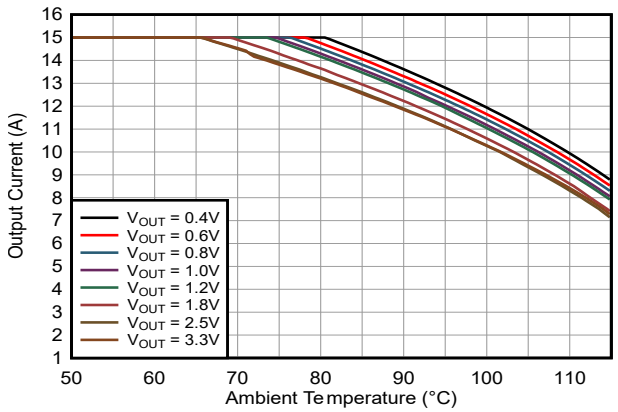
$R_{\Theta JA}$ = 19.5°C/W nat. convection $T_{J,max}$ = 125°C

図 9-35. Safe Operating Area TPSM8287A12BBM V_{IN} = 5.0V



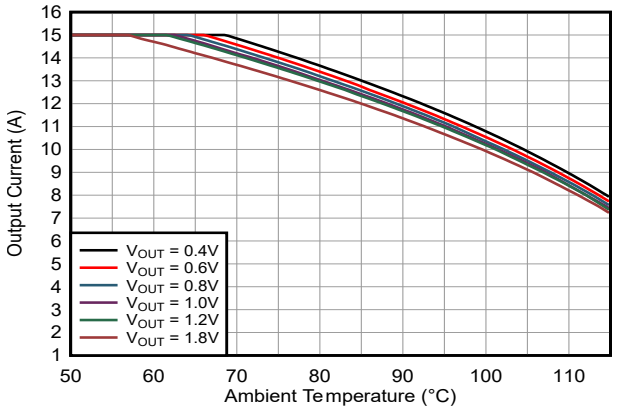
$R_{\Theta JA}$ = 20.0°C/W nat. convection $T_{J,max}$ = 125°C

図 9-36. Safe Operating Area TPSM8287A15BAM V_{IN} = 3.3V



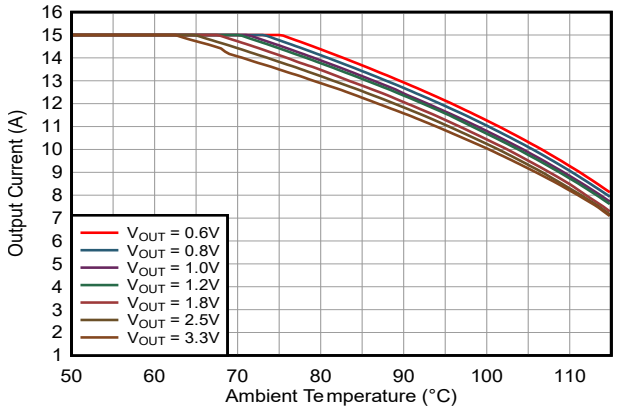
$R_{\Theta JA}$ = 20.0°C/W nat. convection $T_{J,max}$ = 125°C

図 9-37. Safe Operating Area TPSM8287A15BAM V_{IN} = 5.0V



$R_{\Theta JA}$ = 20.0°C/W nat. convection $T_{J,max}$ = 125°C

図 9-38. Safe Operating Area TPSM8287A15BBM V_{IN} = 3.3V



$R_{\Theta JA}$ = 20.0°C/W nat. convection $T_{J,max}$ = 125°C

図 9-39. Safe Operating Area TPSM8287A15BBM V_{IN} = 5.0V

9.3 Typical Application Using Four TPSM8287A1xM in Parallel Operation

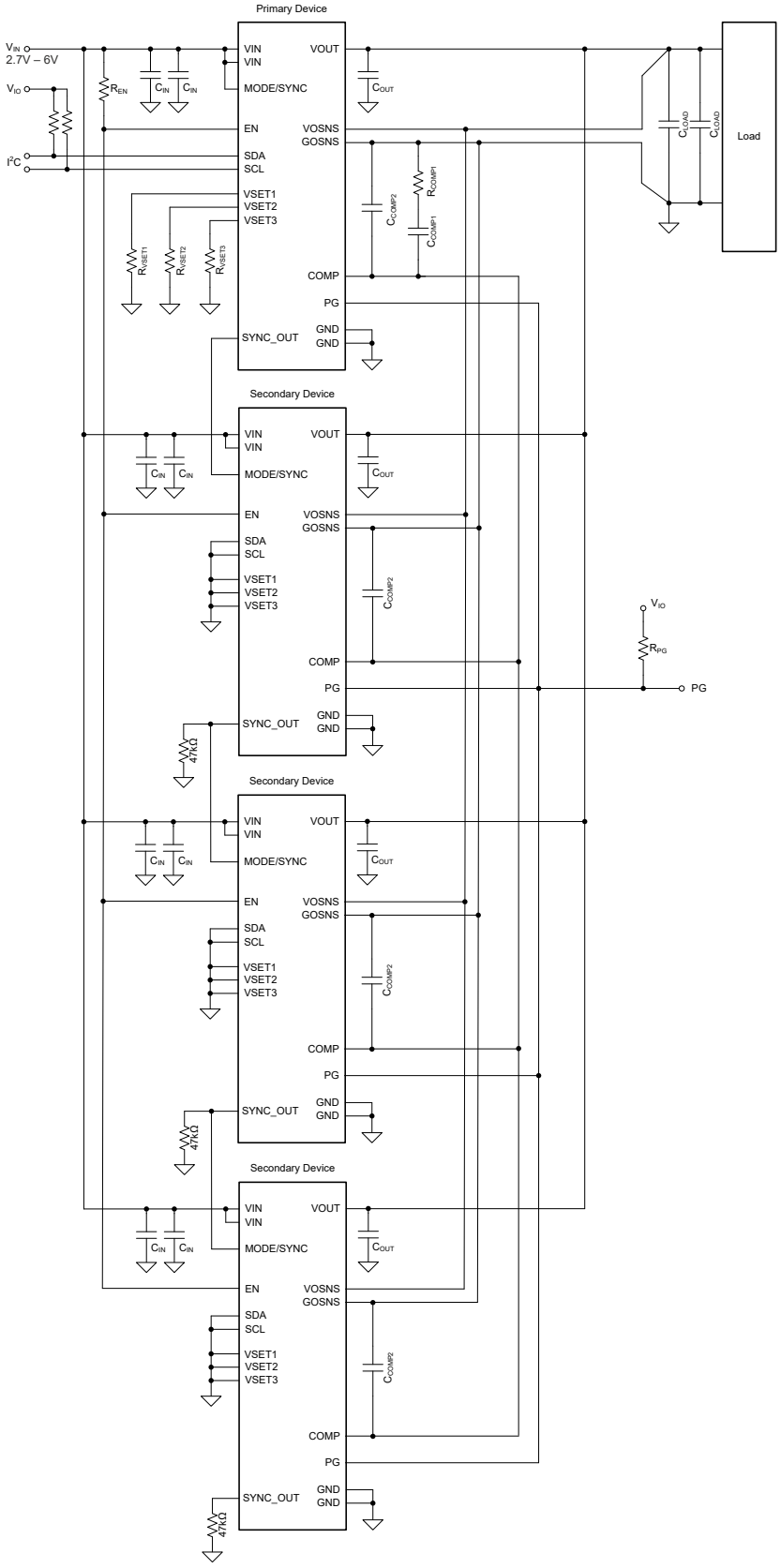


図 9-40. Typical Application Schematic

表 9-3. List of Components

REFERENCE	VALUE	DESCRIPTION	PART NUMBER	MANUFACTURER [1]
C_{Comp1}	1.5nF	Ceramic Capacitor, X7R	Std	Std
C_{Comp2}	10pF	Ceramic Capacitor, C0G/NP0	Std	Std
C_{OUT}	13 × 47µF	Ceramic Capacitor, 6.3V, X6S, size 0805	GRM21BC80J476ME01L	Murata
C_{LOAD}	5 × 220µF	Ceramic Capacitor, 4V, X6S, size 1210	GRM32EC80G227ME05L	Murata
C_{IN}	8 × 22µF	Ceramic Capacitor, 10V, X7R, size 0805	GRM21BZ71A226ME15L	Murata
R_{Comp1}	2000Ω	Resistor 1%, 0.1W	Std	Std
R_{VSET1}, R_{VSET2}, R_{VSET3}	set per 表 7-2	Resistor 5%, 0.1W	Std	Std
R_{EN}	15kΩ	Resistor 5%, 0.1W	Std	Std

9.3.1 Design Requirements

表 9-4 lists the operating parameters for this application example with four TPSM8287A12BAM devices working in parallel to increase the output current.

表 9-4. Design Parameters

SYMBOL	PARAMETER	VALUE
V_{IN}	Input voltage	2.7 – 6.0V
V_{OUT}	Output voltage	0.60V
TOL_{VOUT}	Output voltage tolerance allowed by the application	±3.5%
TOL_{DC}	Output voltage tolerance of the TPSM8287A12BAM (DC accuracy)	±1.0%
$\Delta I_{OUT(step)}$	Output current load step	±30.0A
t_t	Load step transition time	1µs
f_{SW}	Switching frequency	1.5MHz
L	Integrated inductor	100nH
TOL_{IND}	Integrated inductor tolerance	±20%
g_m	Error amplifier transconductance	1.5mS
τ	Emulated current time constant	12.5µs
TOL_τ	Tolerance of the emulated current time constant	±30%
BW_τ	Target loop bandwidth	375kHz
N_Φ	Number of paralleled devices (phases)	4

Preliminary Calculations

The maximum allowable deviation of the power supply is ±3.5%. The DC accuracy of the TPSM8287A1xM is specified as ±1.0%, and therefore the maximum output voltage variation during a transient is given by:

$$\Delta V_{OUT} = \pm V_{OUT} \times (TOL_{VOUT} - TOL_{DC}) \quad (34)$$

$$\Delta V_{OUT} = \pm V_{OUT} \times (3.5\% - 1.0\%) = \pm 15mV \quad (35)$$

式 36 computes the peak-to-peak inductor current ripple, which is the greatest at the maximum input voltage:

$$I_{L(PP)} = \frac{V_{OUT}}{V_{IN(max)}}\left(\frac{V_{IN(max)} - V_{OUT}}{L \times f_{sw} \times N\Phi}\right) \quad (36)$$

$$I_{L(PP)} = \frac{0.6}{6.0}\left(\frac{6.0 - 0.6}{100 \times 10^{-9} \times 1.5 \times 10^{6} \times 4}\right) = 0.9A \quad (37)$$

The maximum load step occurs when the load step from the application occurs at exactly the same time as the peak (or trough) of the inductor ripple current, and is given by:

$$\Delta I_{OUT(max)} = \Delta I_{OUT(step)} + \frac{\Delta I_{L(PP)}}{2} \quad (38)$$

$$\Delta I_{OUT(max)} = 30.0 + \frac{0.9}{2} = 30.5A \quad (39)$$

9.3.2 Detailed Design Procedure

The following subsections describe how to calculate the external components required to meet the specified transient requirements of a given application. The calculations include the worst-case variation of components and use the RMS method to combine the variation of uncorrelated parameters.

9.3.2.1 Selecting the Input Capacitors

The TPSM8287A1xM devices feature a *butterfly* or parallel layout with two pairs of VIN and GND pins on opposite sides of the package.

The duty cycle of the converter is given by:

$$D = \frac{V_{OUT}}{\eta \times V_{IN}} \quad (40)$$

$$D = \frac{0.60}{0.78 \times 2.7} = 0.284 \quad (41)$$

The value of input capacitance needed to meet any system-level input voltage ripple requirement is given by 式 42. For this example, the lowest input voltage and highest load current are used to generate a worst case input voltage ripple of 100mV.

$$C_{IN} = \frac{D \times (1 - D) \times I_{OUT}}{V_{IN(PP)} \times f_{sw}} \quad (42)$$

$$C_{IN} = \frac{0.284 \times (1 - 0.284) \times 12.0}{0.1 \times 1.5 \times 10^{6}} = 16.3\mu F \quad (43)$$

The value of C_{IN} calculated with 式 42 is the *effective* capacitance after all derating, tolerance, and aging effects have been considered. In this parallel configuration, make sure to distribute the calculated input capacitance equally across all phases.

9.3.2.2 Selecting the Target Loop Bandwidth

The control loop bandwidth measures how quickly the device responds to a change in output voltage. With the TPSM8287A1xM external compensation, the loop bandwidth is adjustable to balance the tradeoff of a fast response versus stability and ringing. The R_{Comp1} resistor and output capacitance are the primary means of adjusting the loop bandwidth.

TI recommends setting the target loop bandwidth to 200kHz for a simple design. If strong load transients are expected in the application, the target bandwidth can be set as high as ¼ of the switching frequency. A target bandwidth of 375kHz is used for this example design.

9.3.2.3 Selecting the Compensation Resistor

Use 式 44 to calculate the recommended value of compensation resistor, R_{Comp1}:

$$R_{Comp1} = \frac{1}{g_m}\left(\frac{\pi \times \Delta I_{OUT(step)} \times L}{4 \times \tau \times \Delta V_{OUT} \times N\phi} - 1\right)\left(1 + \sqrt{TOL_{IND}{}^2 + TOL_{\tau}{}^2}\right) \quad (44)$$

$$R_{Comp1} = \frac{1}{1.5 \times 10^{-3}}\left(\frac{\pi \times 30.0 \times 100 \times 10^{-9}}{4 \times 12.5 \times 10^{-6} \times 15 \times 10^{-3} \times 4} - 1\right)\left(1 + \sqrt{20\%^2 + 30\%^2}\right) = 1943\Omega \quad (45)$$

Picking a standard component above the calculated value, a 2000Ohm resistor is chosen in this example. The selected value must be used for the further calculations.

9.3.2.4 Selecting the Output Capacitors

If the converter remains in regulation, the minimum required output capacitance is given by:

$$C_{OUT(min)(reg)} = \left(\frac{\tau \times \left(1 + g_m \times R_{Comp1}\right)}{2 \times \pi \times \frac{L}{N\phi} \times BW_{\tau}}\right)\left(1 + \sqrt{TOL_{\tau}{}^2 + TOL_{IND}{}^2 + TOL_{fSW}{}^2}\right) \quad (46)$$

$$C_{OUT(min)(reg)} = \left(\frac{12.5 \times 10^{-6} \times \left(1 + 1.5 \times 10^{-3} \times 2000\right)}{2 \times \pi \times \frac{100 \times 10^{-9}}{4} \times 400 \times 10^{3}}\right)\left(1 + \sqrt{30\%^2 + 20\%^2 + 10\%^2}\right) = 1166\mu F \quad (47)$$

If the converter loop saturates, the minimum output capacitance is given by:

$$C_{OUT(min)(sat)} = \frac{1}{\Delta V_{OUT}}\left(\frac{L \times \Delta I_{OUT(max)}{}^2}{2 \times V_{OUT} \times N\phi} - \frac{\Delta I_{OUT(step)} \times t_t}{2}\right)(1 + TOL_{IND}) \quad (48)$$

$$C_{OUT(min)(sat)} = \frac{1}{15 \times 10^{-3}}\left(\frac{100 \times 10^{-9} \times 30.5^2}{2 \times 0.6 \times 4} - \frac{30.0 \times 1 \times 10^{-6}}{2}\right)(1 + 20\%) = 345\mu F \quad (49)$$

In this case, choose $C_{OUT(min)}$ = 1166µF as the larger of the two values for the output capacitance.

表 9-3 lists the output capacitors chosen. 2 × 47µF capacitors are placed close to each of the four modules, giving a minimum effective capacitance of about 27µF each. Five 220µF capacitors and five 47µF are placed near the load to approximate the total decoupling capacitance required by a typical load. Each of the 220µF capacitors yield about 138µF of effective capacitance. Together, the 1041µF of effective capacitance is very close to the required minimum value calculated above. For further calculations, use C_{OUT} = 1041µF.

式 50 checks that most of the output capacitance is placed at the load. If the ratio is less than 1, increase the capacitance at the load or place the device, output capacitance, and load next to each other such that there is no separation between the output capacitances.

$$\frac{C_{LOAD}}{2 \times C_{OUT}} > 1 \quad (50)$$

$$\frac{5 \times 27 \times 10^{-6} + 5 \times 138 \times 10^{-6}}{2 \times \left(4 \times 2 \times 27 \times 10^{-6}\right)} > 1 = \text{True} \quad (51)$$

式 52 calculates the output voltage ripple, based on the effective output capacitance value.

$$V_{OUT}(p-p) = \frac{I_{L(PP)}}{8 \times C_{OUT} \times f_{sw}} \quad (52)$$

$$V_{OUT(p-p)} = \frac{0.9}{8 \times 1041 \times 10^{-6} \times 1.5 \times 10^{6}} = 0.072 \quad mV \tag{53}$$

The ripple is slightly higher in the application due to the ESR and ESL in the output capacitors and the application board parasitics.

9.3.2.5 Selecting the Compensation Capacitor, C_{Comp1}

First, use 式 54 to calculate the bandwidth of the inner loop:

$$BW_{INNER} = \frac{\tau}{2\pi \times \frac{L}{N\Phi} \times C_{OUT}} \tag{54}$$

$$BW_{INNER} = \frac{12.5 \times 10^{-6}}{2\pi \times \frac{100 \times 10^{-9}}{4} \times 1041 \times 10^{-6}} = 76.4\text{kHz} \tag{55}$$

Next, calculate the product of $g_m R_{Comp1}$:

$$g_m \times R_{Comp1} = 1.5 \times 10^{-3} \times 2000 = 3.0 \tag{56}$$

If $g_m R_{Comp1}$ > than 1, use 式 57 to calculate the recommended value of C_{Comp1}, which sets a zero in the control loop. If $g_m R_{Comp1}$ < 1, use 式 59 to calculate the recommended value of C_{Comp1}.

$$C_{Comp1} = \frac{2}{\pi \times BW_{INNER} \times g_m \times {R_{Comp1}}^2} \tag{57}$$

$$C_{Comp1} = \frac{2}{\pi \times 76.4 \times 10^{3} \times 1.5 \times 10^{-3} \times (2000)^2} = 1.39\text{nF} \tag{58}$$

The closest standard value is 1.5nF.

$$C_{Comp1} = \frac{2 \times g_m}{\pi \times BW_{INNER}} \tag{59}$$

式 60 approximates the loop bandwidth.

$$BW = BW_{INNER} \times 2 \times \left(1 + R_{Comp1} \times g_m\right) \tag{60}$$

$$BW = 76.4 \times 10^{3} \times 2 \times \left(1 + 2000 \times 1.5 \times 10^{-3}\right) = 612kHz \tag{61}$$

9.3.2.6 Selecting the Compensation Capacitor, C_{Comp2}

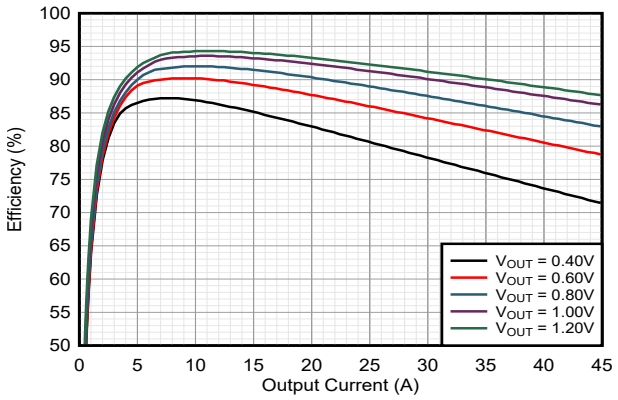
The compensation capacitor, C_{Comp2}, is an optional capacitor that TI recommends the user include to bypass high-frequency noise away from the COMP pin. The value of this capacitor is not critical; 10pF or 22pF capacitors are designed for typical applications.

This capacitor can be made larger to suppress high-frequency zeros or resonances that occur in the system output voltage routing and decoupling network. 式 62 calculates the pole created by C_{Comp2}.

$$f_{pole} = \frac{1}{2 \times \pi \times R_{Comp1} \times C_{Comp2}} \tag{62}$$

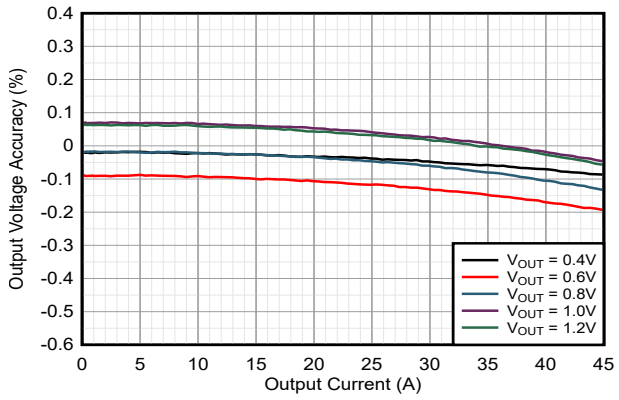
9.3.3 Application Curves

V_{IN} = 5.0V, V_{OUT} = 0.6V, T_A = 25°C, BOM = 表 9-3, 4 × TPSM8287A12BAM in parallel operation, unless otherwise noted.



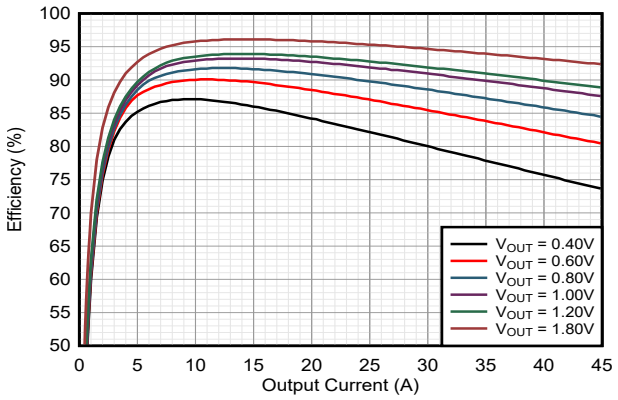
V_{IN} = 2.7V F_{SW} = 1.5MHz FPWM

図 9-41. Efficiency



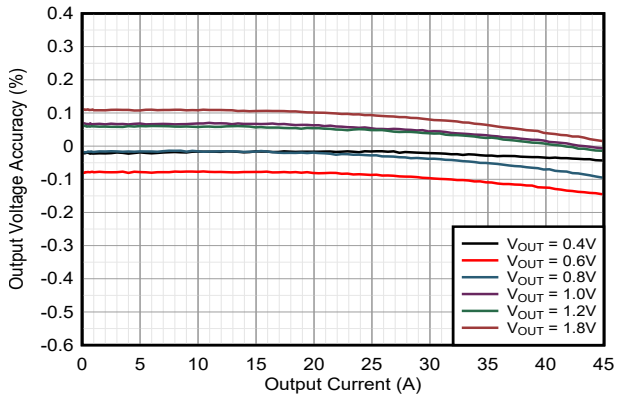
V_{IN} = 2.7V F_{SW} = 1.5MHz FPWM

図 9-42. Load Regulation



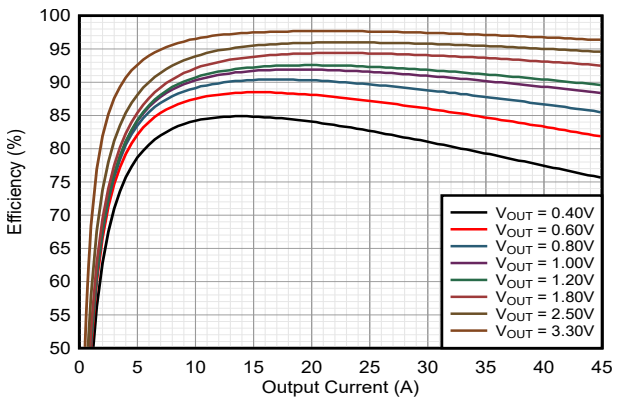
V_{IN} = 3.3V F_{SW} = 1.5MHz FPWM

図 9-43. Efficiency



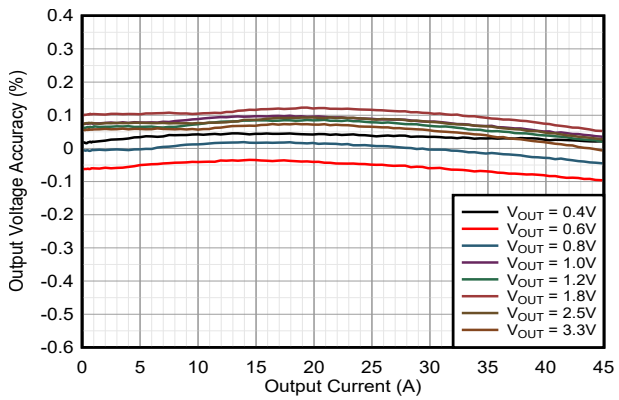
V_{IN} = 3.3V F_{SW} = 1.5MHz FPWM

図 9-44. Load Regulation



V_{IN} = 5.0V F_{SW} = 1.5MHz FPWM

図 9-45. Efficiency



V_{IN} = 5.0V F_{SW} = 1.5MHz FPWM

図 9-46. Load Regulation

9.4 Power Supply Recommendations

The TPSM8287A1xM family has no special requirements for the input power supply. The output current rating of the input power supply must be rated according to the supply voltage and current requirements of the TPSM8287A1xM. For proper operation, the input voltage must be at least 1.4V above the selected output voltage.

9.5 Layout

9.5.1 Layout Guidelines

A proper layout is critical for the operation of any switched mode power supply, especially at high switching frequencies. Therefore, the PCB layout of the TPSM8287A1xM demands careful attention to make sure of best performance. A poor layout can lead to issues like the following:

- Bad line and load regulation
- Instability
- Increased EMI radiation
- Noise sensitivity

Refer to the *Five Steps to a Great PCB Layout for a Step-Down Converter* analog design journal for a detailed discussion of general best practices. The following are specific recommendations for the TPSM8287A1xM:

- Place the input capacitors as close as possible to the VIN and GND pins of the device. This placement is the most critical component placement. Route the input capacitors directly to the VIN and GND pins avoiding vias.
- Place the output capacitors close to the VOUT and GND pins and route them directly avoiding vias.
- Place the IC close to the load to minimize the power loss from voltage drop on the output and to minimize parasitic inductance between the output capacitors at the TPSM8287A1xM and those at the load.
- Use GND vias under the three exposed thermal pads to improve thermal performance. Directly connect the GND pins to the exposed thermal pad with copper on the top PCB layer.
- Route the VOSNS and GOSNS remote sense lines as a differential pair and connect them to the lowest impedance point at the load. Do not route the VOSNS and GOSNS traces close to any switch nodes, the input capacitors, clock signals, or other aggressor signals.
- Connect the compensation components between COMP and GOSNS. Do not connect the compensation components directly to power ground.
- Place the VSETx resistors (and SYNC_OUT resistor in the secondary devices) close to the TPSM8287A1xM to minimize parasitic capacitance.
- Route VOSNS, GOSNS, and COMP directly to keep them short and avoid noisy aggressor signals in the stacked configuration.
- Refer to 図 9-47 for an example of component placement, routing, and thermal design.
- See the recommended land pattern for the TPSM8287A1xM at the end of this data sheet. For best manufacturing results, create the pads as solder mask defined (SMD) when some pins (such as VIN, VOUT, and GND) are connected to large copper planes. Using SMD pads keeps each pad the same size and avoids solder pulling the device during reflow.

9.5.2 Layout Example

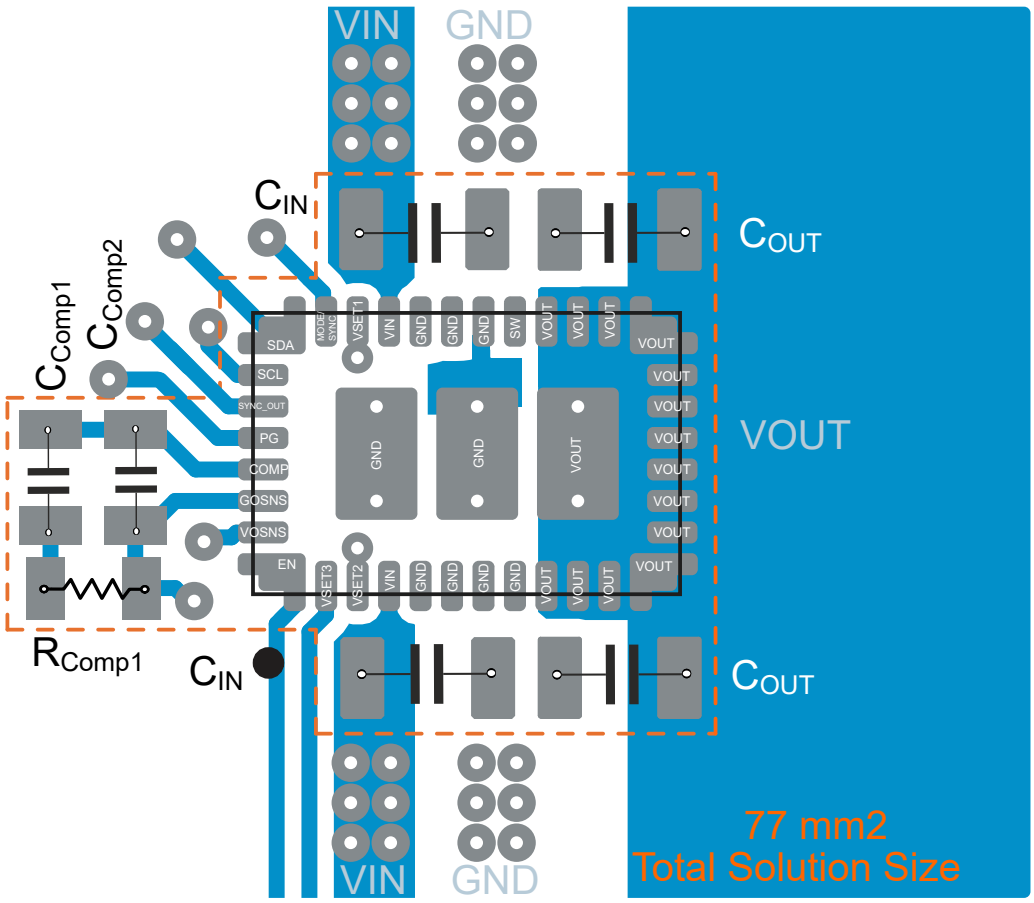


図 9-47. Layout Example

10 Device and Documentation Support

10.1 Device Support

10.1.1 サード・パーティ製品に関する免責事項

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10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Achieving a clean startup by using a DC/DC converter with a precise enable-pin threshold* analog design journal
- Texas Instruments, *Five Steps to a Great PCB Layout for a Step-Down Converter* analog design journal

10.3 ドキュメントの更新通知を受け取る方法

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10.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

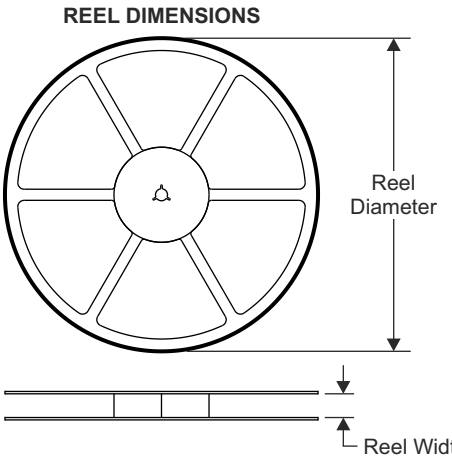
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

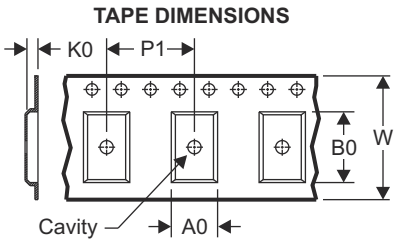
DATE	REVISION	NOTES
August 2024	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

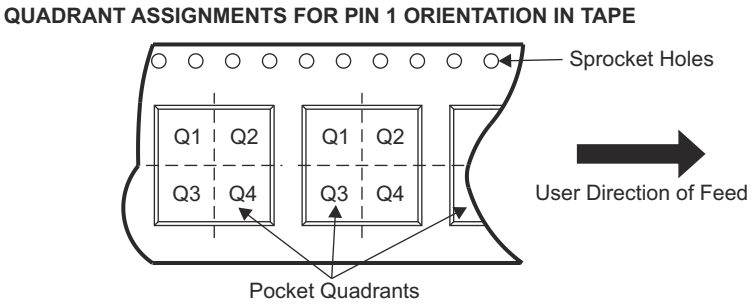
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Tape and Reel Information



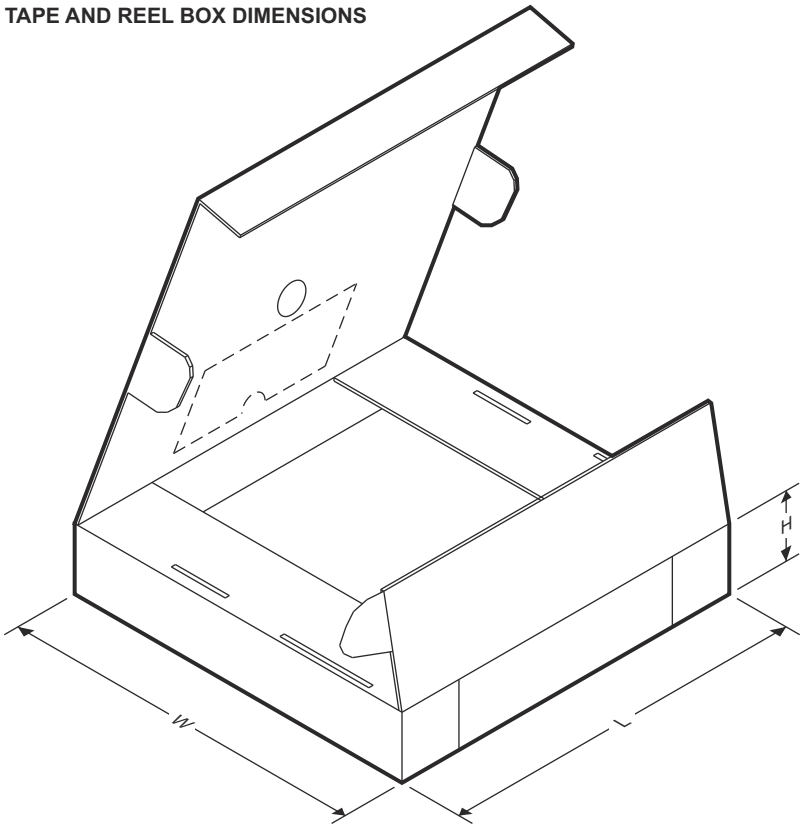


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM8287A12BAMRDVT	B0QFN	RDV	39	250	330	16.4	4.80	7.10	2.05	8.0	16.0	Q1
TPSM8287A12BBMRDVT	B0QFN	RDV	39	250	330	16.4	4.80	7.10	2.05	8.0	16.0	Q1
TPSM8287A15BAMRDWT	B3QFN	RDW	39	250	330	16.4	4.90	7.20	4.30	8.0	16.0	Q1
TPSM8287A15BBMRDWT	B3QFN	RDW	39	250	330	16.4	4.90	7.20	4.30	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM8287A12BAMRDVT	B0QFN	RDV	39	250	336.0	336.0	48.0
TPSM8287A12BBMRDVT	B0QFN	RDV	39	250	336.0	336.0	48.0
TPSM8287A15BAMRDWT	B0QFN	RDV	39	250	336.0	336.0	48.0
TPSM8287A15BBMRDWT	B0QFN	RDV	39	250	336.0	336.0	48.0

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPSM8287A12BAMRDVT	ACTIVE				250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	TM87A12BAM	Samples
TPSM8287A12BBMRDVT	ACTIVE				250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	TM87A12BBM	Samples
TPSM8287A15BAMRDWT	ACTIVE				250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	TM87A15BAM	Samples
TPSM8287A15BBMRDWT	ACTIVE				250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	TM87A15BBM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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