TEXAS INSTRUMENTS
TPSM83100, TPSM83101
JAJSOX4A – MARCH 2023 – REVISED JUNE 2023

TPSM83100 および TPSM83101 インダクタ内蔵の 1.5A 出力電流、昇降圧 MicroSiP™ 電源モジュール

1 特長

- 入力電圧範囲:1.6V～5.5V
  - スタートアップ時のデバイス入力電圧 > 1.65V
- 出力電圧範囲:1.2V～5.5V
  - PFM モードでは 1.0V の V_{out} をサポート
- 高い出力電流能力、3A ピーク・スイッチ電流
  - V_{IN} ≧ 3V、V_{OUT} = 3.3V 時の I_{out} は 1.5A
  - V_{IN} ≧ 2.7V、V_{OUT} = 3.3V 時の I_{out} は 1.2A
- アクティブな出力放電 (TPSM83101 のみ)
- 全負荷範囲にわたって高効率を実現
  - 静止電流 8µA (標準値)
  - 自動パワー・セーブ・モードおよび強制 PWM モード
- ピーク電流昇降圧モード・アーキテクチャ
  - シームレスなモード遷移
  - 順方向および逆方向電流動作
  - あらかじめ出力にバイアスを印加した状態で起動
  - 2MHz スイッチングの固定周波数動作
- 安全で堅牢な動作を実現する機能
  - 過電流イベントおよび短絡保護
  - アクティブ・ランプを採用したソフト・スタート機能内蔵
  - 過熱保護および過電圧保護
  - 負荷切断による真のシャットダウン機能
  - 順方向および逆方向の電流制限
- 小型ソリューション・サイズ
  - MicroSiP™ 電源モジュール、インダクタ内蔵
  - 2.0mm × 2.6mm × 1.2mm (最大値) の 8 ピン µSiP パッケージ

2 アプリケーション

- 電圧スタビライザ (データコム、光モジュール、冷却 / 加熱)
- システム・プリレギュレータ (スマートフォン、タブレット、端末、テレマティクス)
- ポイント・オブ・ロード・レギュレーション (有線センサ、ポート / ケーブル・アダプタ、ドングル)
- 指紋、カメラ・センサ (電子スマート・ロック、IP ネットワーク・カメラ)

3 概要

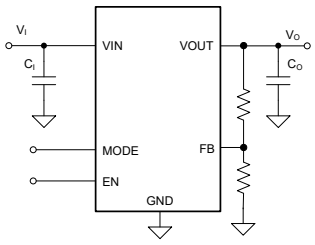
TPSM83100 および TPSM83101 は、固定周波数のピーク電流モード制御昇降圧 MicroSiP™ 電源モジュールで、小型ソリューション・サイズや高効率を求められる場合に最適です。この電源モジュールにはインダクタが組み込まれているため、設計を簡素化し、外付け部品を減らして、PCB 面積を削減できます。ピーク電流制限 (標準値) は 3A で、入力電圧範囲は 1.6V～5.5V です。TPSM83100 および TPSM83101 は、システム・プリレギュレータおよび電圧スタビライザ用の電源ソリューションを提供します。

TPSM83100 および TPSM83101 は、入力電圧に応じて自動的に昇圧モード、降圧モードに切替わり、入力電圧が出力電圧とほぼ等しい場合は 3 サイクル昇降圧モードで動作します。モード間の遷移は定義されたデューティ・サイクルで発生し、モード間の不要な切り替えが避けられるので出力電圧リップルを減らすことができます。8µA の静止電流とパワー・セーブ・モードにより、軽負荷から無負荷までの状況で最高の効率を実現します。

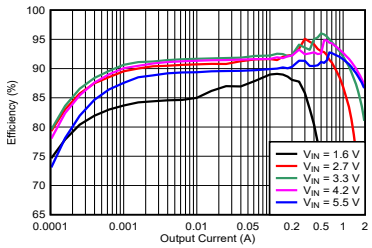
パッケージ情報

部品番号	パッケージ(1)	本体サイズ (公称)
TPSM83100	µSiP (8)	2.0mm × 2.6mm
TPSM83101(2)		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。
(2) 製品プレビュー詳細はテキサス・インスツルメンツまでお問い合わせください。



代表的なアプリケーション



効率と出力電流との関係 (V_{OUT} = 3.3V)

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (March 2023) to Revision A (June 2023)	Page
• ドキュメントのステータスを「事前情報」から「量産データ」に変更	1
• 初版リリース	1

5 Device Comparison Table

PART NUMBER	Output Discharge
TPSM83100	No
TPSM83101(1)	Yes

(1) Product Preview. Contact TI factory for more information.

6 Pin Configuration and Functions

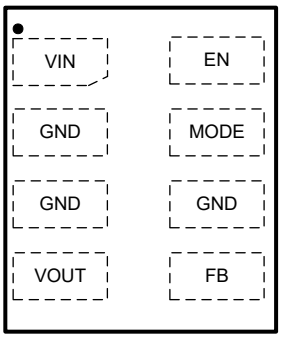


図 6-1. 8-Pin µSiP package (Top View)

表 6-1. Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
VIN	1	PWR	Supply input voltage
GND	2	PWR	Power ground
GND	3	PWR	Power ground
VOUT	4	PWR	Power stage output
FB	5	I	Voltage feedback. Sensing pin
GND	6	PWR	Power ground
MODE	7	I	PFM/PWM selection. Set low for power save mode, set high for forced PWM. It must not be left floating.
EN	8	I	Device enable. Set high to enable and low to disable. It must not be left floating.

(1) PWR = power, I = input

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_I	Input voltage (VIN, VOUT, EN, FB, MODE)(2)	–0.3	6.0	V
V_I	Input voltage for less than 10 ns	–0.3	7.0	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal, unless otherwise noted.

7.2 ESD Rating

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JS-002(2)	± 500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating junction temperature (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_I	Supply voltage		1.6		5.5	V
V_O	Output voltage		1.2		5.5	V
C_I	Input effective capacitance	V_I = 1.6 V to 5.5 V	4.2			µF
C_O	Output effective capacitance	1.2 V ≤ V_O ≤ 3.6 V, nominal value at V_O = 3.3 V	10.4	16.9	330	µF
		3.6 V < V_O ≤ 5.5 V, nominal value at V_O = 5 V	7.95	10.6	330	µF
T_J	Operating junction temperature range		–40		125	°C

7.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC		TPSM83100 TPSM83101 µSiP-8 PINS Standard	TPSM83100 TPSM83101 µSiP-8 PINS EVM	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	100	48.9	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	42.2	N/A	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	33.2	N/A	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	N/A	N/A	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	32.2	24.5	°C/W

7.5 Electrical Characteristics

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted). Typical values are at V_I = 3.8 V , V_O = 3.3 V and T_J = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY								
I_{SD}	Shutdown current into VIN		V_I = 3.8 V, $V_{(EN)}$ = 0 V	T_J = 25°C		0.5	0.9	µA
I_Q	Quiescent current into VIN		V_I = 2.2 V, V_O = 3.3 V, $V_{(EN)}$ = 2.2 V, no switching			0.15	6.1	µA
I_Q	Quiescent current into VOUT		V_I = 2.2 V, V_O = 3.3 V, $V_{(EN)}$ = 2.2 V, no switching			8		µA
V_{IT+}	Positive-going UVLO threshold voltage				1.5	1.55	1.599	V
V_{IT-}	Negative-going UVLO threshold voltage		During start-up		1.4	1.45	1.499	V
V_{hys}	UVLO threshold voltage hysteresis				99			mV
$V_{I(POR)T+}$	Positive-going POR threshold voltage		maximum of V_I or V_O		1.25	1.45	1.65	V
$V_{I(POR)T-}$	Negative-going POR threshold voltage				1.22	1.43	1.6	V
I/O SIGNALS								
V_{T+}	Positive-going threshold voltage	EN, MODE			0.77	0.98	1.2	V
V_{T-}	Negative-going threshold voltage	EN, MODE			0.5	0.66	0.76	V
V_{hys}	Hysteresis voltage	EN, MODE				300		mV
I_{IH}	High-level input current	EN, MODE	$V_{(EN)}$ = $V_{(MODE)}$ = 1.5 V, no pullup resistor			±0.01	±0.25	µA
I_{IL}	Low-level input current	EN, MODE	$V_{(EN)}$ = $V_{(MODE)}$ = 0 V,			±0.01	±0.1	µA
	Input bias current	EN, MODE	$V_{(EN)}$ = 5.5 V			±0.01	±0.3	µA
POWER SWITCH								
$r_{DS(on)}$	On-state resistance	Q1	V_I = 3.8 V, V_O = 3.3 V, test current = 0.2 A			45		mΩ
		Q2				50		mΩ
		Q3				50		mΩ
		Q4				85		mΩ
CURRENT LIMIT								
$I_{L(PEAK)}$	Switch peak current limit (1)	Q1	V_O = 3.3 V	Output sourcing current	2.6	3	3.35	A
				Output sinking current, V_I = 3.3 V	–0.7	–0.55	–0.45	A
	PFM mode entry threshold (peak) current (1)		I_O falling			145		mA
OUTPUT								
I_{DIS}	TPSM83101 output discharge current		EN = LOW, V_I = 2.2V V_O = 3.3V			–67		mA
V_{FB}	Reference voltage on feedback pin				495	500	505	mV
PROTECTION FEATURES								
$V_{T+(OVP)}$	Positive-going OVP threshold voltage				5.55	5.75	5.95	V
$V_{T+(IVP)}$	Positive-going IVP threshold voltage				5.55	5.75	5.95	V
T_{JT+}	Thermal shutdown threshold temperature		T_J rising			160		°C
	Thermal shutdown hysteresis					25		°C
TIMING PARAMETERS								
$t_{d(EN)}$	Delay between a rising edge on the EN pin and the start of the output voltage ramp					0.87	1.5	ms
$t_{d(ramp)}$	Soft-start ramp time				6.42	7.55	8.68	ms
f_{SW}	Switching frequency				1.8	2	2.2	MHz

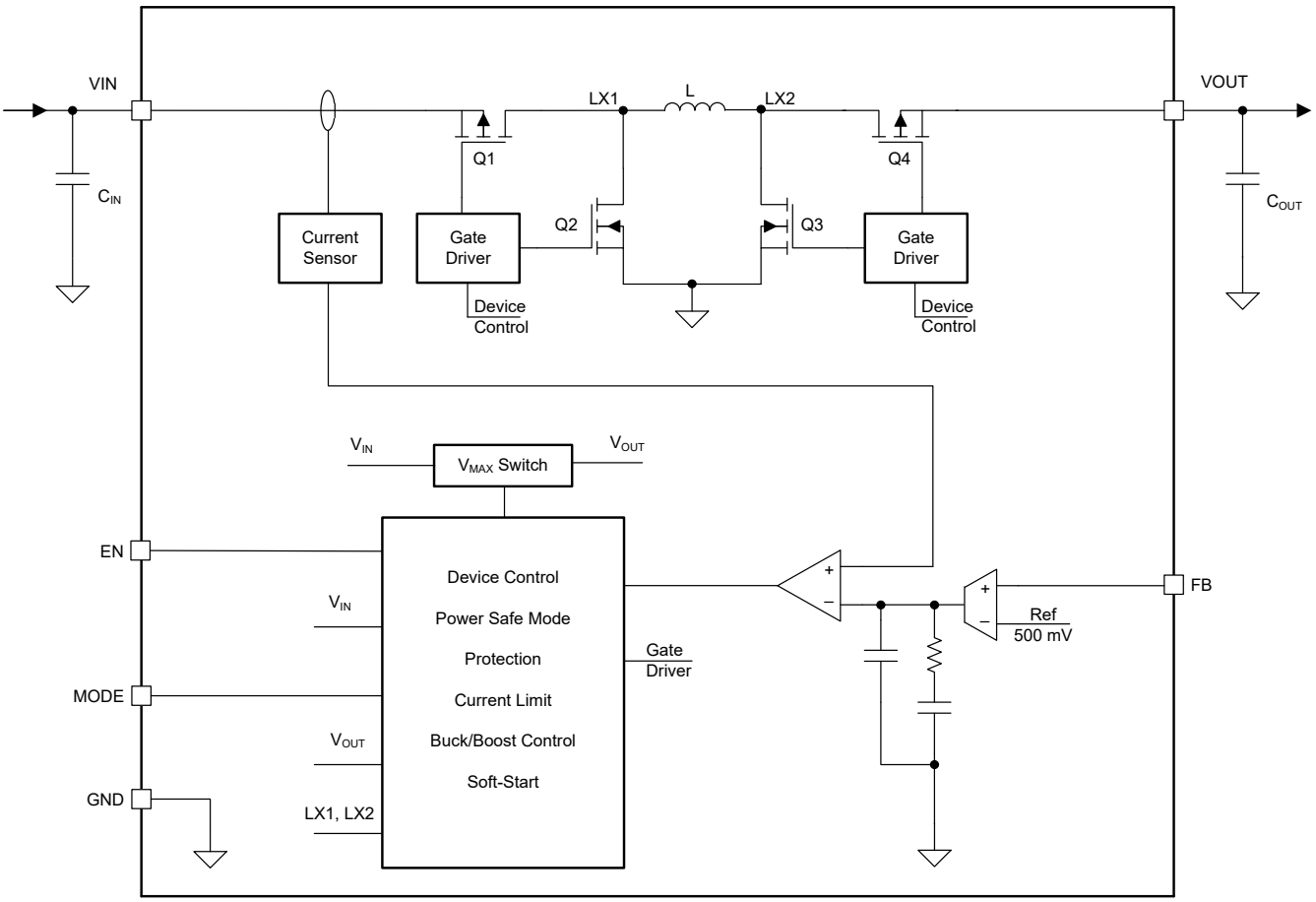
(1) Current limit production test are performed under DC conditions. The current limit in operation is somewhat higher and depends on propagation delay and the applied external components

8 Detailed Description

8.1 Overview

The TPSM83100 and TPSM83101 are constant frequency peak current mode control buck-boost MicroSiP™ power modules. The modules use a fixed-frequency topology with approximately 2-MHz switching frequency. The modulation scheme has three clearly defined operation modes where the modules enter with defined thresholds over the full operation range of V_{IN} and V_{OUT}. The maximum output current is determined by the Q1 peak current limit which is typically 3 A and by the thermal limitation.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Undervoltage Lockout (UVLO)

The input voltage of the VIN pin is continuously monitored if the device is not in shutdown mode. UVLO only stops or starts the module operation. The UVLO does not impact the core logic of the device. UVLO avoids a brownout of the device during device operation. In case the supply voltage on the VIN pin is lower than the negative-going threshold of UVLO, the module stops its operation. To avoid a false disturbance of the power conversion, the UVLO falling threshold logic signal is digitally de-glitched.

If the supply voltage on the VIN pin recovers to be higher than the UVLO rising threshold, the module returns to operation. In this case, the soft-start procedure restarts faster than under start-up without a pre-biased output.

8.3.2 Enable and Soft Start

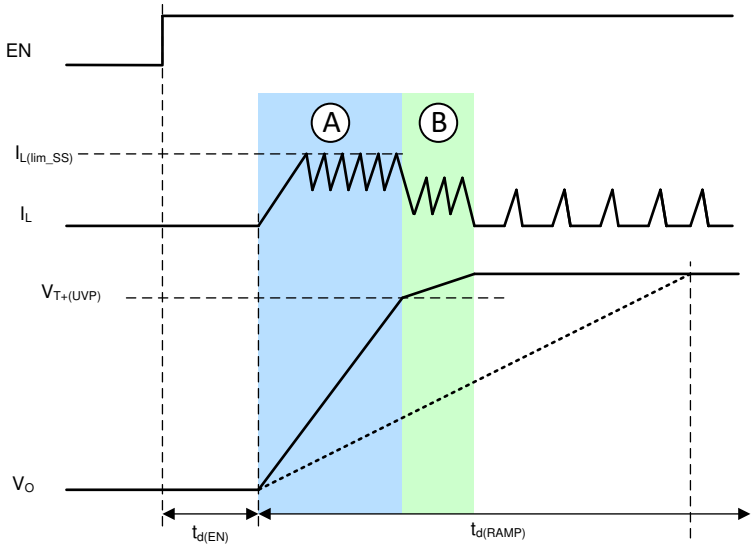


図 8-1. Typical Soft-Start Behavior

When the input voltage is above the UVLO rising threshold and the EN pin is pulled to a voltage above 1.2 V, the TPSM83100 and TPSM83101 are enabled and start up after a short delay time, $t_{d(EN)}$.

The TPSM83100 and TPSM83101 have an inductor peak current clamp to limit inrush current during start-up. When the minimum current clamp ($I_{L(lim\_SS)}$) is lower than the current that is necessary to follow the voltage ramp, the current automatically increases to follow the voltage ramp. The minimum current limit ensures as fast as possible soft start if the capacitance is chosen lower than what the ramp time $t_{d(RAMP)}$ was selected for.

In a typical start-up case as shown in 図 8-1 (low output load, typical output capacitance), the minimum current clamp limits the inrush current and charges the output capacitor. The output voltage then rises faster than the reference voltage ramp (see phase A in 図 8-1). To avoid an output overshoot, the current clamp is deactivated when the output is close to the target voltage and follows the reference voltage ramp slew value given by the voltage ramp, which is finishing the start up (see phase B in 図 8-1). The transition from the minimum current clamp operation is sensed by using the threshold $V_{T+(UVP)}$. After phase B, the output voltage is well regulated to the nominal target voltage. The current waveform depends on the output load and operation mode.

8.3.3 Adjustable Output Voltage

The output voltage is set by an external resistor divider. The resistor divider must be connected between VOUT, FB, and GND. The feedback voltage is given by V_{FB}. The recommended low-side resistor R2 (between FB and GND) is below 100 kΩ. The high-side resistor R1 (between FB and VOUT) is calculated by 式 1.

$$R1 = R2 \times (V_{OUT} / V_{FB} - 1) \quad (1)$$

The typical V_{FB} voltage is 0.5 V.

8.3.4 Mode Selection (PFM/FPWM)

The mode pin is a digital input to enable PFM/FPWM.

When the MODE pin is connected to logic low, the device works in auto PFM mode. The device features a power save mode to maintain the highest efficiency over the full operating output current range. PFM automatically changes the converter operation from CCM to pulse frequency modulation.

When the MODE pin is connected to logic high, the device works in forced PWM mode, regardless of the output current, to achieve minimum output ripple.

8.3.5 Output Discharge

TPSM83101 provides an active pull down current(67mA typ) to quickly discharge output when the EN is logic low. With this function, the VOUT is connected to ground through internal circuitry, preventing the output from “floating” or entering into an undetermined state. The output discharge function makes the power on and off sequencing smooth. Pay attention to the output discharge function if use this device in applications such as power multiplexing, because the output discharge circuitry creates a constant current path between the multiplexer output and the ground.

8.3.6 Reverse Current Operation

The device can support reverse current operation (the current flows from VOUT pin to VIN pin) in FPWM mode. If the output feedback voltage on the FB pin is higher than the reference voltage, the module regulation forces a current into the input capacitor. The reverse current operation is independent of the V_{IN} voltage or V_{OUT} voltage ratio, hence it is possible on all device operation modes boost, buck, or buck-boost.

8.3.7 Protection Features

The following sections describe the protection features of the device.

8.3.7.1 Input Overvoltage Protection

The TPSM83100 and TPSM83101 have input overvoltage protection which avoids any damage to the device in case the current flows from the output to the input and the input source cannot sink current (for example, a diode in the supply path).

If forced PWM mode is active, the current can go negative until it reaches the sink current limit. Once the input voltage threshold, $V_{T+(IVP)}$, is reached on the VIN pin, the protection disables forced PWM mode and only allows current to flow from VIN to VOUT. After the input voltage drops under the input voltage protection threshold, forced PWM mode can be activated again.

8.3.7.2 Output Overvoltage Protection

The TPSM83100 and TPSM83101 have the output overvoltage protection which avoids any damage to the device in case the external feedback pin is not working properly.

When the output voltage threshold $V_{T+(OVP)}$ is reached at the VOUT pin, the protection disables the module power stage and makes the switching nodes high impedance.

8.3.7.3 Short Circuit Protection

The device features peak current limit performance at short circuit protection. 図 8-2 shows a typical device behavior of an short/overload event of the short circuit protection.

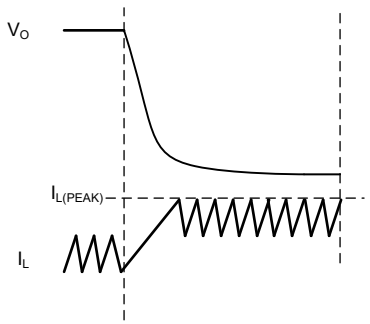


図 8-2. Typical Device Behavior During Short Circuit Protection

8.3.7.4 Thermal Shutdown

To avoid thermal damage of the device, the temperature of the die is monitored. The device stops operation once the sensed temperature rises over the typical thermal threshold 160 ˚C. After the temperature drops below the typical thermal shutdown hysteresis 25 ˚C, the module returns to normal operation.

8.4 Device Functional Modes

The device has two functional modes: off and on. The device enters the on mode when the voltage on the VIN pin is higher than the UVLO threshold and a high logic level is applied to the EN pin. The device enters the off mode when the voltage on the VIN pin is lower than the UVLO threshold or a low logic level is applied to the EN pin.

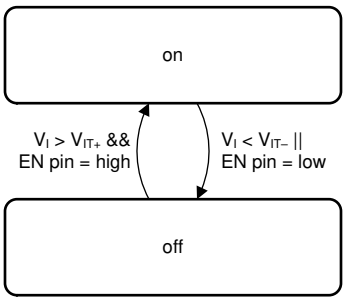


図 8-3. Device Functional Modes

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPSM83100 and TPSM83101 are high-efficiency, low-quiescent current, buck-boost modules. The devices are suitable for applications needing a regulated output voltage from an input supply that can be higher or lower than the output voltage.

9.2 Typical Application

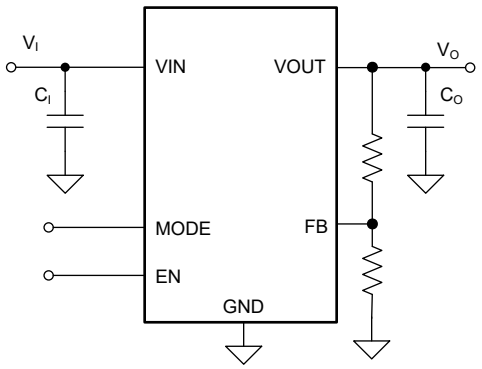


図 9-1. 3.3-V_{OUT} Typical Application

9.2.1 Design Requirements

The design parameters are listed in 表 9-1.

表 9-1. Design Parameters

PARAMETERS	VALUES
Input voltage	2.7 V to 4.3 V
Output voltage	3.3 V
Output current	1.0 A

9.2.2 Detailed Design Procedure

The first step is the selection of the output filter components. To simplify this process, Recommended Operating Conditions outlines minimum and maximum values for capacitance. Pay attention to the tolerance and derating when selecting nominal capacitance.

9.2.2.1 Output Capacitor Selection

For the output capacitor, use small ceramic capacitors placed as close as possible to the VOUT and PGND pins of the module. The recommended total nominal output capacitor value is 47 µF. If, for any reason, the application requires the use of large capacitors that cannot be placed close to the module, use a smaller ceramic capacitor in parallel to the large capacitor, and place the small capacitor as close as possible to the VOUT and PGND pins of the module.

It is important that the effective capacitance is given according to the recommended value in Recommended Operating Conditions. In general, consider DC bias effects resulting in less effective capacitance. The choice of the output capacitance is mainly a tradeoff between size and transient behavior as higher capacitance reduces transient response over/undershoot and increases transient response time. Possible output capacitors are listed in 表 9-2.

表 9-2. List of Recommended Capacitors

CAPACITOR VALUE [µF]	VOLTAGE RATING [V]	ESR [mΩ]	PART NUMBER	MANUFACTURER(1)	SIZE (METRIC)
47	6.3	10	GRM219R60J476ME44	Murata	0805 (2012)
47	10	40	CL10A476MQ8QRN	Semco	0603 (1608)

(1) See the *Third-Party Products Disclaimer*.

9.2.2.2 Input Capacitor Selection

A 22-µF input capacitor is recommended to improve line transient behavior of the regulator and EMI behavior of the total power supply circuit. An X5R or X7R ceramic capacitor placed as close as possible to the VIN and PGND pins of the module is recommended. This capacitance can be increased without limit. If the input supply is located more than a few inches from the TPSM83100, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

表 9-3. List of Recommended Capacitors

CAPACITOR VALUE [µF]	VOLTAGE RATING [V]	ESR [mΩ]	PART NUMBER	MANUFACTURER(1)	SIZE (METRIC)
22	6.3	43	GRM187R61A226ME15	Murata	0603 (1608)
10	10	40	GRM188R61A106ME69	Murata	0603 (1608)

(1) See the *Third-Party Products Disclaimer*.

9.2.2.3 Setting the Output Voltage

The output voltage is set by an external resistor divider. The resistor divider must be connected between VOUT, FB, and GND. The feedback voltage is 500 mV nominal.

Keep the low-side resistor R2 (between FB and GND) below 100 kΩ. The high-side resistor (between FB and VOUT) R1 is calculated with 式 2.

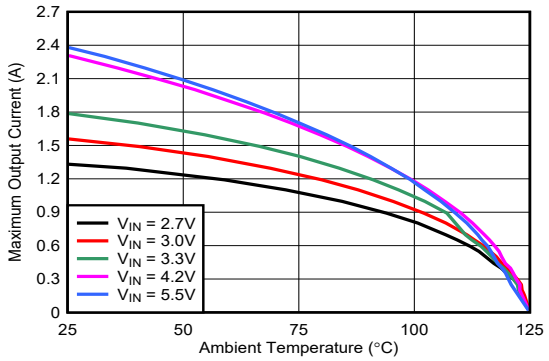
$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (2)$$

where V_{FB} = 500 mV.

表 9-4. Resistor Selection For Typical Output Voltages

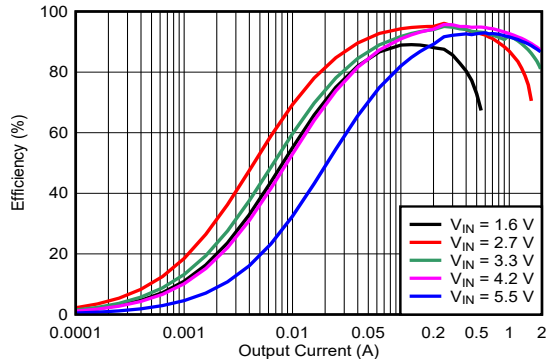
V_{OUT}	R1	R2
2.5 V	365 K	91 K
3.3 V	511 K	91 K
3.6 V	562 K	91 K
5.0 V	806 K	91 K

9.2.3 Application Curves



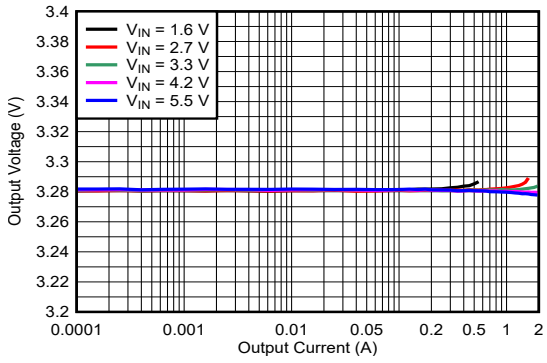
V_{OUT} = 3.3 V $R_{\Theta JA}$ = 48.9 ˚C/W

図 9-2. Safe Operating Area Based on Thermal Limitation



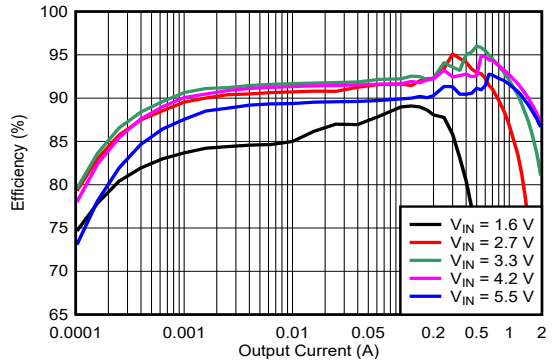
V_{OUT} = 3.3 V MODE = High

図 9-3. Efficiency vs Output Current (FPWM)



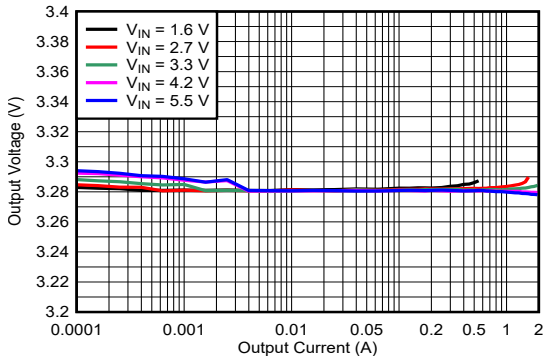
V_{OUT} = 3.3 V MODE = High

図 9-4. Load Regulation (FPWM)



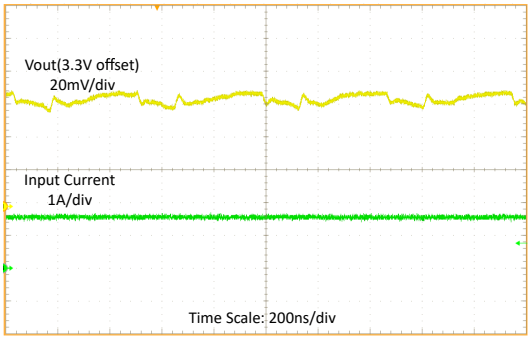
V_{OUT} = 3.3 V MODE = Low

図 9-5. Efficiency vs Input Voltage (PFM)



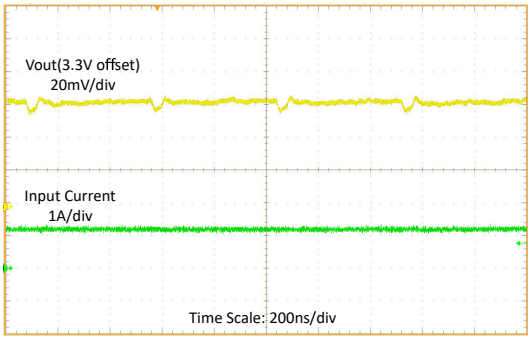
V_O = 3.3 V MODE = Low

図 9-6. Load Regulation (PFM)



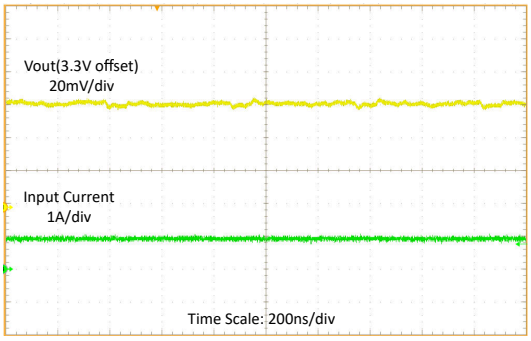
V_{IN} = 2.7 V, V_{OUT} = 3.3 V I_{OUT} = 1 A, MODE = Low

図 9-7. Steady State Waveforms, Boost Operation with 1-A Load



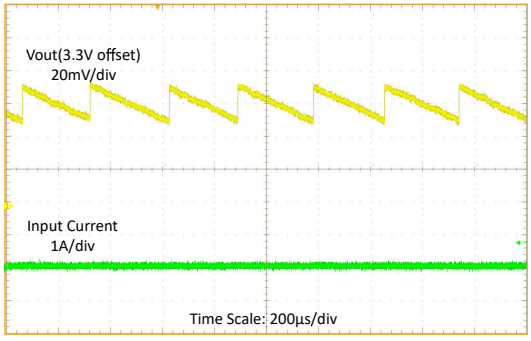
V_{IN} = 3.3 V, V_{OUT} = 3.3 V I_{OUT} = 1 A, MODE = Low

図 9-8. Steady State Waveforms, Buck-Boost with 1-A Load



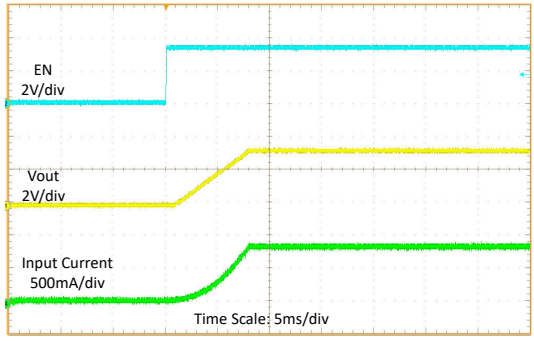
V_{IN} = 4.3 V, V_{OUT} = 3.3 V I_{OUT} = 1 A, MODE = Low

図 9-9. Steady State Waveforms, Buck Operation with 1-A Load



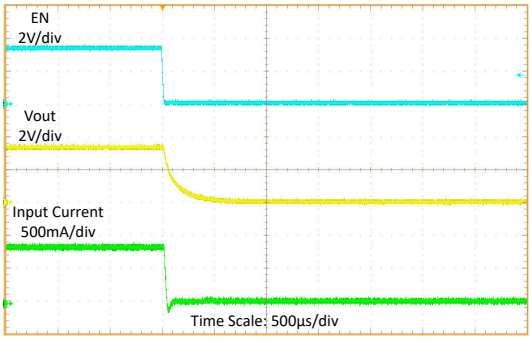
V_{IN} = 3.6 V, V_{OUT} = 3.3 V I_{OUT} = 1 mA, MODE = Low

図 9-10. Steady State Waveforms, with 1-mA Load



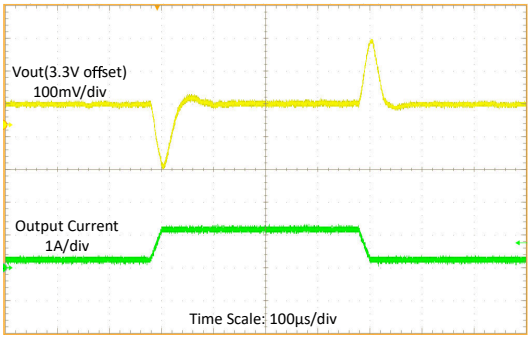
V_{IN} = 3.6 V, V_{OUT} = 3.3 V R_{load} = 4 Ω, MODE = Low

図 9-11. Start-Up by EN



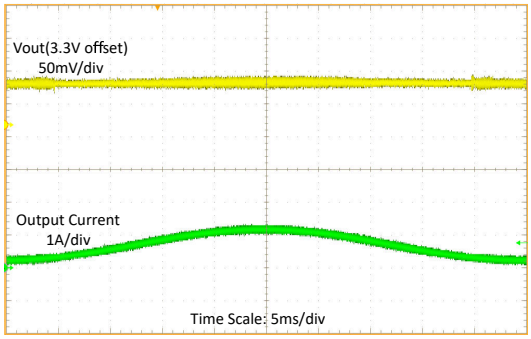
V_{IN} = 3.6 V, V_{OUT} = 3.3 V R_{load} = 4 Ω, MODE = Low

図 9-12. Shutdown by EN



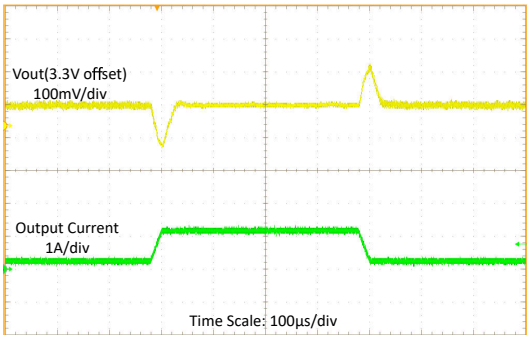
V_{IN} = 2.7 V, V_{OUT} = 3.3 V I_{OUT} = 100 mA to 1 A with 20-µs slew rate

図 9-13. Load Transient at 2.7-V Input Voltage



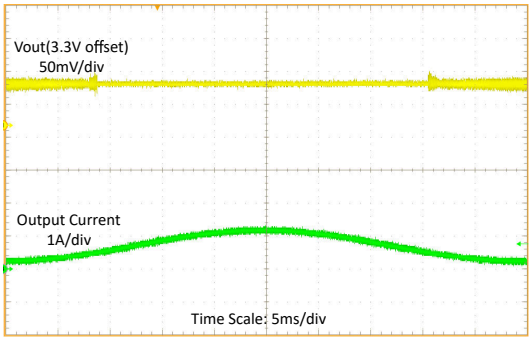
V_{IN} = 2.7 V, V_{OUT} = 3.3 V I_{OUT} = 100 mA to 1-A sweep

図 9-14. Load Sweep at 2.7-V Input Voltage



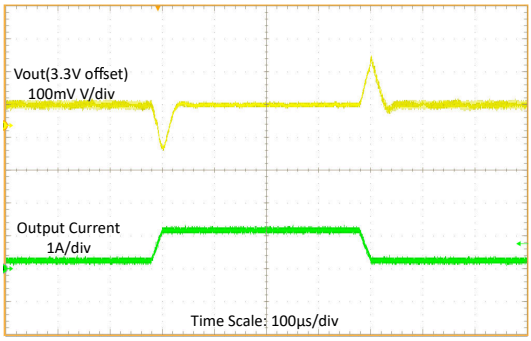
V_{IN} = 3.6 V, V_{OUT} = 3.3 V I_{OUT} = 100 mA to 1 A with 20-µs slew rate

図 9-15. Load Transient at 3.6-V Input Voltage



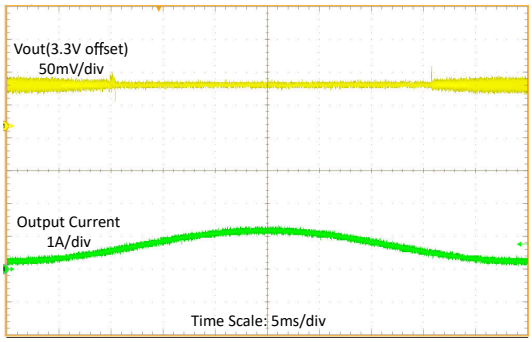
V_{IN} = 3.6 V, V_{OUT} = 3.3 V I_{OUT} = 100 mA to 1-A sweep

図 9-16. Load Sweep at 3.6-V Input Voltage



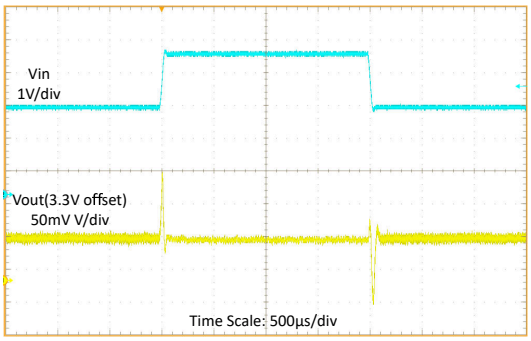
V_{IN} = 4.3 V, V_{OUT} = 3.3 V I_{OUT} = 100 mA to 1 A with 20-µs slew rate

図 9-17. Load Transient at 4.3-V Input Voltage



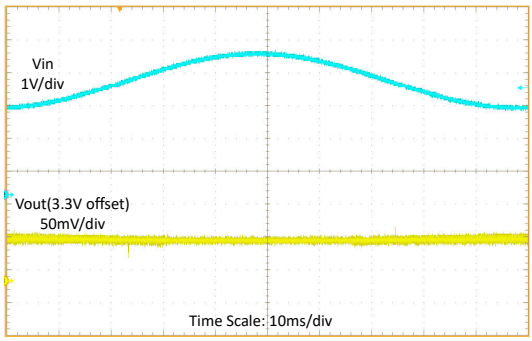
V_{IN} = 4.3 V, V_{OUT} = 3.3 V I_{OUT} = 100 mA to 1-A sweep

図 9-18. Load Sweep at 4.3-V Input Voltage



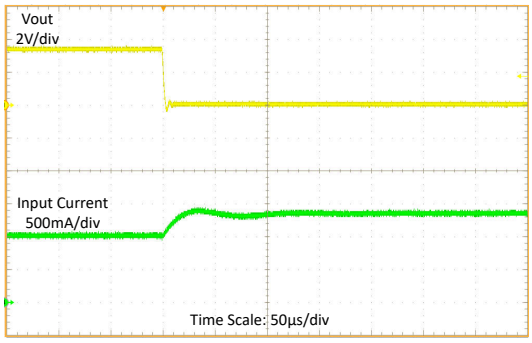
V_{IN} = 2.7 V to 4.3 V with 20-µs slew rate, V_{OUT} = 3.3 V I_{OUT} = 1 A

図 9-19. Line Transient at 1-A Load Current



V_{IN} = 2.7-V to 4.3-V sweep, V_{OUT} = 3.3 V I_{OUT} = 1 A

図 9-20. Line Sweep at 1-A Load Current



V_{IN} = 3.6 V, V_{OUT} = 3.3 V I_{OUT} = 1 A, FPWM

図 9-21. Output Short Protection (Entry)

表 9-5. Components for Application Characteristic Curves for V_{OUT} = 3.3 V

REFERENCE	DESCRIPTION(2)	PART NUMBER	MANUFACTURER(1)
U1	High Power Density 1.5 A Buck-Boost module	TPSM83100	Texas Instruments
C1	22 µF, 0603, Ceramic Capacitor, ±20%, 6.3 V	GRM187R61A226ME15	Murata
C2	47 µF, 0805, Ceramic Capacitor, ±20%, 6.3 V	GRM219R60J476ME44	Murata
R1	511 kΩ, 0603 Resistor, 1%, 100 mW	Standard	Standard
R2	91 kΩ, 0603 Resistor, 1%, 100 mW	Standard	Standard

(1) See the *Third-Party Products Disclaimer*.
(2) For other output voltages, refer to Resistor Selection for Typical Output Voltages for resistor values.

9.3 Power Supply Recommendations

The TPSM83100 and TPSM83101 have no special requirements for its input power supply. The input power supply output current needs to be rated according to the supply voltage, output voltage, and output current.

9.4 Layout

9.4.1 Layout Guidelines

The PCB layout is an important step to maintain the high performance of the TPSM83100 device.

- Place input and output capacitors as close as possible to the module. Traces need to be kept short. Route wide and direct traces to the input and output capacitors results in low trace resistance and low parasitic inductance.

9.4.2 Layout Example

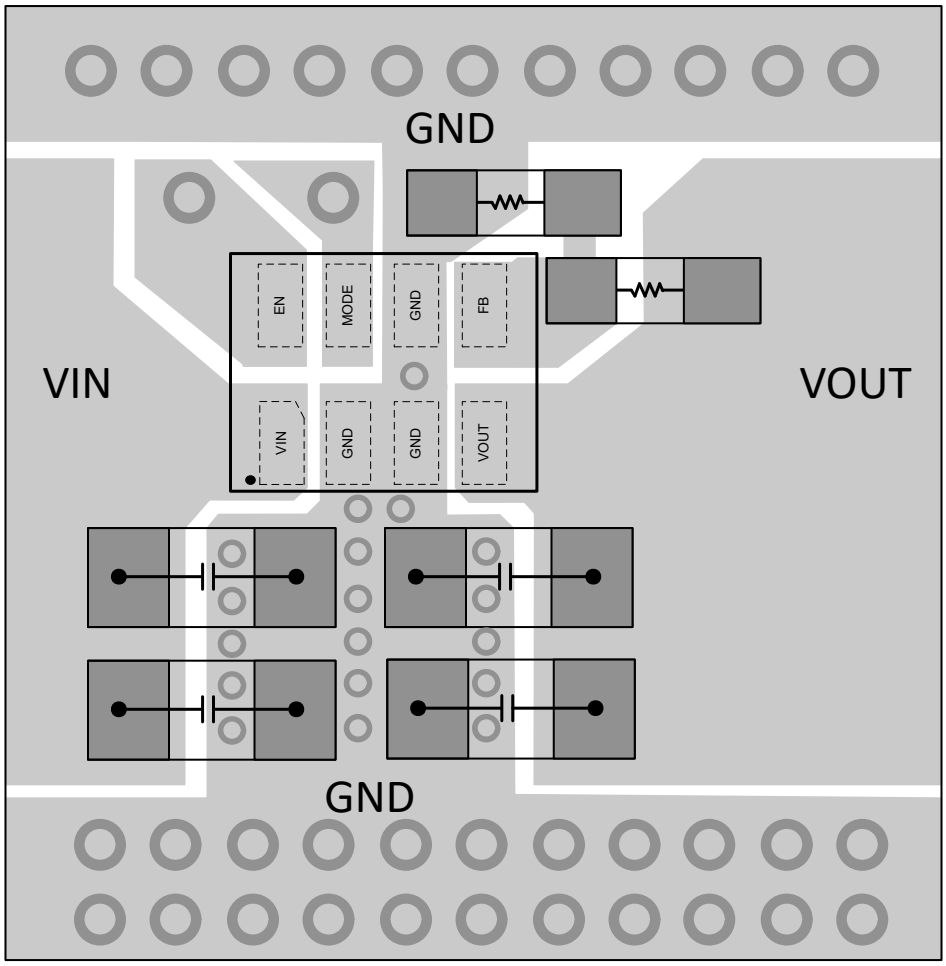


図 9-22. Layout Example

10 Device and Documentation Support

10.1 Device Support

10.1.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

10.1.2 Development Support

10.1.2.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the TPSM83100 and TPSM83101 devices with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint or cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you can:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

10.4 Trademarks

MicroSiP™ is a trademark of TI.
TI E2E™ are trademarks of Texas Instruments.
WEBENCH® is a registered trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

10.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

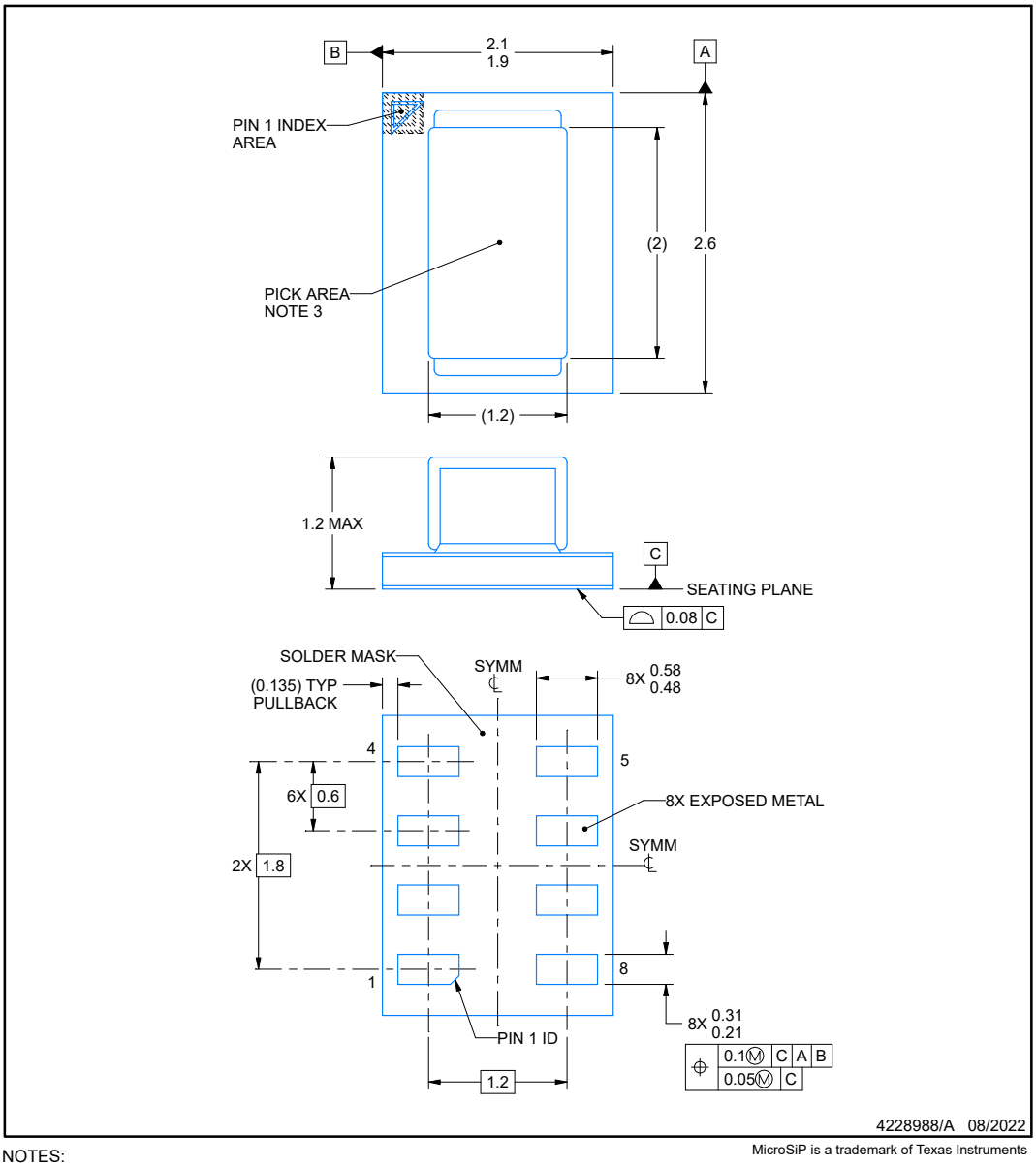
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

SIU0008A

MicroSiP™ - 1.2 mm max height

MICRO SYSTEM IN PACKAGE



MicroSiP is a trademark of Texas Instruments

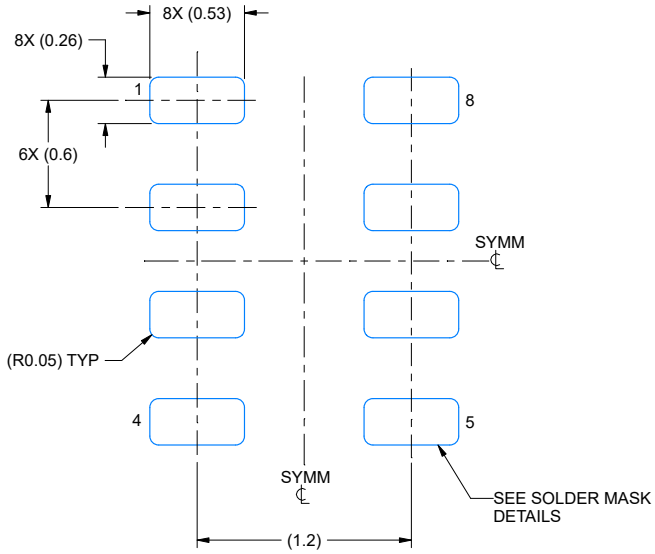
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pick and place nozzle ∅0.33 mm or smaller recommended.

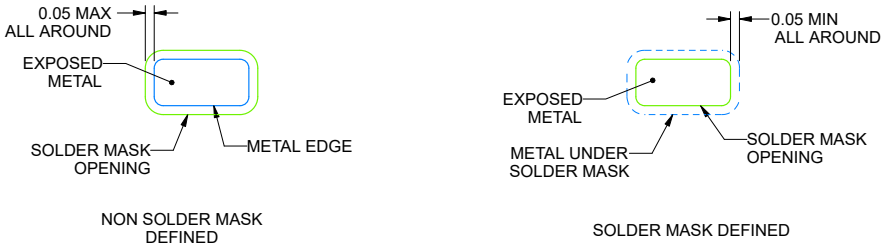
EXAMPLE BOARD LAYOUT

SIU0008A — **MicroSiP™ - 1.2 mm max height**

MICRO SYSTEM IN PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

4228988/A 08/2022

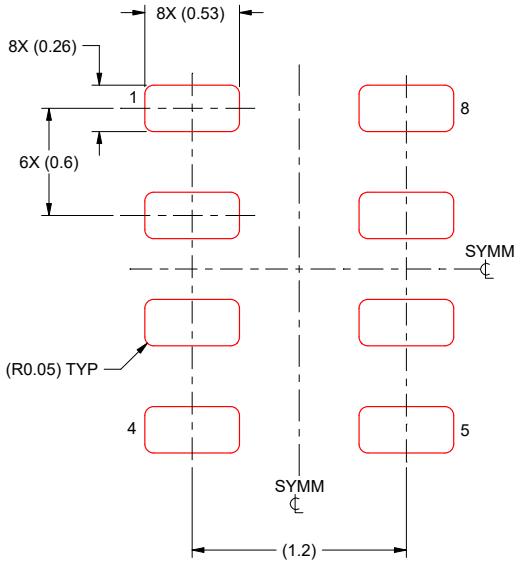
NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

SIU0008A — **MicroSiP™ - 1.2 mm max height**

MICRO SYSTEM IN PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:30X

4228988/A 08/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPSM83100SIUR	ACTIVE	uSiP	SIU	8	3000	RoHS & Green	ENEPIG	Level-2-260C-1 YEAR	-40 to 125	31NL TPSM8310X	Samples
TPSM83101SIUR	ACTIVE	uSiP	SIU	8	3000	RoHS & Green	ENEPIG	Level-2-260C-1 YEAR	-40 to 125	3EIL HYBM83101	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265