TEXAS INSTRUMENTS
TPSM83102, TPSM83103
JAJSP72 – AUGUST 2024

TPSM83102 および TPSM83103 1.2A 出力電流、昇降圧モジュール

1 特長

- 入力電圧範囲:1.6V～5.5V
  - スタートアップ時のデバイス入力電圧 > 1.65V
- 出力電圧範囲 (調整可能):1V～5.5V
- 高い出力電流能力、3A ピーク スイッチ電流
  - V_{IN} ≧ 3V、V_{OUT} = 3.3V 時の出力電流:1.5A
  - V_{IN} ≧ 2.7V、V_{OUT} = 3.3V 時の出力電流:1.2A
- 全負荷範囲にわたって高効率を実現
  - 静止電流:8µA (代表値)
  - 自動パワー セーブ モードおよび強制 PWM モードを構成可能
- ピーク電流昇降圧モード アーキテクチャ
  - シームレスなモード遷移
  - 順方向および逆方向電流動作
  - あらかじめ出力にバイアスを印加した状態で起動
  - 2MHz スイッチングの固定周波数動作
- 安全性と堅牢な動作機能
  - 過電流保護および短絡保護
  - アクティブ ランプを採用したソフト スタート機能内蔵
  - 過熱保護および過電圧保護
  - 負荷の切り離しを伴う真のシャットダウン機能
  - 順方向および逆方向の電流制限
- 小型ソリューション サイズ
  - 2.6mm × 2.0mm × 1.2mm (最大) 8 ピン µSiP パッケージ

2 アプリケーション

- TWS
- システム プリレギュレータ (スマートフォン、タブレット、端末、テレマティクス)
- ポイント オブ ロード レギュレーション (有線センサ、ポート / ケーブル アダプタ、ドングル)
- 指紋、カメラ センサ (電子スマート ロック、IP ネットワーク カメラ)
- 電圧スタビライザ (データコム、光モジュール、冷却 / 加熱)

3 概要

TPSM83102 および TPSM83103 は、小型 µSiP モジュール パッケージに封止された定周波数ピーク電流モード制御昇降圧コンバータです。3A のピーク電流制限 (標準値) と 1.6V～5.5V の入力電圧範囲を備え、システム プリレギュレータと電圧スタビライザの電源ソリューションを提供します。

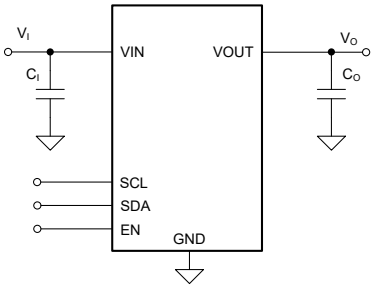
TPSM83102 および TPSM83103 は入力電圧に応じて自動的に昇圧モード、降圧モード、3 サイクル昇降圧モード (入力電圧が出力電圧とほぼ等しい場合) で動作します。モード間の遷移は定義されたデューティ サイクルで発生し、モード間の不要な切り替えが避けられるので出力電圧リップルを減らすことができます。8µA の静止電流とパワー セーブ モードの電力により、軽負荷から無負荷までの状況で最高の効率を実現します。

このデバイスは、µSiP モジュール パッケージで非常に小型のソリューション サイズを実現しています。

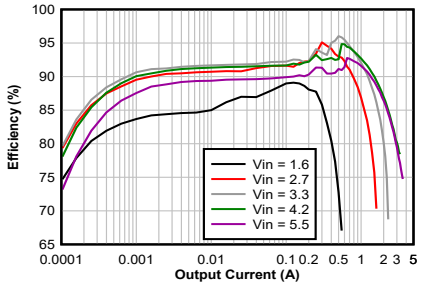
パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)
TPSM83102(2)	µSiP モジュール	2.6mm × 2.0mm × 1.2mm (最大高さ)
TPSM83103	µSiP モジュール	2.6mm × 2.0mm × 1.2mm (最大高さ)

(1) 供給されているすべてのパッケージについては、セクション 12 を参照してください。
(2) 製品プレビュー詳細は テキサス・インスツルメンツまでお問い合わせください。



代表的なアプリケーション



効率と出力電流との関係 (V_{OUT} = 3.3V)

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4 Device Comparison Table

PART NUMBER	Default Setting of Internal EN(2)	I2C Slave Address
TPSM83102(1)	CONVERTER_EN = 0	0x6A
TPSM831021(1)	CONVERTER_EN = 0	0x68
TPSM831022(1)	CONVERTER_EN = 0	0x69
TPSM831023(1)	CONVERTER_EN = 0	0x6B
TPSM83103	CONVERTER_EN = 1	0x6A

(1) Product Preview. Contact TI factory for more information.
(2) Refer to the register map.

5 Pin Configuration and Functions

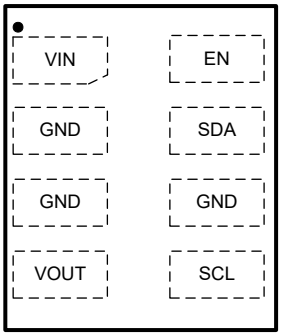


図 5-1. 8-Pin SIU µSiP Module Package (Top View)

表 5-1. Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
VIN	1	PWR	Supply input voltage
GND	2, 3, 6	PWR	Power ground
VOUT	4	PWR	Power stage output
SCL	5	I/O	I2C serial interface clock. Pull this pin up to the I2C bus voltage with a resistor or a current source.
SDA	7	I/O	I2C serial interface data. Pull this pin up to the I2C bus voltage with a resistor or a current source.
EN	8	I	Device enable. Set High to enable and Low to disable. It must not be left floating.

(1) PWR = power, I = input, I/O = input and output

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_I	Input voltage (VIN, VOUT, EN, SCL, SDA)(2)	–0.3	6.0	V
	Input voltage for less than 10 ns	–0.3	7	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal, unless otherwise noted.

6.2 ESD Rating

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JS-002(2)	± 500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_I	Supply voltage		1.6		5.5	V
V_O	Output voltage		1.0		5.5	V
C_I	Effective Input capacitance	V_I = 1.6 V to 5.5 V	4.2			µF
C_O	Effective Output capacitance	1.2 V ≤ V_O ≤ 3.6 V, nominal value at V_O = 3.3 V	10.4	16.9	330	µF
		3.6 V < V_O ≤ 5.5 V, nominal value at V_O = 5 V	7.95	10.6	330	µF
L	Effective Inductance		0.7	1	1.3	µH
T_J	Operating junction temperature range		–40		125	°C

6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC		TPSM83102 TPSM83103	UNIT
		uSiP-SIU	
		8	
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	100	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	42.2	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	33.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	N/A	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	32.2	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

6.5 Electrical Characteristics

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted). Typical values are at V_I = 3.8 V , V_O = 3.3 V and T_J = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY								
I_{SD}	Shutdown current into VIN		V_I = 3.8 V, $V_{(EN)}$ = 0 V	T_J = 25°C		0.5	0.9	µA
I_Q	Quiescent current into VIN		V_I = 2.2 V, V_O = 3.3 V, $V_{(EN)}$ = 2.2 V, no switching			0.15	6.1	µA
I_Q	Quiescent current into VOUT		V_I = 2.2 V, V_O = 3.3 V, $V_{(EN)}$ = 2.2 V, no switching			8		µA
V_{IT+}	Positive-going UVLO threshold voltage				1.5	1.55	1.599	V
V_{IT-}	Negative-going UVLO threshold voltage		During start-up		1.4	1.45	1.499	V
V_{hys}	UVLO threshold voltage hysteresis				99			mV
$V_{I(POR)T+}$	Positive-going POR threshold voltage		maximum of V_I or V_O		1.25	1.45	1.65	V
$V_{I(POR)T-}$	Negative-going POR threshold voltage				1.22	1.43	1.6	V
I/O SIGNALS								
V_{T+}	Positive-going threshold voltage	EN, MODE			0.77	0.98	1.2	V
V_{T-}	Negative-going threshold voltage	EN, MODE			0.5	0.66	0.76	V
V_{hys}	Hysteresis voltage	EN, MODE				300		mV
I_{IH}	High-level input current	(EN, MODE)	$V_{(EN)}$ = $V_{(MODE)}$ = 1.5 V, no pullup resistor			±0.01	±0.25	µA
I_{IL}	Low-level input current	(EN, MODE)	$V_{(EN)}$ = $V_{(MODE)}$ = 0 V,			±0.01	±0.1	µA
	Input bias current	(EN, MODE)	$V_{(EN)}$ = 5.5 V			±0.01	±0.3	µA
POWER SWITCH								
$r_{DS(on)}$	On-state resistance	Q1	V_I = 3.8 V, V_O = 3.3 V, test current = 0.2 A			45		mΩ
		Q2				50		mΩ
		Q3				50		mΩ
		Q4				85		mΩ
CURRENT LIMIT								
$I_{L(PEAK)}$	Switch peak current limit (1)	Q1	Vin=3.8V, V_O = 3.3 V	Output sourcing current	2.6	3	3.35	A
	PFM mode entry threshold (peak) current (1)		I_O falling			145		mA
OUTPUT								
CONTROL[FEEDBACK PIN]								
PROTECTION FEATURES								
$V_{T+(OVP)}$	Positive-going OVP threshold voltage				5.55	5.75	5.95	V
$V_{T+(IVP)}$	Positive-going IVP threshold voltage				5.55	5.75	5.95	V
TIMING PARAMETERS								
$t_{d(EN)}$	Delay between a rising edge on the EN pin and the start of the output voltage ramp					0.87	1.5	ms
$t_{d(ramp)}$	Soft-start ramp time				6.42	7.55	8.68	ms
f_{SW}	Switching frequency				1.8	2	2.2	MHz

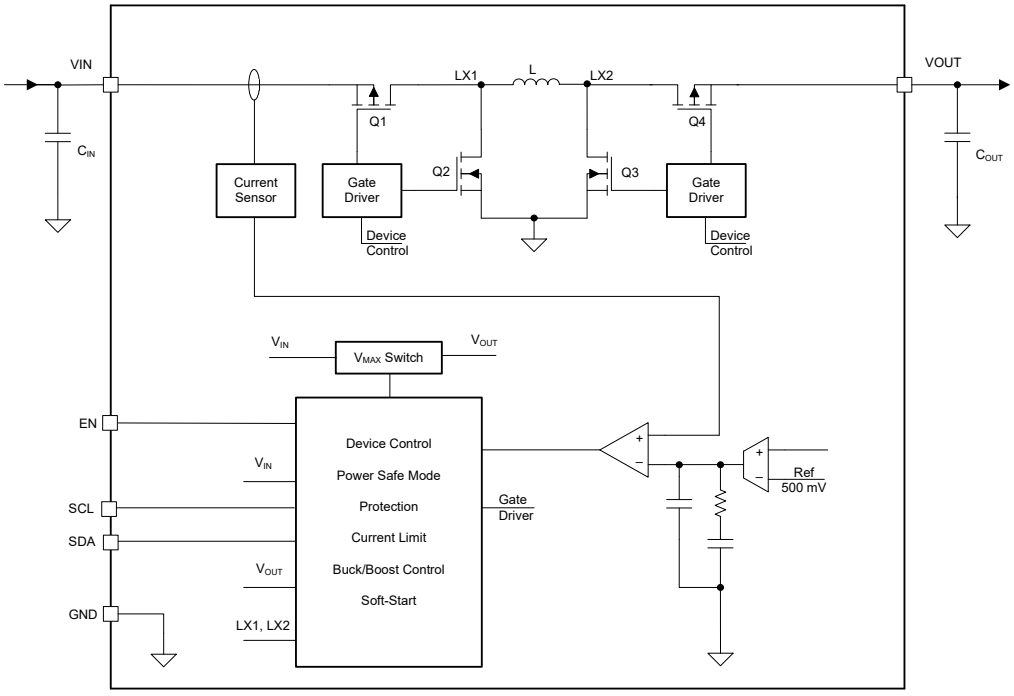
(1) Current limit production test are performed under DC conditions. The current limit in operation is somewhat higher and depending on propagation delay and the applied external components

7 Detailed Description

7.1 Overview

The TPSM83102 and TPSM83103 is a constant frequency peak current mode control buck-boost converter. The converter uses a fixed-frequency topology with approximately 2-MHz switching frequency. The modulation scheme has three clearly defined operation modes where the converters enter with defined thresholds over the full operation range of V_{IN} and V_{OUT}. The maximum output current is determined by the Q1 peak current limit, which is typically 3 A.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

The input voltage of the VIN pin is continuously monitored if the device is not in shutdown mode. UVLO only stops or starts the converter operation. The UVLO does not impact the core logic of the device. UVLO avoids a brownout of the device during device operation. In case the supply voltage on the VIN pin is lower that the negative-going threshold of UVLO, the converter stops its operation. To avoid a false disturbance of the power conversion, the UVLO falling threshold logic signal is digitally de-glitched.

If the supply voltage on the VIN pin recovers to be higher than the UVLO rising threshold, the converter returns to operation. In this case, the soft-start procedure restarts faster than under start-up without a pre-biased output.

7.3.2 Enable and Soft Start

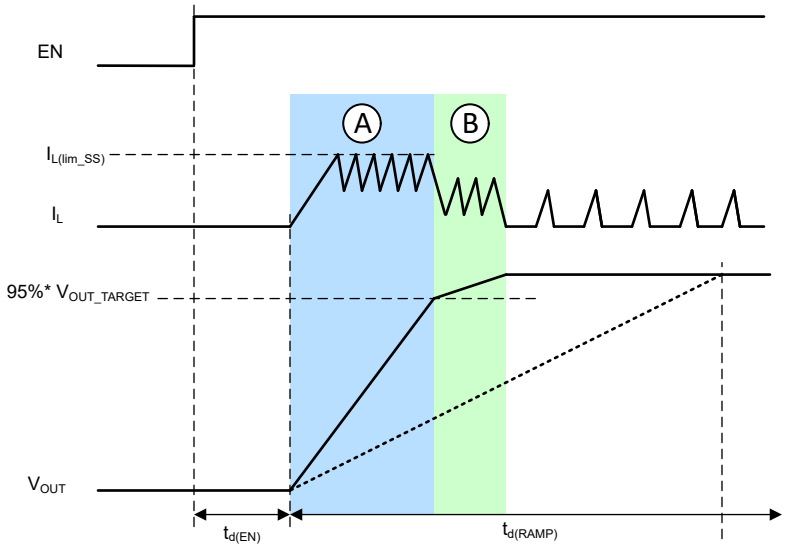


図 7-1. Typical Soft-Start Behavior

When the input voltage is above the UVLO rising threshold and the EN pin is pulled to a voltage above 1.2 V, the TPSM83102 and TPSM83103 are enabled and start up after a short delay time, $t_{d(EN)}$.

The devices have an inductor peak current clamp to limit the inrush current during start-up. When the minimum current clamp ($I_{L(lim\_SS)}$) is lower than the current that is necessary to follow the voltage ramp, the current automatically increases to follow the voltage ramp. The minimum current limit ensures as fast as possible soft start if the capacitance is chosen lower than what the ramp time $t_{d(RAMP)}$ was selected for.

In a typical start-up case as shown in 図 7-1 (low output load, typical output capacitance), the minimum current clamp limits the inrush current and charges the output capacitor. The output voltage then rises faster than the reference voltage ramp (see phase A in 図 7-1). To avoid an output overshoot, the current clamp is deactivated when the output is close to the target voltage and follows the reference voltage ramp slew value given by the voltage ramp, which is finishing the start up (see phase B in 図 7-1). The transition from the minimum current clamp operation is sensed by using the threshold 95% Vout_target. After phase B, the output voltage is well regulated to the nominal target voltage. The current waveform depends on the output load and operation mode.

7.3.3 Adjustable Output Voltage

The output voltage is adjusted by the I2C control. Please refer to the part of "Programming" and "Register Map" for the Vout settings.

7.3.4 Reverse Current Operation

The device can support reverse current operation in FPWM mode(the current flows from VOUT pin to VIN pin). If the output feedback voltage on the FB pin is higher than the reference voltage, the converter regulation forces a current into the input capacitor. The reverse current operation is independent of the V_{IN} voltage or V_{OUT} voltage ratio, hence it is possible on all device operation modes boost, buck, or buck-boost.

7.3.5 Protection Features

The following sections describe the protection features of the device.

7.3.5.1 Input Overvoltage Protection

The TPSM83102 and TPSM83103 have input overvoltage protection which avoids any damage to the device in case the current flows from the output to the input and the input source cannot sink current (for example, a diode in the supply path).

If forced PWM mode is active, the current can go negative until it reaches the sink current limit. Once the input voltage threshold, $V_{T+(IVP)}$, is reached on the VIN pin, the protection disables forced PWM mode and only allows current to flow from VIN to VOUT. After the input voltage drops under the input voltage protection threshold, forced PWM mode can be activated again.

7.3.5.2 Short Circuit Protection

The device features peak current limit performance at short circuit protection. 図 7-2 shows a typical device behavior of an short/overload event of the short circuit protection.

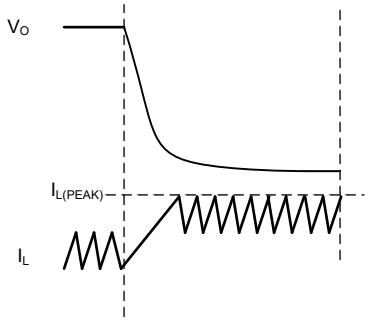


図 7-2. Typical Device Behavior During Short Circuit Protection

7.3.5.3 Thermal Shutdown

To avoid thermal damage of the device, the temperature of the die is monitored. The device stops operation once the sensed temperature rises over the thermal threshold. After the temperature drops below the thermal shutdown hysteresis, the converter returns to normal operation.

7.4 Device Functional Modes

The device has two functional modes: off and on. The device enters the on mode when the voltage on the VIN pin is higher than the UVLO threshold and a high logic level is applied to the EN pin. The device enters the off mode when the voltage on the VIN pin is lower than the UVLO threshold or a low logic level is applied to the EN pin.

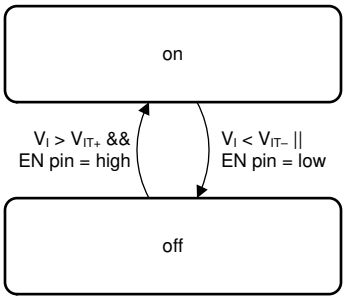


図 7-3. Device Functional Modes

7.5 Programming

7.5.1 Serial Interface Description

I²C is a 2-wire serial interface developed by Philips Semiconductor, now NXP Semiconductors (see *NXP Semiconductors, UM10204 – I²C-Bus Specification and User Manual*). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C-compatible devices connect to the I²C bus through open-drain I/O pins, SDA, and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START

and STOP of data transfer. A slave device receives and transmits data on the bus under control of the master device.

The device works as a slave and supports the following data transfer modes, as defined in the I²C-Bus Specification:

- Standard-mode (100 kbps)
- Fast-mode (400 kbps)
- Fast-mode Plus (1 Mbps)

The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values, depending on the instantaneous application requirements. Register contents remain intact as long as supply voltage remains above $V_{IT+(POR)}$.

The data transfer protocol for standard and fast modes is exactly the same, therefore, it is referred to as F/S-mode in this document. The device supports 7-bit addressing; 10-bit addressing and general call address are not supported. The device 7-bit address is 6Ah (01101010b).

To make sure that the I²C function in the device is correctly reset, it is recommended that the I²C master initiates a STOP condition on the I²C bus after the initial power up of SDA and SCL pullup voltages.

7.5.2 Standard-, Fast-, and Fast-Mode Plus Protocol

The master initiates a data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in 図 7-4. All I²C-compatible devices recognize a start condition.

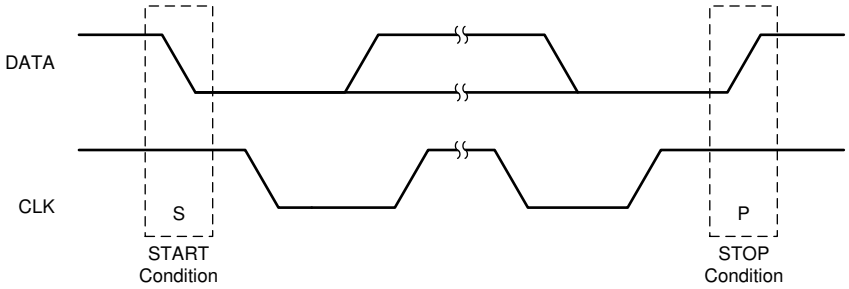


図 7-4. START and STOP Conditions

The master then generates the SCL pulses and transmits the 7-bit address and the read/write direction bit, R/W, on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see 図 7-5). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see 図 7-6) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

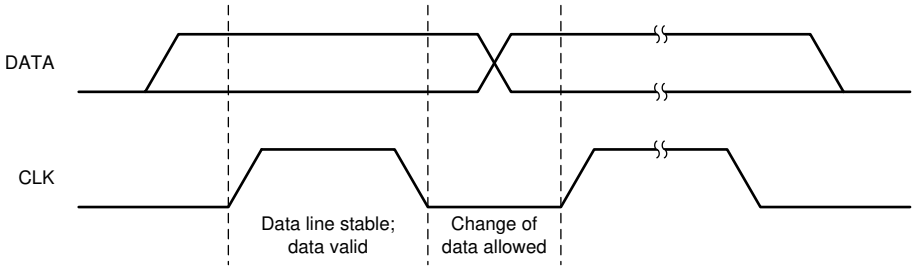


図 7-5. Bit Transfer on the Serial Interface

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. An acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see 図 7-4). This releases the bus and stops the communication link with the addressed slave. All I^2C-compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released and they wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section results in 00h being read out.

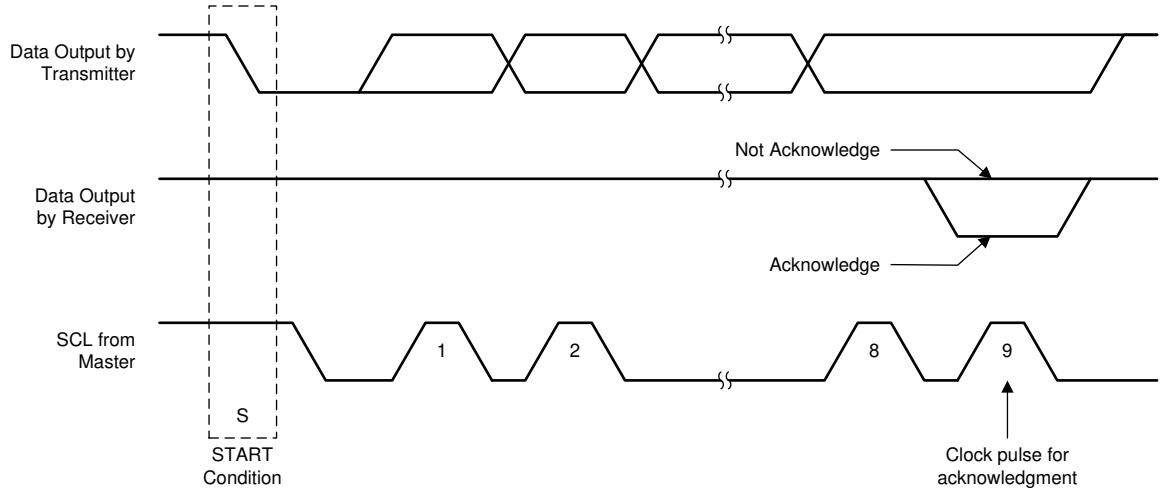


図 7-6. Acknowledge on the I^2C Bus

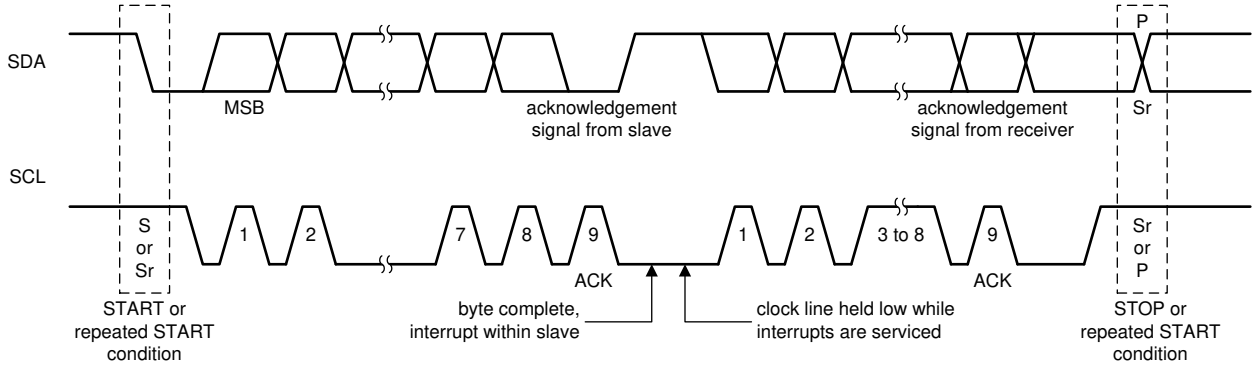


図 7-7. Bus Protocol

7.5.3 I^2C Update Sequence

A single update requires the following:

- A start condition
- A valid I^2C slave address
- A register address
- A data byte

To acknowledge the receipt of each byte, the device pulls the SDA line low during the high period of a single clock pulse. The device performs an update on the falling edge of the acknowledge signal that follows the last byte.

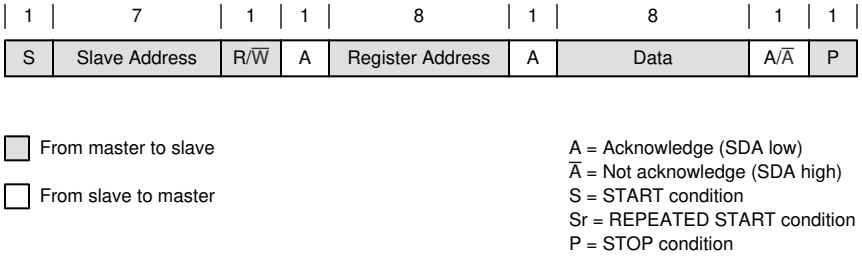


図 7-8. “Write” Data Transfer Format in Standard, Fast, and Fast-Plus Modes

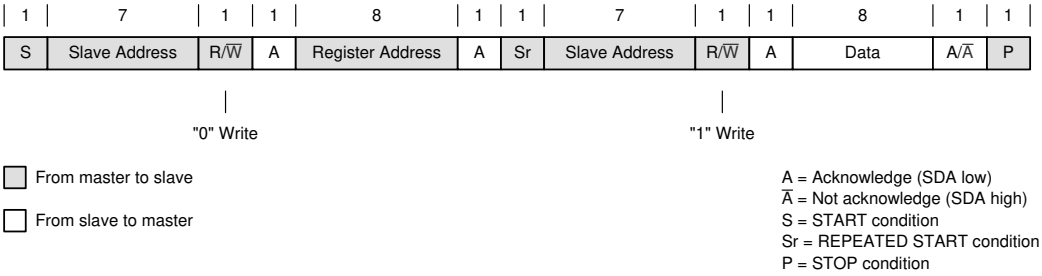


図 7-9. “Read” Data Transfer Format in Standard, Fast, and Fast-Plus Modes

7.6 Register Map

7.6.1 Register Description

7.6.1.1 Register Map

表 7-1. Register Map

ADDRESS	ACRONYM	REGISTER NAME	SECTION
0x02	CONTROL1	Control 1 Register	Go
0x03	VOUT	VOUT Register	Go
0x05	CONTROL2	Control 2 Register	Go

7.6.1.2 Register CONTROL1 (Register address: 0x02; Default: 0x08)

Return to Register Map

表 7-2. Register CONTROL1 Format

7	6	5	4	3	2	1	0
NIL[3:0]				NIL	EN_SCP	NIL	CONVERTER_EN
R				R	R/W	R	R/W

LEGEND: R/W = Read/Write; R = Read only

SCP: Short Circuit Protection

表 7-3. Register CONTROL1 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	NIL	R	0b0000	Not used. During write operations data for these bits are ignored. During read operations 0 is returned
3	EN_FAST_DVS	R/W	0b1	Sets DVS to fast mode 0 : DISABLE, 1 : ENABLE
2	EN_SCP	R/W	0b0	Enable short circuit hiccup protection 0 : DISABLE, 1 : ENABLE
1	NIL	R	0b0	Not used.
0	CONVERTER_EN	R/W	0b0	Enable Converter ('AND'ed with EN-pin) 0 : DISABLE, 1 : ENABLE

7.6.1.3 Register VOUT (Register address: 0x03; Default: 0x5C)

Return to Register Map

表 7-4. Register VOUT Format

7	6	5	4	3	2	1	0
VOUT[7 :0]							
R/W							

LEGEND: R/W = Read/Write

表 7-5. Register VOUT Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VOUT[7:0]	R/W	0x5C	These bits set the output voltage Output voltage = 1.000 + (VOUT[7 :0] × 0.025) V when 0x00<=VOUT[7 :0]<=0xB4; Output voltage = 5.5 V when 0xB5<=VOUT[7 :0]<=0xFF

7.6.1.4 Register CONTROL2 (Register address: 0x05; Default: 0x45)

Return to Register Map

表 7-6. Register CONTROL2 Format

7	6	5	4	3	2	1	0
FPWM	FAST_RAMP_EN	EN_DISCH_VOUT[1:0]		CL_RAMP_MIN	TD_RAMP[2:0]		
R/W	R/W	R/W		R/W	R/W		

LEGEND: R/W = Read/Write

表 7-7. Register CONTROL2 Field Descriptions

Bit	Field	Type	Reset	Description
7	FPWM	R/W	0b0	Force PWM operation 0 : DISABLE, 1 : ENABLE
6	FAST_RAMP_EN	R/W	0b1	Device can start-up faster then VOUT ramp 0 : DISABLE, 1 : ENABLE

表 7-7. Register CONTROL2 Field Descriptions (続き)

Bit	Field	Type	Reset	Description
5:4	EN_DISCH_VOUT[1:0]	R/W	0b00	Enable of BUBO Vout Discharge 00 : DISABLE 01 : SLOW (34mA) 10 : MEDIUM (67mA) 11 : FAST (100mA)
3	CL_RAMP_MIN	R/W	0b0	Define the minimum current limit during the soft start ramp 0 : Low (500mA) 1 : High (2x Low)
2:0	TD_RAMP[2:0]	R/W	0b101	Defines the ramp time for the Vo soft start ramp 000: 0.256ms 001: 0.512ms 010: 1.024ms 011: 1.920ms 100: 3.584ms 101: 7.552ms 110: 9.600ms 111: 24.320ms

8 Application and Implementation

注

以下のアプリケーション情報は、テキサス・インスツルメンツの製品仕様に含まれるものではなく、テキサス・インスツルメンツはその正確性も完全性も保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TPSM83102 and TPSM83103 are a high-efficiency, low-quiescent current, buck-boost modules. The devices are suitable for applications needing a regulated output voltage from an input supply that can be higher or lower than the output voltage. The output voltage can be set from 1.0V to 5.5V conveniently by I2C.

8.2 Typical Application

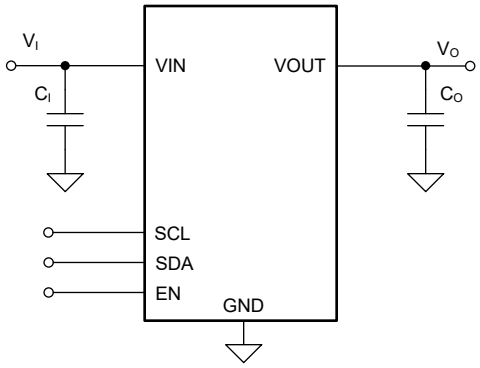


図 8-1. 3.3-V_{OUT} Typical Application

8.2.1 Design Requirements

The design parameters are listed in 表 8-1.

表 8-1. Design Parameters

PARAMETERS	VALUES
Input voltage	2.7 V to 4.3 V
Output voltage	3.3 V
Output current	1.5 A

8.2.2 Detailed Design Procedure

The first step is the selection of the output filter components. To simplify this process, セクション 6.3 outlines minimum and maximum values for capacitance. Pay attention to the tolerance and derating when selecting nominal capacitance.

8.2.2.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the TPSM83102 and TPSM83103 devices with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint or cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you can:

- Run electrical simulations to see important waveforms and circuit performance,
- Run thermal simulations to understand the thermal performance of your board,
- Export your customized schematic and layout into popular CAD formats,
- Print PDF reports for the design, and share your design with colleagues.

5. Get more information about WEBENCH tools at www.ti.com/webench.

8.2.2.2 Output Capacitor Selection

For the output capacitor, use small ceramic capacitors placed as close as possible to the VOUT and PGND pins of the IC. The recommended nominal output capacitor value is a single 47 µF. If, for any reason, the application requires the use of large capacitors that cannot be placed close to the IC, use a smaller ceramic capacitor in parallel to the large capacitor. and place the small capacitor as close as possible to the VOUT and PGND pins of the module.

It is important that the effective capacitance is given according to the recommended value in セクション 6.3. In general, consider DC bias effects resulting in less effective capacitance. The choice of the output capacitance is mainly a tradeoff between size and transient behavior as higher capacitance reduces transient response over/undershoot and increases transient response time. Possible output capacitors are listed in 表 8-2.

表 8-2. List of Recommended Capacitors

CAPACITOR VALUE [µF]	VOLTAGE RATING [V]	ESR [mΩ]	PART NUMBER	MANUFACTURER(1)	SIZE (METRIC)
47	6.3	10	GRM219R60J476ME44	Murata	0805 (2012)
47	10	40	CL10A476MQ8QRN	Semco	0603 (1608)

(1) See the セクション 10.1.1.

8.2.2.3 Input Capacitor Selection

A 22-µF input capacitor is recommended to improve line transient behavior of the regulator and EMI behavior of the total power supply circuit. An X5R or X7R ceramic capacitor placed as close as possible to the VIN and PGND pins of the module is recommended. This capacitance can be increased without limit. If the input supply is located more than a few inches from the TPSM83102 or TPSM83103, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

表 8-3. List of Recommended Capacitors

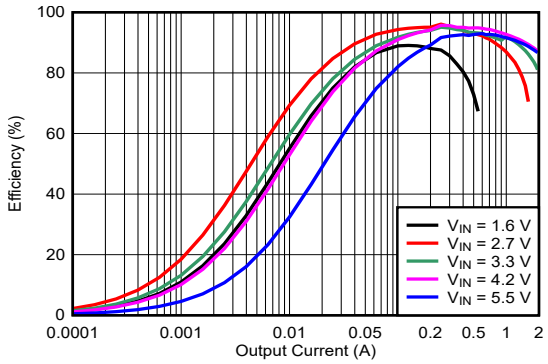
CAPACITOR VALUE [µF]	VOLTAGE RATING [V]	ESR [mΩ]	PART NUMBER	MANUFACTURER(1)	SIZE (METRIC)
22	6.3	43	GRM187R61A226ME15	Murata	0603 (1608)
10	10	40	GRM188R61A106ME69	Murata	0603 (1608)

(1) See the セクション 10.1.1.

8.2.2.4 Setting the Output Voltage

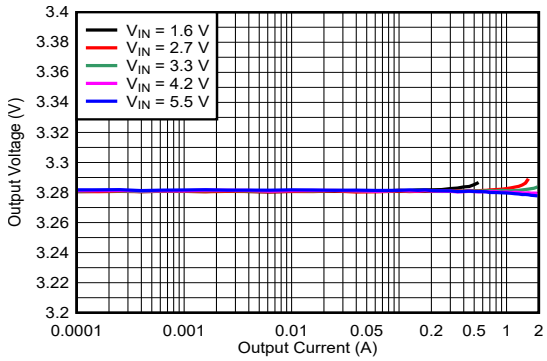
The output voltage is set by I2C. Please refer to the part of "Register Vout" for the detailed output voltage settings.

8.2.3 Application Curves



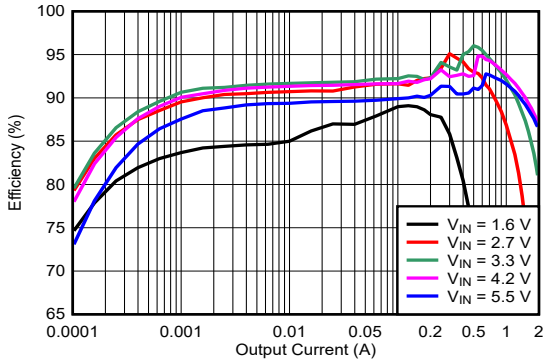
V_{OUT} = 3.3 V MODE = High

図 8-2. Efficiency vs Output Current (FPWM)



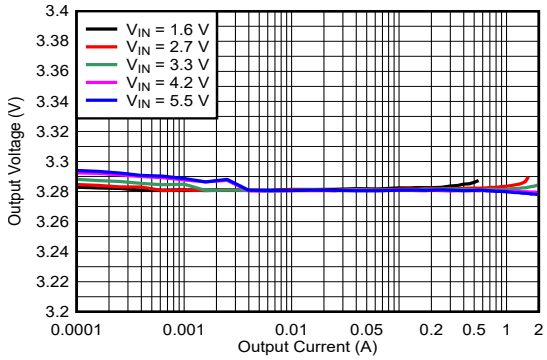
V_{OUT} = 3.3 V MODE = High

図 8-3. Load Regulation (FPWM)



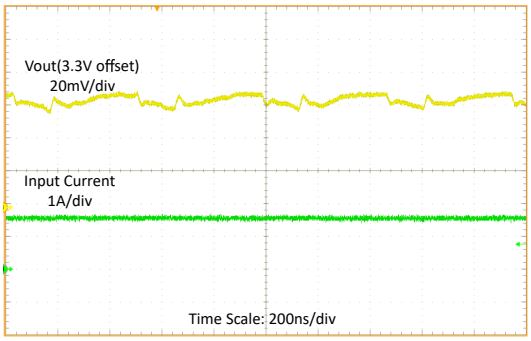
V_{OUT} = 3.3 V MODE = Low

図 8-4. Efficiency vs Input Voltage (PFM)



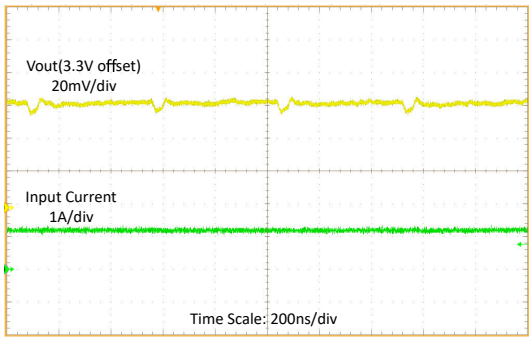
V_O = 3.3 V MODE = High

図 8-5. Load Regulation (PFM)



V_{IN} = 2.7 V, V_{OUT} = 3.3 V I_{OUT} = 1 A, MODE = Low

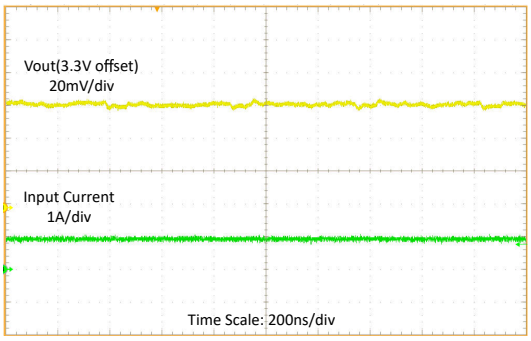
図 8-6. Switching Waveforms, Boost Operation with 1-A Load



V_{IN} = 3.3 V, V_{OUT} = 3.3 V I_{OUT} = 1 A, MODE = Low

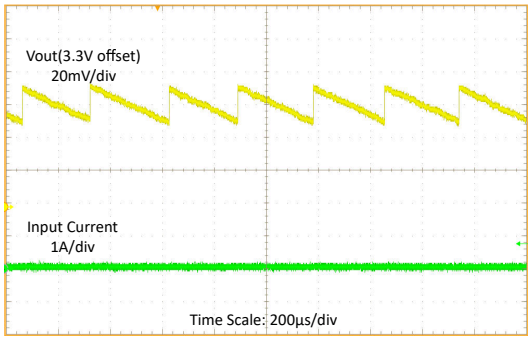
図 8-7. Switching Waveforms with 1-A Load

8.2.3 Application Curves (continued)



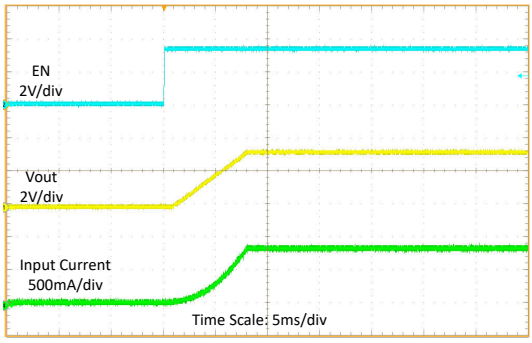
V_{IN} = 4.3 V, V_{OUT} = 3.3 V I_{OUT} = 1 A, MODE = Low

図 8-8. Switching Waveforms, Buck Operation with 1-A Load



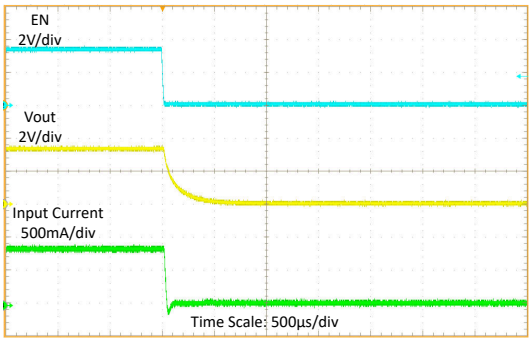
V_{IN} = 3.6 V, V_{OUT} = 3.3 V I_{OUT} = 1 mA, MODE = Low

図 8-9. Switching Waveforms at 1-mA Load



V_{IN} = 3.6 V, V_{OUT} = 3.3 V R_{load} = 4 Ω, MODE = Low

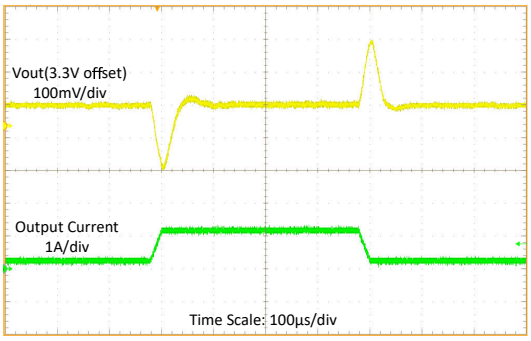
図 8-10. Start-Up by EN



V_{IN} = 3.6 V, V_{OUT} = 3.3 V R_{load} = 4 Ω, MODE = Low

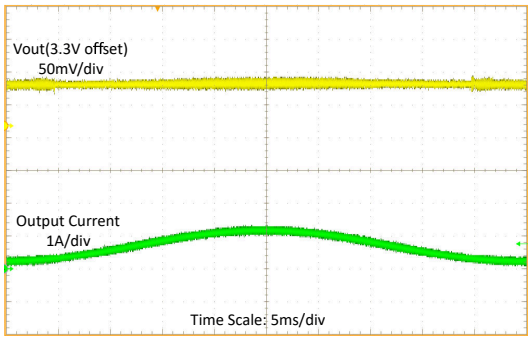
図 8-11. Shutdown by EN

8.2.3 Application Curves (continued)



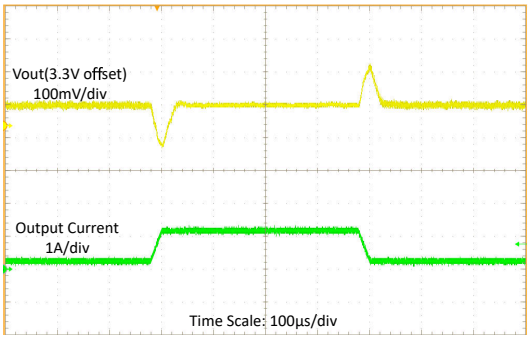
V_{IN} = 2.7 V, V_{OUT} = 3.3 V I_{OUT} = 100 mA to 1 A with 20-µs slew rate

図 8-12. Load Transient at 2.7-V Input Voltage



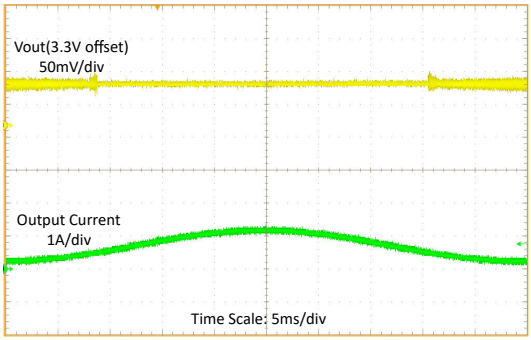
V_{IN} = 2.7 V, V_{OUT} = 3.3 V I_{OUT} = 100 mA to 1-A sweep

図 8-13. Load Sweep at 2.7-V Input Voltage



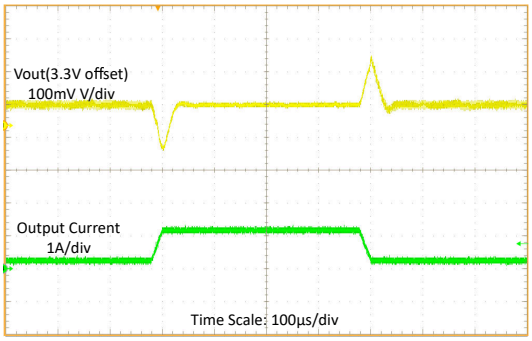
V_{IN} = 3.6 V, V_{OUT} = 3.3 V I_{OUT} = 100 mA to 1 A with 20-µs slew rate

図 8-14. Load Transient at 3.6-V Input Voltage



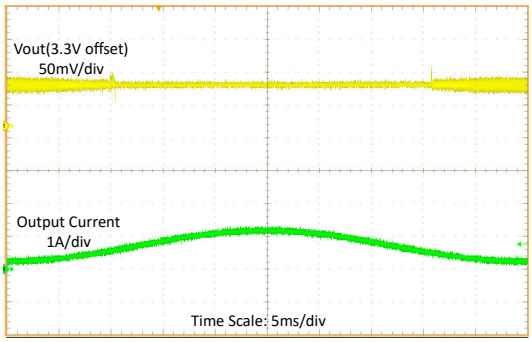
V_{IN} = 3.6 V, V_{OUT} = 3.3 V I_{OUT} = 100 mA to 1-A sweep

図 8-15. Load Sweep at 3.6-V Input Voltage



V_{IN} = 4.3 V, V_{OUT} = 3.3 V I_{OUT} = 100 mA to 1 A with 20-µs slew rate

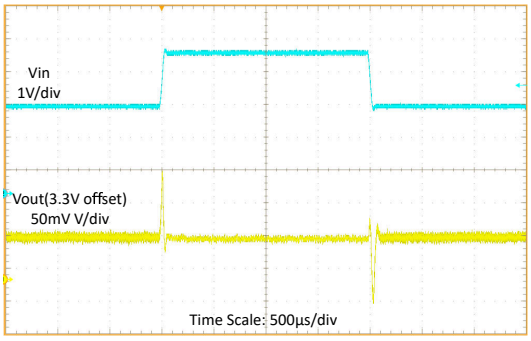
図 8-16. Load Transient at 4.3-V Input Voltage



V_{IN} = 4.3 V, V_{OUT} = 3.3 V I_{OUT} = 100 mA to 1-A sweep

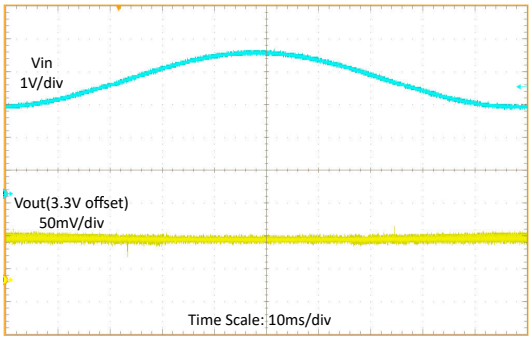
図 8-17. Load Sweep at 4.3-V Input Voltage

8.2.3 Application Curves (continued)



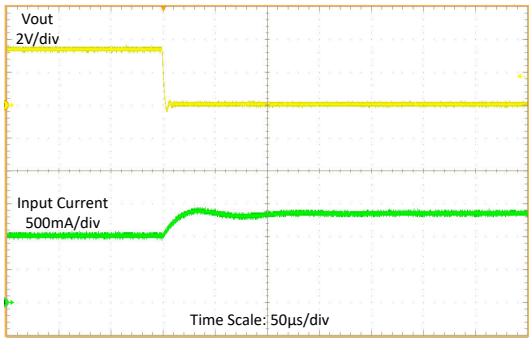
V_{IN} = 2.7 V to 4.3 V with 20-µs slew rate, V_{OUT} = 3.3 V I_{OUT} = 1 A

図 8-18. Line Transient at 1-A Load Current



V_{IN} = 2.7-V to 4.3-V sweep, V_{OUT} = 3.3 V I_{OUT} = 1 A

図 8-19. Line Sweep at 1-A Load Current



V_{IN} = 3.6 V, V_{OUT} = 3.3 V I_{OUT} = 1 A, FPWM

図 8-20. Output Short Protection (Entry)

表 8-4. Components for Application Characteristic Curves for V_{OUT} = 3.3 V

REFERENCE	DESCRIPTION	PART NUMBER	MANUFACTURER(1)
U1	High Power Density 1.5 A Buck-Boost Converter	TPSM83102 or TPSM83103	Texas Instruments
C1	22 µF, 0603, Ceramic Capacitor, ±20%, 6.3 V	GRM187R61A226ME15	Murata
C2	47 µF, 0805, Ceramic Capacitor, ±20%, 6.3 V	GRM219R60J476ME44	Murata

(1) See the セクション 10.1.1.

9 Layout

9.1 Layout Guidelines

The PCB layout is an important step to maintain the high performance of the TPSM83102 and TPSM83103 devices.

- Place input and output capacitors as close as possible to the IC. Traces need to be kept short. Route wide and direct traces to the input and output capacitors results in low trace resistance and low parasitic inductance.

9.2 Layout Example

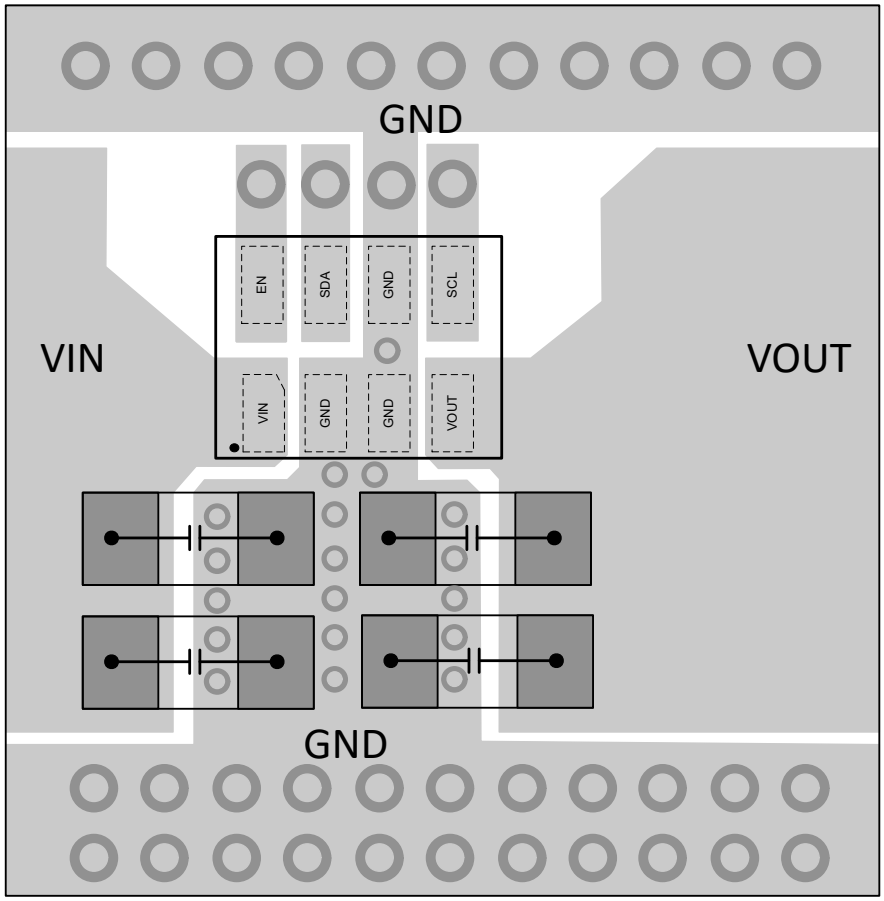


図 9-1. Layout Example

10 Device and Documentation Support

10.1 Device Support

10.1.1 サード・パーティ製品に関する免責事項

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10.1.2 Development Support

10.1.2.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the TPSM83102 and TPSM83103 devices with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint or cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you can:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

10.4 Trademarks

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10.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.6 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

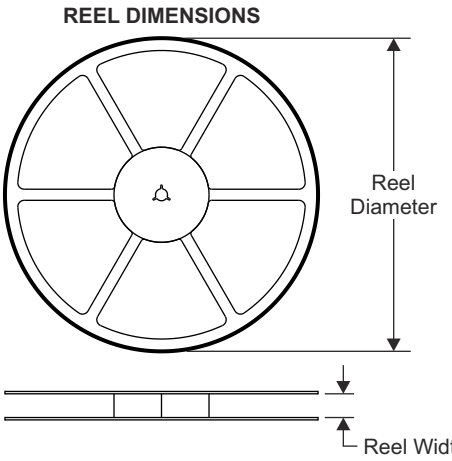
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

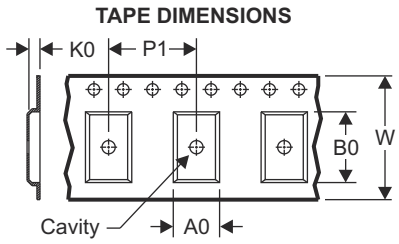
DATE	REVISION	NOTES
August 2024	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

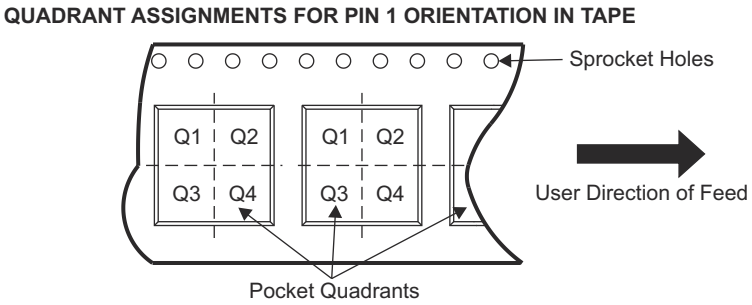
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Tape and Reel Information



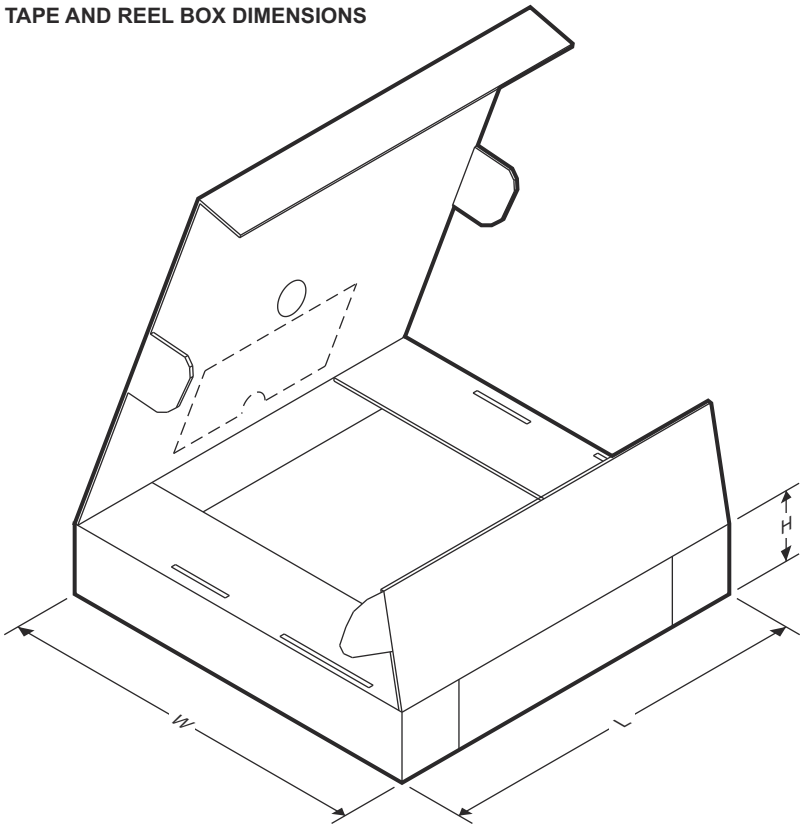


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



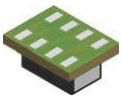
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM83103SIUR	µSiP	SIU	8	3000	330	12.4	2.3	2.9	1.35	8	12	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM83103SIUR	µSiP	SIU	8	3000	383	353	58

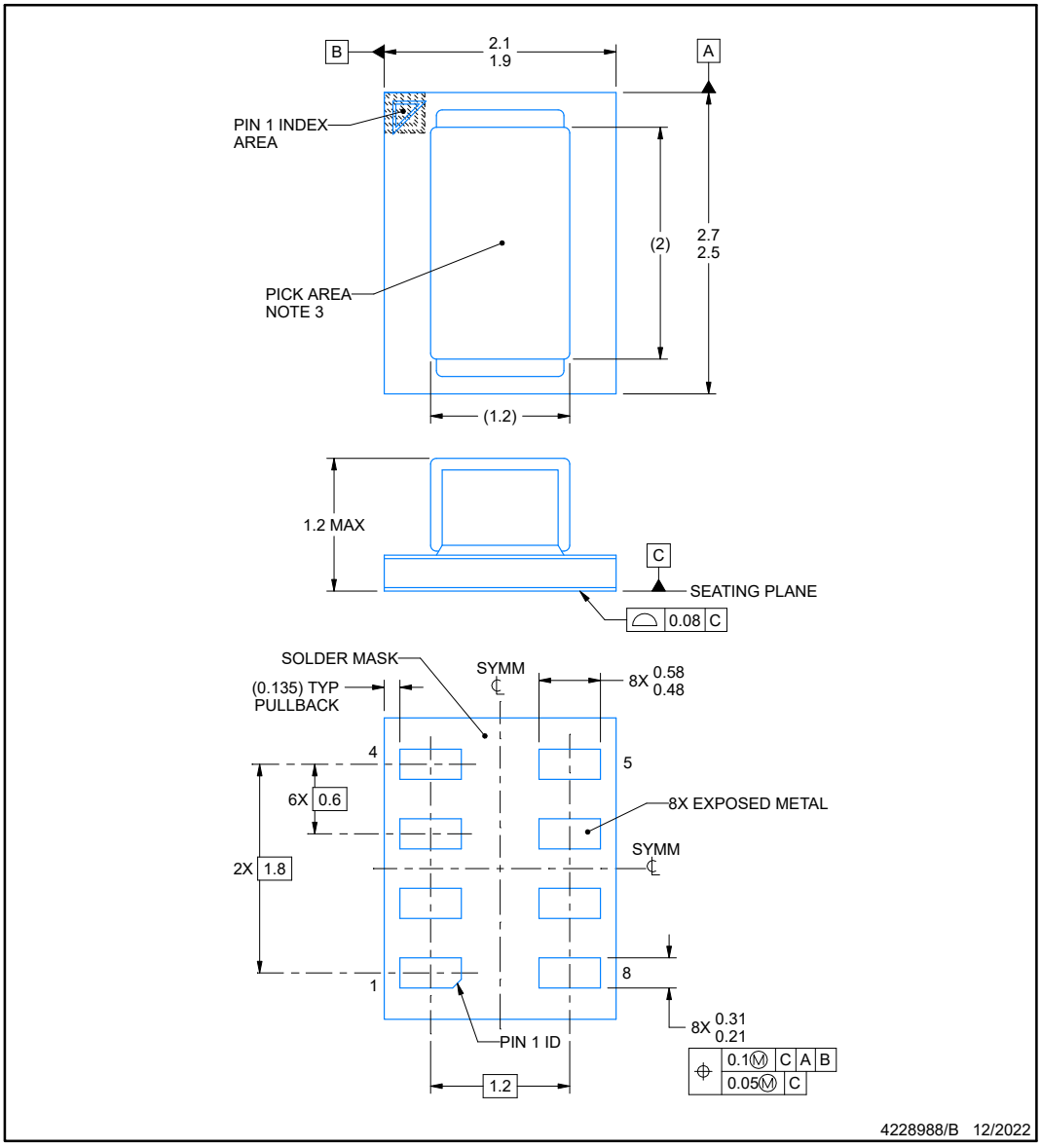
12.2 Mechanical Data



PACKAGE OUTLINE

SIU0008A — **MicroSiP™ - 1.2 mm max height**

MICRO SYSTEM IN PACKAGE



MicroSiP is a trademark of Texas Instruments

NOTES:

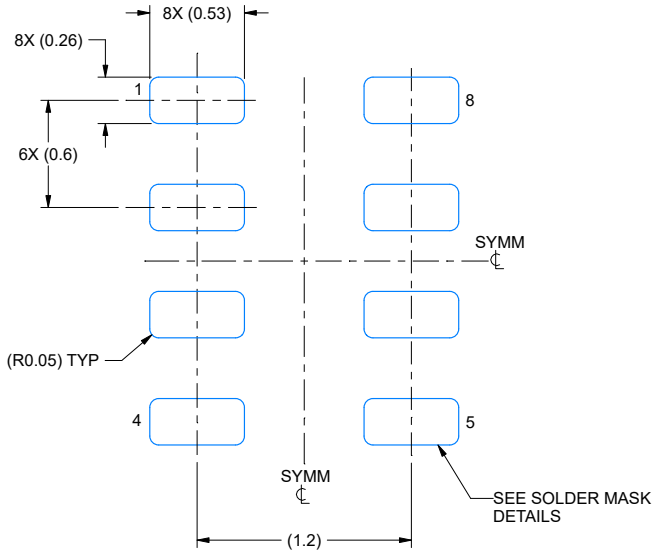
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pick and place nozzle ∅ 0.33 mm or smaller recommended.

www.ti.com

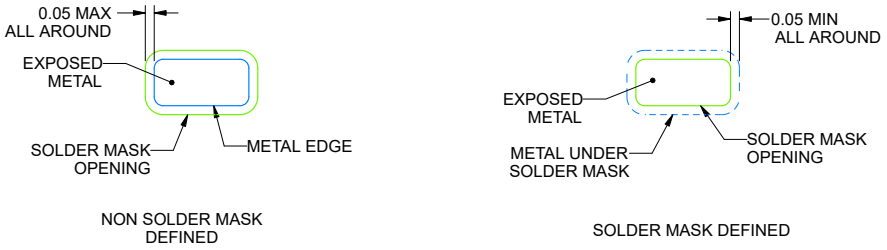
EXAMPLE BOARD LAYOUT

SIU0008A — **MicroSiP™ - 1.2 mm max height**

MICRO SYSTEM IN PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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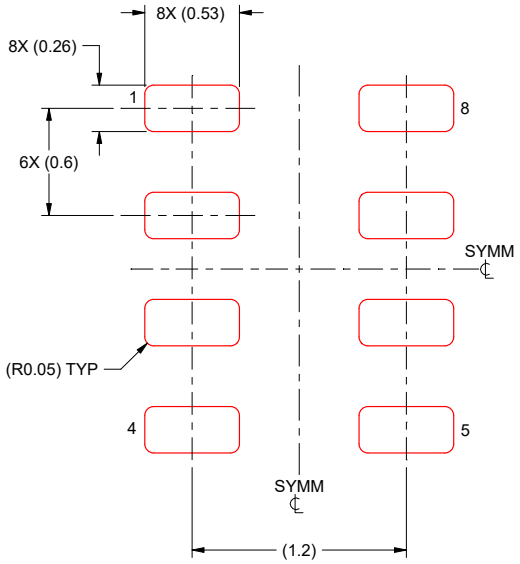
NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

SIU0008A — **MicroSiP™ - 1.2 mm max height**

MICRO SYSTEM IN PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPSM831021SIUR	ACTIVE	uSiP	SIU	8	3000	RoHS & Green	ENEPIG	Level-2-260C-1 YEAR	-40 to 125	3I8P HYBM831021	Samples
TPSM831022SIUR	ACTIVE	uSiP	SIU	8	3000	RoHS & Green	ENEPIG	Level-2-260C-1 YEAR	-40 to 125	3I9P HYBM831022	Samples
TPSM831023SIUR	ACTIVE	uSiP	SIU	8	3000	RoHS & Green	ENEPIG	Level-2-260C-1 YEAR	-40 to 125	3IAP HYBM831023	Samples
TPSM83102SIUR	ACTIVE	uSiP	SIU	8	3000	RoHS & Green	ENEPIG	Level-2-260C-1 YEAR	-40 to 125	3EGL HYBM83102	Samples
TPSM83103SIUR	ACTIVE	uSiP	SIU	8	3000	RoHS & Green	ENEPIG	Level-2-260C-1 YEAR	-40 to 125	3EHL HYBM83103	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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