TRSF3243E ±15kV IEC ESD 保護機能搭載、3V～5.5V マルチチャネル RS-232 互換ライン・ドライバ / レシーバ

1 特長

- RS-232 バス・ピンの ESD 保護機能
  - ±15kV 人体モデル (HBM)
  - ±8kV IEC 61000-4-2、接触放電
  - ±15kV IEC 61000-4-2、エアギャップ放電
- 3V～5.5V の 単一 V_{CC} 電源で動作
- 常時アクティブの非反転レシーバ出力 (ROUT2B)
- 小さいスタンバイ電流:1µA (標準値)
- 外付けコンデンサ:4 × 0.1µF
- 3.3V 電源で 5V ロジック入力を許容
- シリアルマウス駆動可能
- 最大 1Mbit/s で動作
- 有効な RS-232 信号が検出されない場合、自動パワー・ダウン機能によりドライバ出力をディセーブル
- 省スペースの RHB (5mm x 5mm QFN-32) パッケージで供給

2 アプリケーション

- 産業用 PC
- 有線ネットワーク
- データ・センターおよびネットワーク機器
- ノート PC
- ハンドヘルド機器

3 概要

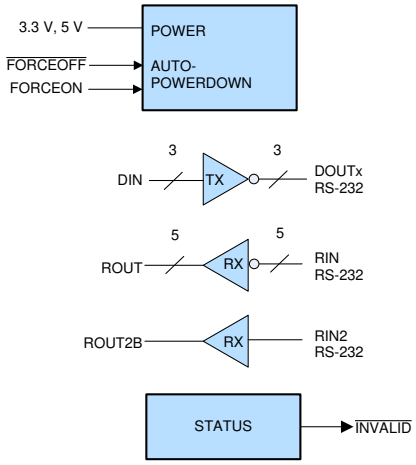
TRSF3243E は、3 つのライン・ドライバ、5 つのライン・レシーバ、デュアル・チャージ・ポンプ回路で構成されており、シリアル・ポート接続ピンには、±15kV ESD (HBM および IEC61000-4-2、気中放電) および ±8kV ESD (IEC61000-4-2、接触放電) の保護を備えています。このデバイスは、非同期通信コントローラとシリアルポート・コネクタの間の電気的インターフェイスとして機能します。チャージ・ポンプと 4 つの小さな外付けコンデンサにより、3V～5.5V の単一電源で動作できます。さらに、このデバイスには常時アクティブな非反転出力 (ROUT2B) があり、リング・インジケータを使用するアプリケーションが、デバイスの電源がオフのときにもデータを送信できるようになっています。このデバイスは、最大 1Mbit/s のデータ信号速度、18V/µs～150V/µs の高い出力スルーレートで動作します。

シリアル・ポートが使われていない際のパワー・マネージメントを柔軟に制御できます。FORCEON が LOW かつ $\overline{\text{FORCEOFF}}$ が HIGH の場合、自動パワー・ダウン機能が動作します。この動作モード中、有効な RS-232 信号を検出しない場合、ドライバ出力はディセーブルになります。$\overline{\text{FORCEOFF}}$ が LOW になっている場合、ドライバおよびレシーバ (ROUT2B を除く) が遮断され、供給電流は 1µA に減少します。シリアル・ポートを切り離した場合、またはペリフェラル・ドライバをオフにした場合、自動パワー・ダウン状態になります。

パッケージ情報

部品番号	パッケージ(1)	本体サイズ (公称)
TRSF3243E	VQFN (RHB) (32)	5.00mm × 5.00mm
	TSSOP (PW) (28)	9.70mm × 4.40mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (November 2021) to Revision A (September 2022)	Page
• 「製品情報」表の TSSOP (PW) から製品プレビューの注を削除	1

5 Pin Configuration and Functions

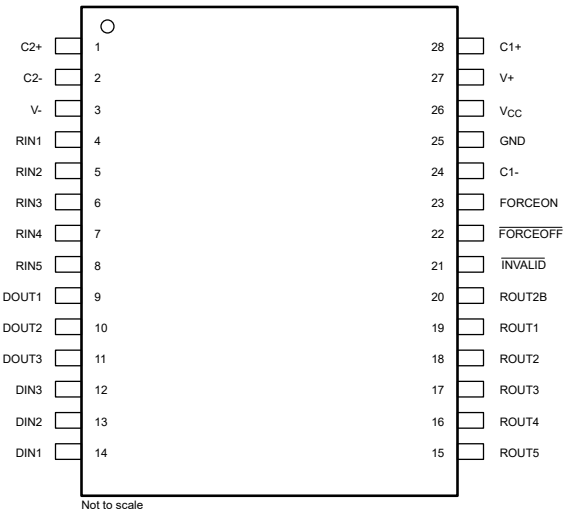


図 5-1. PW (TSSOP) Packages, 28 Pin, Top View

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	C2+	—	Positive terminal of the charge-pump capacitor
2	C2-	—	Negative terminal of the charge-pump capacitor
3	V-		Negative charge-pump rail
4	RIN1	I	RS-232 receiver inputs
5	RIN2		
6	RIN3		
7	RIN4		
8	RIN5		
9	DOUT1	O	RS-232 driver outputs
10	DOUT2		
11	DOUT3		
12	DIN3	I	Driver logic inputs
13	DIN2		
14	DIN1		
15	ROUT5	O	Receiver logic outputs
16	ROUT4		
17	ROUT3		
18	ROUT2		
19	ROUT1		
20	ROUT2B	—	Always-active non-inverting receiver logic output
21	$\overline{\text{INVALID}}$	O	Invalid Output Pin
22	$\overline{\text{FORCEOFF}}$	I	Auto Powerdown Control input (Refer to Truth Table)
23	FORCEON	I	Auto Powerdown Control input (Refer to Truth Table)
24	C1-	—	Negative terminal of the charge-pump capacitor
25	GND	—	Ground
26	V_{CC}	—	3-V to 5.5-V supply voltage
27	V+	—	Positive charge-pump rail
28	C1+	—	Positive terminal of the charge-pump capacitor

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

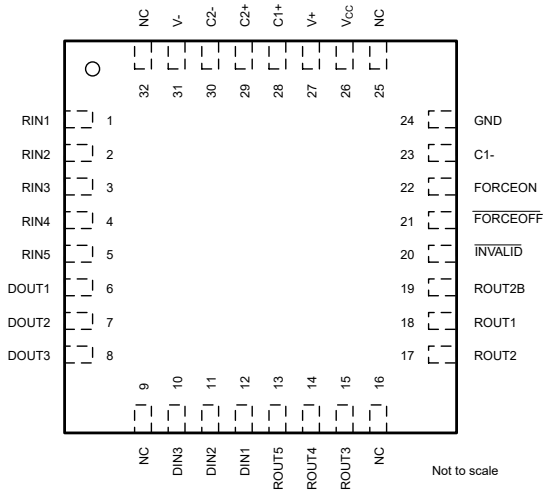


図 5-2. RHB (VQFN) Package, 32 Pin, Top View

表 5-2. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	RIN1	I	RS-232 receiver inputs
2	RIN2		
3	RIN3		
4	RIN4		
5	RIN5		
6	DOUT1	O	RS-232 driver outputs
7	DOUT2		
8	DOUT3		
9	NC	—	No internal connection
10	DIN3	I	Driver logic inputs
11	DIN2		
12	DIN1		
13	ROUT5	O	Receiver logic outputs
14	ROUT4		
15	ROUT3		
16	NC	—	No internal connection
17	ROUT2	O	Receiver outputs
18	ROUT1		
19	ROUT2B	O	Always-active non-inverting receiver output
20	$\overline{\text{INVALID}}$	O	Invalid Output Pin
21	$\overline{\text{FORCEOFF}}$	I	Auto Powerdown Control input (Refer to Truth Table)
22	FORCEON	I	Auto Powerdown Control input (Refer to Truth Table)
23	C1-	—	Negative terminal of the charge-pump capacitor
24	GND	—	Ground
25	NC	—	No internal connection
26	V_{CC}	—	3-V to 5.5-V supply voltage
27	V+	—	Positive charge-pump rail
28	C1+	—	Positive terminal of the charge-pump capacitor
29	C2+	—	
30	C2-	—	Negative terminal of the charge-pump capacitor
31	V-	—	Negative charge-pump rail
32	NC	—	No internal connection

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		–0.3	6	V
V+	Positive-output supply voltage range(2)		–0.3	7	V
V–	Negative-output supply voltage range(2)		0.3	–7	V
V+ – V–	Supply voltage difference(2)			13	V
V_I	Input voltage range	Driver ($\overline{\text{FORCEOFF}}$, FORCEON)	–0.3	6	V
		Receiver	–25	25	
V_O	Output voltage range	Driver	–13.2	13.2	V
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to network GND.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except RIN1, RIN2, RIN3, RIN4, RIN5, DOUT1, DOUT2 and DOUT3 pins	±3000	V
			RIN1, RIN2, RIN3, RIN4, RIN5, DOUT1, DOUT2 and DOUT3 pins to GND	±15000	
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings - IEC Specifications

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge (1)	RIN1, RIN2, RIN3, RIN4, RIN5, DOUT1, DOUT2 and DOUT3 pins	±8,000	V
		IEC 61000-4-2 Air-gap Discharge (1)		±15,000	

(1) A minimum of 1-µF capacitor between V_{CC} and GND is required to meet the specified IEC 61000-4-2 rating.

6.4 Recommended Operating Conditions

see (1)

				MIN	NOM	MAX	UNIT
	Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
			V_{CC} = 5 V	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON	V_{CC} = 3.3 V	2			V
			V_{CC} = 5 V	2.4			
V_{IL}	Driver and control low-level input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON				0.8	V
V_I	Driver and control input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON		0		5.5	V
V_I	Receiver input voltage			–25		25	V
T_A	Operating free-air temperature			–40		85	°C

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

6.5 Thermal Information

THERMAL METRIC(1)		TRSF3243E		UNIT
		VQFN (RHB)	TSSOP (PW)	
		32 PINS	28 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.1	70.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.9	21.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.6	29.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.6	28.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.1	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS(2)	MIN	TYP(1)	MAX	UNIT
I_I	Input leakage current	$\overline{\text{FORCEOFF}}$, FORCEON			±0.01	±1	µA
I_{CC}	Supply current	Auto-powerdown disabled	No load, $\overline{\text{FORCEOFF}}$ and FORCEON = V_{CC}		0.3	1.2	mA
		Powered off	No load, $\overline{\text{FORCEOFF}}$ = GND		1	10	µA
		Auto-powerdown enabled	No load, $\overline{\text{FORCEOFF}}$ = V_{CC}, FORCEON = GND, All RIN are open or grounded, All DIN are grounded		1	10	

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

6.7 Electrical Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS(3)			MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	All DOUT at R_L = 3 kΩ to GND			5	5.4		V
V_{OL}	Low-level output voltage	All DOUT at R_L = 3 kΩ to GND				–5.4	-5	V
V_O	Output voltage (mouse driveability)	DIN1 = DIN2 = GND, DIN3 = V_{CC}, 3-kΩ to GND at DOUT3, DOUT1 = DOUT2 = 2.5 mA			±5			V
I_{IH}	High-level input current	$V_I = V_{CC}$				±0.01	±1	µA
I_{IL}	Low-level input current	V_I = GND				±0.01	±1	µA
I_{OS}	Short-circuit output current(2)	V_{CC} = 3.6 V,	V_O = 0 V			±35	±60	mA
		V_{CC} = 5.5 V,	V_O = 0 V					
r_o	Output resistance	V_{CC}, V+, and V– = 0 V,	V_O = ±2 V		300	10M		Ω
I_{off}	Output leakage current	$\overline{FORCEOFF}$ = GND	V_O = ±12 V,	V_{CC} = 3 V to 3.6 V			±25	µA
			V_O = ±10 V,	V_{CC} = 4.5 V to 5.5 V			±25	

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.
(3) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

6.8 Switching Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS(3)			MIN	TYP(1)	MAX	UNIT
	Maximum data rate (see 図 7-1)	R_L = 3 kΩ, One DOUT switching	C_L = 1000 pF		250			kbit/s
			C_L = 250 pF,	V_{CC} = 3 V to 4.5 V	1000			
			C_L = 1000 pF,	V_{CC} = 4.5 V to 5.5 V	1000			
$t_{sk(p)}$	Pulse skew(2)	C_L = 150 pF to 2500 pF,	R_L = 3 kΩ to 7 kΩ,	See 図 7-2		25		ns
SR(tr)	Slew rate, transition region (see 図 7-1)	C_L = 150 pF to 1000 pF,	R_L = 3 kΩ to 7 kΩ,	V_{CC} = 3.3 V	18		150	V/µs

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

6.9 Electrical Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS(2)	MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA	V_{CC} – 0.6	V_{CC} – 0.1		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3 V		1.6	2.4	V
		V_{CC} = 5 V		1.9	2.4	
$V_{IT–}$	Negative-going input threshold voltage	V_{CC} = 3.3 V	0.6	1.1		V
		V_{CC} = 5 V	0.8	1.4		
V_{hys}	Input hysteresis ($V_{IT+} – V_{IT–}$)			0.5		V
I_{off}	Output leakage current (except ROUT2B)	$\overline{FORCEOFF}$ = 0 V		±0.05	±10	µA
r_i	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

6.10 Switching Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS(3)	TYP(1)	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF, See 図 7-3	150	ns
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 150 pF, See 図 7-3	150	ns
t_{en}	Output enable time	C_L = 150 pF, R_L = 3 kΩ, See 図 7-4	200	ns
t_{dis}	Output disable time	C_L = 150 pF, R_L = 3 kΩ, See 図 7-4	200	ns
$t_{sk(p)}$	Pulse skew(2)	See 図 7-3	50	ns

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

6.11 Electrical Characteristics: Auto-Powerdown

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 図 7-5)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{T+(valid)}$	Receiver input threshold for $\overline{\text{INVALID}}$ high-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}		2.7	V
$V_{T-(valid)}$	Receiver input threshold for $\overline{\text{INVALID}}$ high-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}	–2.7		V
$V_{T(invalid)}$	Receiver input threshold for $\overline{\text{INVALID}}$ low-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}	–0.3	0.3	V
V_{OH}	$\overline{\text{INVALID}}$ high-level output voltage	I_{OH} = –1 mA, FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}	V_{CC} – 0.6		V
V_{OL}	$\overline{\text{INVALID}}$ low-level output voltage	I_{OL} = 1.6 mA, FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}		0.4	V

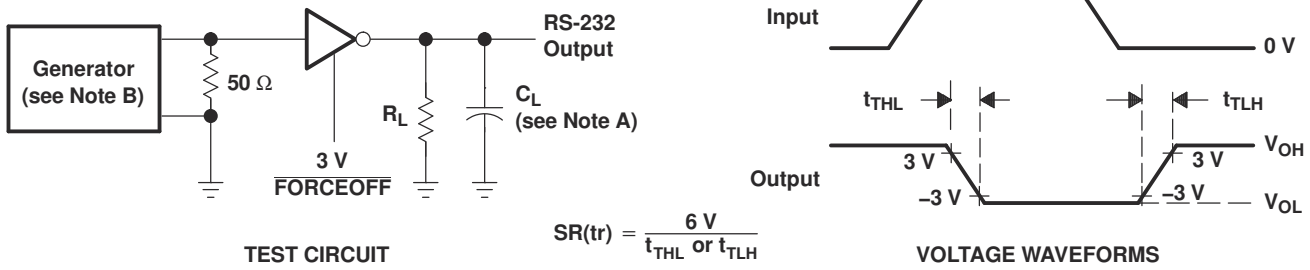
6.12 Switching Characteristics: Auto-Powerdown

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 図 7-5)

PARAMETER		TYP(1)	UNIT
t_{valid}	Propagation delay time, low- to high-level output	1	µs
$t_{invalid}$	Propagation delay time, high- to low-level output	30	µs
t_{en}	Supply enable time	100	µs

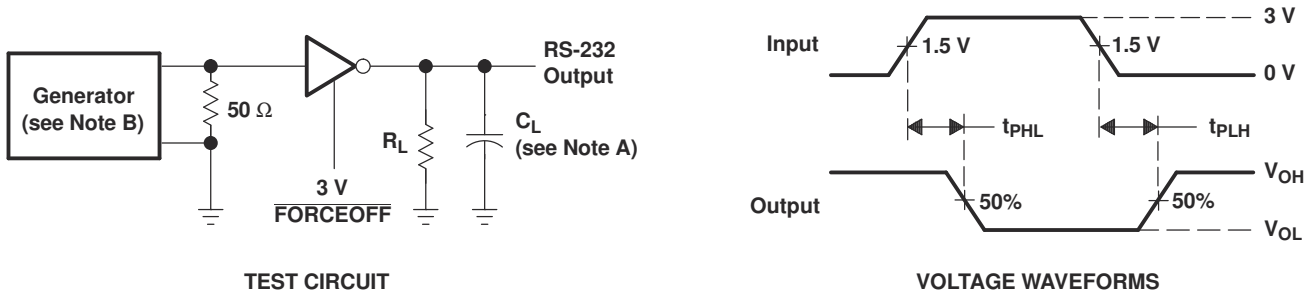
(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

Parameter Measurement Information



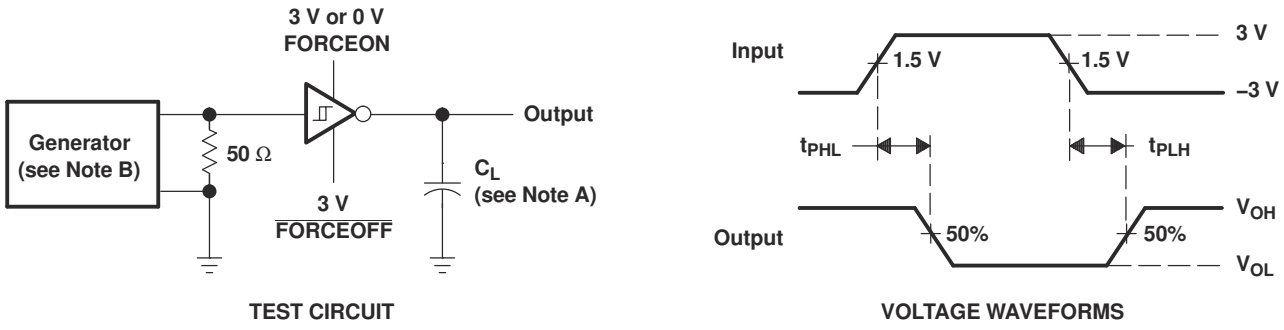
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 1 Mbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

図 7-1. Driver Slew Rate



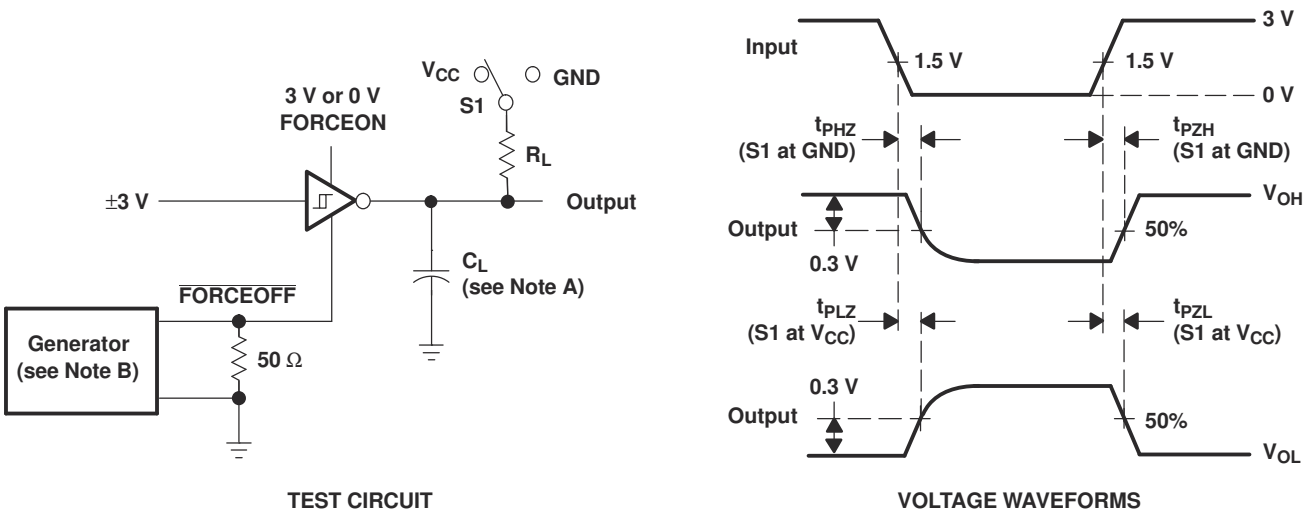
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 1 Mbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

図 7-2. Driver Pulse Skew



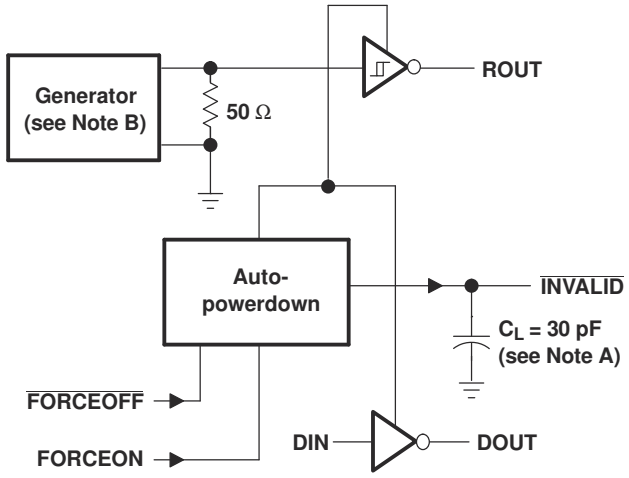
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

図 7-3. Receiver Propagation Delay Times

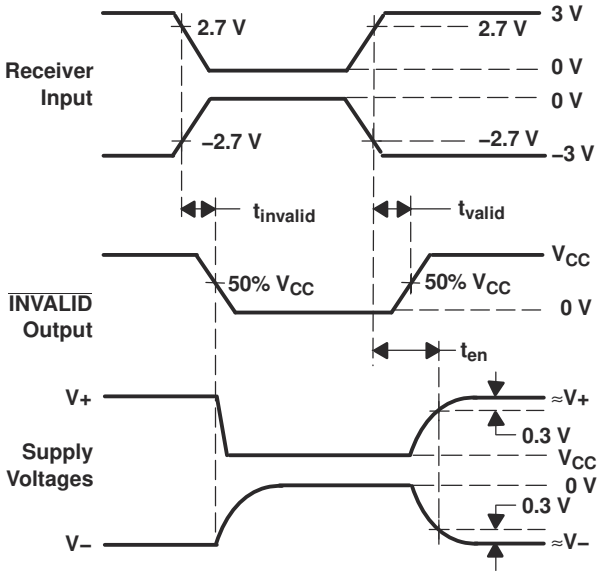


NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.
C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
D. t_{PZL} and t_{PZH} are the same as t_{en}.

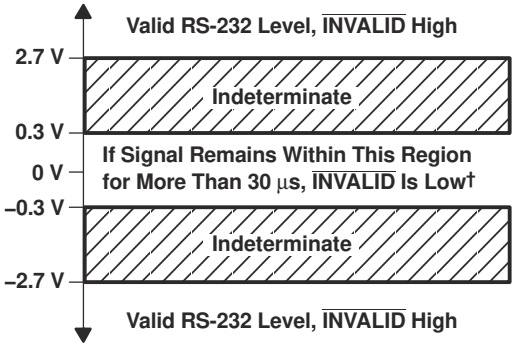
図 7-4. Receiver Enable and Disable Times



TEST CIRCUIT



VOLTAGE WAVEFORMS



† Auto-powerdown disables drivers and reduces supply current to 1 µA.

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 5 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

図 7-5. INVALID Propagation Delay Times and Supply Enabling Time

7 Detailed Description

7.1 Overview

The TRSF3243E device consists of three line drivers, five line receivers, and a dual charge-pump circuit with ±15-kV ESD (HBM and IEC61000-4-2, Air-Gap Discharge) and ±8-kV ESD (IEC61000-4-2, Contact Discharge) protection on serial-port connection pins. The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector.

The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. In addition, the device includes an always-active noninverting output (ROUT2B), which allows applications using the ring indicator to transmit data while the device is powered down. The device operates at data signaling rates up to 500 kbit/s and a maximum of 30-V/µs driver output slew rate.

Functional Block Diagram

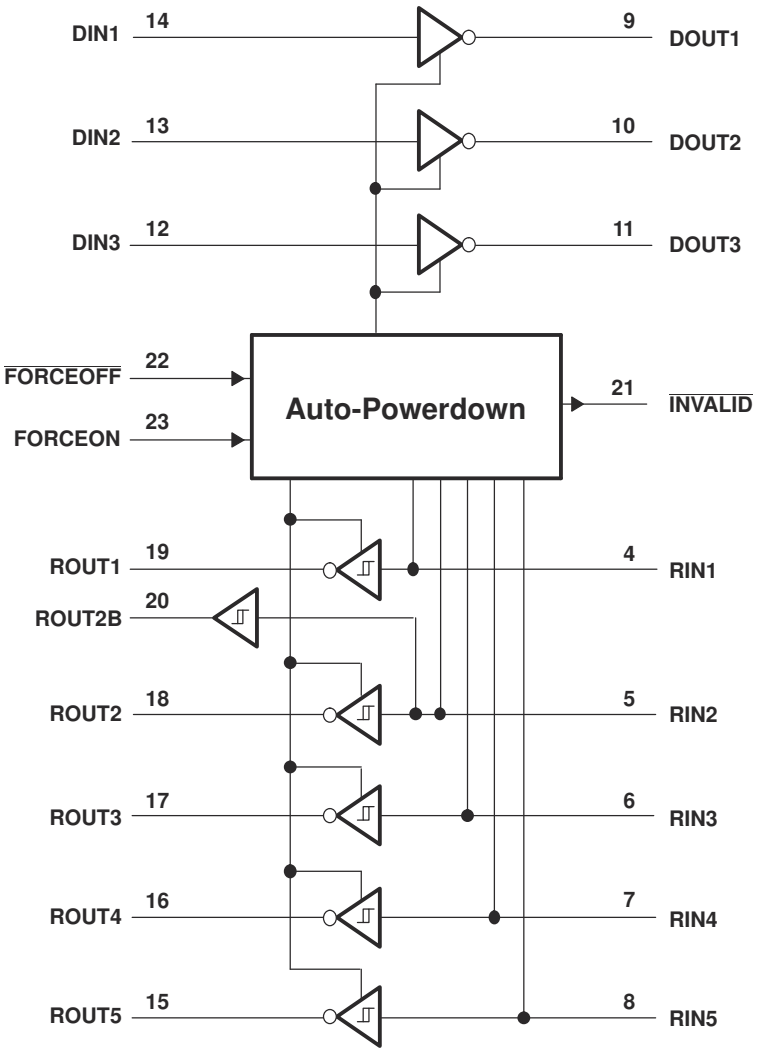


図 7-1. Logic Diagram

7.2 Feature Description

Auto-powerdown can be disabled when FORCEON and $\overline{\text{FORCEOFF}}$ are high and should be done when driving a serial mouse. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to any receiver input. The $\overline{\text{INVALID}}$ output is used to notify the user if an RS-232 signal is present at any receiver input. $\overline{\text{INVALID}}$ is high (valid data) if any receiver input voltage is greater than 2.7 V or less than –2.7 V or has been between –0.3 V and 0.3 V for less than 30 µs. $\overline{\text{INVALID}}$ is low (invalid data) if all receiver input voltages are between –0.3 V and 0.3 V for more than 30 µs. Refer to 図 7-5 for receiver input levels.

7.3 Device Functional Modes

表 7-1 through 表 7-3 show the device functional modes.

表 7-1. Each Driver

INPUTS(1)				OUTPUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	VALID RIN RS-232 LEVEL	DOUT	
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
X	L	H	No	Z	Powered off by auto-powerdown feature

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

表 7-2. Each Receiver

INPUTS(1)			OUTPUT	RECEIVER STATUS
RIN	FORCEON	$\overline{\text{FORCEOFF}}$	ROUT	
X	X	L	Z	Powered off
L	X	H	H	Normal operation with auto-powerdown disabled/enabled
H	X	H	L	
Open	X	H	H	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

表 7-3. ROUT2B And Outputs $\overline{\text{INVALID}}$

INPUTS(1)				OUTPUTS		OUTPUT STATUS
VALID RIN RS-232 LEVEL	RIN2	FORCEON	$\overline{\text{FORCEOFF}}$	$\overline{\text{INVALID}}$	ROUT2B	
Yes	L	X	X	H	L	Always active
Yes	H	X	X	H	H	
Yes	Open	X	X	H	L	
No	Open	X	X	L	L	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

8 Application and Implementation

注

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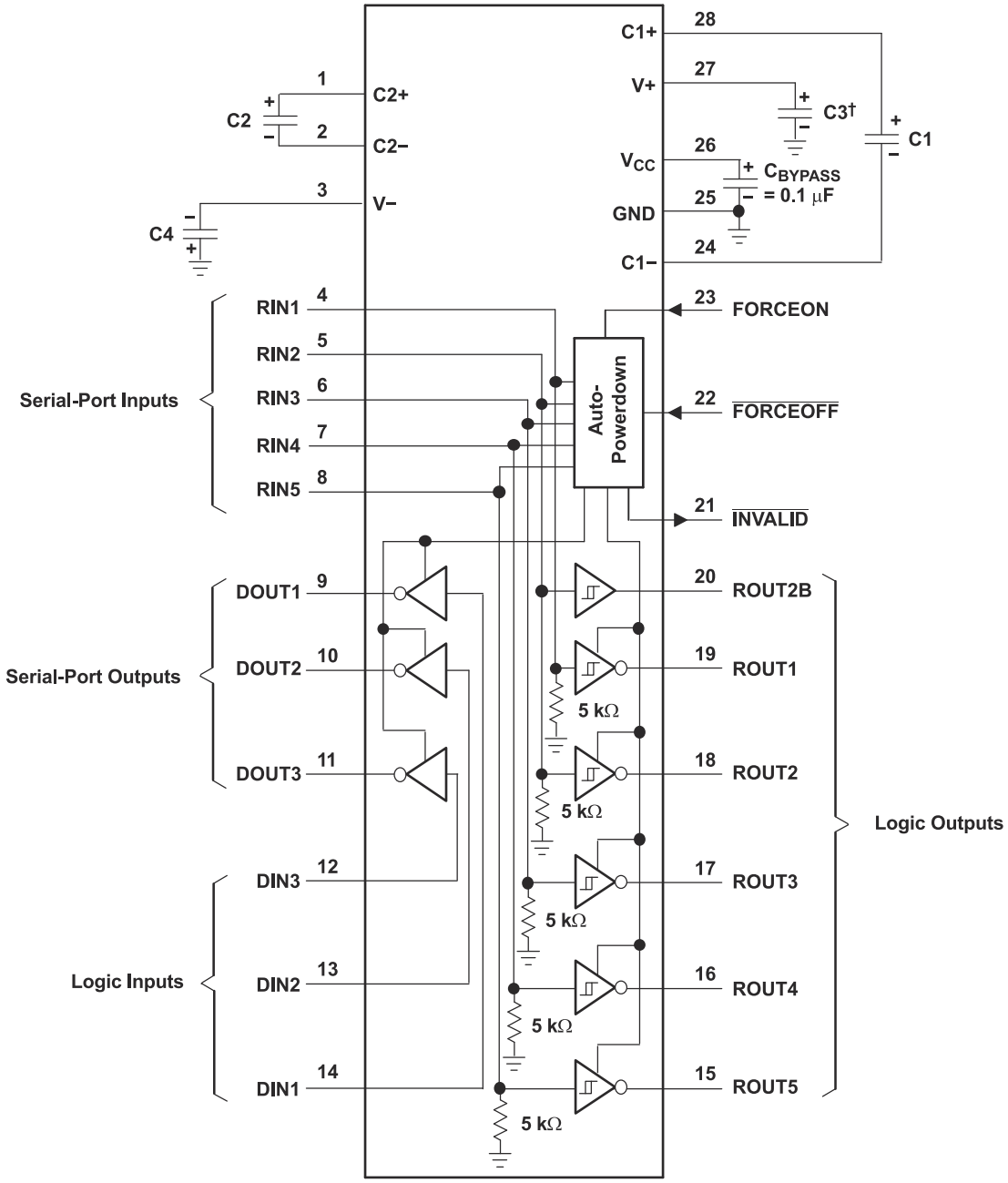
8.1 Application Information

For proper operation, add capacitors as shown in 図 8-1. Pins 12 through 23 connect to UART or general-purpose logic lines. RS-232 lines on Pins 4 through 11 connect to a connector or cable.

8.2 Typical Application

Three driver and five receiver channels are supported for full duplex transmission with hardware flow control. The five 5-kΩ resistors are internal to the device.



A. C3 can be connected to V_{CC} or GND
B. Resistor values shown are nominal.

図 8-1. Typical Operating Circuit and Capacitor Values

8.3 Design Requirements

For this design example, use the values in V_{CC} vs Capacitor Values.

- V_{CC} minimum is 3 V and maximum is 5.5 V.
- Maximum recommended bit rate is 1 Mbps.

表 8-1. V_{CC} vs Capacitor Values

V_{CC}	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 µF	0.1 µF
5 V ± 0.5 V	0.047 µF	0.33 µF
3 V to 5.5 V	0.1 µF	0.47 µF

8.4 Detailed Design Procedure

TRSF3243E has integrated charge-pump that generates positive and negative rails needed for RS-232 signal levels. Main design requirement is that charge-pump capacitor terminals must be connected with recommended capacitor values. Charge-pump rail voltages and device supply pin must be properly bypassed with ceramic capacitors.

9 Power Supply Recommendations

The V_{CC} voltage must be connected to the same power source used for logic device connected to DIN and ROUT pins. V_{CC} must be between 3 V and 5.5 V.

10 Layout

10.1 Layout Guidelines

As shown in Layout Example, charge-pump and supply voltage capacitors must be located very close to device pins. Non-polarized ceramic capacitors are recommended. If polarized tantalum or electrolytic capacitors are used, they should be connected as per Typical Operating Circuit and Capacitor Values.

10.2 Layout Example

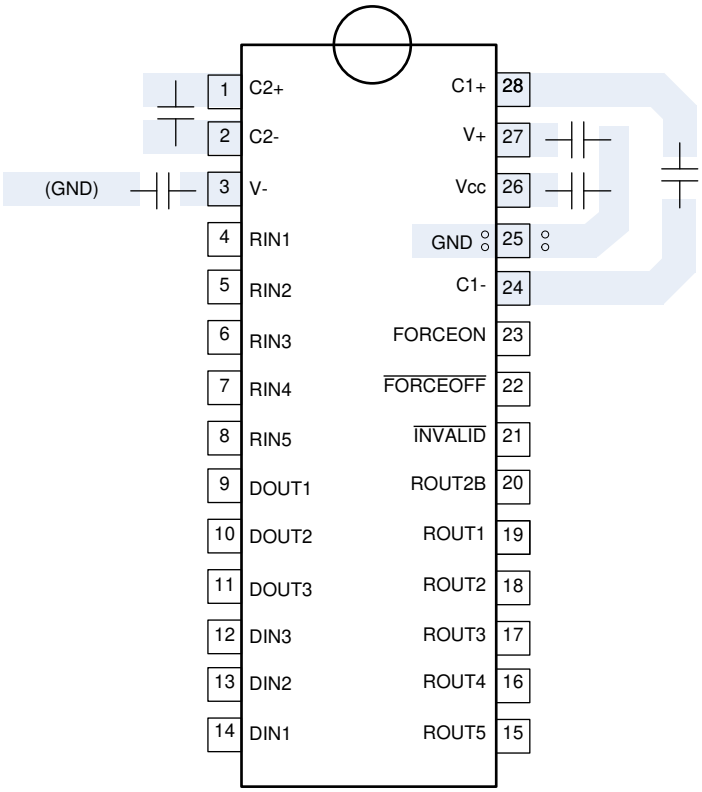


図 10-1. Example Layout

Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 サポート・リソース

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11.3 Trademarks

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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRSF3243EIPWR	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F3243	Samples
TRSF3243EIRHBR	ACTIVE	VQFN	RHB	32	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRSF 3243	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

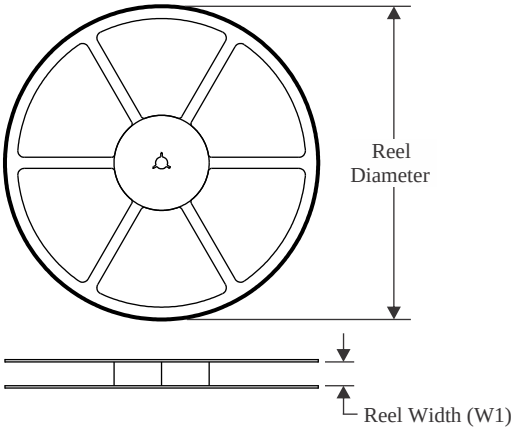
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

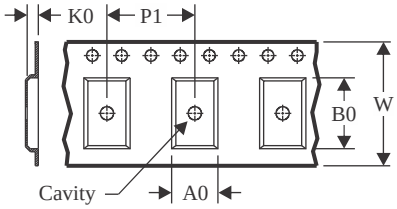
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

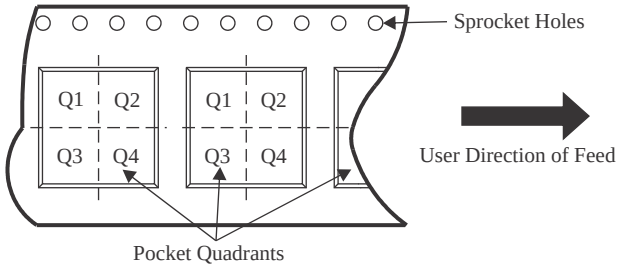


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

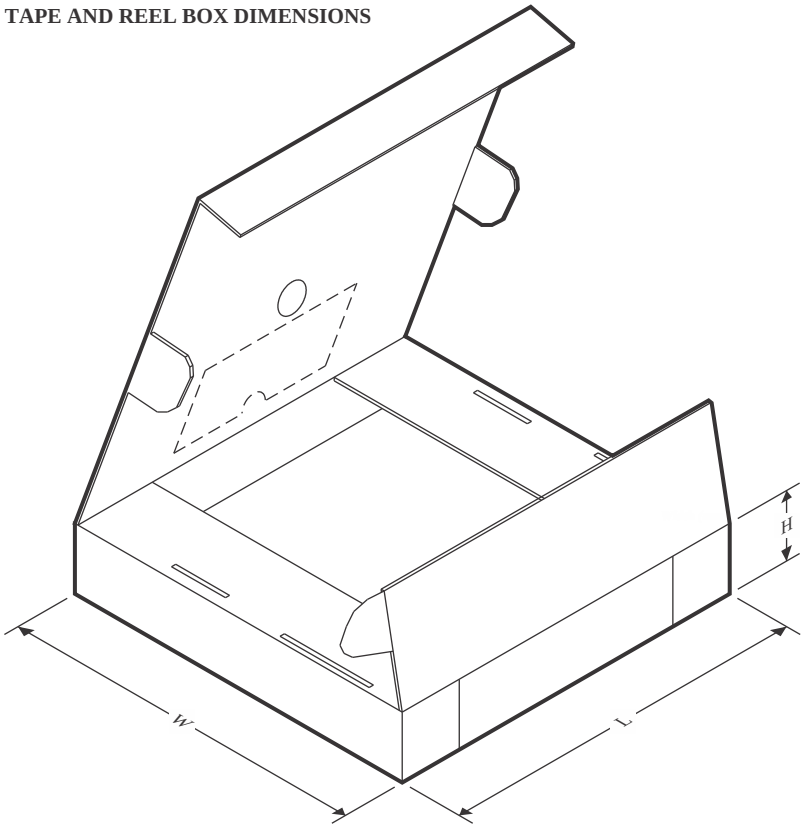
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRSF3243EIPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TRSF3243EIRHBR	VQFN	RHB	32	5000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

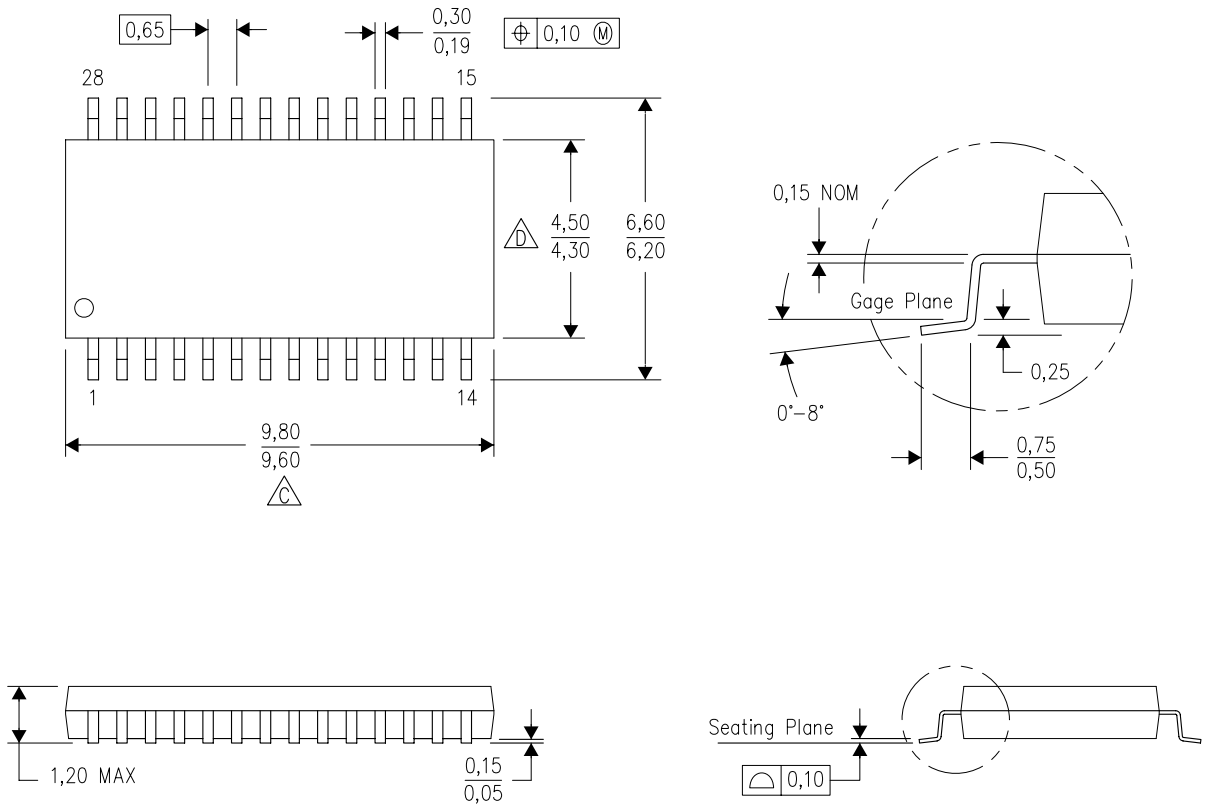
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRSF3243EIPWR	TSSOP	PW	28	2000	356.0	356.0	35.0
TRSF3243EIRHBR	VQFN	RHB	32	5000	367.0	367.0	35.0

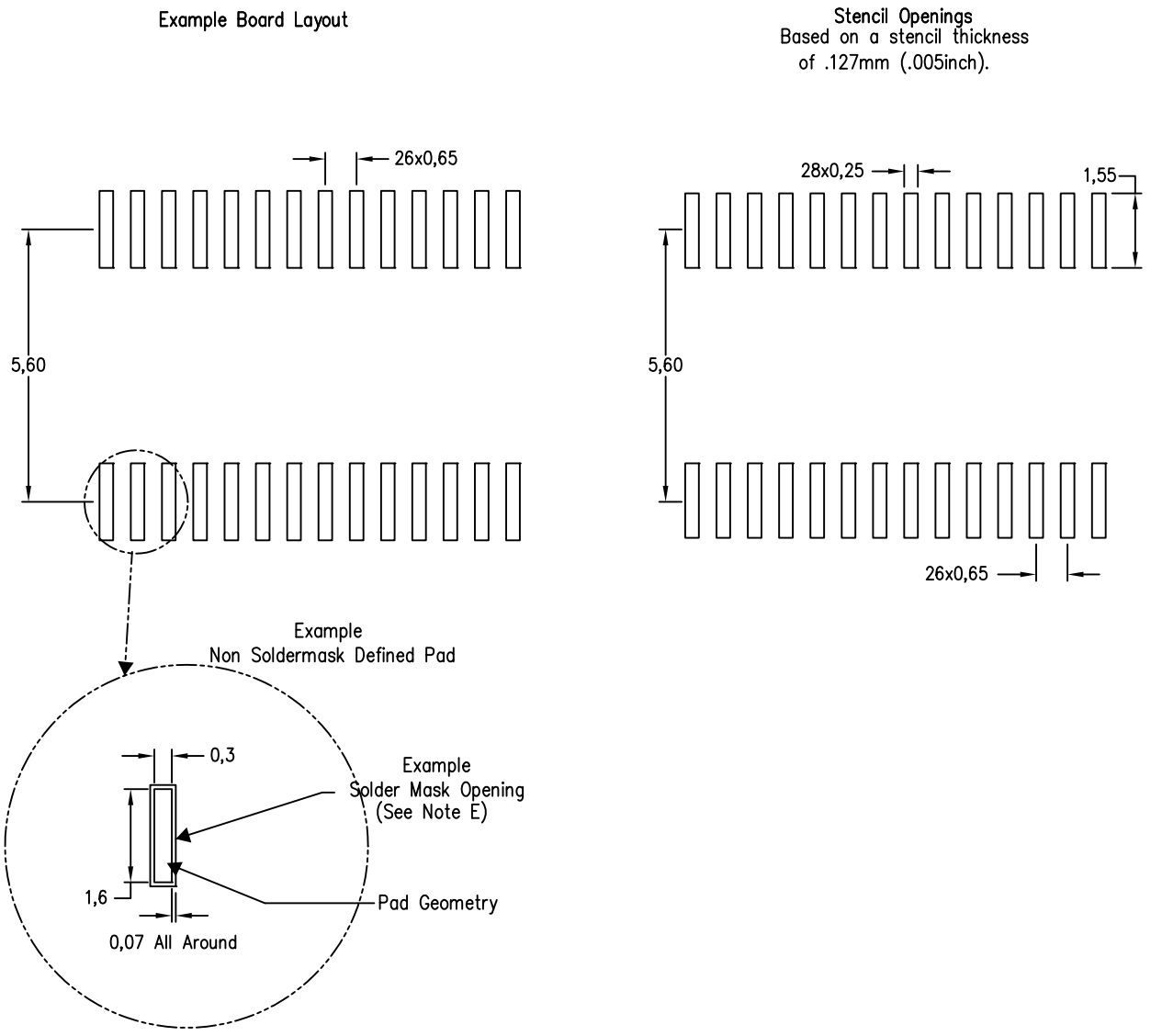
PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

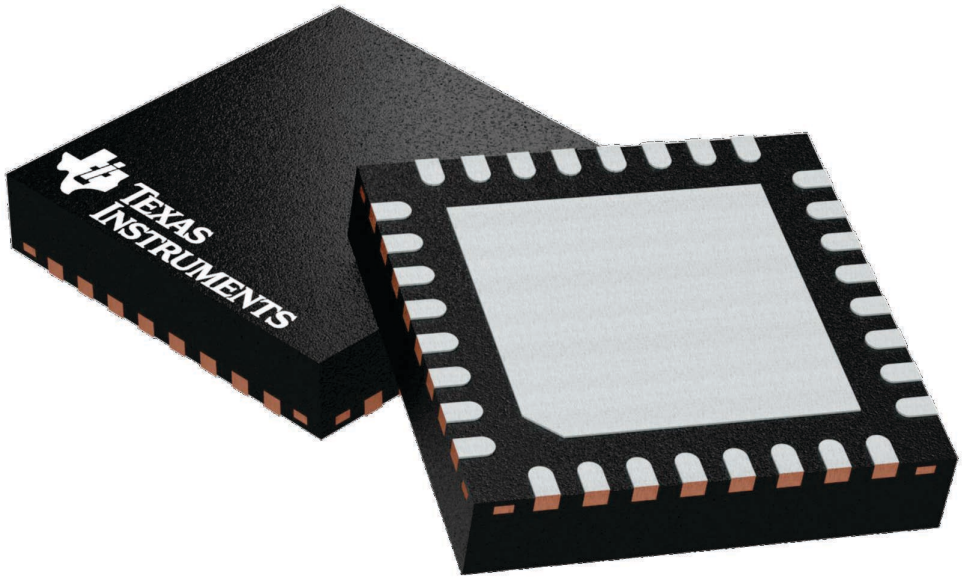
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

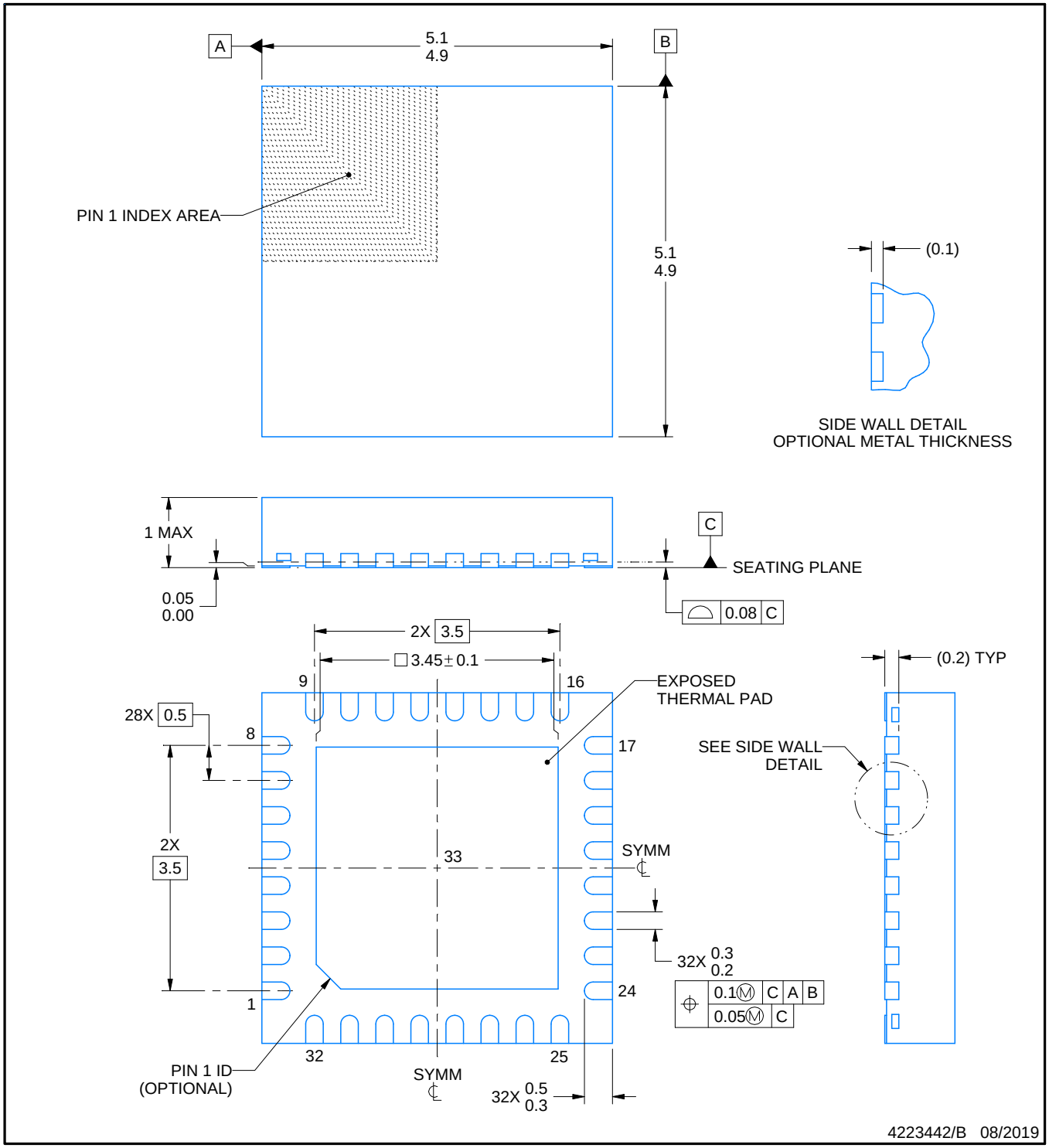
4224745/A

RHB0032E

PACKAGE OUTLINE

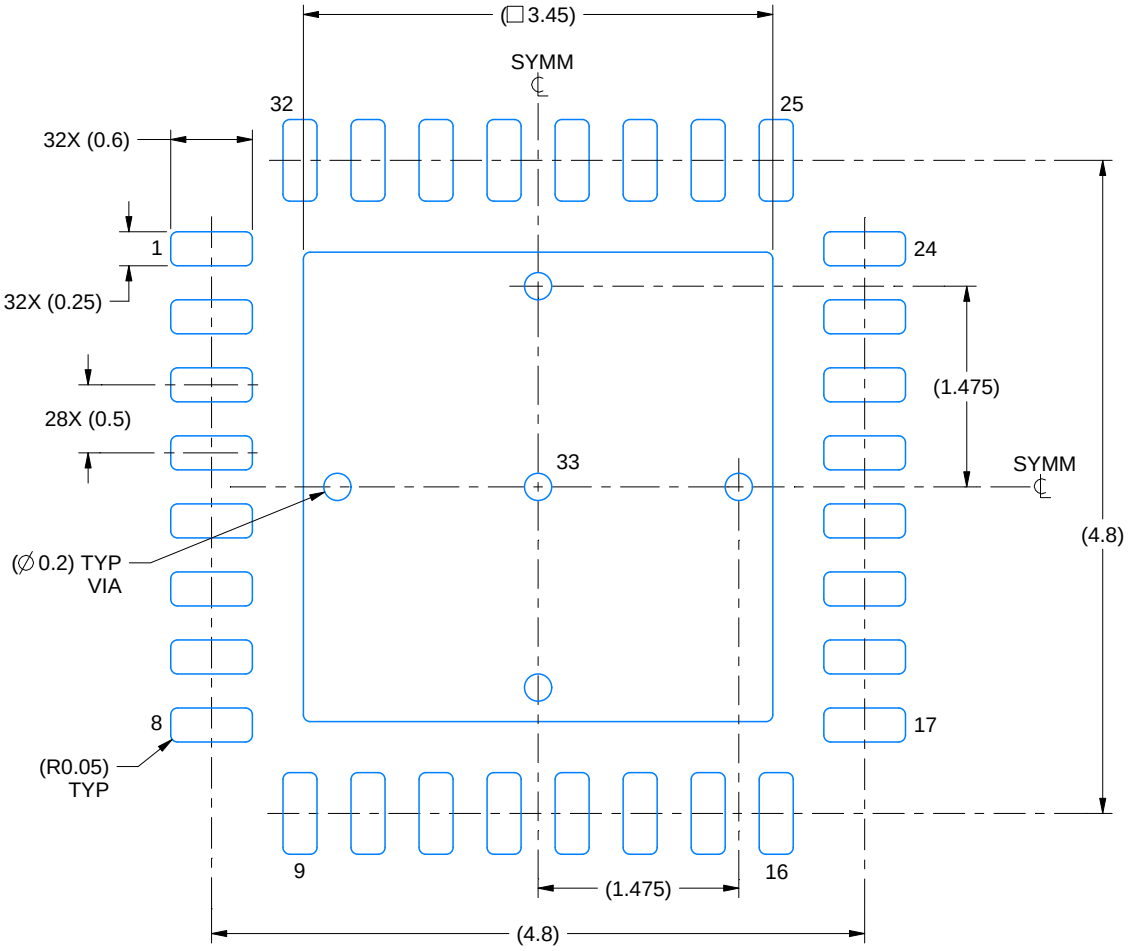
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

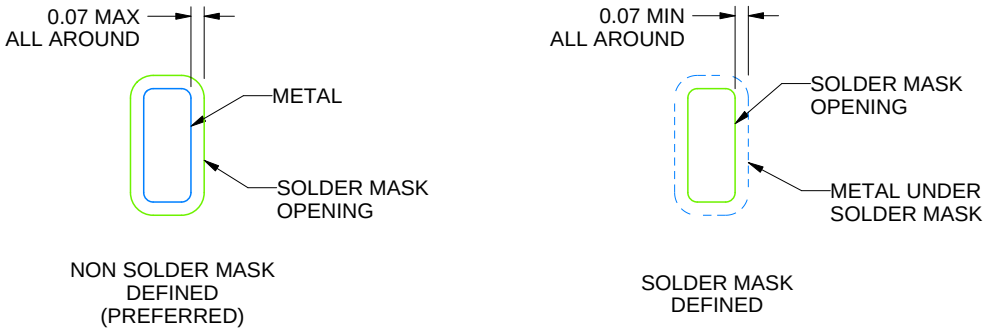


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

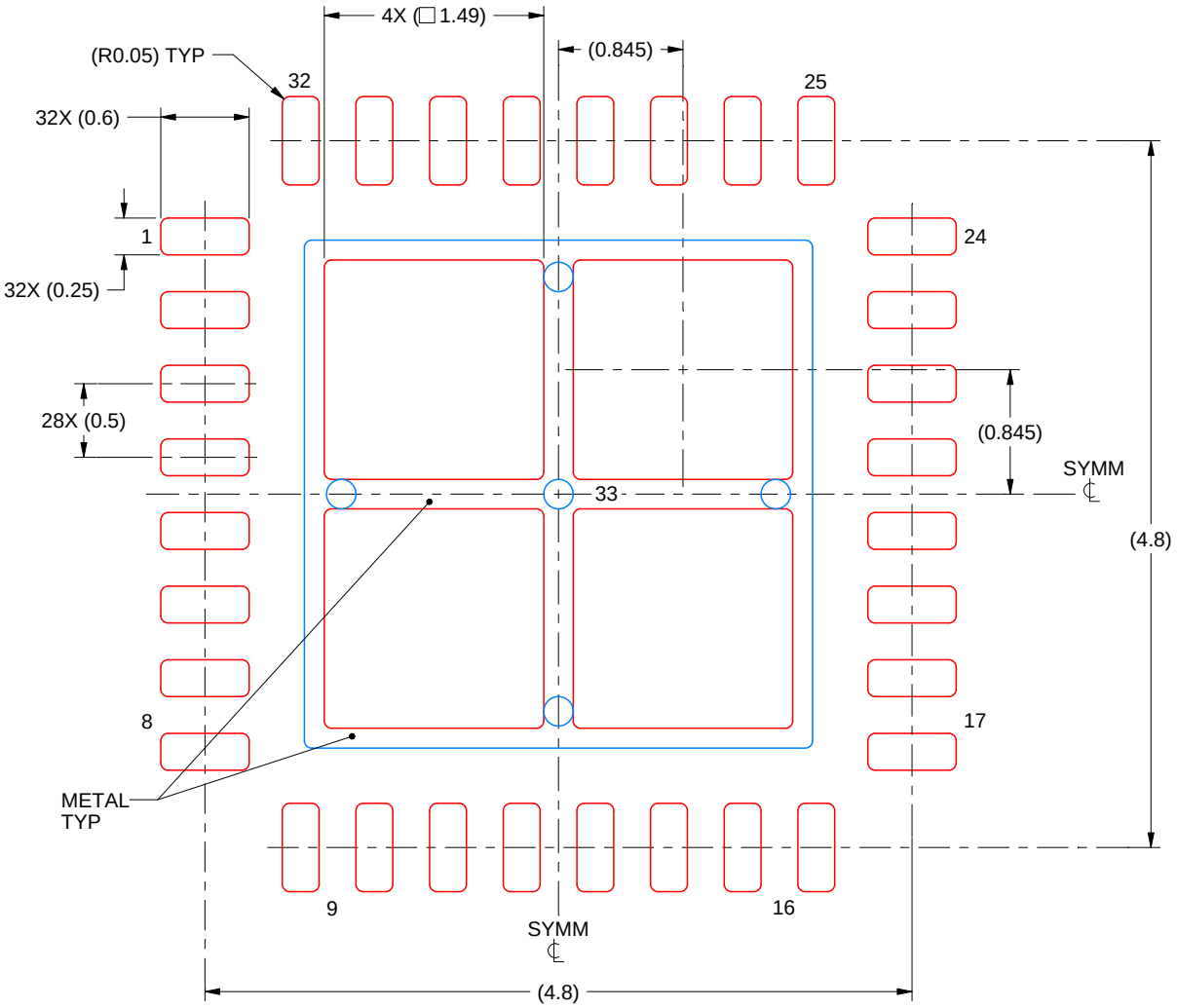


SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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