TEXAS INSTRUMENTS
TS3A24159
JAJSH41H – MARCH 2007 – REVISED AUGUST 2022

TS3A24159 0.3Ω、2 チャネル SPDT 双方向アナログ・スイッチ デュアル・チャネル 2 : 1 マルチプレクサ / デマルチプレクサ

1 特長

- ブレイク・ビフォー・メイクのスイッチングを規定
- 低いオン抵抗 (最大値 0.3Ω)
- 低い電荷注入
- 非常に優れたオン抵抗マッチング
- 低い全高調波歪 (THD)
- 1.65V～3.6V の単一電源で動作
- 制御入力は 1.8V ロジック互換
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 準拠で ESD 性能を試験済み
  - 2000V、人体モデル (A114-B、Class II)
  - 1000V、荷電デバイス・モデル (C101)

2 アプリケーション

- 携帯電話
- パーソナル・デジタル・アシスタント (PDA)
- ポータブル計測装置
- オーディオおよびビデオ信号のルーティング
- 低電圧のデータ収集システム
- 通信用回路
- モデム
- ハードディスク
- コンピュータ周辺機器
- ワイヤレス端末およびペリフェラル

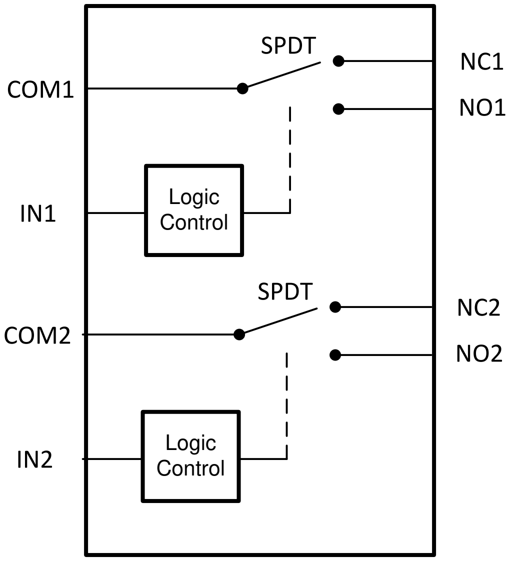
3 概要

TS3A24159 は 2 チャネルの単極双投 (SPDT) 双方向アナログ・スイッチで、1.65V～3.6V で動作するよう設計されています。このデバイスはオン抵抗が低く、オン抵抗マッチングが非常に優れており、Break-Before-Make 機能によってチャネル間の信号転送時に信号が歪むのを防ぎます。このデバイスは全高調波歪み (THD) 特性が非常に優れており、オン抵抗が低く、極めて低消費電力です。これらの特長も含めた多くの特長から、このデバイスは各種の市場、多くの種類のアプリケーションに適しています。

製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
TS3A24159	VSSOP (10)	3.00mm × 3.00mm
	VSON (10)	3.00mm × 3.00mm
	DSBGA (10)	1.86mm × 1.35mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ブロック図

English Data Sheet: SCDS238

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision G (February 2022) to Revision H (August 2022) **Page**

- Changed the maximum V_{CC} from: *3.6 V* to: *4 V* 5

Changes from Revision F (September 2019) to Revision G (February 2022) **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 1
- Updated the part number in the *Detailed Design Procedure* 20

Changes from Revision E (March 2019) to Revision F (September 2019) **Page**

- Changed the YZP package image view From: Top-Through View To: Bottom View 3

Changes from Revision D (July 2015) to Revision E (March 2019) **Page**

- Changed the YZP package image and deleted the *YZP Package, Terminal Assignments* table 3
- Changed Turnon time V_{CC} (Full) value From: 2.3 V to 2.7 V To: 2.7 V to 3.6 V in *Switching Characteristics for a 3-V Supply* 10
- Changed Turnon time V_{CC} (Full) value From: 2.3 V to 2.7 V To: 2.7 V to 3.6 V in *Switching Characteristics for a 2.5-V Supply* 10

Changes from Revision C (February 2008) to Revision D (March 2015) **Page**

- 「*ピン構成および機能*」セクション、「*ESD 定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 1
- JEDEC 規格を満たすように、文書全体にわたって V+ を V_{CC} に変更 1

5 Pin Configuration and Functions

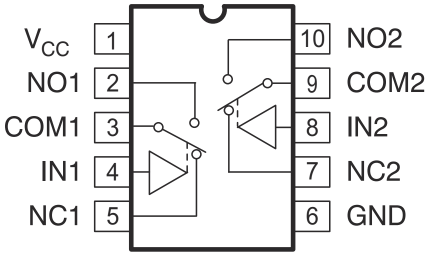


図 5-1. DGS Package, 10-Pin VSSOP (Top View)

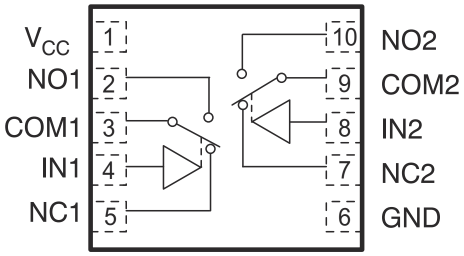
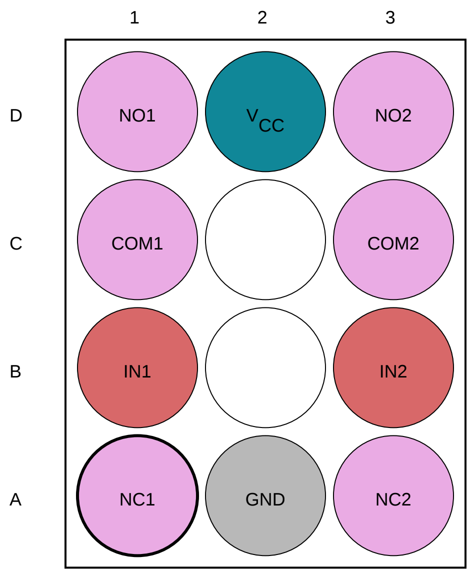


図 5-2. DRC Package, 10-Pin VSON (Top View)

表 5-1. Pin Functions – VSSOP and VSON

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	V_{CC}	—	Power supply
2	NO1	I/O	Normally open signal path
3	COM1	I/O	Common signal path
4	IN1	I	Digital control to connect COM to NO or NC
5	NC1	I/O	Normally closed signal path
6	GND	—	Ground
7	NC2	I/O	Normally closed signal path
8	IN2	I	Digital control to connect COM to NO or NC
9	COM2	I/O	Common signal path
10	NO2	I/O	Normally open signal path

(1) I = input, O = output



Not to scale

図 5-3. YZP Package, 10-Pin DSBGA (Bottom View)

Legend	
Input or Output	Input
Ground	Power

表 5-2. Pin Functions – DSBGA

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
A1	NC1	I/O	Normally closed signal path
A2	GND	—	Ground
A3	NC2	I/O	Normally closed signal path
B1	IN1	I	Digital control to connect COM to NO or NC
B3	IN2	I	Digital control to connect COM to NO or NC
C1	COM1	I/O	Common signal path
C3	COM2	I/O	Common signal path
D1	NO1	I/O	Normally open signal path
D2	V_{CC}	—	Power supply
D3	NO2	I/O	Normally open signal path

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(3)		–0.5	4	V
V_{NC} V_{NO} V_{COM}	Signal voltage(3) (4)		–0.5	V_{CC} + 0.5	V
$I_{I/OK}$	Analog port diode current	V_{NC}, V_{NO}, V_{COM} < 0	–50	50	mA
I_{NC} I_{NO} I_{COM}	ON-state switch current	V_{NC}, V_{NO}, V_{COM} = 0 to V_{CC}	–300	300	mA
	ON-state peak switch current(5)		–500	500	
V_{IN}	Digital input voltage		–0.5	3.6	V
I_{IK}	Digital input clamp current(3)	V_I < 0	–50		mA
I_{CC}	Continuous current through V_{CC}			100	mA
I_{GND}	Continuous current through GND		–100		mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) This value is limited to 5.5 V maximum.
(5) Pulse at 1-ms duration <10% duty cycle.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply Voltage	1.65	3.6	V
V_{NC} V_{NO} V_{COM}	Signal Voltage	0	V_{CC}	V
V_{IN}	Digital Input Voltage	0	V_{CC}	V

6.4 Thermal Information

THERMAL METRIC(1)		TS3A24159			UNIT
		DGS (VSSOP)	DRC (VSON)	YZP (DSBGA)	
		10 PINS	10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	154	49.4	90.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.9	71.2	0.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	83.6	23.8	8.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.4	2.2	3.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	82.2	23.8	8.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	6.1	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics for 3-V Supply

V_{CC} = 2.7 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_{CC}	V
Peak ON resistance	r_{peak}	0 ≤ (V_{NO} or V_{NC}) ≤ V_{CC}, I_{COM} = –100 mA,	Switch ON, See 図 7-1	25°C	2.7 V		0.2	0.3	Ω
				Full				0.35	
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 2 V, I_{COM} = –100 mA,	Switch ON, See 図 7-1	25°C	2.7 V		0.26	0.3	Ω
				Full				0.34	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See 図 7-1	25°C	2.7 V		0.01	0.05	Ω
				Full				0.05	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NO} or V_{NC}) ≤ V_{CC}, I_{COM} = –100 mA,	Switch ON, See 図 7-1	25°C	2.7 V		0.13		Ω
		V_{NO} or V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See 図 7-1	25°C			0.01	0.04	Ω
				Full				0.05	
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 1 V, V_{COM} = 3 V, or V_{NC} or V_{NO} = 3 V, V_{COM} = 1 V,	Switch OFF, See 図 7-2	25°C	3.6 V	–10		10	nA
				Full		–50		50	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 1 V, V_{COM} = Open, or V_{NC} or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, See 図 7-3	25°C	3.6 V	–10		10	nA
				Full		–100		100	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 1 V, or V_{NC} or V_{NO} = Open, V_{COM} = 3 V,	Switch ON, See 図 7-3	25°C	3.6 V	–10		10	nA
				Full		–100		100	
DIGITAL CONTROL INPUTS (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		1.4			V
Input logic low	V_{IL}			Full				0.5	V
Input leakage current	I_{IH}, I_{IL}	V_I = 3.6 V or 0		25°C	3.6 V	–40	5	40	nA
				Full		–50		50	

6.5 Electrical Characteristics for 3-V Supply (continued)

V_{CC} = 2.7 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
DYNAMIC									
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See 図 7-10	25°C	3 V		9		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_{CC} or GND, Switch OFF,	See 図 7-4	25°C	3 V		90		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_{CC} or GND, Switch ON,	See 図 7-4	25°C	3 V		224		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_{CC} or GND, Switch ON,	See 図 7-4	25°C	3 V		250		pF
Digital input capacitance	C_I	V_{IN} = V_{CC} or GND,	See 図 7-4	25°C	3 V		2		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See 図 7-7	25°C	3 V		23		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	See 図 7-8	25°C	3 V		–72		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	See 図 7-9	25°C	3 V		–96		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See 図 7-11	25°C	3 V		0.003%		
SUPPLY									
Positive supply current	I_{CC}	V_{IN} = V_{CC} or GND		25°C	3.6 V		15	100	nA
				Full			1		μA

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*.

6.6 Electrical Characteristics for 2.5-V Supply

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_{CC}	V
Peak ON resistance	r_{peak}	0 ≤ (V_{NO} or V_{NC}) ≤ V_{CC}, I_{COM} = –8 mA,	Switch ON, See 図 7-1	25°C	2.3 V			0.35	Ω
				Full				0.45	
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 1.8 V, I_{COM} = –8 mA,	Switch ON, See 図 7-1	25°C	2.3 V				Ω
				Full				0.4	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 1.8 V, 0.8 V, I_{COM} = –8 mA,	Switch ON, See 図 7-1	25°C	2.3 V		0.01	0.05	Ω
				Full			0.05	0.05	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NO} or V_{NC}) ≤ V_{CC}, I_{COM} = –8 mA,	Switch ON, See 図 7-1	25°C	2.3 V		0.05		Ω
		V_{NO} or V_{NC} = 0.8 V, 1.8 V, I_{COM} = –8 mA,	Switch ON, See 図 7-1	25°C			0.03	0.08	
				Full				0.1	
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 0.5 V, V_{COM} = 2.2 V, or V_{NC} or V_{NO} = 2.2 V, V_{COM} = 0.5 V,	Switch OFF, See 図 7-2	25°C	2.7 V	–10		10	nA
				Full		–50		50	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 0.5 V, V_{COM} = Open, or V_{NC} or V_{NO} = 2.2 V, V_{COM} = Open,	Switch ON, See 図 7-3	25°C	2.7 V	–10		10	nA
				Full		–100		100	

6.6 Electrical Characteristics for 2.5-V Supply (continued)

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH (continued)									
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 0.5 V, or V_{NC} or V_{NO} = Open, V_{COM} = 2.2 V,	Switch ON, See 図 7-3	25°C	2.7 V	–10		10	nA
				Full		–100		100	
DIGITAL CONTROL INPUTS (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		1.25			V
Input logic low	V_{IL}			Full				0.5	V
Input leakage current	I_{IH}, I_{IL}	V_I = 2.7 V or 0		25°C	2.7 V	–40	5	40	nA
				Full		–50		50	
DYNAMIC									
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See 図 7-10	25°C	2.5 V		8		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_{CC} or GND, Switch OFF,	See 図 7-4	25°C	2.5 V		90		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_{CC} or GND, Switch ON,	See 図 7-4	25°C	2.5 V		250		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_{CC} or GND, Switch ON,	See 図 7-4	25°C	2.5 V		250		pF
Digital input capacitance	C_I	V_I = V_{CC} or GND,	See 図 7-4	25°C	2.5 V		2		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See 図 7-7	25°C	2.5 V		23		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	See 図 7-8	25°C	2.5 V		–72		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	See 図 7-9	25°C	2.5 V		–96		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See 図 7-11	25°C	2.5 V		0.003%		
SUPPLY									
Positive supply current	I_{CC}	V_I = V_{CC} or GND		25°C	2.7 V		10	100	nA
				Full			700		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*.

6.7 Electrical Characteristics for 1.8-V Supply

V_{CC} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_{CC}	V
Peak ON resistance	r_{peak}	0 ≤ (V_{NO} or V_{NC}) ≤V_{CC}, I_{COM} = –2 mA,	Switch ON, See 図 7-1	25°C	1.65 V		0.4	0.7	Ω
				Full				0.8	
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 1.5 V, I_{COM} = –2 mA,	Switch ON, See 図 7-1	25°C	1.65 V		0.3	0.45	Ω
				Full				0.5	
ANALOG SWITCH (continued)									
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 0.6 V, 1.5 V, I_{COM} = –2 mA,	Switch ON, See 図 7-1	25°C	1.65 V		0.02	0.04	Ω
				Full				0.05	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NO} or V_{NC}) ≤ V_{CC}, I_{COM} = –2 mA,	Switch ON, See 図 7-1	25°C	1.65 V		0.13		Ω
		V_{NO} or V_{NC} = 0.6 V, 1.5 V, I_{COM} = –8 mA,	Switch ON, See 図 7-1	25°C			0.08	0.15	
				Full				0.2	
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 0.3 V, V_{COM} = 1.65 V, or V_{NC} or V_{NO} = 1.65 V, V_{COM} = 0.3 V,	Switch OFF, See 図 7-2	25°C	1.95	–10		10	nA
				Full		–50		50	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 0.3 V, V_{COM} = Open, or V_{NC} or V_{NO} = 1.65 V, V_{COM} = Open,	Switch ON, See 図 7-3	25°C	1.95 V	–10		10	nA
				Full		–100		100	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 0.3 V, or V_{NC} or V_{NO} = Open, V_{COM} = 1.65 V,	Switch ON, See 図 7-3	25°C	1.95 V	–10		10	nA
				Full		–100		100	
DIGITAL CONTROL INPUTS (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		1			V
Input logic low	V_{IL}			Full				0.4	V
Input leakage current	I_{IH}, I_{IL}	V_I = 1.95 V or 0		25°C	1.95 V	–40	5	40	nA
				Full		–50		50	
DYNAMIC									
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See 図 7-10	25°C	1.8 V		5		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_{CC} or GND, Switch OFF,	See 図 7-4	25°C	1.8 V		90		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_{CC} or GND, Switch ON,	See 図 7-4	25°C	1.8 V		250		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_{CC} or GND, Switch ON,	See 図 7-4	25°C	1.8 V		250		pF
Digital input capacitance	C_{IN}	V_I = V_{CC} or GND,	See 図 7-4	25°C	1.8 V		2		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See 図 7-7	25°C	1.8 V		23		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	See 図 7-8	25°C	1.8 V		–73		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	See 図 7-9	25°C	1.8 V		–97		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See 図 7-11	25°C	1.8 V		0.005%		

6.7 Electrical Characteristics for 1.8-V Supply (continued)

V_{CC} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
SUPPLY								
Positive supply current	I_{CC}	V_I = V_{CC} or GND	25°C	1.95 V		100	50	nA
			Full				700	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*.

6.8 Switching Characteristics for a 3-V Supply

V_{CC} = 2.7 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Dynamic									
Turnon time	t_{ON}	V_{COM} = V_{CC}, R_L = 50 Ω	C_L = 35 pF, See 図 7-5	25°C	3.0 V		20	35	ns
				Full	2.7 V to 3.6 V			40	
Turnoff time	t_{OFF}	V_{COM} = V_{CC}, R_L = 50 Ω	C_L = 35 pF, See 図 7-5	25°C	3.0 V		12	25	ns
				Full	2.7 V to 3.6 V			30	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_{CC}, R_L = 50 Ω	C_L = 35 pF, See 図 7-6	25°C	3.0 V	1	10	25	ns
				Full	2.7 V to 3.6 V	0.5		30	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

6.9 Switching Characteristics for a 2.5-V Supply

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Dynamic									
Turnon time	t_{ON}	V_{COM} = V_{CC}, R_L = 50 Ω	C_L = 35 pF, See 図 7-5	25°C	2.5 V		23	45	ns
				Full	2.3 V to 2.7 V			50	
Turnoff time	t_{OFF}	V_{COM} = V_{CC}, R_L = 50 Ω	C_L = 35 pF, See 図 7-5	25°C	2.5 V		17	27	ns
				Full	2.3 V to 2.7 V			30	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_{CC}, R_L = 50 Ω	C_L = 35 pF, See 図 7-6	25°C	2.5 V	2	14	30	ns
				Full	2.3 V to 2.7 V	1		35	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

6.10 Switching Characteristics for a 1.8-V Supply

V_{CC} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted) (1)

PARAMETER	TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
Dynamic							

V_{CC} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Turnon time	t_{ON}	V_{COM} = V_{CC}, R_L = 50 Ω	C_L = 35 pF, See 図 7-5	25°C	1.8 V		53	75	ns
				Full	1.65 V to 1.96 V			80	
Turnoff time	t_{OFF}	V_{COM} = V_{CC}, R_L = 50 Ω	C_L = 35 pF, See 図 7-5	25°C	1.8 V		24	35	ns
				Full	1.65 V to 1.96 V			40	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_{CC}, R_L = 50 Ω	C_L = 35 pF, See 図 7-6	25°C	1.8 V	2	30	40	ns
				Full	1.65 V to 1.96 V	1		50	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

6.11 Typical Characteristics

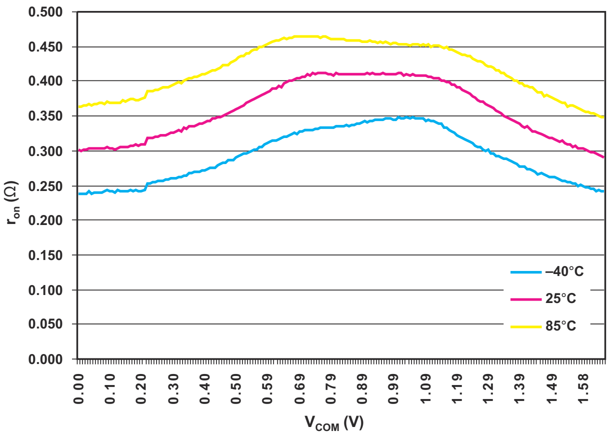


図 6-1. r_{on} vs V_{COM} (V_{CC} = 1.65 V)

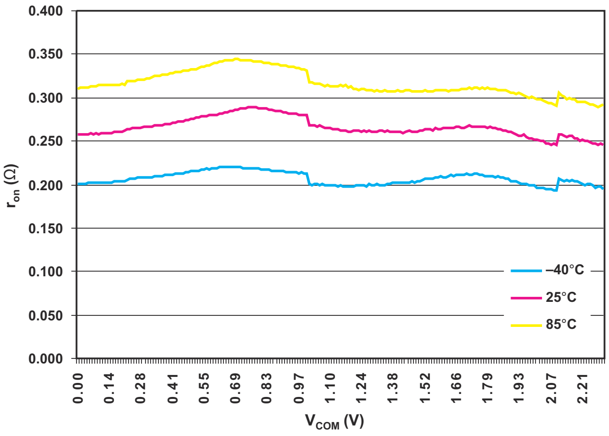


図 6-2. r_{on} vs V_{COM} (V_{CC} = 2.3 V)

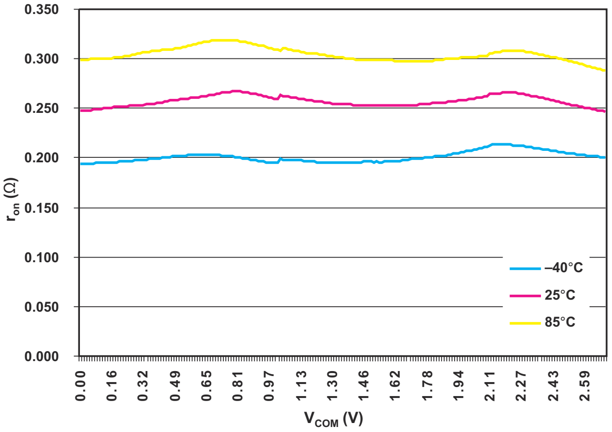


図 6-3. r_{on} vs V_{COM} (V_{CC} = 2.7 V)

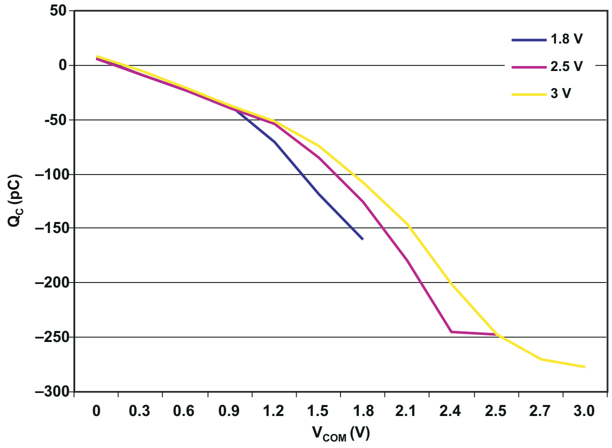


図 6-4. Charge Injection (Q_C) vs V_{COM} (T_A = 25°C)

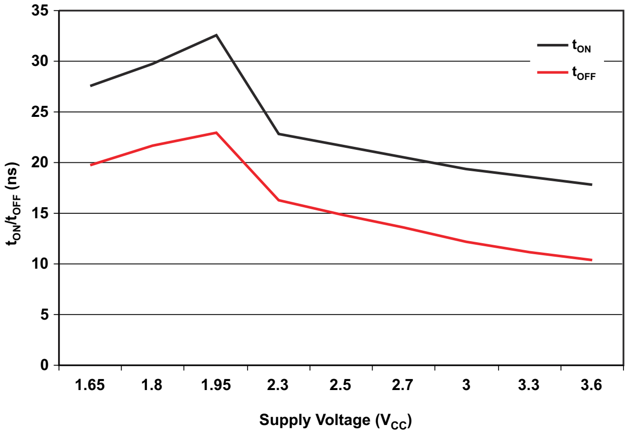


図 6-5. t_{ON} and t_{OFF} vs Supply Voltage (T_A = 25°C)

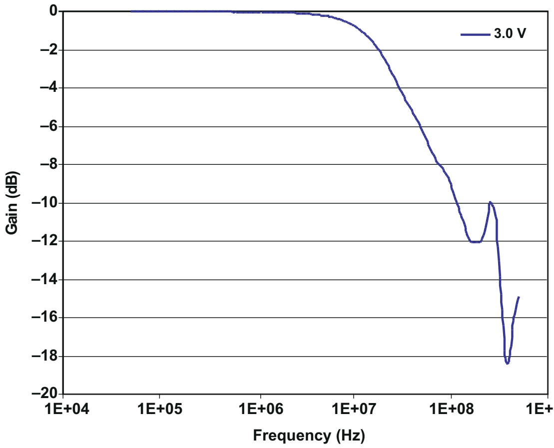


図 6-6. Bandwidth

6.11 Typical Characteristics (continued)

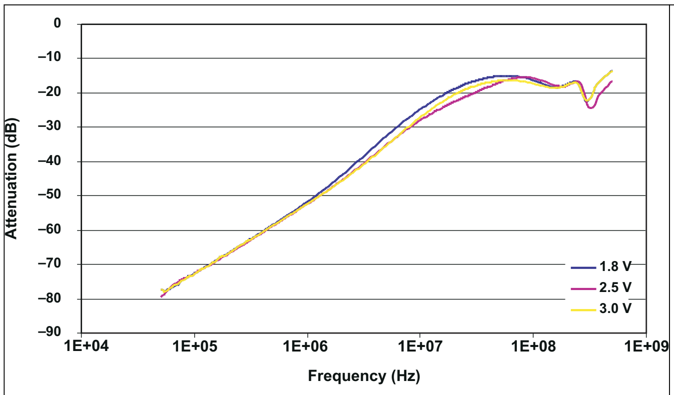


図 6-7. OFF Isolation

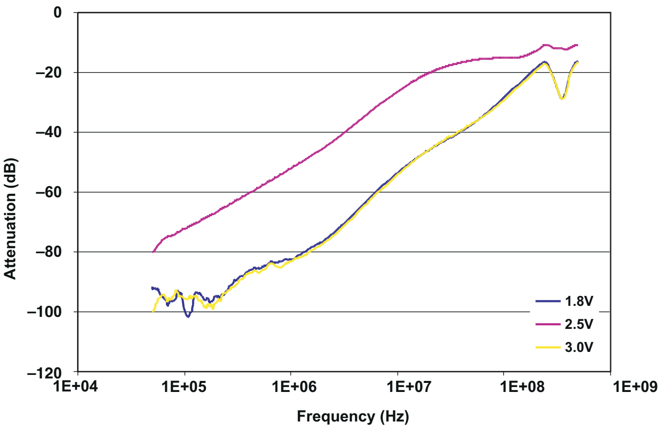


図 6-8. Crosstalk

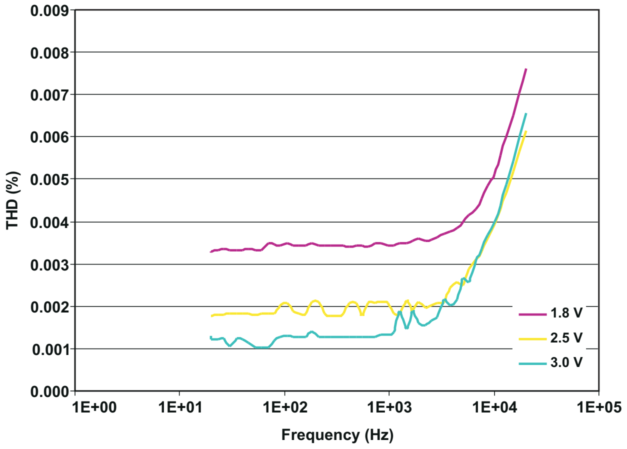


図 6-9. Total Harmonic Distortion vs Frequency

7 Parameter Measurement Information

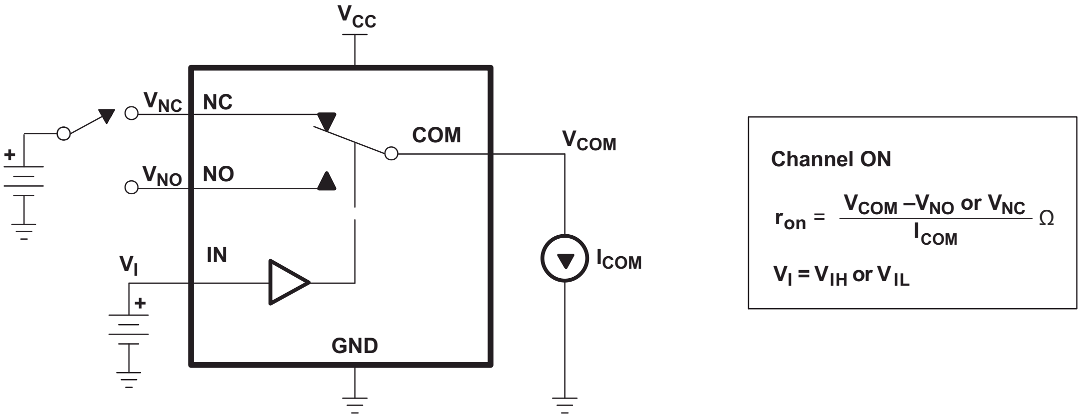


図 7-1. ON-State Resistance

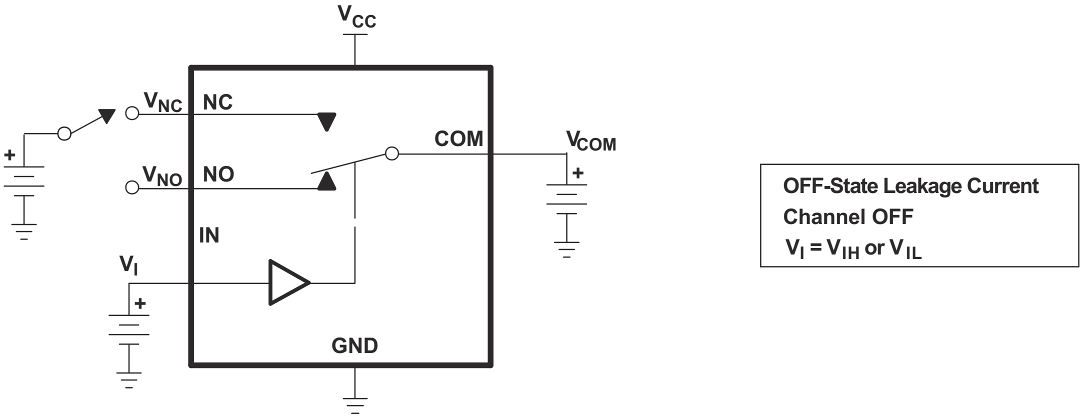


図 7-2. OFF-State Leakage Current ($I_{NC(OFF)}$, $I_{NC(PWROFF)}$, $I_{NO(OFF)}$, $I_{NO(PWROFF)}$, $I_{COM(OFF)}$, $I_{COM(PWROFF)}$)

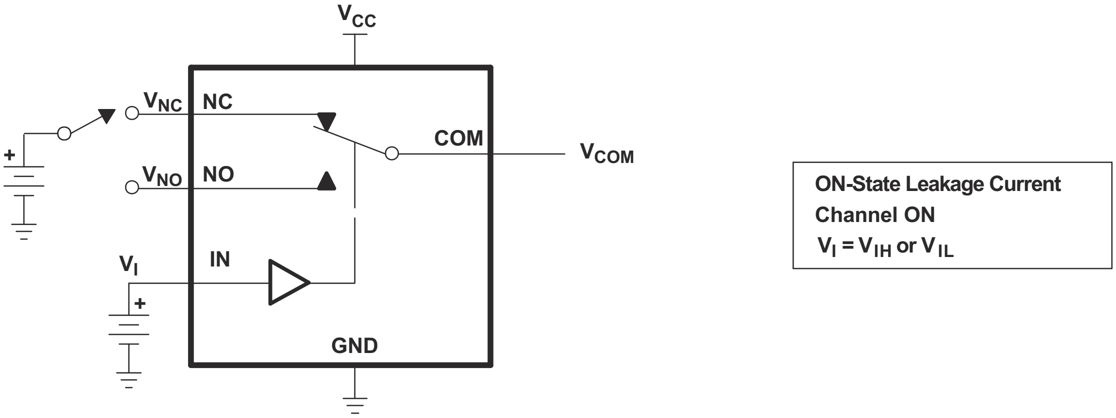
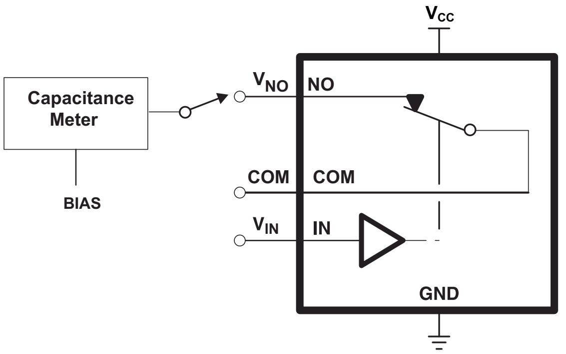
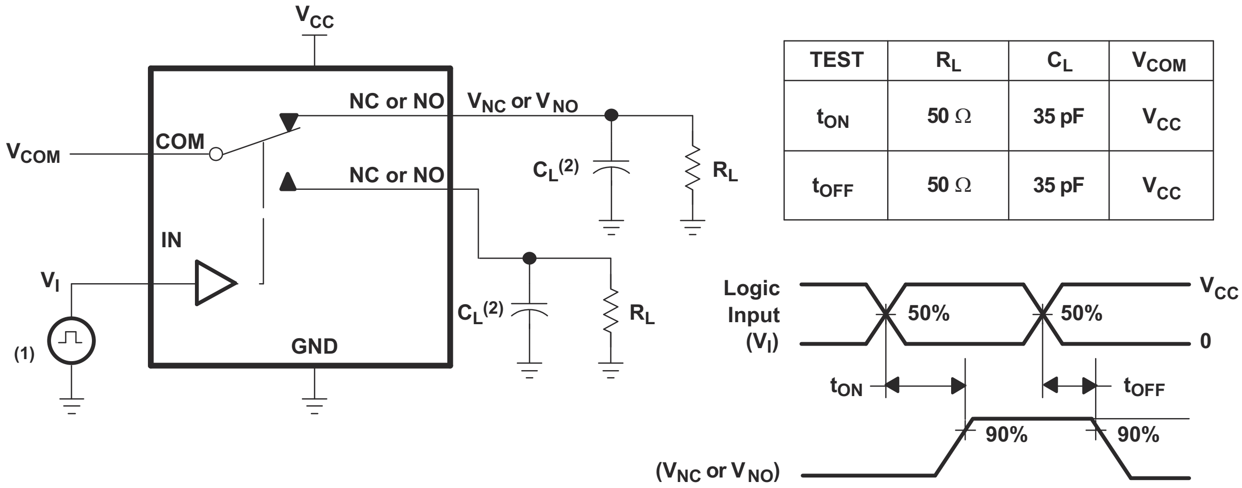


図 7-3. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)



V_{BIAS} = V_{CC} or GND and
V_{IN} = V_{IH} or V_{IL}
Capacitance is measured at NO, COM, and IN inputs during ON and OFF conditions.

図 7-4. Capacitance C_I, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)

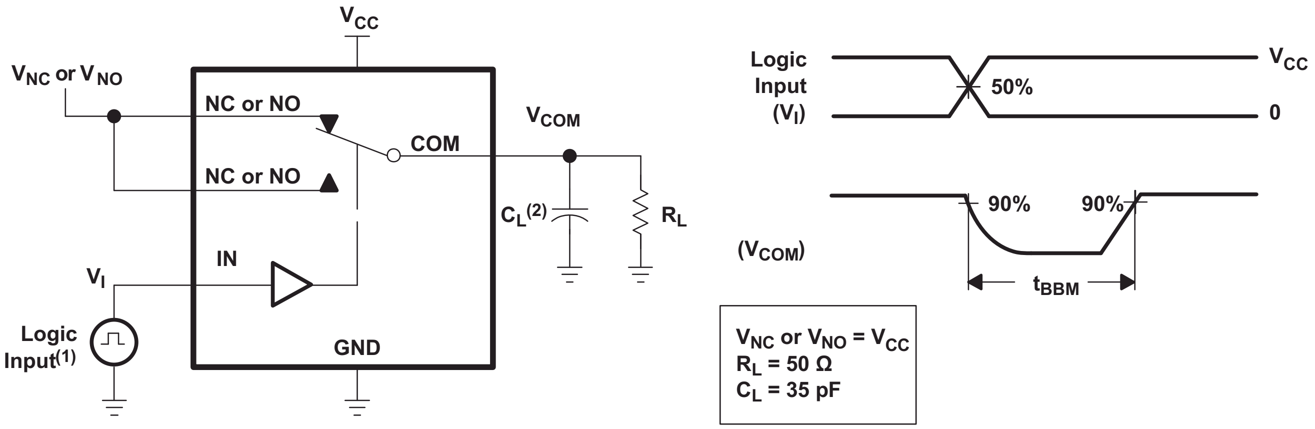


TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V_{CC}
t_{OFF}	50 Ω	35 pF	V_{CC}

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

図 7-5. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

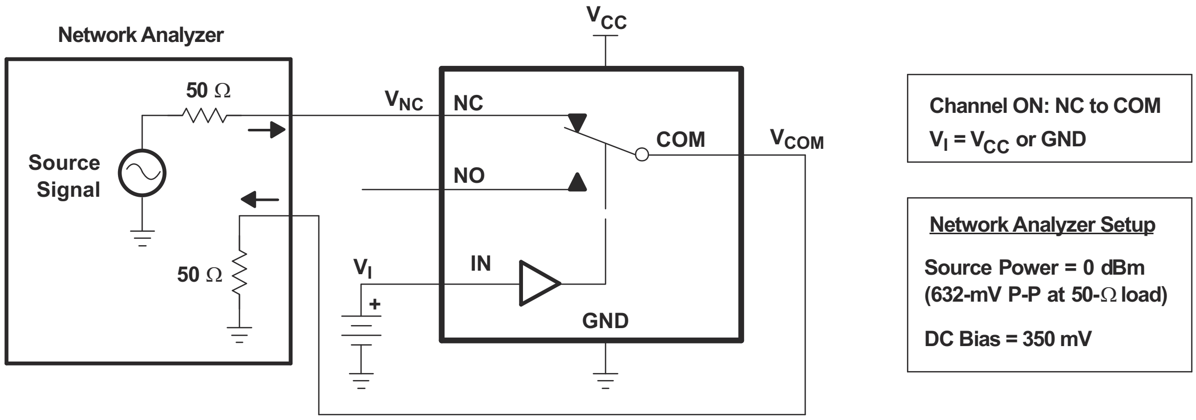


V_{NC} or V_{NO} = V_{CC}
R_L = 50 Ω
C_L = 35 pF

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

図 7-6. Break-Before-Make Time (t_{BBM})



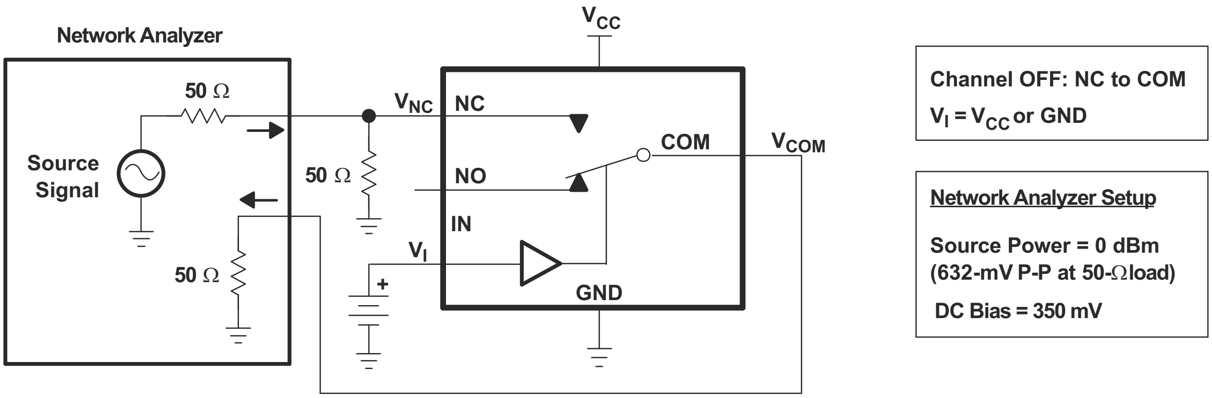
Channel ON: NC to COM
$V_I = V_{CC}$ or GND

Network Analyzer Setup

Source Power = 0 dBm
(632-mV P-P at 50-Ω load)

DC Bias = 350 mV

図 7-7. Bandwidth (BW)



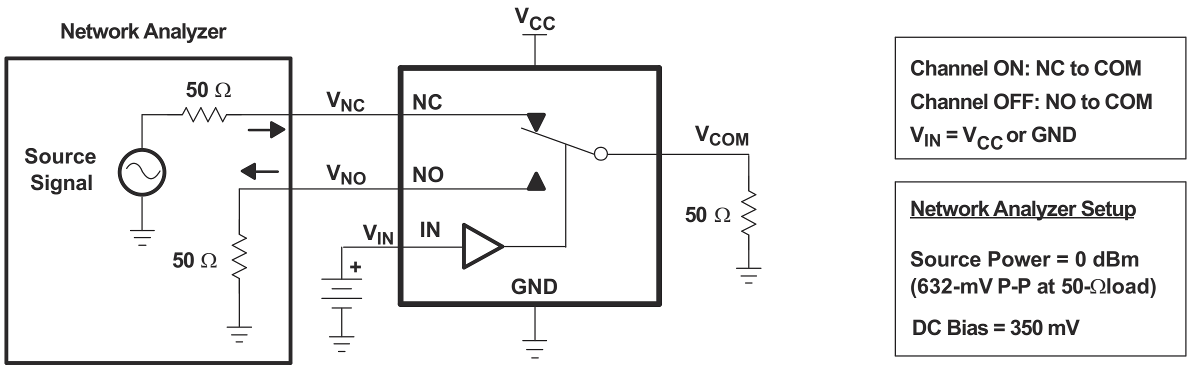
Channel OFF: NC to COM
$V_I = V_{CC}$ or GND

Network Analyzer Setup

Source Power = 0 dBm
(632-mV P-P at 50-Ω load)

DC Bias = 350 mV

図 7-8. OFF Isolation (O_{ISO})



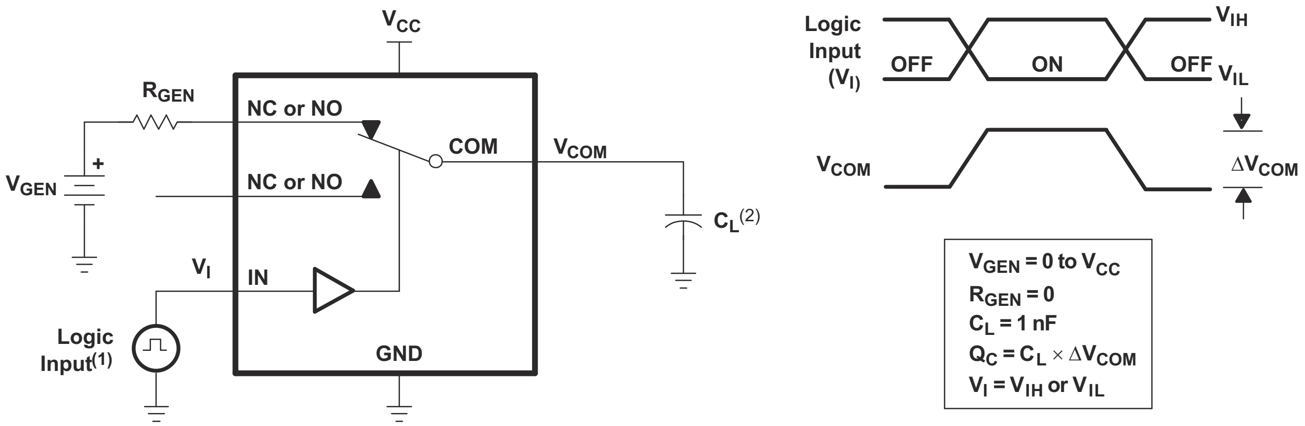
Channel ON: NC to COM
Channel OFF: NO to COM
$V_{IN} = V_{CC}$ or GND

Network Analyzer Setup

Source Power = 0 dBm
(632-mV P-P at 50-Ω load)

DC Bias = 350 mV

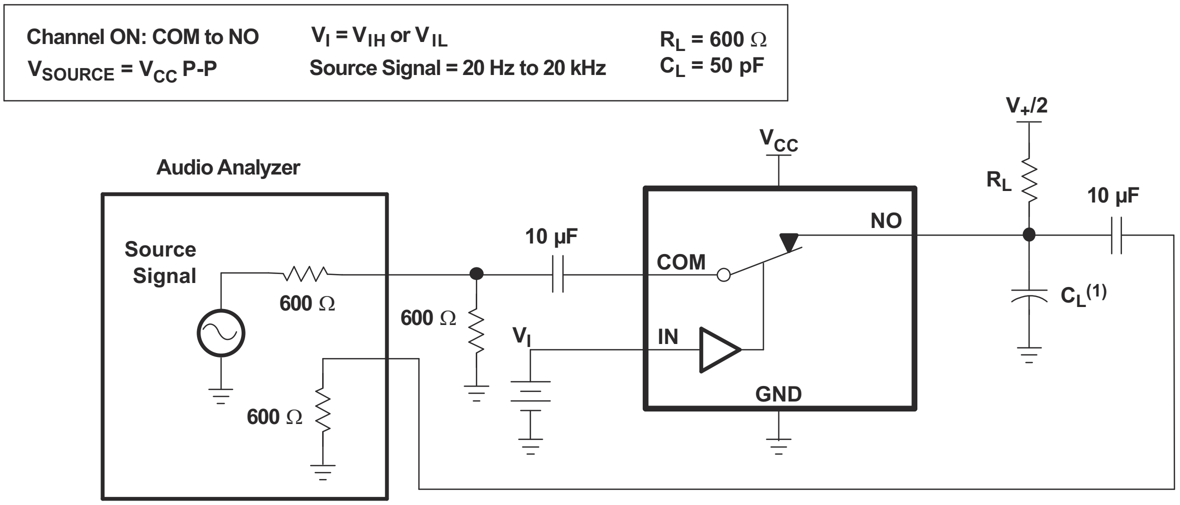
図 7-9. Crosstalk (X_{TALK})



A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

図 7-10. Charge Injection (Q_C)



A. C_L includes probe and jig capacitance.

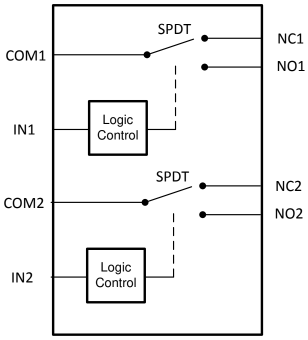
図 7-11. Total Harmonic Distortion (THD)

8 Detailed Description

8.1 Overview

The TS3A24159 is a 2-channel single-pole double-throw (SPDT) bidirectional analog switch that is designed to operate from 1.65 V to 3.6 V. It offers low ON-state resistance and excellent ON-state resistance matching with the break-before-make feature, to prevent signal distortion during the transferring of a signal from one channel to another. The device has excellent total harmonic distortion (THD) performance, low ON-state resistance, and consumes very low power. These are some of the features that make this device suitable for a variety of markets and many different applications.

8.2 Functional Block Diagram



8.3 Feature Description

The TS3A24159 device is bidirectional with two single-pole, double-throw switches. Each of the two switches are controlled independently by two digital signals.

8.4 Device Functional Modes

表 8-1. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

9 Application and Implementation

注

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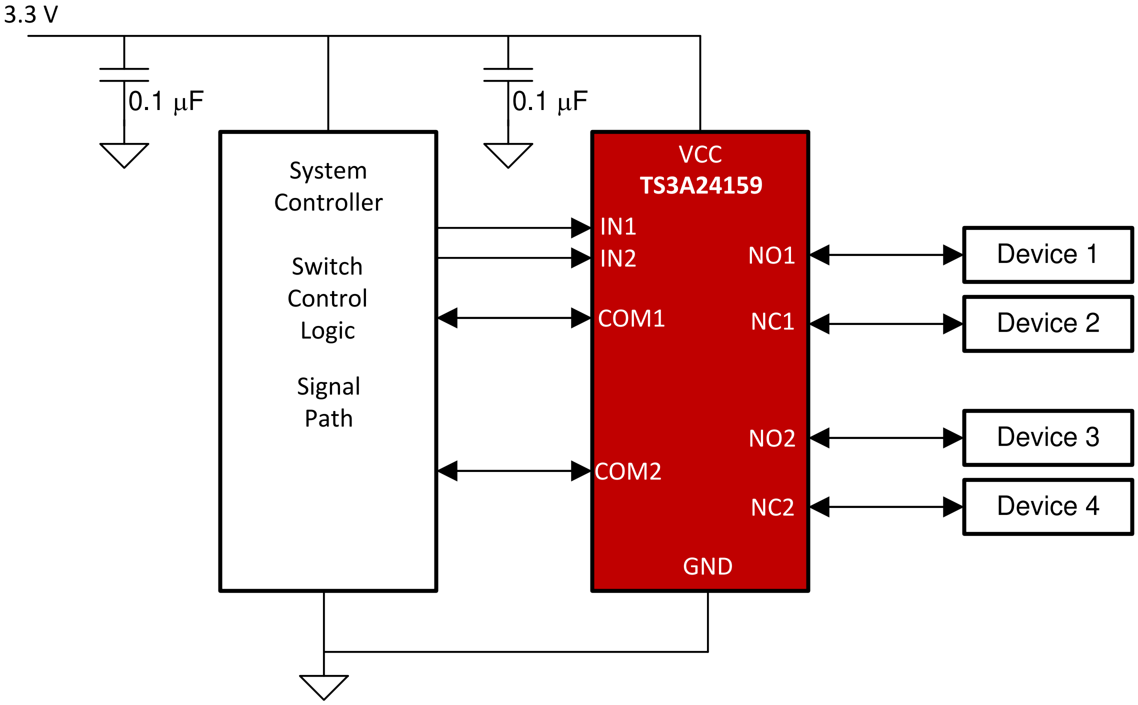
9.1 Application Information

The switch of the TS3A24159 device is bidirectional. Hence, NO, NC, and COM pins can be used as both inputs or outputs.

9.2 Typical Application



9.2.1 Design Requirements

Ensure that all of the signals passing through the switch are within the specified ranges to ensure proper performance.

表 9-1. Design Parameters

		MIN	MAX	UNIT
V_{CC}	Supply Voltage	1.65	3.6	V
V_{NC} V_{NO} V_{COM}	Signal Voltage	0	V_{CC}	V
V_{IN}	Digital Input Voltage	0	V_{CC}	V

9.2.2 Detailed Design Procedure

The TS3A24159 device can be properly operated without any external components. However, it is recommended to connect the unused pins to ground through a 50-Ω resistor to prevent signal reflections back into the device. It is also recommended that the digital control pins (IN1 and IN2) be pulled up to V_{CC} or down to GND to avoid undesired switch positions that could result from the floating pin.

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch because the TS3A24159 input/output signal swing through NO and COM are dependant of the supply voltage V_{CC}.

9.2.3 Application Curve

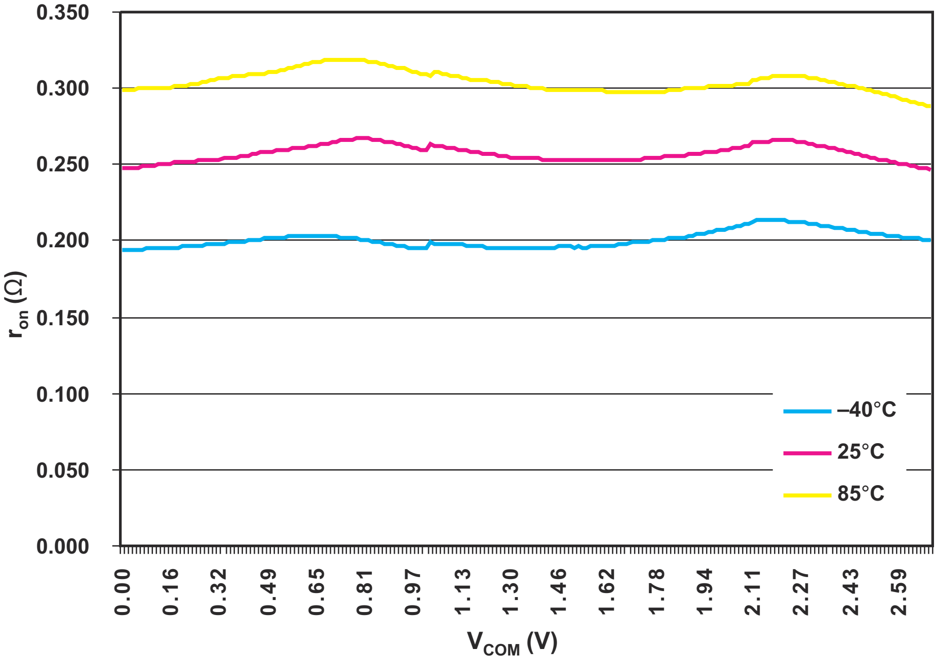


図 9-1. r_{ON} vs V_{COM}

10 Power Supply Recommendations

- Proper power-supply sequencing is recommended for all CMOS devices.
- Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device.
- Always sequence V_{CC} on first, followed by NO or COM.
- Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{CC} supply to other components.
- A 0.1-μF capacitor, connected from V_{CC} to GND, is adequate for most applications.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended. Bypass capacitors must be used on power supplies. Short trace lengths should be used to avoid excessive loading.

11.2 Layout Example

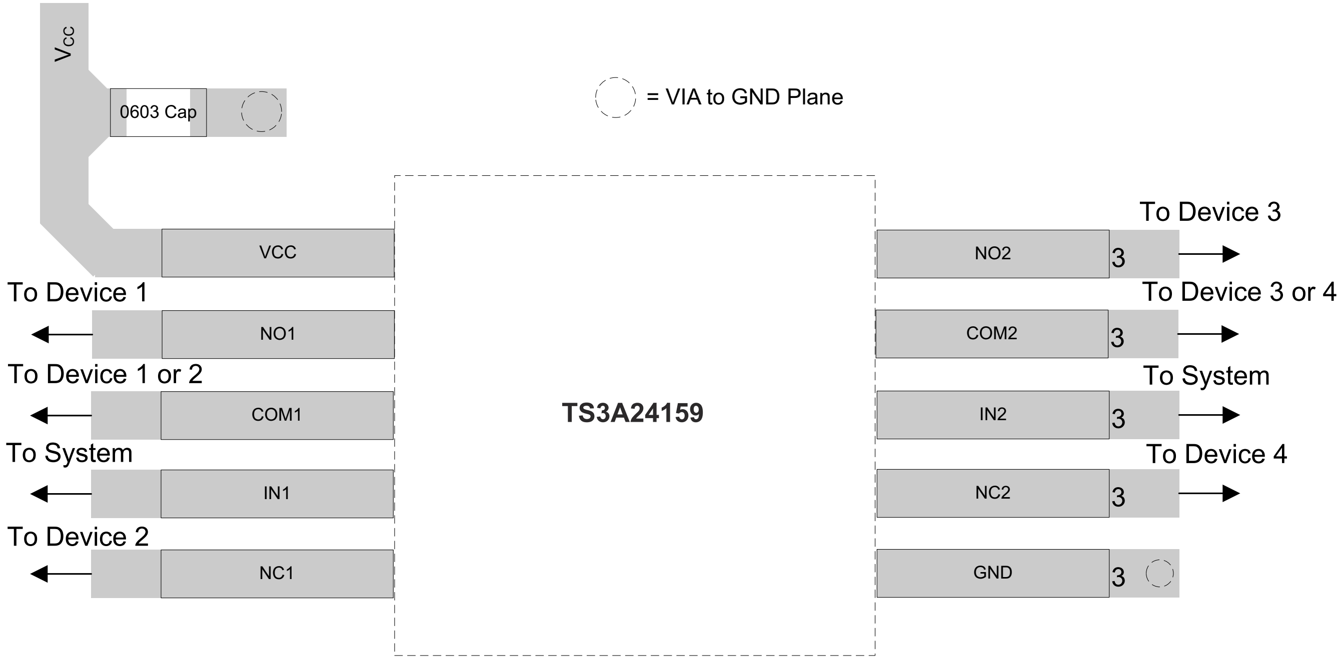


図 11-1. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 サポート・リソース

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12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3A24159DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(L8Q, L8R)	Samples
TS3A24159DRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZWS	Samples
TS3A24159YZPR	ACTIVE	DSBGA	YZP	10	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	L87	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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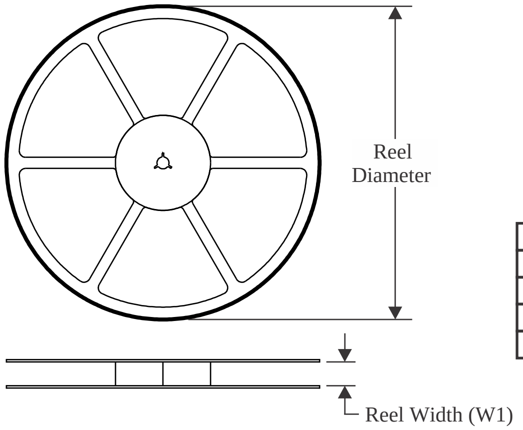
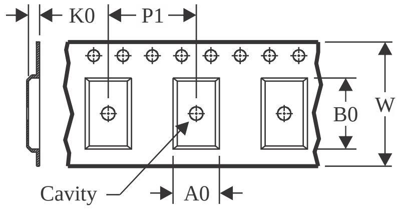
TAPE AND REEL INFORMATION

REEL DIMENSIONS

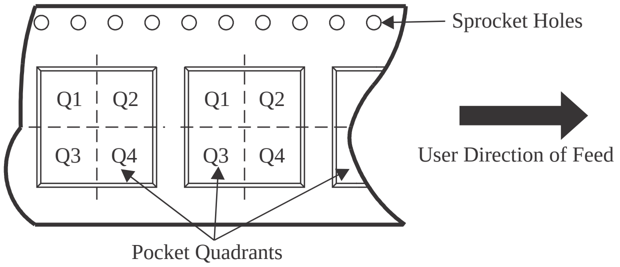


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

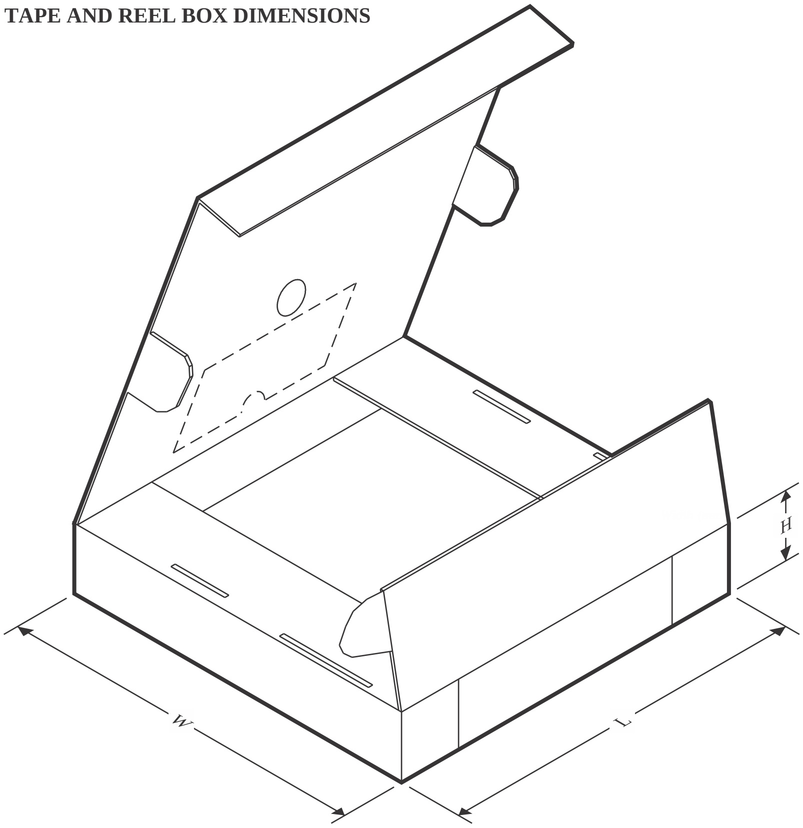
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A24159DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TS3A24159DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TS3A24159YZPR	DSBGA	YZP	10	3000	178.0	9.2	1.49	1.99	0.63	4.0	8.0	Q2

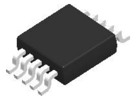
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A24159DGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TS3A24159DRCR	VSON	DRC	10	3000	356.0	356.0	35.0
TS3A24159YZPR	DSBGA	YZP	10	3000	220.0	220.0	35.0

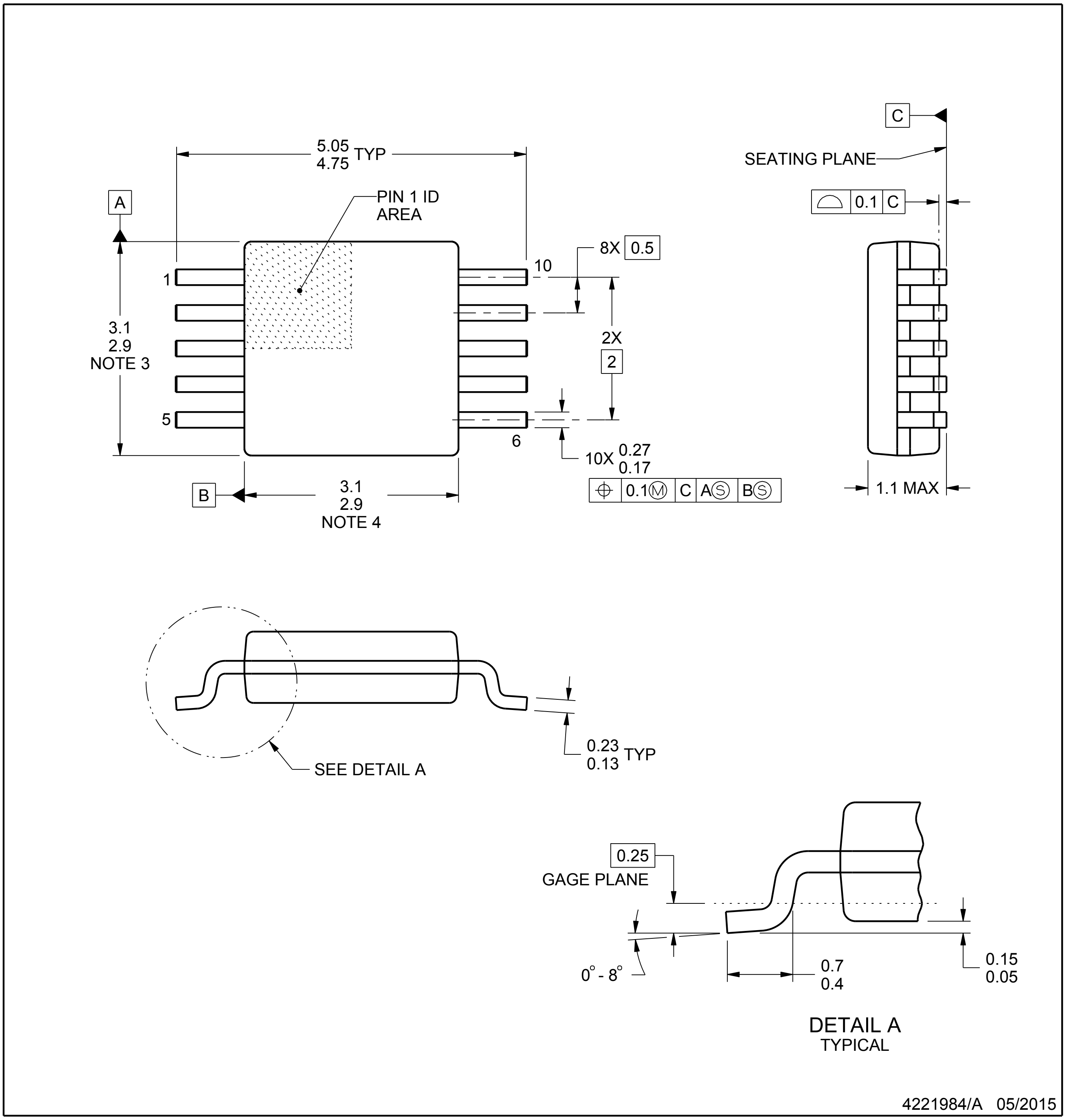
PACKAGE OUTLINE



DGS0010A

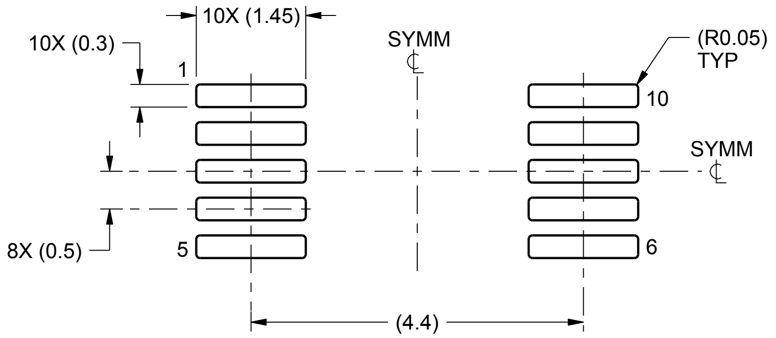
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

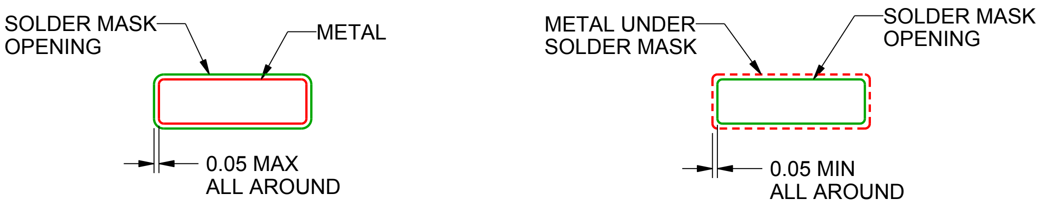


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



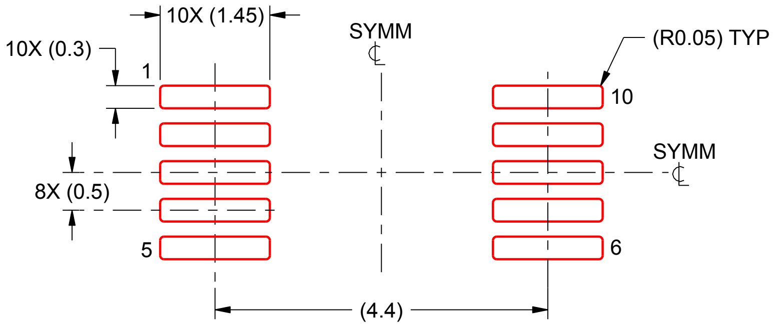
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

NOTES: (continued)

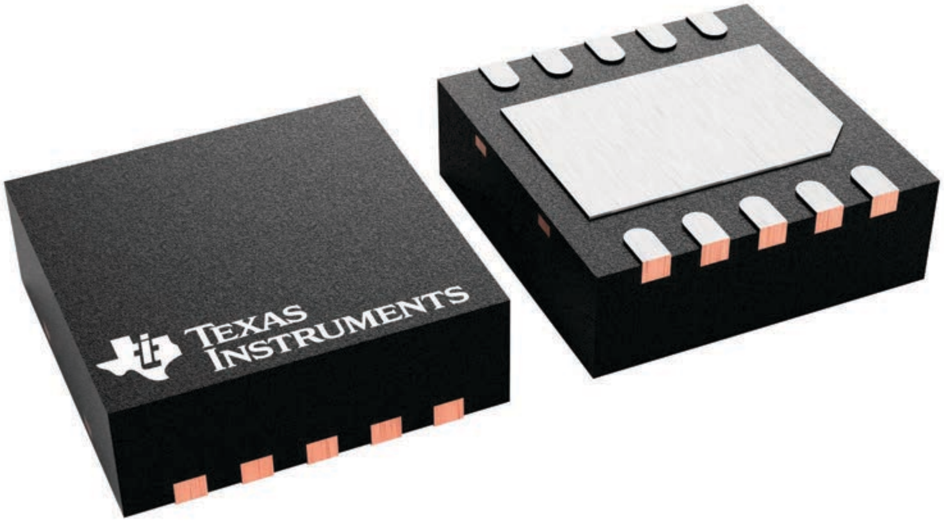
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

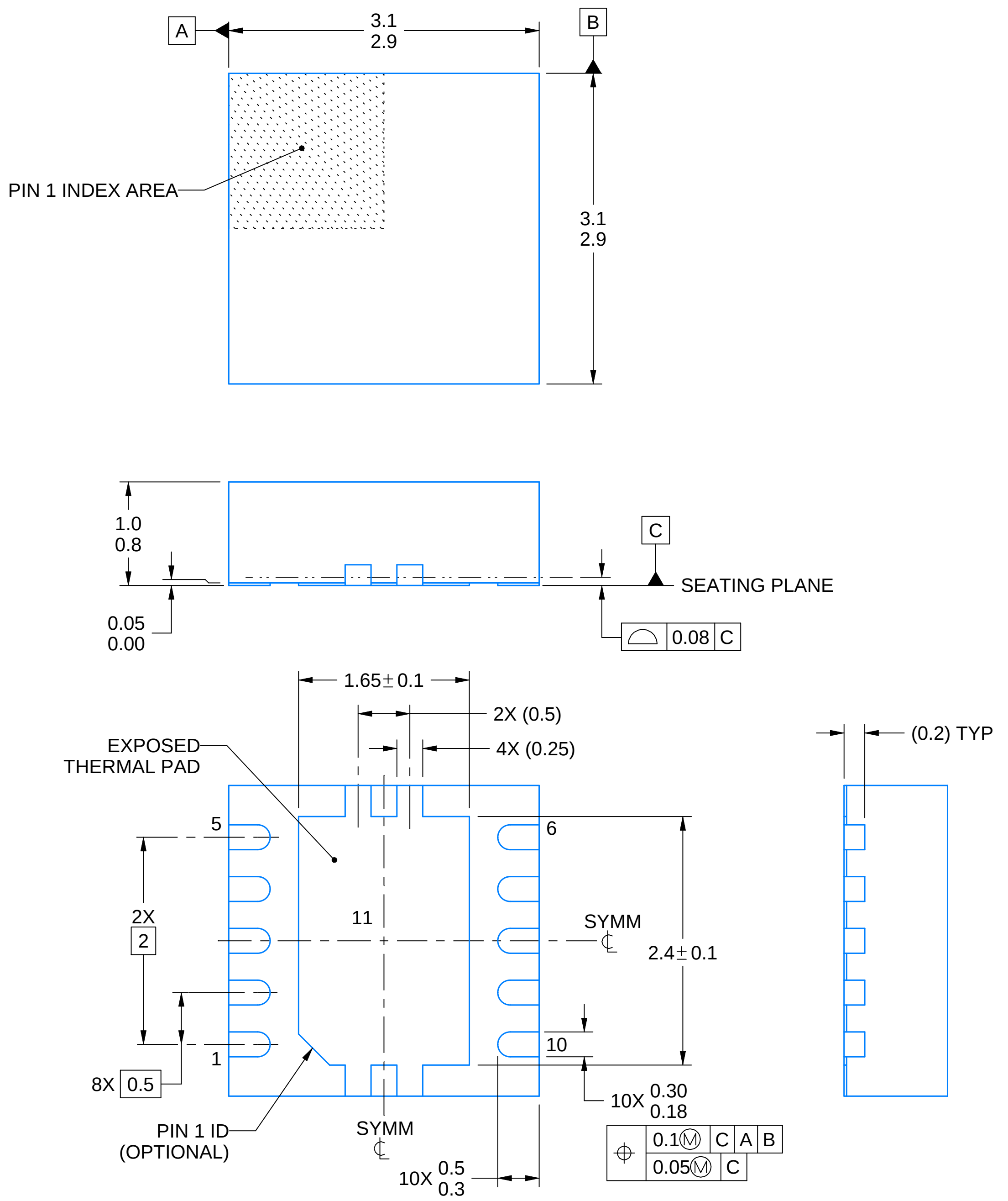
GENERIC PACKAGE VIEW

DRC 10 **VSON - 1 mm max height**

3 x 3, 0.5 mm pitch PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

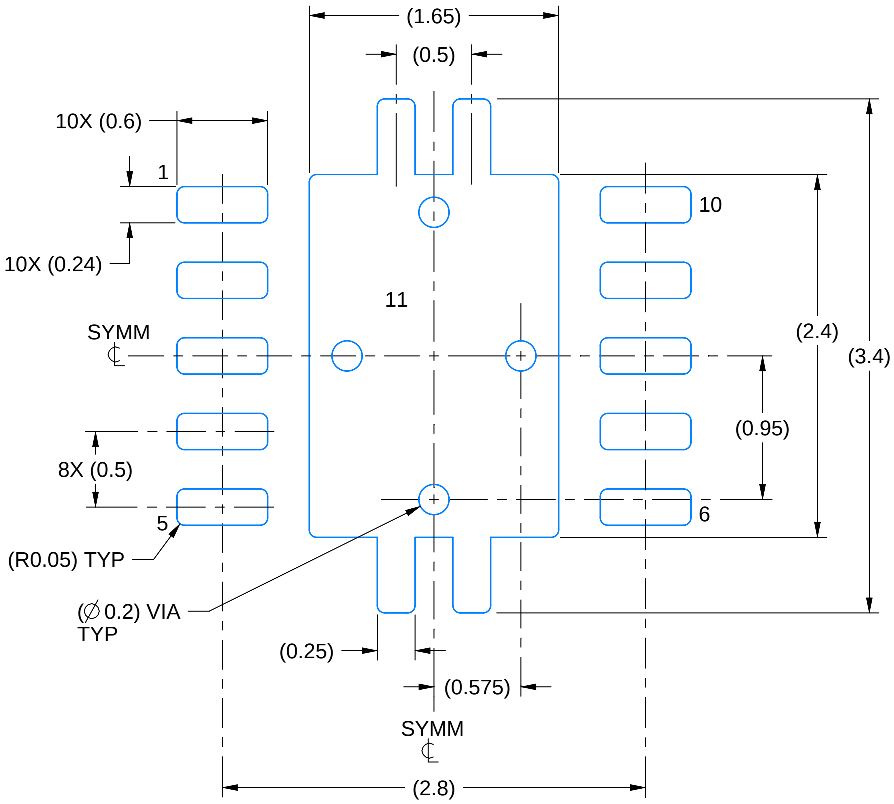




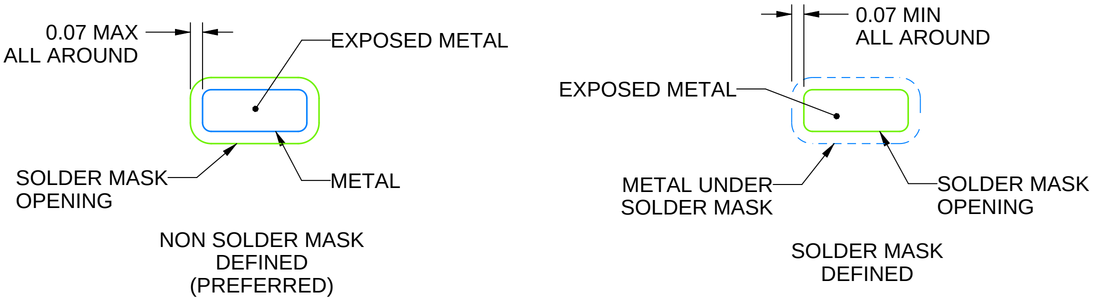
4218878/B 07/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



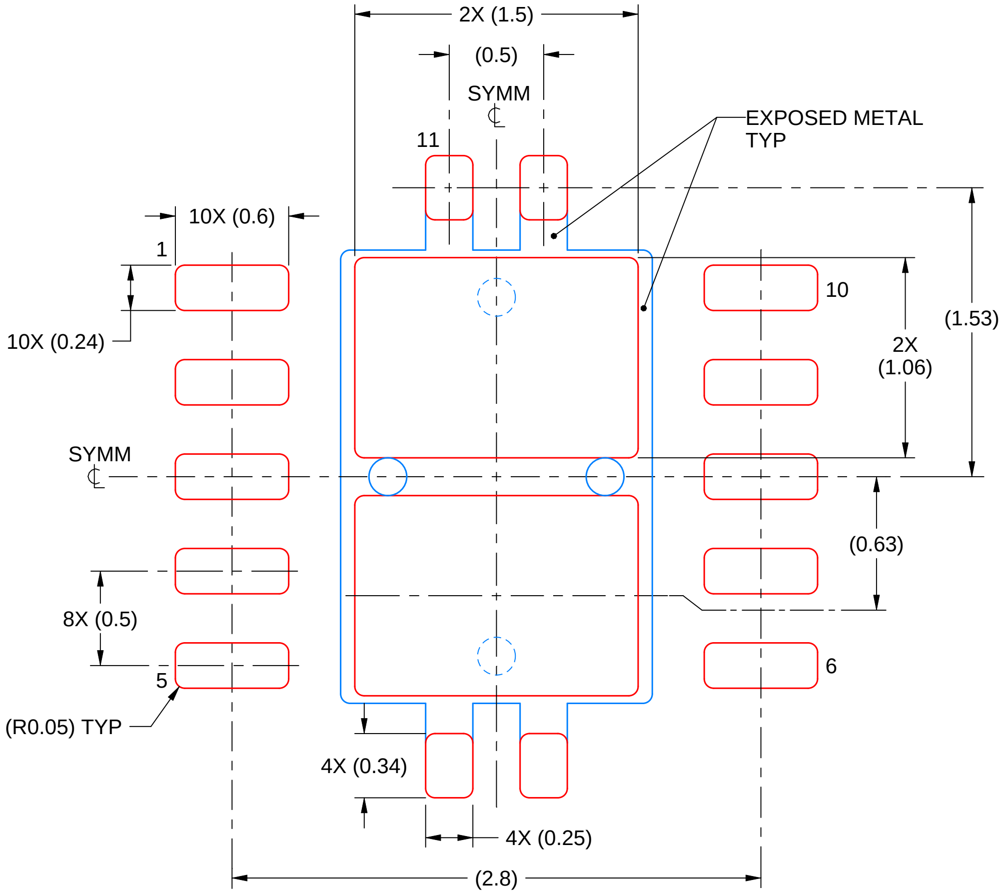
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



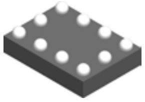
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

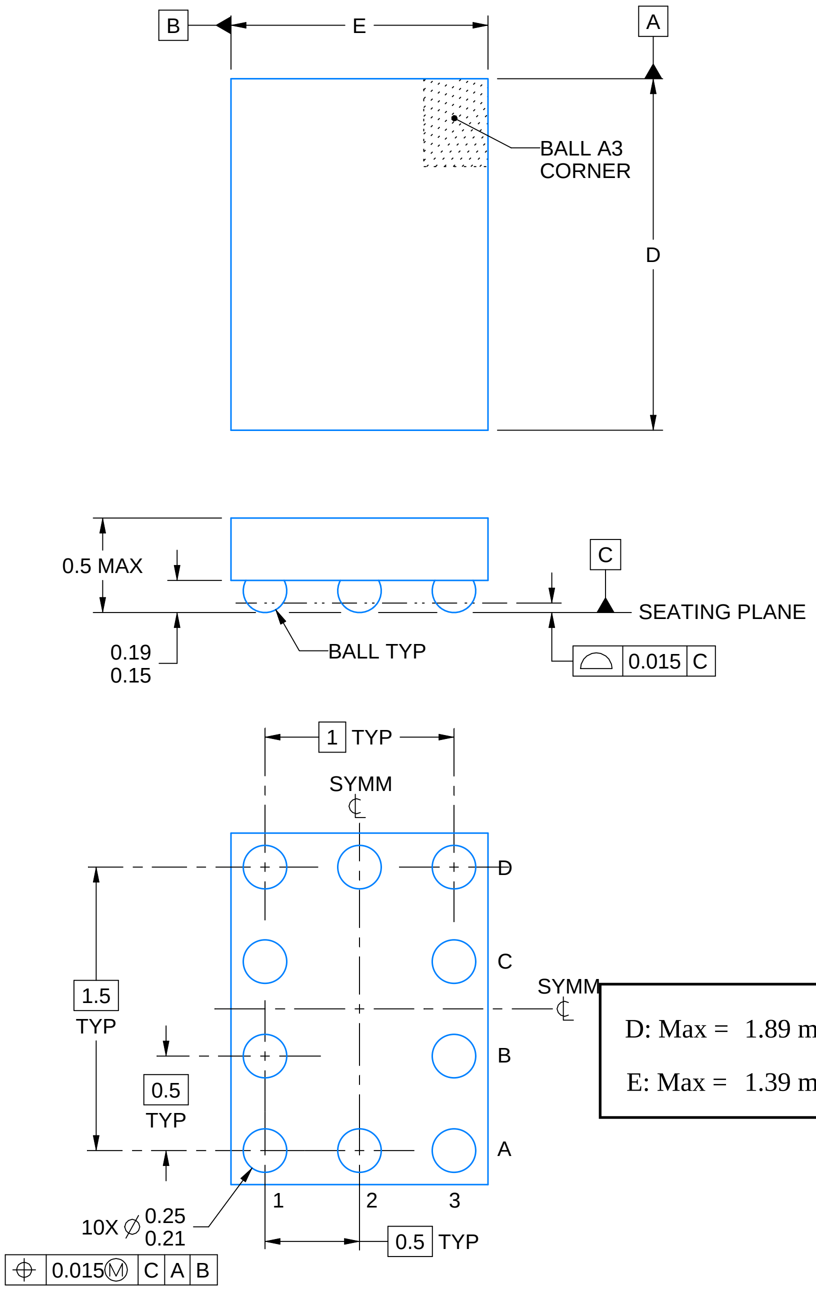


PACKAGE OUTLINE

YZP0010

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



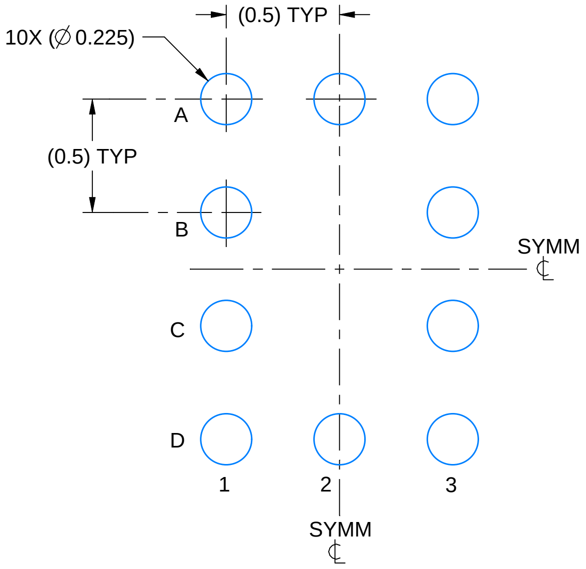
D: Max = 1.89 mm, Min = 1.83 mm

E: Max = 1.39 mm, Min = 1.33 mm

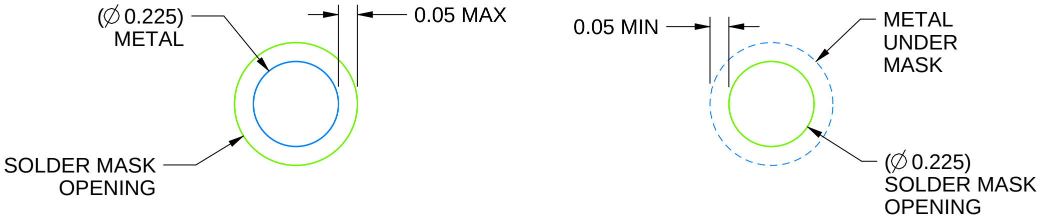
4219350/B 11/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X



NON-SOLDER MASK
DEFINED
(PREFERRED)

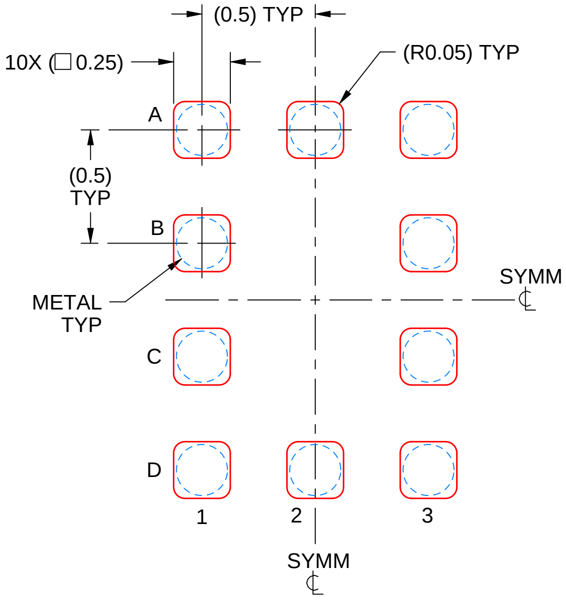
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4219350/B 11/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要なお知らせと免責事項

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