

TS5A23157 デュアル10Ω SPDTアナログ・スイッチ

1 特長

- 低いオン抵抗(125°Cで15Ω)
- 125°Cで動作
- 制御入力は5V許容
- Break-Before-Makeスイッチングを規定
- 低い電荷注入
- 優れたオン抵抗マッチング
- 低い全高調波歪み
- 1.8V~5.5Vの単電源で動作
- JESD 78, Class II準拠で100mA超のラッチアップ性能
- ESD性能はJESD 22に準拠しテスト済み
 - 人体モデルで2000V (A114-B, クラスII)
 - 荷電デバイス・モデルで1000V (C101)

2 アプリケーション

- サンプル・アンド・ホールド回路
- バッテリ駆動の機器
- オーディオおよびビデオ信号のルーティング
- 通信用回路

3 概要

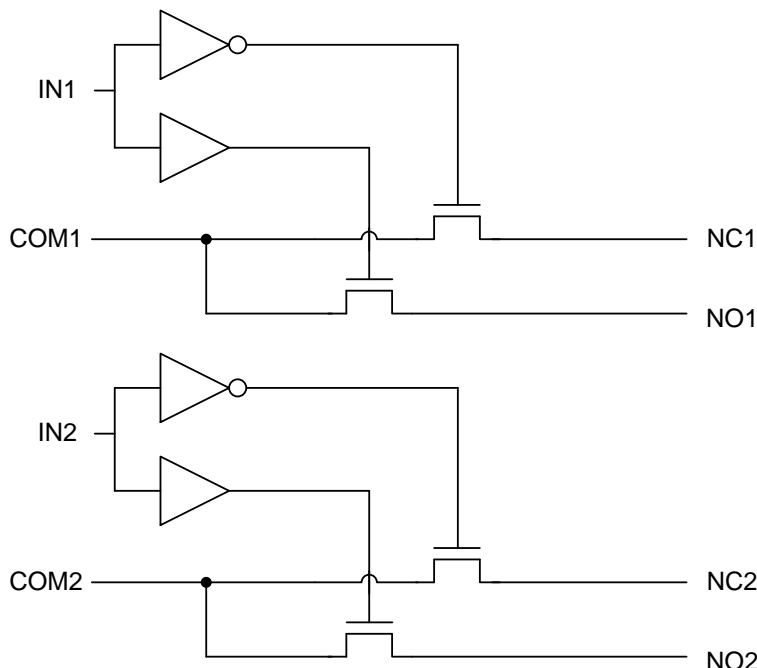
TS5A23157はデュアル単極双投(SPDT)アナログ・スイッチで、1.65V~5.5Vで動作するように設計されています。このデバイスはデジタルとアナログの両方の信号を処理でき、最大5.5V(ピーク)の信号をどちらの方向にも転送できます。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
TS5A23157DGS	VSSOP (10)	3.00mm×3.00mm
TS5A23157RSE	UQFN (10)	2.00mm×1.50mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

ブロック図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision E (June 2015) から Revision F に変更

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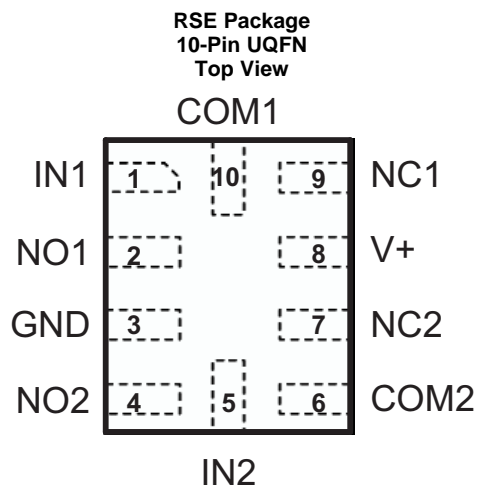
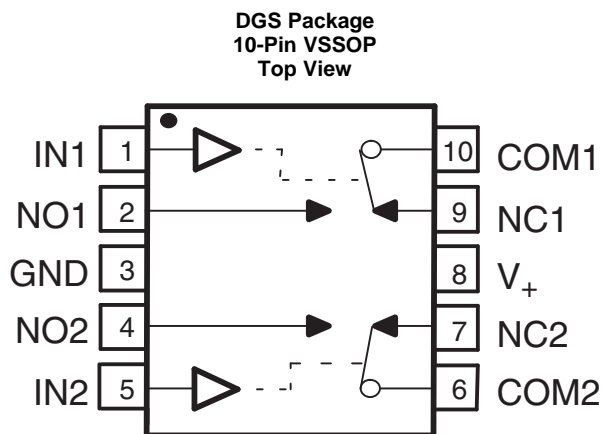
• 「特長」: 低いオン抵抗(10Ω)から低いオン抵抗(125°Cで15Ω)に変更	1
• 「特長」: 125°Cで動作を追加	1
• Added Junction Temperature To the <i>Absolute Maximum Ratings</i> table	4
• Changed the Operating temperature MAX value From: 85°C To: 125°C in the <i>Recommended Operating Conditions</i> table	4
• Changed the <i>Thermal Information</i> table	4
• Changed r_{on} in the <i>Electrical Characteristics for 5-V Supply</i> table	5
• Changed V_{IH} in the <i>Electrical Characteristics for 5-V Supply</i> table	5
• Changed t_{ON} and t_{OFF} in the <i>Electrical Characteristics for 5-V Supply</i> table	5
• Changed r_{on} in the <i>Electrical Characteristics for 3.3-V Supply</i> table	7
• Changed t_{ON} and t_{OFF} in the <i>Electrical Characteristics for 3.3-V Supply</i> table	7
• Changed r_{on} in the <i>Electrical Characteristics for 2.5-V Supply</i> table	8
• Changed t_{ON} and t_{OFF} in the <i>Electrical Characteristics for 2.5-V Supply</i> table	8
• Changed r_{on} in the <i>Electrical Characteristics for 1.8-V Supply</i> table	9
• Changed t_{ON} and t_{OFF} in the <i>Electrical Characteristics for 1.8-V Supply</i> table	9

Revision D (October 2013) から Revision E に変更

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• 「ピン構成および機能」セクション、「ESD定格」表、「機能説明」セクション、「デバイスの機能モード」、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクション 追加	1
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5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN1	I	Select pin for switch 1
2	NO1	I/O	Normally open I/O for switch 1
3	GND	—	Ground
4	NO2	I/O	Normally open I/O for switch 2
5	IN2	I	Select pin for switch 2
6	COM2	I/O	Common I/O for switch 2
7	NC2	I/O	Normally closed I/O for switch 2
8	V ₊	—	Power supply pin
9	NC1	I/O	Normally closed I/O for switch 1
10	COM1	I/O	Common I/O for switch 1

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V ₊	Supply voltage ⁽²⁾	-0.5	6.5	V
V _{NC} V _{NO} V _{COM}	Analog voltage ⁽²⁾⁽³⁾⁽⁴⁾	-0.5	V ₊ + 0.5	V
I _{I/O}	Analog port diode current	V _{NC} , V _{NO} , V _{COM} < 0 or V _{NC} , V _{NO} , V _{COM} > V ₊		±50 mA
I _{NC} I _{NO} I _{COM}	On-state switch current	V _{NC} , V _{NO} , V _{COM} = 0 to V ₊		±50 mA
V _{IN}	Digital input voltage ⁽²⁾⁽³⁾	-0.5	6.5	V
I _{IK}	Digital input clamp current	V _{IN} < 0		-50 mA
Continuous current through V ₊ or GND			±100	mA
T _J	Junction Temperature		150	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) This value is limited to 5.5 V maximum.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{I/O}	Switch input/output voltage	0	V ₊	V
V ₊	Supply voltage	1.65	5.5	V
V _I	Control input voltage	0	5.5	V
T _A	Operating temperature	-40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	TS5A23157		UNIT	
	DGS (VSSOP)	RSE (UQFN)		
	10 PINS	10 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	210.5	215.4	°C/W
R _{θJctop}	Junction-to-case (top) thermal resistance	99.1	140.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	132.4	137.9	°C/W
ψ _{JT}	Junction-to-top characterization parameter	29.1	13.7	°C/W
ψ _{JB}	Junction-to-board characterization parameter	130.5	137.6	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics for 5-V Supply

 $V_+ = 4.5 \text{ V to } 5.5 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	V_+	MIN	TYP ⁽¹⁾	MAX	UNIT
ANALOG SWITCH							
V_{COM}, V_{NO}, V_{NC}	Analog signal range			0		V_+	V
r_{on}	ON-state resistance	$0 \leq V_{NO} \text{ or } V_{NC} \leq V_+$, $I_{COM} = -30 \text{ mA}$, Switch ON, see Figure 9	Full -40 to 125°C	4.5 V		10 15	Ω
Δr_{on}	ON-state resistance match between channels	$V_{NO} \text{ or } V_{NC} = 3.15 \text{ V}$, $I_{COM} = -30 \text{ mA}$, Switch ON, see Figure 9	25°C	4.5 V	0.15		Ω
$r_{on(Flat)}$	ON-state resistance flatness	$0 \leq V_{NO} \text{ or } V_{NC} \leq V_+$, $I_{COM} = -30 \text{ mA}$, Switch ON, see Figure 9	25°C	4.5 V	4		Ω
$I_{NC(OFF)}, I_{NO(OFF)}$	NC, NO OFF leakage current	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$, $V_{COM} = 0 \text{ to } V_+$, Switch OFF, see Figure 10	25°C Full	5.5 V	-1	0.05 1	μA
$I_{NC(ON)}, I_{NO(ON)}$	NC, NO ON leakage current	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$, $V_{COM} = \text{Open}$, Switch ON, see Figure 10	25°C Full	5.5 V	-0.1	0.1 1	μA
$I_{COM(ON)}$	COM ON leakage current	$V_{NC} \text{ or } V_{NO} = \text{Open}$, $V_{COM} = 0 \text{ to } V_+$, Switch ON, see Figure 10	25°C Full	5.5 V	-0.1	0.1 1	μA
DIGITAL INPUTS (IN12, IN2)⁽²⁾							
V_{IH}	Input logic high		Full -40 to 125°C	4.75 V to 5.25 V	$V_+ \times 0.7$ 3.1		V
V_{IL}	Input logic low		Full			$V_+ \times 0.3$	V
I_{IH}, I_{IL}	Input leakage current	$V_{IN} = 5.5 \text{ V or } 0$	25°C Full	5.5 V	-1	0.05 1	μA
DYNAMIC							
t_{ON}	Turnon time	$V_{NC} = \text{GND and } V_{NO} = V_+$ or $V_{NC} = V_+ \text{ and } V_{NO} = \text{GND}$, $R_L = 500 \Omega$, $C_L = 50 \text{ pF}$, see Figure 12	Full -40 to 125°C	4.5 V to 5.5 V 4.75 V to 5.25 V	1.7 1.2	5.7 8.7	ns
t_{OFF}	Turnoff time	$V_{NC} = \text{GND and } V_{NO} = V_+$ or $V_{NC} = V_+ \text{ and } V_{NO} = \text{GND}$, $R_L = 500 \Omega$, $C_L = 50 \text{ pF}$, see Figure 12	Full -40 to 125°C	4.5 V to 5.5 V 4.75 V to 5.25 V	0.8 0.5	3.8 6.8	ns
t_{BBM}	Break-before-make time	$V_{NC} = V_{NO} = V_+/2$, $R_L = 50 \Omega$, $C_L = 35 \text{ pF}$, see Figure 13	Full	4.5 V to 5.5 V	0.5		ns
Q_C	Charge injection	$V_{NC} = V_{NO} = V_+/2$, $R_L = 50 \Omega$, See Figure 17	25°C	5 V	7		pC
$C_{NC(OFF)}, C_{NO(OFF)}$	NC, NO OFF capacitance	$V_{NC} \text{ or } V_{NO} = V_+ \text{ or GND}$, Switch OFF, see Figure 11	25°C	5 V	5.5		pF
$C_{NC(ON)}, C_{NO(ON)}$	NC, NO ON capacitance	$V_{NC} \text{ or } V_{NO} = V_+ \text{ or GND}$, Switch ON, see Figure 11	25°C	5 V	17.5		pF
$C_{COM(ON)}$	COM ON capacitance	$V_{COM} = V_+ \text{ or GND}$, Switch ON, see Figure 11	25°C	5 V	17.5		pF
C_{IN}	Digital input capacitance	$V_{IN} = V_+ \text{ or GND}$, See Figure 11	25°C	5 V	2.8		pF
BW	Bandwidth	$R_L = 50 \Omega$, Switch ON, see Figure 14	25°C	4.5 V	220		MHz

(1) $T_A = 25^\circ\text{C}$.

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs, SCBA004*.

Electrical Characteristics for 5-V Supply (continued)
 $V_+ = 4.5\text{ V to }5.5\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP ⁽¹⁾	MAX	UNIT
O_{ISO}	OFF isolation	$R_L = 50\ \Omega$, $f = 10\text{ MHz}$,	Switch OFF, see Figure 15	25°C	4.5 V		-65		dB
X_{TALK}	Crosstalk	$R_L = 50\ \Omega$, $f = 10\text{ MHz}$,	Switch ON, see Figure 16	25°C	4.5 V		-66		dB
THD	Total harmonic distortion	$R_L = 600\ \Omega$, $C_L = 50\text{ pF}$,	$f = 600\text{ Hz to }20\text{ kHz}$, see Figure 18	25°C	4.5 V		0.01%		
SUPPLY									
I_+	Positive supply current	$V_{IN} = V_+$ or GND,	Switch ON or OFF	25°C	5.5 V			1	μA
				Full				10	
ΔI_+	Change in supply current	$V_{IN} = V_+ - 0.6\text{ V}$		Full	5.5 V			500	μA

6.6 Electrical Characteristics for 3.3-V Supply

 $V_+ = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	V_+	MIN	TYP ⁽¹⁾	MAX	UNIT	
ANALOG SWITCH								
V_{COM}, V_{NO}, V_{NC}	Analog signal range			0		V_+	V	
r_{on}	ON-state resistance	$0 \leq V_{NO} \text{ or } V_{NC} \leq V_+$, $I_{COM} = -24\text{ mA}$,	Switch ON, see Figure 9	Full -40 to 125°C	3 V	18 23	Ω	
Δr_{on}	ON-state resistance match between channels	$V_{NO} \text{ or } V_{NC} = 2.1\text{ V}$, $I_{COM} = -24\text{ mA}$,	Switch ON, see Figure 9	25°C	3 V	0.2	Ω	
$r_{on(Flat)}$	ON-state resistance flatness	$0 \leq V_{NO} \text{ or } V_{NC} \leq V_+$, $I_{COM} = -24\text{ mA}$,	Switch ON, see Figure 11	25°C	3 V	9	Ω	
$I_{NC(OFF)}, I_{NO(OFF)}$	NC, NO OFF leakage current	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$, $V_{COM} = 0 \text{ to } V_+$,	Switch OFF, see Figure 10	25°C Full	3.6 V	-1 -1	1 1	μA
$I_{NC(ON)}, I_{NO(ON)}$	NC, NO ON leakage current	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$, $V_{COM} = \text{Open}$,	Switch ON, see Figure 10	25°C Full	3.6 V	-0.1 -1	0.1 1	μA
$I_{COM(ON)}$	COM ON leakage current	$V_{NC} \text{ or } V_{NO} = \text{Open}$, $V_{COM} = 0 \text{ to } V_+$,	Switch ON, see Figure 10	25°C Full	3.6 V	-0.1 -1	0.1 1	μA
DIGITAL INPUTS (IN12, IN2)⁽²⁾								
V_{IH}	Input logic high		Full			$V_+ \times 0.7$	V	
V_{IL}	Input logic low		Full			$V_+ \times 0.3$	V	
I_{IH}, I_{IL}	Input leakage current	$V_{IN} = 5.5\text{ V or }0$	25°C Full	3.6 V	-1 -1	0.05 1	1 1	μA
DYNAMIC								
t_{ON}	Turn-on time	$V_{NC} = \text{GND and } V_{NO} = V_+$ or $V_{NC} = V_+ \text{ and } V_{NO} = \text{GND}$,	$R_L = 500\ \Omega$, $C_L = 50\text{ pF}$, see Figure 12	Full -40 to 125°C	3 V to 3.6 V	2.5 2.0	7.6 10.6	ns ns
t_{OFF}	Turnoff time	$V_{NC} = \text{GND and } V_{NO} = V_+$ or $V_{NC} = V_+ \text{ and } V_{NO} = \text{GND}$,	$R_L = 500\ \Omega$, $C_L = 50\text{ pF}$, see Figure 12	Full -40 to 125°C	3 V to 3.6 V	1.5 1.0	5.3 8.3	ns ns
t_{BBM}	Break-before-make time	$V_{NC} = V_{NO} = V_+/2$, $R_L = 50\ \Omega$,	$C_L = 35\text{ pF}$, see Figure 13	Full	3 V to 3.6 V	0.5		ns
Q_C	Charge injection	$R_L = 50\ \Omega$, $C_L = 0.1\text{ nF}$,	see Figure 17	25°C	3.3 V	3		pC
BW	Bandwidth	$R_L = 50\ \Omega$, Switch ON,	see Figure 14	25°C	3 V	220		MHz
O_{ISO}	OFF isolation	$R_L = 50\ \Omega$, $f = 10\text{ MHz}$,	Switch OFF, see Figure 15	25°C	3 V	-65		dB
X_{TALK}	Crosstalk	$R_L = 50\ \Omega$, $f = 10\text{ MHz}$,	Switch ON, see Figure 16	25°C	3 V	-66		dB
THD	Total harmonic distortion	$R_L = 600\ \Omega$, $C_L = 50\text{ pF}$,	$f = 600\text{ Hz to }20\text{ kHz}$, see Figure 18	25°C	3 V	0.015%		
SUPPLY								
I_+	Positive supply current	$V_{IN} = V_+ \text{ or GND}$,	Switch ON or OFF	25°C Full	3.6 V		1 10	μA
ΔI_+	Change in supply current	$V_{IN} = V_+ - 0.6\text{ V}$		Full	3.6 V		500	μA

(1) $T_A = 25^\circ\text{C}$.

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

6.7 Electrical Characteristics for 2.5-V Supply

 $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	V_+	MIN	TYP ⁽¹⁾	MAX	UNIT	
ANALOG SWITCH								
$V_{\text{COM}}, V_{\text{NO}}, V_{\text{NC}}$	Analog signal range			0		V_+	V	
r_{on}	ON-state resistance	$0 \leq V_{\text{NO}} \text{ or } V_{\text{NC}} \leq V_+$, $I_{\text{COM}} = -8 \text{ mA}$,	Switch ON, see Figure 9	Full -40 to 125°C	2.3 V	45 50	Ω	
Δr_{on}	ON-state resistance match between channels	$V_{\text{NO}} \text{ or } V_{\text{NC}} = 1.6 \text{ V}$, $I_{\text{COM}} = -8 \text{ mA}$,	Switch ON, see Figure 9	25°C	2.3 V	0.5	Ω	
$r_{\text{on(Flat)}}$	ON-state resistance flatness	$0 \leq V_{\text{NO}} \text{ or } V_{\text{NC}} \leq V_+$, $I_{\text{COM}} = -8 \text{ mA}$,	Switch ON, see Figure 9	25°C	2.3 V	27	Ω	
$I_{\text{NC(OFF)}}, I_{\text{NO(OFF)}}$	NC, NO OFF leakage current	$V_{\text{NC}} \text{ or } V_{\text{NO}} = 0 \text{ to } V_+$, $V_{\text{COM}} = 0 \text{ to } V_+$,	Switch OFF, see Figure 10	25°C Full	2.7 V	-1 -1	0.05 1	μA
$I_{\text{NC(ON)}}, I_{\text{NO(ON)}}$	NC, NO ON leakage current	$V_{\text{NC}} \text{ or } V_{\text{NO}} = 0 \text{ to } V_+$, $V_{\text{COM}} = \text{Open}$,	Switch ON, see Figure 10	25°C Full	2.7 V	-0.1 -1	0.1 1	μA
$I_{\text{COM(ON)}}$	COM ON leakage current	$V_{\text{NC}} \text{ or } V_{\text{NO}} = \text{Open}$, $V_{\text{COM}} = 0 \text{ to } V_+$,	Switch ON, see Figure 10	25°C Full	2.7 V	-0.1 -1	0.1 1	μA
DIGITAL INPUTS (IN1, IN2)⁽²⁾								
V_{IH}	Input logic high		Full			$V_+ \times 0.7$	V	
V_{IL}	Input logic low		Full			$V_+ \times 0.3$	V	
$I_{\text{IH}}, I_{\text{IL}}$	Input leakage current	$V_{\text{IN}} = 5.5 \text{ V or } 0$	25°C Full	2.7 V	-1 -1	0.05 1	1 1	μA
DYNAMIC								
t_{ON}	Turnon time	$V_{\text{NC}} = \text{GND and } V_{\text{NO}} = V_+$ or $V_{\text{NC}} = V_+ \text{ and } V_{\text{NO}} = \text{GND}$,	$R_L = 500 \Omega$, $C_L = 50 \text{ pF}$, see Figure 12	Full -40 to 125°C	2.3 V to 2.7 V	3.5 2.5	14 17	ns
t_{OFF}	Turnoff time	$V_{\text{NC}} = \text{GND and } V_{\text{NO}} = V_+$ or $V_{\text{NC}} = V_+ \text{ and } V_{\text{NO}} = \text{GND}$,	$R_L = 500 \Omega$, $C_L = 50 \text{ pF}$, see Figure 12	Full -40 to 125°C	2.3 V to 2.7 V	2 1.5	7.5 10.5	ns
t_{BBM}	Break-before-make time	$V_{\text{NC}} = V_{\text{NO}} = V_+/2$, $R_L = 50 \Omega$,	$C_L = 35 \text{ pF}$, see Figure 13	Full	2.3 V to 2.7 V	0.5		ns
BW	Bandwidth	$R_L = 50 \Omega$,	Switch ON, see Figure 14	25°C	2.3 V	220		MHz
O_{ISO}	OFF isolation	$R_L = 50 \Omega$, $f = 10 \text{ MHz}$,	Switch OFF, see Figure 15	25°C	2.3 V	-65		dB
X_{TALK}	Crosstalk	$R_L = 50 \Omega$, $f = 10 \text{ MHz}$,	Switch ON, see Figure 16	25°C	2.3 V	-66		dB
THD	Total harmonic distortion	$R_L = 600 \Omega$, $C_L = 50 \text{ pF}$,	$f = 600 \text{ Hz to } 20 \text{ kHz}$, see Figure 18	25°C	2.3 V	0.025%		
SUPPLY								
I_+	Positive supply current	$V_{\text{IN}} = V_+ \text{ or GND}$,	Switch ON or OFF	25°C Full	2.7 V		1 10	μA
ΔI_+	Change in supply current	$V_{\text{IN}} = V_+ - 0.6 \text{ V}$		Full	2.7 V		500	μA

 (1) $T_A = 25^\circ\text{C}$.

 (2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

6.8 Electrical Characteristics for 1.8-V Supply

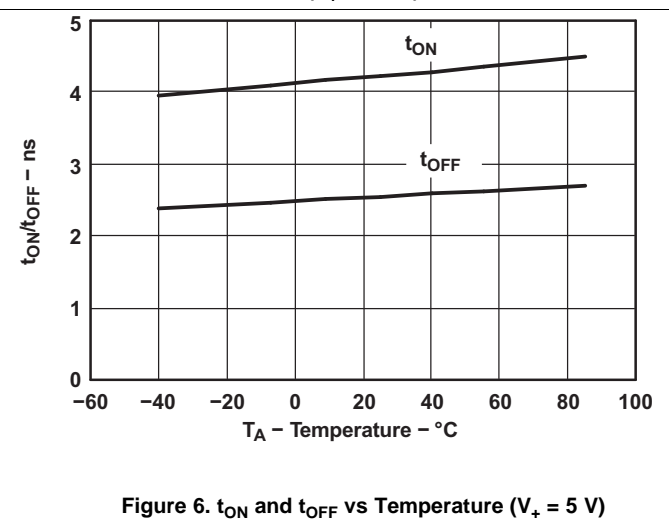
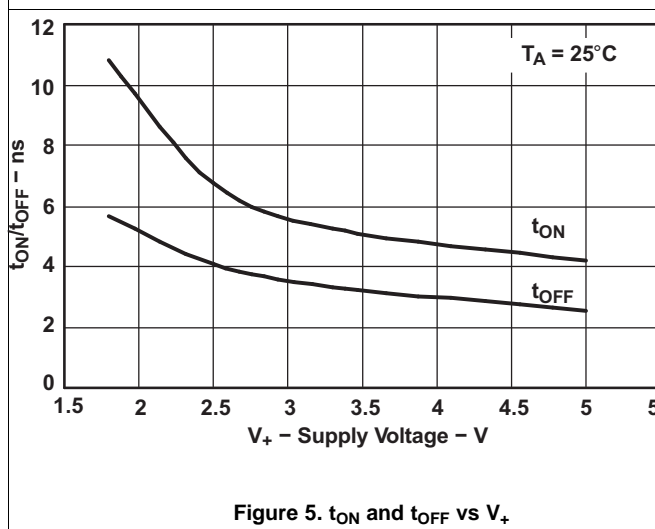
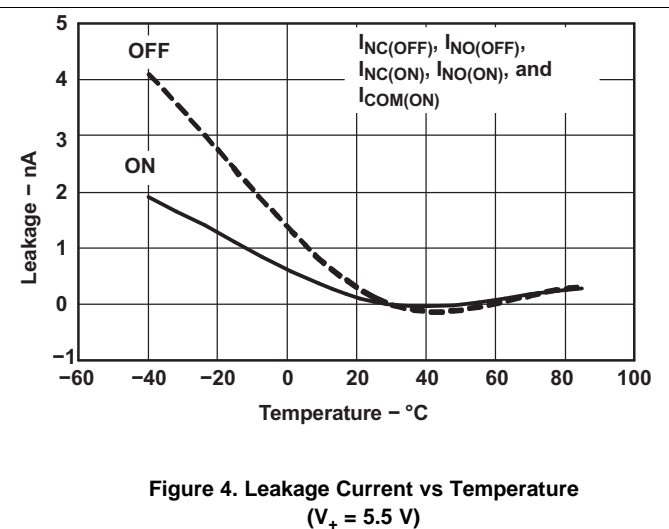
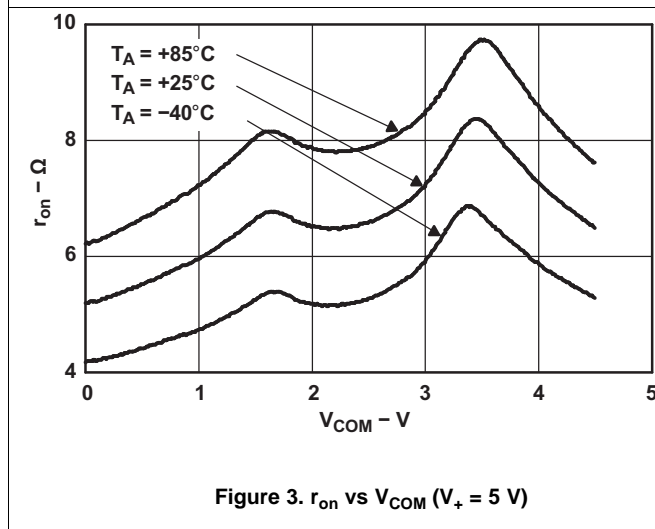
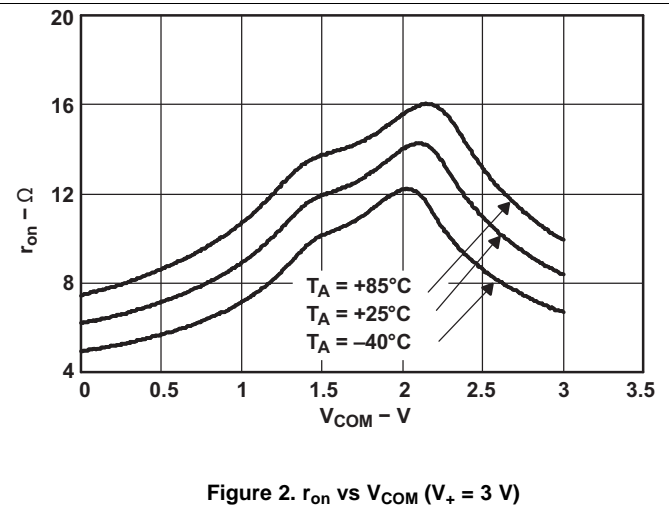
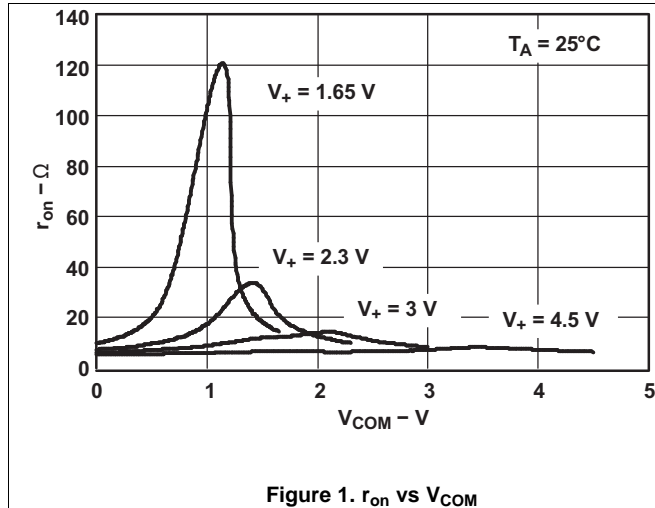
 $V_+ = 1.65\text{ V to }1.95\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP ⁽¹⁾	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{on}	ON-state resistance	$0 \leq V_{NO} \text{ or } V_{NC} \leq V_+$, $I_{COM} = -4\text{ mA}$,	Switch ON, see Figure 9	Full -40 to 125°C	1.65 V			140 180	Ω
Δr_{on}	ON-state resistance match between channels	$V_{NO} \text{ or } V_{NC} = 1.15\text{ V}$, $I_{COM} = -4\text{ mA}$,	Switch ON, see Figure 9	25°C	1.65 V		1		Ω
$r_{on(Flat)}$	ON-state resistance flatness	$0 \leq V_{NO} \text{ or } V_{NC} \leq V_+$, $I_{COM} = -4\text{ mA}$,	Switch ON, see Figure 9	25°C	1.65 V		110		Ω
$I_{NC(OFF)}, I_{NO(OFF)}$	NC, NO OFF leakage current	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$, $V_{COM} = 0 \text{ to } V_+$,	Switch OFF, see Figure 10	25°C Full	1.95 V	-1	0.05	1	μA
$I_{NC(ON)}, I_{NO(ON)}$	NC, NO ON leakage current	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$, $V_{COM} = \text{Open}$,	Switch ON, see Figure 10	25°C Full	1.95 V	-0.1		0.1	μA
$I_{COM(ON)}$	COM ON leakage current	$V_{NC} \text{ or } V_{NO} = \text{Open}$, $V_{COM} = 0 \text{ to } V_+$,	Switch ON, see Figure 10	25°C Full	1.95 V	-0.1		0.1	μA
DIGITAL INPUTS (IN12, IN2)⁽²⁾									
V_{IH}	Input logic high			Full		$V_+ \times 0.75$			V
V_{IL}	Input logic low			Full				$V_+ \times 0.25$	V
I_{IH}, I_{IL}	Input leakage current	$V_{IN} = 5.5\text{ V or }0$		25°C Full	1.95 V	-1	0.05	1	μA
DYNAMIC									
t_{ON}	Turnon time	$V_{NC} = \text{GND and } V_{NO} = V_+$ or $V_{NC} = V_+ \text{ and } V_{NO} = \text{GND}$,	$R_L = 500\ \Omega$, $C_L = 50\text{ pF}$, see Figure 12	Full -40 to 125°C	1.65 V to 1.95 V	7 5.5		24 27	ns
t_{OFF}	Turnoff time	$V_{NC} = \text{GND and } V_{NO} = V_+$ or $V_{NC} = V_+ \text{ and } V_{NO} = \text{GND}$,	$R_L = 500\ \Omega$, $C_L = 50\text{ pF}$, see Figure 12	Full -40 to 125°C	1.65 V to 1.95 V	3 2		13 16	ns
t_{BBM}	Break-before-make time	$V_{NC} = V_{NO} = V_+/2$, $R_L = 50\ \Omega$,	$C_L = 35\text{ pF}$, see Figure 13	Full	1.65 V to 1.95 V	0.5			ns
BW	Bandwidth	$R_L = 50\ \Omega$,	Switch ON, see Figure 14	25°C	1.8 V		220		MHz
O_{ISO}	OFF isolation	$R_L = 50\ \Omega$, $f = 10\text{ MHz}$,	Switch OFF, see Figure 15	25°C	1.8 V		-60		dB
X_{TALK}	Crosstalk	$R_L = 50\ \Omega$, $f = 10\text{ MHz}$,	Switch ON, see Figure 16	25°C	1.8 V		-66		dB
THD	Total harmonic distortion	$R_L = 600\ \Omega$, $C_L = 50\text{ pF}$,	$f = 600\text{ Hz to }20\text{ kHz}$, see Figure 18	25°C	1.8 V		0.015%		
SUPPLY									
I_+	Positive supply current	$V_{IN} = V_+ \text{ or GND}$,	Switch ON or OFF	25°C Full	1.95 V			1 10	μA
ΔI_+	Change in supply current	$V_{IN} = V_+ - 0.6\text{ V}$		Full	1.95 V			500	μA

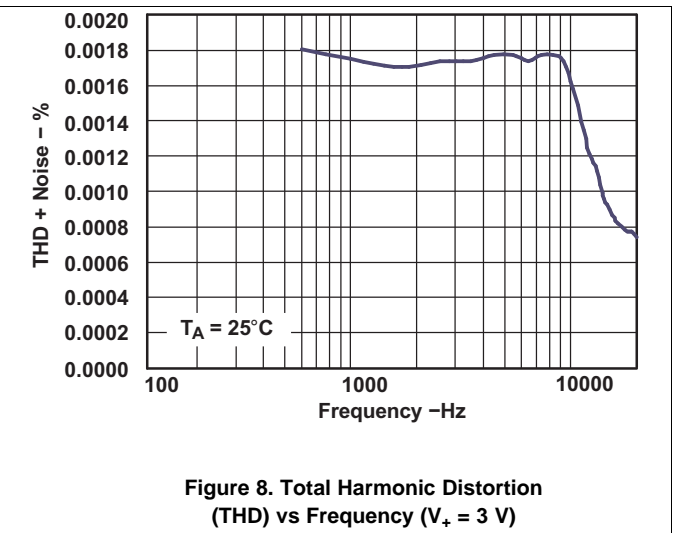
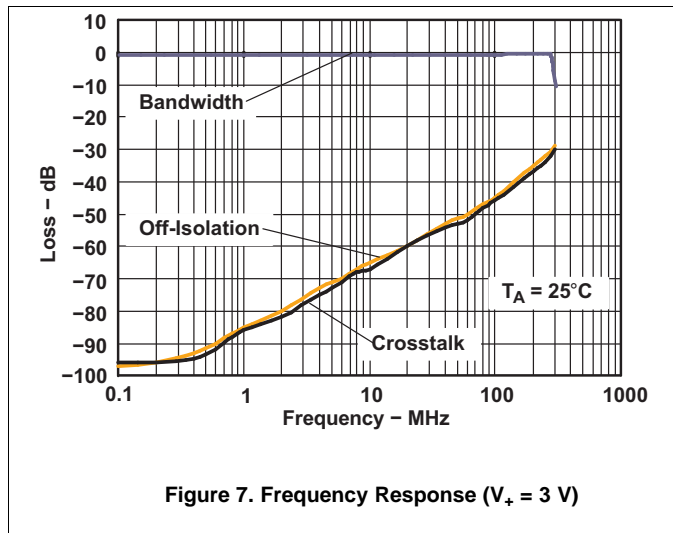
(1) $T_A = 25^\circ\text{C}$.

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

6.9 Typical Characteristics



Typical Characteristics (continued)



7 Parameter Measurement Information

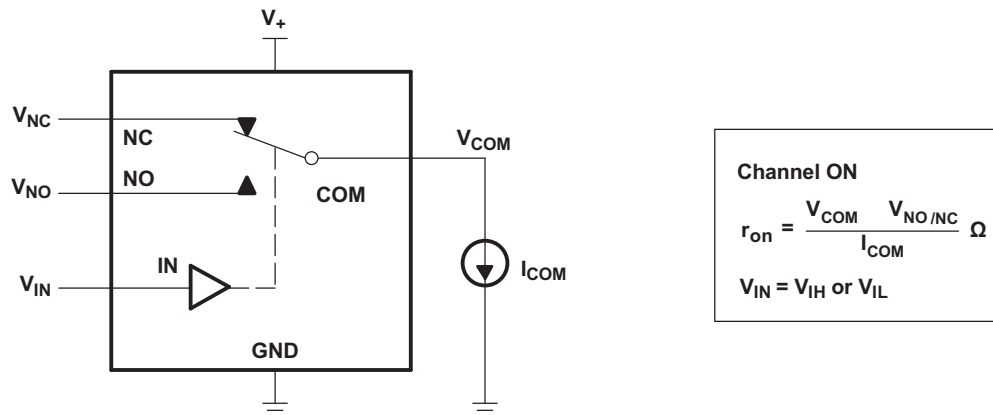


Figure 9. ON-State Resistance (r_{on})

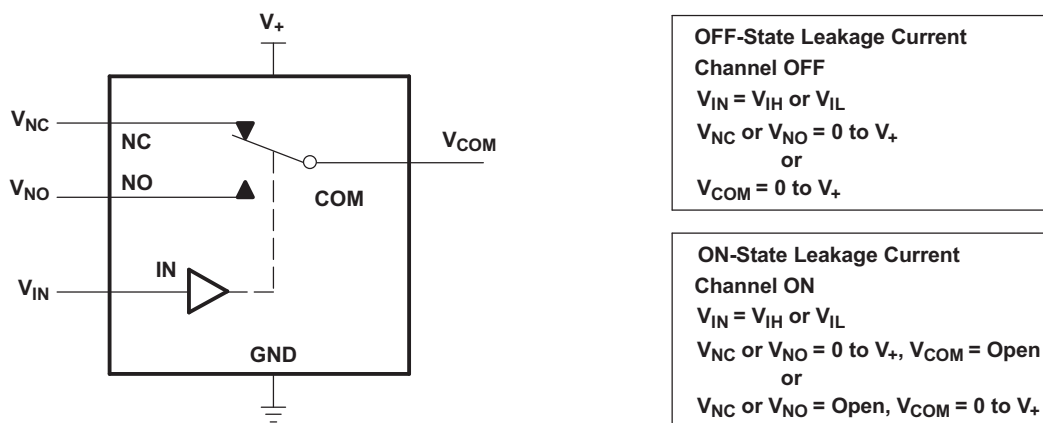


Figure 10. ON- and OFF-State Leakage Current ($I_{COM(ON)}$, $I_{NC(OFF)}$, $I_{NO(OFF)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

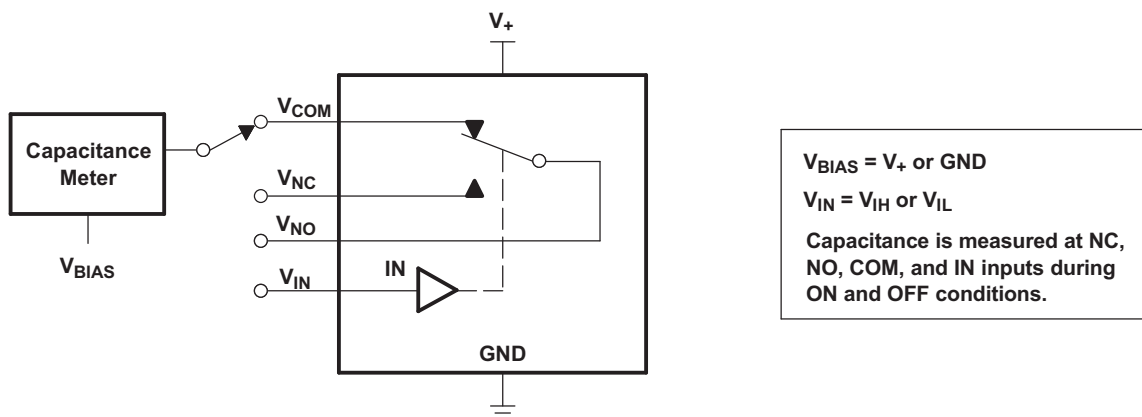


Figure 11. Capacitance (C_{IN} , $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)

Parameter Measurement Information (continued)

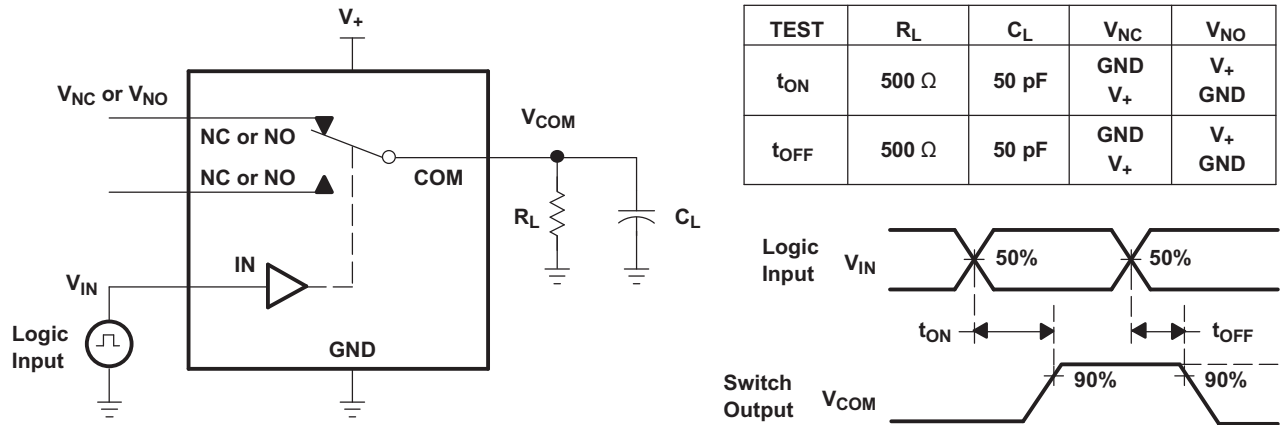


Figure 12. Turnon (t_{ON}) and Turnoff (t_{OFF}) Time

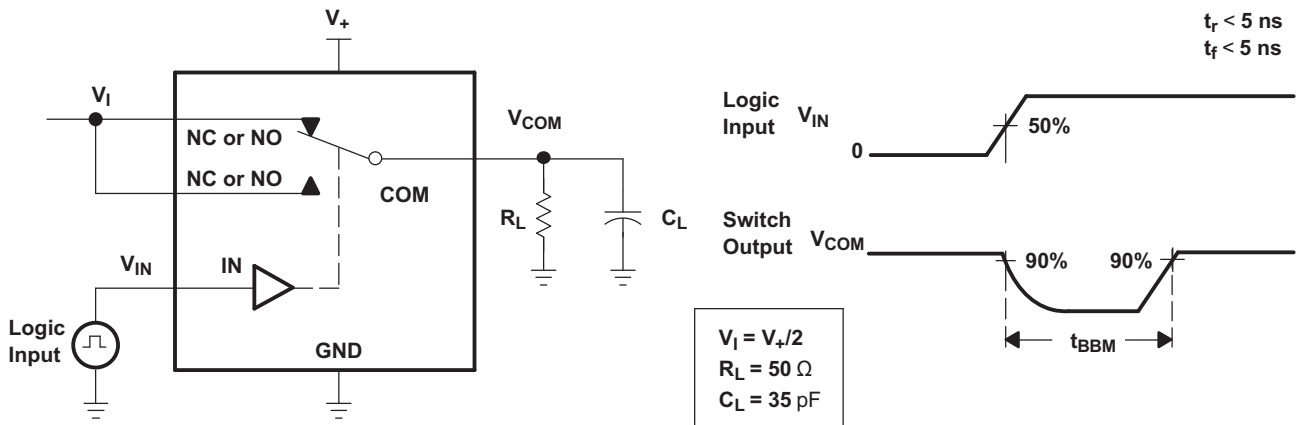


Figure 13. Break-Before-Make (t_{BBM}) Time

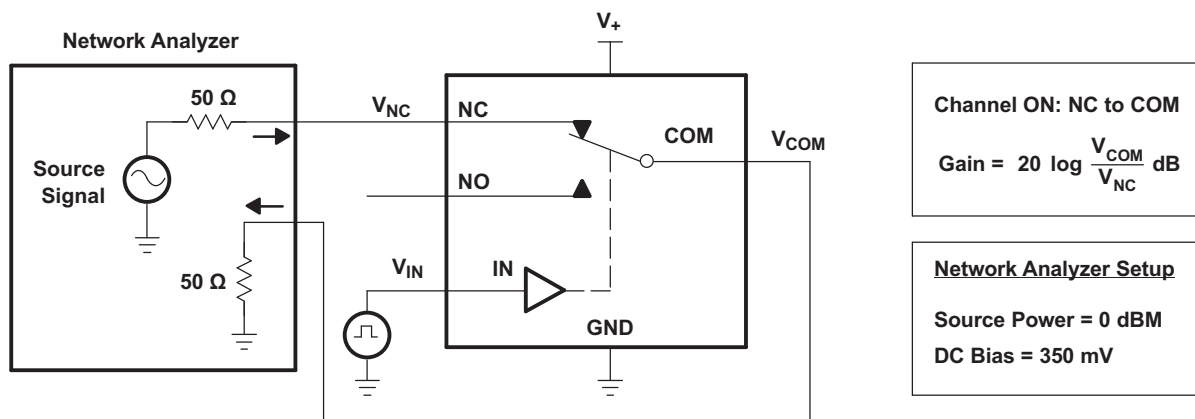


Figure 14. Frequency Response (BW)

Parameter Measurement Information (continued)

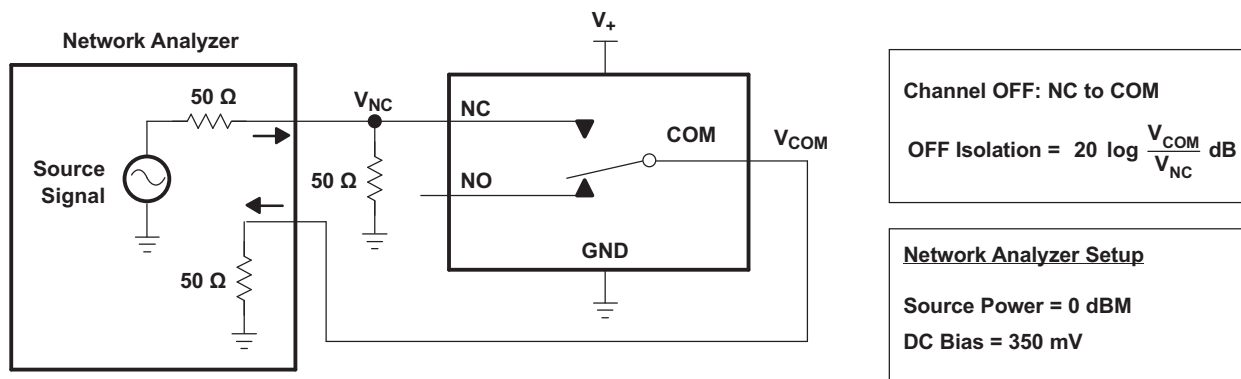


Figure 15. OFF Isolation (O_{ISO})

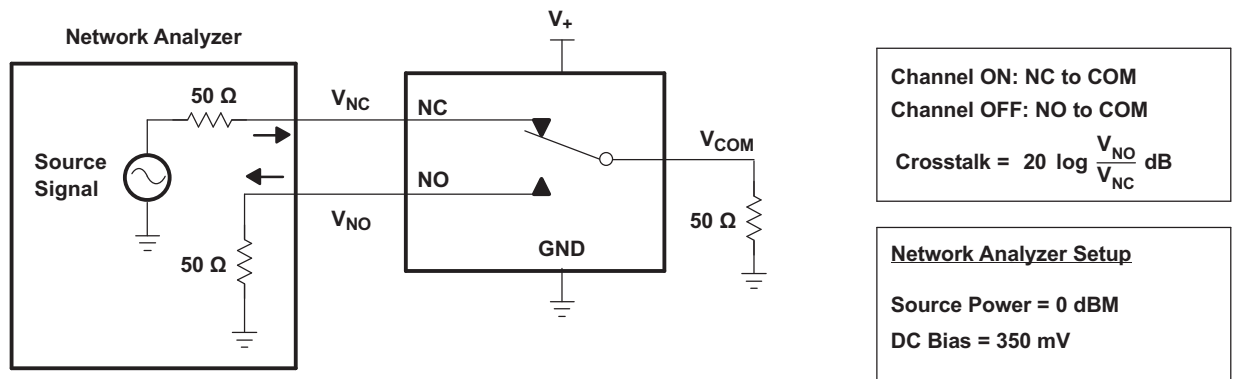


Figure 16. Crosstalk (X_{TALK})

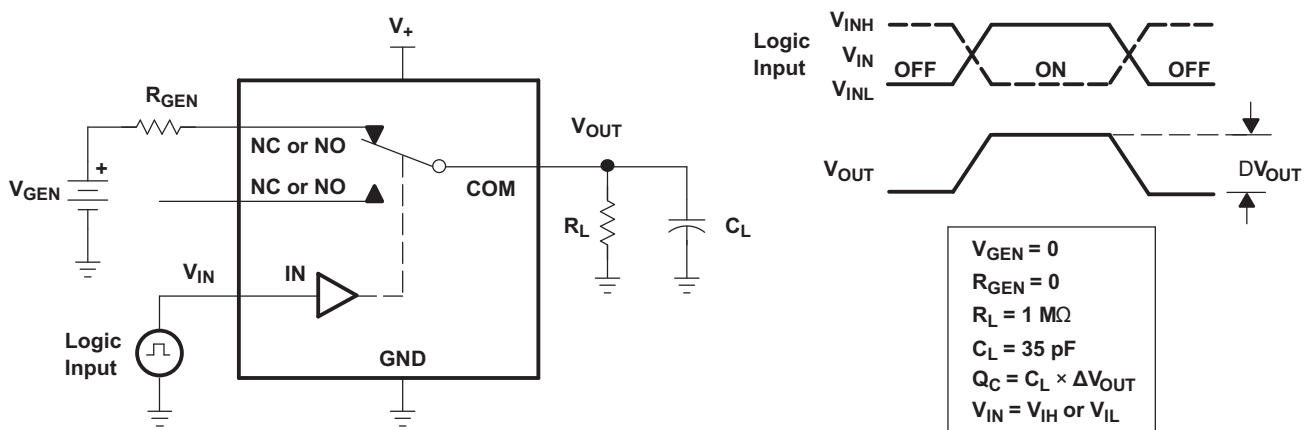


Figure 17. Charge Injection (Q_C)

Parameter Measurement Information (continued)

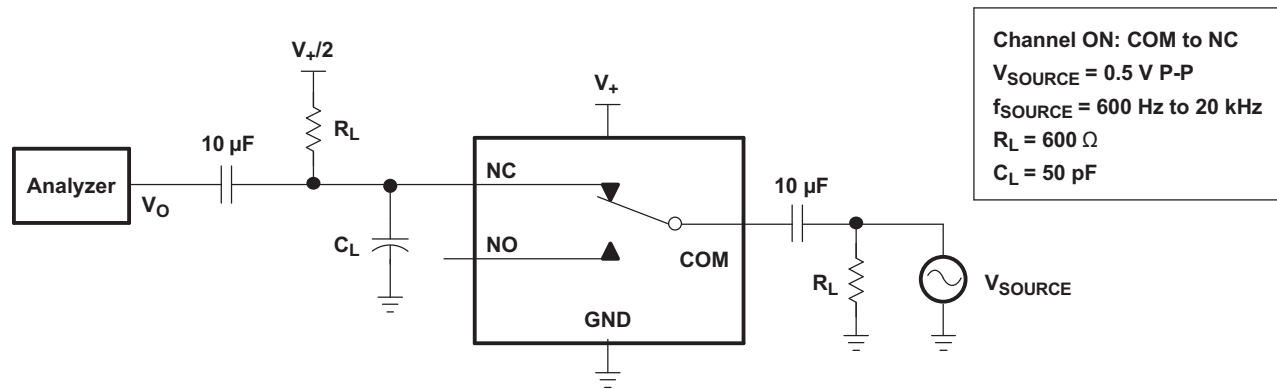


Figure 18. Total Harmonic Distortion (THD)

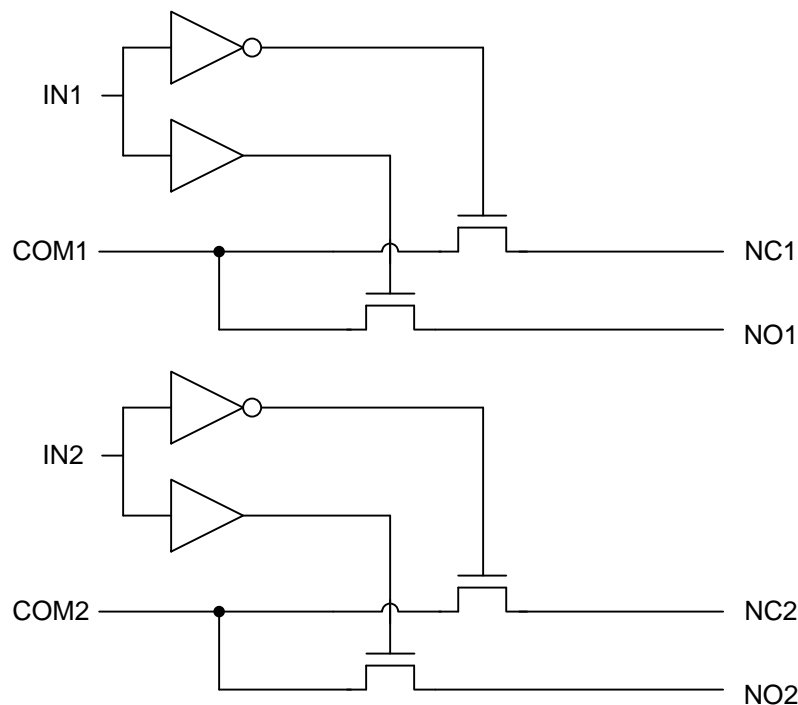
8 Detailed Description

8.1 Overview

The TS5A23157 is a dual single-pole-double-throw (SPDT) solid-state analog switch. The TS5A23157, like all analog switches, is bidirectional. When powered on, each COM pin is connected to its respective NC pin when the IN pin is low. For this device, NC stands for *normally closed* and NO stands for *normally open*. If IN is low, COM is connected to NC. If IN is high, COM is connected to NO.

The TS5A23157 is a break-before-make switch. This means that during switching, a connection is broken before a new connection is established. The NC and NO pins are never connected to each other.

8.2 Functional Block Diagram



8.3 Feature Description

The low ON-state resistance, ON-state resistance matching, and charge injection in the TS5A23157 make this switch an excellent choice for analog signals that require minimal distortion. In addition, the low THD allows audio signals to be preserved more clearly as they pass through the device.

The 1.65-V to 5.5-V operation allows compatibility with more logic levels, and the bidirectional I/Os can pass analog signals from 0 V to V_+ with low distortion. The control inputs are 5-V tolerant, allowing control signals to be present without V_{CC} .

8.4 Device Functional Modes

[Table 1](#) lists the functional modes for TS5A23157.

Table 1. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS5A3157 can be used in a variety of customer systems. The TS5A3157 can be used anywhere multiple analog or digital signals must be selected to pass across a single line.

9.2 Typical Application

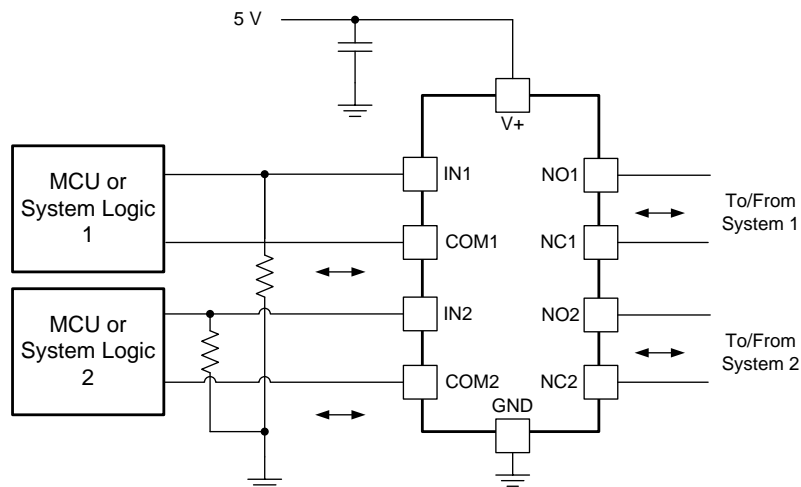


Figure 19. System Schematic for TS5A23157

9.2.1 Design Requirements

In this particular application, V_+ was 5 V, although V_+ is allowed to be any voltage specified in [Recommended Operating Conditions](#). A decoupling capacitor is recommended on the V_+ pin. See [Power Supply Recommendations](#) for more details.

9.2.2 Detailed Design Procedure

In this application, IN is, by default, pulled low to GND. Choose the resistor size based on the current driving strength of the GPIO, the desired power consumption, and the switching frequency (if applicable). If the GPIO is open-drain, use pullup resistors instead.

Typical Application (continued)

9.2.3 Application Curve

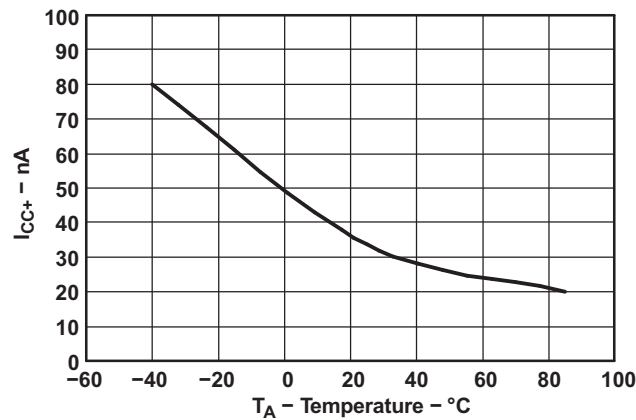


Figure 20. Power-Supply Current vs Temperature ($V_+ = 5\text{ V}$)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#).

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μF bypass capacitor is recommended. If there are multiple pins labeled V_{CC} , then a 0.01- μF or 0.022- μF capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD} , a 0.1- μF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Below figure shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

Unused switch I/Os, such as NO, NC, and COM, can be left floating or tied to GND. However, the IN pin must be driven high or low. Due to partial transistor turnon when control inputs are at threshold levels, floating control inputs can cause increased I_{CC} or unknown switch selection states.

11.2 Layout Example

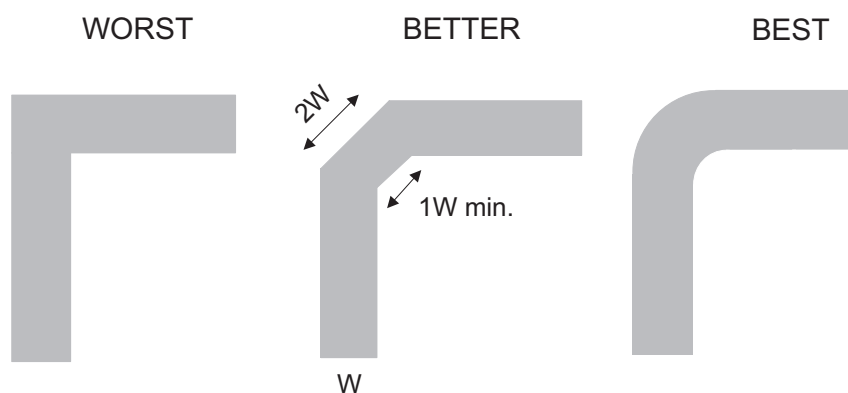


Figure 21. Trace Example

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デバイスの項目表記

表 2. パラメータの説明

記号	説明
V_{COM}	COM電圧
V_{NC}	NC電圧
V_{NO}	NO電圧
r_{on}	チャンネルがオンのときの、COMポートとNCポートの間、またはCOMポートとNOポートの間の抵抗
Δr_{on}	チャンネル間の r_{on} の差
$r_{on(flat)}$	規定の条件の範囲における、チャンネルの r_{on} の最大値と最小値との差
$I_{NC(OFF)}$	ワーストケースの入力および出力条件で、対応チャンネル(NCからCOM)がオフ状態のとき、NCポートで測定されるリーク電流
$I_{NO(OFF)}$	ワーストケースの入力および出力条件で、対応チャンネル(NOからCOM)がオフ状態のとき、NOポートで測定されるリーク電流
$I_{NC(ON)}$	対応チャンネル(NCからCOM)がオン状態、出力(COM)がオープンするとき、NCポートで測定されるリーク電流
$I_{NO(ON)}$	対応チャンネル(NOからCOM)がオン状態、出力(COM)がオープンするとき、NOポートで測定されるリーク電流
$I_{COM(ON)}$	対応チャンネル(NOからCOM、またはNCからCOM)がオン状態、出力(NCまたはNO)がオープンするとき、COMポートで測定されるリーク電流
V_{IH}	制御入力(IN)の論理HIGHの最小入力電圧
V_{IL}	制御入力(IN)の論理LOWの最大入力電圧
V_{IN}	INの電圧
I_{IH}, I_{IL}	INで測定されるリーク電流
t_{ON}	スイッチのターンオン時間。このパラメータは、規定された条件の範囲で、スイッチがオンになるときのデジタル制御(IN)信号とアナログ出力(COM/NC/NO)信号との間の伝搬遅延により測定されます。
t_{OFF}	スイッチのターンオフ時間。このパラメータは、規定された条件の範囲で、スイッチがオフになるときのデジタル制御(IN)信号とアナログ出力(COM/NC/NO)信号との間の伝搬遅延により測定されます。
t_{BBM}	Break-Before-Make時間。このパラメータは、規定された条件の範囲で、制御信号の状態が変化するときの2つの隣接するアナログ・チャンネル(NCおよびNO)の出力間の伝播遅延により測定されます。
Q_C	電荷注入は、制御(IN)入力からアナログ(NC、NO、COM)出力への、望ましくない信号のカップリングの測定値です。この値はクーロン(C)単位で、制御入力のスイッチングによって誘導される合計電荷により測定されます。電荷注入 $Q_C = C_L \times \Delta V_O$ 。ここで、 C_L は負荷容量、 ΔV_O はアナログ出力電圧の変化です。
$C_{NC(OFF)}$	対応チャンネル(NCからCOM)がオフのときのNCポートの容量
$C_{NO(OFF)}$	対応チャンネル(NCからCOM)がオフのときのNOポートの容量
$C_{NC(ON)}$	対応チャンネル(NCからCOM)がオンのときのNCポートの容量
$C_{NO(ON)}$	対応チャンネル(NCからCOM)がオンのときのNOポートの容量
$C_{COM(ON)}$	対応チャンネル(COMからNC、またはCOMからNO)がオンのときのCOMポートの容量
C_{IN}	INの容量
O_{ISO}	スイッチのオフ絶縁は、オフ状態のスイッチのインピーダンス測定値です。これは、対応チャンネル(NCからCOM、またはNOからCOM)がオフ状態のとき、特定の周波数についてdB単位で測定されます。オフ絶縁 $O_{ISO} = 20 \log(V_{NC}/V_{COM})$ dB。ここで、 V_{COM} は入力、 V_{NC} は出力です。
X_{TALK}	クロストークは、オンのチャンネルからオフのチャンネル(NCからNO、またはNOからNC)への、望ましくない信号カップリングの測定値です。この値は特定の周波数において、dB単位で測定されます。クロストーク $X_{TALK} = 20 \log(V_{NC1}/V_{NO1})$ 。ここで V_{NO1} は入力、 V_{NC1} は出力です。
BW	スイッチの帯域幅。オン状態のチャンネルのゲインがdcゲインより-3dB低くなる周波数です。ゲインは次の式で計測されます。 $20 \log(V_{NC}/V_{COM})$ dB。ここで、 V_{NC} は出力、 V_{COM} は入力です。
I_+	制御(IN)ピンが V_+ またはGNDであるときの静的消費電流
ΔI_+	これは、各制御(IN)入力が規定の電圧であるとき(V_+ またはGNDではなく)の I_+ の増分です。

表 3. 特性の概要

構成	2:1マルチプレクサ/デマルチプレクサ (2 × SPDT)
チャンネル数	2
オン抵抗(r_{on})	10Ω
チャンネル間オン抵抗ばらつき(Δr_{on})	0.15Ω
オン抵抗平坦性($r_{on(flat)}$)	4Ω
ターンオン/ターンオフ時間(t_{ON}/t_{OFF})	5.7ns/3.8ns
Break-Before-Make時間(t_{BBM})	0.5ns
電荷注入(Q_C)	7pC
帯域幅(BW)	220MHz
オフ絶縁(O_{ISO})	10MHz時に-65dB
クロストーク(XTALK)	10MHz時に-66dB
全高調波歪み(THD)	0.01%
リーク電流($I_{COM(OFF)}/I_{NC(OFF)}$)	±1μA
パッケージ・オプション	10ピンDGSおよびRSE

12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください。

- 『低速またはフローティングCMOS入力の影響』、[SCBA004](#)

12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™オンライン・コミュニティ *TIのE2E (Engineer-to-Engineer)* コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

設計サポート *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

12.4 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静電気放電に関する注意事項



これらのデバイスは、限定的なESD(静電破壊)保護機能を内蔵しています。保存時または取り扱い時は、MOSゲートに対する静電破壊を防止するために、リード線同士をショートさせておくか、デバイスを導電フォームに入れる必要があります。

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A23157DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(3BR, JBR)	Samples
TS5A23157DGSRE4	LIFEBUY	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JBR	
TS5A23157DGSRG4	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JBR	Samples
TS5A23157DGST	LIFEBUY	VSSOP	DGS	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JBR	
TS5A23157RSER	ACTIVE	UQFN	RSE	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JBO	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TS5A23157 :

- Automotive : [TS5A23157-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A23157DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TS5A23157DGSRE4	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TS5A23157DGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TS5A23157RSER	UQFN	RSE	10	3000	180.0	9.5	1.7	2.2	0.75	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A23157DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TS5A23157DGSRE4	VSSOP	DGS	10	2500	346.0	346.0	35.0
TS5A23157DGST	VSSOP	DGS	10	250	203.0	203.0	35.0
TS5A23157RSER	UQFN	RSE	10	3000	189.0	185.0	36.0

DGS0010A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4221984/A 05/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

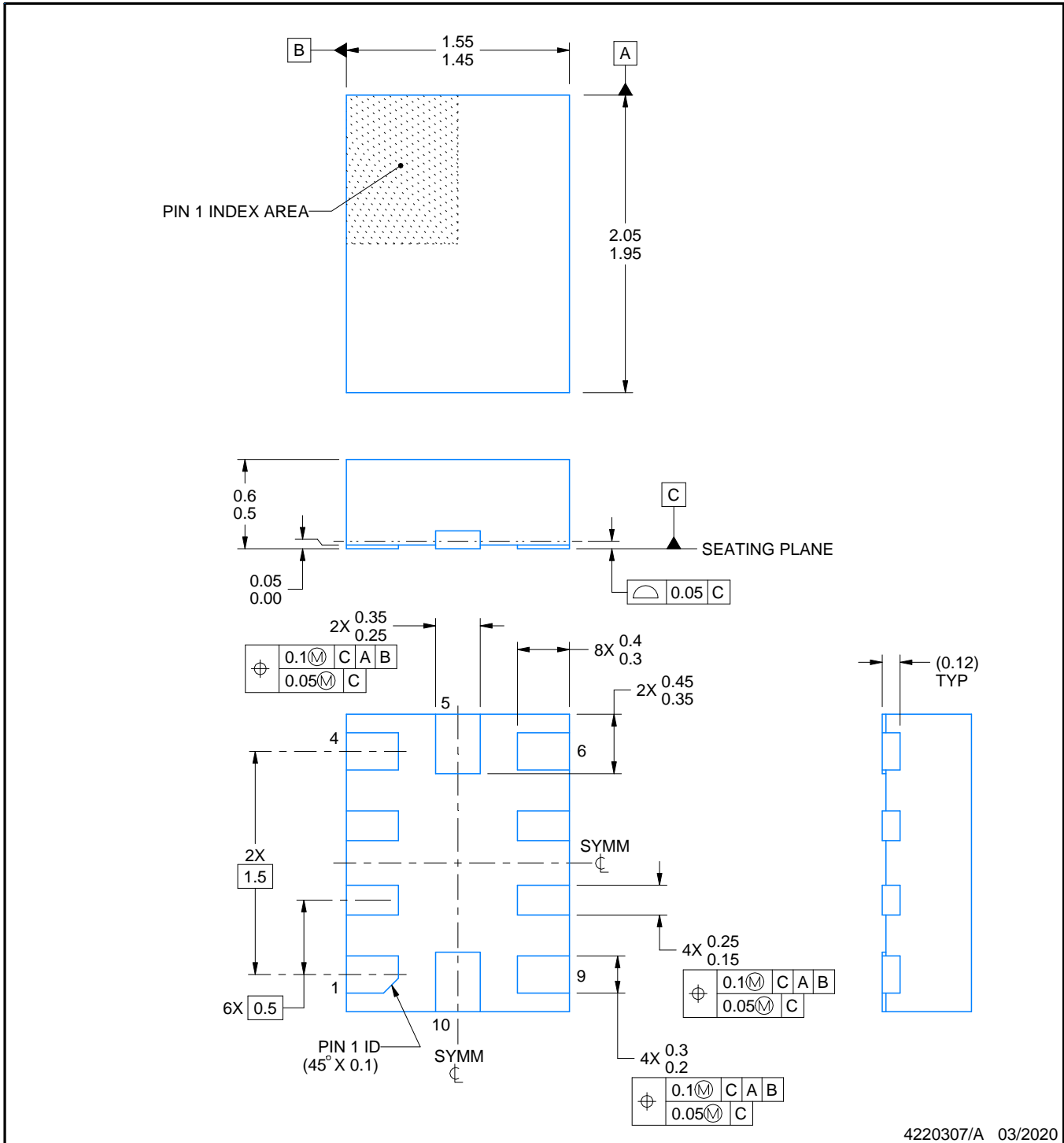
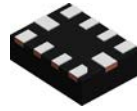


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220307/A 03/2020

NOTES:

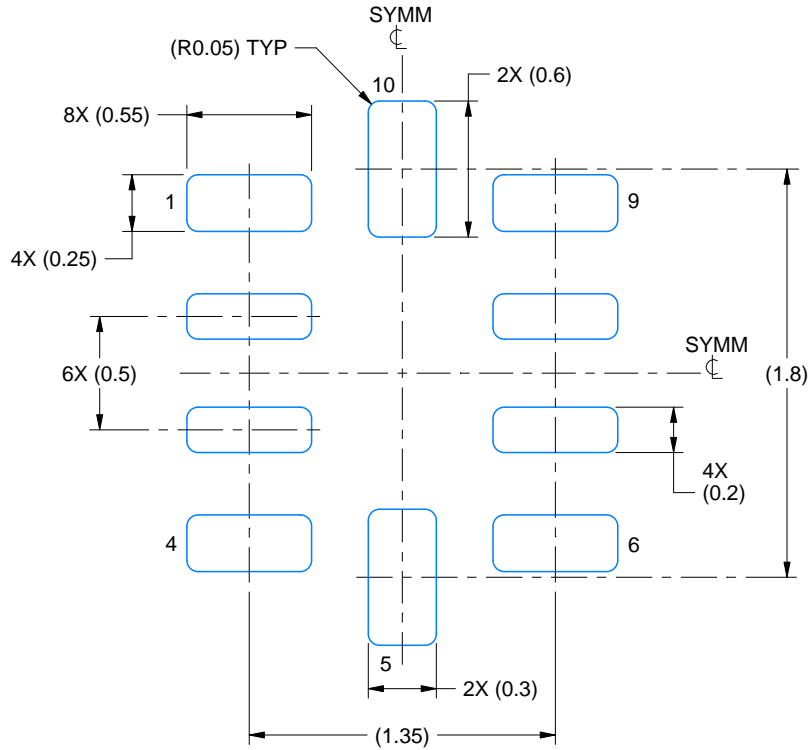
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

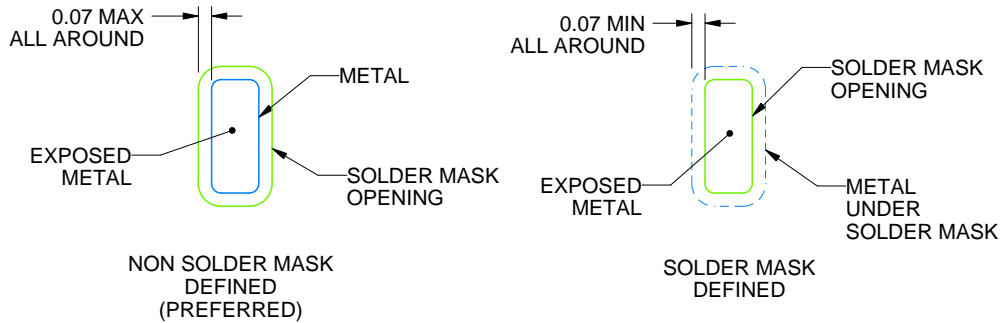
RSE0010A

UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

4220307/A 03/2020

NOTES: (continued)

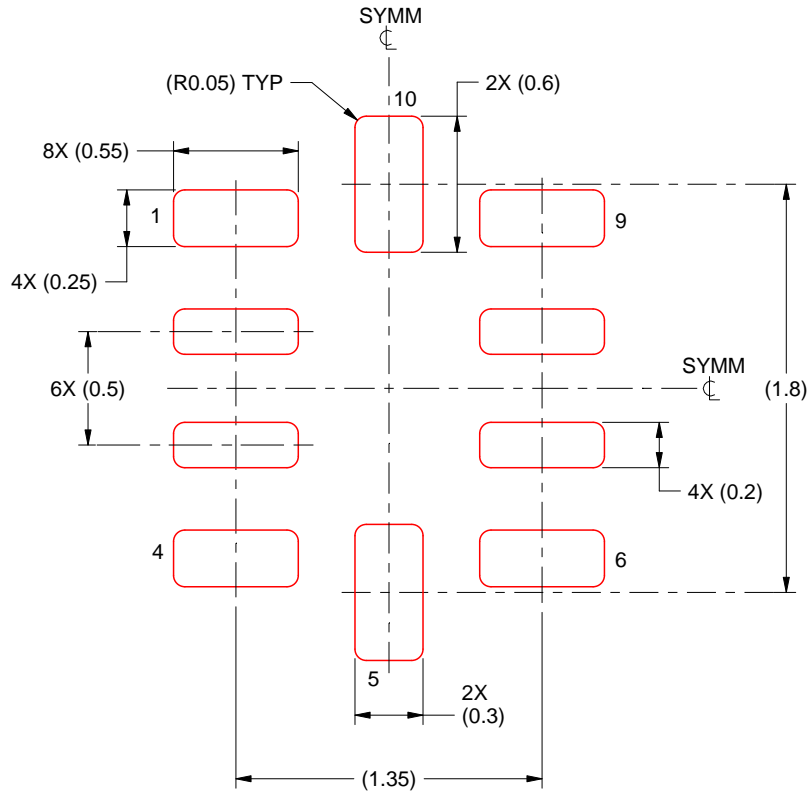
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RSE0010A

UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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