TS5A3159A 1Ω SPDTアナログ・スイッチ 5Vおよび3.3Vシングル・チャネル2:1マルチプレクサ/デマルチプレクサ

1 特長

- Break-Before-Makeスイッチングを規定
- パワーダウン・モードでの絶縁、V_+ = 0
- TS5A3159デバイスと端子互換
- 低いオン抵抗(1Ω)
- 制御入力は5.5V許容
- 低い電荷注入
- 非常に優れたオン抵抗マッチング
- 低い全高調波歪(THD)
- 1.65V～5.5Vの単電源で動作
- JESD 78、Class II準拠で100mA超のラッチアップ性能
- ESD性能はJESDに準拠しテスト済み
  - 人体モデルで2000V (A114-B、クラスII)
  - 1000V、荷電デバイス・モデル(C101)

2 アプリケーション

- 携帯電話
- 携帯情報端末
- ポータブル機器
- オーディオおよびビデオ信号のルーティング
- 低電圧のデータ収集システム
- 通信用回路
- モデム
- ハードディスク
- コンピュータ・ペリフェラル
- ワイヤレス端末およびペリフェラル

3 概要

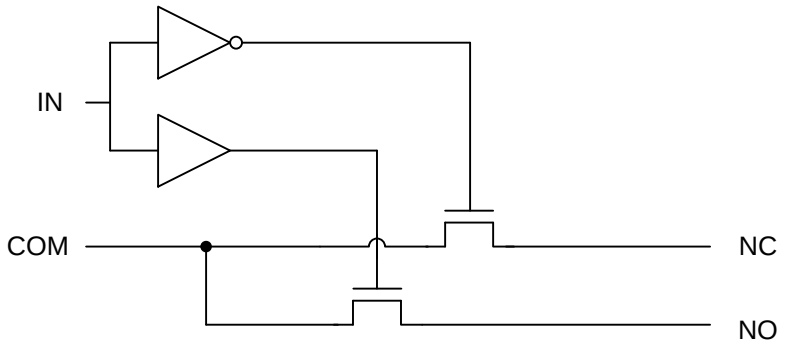
TS5A3159Aデバイスは単極双投(SPDT)アナログ・スイッチで、1.65V～5.5Vで動作するよう設計されています。このデバイスはオン抵抗が低く、オン抵抗マッチングが非常に優れており、Break-Before-Make機能によってチャネル間の信号転送時に信号が歪むのを防ぎます。このデバイスは、全高調波歪(THD)性能が非常に優れており、極めて低消費電力です。これらの特長から、このデバイスは携帯用オーディオ・アプリケーションに適しています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TS5A3159ADBVR	SOT-23 (6)	2.90mm×1.60mm
TS5A3159ADCKR	SC70 (6)	2.00mm×1.25mm
TS5A3159AYZPR	DSBGA (6)	1.41mm×0.91mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

ブロック図



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision E (November 2015) から **Revision F** に変更 **Page**

- Changed the YZP package From: 8 Pins To: 6 Pins in the *Thermal Information* table ... 4

Revision D (June 2015) から **Revision E** に変更 **Page**

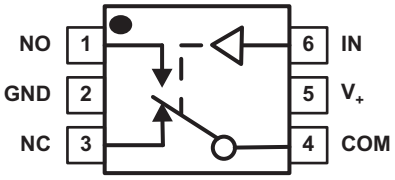
- Changed Pin Descriptions ... 3

Revision C (May 2010) から **Revision D** に変更 **Page**

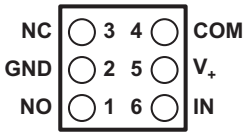
- 「*アプリケーション*」セクション、「*製品情報*」表、「*ピン機能*」表、「*ESD定格*」表、「*熱に関する情報*」表、「*代表的特性*」セクション、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1

5 Pin Configuration and Functions

DBV or DCK Packages
6-Pin SOT-23 or SC-70
Top View



YZP Packages
6-Pin DSBGA
Bottom View



NO – Normally open

NC – Normally closed

Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOT-23, SC-70	DSBGA		
COM	4	C2	I/O	Common switch port
GND	2	B1	—	Ground
IN	6	A2	I/O	Switch select. High = COM connected to NO; Low = COM connected to NC
NC	3	C1	I/O	Normally closed switched port
NO	1	A1	—	Normally open switch port
V+	5	B2	I	Power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
V_+	Supply voltage(3)		–0.5	6.5	V
V_{NO}, V_{NC}, V_{COM}	Analog voltage(3)(4)(5)		–0.5	V_+ + 0.5	V
I_K	Analog port diode current	V_{NC}, V_{NO}, V_{COM} < 0	–50		mA
I_{NO}, I_{NC}, I_{COM}	ON-state switch current	V_{NO}, V_{NC}, V_{COM} = 0 to V_+	–200	200	mA
	ON-state peak switch current(6)		–400	400	mA
V_I	Digital input voltage(3)(4)		–0.5	6.5	V
I_{IK}	Digital input clamp current	V_I < 0	–50		mA
I_+	Continuous current through V_+			100	mA
I_{GND}	Continuous current through GND		–100	100	mA
T_A	Absolute maximum operating temperature(7)	DBV or DCK package		150	°C
		YZP package		125	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) Pulse at 1-ms duration <10% duty cycle.
(7) The lifetime of the device will be reduced if the device operates continually at this temperature.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Switch input/output voltage	0	V_+	V
V+	Supply voltage	1.65	5.5	V
V_I	Control input voltage	0	5.5	V
T_A	Operating temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TS5A3159A			UNIT
		DBV (SOT-23)	DCK (SC-70)	YZP (DSBGA)	
		6 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165	259	123	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics for 5-V Supply

V_+ = 4.5 V to 5.5 V, T = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal					0		V_+	V
r_{peak}	Peak ON resistance	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –100 mA,	Switch on, see Figure 14	25°C	4.5 V		0.8	1.1	Ω
				Full				1.5	
r_{on}	ON-state resistance	V_{NO} or V_{NC} = 2.5 V, I_{COM} = –100 mA,	Switch on, see Figure 14	25°C	4.5 V		0.7	0.9	Ω
				Full				1.1	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 2.5 V, I_{COM} = –100 mA,	Switch on, see Figure 14	25°C	4.5 V		0.05	0.1	Ω
				Full				0.1	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –100 mA,	Switch on, see Figure 14	25°C	4.5 V		0.15		Ω
		V_{NO} or V_{NC} = 1 V, 1.5 V, 2.5 V, I_{COM} = –100 mA,	Switch on, see Figure 14	25°C			0.1	0.25	
				Full				0.25	
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 1 V, V_{COM} = 1 V to 4.5 V, or V_{NC} or V_{NO} = 4.5 V, V_{COM} = 1 V to 4.5 V,	Switch off, see Figure 15	25°C	5.5 V	–20	2	20	nA
				Full		–100		100	
$I_{NC(PWROFF)}$, $I_{NO(PWROFF)}$		V_{NC} or V_{NO} = 0 to 5.5 V, V_{COM} = 5.5 V to 0,	Switch off, see Figure 15	25°C	0 V	–1	0.2	1	µA
				Full		–20		20	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 1 V, V_{COM} = Open, or V_{NC} or V_{NO} = 4.5 V, V_{COM} = Open,	Switch on, see Figure 16	25°C	5.5 V	–20	2	20	nA
				Full		–100		100	
$I_{COM(PWROFF)}$	COM OFF leakage current	V_{NC} or V_{NO} = 0 to 5.5 V, V_{COM} = 5.5 V to 0,	Switch off, see Figure 15	25°	0 V	–1	0.1	1	µA
				Full		–20		20	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 1 V, or V_{NC} or V_{NO} = Open, V_{COM} = 4.5 V,	Switch on, see Figure 16	25°C	5.5 V	–20	2	20	nA
				Full		–100		100	
DIGITAL INPUT (IN)									
V_{IH}	Input logic high			Full		2.4		5.5	V
V_{IL}	Input logic low			Full		0		0.8	
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	5.5 V	–2		2	nA
				Full		100		100	
DYNAMIC									
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 18	25°C	5 V	1	12	30	ns
				Full	4.5 V to 5.5 V	1		35	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 18	25°C	5 V	1	5	20	ns
				Full	4.5 V to 5.5 V	1		30	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 19	25°C	5 V		6		ns
				Full	4.5 V to 5.5 V	1		20	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, see Figure 23	25°C	5 V		–20		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_+ or GND,	Switch off, see Figure 17	25°C	5 V		18		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_+ or GND,	Switch on, see Figure 17	25°C	5 V		55		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND,	Switch on, see Figure 17	25°C	5 V		55		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See Figure 17	25°C	5 V		2		pF
BW	Bandwidth	R_L = 50 Ω,	Switch on, see Figure 20	25°C	5 V		100		MHz

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics for 5-V Supply (continued)

V_+ = 4.5 V to 5.5 V, T = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
O_{ISO}	Off isolation	R_L = 50 Ω, f = 1 MHz,	Switch off, see Figure 21	25°C	5 V		–64		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch on, see Figure 22	25°C	5 V		–64		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 200 Hz to 20 kHz, see Figure 24	25°C	5 V		0.004%		
SUPPLY									
I_+	Positive supply current	V_I = V_+ or GND,	Switch on or off	25°C	5.5 V		10	50	nA
				Full				500	

6.6 Electrical Characteristics for 3.3-V Supply

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{peak}	Peak ON resistance	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –100 mA,	Switch on, See Figure 14	25°C	3 V		1.3	1.6	Ω
				Full				2	
r_{on}	ON-state resistance	V_{NO} or V_{NC} = 2 V, I_{COM} = –100 mA,	Switch on, See Figure 14	25°C	3 V		1.2	1.5	Ω
				Full				1.7	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch on, See Figure 14	25°C	3 V		0.1	0.15	Ω
				Full				0.15	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –100 mA,	Switch on, See Figure 14	25°C	3 V		0.2		Ω
		V_{NO} or V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch on, See Figure 14	25°C			0.15	0.3	
				Full				0.3	
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO off leakage current	V_{NC} or V_{NO} = 1 V, V_{COM} = 1 V to 3 V, or V_{NC} or V_{NO} = 3 V, V_{COM} = 1 V to 3 V,	Switch off, See Figure 15	25°C	3.6 V	–20	2	20	nA
				Full		–50		50	
$I_{NC(PWROFF)}$, $I_{NO(PWROFF)}$		V_{NC} or V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,	Switch off, See Figure 15	25°C	0 V	–1	0.2	1	µA
				Full		–15		15	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO on leakage current	V_{NC} or V_{NO} = 1 V, V_{COM} = Open, or V_{NC} or V_{NO} = 3 V, V_{COM} = Open,	Switch on, See Figure 16	25°C	3.6 V	–10	2	10	nA
				Full		–20		20	
$I_{COM(PWROFF)}$	COM off leakage current	V_{NC} or V_{NO} = 3.6 V to 0, V_{COM} = 0 to 3.6 V,	Switch off, See Figure 15	25°	0 V	–1	0.2	1	µA
				Full		–15		15	
$I_{COM(ON)}$	COM on leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 1 V, or V_{NC} or V_{NO} = Open, V_{COM} = 3 V,	Switch on, See Figure 16	25°C	3.6 V	–10	2	10	nA
				Full		–20		20	
DIGITAL INPUT (IN)									
V_{IH}	Input logic high			Full		2.4		5.5	V
V_{IL}	Input logic low			Full		0		0.8	
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	3.6 V	–2		2	nA
				Full		–100		100	
DYNAMIC									
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	3.3 V	5	16	35	ns
				Full	3 V to 3.6 V	3		50	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	3.3 V	1	9	20	ns
				Full	3 V to 3.6 V	1		30	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics for 3.3-V Supply (continued)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 19	25°C	3.3 V		9		ns
				Full	3 V to 3.6 V	1		40	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 23	25°C	3.3 V		–11		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_+ or GND,	Switch off, See Figure 17	25°C	3.3 V		18		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_+ or GND,	Switch on, See Figure 17	25°C	3.3 V		55		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND,	Switch on, See Figure 17	25°C	3.3 V		55		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See Figure 17	25°C	3.3 V		2		pF
BW	Bandwidth	R_L = 50 Ω,	Switch on, See Figure 20	25°C	3.3 V		100		MHz
O_{ISO}	Off isolation	R_L = 50 Ω, f = 1 MHz,	Switch off, See Figure 21	25°C	3.3 V		–64		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch on, See Figure 22	25°C	3.3 V		–64		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 24	25°C	3.3 V		0.01%		
SUPPLY									
I_+	Positive supply current	V_I = V_+ or GND,	Switch on or off	25°C	3.6 V		10	25	nA
				Full				100	

6.7 Electrical Characteristics for 2.5-V Supply

V_+ = 2.3 V to 2.7, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{peak}	Peak ON resistance	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –8 mA,	Switch on, See Figure 14	25°C	2.3 V		1.8	2.5	Ω
				Full				2.7	
r_{on}	ON-state resistance	V_{NO} or V_{NC} = 1.8 V, I_{COM} = –8 mA,	Switch on, See Figure 14	25°C	2.3 V		1.5	2	Ω
				Full				2.4	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 1.8 V, I_{COM} = –8 mA,	Switch on, See Figure 14	25°C	2.3 V		0.15	0.2	Ω
				Full				0.2	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –8 mA,	Switch on, See Figure 14	25°C	2.3 V		0.6		Ω
		V_{NO} or V_{NC} = 0.8 V, 1.8 V, I_{COM} = –8 mA,	Switch on, See Figure 14	25°C			0.6	1	
				Full				1	
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 0.5 V, V_{COM} = 0.5 V to 2.3 V, or V_{NC} or V_{NO} = 2.3 V, V_{COM} = 0.5 V to 2.3 V,	Switch off, See Figure 15	25°C	2.7 V	–20	2	20	nA
				Full		–50		50	
$I_{NC(PWROFF)}$, $I_{NO(PWROFF)}$		V_{NC} or V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,	Switch off, See Figure 15	25°C	0 V	–1	0.1	1	µA
				Full		–10		10	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 0.5 V, V_{COM} = Open, or V_{NC} or V_{NO} = 2.2 V, V_{COM} = Open,	Switch on, See Figure 16	25°C	2.7 V	–10	2	10	nA
				Full		–20		20	
$I_{COM(PWROFF)}$	COM OFF leakage current	V_{NC} or V_{NO} = 2.7 V to 0, V_{COM} = 0 to 2.7 V,	Switch off, See Figure 15	25°	0 V	–1	0.1	10	µA
				Full		–10		20	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 0.5 V, or V_{NC} or V_{NO} = Open, V_{COM} = 2.2 V,	Switch on, See Figure 16	25°C	2.7 V	–10	2	10	nA
				Full		–20		20	
DIGITAL INPUT (IN)									
V_{IH}	Input logic high			Full		1.8		5.5	V
V_{IL}	Input logic low			Full		0		0.6	
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	2.7 V	–2		2	nA
				Full		20		20	
DYNAMIC									
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	2.5 V	5	22	40	ns
				Full	2.3 V to 2.7 V	5		50	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	2.5 V	2	6	35	ns
				Full	2.3 V to 2.7 V	2		50	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 19	25°C	2.5 V	2	13	35	ns
				Full	2.3 V to 2.7 V	2		45	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 23	25°C	2.5 V		–7		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_+ or GND,	Switch off, See Figure 17	25°C	2.5 V		18		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_+ or GND,	Switch on, See Figure 17	25°C	2.5 V		55		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND,	Switch on, See Figure 17	25°C	2.5 V		55		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See Figure 17	25°C	2.5 V		2		pF
BW	Bandwidth	R_L = 50 Ω,	Switch on, See Figure 20	25°C	2.5 V		100		MHz

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics for 2.5-V Supply (continued)

V_+ = 2.3 V to 2.7, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
O_{ISO}	Off isolation	R_L = 50 Ω, f = 1 MHz,	Switch off, See Figure 21	25°C	2.5 V		–64		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch on, See Figure 22	25°C	2.5 V		–64		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 24	25°C	2.5 V		0.02%		
SUPPLY									
I_+	Positive supply current	V_I = V_+ or GND,	Switch on or off	25°C	2.7 V		10	20	nA
				Full				50	

6.8 Electrical Characteristics for 1.8-V Supply

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{peak}	Peak ON resistance	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –2 mA,	Switch on, See Figure 14	25°C	1.65 V		5		Ω
				Full				15	
r_{on}	ON-state resistance	V_{NO} or V_{NC} = 1.5 V, I_{COM} = –2 mA,	Switch on, See Figure 14	25°C	1.65 V		2	2.5	Ω
				Full				3.5	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 1.5 V, I_{COM} = –2 mA,	Switch on, See Figure 14	25°C	1.65 V		0.15	0.4	Ω
				Full				0.4	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –8 mA,	Switch on, See Figure 14	25°C	1.65 V		5		Ω
		V_{NO} or V_{NC} = 0.6 V, 1.5 V, I_{COM} = –2 mA,	Switch on, See Figure 14	25°C			4.5		
				Full					
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 0.3 V, V_{COM} = 0.3 V to 1.65 V, or V_{NC} or V_{NO} = 1.65 V, V_{COM} = 0.3 V to 1.65 V,	Switch off, See Figure 15	25°C	1.95 V	–5	2	5	nA
				Full		–20		20	
$I_{NC(PWROFF)}$ $I_{NO(PWROFF)}$		V_{NC} or V_{NO} = 0 to 1.95 V, V_{COM} = 1.95 V to 0,	Switch off, See Figure 15	25°C	0 V	–1	0.1	1	µA
				Full		–5		5	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 0.3 V, V_{COM} = Open, or V_{NC} or V_{NO} = 1.65 V, V_{COM} = Open,	Switch on, See Figure 16	25°C	1.95 V	–5	2	5	nA
				Full		–20		20	
$I_{COM(PWROFF)}$	COM OFF leakage current	V_{NC} or V_{NO} = 1.95 V to 0, V_{COM} = 0 to 1.95 V,	Switch off, See Figure 15	25°	0 V	–1	0.1	7	µA
				Full		–5		5	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 0.3 V, or V_{NC} or V_{NO} = Open, V_{COM} = 1.65 V,	Switch on, See Figure 16	25°C	1.95 V	–5	2	5	nA
				Full		–20		20	
DIGITAL INPUT (IN)									
V_{IH}	Input logic high			Full		1.5		5.5	V
V_{IL}	Input logic low			Full		0		0.6	
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	1.95 V	–2		2	nA
				Full		20		20	
DYNAMIC									
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	1.8 V	10	35	70	ns
				Full	1.65 V to 1.95 V	10		75	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics for 1.8-V Supply (continued)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	1.8 V	2	15	40	ns
				Full	1.65 V to 1.95 V	2		50	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 19	25°C	1.8 V		22		ns
				Full	1.65 V to 1.95 V	2		70	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 23	25°C	1.8 V		–4		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_+ or GND,	Switch off, See Figure 17	25°C	1.8 V		18		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_+ or GND,	Switch on, See Figure 17	25°C	1.8 V		55		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND,	Switch on, See Figure 17	25°C	1.8 V		55		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See Figure 17	25°C	1.8 V		2		pF
BW	Bandwidth	R_L = 50 Ω,	Switch on, See Figure 20	25°C	1.8 V		105		MHz
O_{ISO}	Off isolation	R_L = 50 Ω, f = 1 MHz,	Switch off, See Figure 21	25°C	1.8 V		64		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch on, See Figure 22	25°C	1.8 V		64		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 24	25°C	1.8 V		0.06%		
SUPPLY									
I_+	Positive supply current	V_I = V_+ or GND,	Switch on or off	25°C	1.95 V		5	15	µA
				Full				50	

6.9 Typical Characteristics

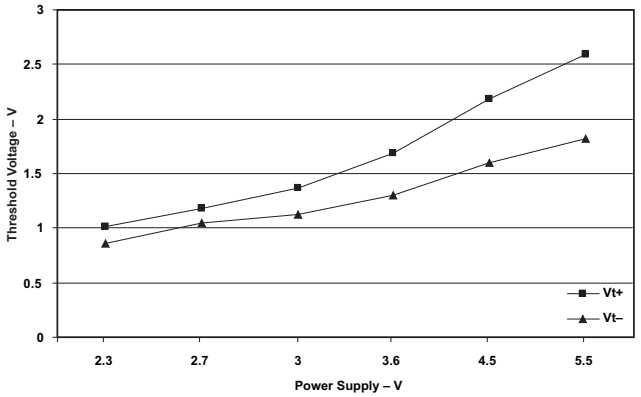


Figure 1. Logic Threshold vs Power Supply

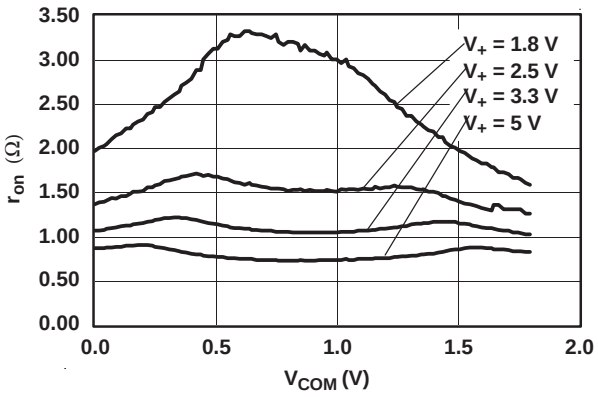


Figure 2. r_{on} vs V_{COM}

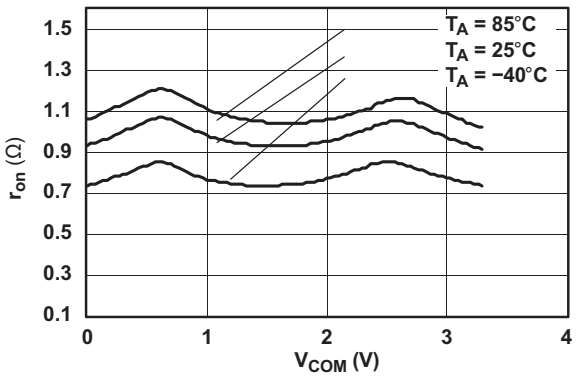


Figure 3. r_{on} vs V_{COM} (V_+ = 3.3 V)

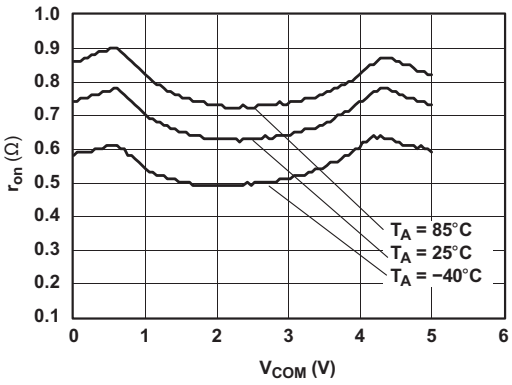


Figure 4. r_{on} vs V_{COM} (V_+ = 5 V)

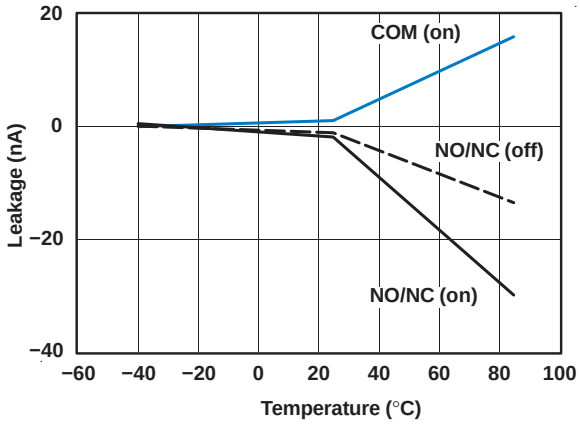


Figure 5. Leakage Current vs Temperature (V_+ = 3.3 V)

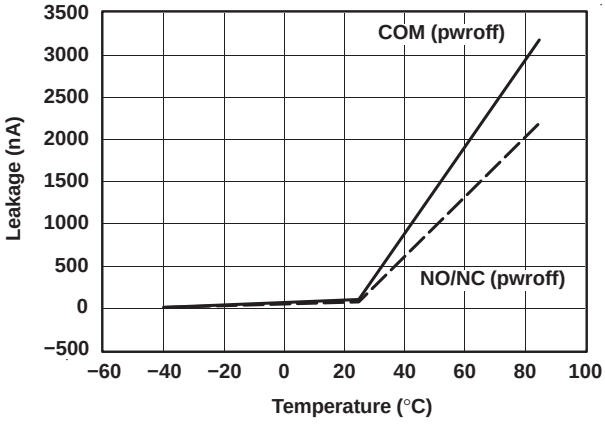


Figure 6. Leakage Current vs Temperature (V_+ = 5 V)

Typical Characteristics (continued)

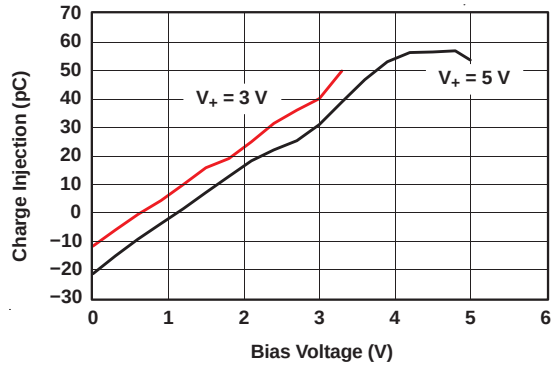


Figure 7. Charge Injection vs Bias Voltage

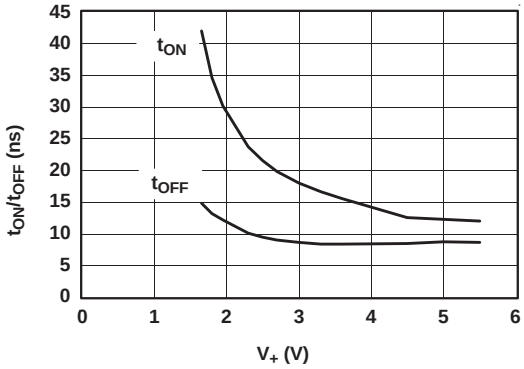


Figure 8. t_{ON} and t_{OFF} vs Supply Voltage

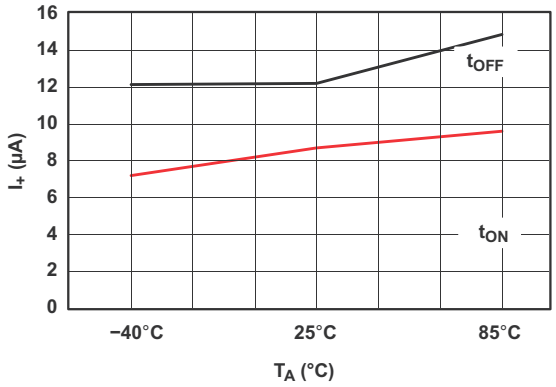


Figure 9. I_+ vs Temperature

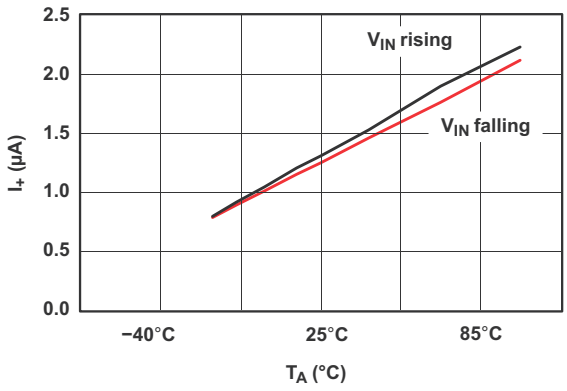


Figure 10. I_+ vs Temperature

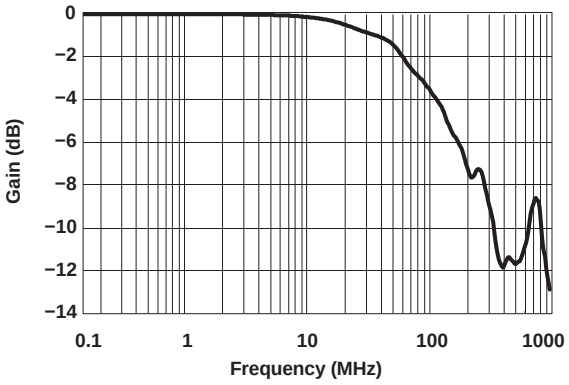


Figure 11. Bandwidth (V_+ = 5 V)

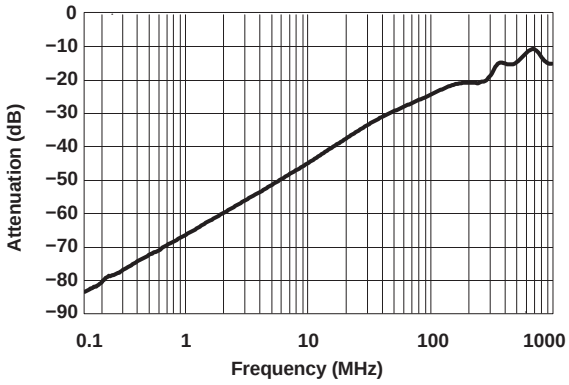


Figure 12. Attenuation vs Frequency

Typical Characteristics (continued)

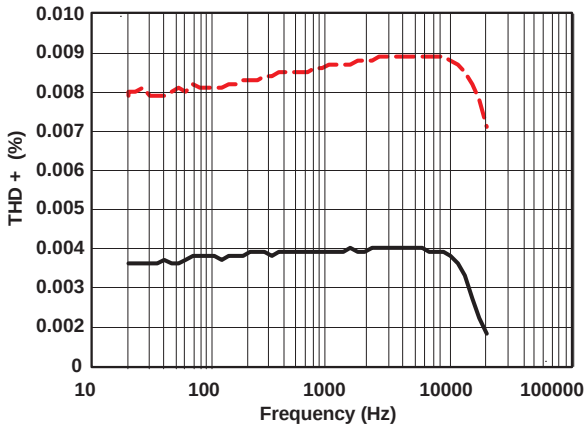


Figure 13. Total Harmonic Distortion vs Frequency (V_+ = 5 V)

7 Parameter Measurement Information

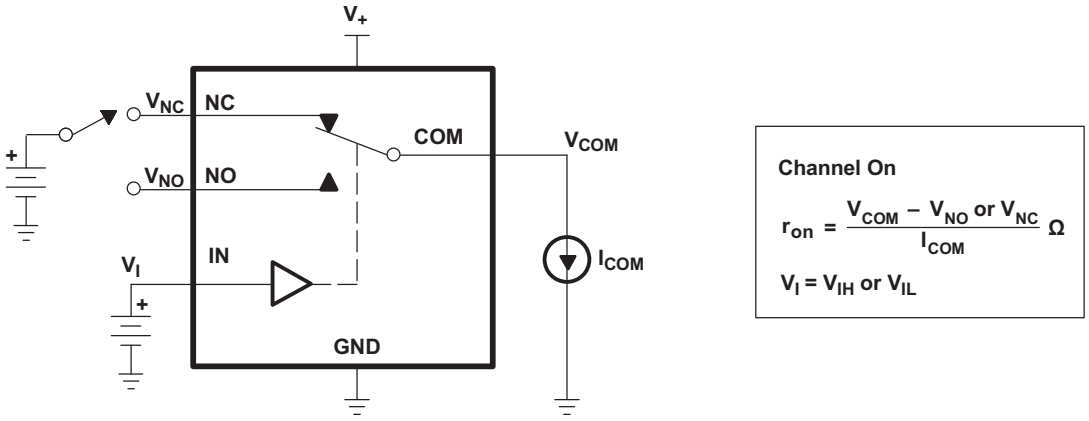


Figure 14. ON-State Resistance (r_{on})

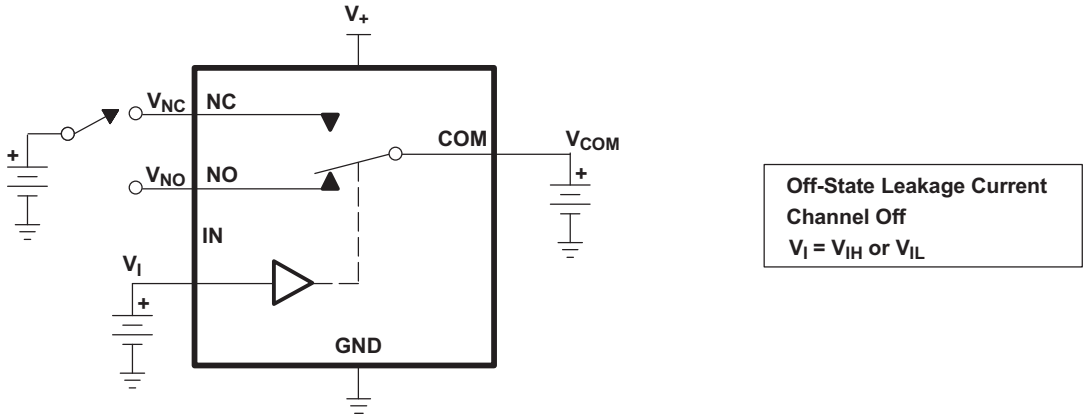


Figure 15. OFF-State Leakage Current ($I_{NC(OFF)}$, $I_{NC(PWROFF)}$, $I_{NO(OFF)}$, $I_{NO(PWROFF)}$, $I_{COM(OFF)}$, $I_{COM(PWROFF)}$)

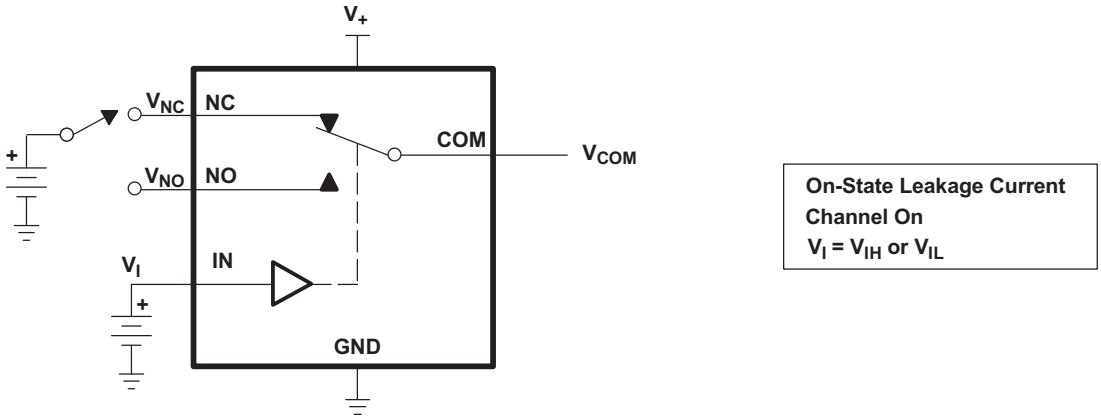


Figure 16. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

Parameter Measurement Information (continued)

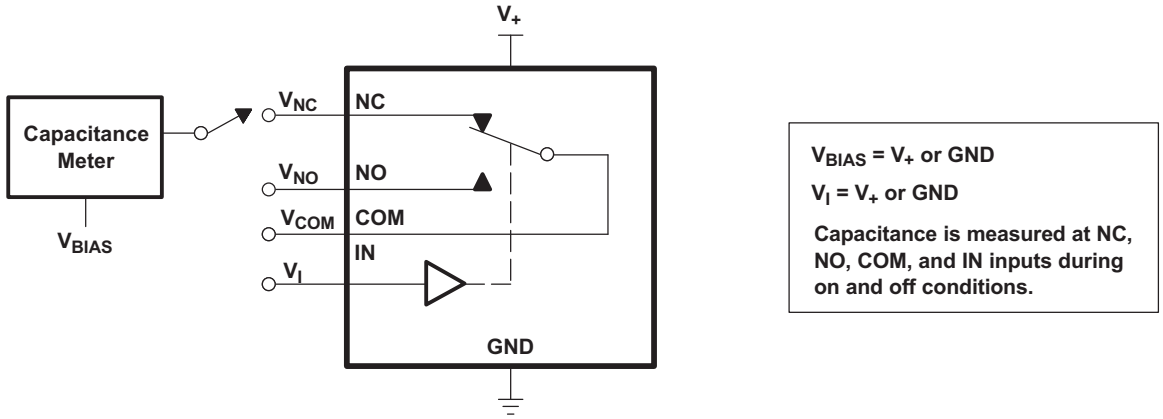
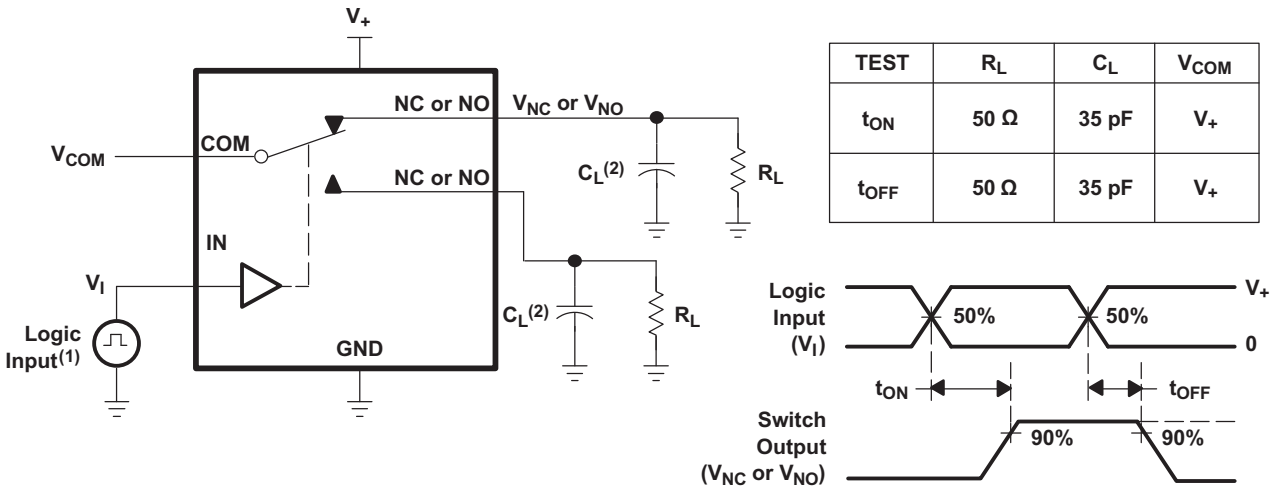


Figure 17. Capacitance (C_I, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)



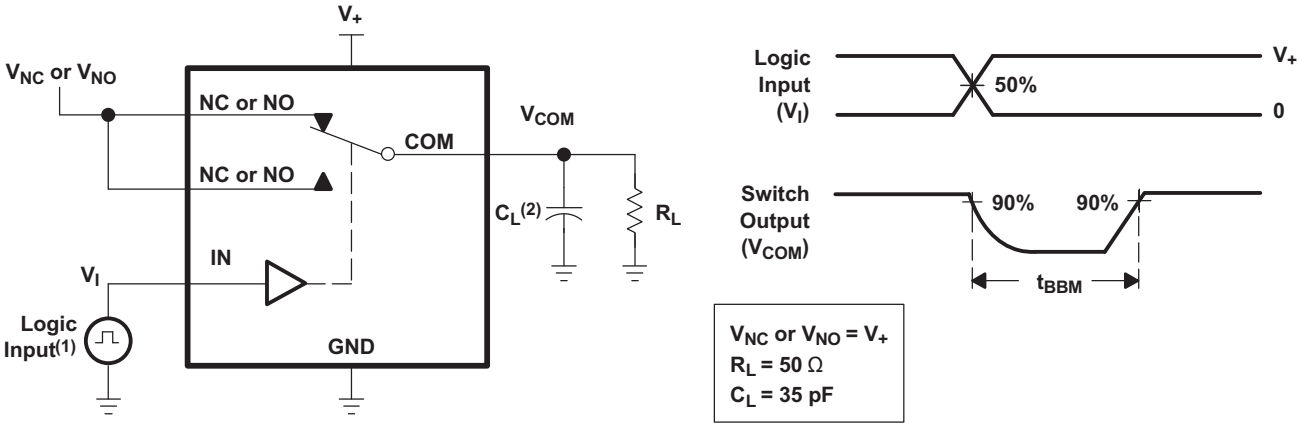
TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V_+
t_{OFF}	50 Ω	35 pF	V_+

(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 18. Turnon (t_{ON}) and Turnoff Time (t_{OFF})

Parameter Measurement Information (continued)



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 19. Break-Before-Make Time (t_{BBM})

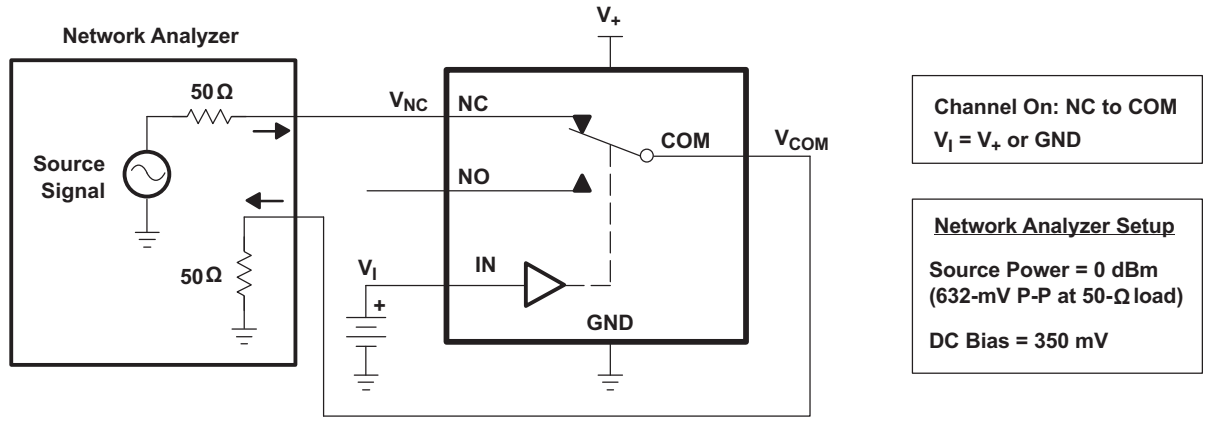


Figure 20. Bandwidth (BW)

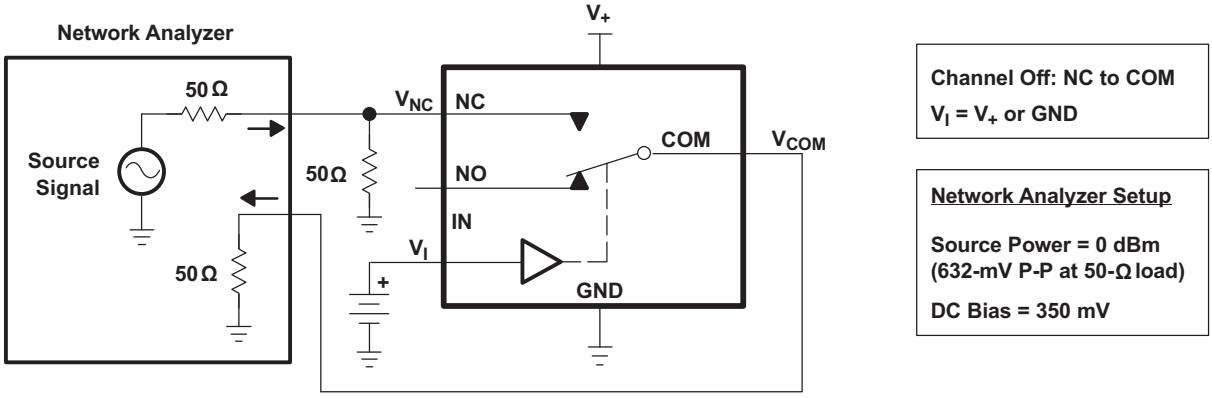


Figure 21. OFF Isolation (O_{ISO})

Parameter Measurement Information (continued)

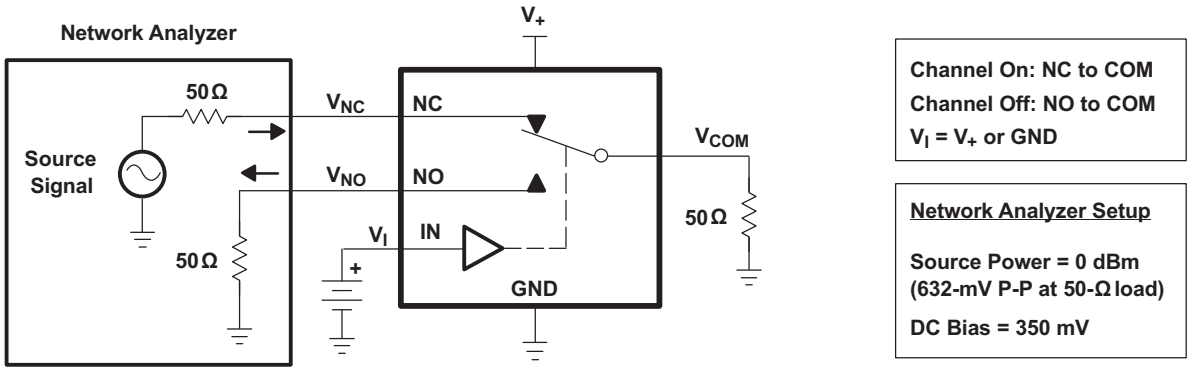
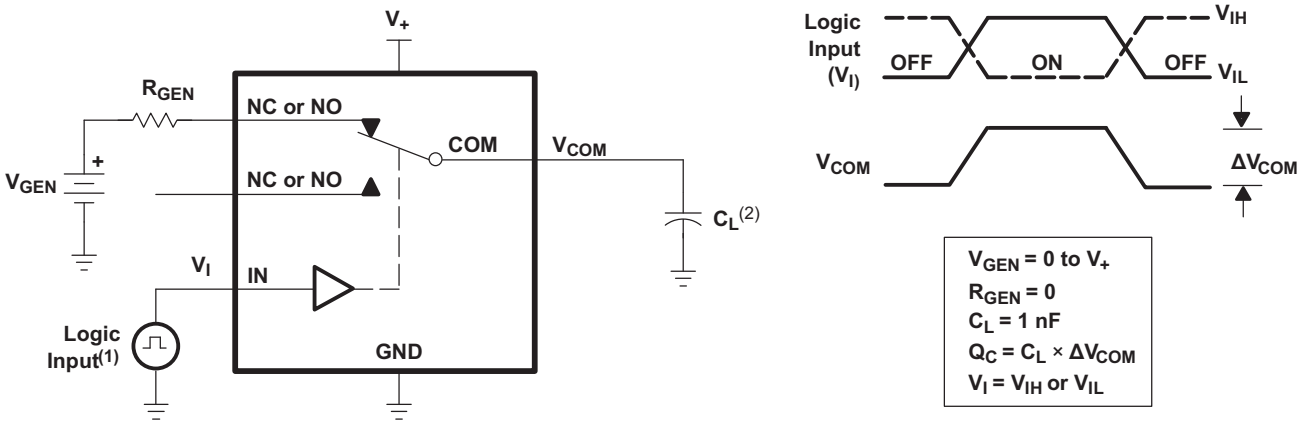


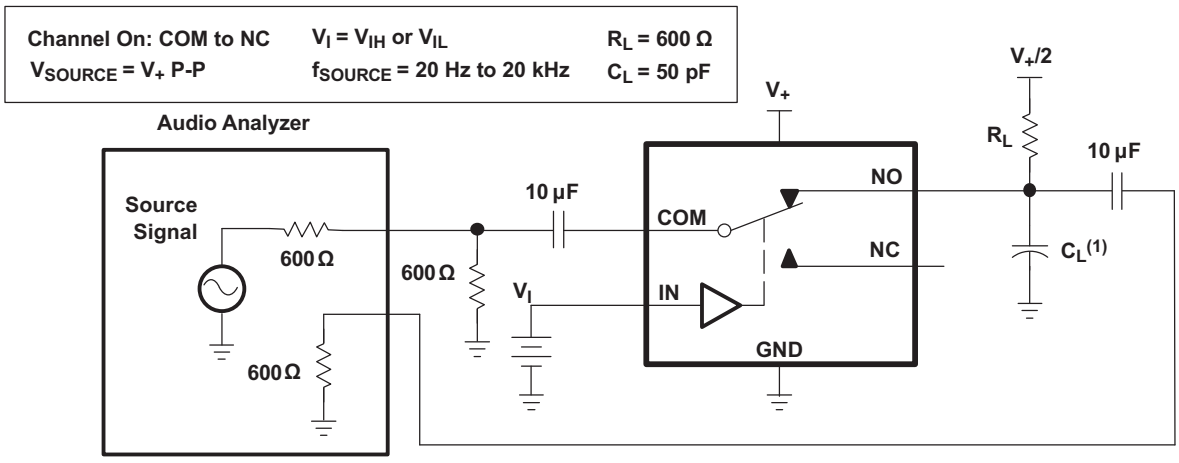
Figure 22. Crosstalk (X_{TALK})



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 23. Charge Injection (Q_C)



(1) C_L includes probe and jig capacitance.

Figure 24. Total Harmonic Distortion (THD)

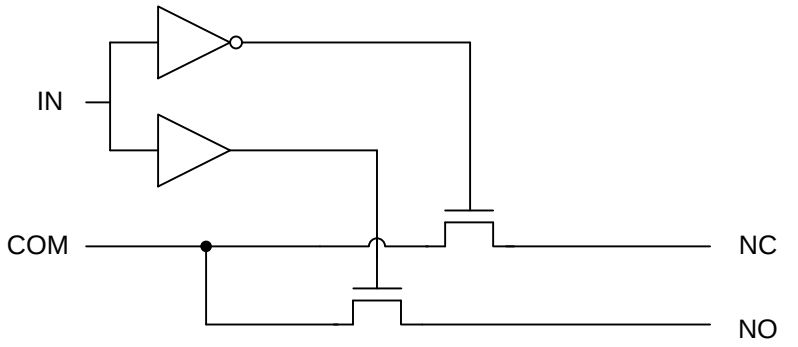
8 Detailed Description

8.1 Overview

The TS5A3159A is a single-pole-double-throw (SPDT) solid-state analog switch. The TS5A3159A, like all analog switches, is bidirectional. When powered on, each COM pin is connected to the NC pin. For this device, NC stands for *normally closed* and NO stands for *normally open*. If IN is low, COM is connected to NC. If IN is high, COM is connected to NO.

The TS5A3159A is a break-before-make switch. This means that during switching, a connection is broken before a new connection is established. The NC and NO pins are never connected to each other.

8.2 Functional Block Diagram



8.3 Feature Description

The low ON-state resistance, ON-state resistance matching, and charge injection in the TS5A3159A make this switch an excellent choice for analog signals that require minimal distortion. In addition, the low THD allows audio signals to be preserved more clearly as they pass through the device.

The 1.65-V to 5.5-V operation allows compatibility with more logic levels, and the bidirectional I/Os can pass analog signals from 0 V to V_+ with low distortion.

8.4 Device Functional Modes

Table 1 lists the functional modes of the TS5A3159A.

Table 1. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS5A3159A can be used in a variety of customer systems. The TS5A3159A can be used anywhere multiple analog or digital signals must be selected to pass across a single line.

9.2 Typical Application

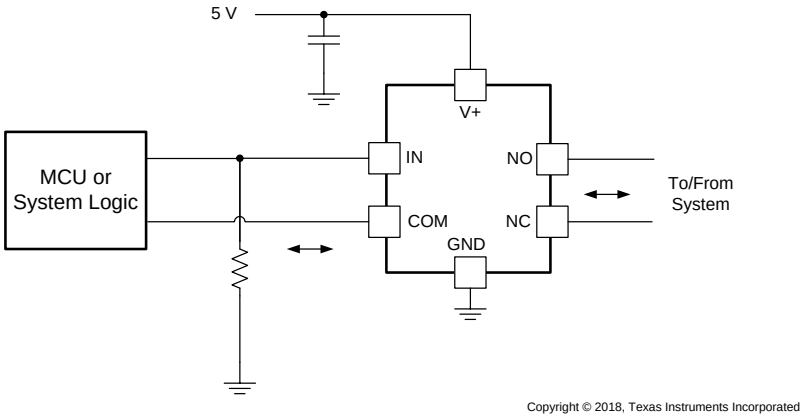


Figure 25. System Schematic for TS5A3159A

9.2.1 Design Requirements

In this particular application, V_+ was 5 V, although V_+ is allowed to be any voltage specified in *Recommended Operating Conditions*. A decoupling capacitor is recommended on the V+ pin. See *Power Supply Recommendations* for more details.

9.2.2 Detailed Design Procedure

In this application, IN is, by default, pulled low to GND. Choose the resistor size based on the current driving strength of the GPIO, the desired power consumption, and the switching frequency (if applicable). If the GPIO is open-drain, use pullup resistors instead.

9.2.3 Application Curve

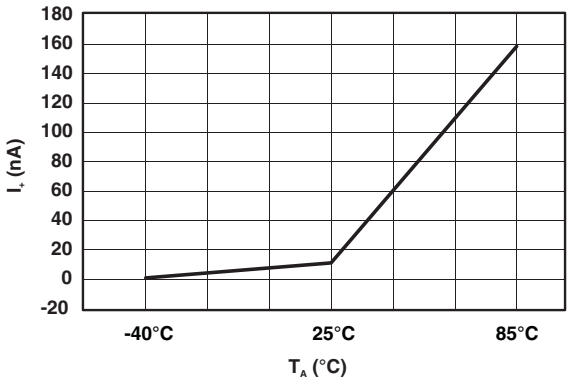


Figure 26. Power-Supply Current vs Temperature (V_+ = 5 V)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-μF or 0.022-μF capacitor is recommended for each V_{CC} because the VCC pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-μF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Figure 27 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

Unused switch I/Os, such as NO, NC, and COM, can be left floating or tied to GND. However, the IN pin must be driven high or low. Due to partial transistor turnon when control inputs are at threshold levels, floating control inputs can cause increased I_{CC} or unknown switch selection states.

11.2 Layout Example

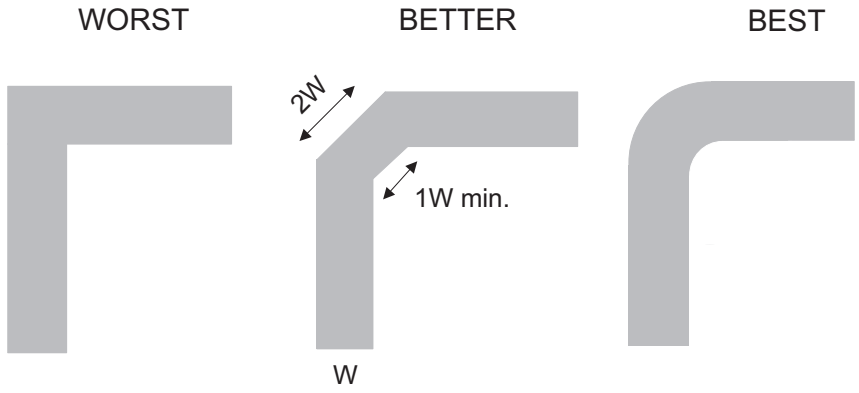


Figure 27. Trace Example

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デバイスの項目表記

表 2. パラメータの説明

記号	説明
V_{COM}	COM電圧
V_{NC}	NC電圧
V_{NO}	NO電圧
r_{on}	チャネルがオンのときのCOMとNCポート間、またはCOMとNOポート間の抵抗
r_{peak}	規定電圧範囲内でのピーク・オン抵抗
Δr_{on}	チャネル間のr_{on}の差
$r_{on(flat)}$	規定の条件の範囲における、チャネルのr_{on}の最大値と最小値との差
$I_{NC(OFF)}$	ワーストケースの入力および出力条件で、対応チャネル(NCからCOMM)がオフ状態のとき、NCポートで測定されるリーク電流
$I_{NC(PWROFF)}$	パワーダウン状況、V_+ =0で、NCポートで測定されるリーク電流
$I_{NO(OFF)}$	ワーストケースの入力および出力条件で、対応チャネル(NOからCOM)がオフ状態のとき、NOポートで測定されるリーク電流
$I_{NO(PWROFF)}$	パワーダウン状況、V_+ = 0で、NOポートで測定されるリーク電流
$I_{NC(ON)}$	対応チャネル(NCからCOM)がオン状態、出力(COM)がオープンのとき、NCポートで測定されるリーク電流
$I_{NO(ON)}$	対応チャネル(NOからCOM)がオン状態、出力(COM)がオープンのとき、NOポートで測定されるリーク電流
$I_{COM(ON)}$	対応チャネル(COMからNO、またはCOMからNC)がオン状態、出力(NCまたはNO)がオープンのとき、COMポートで測定されるリーク電流
$I_{COM(PWROFF)}$	パワーダウン状況、V_+ = 0で、COMポートで測定されるリーク電流
V_{IH}	制御入力(IN)の論理HIGHの最小入力電圧
V_{IL}	制御入力(IN)の論理LOWの最大入力電圧
V_I	(IN)の電圧
I_{IH}、I_{IL}	(IN)で測定されるリーク電流
t_{ON}	スイッチのターンオン時間。このパラメータは、規定された条件の範囲で、スイッチがオンになるときのデジタル制御(IN)信号とアナログ出力(COM、NC、NO)信号との間の伝搬遅延により測定されます。
t_{OFF}	スイッチのターンオフ時間。このパラメータは、規定された条件の範囲で、スイッチがオフになるときのデジタル制御(IN)信号とアナログ出力(COM、NC、NO)信号との間の伝搬遅延により測定されます。
t_{BBM}	Break-Before-Make時間。このパラメータは、規定された条件の範囲で、制御信号の状態が変化するときの2つの隣接するアナログ・チャネル(NCおよびNO)の出力間の伝播遅延により測定されます。
Q_C	電荷注入は、制御(IN)入力からアナログ(NC、NO、COM)出力への、望ましくない信号のカップリングの測定値です。この値はクーロン(C)単位で、制御入力のスイッチングによって誘導される合計電荷により測定されます。電荷注入$Q_C = C_L \times \Delta V_O$で、$C_L$は負荷容量、$\Delta V_O$はアナログ出力電圧の変化です。
$C_{NC(OFF)}$	対応チャネル(NCからCOM)がオフのときのNCポートの容量
$C_{NO(OFF)}$	対応チャネル(NOからCOM)がオフのときのNOポートの容量
$C_{NC(ON)}$	対応チャネル(NCからCOM)がオンのときのNCポートの容量
$C_{NO(ON)}$	対応チャネル(NOからCOM)がオンのときのNOポートの容量
$C_{COM(ON)}$	対応チャネル(COMからNC、またはCOMからNO)がオンのときのCOMポートの容量
C_{IN}	(IN)の容量
O_{ISO}	スイッチのオフ絶縁は、オフ状態のスイッチのインピーダンス測定値です。これは、オフ状態の対応チャネル(NCからCOM、またはNOからCOM)で、特定の周波数についてdB単位で測定されます。
X_{TALK}	クロストークは、オンのチャネルからオフのチャネル(NCからNO、またはNOからNC)への、望ましくない信号カップリングの測定値です。この値は、特定の周波数について、dB単位で測定されます。
BW	スイッチの帯域幅。チャネルのゲインがDCゲインより-3dB低くなる周波数です。
THD	全高調波歪 は、アナログ・スイッチにより発生する信号の歪みです。この値は、2次、3次、およびさらに高次の高調波の値と、基本波の絶対振幅との比または二乗平均(RM)値として定義されます。
I_+	制御(IN)端子がV_+またはGNDであるときの静的消費電流

12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください。

『低速またはフローティングCMOS入力の影響』、SCBA004

12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）コミュニティ。*** エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

12.4 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A3159ADBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAJR JAJH	Samples
TS5A3159ADBVRE4	LIFEBUY	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAJR JAJH	
TS5A3159ADBVRG4	LIFEBUY	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAJR JAJH	
TS5A3159ADBVT	LIFEBUY	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JAJK, JAJR) JAJH	
TS5A3159ADBVTE4	LIFEBUY	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JAJK, JAJR) JAJH	
TS5A3159ADCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JJK, JJR) JJH	Samples
TS5A3159ADCKRE4	LIFEBUY	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JJK, JJR) JJH	
TS5A3159ADCKRG4	LIFEBUY	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JJK, JJR) JJH	
TS5A3159ADCKT	LIFEBUY	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JJK, JJR) JJH	
TS5A3159AYZPR	ACTIVE	DSBGA	YZP	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	JJN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

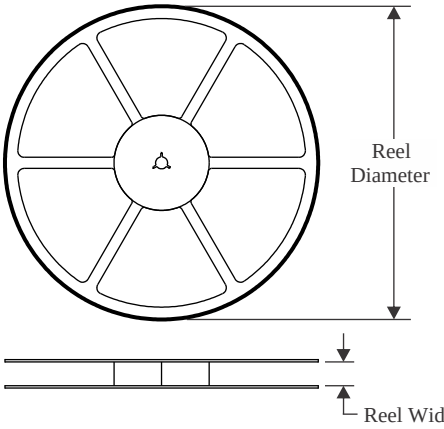
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

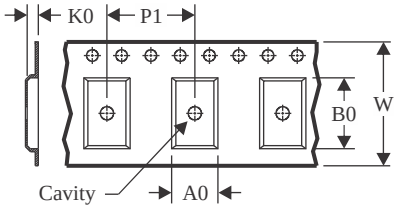
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

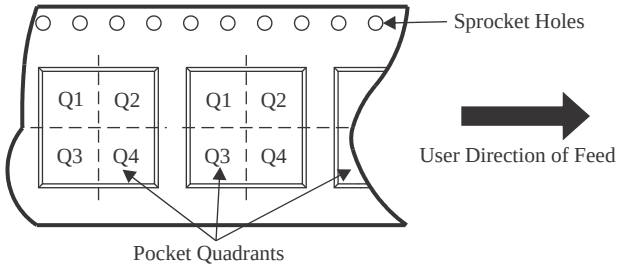


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

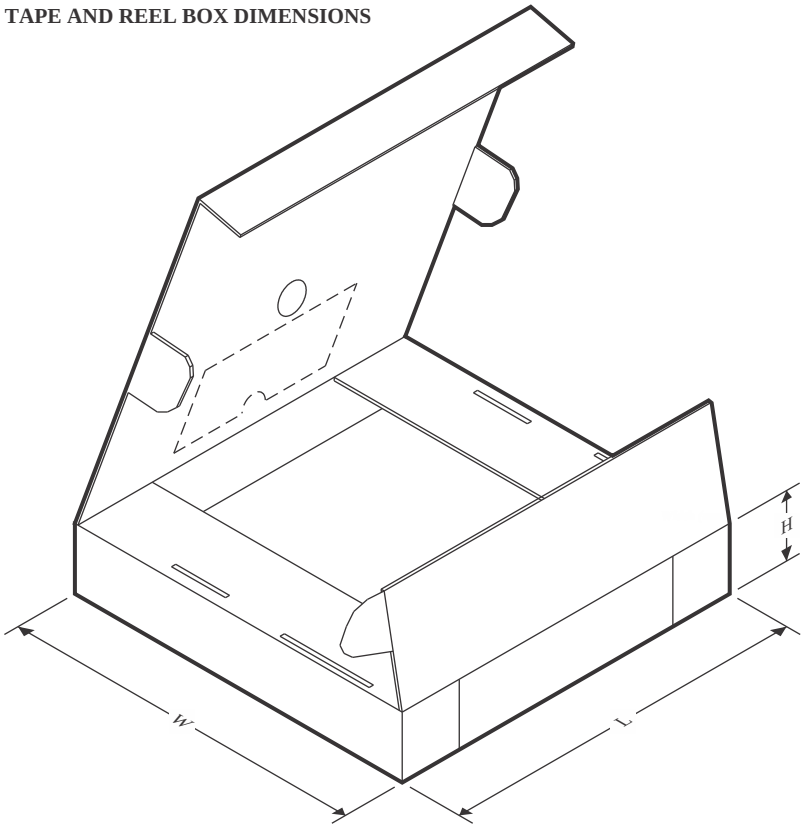
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3159ADBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TS5A3159ADBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TS5A3159ADCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
TS5A3159ADCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TS5A3159ADCKT	SC70	DCK	6	250	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
TS5A3159ADCKT	SC70	DCK	6	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TS5A3159AYZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

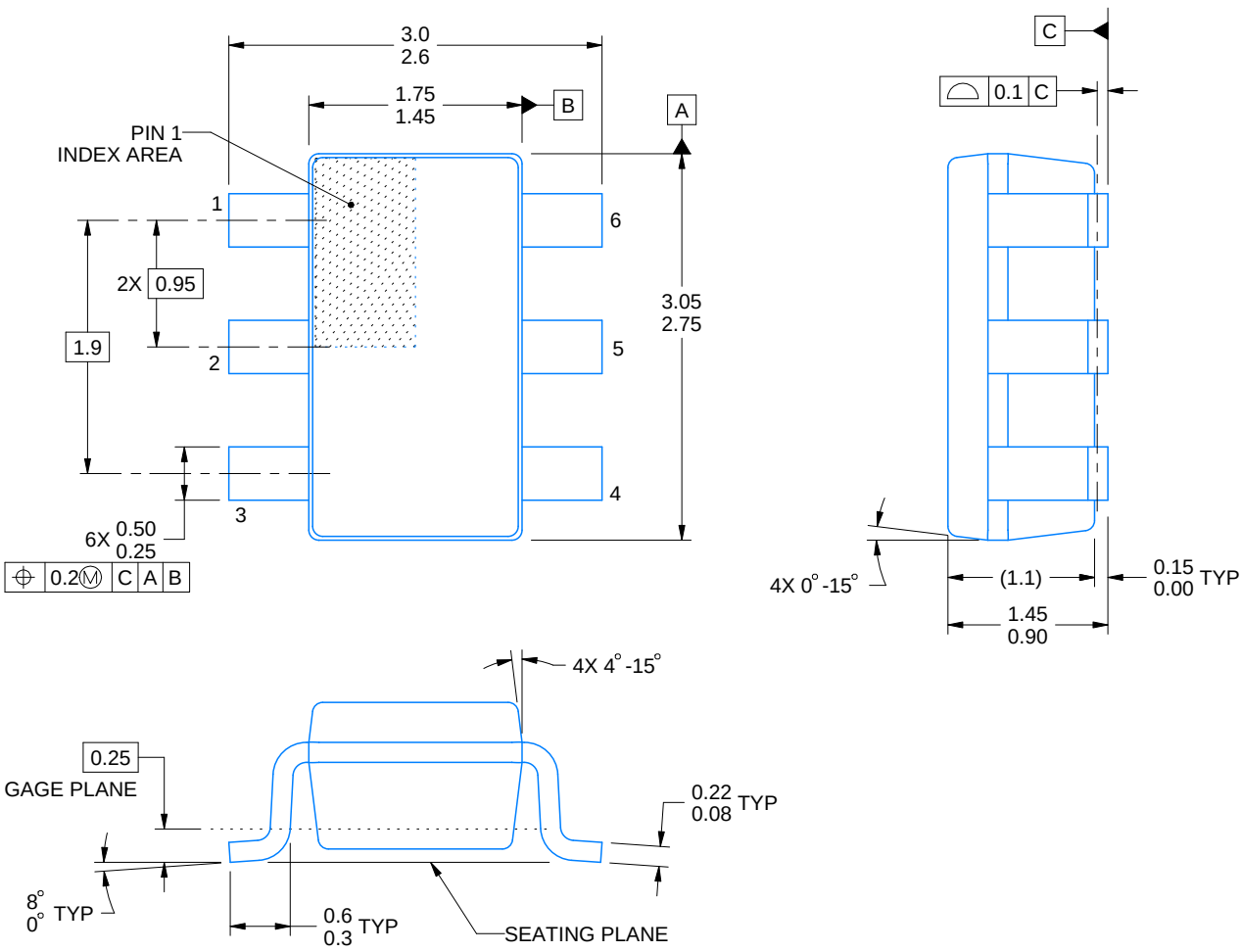
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3159ADBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
TS5A3159ADBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
TS5A3159ADCKR	SC70	DCK	6	3000	205.0	200.0	33.0
TS5A3159ADCKR	SC70	DCK	6	3000	202.0	201.0	28.0
TS5A3159ADCKT	SC70	DCK	6	250	205.0	200.0	33.0
TS5A3159ADCKT	SC70	DCK	6	250	202.0	201.0	28.0
TS5A3159AYZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

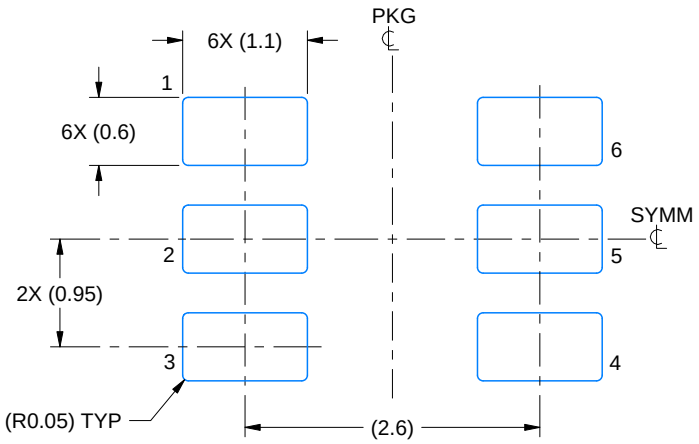
SMALL OUTLINE TRANSISTOR



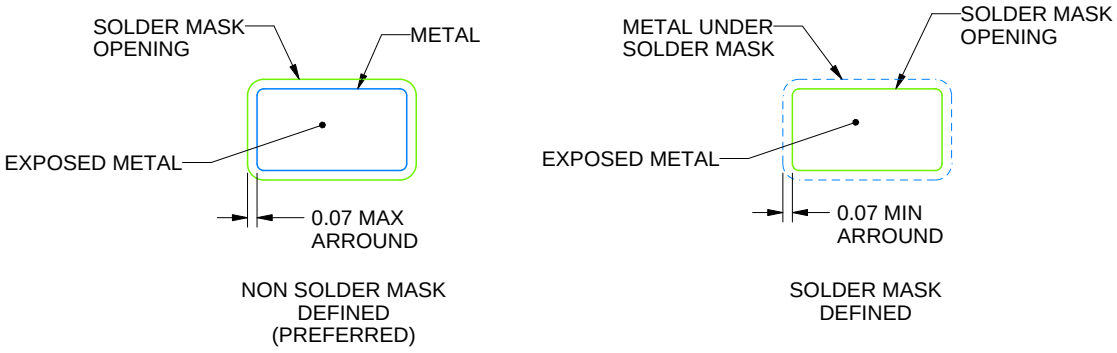
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

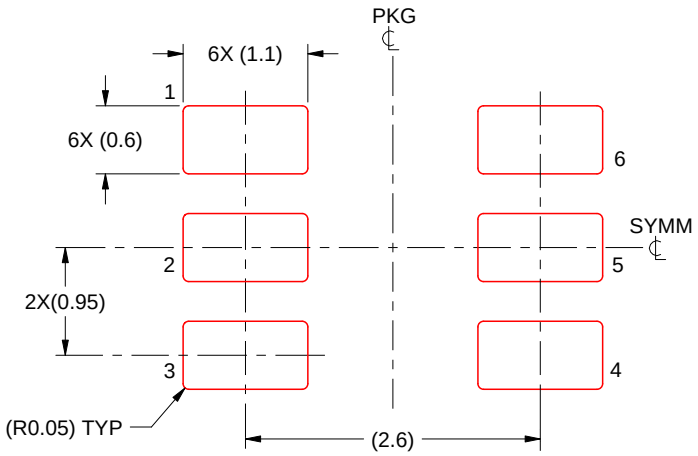


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

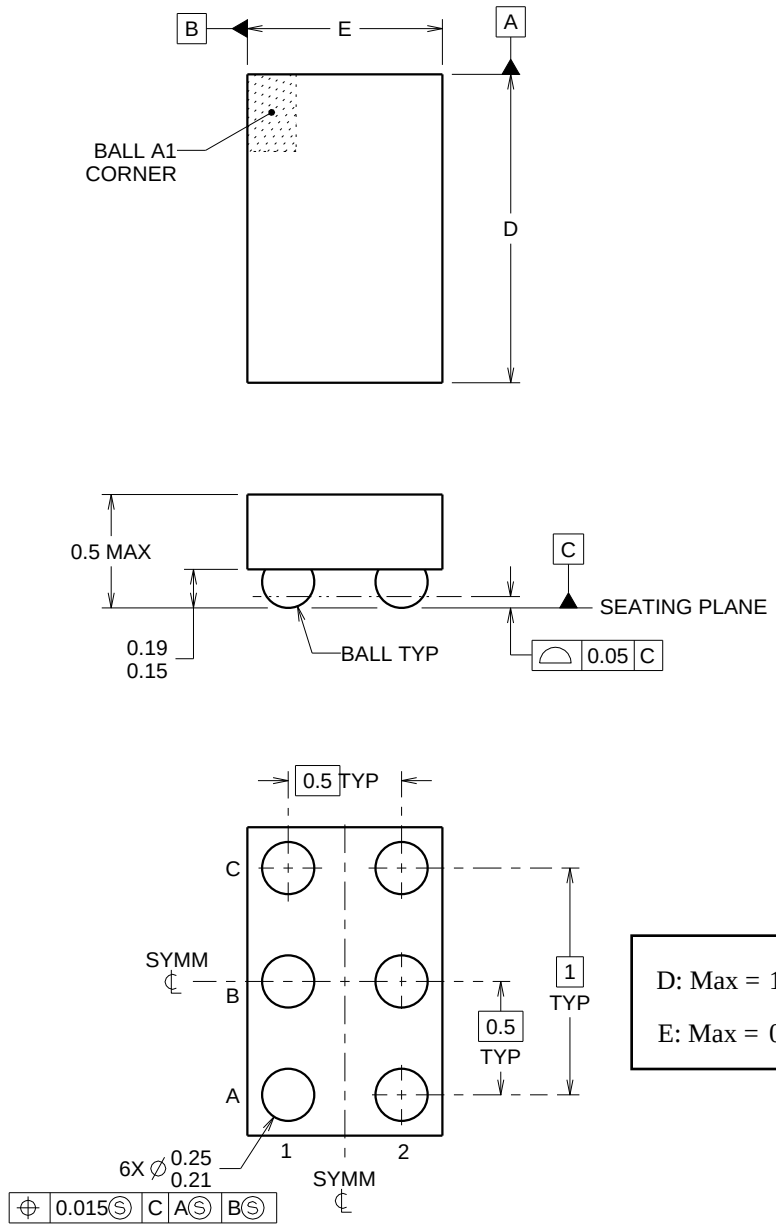
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min =1.358 mm

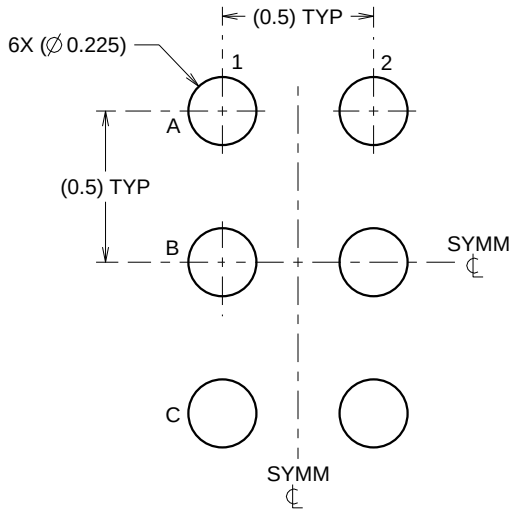
E: Max = 0.918 mm, Min =0.858 mm

4219524/A 06/2014

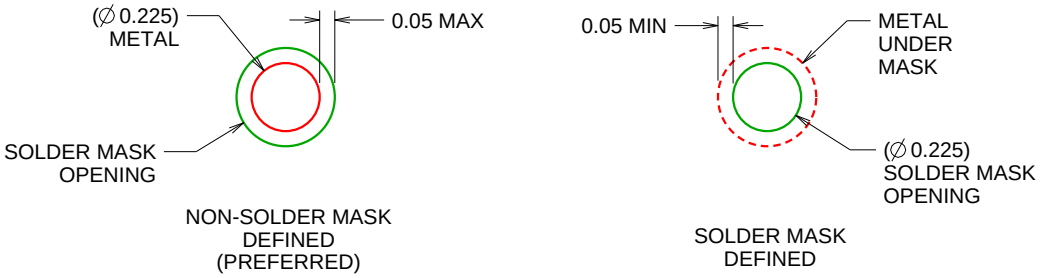
NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
SCALE:40X

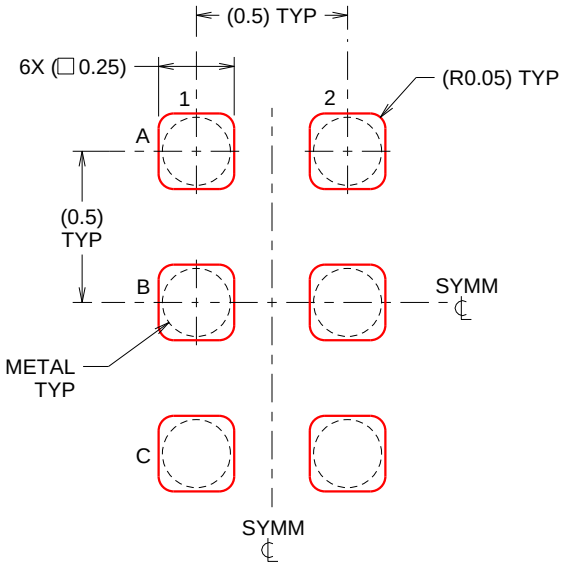


SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

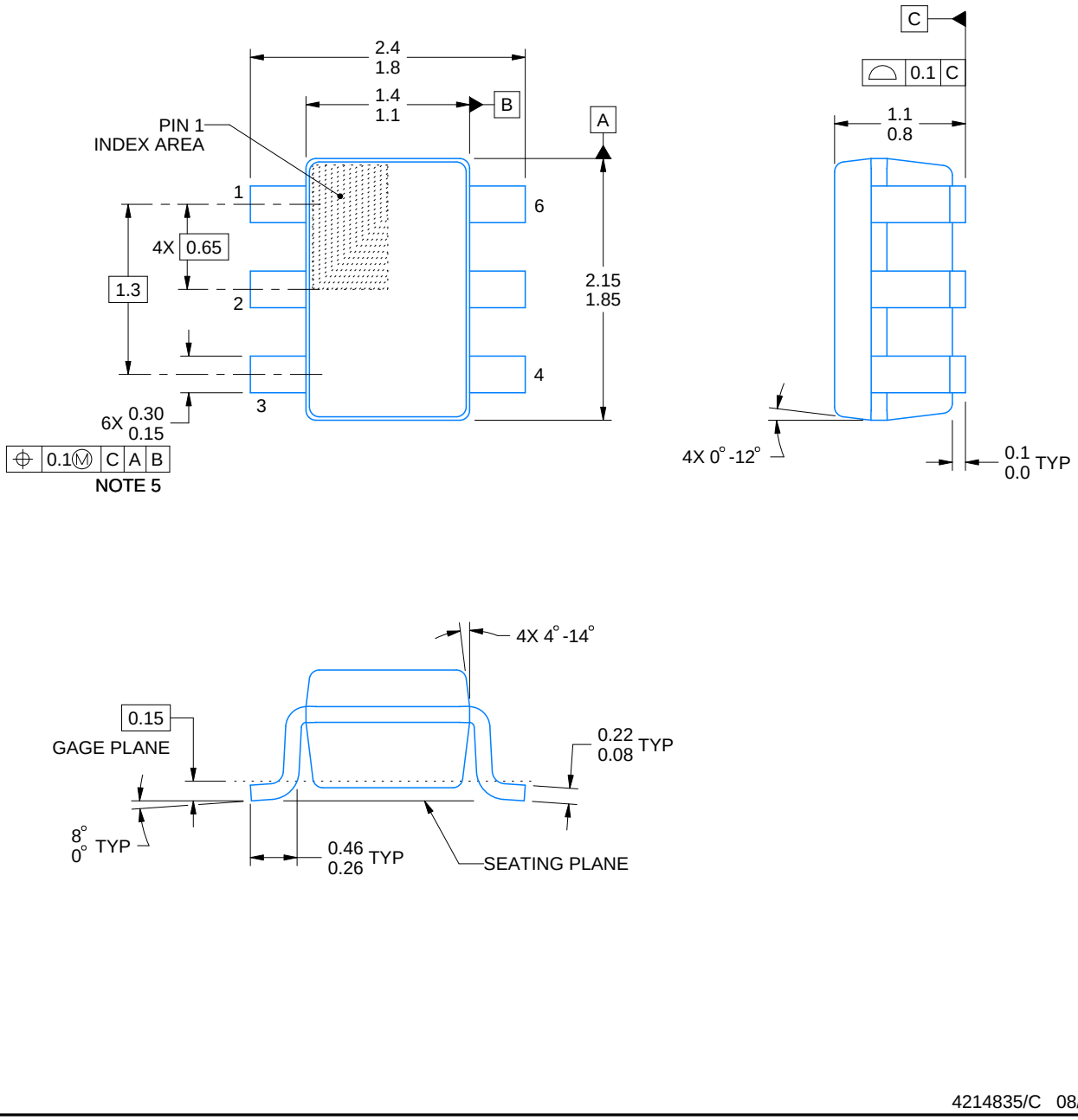
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

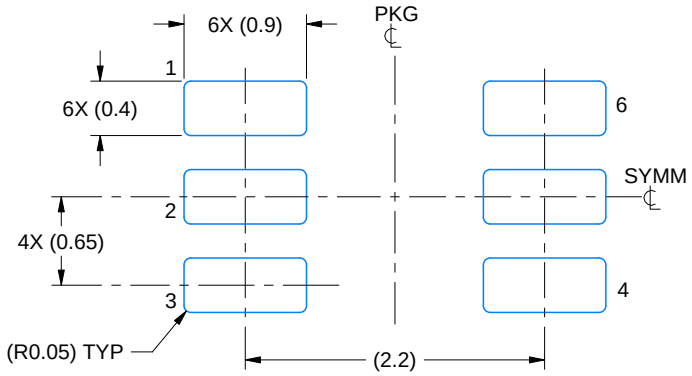
SMALL OUTLINE TRANSISTOR



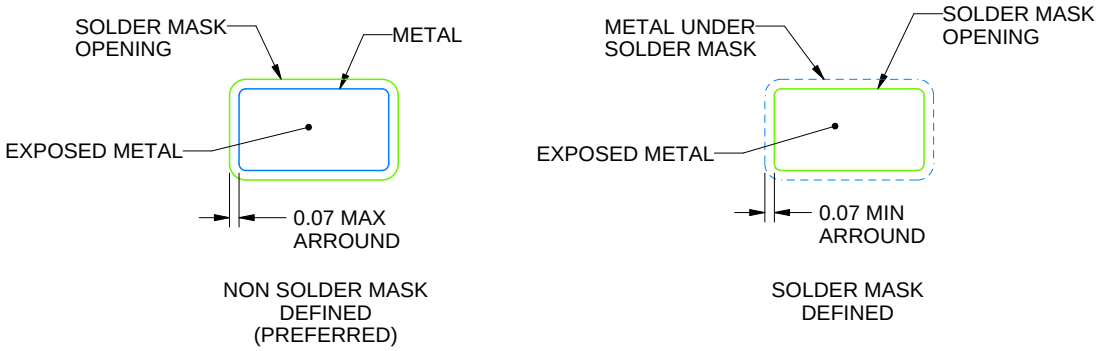
4214835/C 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

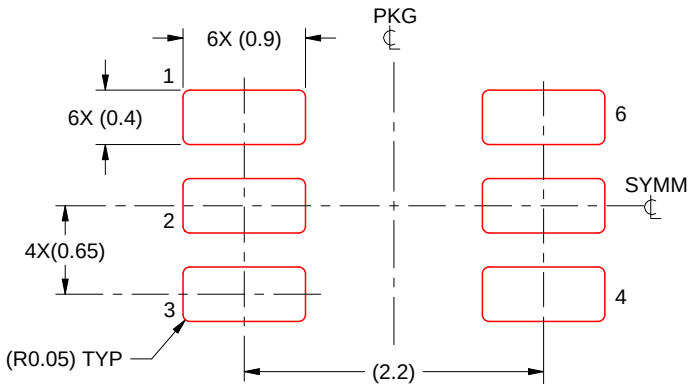


SOLDER MASK DETAILS

4214835/C 08/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/C 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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