

# TS5USBC400 デュアル2:1 USB 2.0マルチプレクサ/デマルチプレクサ、16Vの過電圧保護搭載

## 1 特長

- 電源電圧範囲: 2.3V~5.5V
- 差動2:1または1:2スイッチ/マルチプレクサ
- 共通ピンで0V~16Vの過電圧保護(OVP)
- $V_{CC} = 0V$ での電源オフ保護
- 低い $R_{ON}$ : 9 $\Omega$  (最大値)
- BW: 1.1GHz (標準値)
- $C_{ON}$ : 4.5pF (標準値)
- 低消費電力のディセーブル・モード
- 1.8V互換のロジック入力
- JESD 22を超えるESD保護
  - 人体モデル(HBM) 2000V
- TS5USBC400: 標準温度範囲 0 $^{\circ}C$ ~70 $^{\circ}C$
- TS5USBC400I: 工業用温度範囲 -40 $^{\circ}C$ ~85 $^{\circ}C$
- 小型のDSBGAパッケージ

## 2 アプリケーション

- モバイル
- PC/ノートPC
- タブレット
- USB Type-C™またはMicro-Bコネクタが使用される、あらゆる場所

## 3 概要

TS5USBC400は双方向、低消費電力のデュアル・ポート、高速、USB 2.0アナログ・スイッチで、USB Type-C™システム用の保護機能が内蔵されています。このデバイスはデュアル2:1または1:2スイッチとして構成され、USB Type-C™システムのUSB 2.0 D+/−ラインを扱うよう最適化されています。

TS5USBC400のI/Oピン上の保護機能は、最高16Vに対応し、自動シャットオフ回路により、スイッチより後にあるシステムの部品を保護できます。

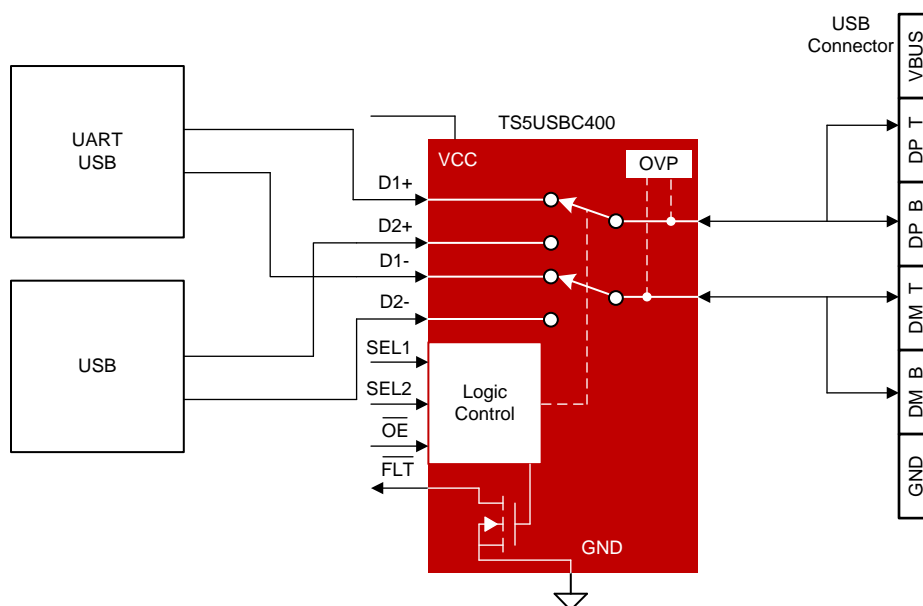
TS5USBC400は小型の12ピンDSBGAパッケージで供給され、モバイル・アプリケーションや容積の制限されるアプリケーションにとって最適な選択肢となります。

### 製品情報<sup>(1)</sup>

型番	パッケージ	本体サイズ(公称)
TS5USBC400 TS5USBC400I	DSBGA (12)	1.582mmx1.182mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

### 概略回路図



Copyright © 2017, Texas Instruments Incorporated



## 目次

<b>1</b>	特長 .....	1	8.2	Functional Block Diagram .....	13
<b>2</b>	アプリケーション .....	1	8.3	Feature Description .....	14
<b>3</b>	概要 .....	1	8.4	Device Functional Modes .....	16
<b>4</b>	改訂履歴 .....	2	<b>9</b>	<b>Application and Implementation</b> .....	17
<b>5</b>	<b>Pin Configuration and Functions</b> .....	3	9.1	Application Information .....	17
<b>6</b>	<b>Specifications</b> .....	4	9.2	Typical Application .....	17
6.1	Absolute Maximum Ratings .....	4	<b>10</b>	<b>Power Supply Recommendations</b> .....	18
6.2	ESD Ratings .....	4	<b>11</b>	<b>Layout</b> .....	19
6.3	Recommended Operating Conditions .....	4	11.1	Layout Guidelines .....	19
6.4	Thermal Information .....	5	11.2	Layout Example .....	20
6.5	Electrical Characteristics .....	5	<b>12</b>	<b>デバイスおよびドキュメントのサポート</b> .....	21
6.6	Dynamic Characteristics .....	7	12.1	ドキュメントのサポート .....	21
6.7	Timing Requirements .....	7	12.2	コミュニティ・リソース .....	21
6.8	Typical Characteristics .....	8	12.3	商標 .....	21
<b>7</b>	<b>Parameter Measurement Information</b> .....	9	12.4	静電気放電に関する注意事項 .....	21
<b>8</b>	<b>Detailed Description</b> .....	13	12.5	Glossary .....	21
8.1	Overview .....	13	<b>13</b>	<b>メカニカル、パッケージ、および注文情報</b> .....	21

## 4 改訂履歴

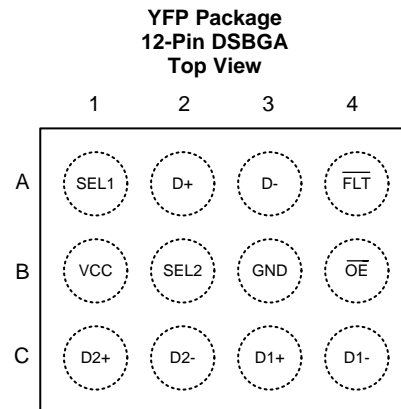
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2017年9月発行のものから更新

Page

- Added  $I_{CC}$  Active supply current and Supply current during OVP condition to the *Electrical Specification* table ..... 4

## 5 Pin Configuration and Functions



**Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
SEL1	A1	I	Switch select1 (Active high)
D+	A2	I/O	Data switch input (Differential +)
D-	A3	I/O	Data switch input (Differential -)
$\overline{\text{FLT}}$	A4	O	Fault indicator output pin (Active low) - open drain
VCC	B1	PWR	Supply Voltage
SEL2	B2	I	Switch select2 (Active high)
GND	B3	GND	Ground
$\overline{\text{OE}}$	B4	I	Output enable (Active low)
D2+	C1	I/O	Data switch output 2 (Differential +)
D2-	C2	I/O	Data switch output 2 (Differential -)
D1+	C3	I/O	Data switch output 1 (Differential +)
D1-	C4	I/O	Data switch output 1 (Differential -)

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup> <sup>(2)</sup>

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage <sup>(3)</sup>		-0.5	6	V
$V_{I/O}$	Input/Output DC voltage (D+, D-) <sup>(3)</sup>		-0.5	18	V
$V_{I/O}$	Input/Output DC voltage (D1+/D1-, D2+/D2-) <sup>(3)</sup>		-0.5	6	V
$V_I$	Digital input voltage (SEL1, SEL2, $\overline{OE}$ )		-0.5	6	V
$V_O$	Digital output voltage ( $\overline{FLT}$ )		-0.5	6	V
$I_K$	Input-output port diode current (D+, D-, D1+, D1-, D2+, D2-)	$V_{IN} < 0$	-50		mA
$I_{IK}$	Digital logic input clamp current (SEL1, SEL2, $\overline{OE}$ ) <sup>(3)</sup>	$V_I < 0$	-50		mA
$I_{CC}$	Continuous current through VCC			100	mA
$I_{GND}$	Continuous current through GND		-100		mA
$T_{stg}$	Storage temperature		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2.3	5.5	V
$V_{I/O}$ (D+, D-)	Analog input/output voltage	0	18	V
$V_{I/O}$ (D1, D1-, D2+, D2-)		0	3.6	V
$V_I$	Digital input voltage (SEL1, SEL2, $\overline{OE}$ )	0	5.5	V
$V_O$	Digital output voltage ( $\overline{FLT}$ )	0	5.5	V
$I_{I/O}$ (D+, D-, D1+, D1-, D2+, D2-)	Analog input/output port continuous current	-50	50	mA
$I_{OL}$	Digital output current		3	mA
$T_A$	Operating free-air temperature (TS5USBC400) Standard	0	70	°C
$T_A$	Operating free-air temperature (TS5USBC400I) Industrial	-40	85	°C
$T_J$	Junction temperature	-40	125	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TS5USBC400	
		YFP	UNIT
		12 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	91.8	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	0.8	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	22.8	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.5	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	23.0	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

T<sub>A</sub> = –40°C to +85°C (Industrial), T<sub>A</sub> = 0°C to 70°C (Standard), V<sub>CC</sub> = 2.3 V to 5.5 V, GND = 0V, Typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY</b>						
V <sub>CC</sub>	Power supply voltage		2.3		5.5	V
I <sub>CC</sub>	Active supply current	$\overline{OE} = 0\text{ V}$ SEL1, SEL2 = 0 V, 1.8 V or V <sub>CC</sub> 0 V < V <sub>I/O</sub> < 3.6 V		72	100	μA
	Supply current during OVP condition	$\overline{OE} = 0\text{ V}$ SEL1, SEL2 = 0 V, 1.8 V or V <sub>CC</sub> V <sub>I/O</sub> > V <sub>POS_THLD</sub>		80	120	μA
I <sub>CC_PD</sub>	Standby powered down supply current	$\overline{OE} = 1.8\text{ V or }V_{CC}$ SEL1 = 0 V, 1.8 V, or V <sub>CC</sub> SEL2 = 0 V, 1.8 V, or V <sub>CC</sub>		2.2	10	μA
<b>DC Characteristics</b>						
R <sub>ON</sub>	ON-state resistance	V <sub>I/O</sub> = 0.4 V I <sub>SINK</sub> = 8 mA Refer to <a href="#">ON-State Resistance Figure</a>		5.6	9	Ω
ΔR <sub>ON</sub>	ON-state resistance match between channels	V <sub>I/O</sub> = 0.4 V I <sub>SINK</sub> = 8 mA Refer to <a href="#">ON-State Resistance Figure</a>		0.07	0.3	Ω
R <sub>ON (FLAT)</sub>	ON-state resistance flatness	V <sub>I/O</sub> = 0 V to 0.4 V I <sub>SINK</sub> = 8 mA Refer to <a href="#">ON-State Resistance Figure</a>		0.07	0.4	Ω
I <sub>OFF</sub>	I/O pin OFF leakage current	V <sub>D±</sub> = 0 V or 3.6 V V <sub>CC</sub> = 2.3 V to 5.5 V V <sub>D1±</sub> or V <sub>D2±</sub> = 3.6 V or 0 V Refer to <a href="#">Off Leakage Figure</a>	-1	1.2	6	μA
		V <sub>D±</sub> = 0 V or 16 V V <sub>CC</sub> = 2.3 V to 5.5 V V <sub>D1±</sub> or V <sub>D2±</sub> = 0 V Refer to <a href="#">Off Leakage Figure</a>	-1	165	200	μA
I <sub>ON</sub>	ON leakage current	V <sub>D±</sub> = 0 V or 3.6 V V <sub>D1±</sub> and V <sub>D2±</sub> = high-Z Refer to <a href="#">On Leakage Figure</a>	-1	1.2	6	μA
<b>Digital Characteristics</b>						
V <sub>IH</sub>	Input logic high	SEL1, SEL2, $\overline{OE}$	1.4			V
V <sub>IL</sub>	Input logic low	SEL1, SEL2, $\overline{OE}$			0.5	V
V <sub>OL</sub>	Output logic low	$\overline{FLT}$ I <sub>OL</sub> = 3 mA			0.4	V
I <sub>IH</sub>	Input high leakage current	SEL1, SEL2, $\overline{OE} = 1.8\text{ V, }V_{CC}$	-1	1	5	μA
I <sub>IL</sub>	Input low leakage current	SEL1, SEL2, $\overline{OE} = 0\text{ V}$	-1	±0.2	5	μA

**Electrical Characteristics (continued)**

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  (Industrial),  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  (Standard),  $V_{CC} = 2.3\text{ V}$  to  $5.5\text{ V}$ ,  $GND = 0\text{V}$ , Typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{PD}$	Internal pull-down resistor on digital input pins			6		$M\Omega$
$C_1$	Digital input capacitance	SEL1, SEL2 = 0 V, 1.8 V or VCC f = 1 MHz		3.4		pF
<b>Protection</b>						
$V_{OVP\_TH}$	OVP positive threshold		4.5	4.8	5.2	V
$V_{OVP\_HYST}$	OVP threshold hysteresis		75	230	425	mV
$V_{CLAMP\_V}$	Maximum voltage to appear on D1± and D2± pins during OVP scenario	$V_{D\pm} = 0$ to 18 V $t_{RISE}$ and $t_{FALL}(10\% \text{ to } 90\%) = 100\text{ ns}$ $R_L = \text{Open}$ Switch on or off $\overline{OE} = 0\text{ V}$	0		9.6	V
		$V_{D\pm} = 0$ to 18 V $t_{RISE}$ and $t_{FALL}(10\% \text{ to } 90\%) = 100\text{ ns}$ $R_L = 50\Omega$ Switch on or off $\overline{OE} = 0\text{ V}$	0		9.0	V
$t_{EN\_OVP}$	OVP enable time	$R_{PU} = 10\text{ k}\Omega$ to VCC ( $\overline{FLT}$ ) $C_L = 35\text{ pF}$ Refer to <a href="#">OVP Timing Diagram Figure</a>		0.6	3	$\mu\text{s}$
$t_{REC\_OVP}$	OVP recovery time	$R_{PU} = 10\text{ k}\Omega$ to VCC ( $\overline{FLT}$ ) $C_L = 35\text{ pF}$ Refer to <a href="#">OVP Timing Diagram Figure</a>		1.5	5	$\mu\text{s}$

## 6.6 Dynamic Characteristics

$T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  (Industrial),  $T_A = 0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$  (Standard),  $V_{CC} = 2.3\text{ V}$  to  $5.5\text{ V}$ ,  $GND = 0\text{ V}$ , Typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ , (unless otherwise noted)

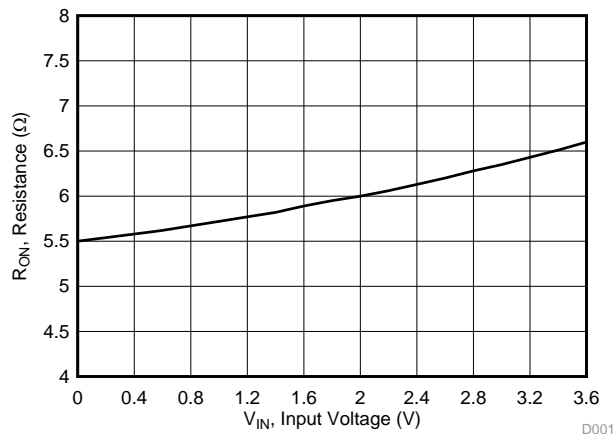
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$C_{OFF}$	D+, D- off capacitance	$V_{D+/-} = 0$ or $3.3\text{ V}$ , $\overline{OE} = V_{CC}$ $f = 240\text{ MHz}$	Switch OFF	1.2	3.5	6.2	pF
	D1+, D1-, D2+, D2- off capacitance	$V_{D+/-} = 0$ or $3.3\text{ V}$ , $\overline{OE} = V_{CC}$ or $\overline{OE} = 0\text{ V}$ with SEL1, SEL2 (switch not selected) $f = 240\text{ MHz}$	Switch OFF or not selected	1.2	3.5	6.2	pF
$C_{ON}$	IO pins ON capacitance	$V_{D+/-} = 0$ or $3.3\text{ V}$ , $f = 240\text{ MHz}$	Switch ON	1.4	4.5	6.2	pF
$O_{ISO}$	Differential off isolation	$R_L = 50\ \Omega$ $C_L = 5\text{ pF}$ $f = 100\text{ kHz}$ Refer to <a href="#">Off Isolation Figure</a>	Switch OFF		-90		dB
		$R_L = 50\ \Omega$ $C_L = 5\text{ pF}$ $f = 240\text{ MHz}$ Refer to <a href="#">Off Isolation Figure</a>	Switch OFF		-22		dB
$X_{TALK}$	Channel to Channel crosstalk	$R_L = 50\ \Omega$ $C_L = 5\text{ pF}$ $f = 100\text{ kHz}$ Refer to <a href="#">Crosstalk Figure</a>	Switch ON		-90		dB
BW	Bandwidth	$R_L = 50\ \Omega$ ; Refer to <a href="#">BW and Insertion Loss Figure</a>	Switch ON		1.1		GHz
$I_{LOSS}$	Insertion loss	$R_L = 50\ \Omega$ $f = 240\text{ MHz}$ ; Refer to <a href="#">BW and Insertion Loss Figure</a>	Switch ON		-0.7		dB

## 6.7 Timing Requirements

$T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  (Industrial),  $T_A = 0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$  (Standard),  $V_{CC} = 2.3\text{ V}$  to  $5.5\text{ V}$ ,  $GND = 0\text{ V}$ , Typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ , (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{switch}$	Switching time between channels (SEL1, SEL2 to output)	$V_{D+/-} = 0.8\text{ V}$ Refer to <a href="#">Tswitch Timing Figure</a>		0.45	1.2	$\mu\text{s}$
$t_{on}$	Device turn on time ( $\overline{OE}$ to output)	$V_{D+/-} = 0.8\text{ V}$ Refer to <a href="#">Ton and Toff Figure</a>	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $V_{CC} = 2.3\text{ V}$ to $5.5\text{ V}$	100	250	$\mu\text{s}$
$t_{off}$	Device turn off time ( $\overline{OE}$ to output)	$V_{D+/-} = 0.8\text{ V}$ Refer to <a href="#">Ton and Toff Figure</a>		0.35	1	$\mu\text{s}$
$t_{SK(P)}$	Skew of opposite transitions of same output (between D+ and D-)	$V_{D+/-} = 0.4\text{ V}$ Refer to <a href="#">Tsk Figure</a>	$R_L = 50\ \Omega$ , $C_L = 1\text{ pF}$ , $V_{CC} = 2.3\text{ V}$ to $5.5\text{ V}$	9	50	ps
$t_{pd}$	Propagation delay	$V_{D+/-} = 0.4\text{ V}$ Refer to <a href="#">Tpd Figure</a>	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $V_{CC} = 2.3\text{ V}$ to $5.5\text{ V}$	130	180	ps

## 6.8 Typical Characteristics



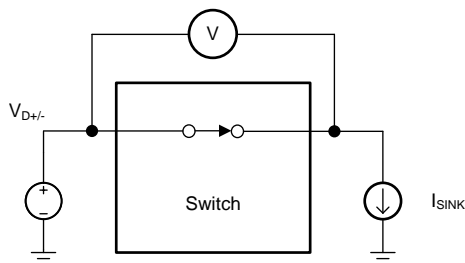
V<sub>CC</sub> = 3.3 V

T<sub>A</sub> = 25°C

☒ 1. ON-Resistance vs Input Voltage



## 7 Parameter Measurement Information



Channel ON,  $R_{ON} = V/I_{SINK}$

图 2. ON-State Resistance ( $R_{ON}$ )

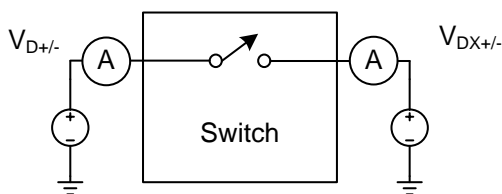


图 3. Off Leakage

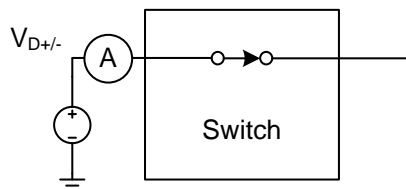
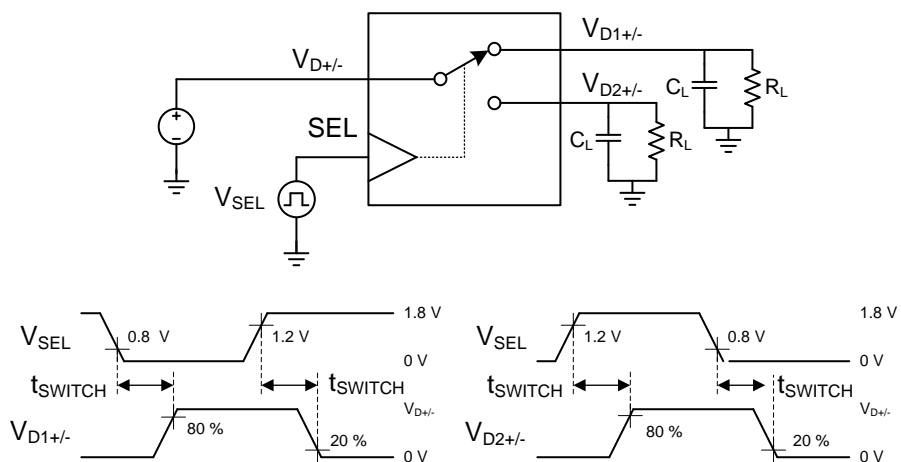


图 4. On Leakage

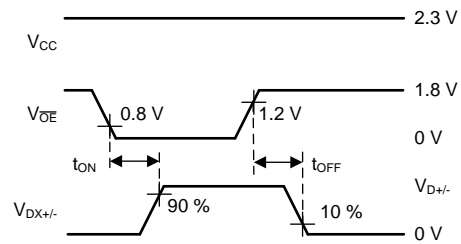
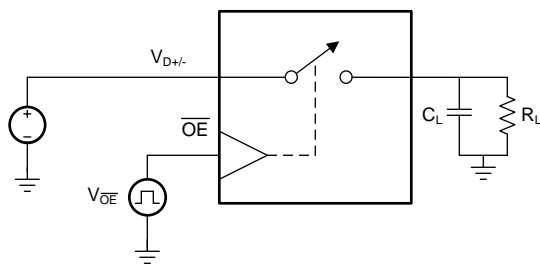


Copyright © 2017, Texas Instruments Incorporated

- (1) All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r < 500 \text{ ps}$ ,  $t_f < 500 \text{ ps}$ .
- (2)  $C_L$  includes probe and jig capacitance.

图 5.  $t_{SWITCH}$  Timing

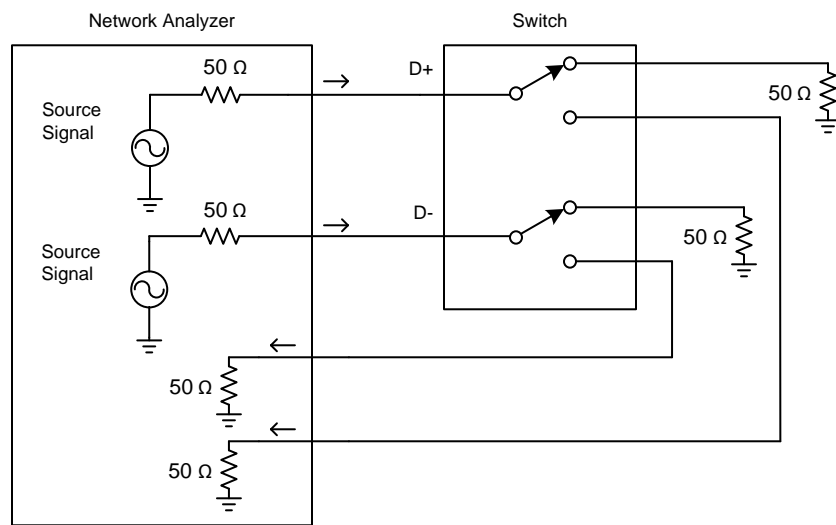
**Parameter Measurement Information (continued)**



Copyright © 2017, Texas Instruments Incorporated

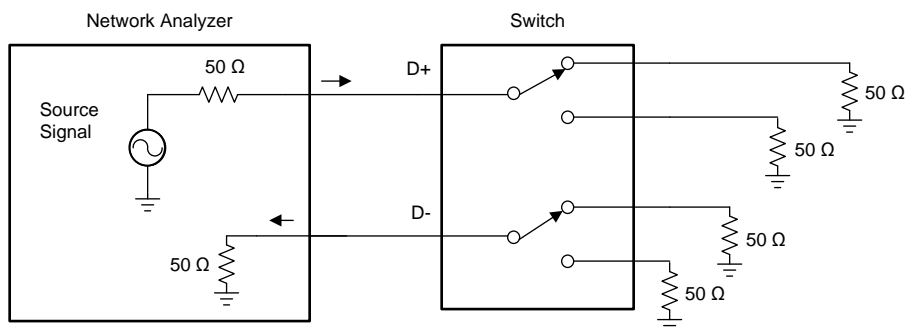
- (1) All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r < 500 \text{ ps}$ ,  $t_f < 500 \text{ ps}$ .
- (2)  $C_L$  includes probe and jig capacitance.

**图 6.  $t_{ON}$ ,  $t_{OFF}$  for  $\overline{OE}$**



Copyright © 2017, Texas Instruments Incorporated

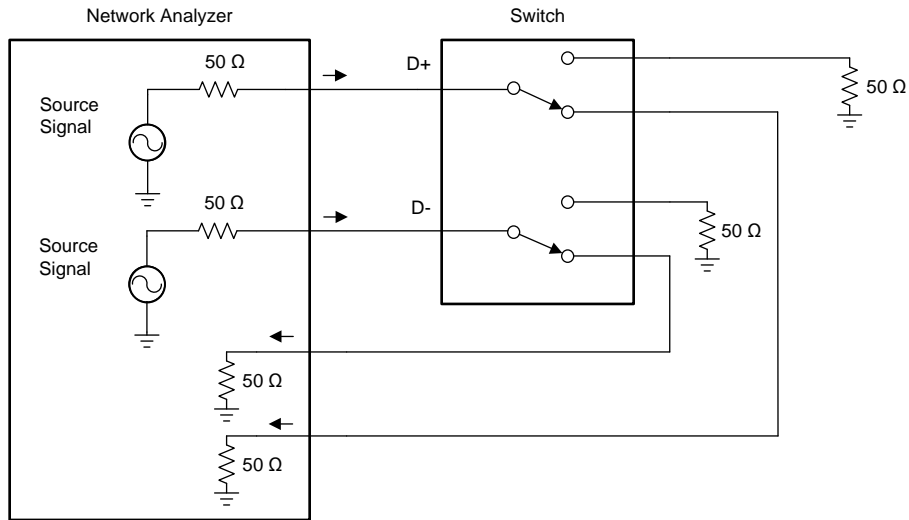
**图 7. Off Isolation**



Copyright © 2017, Texas Instruments Incorporated

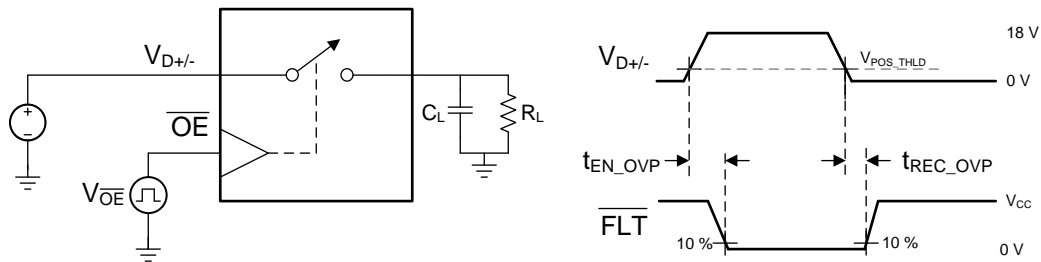
**图 8. Cross Talk**

**Parameter Measurement Information (continued)**



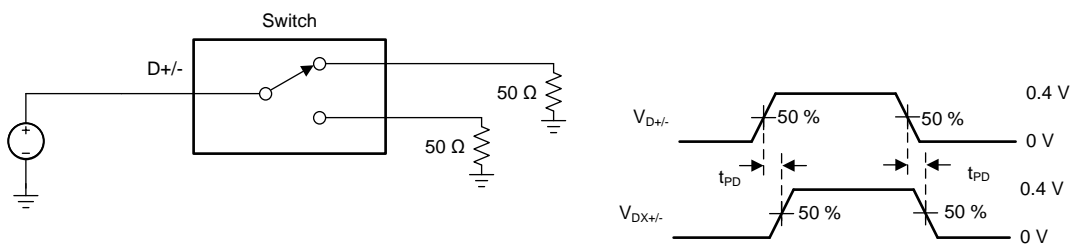
Copyright © 2017, Texas Instruments Incorporated

**图 9. BW and Insertion Loss**



Copyright © 2017, Texas Instruments Incorporated

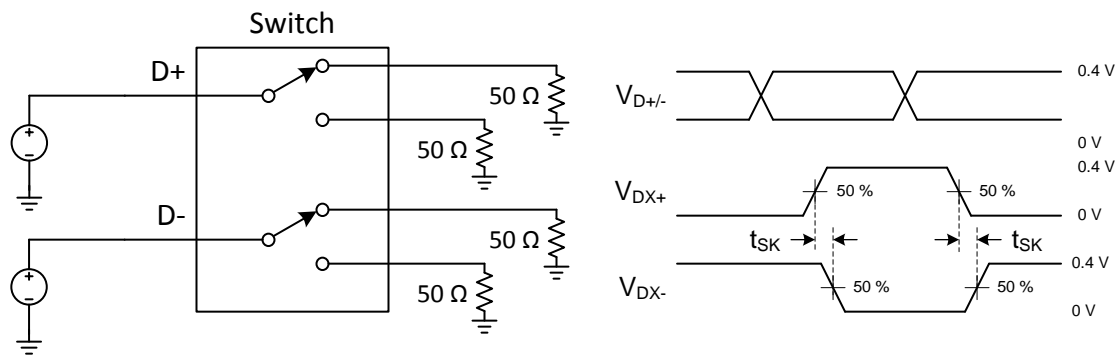
**图 10.  $t_{EN\_OVP}$  and  $t_{DIS\_OVP}$  Timing Diagram**



Copyright © 2017, Texas Instruments Incorporated

- (1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> < 500 ps, t<sub>f</sub> < 500 ps.
- (2) C<sub>L</sub> includes probe and jig capacitance.

**图 11.  $t_{PD}$**

**Parameter Measurement Information (continued)**


Copyright © 2017, Texas Instruments Incorporated

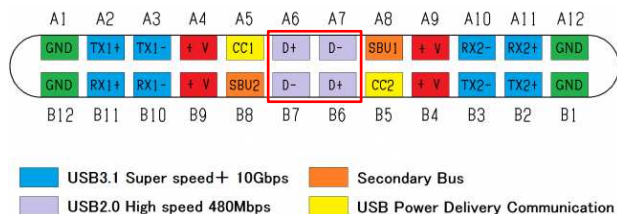
- (1) All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r < 500$  ps,  $t_f < 500$  ps.
- (2)  $C_L$  includes probe and jig capacitance.

**图 12.  $t_{SK}$**

## 8 Detailed Description

### 8.1 Overview

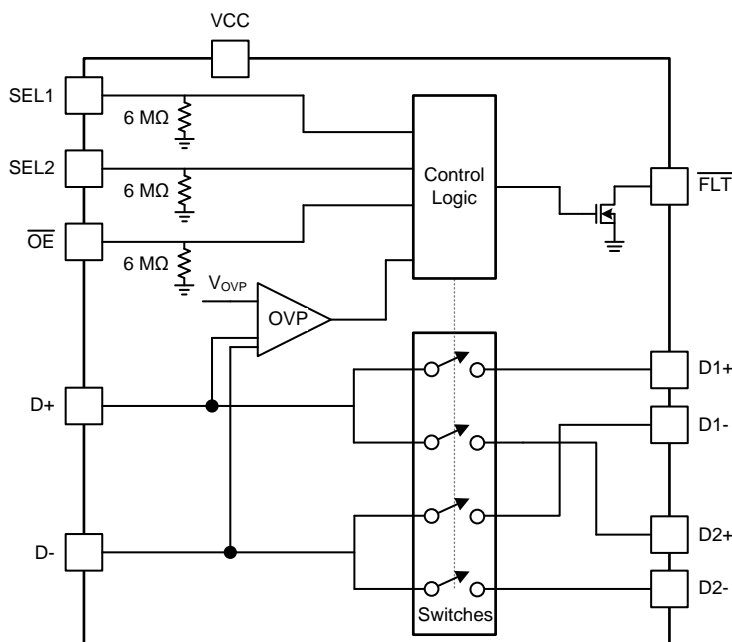
The TS5USBC400 is a bidirectional low-power dual port, high-speed, USB 2.0 analog switch with integrated protection for USB Type-C systems. The device is configured as a dual 2:1 or 1:2 switch and is optimized for handling the USB 2.0 D+/- lines in a USB Type-C system as shown in [Figure 13](#).



**Figure 13. USB Type-C Connector Pinout**

The TS5USBC400 also works in traditional USB systems that need protection from fault conditions such as automotive and applications that require higher voltage charging. The device maintains excellent signal integrity through the optimization of both  $R_{ON}$  and BW while protecting the system with 0 V to 16 V OVP protection. The OVP implementation is designed to protect sensitive system components behind the switch that cannot survive a fault condition where VBUS is shorted the D+ and D- pins on the connector.

### 8.2 Functional Block Diagram



Copyright © 2017, Texas Instruments Incorporated

### 8.3 Feature Description

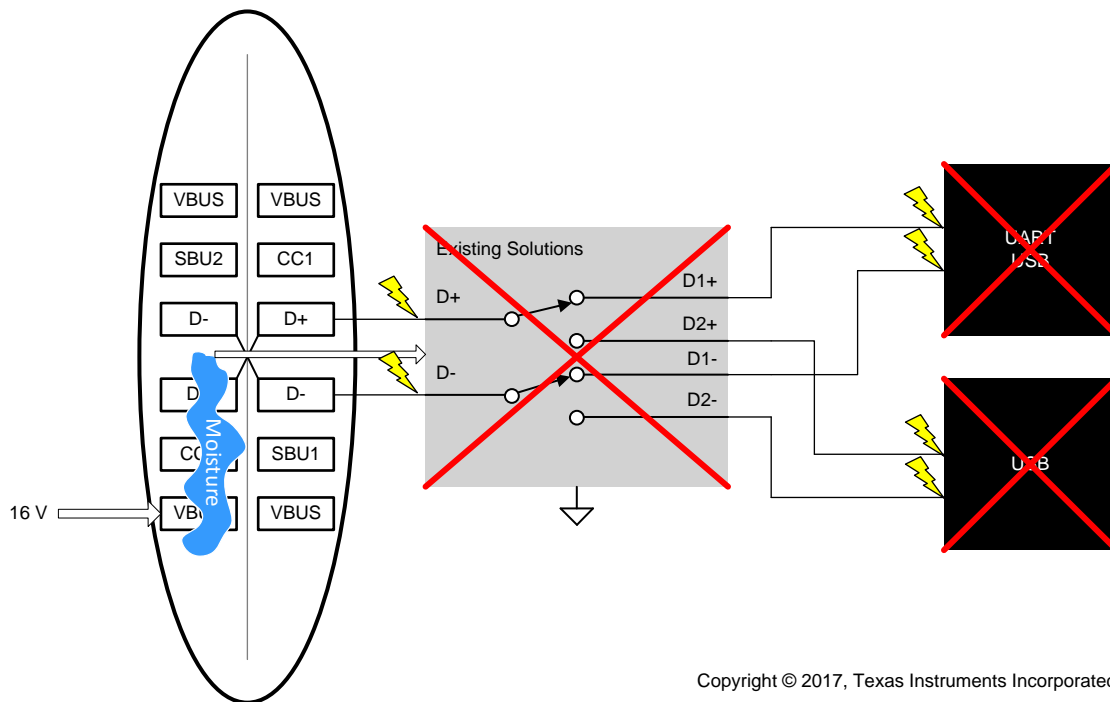
#### 8.3.1 Powered-off Protection

When the TS5USBC400 is powered off the I/Os of the device remain in a high-Z state. The crosstalk, off-isolation, and leakage remain within the [Electrical Specifications](#).

This prevents errant voltages from reaching the rest of the system and maintains isolation when the system is powering up.

#### 8.3.2 Overvoltage Protection

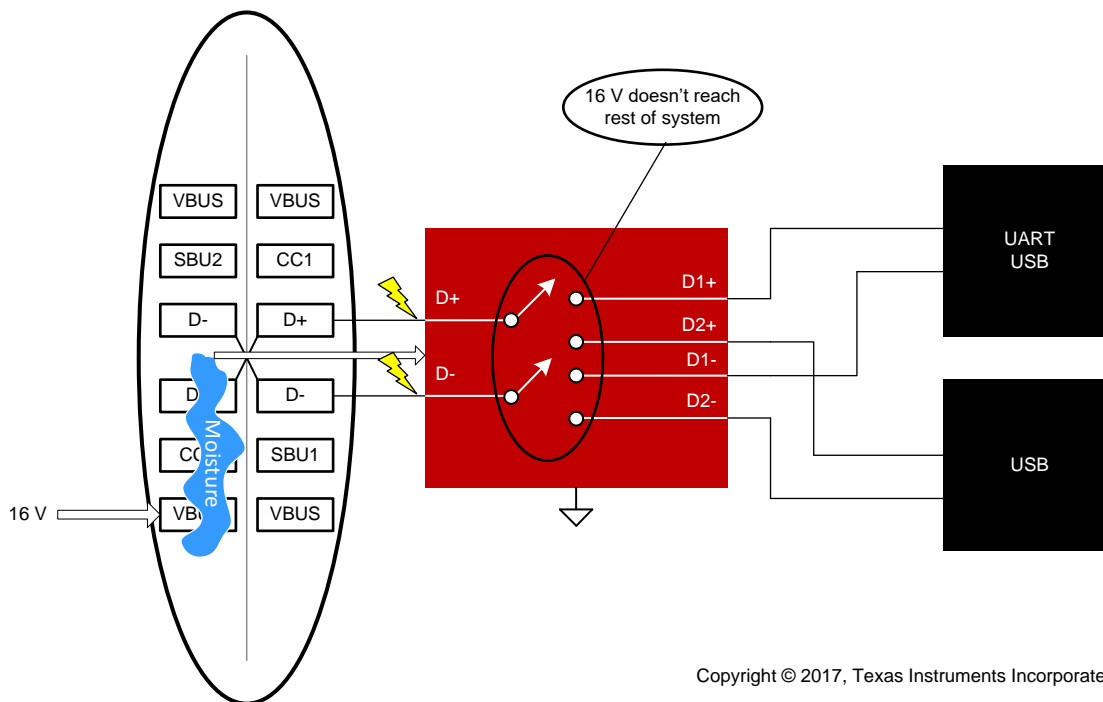
The OVP of the TS5USBC400 is designed to protect the system from D+/- shorts to VBUS at the USB and USB Type-C connector. [Figure 14](#) depicts a moisture short that would cause 16 V to appear on an existing USB solution that could pass through the device and damage components behind the device.



**Figure 14. Existing Solution Being Damaged by a Short, 16 V**

The TS5USBC400 will open the switches and protect the rest of the system by blocking the 16 V as depicted in .

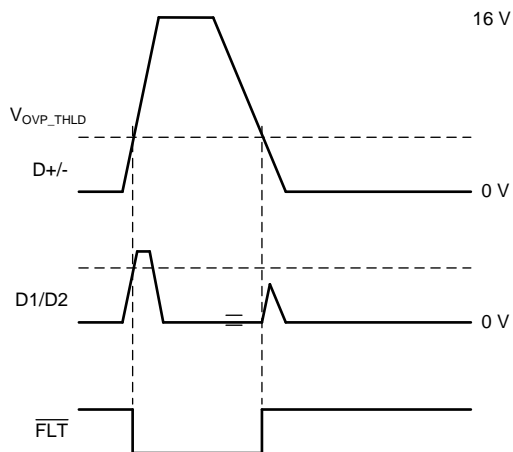
Feature Description (continued)



Copyright © 2017, Texas Instruments Incorporated

⊠ 15. Protecting During a 16-V Short

⊠ 16 is a waveform showing the voltage on the pins during an over-voltage scenario.



⊠ 16. Overvoltage Protection Waveform, 16 V

## 8.4 Device Functional Modes

### 8.4.1 Pin Functions

**表 1. Function Table**

$\overline{OE}$	SEL1	SEL2	D- Connection	D+ Connection
H	X	X	High-Z	High-Z
L	L	L	D- to D1-	D+ to D1+
L	L	H	D- to D1-	D+ to D2+
L	H	L	D- to D2-	D+ to D1+
L	H	H	D- to D2-	D+ to D2+



## 9 Application and Implementation

### 注

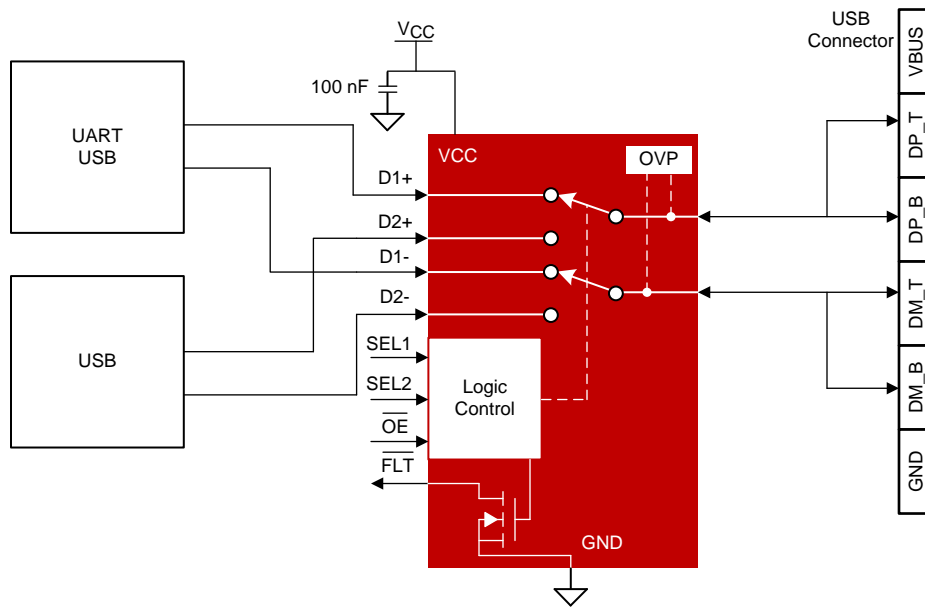
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

There are many USB applications in which the USB hubs or controllers have a limited number of USB I/Os or need to route signals from a single USB connector. The TS5USBC400 solution can effectively expand the limited USB I/Os by switching between multiple USB buses to interface them to a single USB hub or controller or route signals from one connector to two different locations. With independent control of the two switches using SEL1 and SEL2, TS5USBC400 can be used to cross switch single ended signals.

### 9.2 Typical Application

TS5USBC400 USB/UART switch. The TS5USBC400 is used to switch signals between the USB path, which goes to the baseband or application processor, or the UART path, which goes to debug port. The TS5USBC400 has internal 6-M $\Omega$  pull-down resistors on SEL1, SEL2, and OE. The pull-down on SEL1 and SEL2 pins ensure the D1+/D1- channel is selected by default. The pull-down on OE enables the switch when power is applied.



Copyright © 2017, Texas Instruments Incorporated

图 17. Typical TS5USBC400 Application

#### 9.2.1 Design Requirements

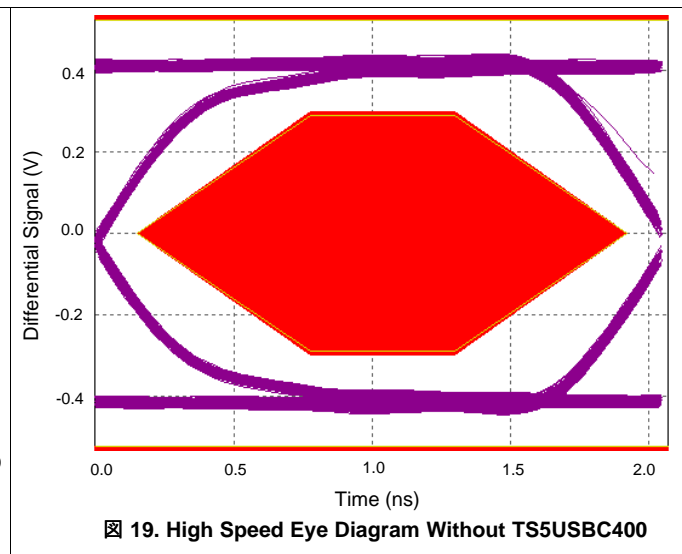
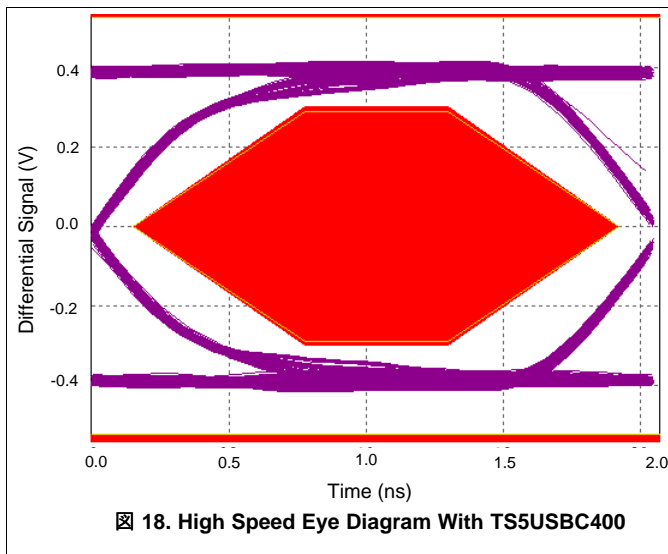
Design requirements of USB 1.0, 1.1, and 2.0 standards must be followed. The TS5USBC400 has internal 6-M $\Omega$  pull-down resistors on SEL1, SEL2, and OE, so no external resistors are required on the logic pins. The internal pull-down resistor on SEL1 and SEL2 pins ensures the D1+ and D1- channels are selected by default. The internal pull-down resistor on OE enables the switch when power is applied to VCC.

#### 9.2.2 Detailed Design Procedure

The TS5USBC400 can be properly operated without any external components. However, TI recommends that unused pins must be connected to ground through a 50- $\Omega$  resistor to prevent signal reflections back into the device. TI does recommend a 100nF bypass capacitor placed close to TS5USBC400 VCC pin.

## Typical Application (continued)

### 9.2.3 Application Curves



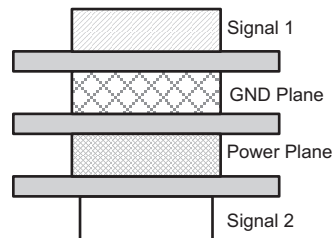
## 10 Power Supply Recommendations

Power to the device is supplied through the VCC pin and must follow the USB 1.0, 1.1, and 2.0 standards. TI recommends placing a 100nF bypass capacitor as close to the supply pin VCC as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

## 11 Layout

### 11.1 Layout Guidelines

1. Place supply bypass capacitors as close to VCC pin as possible and avoid placing the bypass caps near the  $D_{\pm}$  traces.
2. The high-speed  $D_{\pm}$  must match and be no more than 4 inches long; otherwise, the eye diagram performance may be degraded. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In layout, the impedance of  $D+$  and  $D-$  traces must match the cable characteristic differential impedance for optimal performance.
3. Route the high-speed USB signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.
4. When it becomes necessary to turn  $90^{\circ}$ , use two  $45^{\circ}$  turns or an arc instead of making a single  $90^{\circ}$  turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.
5. Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.
6. Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub must be less than 200 mm.
7. Route all high-speed USB signal traces over continuous GND planes, with no interruptions.
8. Avoid crossing over anti-etch, commonly found with plane splits.
9. Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in [Figure 20](#).

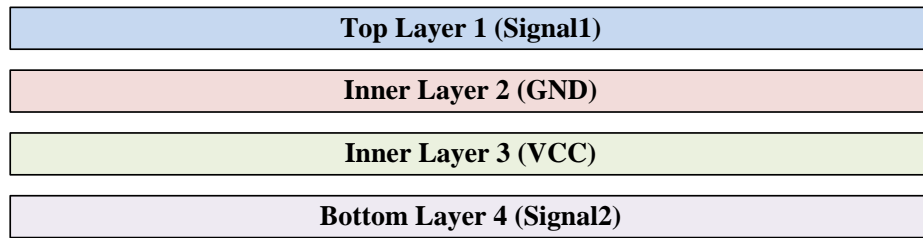


**Figure 20. Four-Layer Board Stack-Up**

The majority of signal traces must run on a single layer, preferably Signal 1. Immediately next to this layer must be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

## 11.2 Layout Example

### Example 4 layer PCB Stackup



- Via to layer 2 (GND)
- Via to layer 3 (VCC)
- Via to layer 4 (Signal)

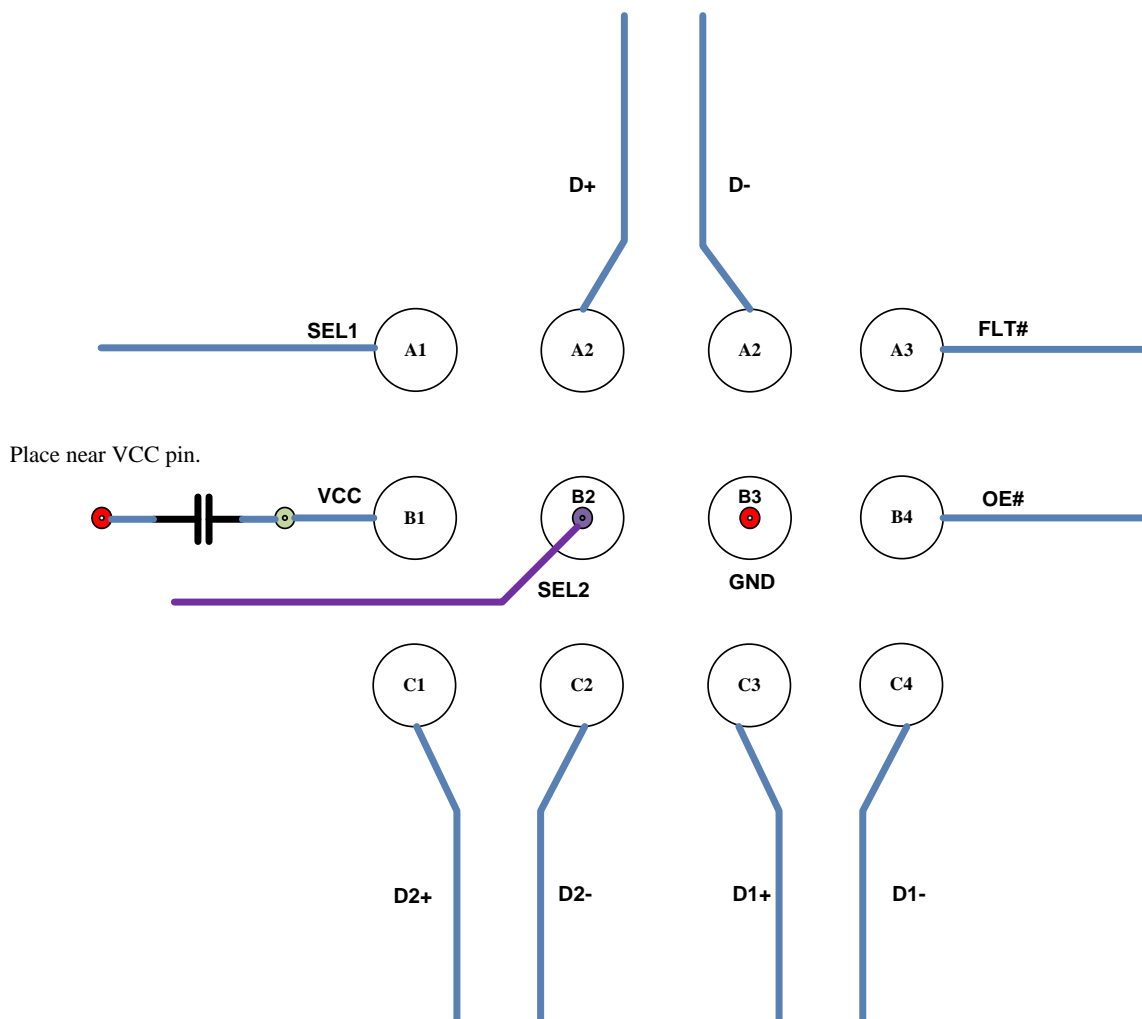


图 21. Layout Example

## 12 デバイスおよびドキュメントのサポート

### 12.1 ドキュメントのサポート

#### 12.1.1 関連資料

関連資料については、以下を参照してください。

- 『[USB 2.0基板の設計およびレイアウトのガイドライン](#)』
- 『[高速レイアウト・ガイドライン](#)』アプリケーション・レポート
- 『[高速インターフェイスのレイアウト・ガイドライン](#)』

### 12.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™オンライン・コミュニティ** *TIのE2E ( Engineer-to-Engineer )* コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

**設計サポート** *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

### 12.3 商標

E2E is a trademark of Texas Instruments.

USB Type-C is a trademark of USB Implementers Forum.

All other trademarks are the property of their respective owners.

### 12.4 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

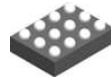
### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

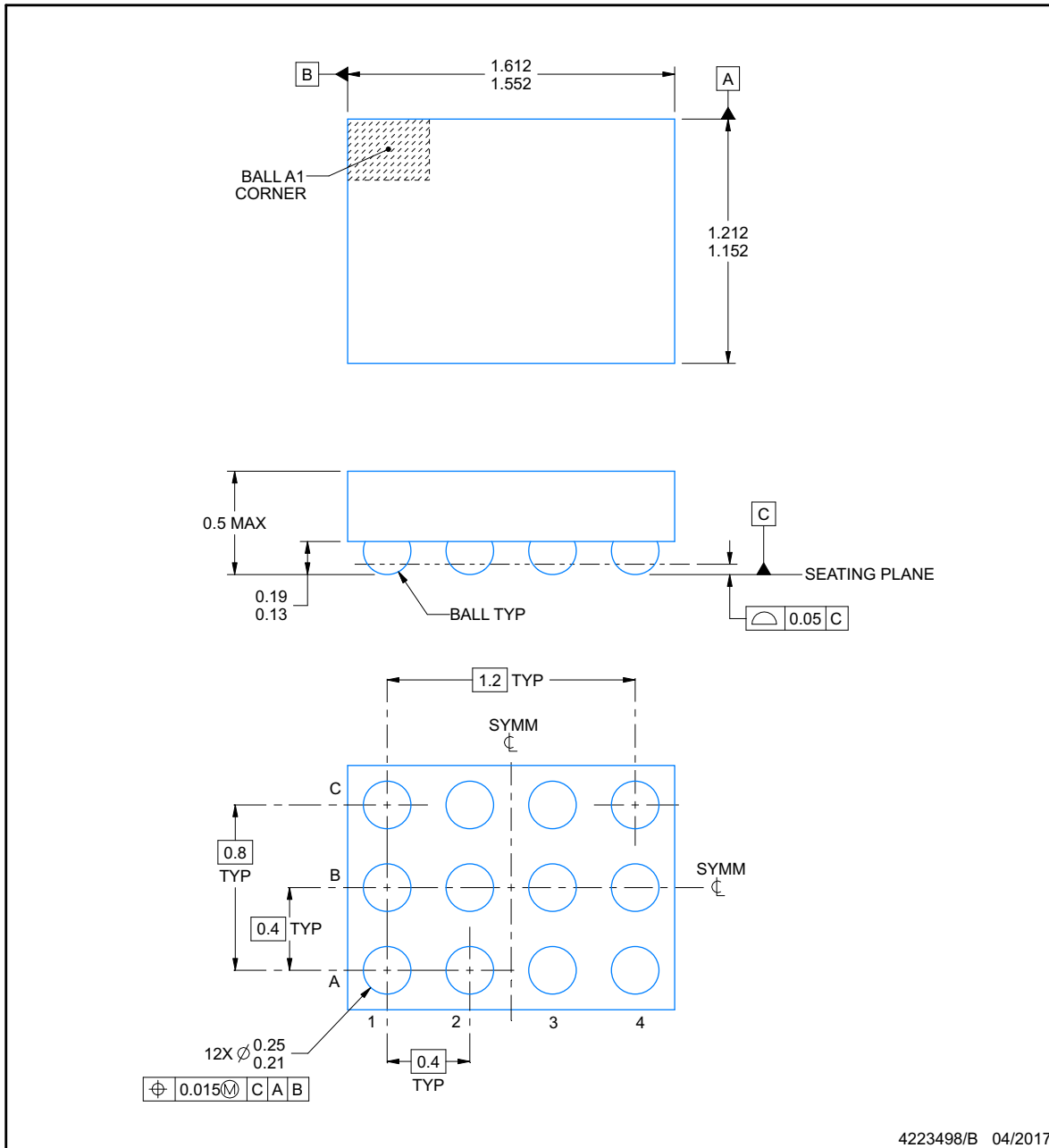


**PACKAGE OUTLINE**

**YFP0012-C01**

**DSBGA - 0.5 mm max height**

DIE SIZE BALL GRID ARRAY



**NOTES:**

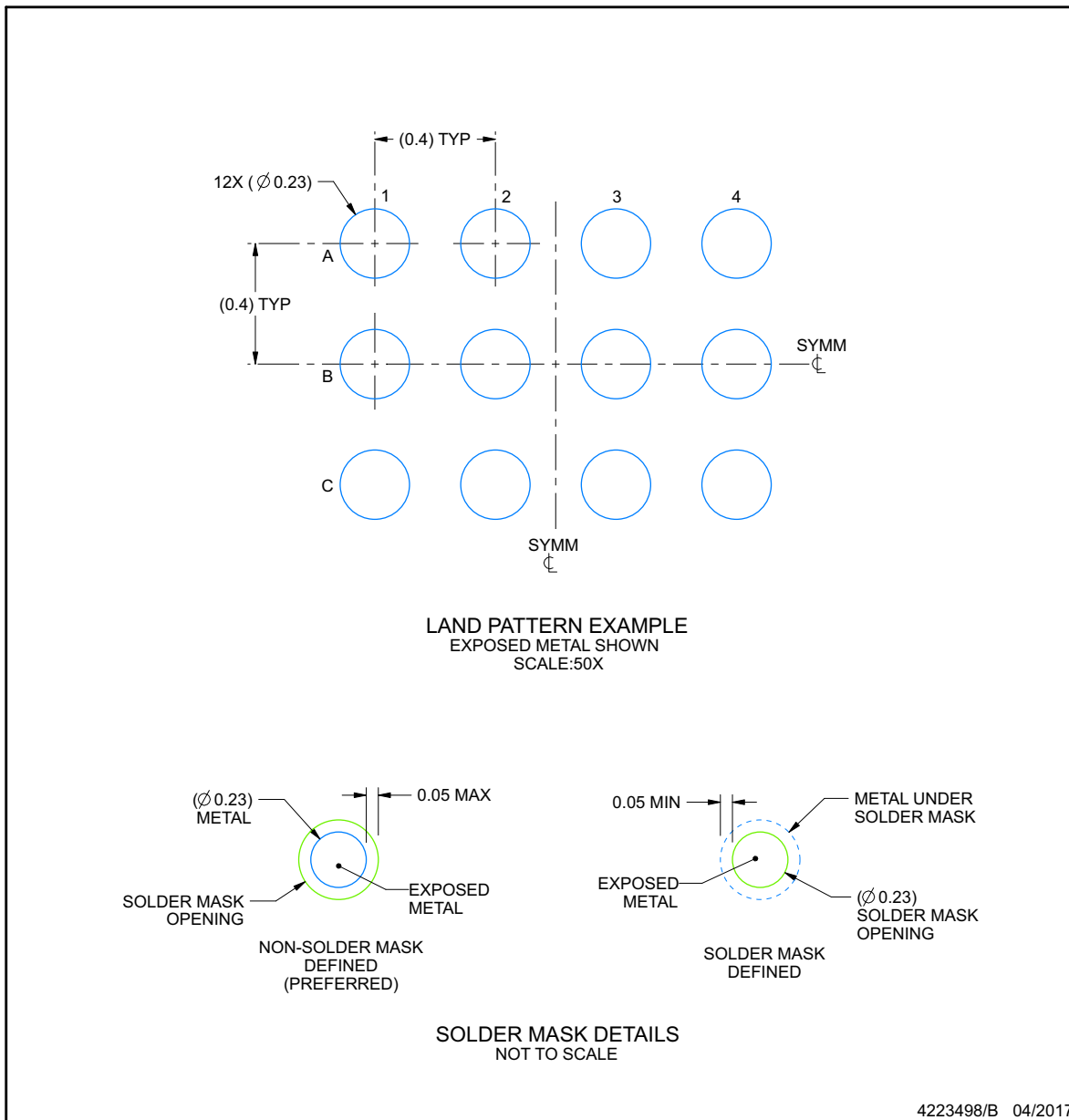
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

**EXAMPLE BOARD LAYOUT**

**YFP0012-C01**

**DSBGA - 0.5 mm max height**

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

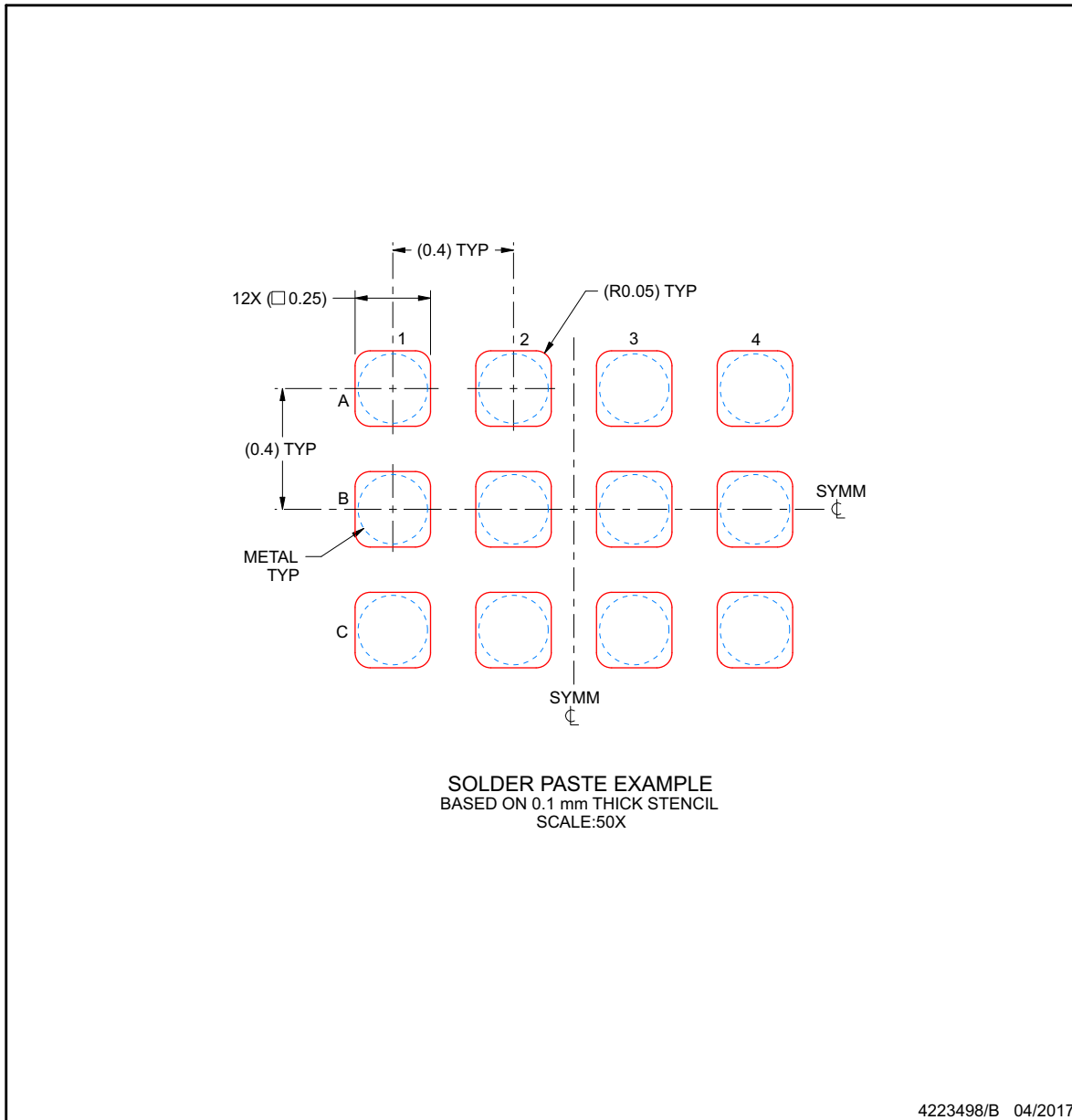
- 3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

**EXAMPLE STENCIL DESIGN**

**YFP0012-C01**

**DSBGA - 0.5 mm max height**

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

- 4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5USBC400IYFPR	ACTIVE	DSBGA	YFP	12	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	USB4	<a href="#">Samples</a>
TS5USBC400IYFPT	ACTIVE	DSBGA	YFP	12	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	USB4	<a href="#">Samples</a>
TS5USBC400YFPR	ACTIVE	DSBGA	YFP	12	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	0 to 70	USB4	<a href="#">Samples</a>
TS5USBC400YFPT	ACTIVE	DSBGA	YFP	12	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	0 to 70	USB4	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5USBC400IYFPR	DSBGA	YFP	12	3000	180.0	8.4	1.32	1.72	0.62	4.0	8.0	Q2
TS5USBC400IYFPT	DSBGA	YFP	12	250	180.0	8.4	1.32	1.72	0.62	4.0	8.0	Q2
TS5USBC400YFPR	DSBGA	YFP	12	3000	180.0	8.4	1.32	1.72	0.62	4.0	8.0	Q2
TS5USBC400YFPT	DSBGA	YFP	12	250	180.0	8.4	1.32	1.72	0.62	4.0	8.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5USBC400IYFPR	DSBGA	YFP	12	3000	182.0	182.0	20.0
TS5USBC400IYFPT	DSBGA	YFP	12	250	182.0	182.0	20.0
TS5USBC400YFPR	DSBGA	YFP	12	3000	182.0	182.0	20.0
TS5USBC400YFPT	DSBGA	YFP	12	250	182.0	182.0	20.0

## 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](https://www.ti.com) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2023, Texas Instruments Incorporated