TUSB1021-Q1 車載用 USB Type-C® 10Gbps リニア リドライバのマルチプレクサとデマルチプレクサ

1 特長

- USB Type-C® 2:1 または 1:2 リドライバ マルチプレクサ
- 最大 10Gbps の USB 3.2 をサポート
- 超低消費電力アーキテクチャ
- 5GHz で最大 13.3dB のイコライゼーションを備えたリニア リドライバ
- 16 のイコライゼーション設定
- GPIO または I²C により設定可能
- 1.8V または 3.3V の I²C 信号レベルをサポート
- ホットプラグ対応
- ホスト / デバイス側の要件が不要
- 3.3V 単一電源で動作
- 車載グレード 2 の温度範囲:-40℃～105℃
- パッケージ:5mm × 7mm、0.5mm ピッチの VQFN

2 アプリケーション

- 車載テスター
- 車載ヘッド ユニット
- 車載用インフォテインメントおよびクラスタ

3 概要

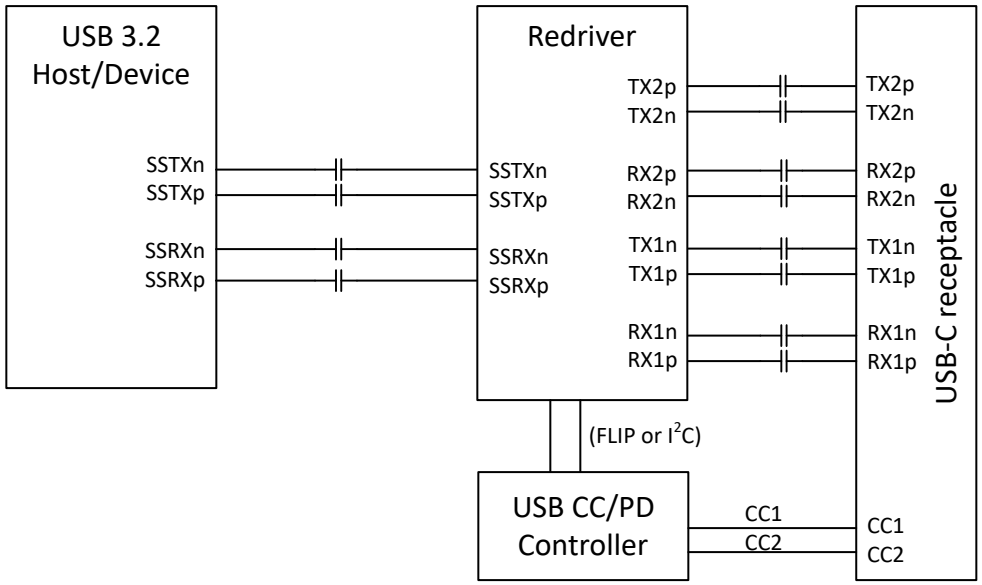
TUSB1021-Q1 は、リニア リドライバで、USB Type-C® アプリケーション向けに 1:2 デマルチプレクサまたは 2:1 マルチプレクサ機能を搭載しています。TUSB1021-Q1 は、ホストと USB-C® レセプタクルの間、または USB デバイスと USB-C® レセプタクルの間に設置することを意図しています。10 は、最大 TUSB1021-Q1Gbps の USB 3.2 データ レートに加えて、USB 3.2 の低消費電力状態 (切断、U1、U2、U3) をサポートしています。

TUSB1021-Q1 には、16 レベルの受信リニア イコライゼーションがあり、ケーブルおよび基板配線での損失によるシンボル間干渉 (ISI) を補償できます。このデバイスは単一の 3.3V 電源で動作し、車載グレード 2 の温度範囲に対応しています。

パッケージ情報

部品番号	パッケージ(1)	パッケージ サイズ(2)
TUSB1021-Q1	RGF (VQFN、40)	7mm × 5 mm

(1) 供給されているすべてのパッケージについては、セクション 12 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



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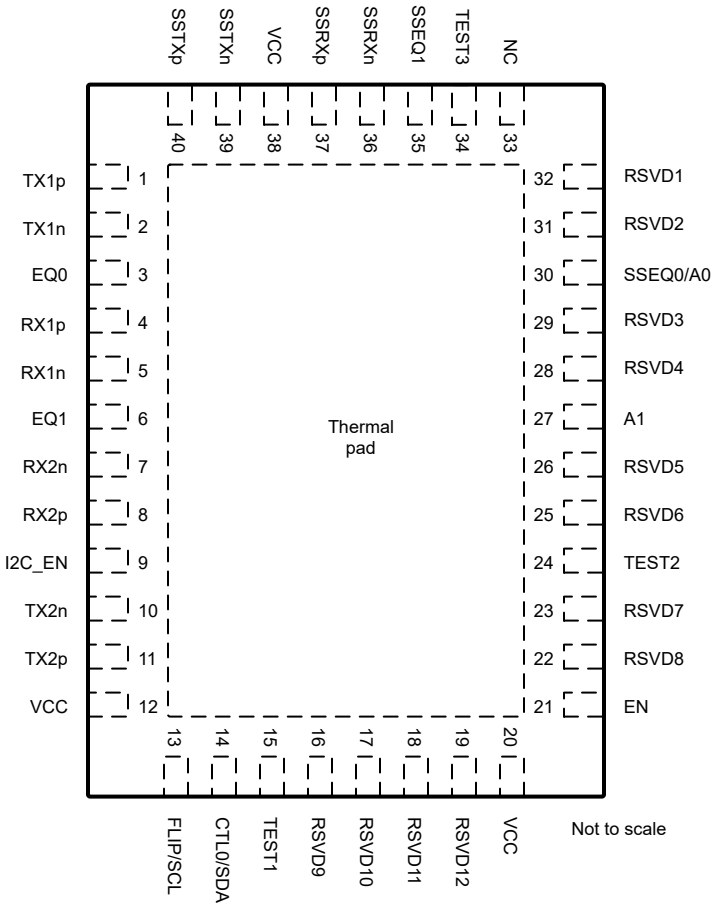


図 4-1. RGF Package, 40-Pin (VQFN) (Top View)

表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
RSVD1	32	O	Reserved. Leave unconnected.
RSVD2	31	O	Reserved. Leave unconnected.
RSVD3	29	O	Reserved. Leave unconnected.
RSVD4	28	O	Reserved. Leave unconnected.
RSVD5	26	O	Reserved. Leave unconnected.
RSVD6	25	O	Reserved. Leave unconnected.
RSVD7	23	O	Reserved. Leave unconnected.
RSVD8	22	O	Reserved. Leave unconnected.
TX1n	2	Diff O	Differential negative output. Connect to the TX1n pin on the Type-C receptacle through an external AC-coupling capacitor.
TX1p	1	Diff O	Differential positive output. Connect to the TX1p pin on the Type-C receptacle through an external AC-coupling capacitor.
RX1n	5	Diff I	Differential negative input. Connect to the RX1n pin on the Type-C receptacle through an external AC-coupling capacitor.
RX1p	4	Diff I	Differential positive input. Connect to the RX1p pin on the Type-C receptacle through an external AC-coupling capacitor.

表 4-1. Pin Functions (続き)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
RX2p	8	Diff I	Differential positive input. Connect to the RX2p pin on the Type-C receptacle through an external AC-coupling capacitor.
RX2n	7	Diff I	Differential negative input. Connect to the RX2p pin on the Type-C receptacle through an external AC-coupling capacitor.
TX2p	11	Diff O	Differential positive output. Connect to the TX2p pin on the Type-C receptacle through an external AC-coupling capacitor.
TX2n	10	Diff O	Differential negative output. Connect to the TX2n pin on the Type-C receptacle through an external AC-coupling capacitor.
SSTXp	40	Diff I	Differential positive input. Connect to the USB3.2 Host/Device transmitter through an external AC-coupling capacitor.
SSTXn	39	Diff I	Differential negative input. Connect to the USB3.2 Host/Device transmitter through an external AC-coupling capacitor.
SSRXp	37	Diff O	Differential positive output. Connect to the USB3.2 Host/Device receiver through an external AC-coupling capacitor.
SSRXn	36	Diff O	Differential negative output. Connect to the USB3.2 Host/Device receiver through an external AC-coupling capacitor.
EQ1	6	4 Level I	This pin along with EQ0 sets the USB receiver equalizer gain for RX1 and RX2. If not used, this pin can be left unconnected.
EQ0	3	4 Level I	This pin along with EQ1 sets the USB receiver equalizer gain for RX1 and RX2. If not used, this pin can be left unconnected.
EN	21	2 Level I (PD)	Device Enable. For normal operation, pull this pin up to 3.3V through a 10k to 50kΩ resistor.
TEST2	24	2 Level I	Test4. Connect directly to GND or pulldown with a 100k or less resistor.
I2C_EN	9	4 Level I	I^2C Programming Mode or GPIO Programming Select. I^2C is only disabled when this pin is "0". 0 = GPIO mode (I^2C disabled) R = TI Test Mode (I^2C enabled at 3.3V) F = I^2C enabled at 1.8V 1 = I^2C enabled at 3.3V.
RSVD9	16	I/O, CMOS	Reserved. Leave unconnected.
RSVD10	17	I/O, CMOS	Reserved. Leave unconnected.
RSVD11	18	I/O, CMOS	Reserved. Leave unconnected.
RSVD12	19	I/O, CMOS	Reserved. Leave unconnected.
TEST3	34	4 Level I	Test pin. Leave unconnected.
A1	27	4 Level I	When I2C_EN ≠ "0", this pin also sets the TUSB1021-Q1 I^2C address.
SSEQ1	35	4 Level I	Along with SSEQ0, sets the USB receiver equalizer gain for SSTXP/N receiver.
SSEQ0/A0	30	4 Level I	Along with SSEQ1, sets the USB receiver equalizer gain for SSTXP/N receiver. When I2C_EN ≠ "0", this pin also sets the TUSB1021-Q1 I^2C address. If I2C_EN = "F", then this pin must be set to "F" or "0".
FLIP/SCL	13	2 Level I (Failsafe) (PD)	When I2C_EN = "0", this is Flip control pin, L: normal orientation H: flip orientation When I2C_EN != "0", this pin is I^2C clock. When used for a I^2C clock, pull up to the VCC I2C supply on the I^2C controller.
CTL0/SDA	14	2 Level I (Failsafe) (PD)	When I2C_EN = "0", this is a USB3.2 control pin, L: USB disabled H: USB enabled When I2C_EN != "0", this pin is I^2C data. When used for I^2C data, pull up to the VCC I2C supply on the I^2C controller.
TEST1	15	2 Level I (PD)	Test. Leave unconnected or pulldown to GND.
VCC	12	P	3.3V Power Supply

表 4-1. Pin Functions (続き)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
VCC	20	P	3.3V Power Supply
VCC	38	P	3.3V Power Supply
NC	33	NC	No connect pin. Leave open.
GND	Thermal Pad	G	Ground

(1) I = input, O = output, Diff = differential, P = power, NC = no connection, G = ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature and voltage range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	–0.3	4	V
V_{IN_DIFF}	Differential voltage at differential inputs		±2.5	V
V_{IN_SE}	Input voltage at differential Inputs	–0.5	4	V
V_{IN_CMOS}	Input voltage at CMOS inputs	–0.3	4	V
T_J	Junction temperature		125	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1), all pins	±4000	V
		Charged device model (CDM), per AEC Q100-011, all pins	±1500	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature and voltage range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{CC_RAMP}	Power supply ramp	0.1		100	ms
V_{I2C}	Supply that external resistors on SDA and SCL are pulled up too	1.7		3.6	V
V_{PSN}	Power supply noise on VCC			100	mV
T_A	Ambient temperature	–40		105	°C
T_{PCB}	PCB temperature (1mm away from the device)	–40		112	°C

5.4 Thermal Information

THERMAL METRIC(1)		Device RGF (VQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	10.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power						
$P_{CC-ACTIVE-USB}$	Average active power in USB-only mode while in U0	CTL0 = H; Link in U0 at 10Gbps;		340		mW
$P_{CC-NC-USB}$	Average power in USB mode while in disconnect state.	CTL0 = H; No USB device detected;		2.5		mW
$P_{CC-U2U3}$	Average power in USB mode while in U2/U3 state	CTL0 = H; Link in U2 or U3;		2.5		mW
$P_{CC-SHUTDOWN}$	Average power in shutdown mode.	CTL0 = L; I2C_EN = "0";		0.7		mW
4-State CMOS Inputs(EQ[1:0], SSEQ[1:0], I2C_EN)						
I_{IH}	High-level input current	V_{CC} = 3.6V; V_{IN} = 3.6V	20		80	µA
I_{IL}	Low-level input current	V_{CC} = 3.6V; V_{IN} = 0V	–160		–40	µA
4-Level V_{TH}	Threshold 0 / R	V_{CC} = 3.3V		0.59		V
	Threshold R/ Float	V_{CC} = 3.3V		1.65		V
	Threshold Float / 1	V_{CC} = 3.3V		2.7		V
R_{PU}	Internal pullup resistance			45		kΩ
R_{PD}	Internal pulldown resistance			95		kΩ
2-State CMOS Input (EN, FLIP, CTL0) CTL0 and FLIP are Failsafe						
V_{IH}	High-level input voltage		2.2		3.6	V
V_{IL}	Low-level input voltage		0		0.8	V
R_{PD}	Internal pull-down resistance for FLIP, CTL0, and EN.			500		kΩ
I_{IH-EN}	High-level input current for EN pin	V_{IN} = 3.6V	4		12	µA
I_{IL-EN}	Low-level input current for EN pin	V_{IN} = GND, V_{CC} = 3.6V	–1		1	µA
$I_{IH-FLIP}$	High-level input current for FLIP pin	V_{IN} = 3.6V	4		12	µA
$I_{IL-FLIP}$	Low-level input current for FLIP pin	V_{IN} = GND, V_{CC} = 3.6V	–1		1	µA
$I_{IH-CTL0}$	High-level input current for CTL0 pin	V_{IN} = 3.6V	4		12	µA
$I_{IL-CTL0}$	Low-level input current for CTL0 pin	V_{IN} = GND, V_{CC} = 3.6V	–1		1	µA
I2C Control Pins SCL, SDA						
V_{IH}	High-level input voltage	I2C_EN = "1" or "R" (3.3V I2C levels)	2.2		3.6	V
V_{IL}	Low-level input voltage	I2C_EN = "1" or "R" (3.3V I2C levels)	0		0.8	V
V_{IH}	High-level input voltage	I2C_EN = "F" (1.8V I2C levels)	1.2		3.6	V
V_{IL}	Low-level input voltage	I2C_EN = "F" (1.8V I2C levels)	0		0.4	V
V_{OL}	Low-level output voltage	I2C_EN ! = "0"; I_{OL} = 3mA	0		0.4	V
I_{OL}	Low-level output current	I2C_EN ! = "0"; V_{OL} = 0.4V	20			mA
I_{i_I2C}	Input current on SDA pin	0.1 × V_{I2C} < Input voltage < 3.3V	–10		10	µA
C_{i_I2C}	Input capacitance				10	pF
USB Differential Receiver (RX1P/N, RX2P/N, SSTXP/N)						
$V_{RX-DIFF-PP}$	Input differential peak-peak voltage swing linear dynamic range	AC-coupled differential peak-to-peak signal measured post CTLE through a reference channel		1200		mVppd
$V_{RX-DC-CM}$	Common-mode voltage bias in the receiver (DC)			0		V
$R_{RX-DIFF-DC}$	Differential input impedance (DC)	Present after a USB3 device is detected on TXP/TXN	72		120	Ω

5.5 Electrical Characteristics (続き)

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{RX-CM-DC}$	Receiver DC common mode impedance	Present after a USB3 device is detected on TXP/TXN	18		30	Ω
$Z_{RX-HIGH-IMP-DC-POS}$	Common-mode input impedance with termination disabled (DC)	Present when no USB3 device is detected on TXP/TXN. Measured over the range of 0V to 500mV with respect to GND.	25			kΩ
$V_{SIGNAL-DET-DIFF-PP}$	Input differential peak-to-peak signal detect assert level	At 10Gbps, No loss and bit rate PRBS7 pattern		95		mVppd
$V_{RX-IDLE-DET-DIFF-PP}$	Input differential peak-to-peak signal detect de-assert level	At 10 Gbps, No loss and bit rate PRBS7 pattern		70		mVppd
$V_{RX-LFPS-DET-DIFF-PP}$	Low-frequency periodic signaling (LFPS) detect threshold	25℃ ≤ T_A ≤ 105℃; Below the minimum is squelched. Tested at 25MHz and 300mVppd VIN.	100		300	mVppd
$RL_{RX-DIFF}$	Differential return loss	50MHz to 1.25GHz at 90Ω; Lowest EQ setting; FLIP = L;		–23		dB
$RL_{RX-DIFF}$	Differential return loss	5GHz at 90Ω; Lowest EQ setting; FLIP = L;		–12		dB
RL_{RX-CM}	Common-mode return loss	50MHz to 5GHz at 90Ω; Lowest EQ setting; FLIP = L;		–8		dB
EQ_{SSP}	Receiver equalization for RX1/2 receivers at maximum setting	At 5GHz; FLIP = L;		13.3		dB
EQ_{SSP}	Receiver equalization for SSTX receiver at maximum setting	At 5GHz; FLIP = L;		10.5		dB
USB Differential Transmitter (TX1P/N, TX2P/N, SSRXP/N)						
$V_{TX-DIFF-PP}$	Transmitter dynamic differential voltage swing range.			1300		mVppd
$V_{TX-RCV-DETECT}$	Amount of voltage change allowed during Receiver Detection	At 3.3V			600	mV
$V_{TX-CM-IDLE-DELTA}$	Transmitter idle common-mode voltage change while in U2/U3 and not actively transmitting LFPS	Measured at the connector side of the AC-coupling capacitor with 50Ω load	–600		600	mV
$V_{TX-DC-CM}$	Common-mode voltage bias in the transmitter (DC)	In U0;	1.5		2.1	V
$V_{TX-CM-AC-PP-ACTIVE}$	TX AC common-mode voltage active	At 3.3V; Maximum mismatch from Txp+Txn for both time and amplitude			100	mVpp
$V_{TX-IDLE-DIFF-AC-PP}$	AC electrical idle differential peak-to-peak output voltage	At package pins after high-pass filter (HPF) to remove DC component; HPF = 1/LPF; No AC or DC signals are applied at RX terminals;	0		10	mV
$V_{TX-IDLE-DIFF-DC}$	DC electrical idle differential output voltage	At package pins after low-pass filter (LPF) to remove AC component; LPF = 1/HPF; No AC or DC signals are applied at RX terminals;	0		10	mV
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute DC common-mode voltage between U1 and U0	At package pin			200	mV
$R_{TX-DIFF}$	Differential impedance of the driver		75		120	Ω
R_{TX-CM}	Common-mode impedance of the driver	Measured with respect to AC ground over 0V to 500mV	18		30	Ω

5.5 Electrical Characteristics (続き)

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{AC-COUPLING}$	External AC-coupling capacitor		75		265	nF
$I_{TX-SHORT}$	TX short-circuit current	TX+/- shorted to GND			67	mA
$RL_{TX-DIFF}$	Differential return loss (SDD22)	50MHz to 1.25GHz at 90Ω; Lowest EQ setting; FLIP = L;		–25		dB
$RL_{TX-DIFF-5G}$	Differential return loss (SDD22)	5GHz at 90Ω; Lowest EQ setting; FLIP = L;		–12		dB
RL_{TX-CM}	Common-mode return loss (SCC22)	50MHz to 5GHz at 90Ω; Lowest EQ setting; FLIP = L;		–9		dB
AC Electrical Characteristics						
Crosstalk	Differential crosstalk between TX and RX signal pairs	At 5GHz; FLIP = L;		–39		dB
G_{LF}	Low-frequency voltage gain.	At 100MHz, 600mVpp V_{ID}	–0.25	0.6	1.5	dB
$G_{LF\_LFPS\_TX1/2}$	Low-frequency voltage gain for SSTX –> TX1/TX2 path	At 10MHz to 50MHz sine wave; 1.0Vpp V_{ID}; EQ = 0; FLIP = 0 and 1;	–0.5	0.8	1.6	dB
$CP_{1\ dB-LF}$	Low-frequency –1dB compression point	At 100MHz, 200mVpp < V_{ID} < 2000mVpp		1000		mVpp
$CP_{1\ dB-HF}$	High-frequency –1dB compression point	At 5GHz, 200mVpp < V_{ID} < 2000mVpp		770		mVpp
D_{J_10G}	TX output deterministic jitter	200mVpp < V_{ID} < 2000mVpp, PRBS7, 10Gbps, 10dB pre-channel and 1dB post-channel, Optimal EQ setting		0.07		UIpp

5.6 Timing Requirements

		MIN	NOM	MAX	UNIT
USB3					
$t_{IDLEEntry}$,	Delay from U0 to electrical idle		10		ns
$t_{IDLEExit\_U1}$	U1 exit time: break in electrical idle to the transmission of LFPS		6		ns
$t_{IDLEExit\_U2U3}$	U2/U3 exit time: break in electrical idle to transmission of LFPS		10		µs
t_{RXDET_INTVL}	RX detect interval while in disconnect			12	ms
$t_{IDLEExit\_DISC}$	Disconnect exit time		10		µs
t_{Exit_SHTDN}	Shutdown exit time (CTL0 = V_{CC}/2 to U2/U3)		1		ms
t_{DIFF_DLY}	Differential propagation delay (20% to 80% of differential voltage measured 1.7 inch from the output pin)			300	ps
$t_{PWRUPACTIVE}$	Time when Vcc reaches 70% to device active			1	ms
t_R, t_F	Output rise/fall time		40		ps
t_{RF-MM}	Output rise/fall time mismatch (20% to 80% of differential voltage measured 1.7 inch from the output pin)			5	ps

5.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I^2C (SDA and SCL)						
f_{SCL}	I^2C clock frequency				1	MHz

5.7 Switching Characteristics (続き)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{BUF}	Bus free time between START and STOP conditions		0.5			µs
t_{HDSTA}	Hold time after repeated START condition. After this period, the first clock pulse is generated		0.26			µs
t_{LOW}	Low period of the I^2C clock		0.5			µs
t_{HIGH}	High period of the I^2C clock		0.26			µs
t_{SUSTA}	Setup time for a repeated START condition		0.26			µs
t_{HDDAT}	Data hold time		0.004			µs
t_{SUDAT}	Data setup time		50			ns
t_R	Rise time of both SDA and SCL signals				120	ns
t_F	Device output fall time for SDA	30pF load	0.7		5	ns
t_{SUSTO}	Setup time for STOP condition		0.26			µs
C_b	Capacitive load for each bus line				100	pF

5.8 Typical Characteristics

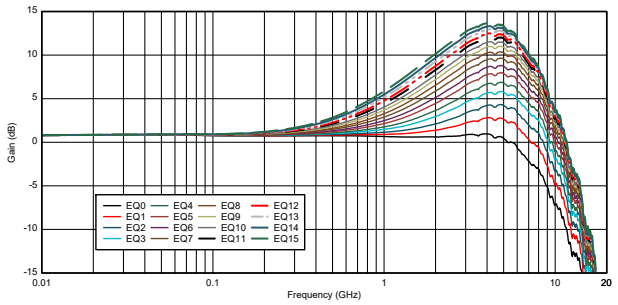


図 5-1. USB RX1 EQ Settings Curves

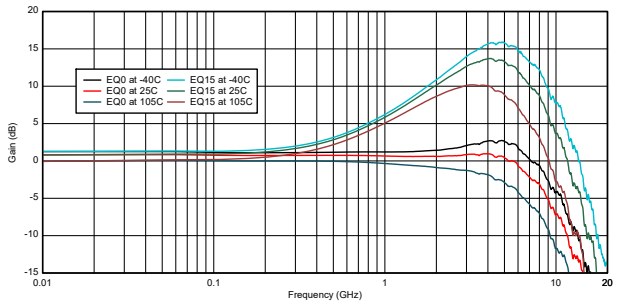


図 5-2. USB3 RX1 EQ0 and EQ15 Across Temperature

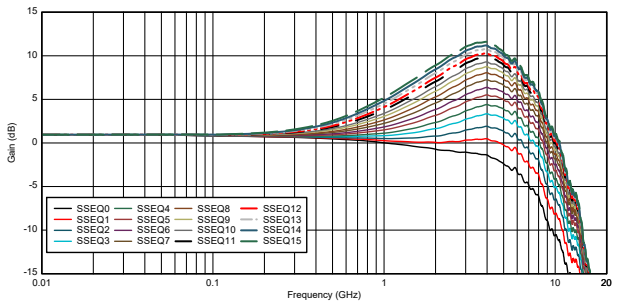


図 5-3. USB SSTX EQ Settings Curves

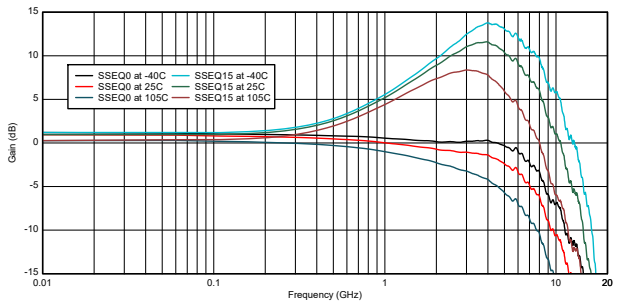


図 5-4. USB3 SSTX SSEQ0 and SSEQ15 Across Temperature

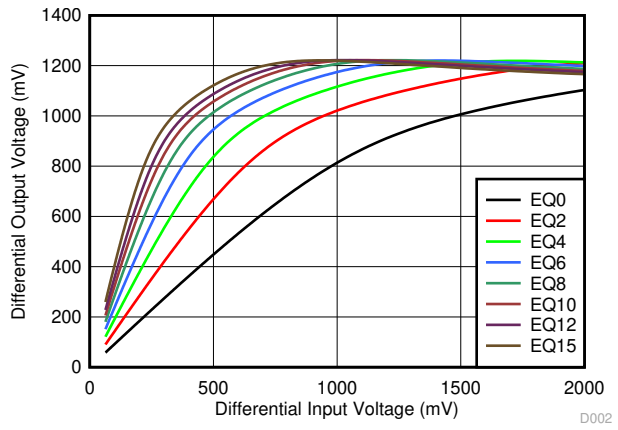


図 5-5. USB SSTX Linearity Curves at 5GHz

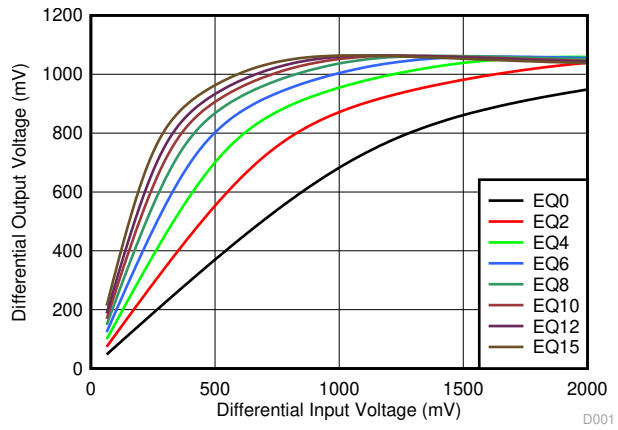


図 5-6. USB RX1 Linearity Curves at 5GHz

5.8 Typical Characteristics (continued)

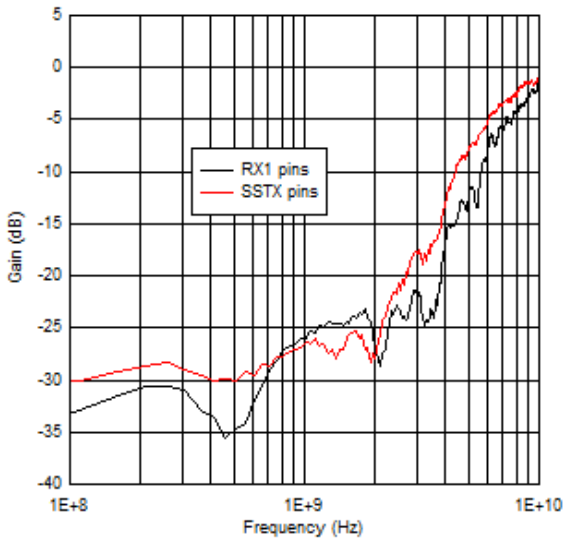


図 5-7. Input Return Loss Performance

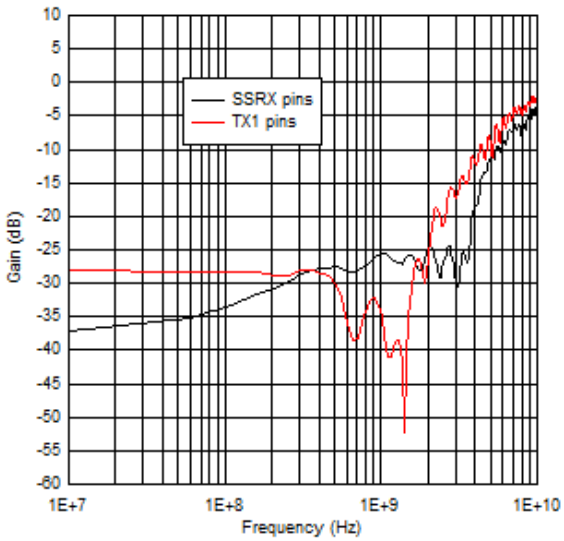


図 5-8. Output Return Loss Performance

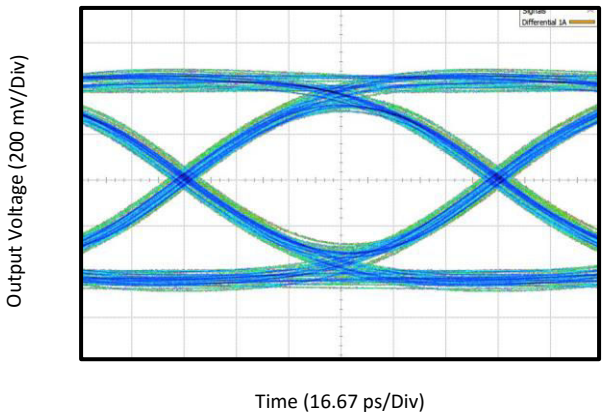


図 5-9. USB 3.2 Gen2 Eye-Pattern Performance with 12-Inch Input PCB Trace at 10Gbps

6 Parameter Measurement Information

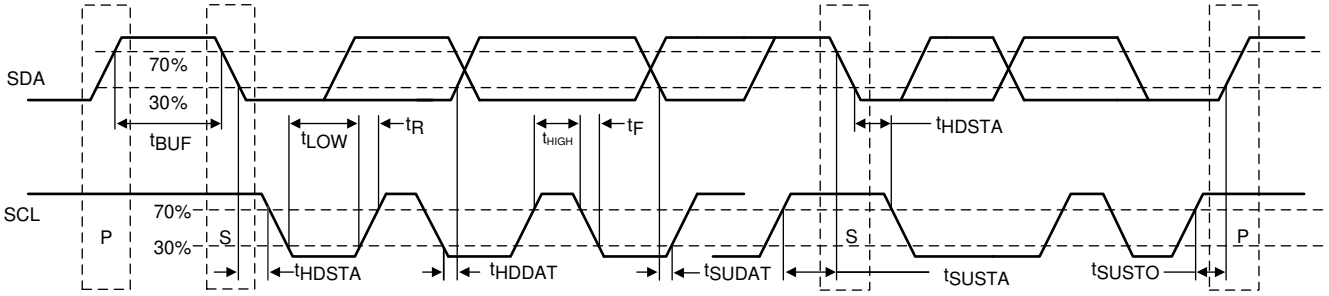


図 6-1. I²C Timing Diagram Definitions

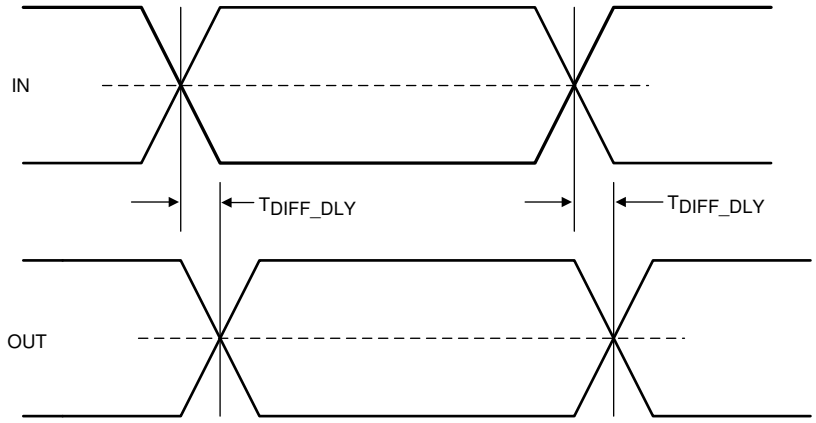


図 6-2. Propagation Delay

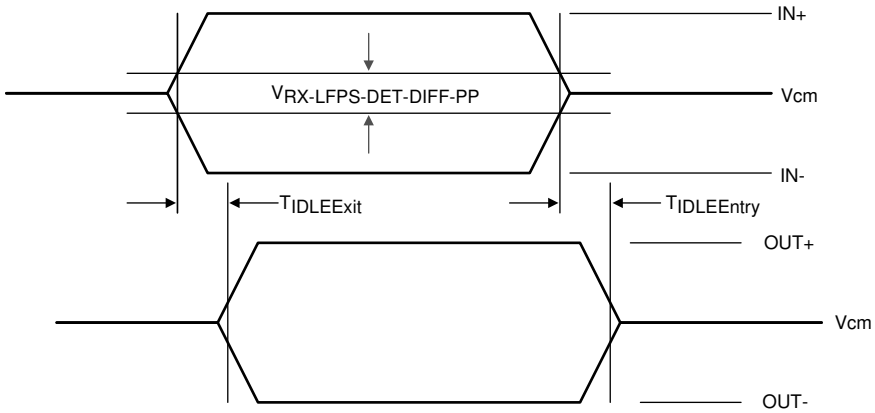


図 6-3. Electrical Idle Mode Exit and Entry Delay

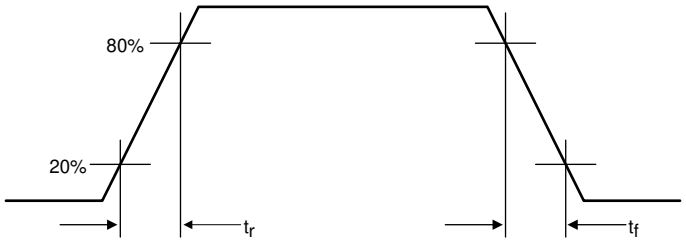


図 6-4. Output Rise and Fall Times

7 Detailed Description

7.1 Overview

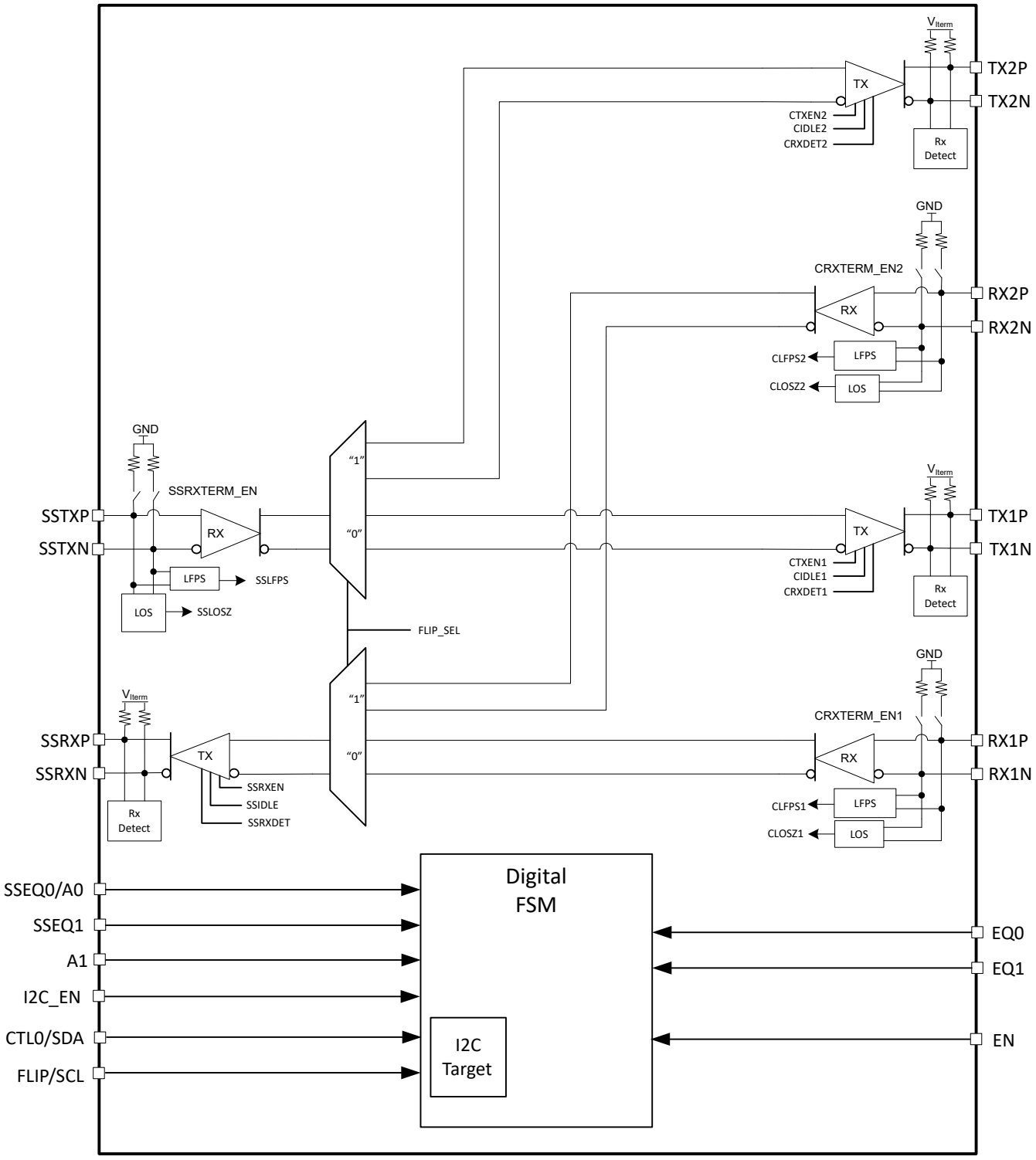
The TUSB1021-Q1 is a linear redriving switch that supports data rates up to 10Gbps. This device uses 5th generation USB redriver technology.

The TUSB1021-Q1 provides sixteen levels of receive equalization to compensate for cable and board trace loss which if not equalized causes inter-symbol interference (ISI) when USB 3.2 signals travel across a PCB or cable. This device requires a 3.3V power supply. The device comes in an automotive grade 2 temperature range.

The TUSB1021-Q1 enables the system to pass both transmitter compliance and receiver jitter tolerance tests for USB 3.2. The redriver recovers incoming data by applying equalization that compensates for channel loss, and drives out signals with a high differential voltage. Each channel has a receiver equalizer with selectable gain settings. Set the equalization based on the amount of insertion loss in the channels connected to the TUSB1021-Q1. Independent equalization control for each channel can be set using EQ[1:0] and SSEQ[1:0] pins.

The TUSB1021-Q1 advanced state machine makes the device transparent to hosts and devices. After power up, the TUSB1021-Q1 periodically performs receiver detection on the TX pairs. If the device detects a USB 3.2 receiver, the RX termination is enabled, and the TUSB1021-Q1 is ready to re-drive.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 USB 3.2

The TUSB1021-Q1 supports USB 3.2 up to 10Gbps. The TUSB1021-Q1 supports all the USB defined power states (U0, U1, U2, and U3). The TUSB1021-Q1 is a linear redriver, therefore the TUSB1021-Q1 cannot decode

USB3.2 physical layer traffic. The TUSB1021-Q1 monitors the actual physical layer conditions like receiver termination, electrical idle, LFPS, and SuperSpeed signaling rate to determine the USB power state of the USB 3.2 interface.

The TUSB1021-Q1 features an intelligent low-frequency periodic signaling (LFPS) detector. The LFPS detector automatically senses the low-frequency signals and disables receiver equalization functionality. When not receiving LFPS, the TUSB1021-Q1 enables receiver equalization based on the EQ[1:0] and SSEQ[1:0] pins or values programmed into EQ1_SEL, EQ2_SEL, and SSEQ_SEL registers.

7.3.2 4-Level Inputs

The TUSB1021-Q1 has (I2C_EN, EQ[1:0], and SSEQ[1:0]) 4-level inputs pins that are used to control the equalization gain and place TUSB1021-Q1 into different modes of operation. These 4-level inputs use a resistor divider to help set the four valid levels and provide a wider range of control settings. There is an internal 35kΩ pullup and a 95kΩ pulldown. These resistors, together with the external resistor connection combine to achieve the desired voltage level.

表 7-1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	Tie 1kΩ 5% to GND
R	Tie 20kΩ 5% to GND
F	Float (leave pin open)
1	Tie 1kΩ 5% to V_{CC}

注

All 4-level inputs are latched after the rising edge of internal reset. After t_{cfg_hd}, the internal pullup and pulldown resistors are isolated to save power.

7.3.3 Receiver Linear Equalization

The purpose of receiver equalization is to compensate for channel insertion loss and the resulting inter-symbol interference in the system before the input or after the output of the TUSB1021-Q1. The receiver overcomes these losses by attenuating the low-frequency components of the signals with respect to the high-frequency components. Select the proper gain setting to match the channel insertion loss. Two 4-level input pins enable up to 16 possible equalization settings. USB3.2 upstream path and USB3.2 downstream path each have two 4-level inputs. The TUSB1021-Q1 also provides the flexibility of adjusting settings through I^2C registers.

7.4 Device Functional Modes

7.4.1 USB 3.2 2:1 MUX Description

The TUSB1021-Q1 implements a 2:1 MUX between the USB-C receptacle and the USB 3.2 host, hub, or device. In pin-strap mode the selection of MUX path is controlled from the FLIP pin. In I^2C mode, the MUX is controlled by FLIP_SEL register.

表 7-2. USB 3.2 MUX Control

FLIP PIN OR FLIP_SEL REGISTER	CTL0 PIN OR CTLSEL REGISTER	USB PATH
X	0	Disabled
0	1	RX1 → SSRX
		SSTX → TX1
1	1	RX2 → SSRX
		SSTX → TX2

7.4.2 Linear EQ Configuration

Each of the TUSB1021-Q1 receiver lanes has individual controls for receiver equalization. The receiver equalization gain value can be controlled either through I^2C registers or through GPIOs. The following table details the gain value for each available combination when TUSB1021-Q1 is in GPIO mode. These same options are also available in I^2C mode by updating registers EQ1_SEL, EQ2_SEL, and SSEQ_SEL. Each of the 4-bit EQ configuration registers is mapped to the configuration pins as follows: x_SEL = {x1[1:0],x0[1:0]} where xn[1:0] are the EQ configuration pins with pin levels mapped to 2-bit values as: 0 = 00, R = 01, F = 10, 1 = 11.

表 7-3. TUSB1021-Q1 Receiver Equalization GPIO Control

EQUALIZATION SETTING #	RX1 and RX2 PORTS			SSTX PORT		
	EQ1 PIN LEVEL	EQ0 PIN LEVEL	EQ GAIN AT 5GHz (dB)	SSEQ1 PIN LEVEL	SSEQ0 PIN LEVEL	EQ GAIN AT 5GHz (dB)
0	0	0	0.4	0	0	–2.4
1	0	R	2.6	0	R	–0.2
2	0	F	4.2	0	F	1.3
3	0	1	5.7	0	1	2.8
4	R	0	6.7	R	0	3.8
5	R	R	7.9	R	R	4.9
6	R	F	8.7	R	F	5.8
7	R	1	9.5	R	1	6.6
8	F	0	10.2	F	0	7.3
9	F	R	10.9	F	R	7.9
10	F	F	11.4	F	F	8.4
11	F	1	11.9	F	1	8.9
12	1	0	12.2	1	0	9.3
13	1	R	12.6	1	R	9.7
14	1	F	12.9	1	F	10.0
15	1	1	13.3	1	1	10.5

7.4.3 USB3.2 Modes

The TUSB1021-Q1 monitors the physical layer conditions like receiver termination, electrical idle, LFPS, and SuperSpeed signaling rate to determine the state of the USB3.2 interface. Depending on the state of the USB 3.2 interface, the TUSB1021-Q1 can be in one of four primary modes of operation when USB 3.2 is enabled (CTL0 = H or CTLSEL0 = 1b1): Disconnect, U2/U3, U1, and U0.

The Disconnect mode is the state in which TUSB1021-Q1 has not detected far-end termination on upstream facing port (UFP) or downstream facing port (DFP). The Disconnect mode is the lowest power mode of each of the four modes. The TUSB1021-Q1 remains in this mode until far-end receiver termination has been detected on both UFP and DFP. The TUSB1021-Q1 immediately exits this mode and enter U0 after far-end termination is detected.

When in U0 mode, the TUSB1021-Q1 redrives all traffic received on UFP and DFP. U0 is the highest power mode of all USB3.1 modes. The TUSB1021-Q1 remains in U0 mode until electrical idle occurs on both UFP and DFP. Upon detecting electrical idle, the TUSB1021-Q1 immediately transitions to U1.

The U1 mode is the intermediate mode between U0 mode and U2/U3 mode. In U1 mode, the TUSB1021-Q1 UFP and DFP receiver termination remains enabled. The UFP and DFP transmitter DC common mode is maintained. The power consumption in U1 is similar to power consumption of U0.

Next to the Disconnect mode, the U2/U3 mode is next lowest power state. While in this mode, the TUSB1021-Q1 periodically performs far-end receiver detection. Anytime the far-end receiver termination is not detected on either UFP or DFP, the TUSB1021-Q1 leaves the U2/U3 mode and transitions to the Disconnect mode. The device also monitors for a valid LFPS. Upon detection of a valid LFPS, the TUSB1021-Q1 immediately transitions to the U0 mode. In U2/U3 mode, the TUSB1021-Q1 receiver terminations remain enabled but the TX DC common-mode voltage is not maintained.

7.4.4 Operation Timing – Power Up

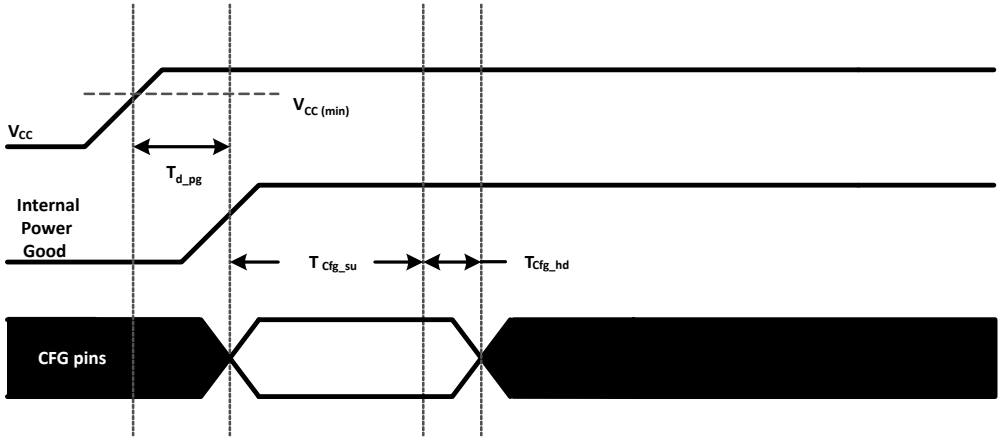


図 7-1. Power-Up Timing

表 7-4. Power-Up Timing (1) (2)

PARAMETER		MIN	MAX	UNIT
t_{d_pg}	V_{CC} (minimum) to Internal Power Good asserted high		500	µs
t_{cfg_su}	CFG(1) pins setup(2)	50		µs
t_{cfg_hd}	CFG(1) pins hold	10		µs
t_{VCC_RAMP}	V_{CC} supply ramp requirement (10% to 90%)	0.1	50	ms

(1) Following pins comprise CFG pins: I2C_EN, EQ[1:0], and SSEQ[1:0].
(2) Recommend CFG pins are stable when V_{CC} is at minimum value.

7.5 Programming

For further programmability, the TUSB1021-Q1 can be controlled using I^2C. The SCL and SDA pins are used for I^2C clock and I^2C data respectively.

表 7-5. TUSB1021-Q1 I^2C Target Address

A1 PIN LEVEL	SSEQ0/A0 PIN LEVEL	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (W/R)
0	0	1	0	0	0	1	0	0	0/1
0	R	1	0	0	0	1	0	1	0/1
0	F	1	0	0	0	1	1	0	0/1
0	1	1	0	0	0	1	1	1	0/1
R	0	0	1	0	0	0	0	0	0/1
R	R	0	1	0	0	0	0	1	0/1
R	F	0	1	0	0	0	1	0	0/1
R	1	0	1	0	0	0	1	1	0/1
F	0	0	0	1	0	0	0	0	0/1
F	R	0	0	1	0	0	0	1	0/1
F	F	0	0	1	0	0	1	0	0/1
F	1	0	0	1	0	0	1	1	0/1
1	0	0	0	0	1	1	0	0	0/1
1	R	0	0	0	1	1	0	1	0/1
1	F	0	0	0	1	1	1	0	0/1
1	1	0	0	0	1	1	1	1	0/1

7.5.1 TUSB1021-Q1 I²C Target Behavior

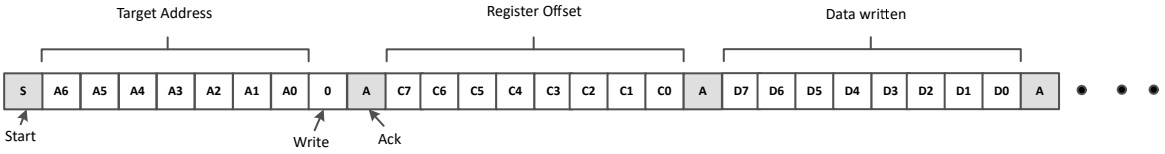


図 7-2. I²C Write with Data

Use the following procedure to write data to TUSB1021-Q1 I²C registers (refer to 図 7-2):

1. The controller initiates a write operation by generating a start condition (S), followed by the TUSB1021-Q1 7-bit address and a zero-value W/R bit to indicate a write cycle.
2. The TUSB1021-Q1 acknowledges the address cycle.
3. The controller presents the register offset within TUSB1021-Q1 to be written, consisting of one byte of data, MSB-first.
4. The TUSB1021-Q1 acknowledges the sub-address cycle.
5. The controller presents the first byte of data to be written to the I²C register.
6. The TUSB1021-Q1 acknowledges the byte transfer.
7. The controller can continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the TUSB1021-Q1.
8. The controller terminates the write operation by generating a stop condition (P).

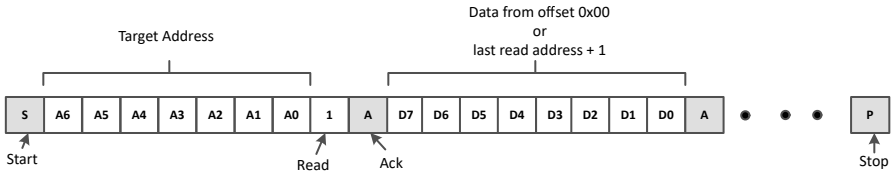


図 7-3. I²C Read Without Repeated Start

Use the following procedure to read the TUSB1021-Q1 I²C registers without a repeated Start (refer 図 7-3).

1. The controller initiates a read operation by generating a start condition (S), followed by the TUSB1021-Q1 7-bit address and a zero-value W/R bit to indicate a read cycle.
2. The TUSB1021-Q1 acknowledges the 7-bit address cycle.
3. Following the acknowledge the controller continues sending clock.
4. The TUSB1021-Q1 transmit the contents of the memory registers MSB-first starting at register 00h or last read register offset+1. If a write to the I²C register occurred prior to the read, then the TUSB1021-Q1 shall start at the register offset specified in the write.
5. The TUSB1021-Q1 waits for either an acknowledge (ACK) or a not-acknowledge (NACK) from the controller after each byte transfer; the I²C controller acknowledges reception of each data byte transfer.
6. If an ACK is received, the TUSB1021-Q1 transmits the next byte of data as long as controller provides the clock. If a NAK is received, the TUSB1021-Q1 stops providing data and waits for a stop condition (P).
7. The controller terminates the write operation by generating a stop condition (P).

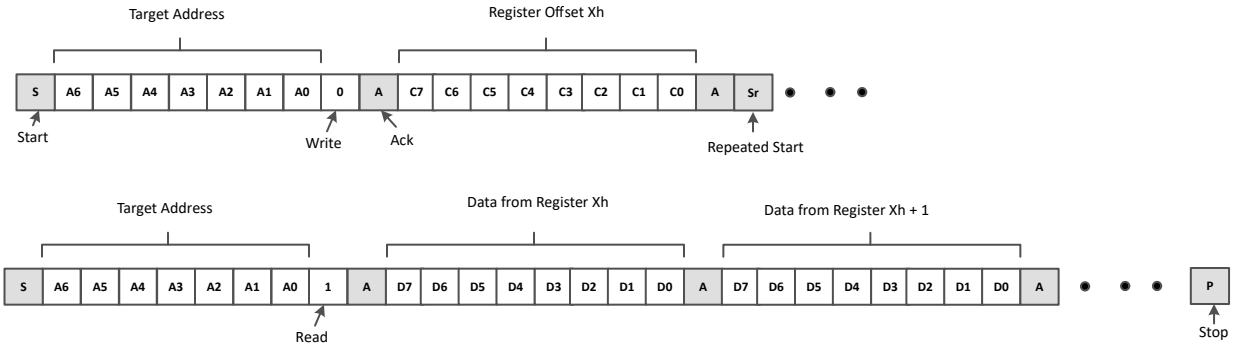


図 7-4. I²C Read with Repeated Start

Use the following procedure to read the TUSB1021-Q1 I²C registers with a repeated Start (refer 図 7-4).

1. The controller initiates a read operation by generating a start condition (S), followed by the TUSB1021-Q1 7-bit address and a zero-value W/R bit to indicate a write cycle.
2. The TUSB1021-Q1 acknowledges the 7-bit address cycle.
3. The controller presents the register offset within TUSB1021-Q1 to be written, consisting of one byte of data, MSB-first.
4. The TUSB1021-Q1 acknowledges the register offset cycle.
5. The controller presents a repeated start condition (Sr).
6. The controller initiates a read operation by generating a start condition (S), followed by the TUSB1021-Q1 7-bit address and a one-value W/R bit to indicate a read cycle.
7. The TUSB1021-Q1 acknowledges the 7-bit address cycle.
8. The TUSB1021-Q1 transmit the contents of the memory registers MSB-first starting at the register offset.
9. The TUSB1021-Q1 shall wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the controller after each byte transfer; the I²C controller acknowledges reception of each data byte transfer.
10. If an ACK is received, the TUSB1021-Q1 transmits the next byte of data as long as controller provides the clock. If a NAK is received, the TUSB1021-Q1 stops providing data and waits for a stop condition (P).
11. The controller terminates the read operation by generating a stop condition (P).

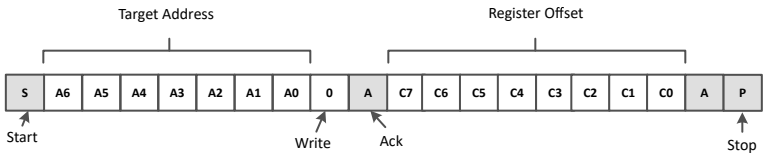


図 7-5. I²C Write Without Data

Use the following procedure to set a starting sub-address for I²C reads (refer to 図 7-5).

1. The controller initiates a write operation by generating a start condition (S), followed by the TUSB1021-Q1 7-bit address and a zero-value W/R bit to indicate a write cycle.
2. The TUSB1021-Q1 acknowledges the address cycle.
3. The controller presents the register offset within TUSB1021-Q1 to be written, consisting of one byte of data, MSB-first.
4. The TUSB1021-Q1 acknowledges the register offset cycle.
5. The controller terminates the write operation by generating a stop condition (P).

注

After initial power up, if no register offset is included for the read procedure (refer to 図 7-3), then reads start at register offset 00h and continue byte by byte through the registers until the I^2C controller terminates the read operation. During a read operation, the TUSB1021-Q1 auto-increments the I^2C internal register address of the last byte transferred independent of whether or not an ACK was received from the I^2C controller.

Software must only access (read or write) addresses detailed in this document. Accessing reserved or undocumented addresses can result in TUSB1021-Q1 entering an undefined state.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TUSB1021-Q1 is a linear redriver designed specifically to compensate for intersymbol interference (ISI) jitter causes by signal attenuation through a passive medium like PCB traces or cables. Placing the TUSB1021-Q1 between the USB connector and a USB 3.2 host, hub, and device can correct signal integrity issues resulting in a more robust system.

8.2 Typical Application

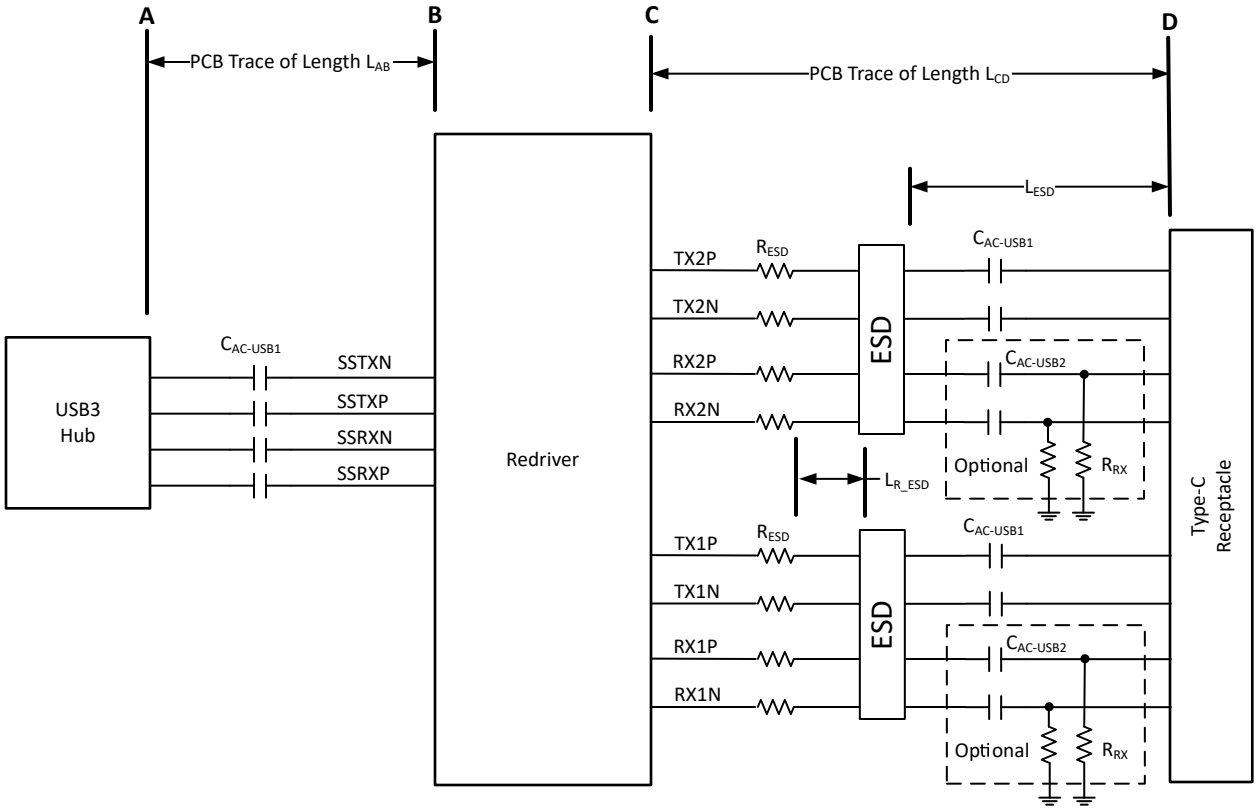


図 8-1. TUSB1021-Q1 in a Host Application

8.2.1 Design Requirements

For this design example, use the parameters shown in 表 8-1.

表 8-1. Design Parameters

PARAMETER(1)	VALUE
Pre-channel A to B PCB trace length, L_{AB}. Refer to 図 8-1.	1 inches ≤ L_{AB} ≤ 9 inches – L_{CD}
Post-channel C to D PCB trace length, L_{CD}. Refer to 図 8-1.	up to 3 inches
Maximum distance of ESD component from the USB receptacle, L_{ESD}	1.0 inches
Maximum distance of series resistor (R_{ESD}) from ESD component, L_{R_ESD}.	0.25 inches
$C_{AC-USB1}$ AC-coupling capacitor (75nF to 265nF)	220nF
$C_{AC-USB2}$ AC-coupling capacitor (297nF to 363nF)	Options: • RX1 and RX2 are DC-coupled to USB receptacle • 330nF AC-couple with R_{RX} resistor
Optional R_{RX} resistor (220kΩ ± 5%)	Not used
Optional R_{ESD} (0Ω to 2.2Ω)	0Ω
V_{CC} supply (3V to 3.6V)	3.3V
I^2C Mode or Pin-strap Mode	I^2C Mode. (MODE = "F")
1.8V or 3.3V I^2C Interface	3.3V I^2C. VIO_SEL pin to Float "F".

(1) Maximum trace length assumes an insertion loss of 0.2dB/inch/GHz. If insertion loss is more than 0.2dB/inch/GHz, then maximum trace length must be reduced accordingly.

8.2.2 Detailed Design Procedure

図 8-2 shows a typical usage of the TUSB1021-Q1 device. The device can be controlled either through the GPIO pins or the I^2C interface. In the example shown below, a Type-C PD controller is used to configure the device through the I^2C interface. In I^2C mode, the equalization settings for each receiver can be independently controlled through I^2C registers. For this reason, all of the equalization pins (EQ[1:0], SSEQ[1:0]) can be left unconnected. If these pins are left unconnected, the TUSB1021-Q1 7-bit I^2C target address is 0x12 because both A1 and SSEQ0/A0 are at pin level "F". If a different I^2C target address is desired, set the A1 and SSEQ0/A0 pins to a level which produces the desired I^2C target address.

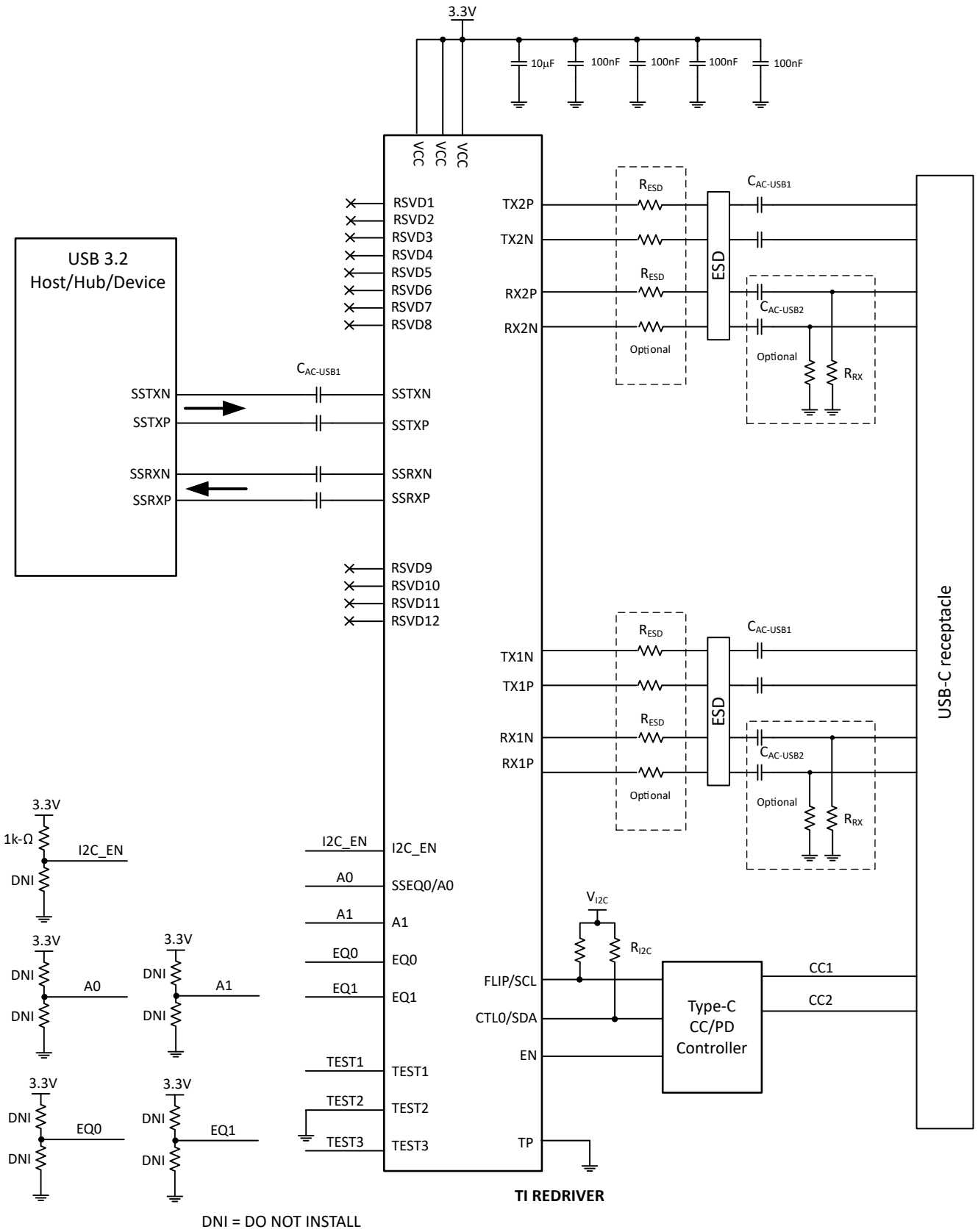


図 8-2. Application Circuit

8.2.2.1 ESD Protection

It may be necessary to incorporate an ESD component to protect the TUSB1021-Q1 from electrostatic discharge (ESD). TI recommends following the ESD protection recommendations listed in 表 8-2. A clamp voltage greater than value specified in 表 8-2 may require a R_{ESD} on each differential pin. Place the ESD component near the USB connector.

表 8-2. ESD Diodes Recommended Characteristics

PARAMETER	RECOMMENDATION
Breakdown voltage	≥ 3.5V
I/O line capacitance	Data rates ≤ 5Gbps: ≤ 0.50pF
	Data rates > 5Gbps: ≤ 0.35pF
Delta capacitance between any P and N I/O pins	≤ 0.07pF
Clamping voltage at 8A I_{PP} IO to GND (1)	≤ 4.5V
Typical dynamic resistance	≤ 30mΩ

(1) According to IEC 61000-4-5 (8/20µs current waveform)

表 8-3. Recommended ESD Protection Component

MANUFACTURER	PART NUMBER	R_{ESD} TO SUPPORT IEC 61000-4-2 CONTACT ±8kV
Nexperia	PUSB3FR4	1Ω
Nexperia	PESD2V8Y1BSF	1Ω
Texas Instruments	TPD1E04U04DPLR	2Ω
Texas Instruments	TPD4E02B04DQAR	2Ω

8.2.3 Application Curve

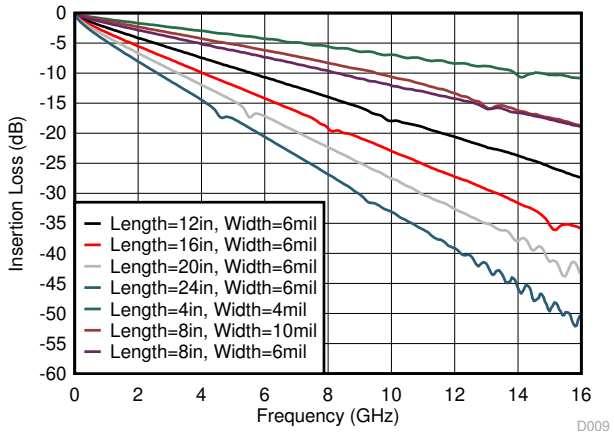


図 8-3. Insertion Loss of FR4 PCB Traces

8.3 Power Supply Recommendations

The TUSB1021-Q1 is designed to operate with a 3.3V power supply. Do not use levels above those listed in *Recommended Operating Conditions*. If using a higher voltage system power supply, a voltage regulator can be used to step down to 3.3V. Use decoupling capacitors to reduce noise and improve power supply integrity. Use a 0.1µF capacitor on each power pin.

8.4 Layout

8.4.1 Layout Guidelines

1. Reroute the RXP/N and TXP/N with controlled 90Ω differential impedance (±15%).
2. Keep away from other high speed signals.

3. Keep the intra-pair routing to within 2 mils.
4. Place length matching near the location of mismatch.
5. Separate each pair by at least 3 times the signal trace width.
6. Keep the use of bends in differential traces to a minimum. When bends are used, make sure to keep the number of left and right bends as equal as possible and the angle of the bend ≥ 135 degrees. This minimizes any length mismatch causes by the bends and therefore minimizes the impact bends have on EMI.
7. Route all differential pairs on the same of layer.
8. Keep the number of vias to a minimum. TI recommends to keep the via count to 2 or less.
9. Keep traces on layers adjacent to ground plane.
10. Do NOT route differential pairs over any plane split.
11. Note that adding test points can cause impedance discontinuity, and therefore negatively impact signal performance. If test points are used, place the points in series and symmetrically. The points must not be placed in a manner that causes a stub on the differential pair.

8.4.2 Layout Example

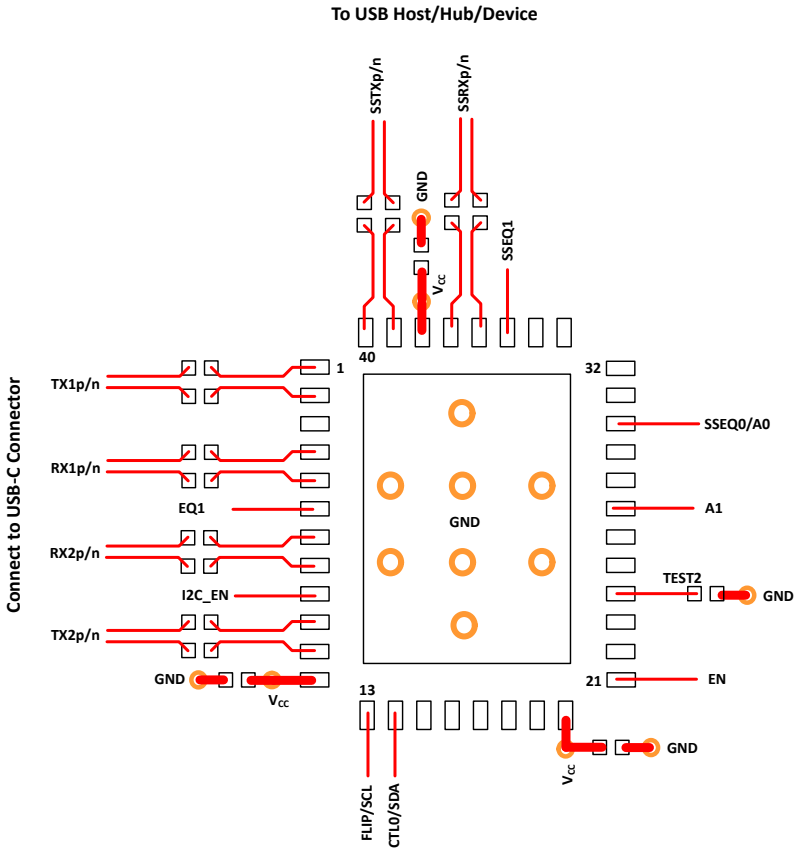


図 8-4. Layout Example

9 Register Maps

表 9-1. Register Legend

ACCESS TAG	NAME	MEANING
R	Read	The field may be read by software
W	Write	The field may be written by software
S	Set	The field may be set by a write of one. Writes of zeros to the field have no effect.
C	Clear	The field may be cleared by a write of one. Write of zero to the field have no effect.
U	Update	Hardware may autonomously update this field.
NA	No Access	Not accessible or not applicable

9.1 General Register (address = 0x0A) [reset = 00000001]

図 9-1. General Registers

7	6	5	4	3	2	1	0
Reserved		Reserved	EQ_OVERRIDE	Reserved	FLIP_SEL	Reserved	CTLSEL
R		R	R/W	R/W	R/W	R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9-2. General Registers

Bit	Field	Type	Reset	Description
7:5	Reserved.	R	00	Reserved.
4	EQ_OVERRIDE	R/W	0	Setting this field allows software to use EQ settings from registers instead of value sample from pins. 0: EQ settings based on sampled state of the EQ pins (SSEQ[1:0], EQ[1:0]). 1: EQ settings based on programmed value of each of the EQ registers
3	Reserved	R/W	0	Reserved
2	FLIP_SEL	R/W	0	FLIP_SEL. 0: Normal orientation 1: Flip orientation
1	Reserved	R/W	0	Reserved
0	CTLSEL	R/W	1	0: Disabled. All RX and TX are disabled. 1: USB3.1 enabled. (Default)

9.2 USB3.2 Control/Status Registers (address = 0x20) [reset = 00000000]

図 9-2. USB3.2 Control/Status Registers (0x20)

7	6	5	4	3	2	1	0
EQ2_SEL				EQ1_SEL			
R/W/U				R/W/U			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9-3. USB3.2 Control/Status Registers (0x20)

Bit	Field	Type	Reset	Description
7:4	EQ2_SEL	R/W/U	0000	Field selects EQ level for USB3.2 RX2 receiver. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of EQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for USB3.2 RX2 receiver based on value written to this field.

表 9-3. USB3.2 Control/Status Registers (0x20) (続き)

Bit	Field	Type	Reset	Description
3:0	EQ1_SEL	R/W/U	0000	Field selects EQ level for USB3.2 RX1 receiver. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of EQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for USB3.2 RX1 receiver based on value written to this field.

9.3 USB3.2 Control/Status Registers (address = 0x21) [reset = 00000000]

図 9-3. USB3.2 Control/Status Registers (0x21)

7	6	5	4	3	2	1	0
Reserved				SSEQ_SEL			
R				R/W/U			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9-4. USB3.2 Control/Status Registers (0x21)

Bit	Field	Type	Reset	Description
7:4	Reserved	R	0000	Reserved
3:0	SSEQ_SEL	R/W/U	0000	Field selects EQ for USB3.1 SSTXP/N receiver. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of SSEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for USB3.2 SSTXP/N receiver based on value written to this field.

9.4 USB3.2 Control/Status Registers (address = 0x22) [reset = 00000000]

図 9-4. USB3.2 Control/Status Registers (0x22)

7	6	5	4	3	2	1	0
CM_ACTIVE	LFPS_EQ	U2U3_LFPS_DEBOUNCE	DISABLE_U2U3_RXDET	DFP_RXDET_INTERVAL		USB3_COMPLIANCE_CTRL	
R/U	R/W	R/W	R/W	R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9-5. USB3.2 Control/Status Registers (0x22)

Bit	Field	Type	Reset	Description
7	CM_ACTIVE	R/U	0	0: Device not in USB 3.2 compliance mode. (Default) 1: Device in USB 3.2 compliance mode
6	LFPS_EQ	R/W	0	Controls whether settings of EQ based on EQ1_SEL, EQ2_SEL and SSEQ_SEL applies to received LFPS signal. 0: EQ set to zero when receiving LFPS (default) 1: EQ set to EQ1_SEL, EQ2_SEL, and SSEQ_SEL when receiving LFPS.
5	U2U3_LFPS_DEBOUNCE	R/W	0	0: No debounce of LFPS before U2/U3 exit. (Default) 1: 200µs debounce of LFPS before U2/U3 exit.
4	DISABLE_U2U3_RXDET	R/W	0	0: Rx.Detect in U2/U3 enabled. (Default) 1: Rx.Detect in U2/U3 disabled.
3:2	DFP_RXDET_INTERVAL	R/W	00	This field controls the Rx.Detect interval for the Downstream facing port (TX1P/N and TX2P/N). 00: 8ms 01: 12ms (default) 10: Reserved 11: Reserved

表 9-5. USB3.2 Control/Status Registers (0x22) (続き)

Bit	Field	Type	Reset	Description
1:0	USB3_COMPLIANCE_CTRL	R/W	00	00: FSM determined compliance mode. (Default) 01: Compliance Mode enabled in DFP direction (SSTX -> TX1/TX2) 10: Compliance Mode enabled in UFP direction (RX1/RX2 -> SSRX) 11: Compliance Mode Disabled.

10 Device and Documentation Support

10.1 ドキュメントの更新通知を受け取る方法

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10.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

DATE	REVISION	NOTES
September 2024	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB1021RGFRQ1	ACTIVE	VQFN	RGF	40	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TSB6421	Samples
TUSB1021RGFTQ1	ACTIVE	VQFN	RGF	40	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TSB6421	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
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(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

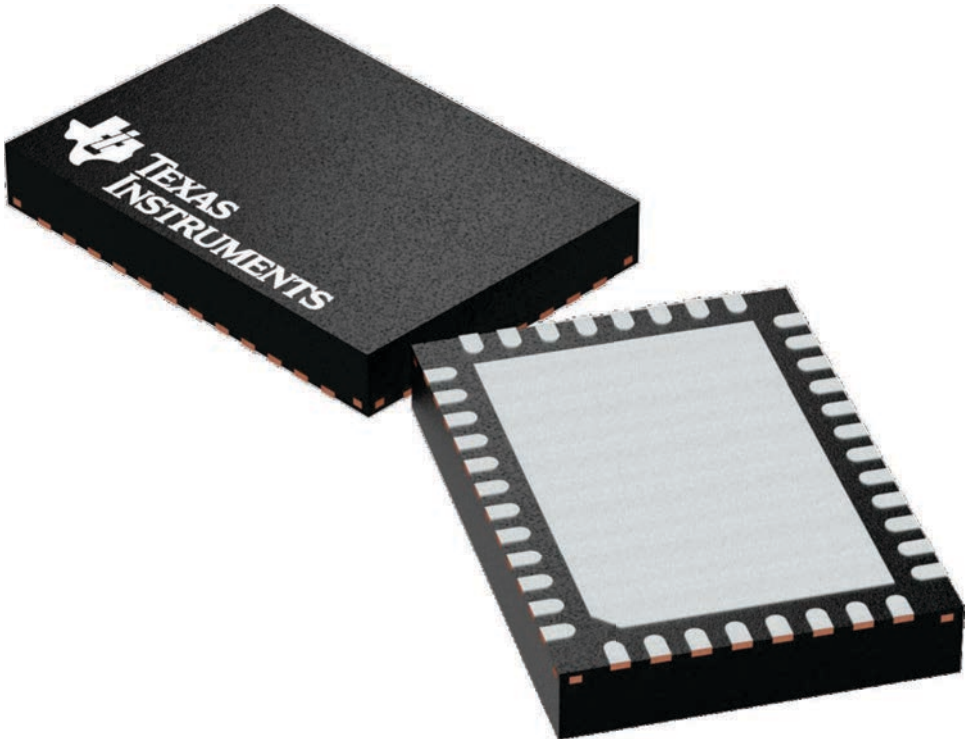
RGF 40

VQFN - 1 mm max height

5 x 7, 0.5 mm pitch

PLASTIC QUAD FLAT PACK- NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225115/A

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