

# TUSB2E11 USB 2.0-eUSB2 リピータ

## 1 特長

- USB 2.0 および eUSB2 (rev 1.2) に準拠
- ロースピード、フルスピード、ハイスピード信号伝送
- クラス最高の高速合計ジッタ: 20ps
- レジスタ アクセス プロトコル レセプタ対応
- ホスト モードおよびデバイス モードをサポート (デュアル ロール デバイス)
- I<sup>2</sup>C カストラップ ピンかを自動検出
  - USB 2.0 ハイスピード チャンネル補償設定用の 3 本のストラップピン
  - I<sup>2</sup>C デバイス インターフェイスを使用すると、より柔軟な設定が可能
- さまざまなデバイス バリエーションを用意
  - eUSB2 1.0V または 1.2V 信号インターフェイス
  - さまざまな eUSB2 トレース損失補償レベルで多様な製品フォーム ファクタに対応
  - 1.2V または 1.8V I<sup>2</sup>C インターフェイス
- オプションのバッテリー充電および検出サポート
  - BC 1.2 CDP または DCP デバイダ モードのアドバタイズ
  - データ認識型 USB Type-C™ 互換の BC 1.2 SDP、CDP、DCP デバイダ モード検出機能
  - チャージャのアドバタイズと検出を切り替えるデュアルロールの自動スイッチング
- CTA-936 USB CarKit UART のサポート
- 自動再開 ECR と L2 割り込み再開モードをサポート
- オプションの GPIO: 割り込み GPIO2、デバッグ、I<sup>2</sup>C ↔ GPIO0/1
- I<sup>2</sup>C からアクセスできる製造試験用のデバッグ機能

## 2 アプリケーション

- ノート PC およびデスクトップ PC
- 携帯電話
- タブレット
- ウェアラブル
- ポータブル・エレクトロニクス

## 3 概要

TUSB2E11 は、デバイス モードとホスト モードの両方をサポートする USB 規格準拠の eUSB2 - USB 2.0 リピータです。

このデバイスは、USB ロースピード (LS) 信号、フルスピード (FS) 信号、ハイスピード (HS) 信号をサポートしています。

このデバイスは、堅牢な相互運用性、最適な性能、消費電力を実現するために、特許申請中の複数の設計を採用しています。

I<sup>2</sup>C インターフェイスを使用しないシステムでは、このデバイスは最大 20Ω の USB 2.0 チャンネル等価直列抵抗 (ESR) に対応する 3 本のストラップピンによる 8 つの個別設定を提供します。このデバイスは、最大 10 インチまでのさまざまなレベルの eUSB2 トレース長補償機能を備えるバリエーションが利用可能です。

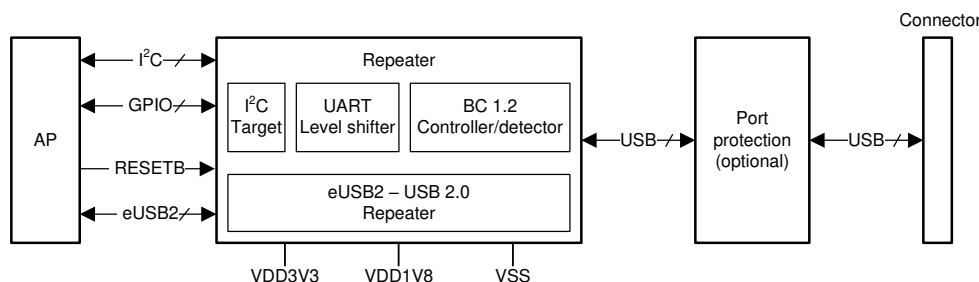
I<sup>2</sup>C インターフェイスを使用すると、さらに柔軟性が向上し、デバイスの RX イコライゼーションと TX 振幅、スループレート、プリエンファシスを微調整して、電気的適合性試験への対応とチャンネル損失の補償が可能です。

各種のデバッグ オプションが利用可能であり、3 本の GPIO ピンを使用してさまざまな USB バス状態や割り込みを監視するように構成できるほか、CTA-936 UART モードで SoC デバッグ機能を利用できます。GPIO0 および GPIO1 は、汎用 I<sup>2</sup>C から GPIO へのブリッジとして使用できます。

### パッケージ情報

部品番号 <sup>(1)</sup>	パッケージ <sup>(2)</sup>	パッケージサイズ <sup>(3)</sup>
TUSB2E11	YCG (DSBGA, 15)	1.75mm × 1.05mm

- (1) 製品比較表を参照してください。
- (2) 詳細については、セクション 14 を参照してください。
- (3) パッケージサイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



アプリケーション概略図



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## 4 Device Version Comparison

表 4-1. Device Register Comparison Table

	Register Address	B0 default	B1 default
表 10-5	0x70h	0x73h	0x7Ch
表 10-6	0x71h	0x38h	0x3Ch
表 10-7	0x72h	0x90h	0x92h
表 10-8	0x73h	0x04h	0x83h
表 10-9	0x77h	0x00h	0x00h
表 10-10	0x78h	0x0Bh	0x0Bh
表 10-11	0x79h	0x40h	0x60h
表 10-12	0x50h	0x02h	0x02h
表 10-13	0xB0h	0x02h	0x03h
表 10-14	0xB2h	0x00h	0x00h
表 10-15	0xB3h	0x00h	0x00h
表 10-16	0xB4h	0x00h	0x00h
表 10-18	0xB6h	0xC0h	0xC0h
表 10-22	0x60h	0x00h	0x00h
表 10-23	0xF5h	0x32h	0x32h

表 4-2. Device Feature Comparison Table

Features	B0	B1
Low Power Mode (RESETB = low)	not supported	supported (9 $\mu$ W)
Auto-resume ECR	not supported	supported (enabled by default) [see <a href="#">register 0x78h</a> ]
L2 State Interrupt Resume	supported	supported

## 4.1 Device Variants

The following table describes the key differences between TUSB2E11x device variants.

**表 4-3. Device Variant Information**

Orderable Device	Package Type	Package Drawing	Pins	Version	I/O Voltage <sup>(1)</sup>	Device Marking
TUSB2E111YCGR	WCSP	YCG	15	B1	1.8V	T2E111A
TUSB2E112YCGR	WCSP	YCG	15	B1	1.2V	T2E112

(1) **I/O Voltage:** I2C Bus voltage and GPIO voltage

For more information and availability of device variants such as eUSB2 1.0 signaling interface, 1.2V I<sup>2</sup>C interface, and 1.2V GPIO interface please contact [support](#).

## 5 Pin Configuration and Functions



図 5-1. TUSB2E11 YCG Package, 15-Pin DSBGA (Top View)

表 5-1. Pin Functions

PIN		TYPE <sup>(2)</sup>	REST STATE	ASSOCIATED ESD SUPPLY	DESCRIPTION
NAME	NO.				
VDD3V3	B2	PWR	N/A	N/A	3.3V Supply Voltage
VDD1V8	D2, E3	PWR	N/A	N/A	1.8V Supply Voltage
VSS	A3, D3	GND	N/A	N/A	GND
RESETB	D1	I	N/A	VDD1V8	<ul style="list-style-type: none"> <li>Active Low Reset</li> <li>Upon de-assertion of RESETB, the repeater is enabled and be in eUSB2 default mode awaiting configuration from eDSPr or eUSPr.</li> <li>If RESETB is not actively controlled, a pullup resistor 100kΩ to VDD1V8 is required.</li> </ul>

表 5-1. Pin Functions (続き)

PIN		TYPE <sup>(2)</sup>	REST STATE	ASSOCIATED ESD SUPPLY	DESCRIPTION				
NAME	NO.				SCL	SDA	Mode		
SCL	C3	I	Internal pulldown 1MΩ typical (disabled after reset) <sup>(1)</sup>	VDD1V8	I <sup>2</sup> C Clock	Device Mode Matrix	Low	See 表 5-4 for more details	Non-I <sup>2</sup> C USB Repeater
SDA	B3	I/O	Hi-Z <sup>(1)</sup>	VDD1V8			Bidirectional I <sup>2</sup> C data Open drain I/O	High	Low
								High	High
GPIO2	C2	I/O	Internal pulldown 1MΩ typical (disabled after reset)	VDD1V8	<ul style="list-style-type: none"> <li>In I<sup>2</sup>C mode GPIO2 is an open-drain active low level interrupt output. Connect GPIO2 to input of APU and a pullup resistor to use interrupt features</li> <li>In non I<sup>2</sup>C mode GPIO2 defaults to USB configuration input at power up reset.</li> <li>When a pullup resistor is used to set high input, ensure V<sub>IH</sub> is met accounting for internal pulldown as small as 500kΩ</li> <li>GPIO2 is an open-drain output after reset and can be left floating when not used.</li> </ul>				
GPIO0	B1	I/O	Internal pulldown 1MΩ typical (disabled after reset) <sup>(1)</sup>	VDD1V8	Defaults to an input mode at power up reset. RESETB assertion and de-assertion or soft reset reverts GPIO0 to input mode <ul style="list-style-type: none"> <li>In I<sup>2</sup>C mode GPIO0 defaults to control CarKit UART mode: active low to enable CarKit UART mode. Default CarKit UART direction is DP → eDP (RX) and eDN → DN (TX). GPIO0 must be pulled up to be in USB repeater mode.</li> <li>In non I<sup>2</sup>C mode GPIO0 defaults to USB configuration input at power up reset.</li> <li>When a pullup resistor is used to set high input, ensure V<sub>IH</sub> is met accounting for internal pulldown as small as 500kΩ</li> </ul>				
GPIO1	C1	I/O	Internal pulldown 1MΩ typical (disabled after reset) <sup>(1)</sup>	VDD1V8	Defaults to an input mode at power up reset. RESETB assertion and de-assertion or soft reset reverts GPIO1 to input mode <ul style="list-style-type: none"> <li>In I<sup>2</sup>C mode GPIO1 defaults to debug input</li> <li>In non I<sup>2</sup>C mode GPIO1 defaults to USB Configuration input at power up reset.</li> <li>When a pullup resistor is used to set high input, ensure V<sub>IH</sub> is met accounting for internal pulldown as small as 500kΩ</li> </ul>				
eDN	A2	I/O	Hi-Z	VDD1V8	eUSB2 port D-				
eDP	A1	I/O	Hi-Z	VDD1V8	eUSB2 port D+				
DN	E2	I/O	Hi-Z	VDD3V3	USB port D-				
DP	E1	I/O	Hi-Z	VDD3V3	USB port D+				

(1) When configured as an input but not actively driven, use 1MΩ external pulldown to strap low.

(2) I = input, I/O = input or output, PWR= power, GND = ground

表 5-2. Pin Configuration for Device Mode

Device Mode	SCL (C3)	SDA (B3)	GPIO0 (B1)	GPIO1 (C1)	GPIO2 (C2)
I <sup>2</sup> C Mode	Pull-up Input sampled at reset	Pull-up Input sampled at reset	Default to Input <ul style="list-style-type: none"> <li>• Low = UART Mode</li> <li>• High = USB repeater mode</li> </ul> Function can be reconfigured through register	Default to Input Function can be reconfigured through register	Default to Open drain output (can be left floating when not used) Function can be reconfigured through register
Non I <sup>2</sup> C UART mode	Pull-up Input sampled at reset	Pull-down Input sampled at reset	Default to Input <ul style="list-style-type: none"> <li>• Low = UART transfer enabled</li> <li>• High = UART transfer disabled</li> </ul>	High-Z (can be left floating)	High-Z (can be left floating)
Non I <sup>2</sup> C USB repeater mode	Pull-down Input sampled at reset See 表 5-4	See 表 5-4	Default input sampled at reset. See 表 5-3		

**表 5-3. Pin Configuration for USB PHY Tuning without I<sup>2</sup>C**

GPIO2	GPIO1	GPIO0	Equivalent series resistance (ESR) between repeater and USB connector	U_EQ_P1 setting	U_HS_TX_AMPLITUDE_P1 setting	U_HS_TX_PRE_EMPHASIS_P1 setting	U_SQUELCH_THRESHOLD_P1 setting	U_DISCONNECT_THRESHOLD_P1 setting	HS Term
			Ω	dB	mV	dB	mV	mV	
Float	Float	Float	2.5	0.06	840	0.5	104	625	45
				(3'b000)	(4'b0101)	(3'b000)	(3'b100)	(4'b0101)	
Float	Float	Pull-Up	5	0.06	880	0.9	98	645	45
				(3'b000)	(4'b0111)	(3'b001)	(3'b101)	(4'b0110)	
Float	Pull-Up	Float	7.5	0.58	900	0.9	98	645	45
				(3'b001)	(4'b1000)	(3'b001)	(3'b101)	(4'b0110)	
Float	Pull-Up	Pull-Up	10	1.09	920	0.9	98	685	45
				(3'b010)	(4'b1001)	(3'b001)	(3'b101)	(4'b1000)	
Pull-Up	Float	Float	12.5	1.56	940	1.2	91	685	45
				(3'b011)	(4'b1010)	(3'b010)	(3'b110)	(4'b1000)	
Pull-Up	Float	Pull-Up	15	2.26	980	1.2	91	685	45
				(3'b100)	(4'b1100)	(3'b010)	(3'b110)	(4'b1000)	
Pull-Up	Pull-Up	Float	17.5	2.67	1000	1.7	91	685	45
				(3'b101)	(4'b1101)	(3'b011)	(3'b110)	(4'b1000)	
Pull-Up	Pull-Up	Pull-Up	20	2.67	1020	1.7	85	705	42.75
				(3'b101)	(4'b1110)	(3'b011)	(3'b111)	(4'b1001)	

表 5-4. Pin Configuration for Battery Charging in non I<sup>2</sup>C Mode

Device Mode			Repeater State			Charger Detection Status	VBUS Control Output
	SCL (C3)	SDA (B3)	Unconfigured	Host Repeater	Peripheral Repeater	{GPIO2, GPIO1}	GPIO0
Non I <sup>2</sup> C USB repeater mode	Pull-down resistor to ground 0 to 160Ω	Input <ul style="list-style-type: none"> <li>Low = BC 1.2 disabled</li> <li>High = BC 1.2 enabled</li> </ul>	When BC 1.2 is enabled, charger detection	N/A	N/A	<ul style="list-style-type: none"> <li>2'b00: No charger detected</li> <li>2'b01: CDP or DCP charger detected</li> </ul>	N/A
Non I <sup>2</sup> C USB repeater mode	Pull-down resistor to ground 1.5kΩ to 2kΩ	Input VBUS_Valid input: use a voltage divider to reduce VBUS voltage to appropriate VIH for 1.8V or 1.2V I/O mode.	When VBUS_valid is high enable charger detection	N/A	Charger detection is enabled	<ul style="list-style-type: none"> <li>2'b10: DCP (1.5A) or Divider Mode (2.1A) charger detected</li> <li>2'b11: Divider Mode (2.4A) charger detected</li> </ul>	
Non I <sup>2</sup> C USB repeater mode	Pull-down resistor to ground 3.4kΩ to 3.96kΩ	Input <ul style="list-style-type: none"> <li>Low = BC 1.2 disabled</li> <li>High = BC 1.2 enabled</li> </ul>	When BC 1.2 is enabled, advertise charging BC 1.2 DCP	Advertise CDP	N/A	N/A	Active High Push-Pull output for VBUS switch Control
Non I <sup>2</sup> C USB repeater mode	Pull-down resistor to ground 7.5kΩ to 11kΩ	Input <ul style="list-style-type: none"> <li>Low = BC 1.2 disabled</li> <li>High = BC 1.2 enabled</li> </ul>	When BC 1.2 is enabled, advertise charging (auto cycle between BC 1.2 DCP and Divider mode)	Advertise CDP	N/A	N/A	<ul style="list-style-type: none"> <li>High = VBUS ON</li> <li>Low = VBUS OFF</li> </ul>



## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage range	V <sub>DD3V3</sub>	-0.3	4.32	V
Analog Supply voltage range	V <sub>DD1V8</sub>	-0.3	2.1	V
Voltage range	DP, DN, (with OVP enabled), 1000 total number of short events and cumulative duration of 1000 hrs.	-0.3	6	V
Voltage range	eDP, eDN	-0.3	1.6	V
Voltage range	RESETB, GPIO0, GPIO1, GPIO2, SCL, SDA	-0.3	2.1	V
Junction temperature	T <sub>J(max)</sub>		125	°C
Storage temperature	T <sub>stg</sub>	-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±1500	V
		Charged device model (CDM), per JEDEC specification JS-002, all pins <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>DD3V3</sub>	Supply voltage (VDD3V3)	3.0	3.3	3.6	V
V <sub>DD1V8</sub>	Analog Supply voltage (VDD1V8)	1.62	1.8	1.98	V
V <sub>I2C_Pullup</sub>	I2C and GPIO open drain Bus Voltage (1.2 V Variant)	1.08	1.2	1.32	V
V <sub>I2C_Pullup</sub>	I2C and GPIO open drain Bus Voltage (1.8 V Variant)	1.62	1.8	1.98	V
USB Voltage	DP, DN	0		3.6	V
eUSB2 voltage	eDP, eDN	0		1.32	V
Digital voltage	GPIO0, GPIO1, GPIO2, SCL, SDA (1.8 V Variant)	0		1.98	V
Digital voltage	GPIO0, GPIO1, GPIO2, SCL, SDA (1.2 V Variant)	0		1.32	V
RESETB	RESETB (1.2 V or 1.8 V Variant)	0		1.98	V
T <sub>A</sub>	Operating free-air temperature	-20		85	°C
T <sub>J</sub>	Junction temperature	-20		105	°C
T <sub>CASE</sub>	Case temperature	-20		105	°C

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T <sub>PCB</sub>	PCB temperature (1 mm away from the device)	-20		92	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TUSB2E11	UNIT
		YCG (DSBGA)	
		15 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	90.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	0.6	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	22.9	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.4	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	22.9	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER</b>						
P <sub>WC_1V8</sub>	Absolute worst case peak power consumption (VDD1V8 only) for power supply budgeting	I2C interface active, GPIOs in output mode, repeater in HS mode with USB transmitting, maximum RX EQ, max TX VOD and PE settings, maximum transition density. T <sub>A</sub> = -20°C to 85°C.			280	mW
P <sub>WC_3V3</sub>	Absolute worst case peak power consumption (VDD3V3 only) for power supply budgeting	I2C interface active, GPIOs in output mode, repeater in HS mode with USB transmitting, maximum RX EQ, max TX VOD and PE settings, maximum transition density. T <sub>A</sub> = -20°C to 85°C.			30	mW
P <sub>WCFS_3V3</sub>	Absolute worst case peak power consumption (VDD3V3 only) for power supply budgeting	I2C interface active, GPIOs in output mode, repeater in FS mode with USB Asynchronous traffic. T <sub>A</sub> = -20°C to 85°C.			75	mW
P <sub>HS_IOC</sub>	USB Audio ISOC High-speed	Maximum TX Vod/Maximum TX PE for both USB and eUSB2. Averaged over 8 ms and only 1 uFrame with data packet. Toff threshold = 1/32. Host Peripheral Mode.		35		mW
P <sub>PD</sub>	Powered down	Device powered, RESETB=Low, T <sub>A</sub> =25°C, (DP/DN Voltage ≤ VDD3V3).			9	μW
P <sub>Disabled</sub>	Disabled	Device powered, I2C/GPIO interfaces functional but idle, repeater is disabled and put into the lowest power state and non-functional. T <sub>A</sub> =25°C, (DP/DN Voltage ≤ VDD3V3).		43	95	μW
P <sub>Detach</sub>	USB unconnected	I2C/GPIO interfaces idle, repeater is connected to a eUSB2 PHY and waiting for a USB attach event. T <sub>A</sub> = 25°C, (DP/DN Voltage ≤ VDD3V3)		43	85	μW
P <sub>Suspend</sub>	L2 Suspend (host mode)	I2C/GPIO interfaces idle, USB link is in L2, repeater is monitoring for a resume/remote wake event. T <sub>A</sub> = 25°C, (DP/DN Voltage ≤ VDD3V3). In peripheral mode additional current is present due the DP pull up.		45	85	μW

## 6.5 Electrical Characteristics (続き)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_{Sleep}$	L1 Sleep	I2C/GPIO interfaces idle, repeater is supporting a USB connection, USB link is in L1 (host exists L1 every 1 ms) and repeater is monitoring for a L1 exit event. $T_A = 25^\circ\text{C}$ , (DP/DN Voltage $\leq$ VDD3V3)		2.3	5	mW
$P_{LS\_Active}$	Low Speed Active	I2C/GPIO interfaces idle, repeater in LS mode, maximum transition density. $T_A = 85^\circ\text{C}$ .		7.2	24	mW
$P_{FS1\_Active}$	Full Speed Active (ASYNC Traffic)	I2C/GPIO interfaces idle, repeater in FS mode, maximum transition density. $T_A = 85^\circ\text{C}$ .		45	80	mW
$P_{FS2\_Active}$	Full Speed Active (ISO Traffic)	I2C/GPIO interfaces idle, repeater in FS mode, maximum transition density. $T_A = 85^\circ\text{C}$ .		9	24	mW
$P_{HS\_Idle\_Host}$	High Speed Idle (Host mode)	L0.Idle. $T_A = 85^\circ\text{C}$ . (Typical at $25^\circ\text{C}$ ).		26	70	mW
$P_{HS\_Idle\_Peripheral}$	High Speed Idle (Peripheral mode)	L0.Idle. $T_A = 85^\circ\text{C}$ . (Typical at $25^\circ\text{C}$ ).		108	200	mW
<b>DIGITAL INPUTS</b>						
$V_{IH}$	High level input voltage	GPIO0, GPIO1, GPIO2 (1.2 V Variant)	0.702			V
$V_{IH}$	High level input voltage	GPIO0, GPIO1, GPIO2 (1.8 V Variant)	1.053			V
$V_{IL}$	Low-level input voltage	GPIO0, GPIO1, GPIO2 (1.2 V Variant)			0.462	V
$V_{IL}$	Low-level input voltage	GPIO0, GPIO1, GPIO2 (1.8 V Variant)			0.693	V
$V_{IL}$	Low-level input voltage	RESETB			0.35	V
$V_{IH}$	High level input voltage	RESETB	0.75			V
$I_{IH}$	High level input current	$V_{IH} = 1.98\text{ V}$ , VDD3V3=3.0 V or 0 V, VDD1V8=1.62 V or 0 V RESETB, GPIO0, GPIO1			0.5	$\mu\text{A}$
$I_{IL}$	Low level input current	$V_{IL} = 0\text{ V}$ , VDD3V3=3.0 V or 0 V, VDD1V8=1.62 V or 0 V RESETB, GPIO0, GPIO1			0.5	$\mu\text{A}$
<b>DIGITAL OUTPUTS</b>						
$V_{OH}$	High level output voltage	GPIO0, GPIO1, GPIO2, push-pull I/O mode ( $I_{OH} = 20\ \mu\text{A}$ and maximum 3 pF $C_{load}$ ) (1.2 V Variant)	0.81			V
$V_{OH}$	High level output voltage	GPIO0, GPIO1, GPIO2, push-pull I/O mode ( $I_{OH} = 20\ \mu\text{A}$ and maximum 3 pF $C_{load}$ ) (1.8 V Variant)	1.21			V
$V_{OL}$	Low level output voltage	GPIO0, GPIO1, GPIO2, push-pull I/O mode ( $I_{OL} = 1\ \text{mA}$ ) (1.2 V Variant)			0.25	V
$V_{OL}$	Low level output voltage	GPIO0, GPIO1, GPIO2, push-pull I/O mode ( $I_{OL} = 1\ \text{mA}$ ) (1.8 V Variant)			0.35	V
$I_{OL\_PP}$	Low level output current in push-pull mode	GPIO0, GPIO1, GPIO2 (1.2 V Variant), $V_{OL}=0.4\ \text{V}$	2.5	4	5.6	mA
$I_{OL\_PP}$	Low level output current in push-pull mode	GPIO0, GPIO1, GPIO2 (1.8 V Variant), $V_{OL}=0.4\ \text{V}$	4	6	8	mA
$I_{OH\_PP}$	High level output current in push-pull mode	GPIO0, GPIO1, GPIO2, push-pull I/O mode, $V_{OH}=0.9\ \text{V}$ (1.2 V Variant)	22			$\mu\text{A}$
$I_{OH\_PP}$	High level output current in push-pull mode	GPIO0, GPIO1, GPIO2, push-pull I/O mode, $V_{OH}=0.9\ \text{V}$ (1.8 V Variant)	50			$\mu\text{A}$
<b>I2C (SDA, SCL)</b>						
$V_{IL}$	Low level input voltage, 1.2 V variant	SDA, SCL, $V_{I2C\_Pullup} = 1.08\ \text{V}$			0.387	V

## 6.5 Electrical Characteristics (続き)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>IL</sub>	Low level input voltage, 1.8 V variant	SDA, SCL, V <sub>I2C_Pullup</sub> = 1.96 V			0.588	V
V <sub>IH</sub>	High level input voltage, 1.2 V variant	SDA, SCL, V <sub>I2C_Pullup</sub> = 1.08 V	0.833			V
V <sub>IH</sub>	High level input voltage, 1.8 V variant	SDA, SCL, V <sub>I2C_Pullup</sub> = 1.96 V	1.372			V
V <sub>HYS</sub>	Input hysteresis, 1.2 V variant	V <sub>I2C_Pullup</sub> = 1.08 V	0.020			V
V <sub>HYS</sub>	Input hysteresis, 1.8 V variant	V <sub>I2C_Pullup</sub> = 1.96 V	0.098			V
I <sub>IH</sub>	High level input leakage current	V <sub>IH</sub> = 1.98 V			0.5	μA
I <sub>IL</sub>	Low level input leakage current	V <sub>IL</sub> = 0 V			0.5	μA
V <sub>OL</sub>	Low level output voltage (1 kΩ pull up), 1.2 V variant	I <sub>OL</sub> = 2.5 mA, V <sub>I2C_Pullup</sub> = 1.08 V			0.2	V
V <sub>OL</sub>	Low level output voltage (1 kΩ pull up), 1.8V variant	I <sub>OL</sub> = 2.5 mA, V <sub>I2C_Pullup</sub> = 1.96 V			0.3	V
I <sub>OL</sub>	Open drain drive strength, 1.2 V Variant	V <sub>OL</sub> = 0.4 V	1.6	2.4	3.0	mA
I <sub>OL</sub>	Open drain drive strength, 1.8 V Variant	V <sub>OL</sub> = 0.4 V	8	10	12.6	mA
<b>UART I/O</b>						
V <sub>OLI</sub>	Internal output low	Internal UART output (eDP/eDN) 1.2 V signaling			0.1	V
V <sub>OHI</sub>	Internal output high	Internal UART output (eDP/eDN) 1.2 V signaling	0.918		1.32	V
V <sub>ILI</sub>	Internal input low	Internal UART input (eDP/eDN) 1.2 V signaling	-0.1		0.399	V
V <sub>IHI</sub>	Internal input high	Internal UART input (eDP/eDN) 1.2 V signaling	0.819		1.386	V
V <sub>OLE</sub>	External output low	External UART output (DP/DN) 3.3 V signaling	0		0.3	V
V <sub>OHE</sub>	External output high	External UART output (DP/DN) 3.3 V signaling	2.8		3.6	V
V <sub>ILE</sub>	External input low	External UART input (DP/DN) 3.3 V signaling			0.8	V
V <sub>IHE</sub>	External input high	External UART input (DP/DN) 3.3 V signaling	2			V
<b>USB (DP, DN)</b>						
Z <sub>inp_Dx</sub>	Impedance to GND, no pull up or pull down	V <sub>in</sub> =3.6 V, V <sub>DD3V3</sub> =3.0 V, <i>Input Characteristics</i> <sup>(1)</sup>	390			kΩ
C <sub>IO_Dx</sub>	Capacitance to GND	Measured with VNA at 240 MHz, Driver Hi-Z			10	pF
R <sub>PUI</sub>	Bus pull-up resistor on upstream facing port (idle)	<i>High-speed Device Speed Identification</i> <sup>(1)</sup>	0.92	1.1	1.475	kΩ
R <sub>PUR</sub>	Bus pull-up resistor on upstream facing port (receiving)	<i>High-speed Device Speed Identification</i> <sup>(1)</sup>	1.525	2.2	2.99	kΩ
R <sub>PD</sub>	Bus pull-down resistor on downstream facing port	<i>High-speed Device Speed Identification</i> <sup>(1)</sup>	14.35	19	24.6	kΩ
V <sub>HSTERM</sub>	Termination voltage in high speed	The output voltage in the high-speed idle state, <i>High-speed Input Characteristics</i> <sup>(1)</sup>	-10		10	mV
<b>USB TERMINATION</b>						
Z <sub>HSTERM_P</sub>	Driver Output Resistance (which also serves as high speed termination)	(V <sub>OH</sub> = 0 to 600 mV) <i>Full-speed (12 Mb/s) Driver Characteristics</i> <sup>(1)</sup> , Default, U_HS_TERM_Px setting 01	40.6	45	49.4	Ω

## 6.5 Electrical Characteristics (続き)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z <sub>HSTERM_N</sub>	Driver Output Resistance (which also serves as high speed termination)	(VOH= 0 to 600 mV) <i>Full-speed</i> (12 Mb/s) <i>Driver Characteristics</i> <sup>(1)</sup> , Default, U_HS_TERM_Px setting 01	40.6	45	49.4	Ω
<b>USB INPUT LEVELS LS/FS</b>						
V <sub>IH</sub>	High (driven)	<i>Receiver Characteristics</i> <sup>(1)</sup> (measured at the connector)	2			V
V <sub>IHZ</sub>	High (floating)	<i>Receiver Characteristics</i> <sup>(1)</sup> (HOST downstream port pull-down resistor enabled and external device pull up 1.5 kΩ ± 5% to 3.0-3.6 V)	2.7		3.6	V
V <sub>IL</sub>	Low	<i>Receiver Characteristics</i> <sup>(1)</sup>			0.8	V
V <sub>DI</sub>	Differential Input Sensitivity (hysteresis is off)	[(D+)-(D-)] ; Differential Input Sensitivity Range for Low-/full-speed <sup>(1)</sup> ; (measured at connector) V <sub>CM</sub> =0.8 V to 2.0 V			0.2	V
<b>USB OUTPUT LEVELS LS/FS</b>						
V <sub>OL</sub>	Low	<i>USB Driver Characteristics</i> <sup>(1)</sup> , (measured at connector with RL of 1.425 kΩ to 3.6 V.)	0		0.3	V
V <sub>OH</sub>	High (Driven)	<i>USB Driver Characteristics</i> <sup>(1)</sup> , (measured at the connector with RL of 14.25 kΩ to GND.)	2.8		3.6	V
Z <sub>FSTERM</sub>	Driver Series Output Resistance	<i>USB Driver Characteristics</i> <sup>(1)</sup> , measured it during VOL or VOH	28		44	Ω
V <sub>CRS2</sub>	Output Signal Crossover Voltage	Measured as in <i>Data Signal Rise and Fall Time</i> <sup>(1)</sup> , excluding the first transition from the Idle state. With external 1.5 kΩ pull up on DP to 3.0 V	1.3		2	V
V <sub>CRS</sub>	Output Signal Crossover Voltage	Measured as in <i>Data Signal Rise and Fall Time</i> <sup>(1)</sup> , excluding the first transition from the Idle state	1.3		2	V
<b>USB INPUT LEVELS HS</b>						
V <sub>HSSQ</sub>	High-speed squelch/no-squelch detection threshold	<i>Full-/High-speed Signaling Level</i> <sup>(1)</sup> , specification refers to peak differential signal amplitude), measured at 240 MHz with increasing amplitude, U_SQUELCH_THRESHOLD_Px setting 011, V <sub>CM</sub> = -50 mV to 500 mV	111	128	161	mV
V <sub>HSSQ</sub>	High-speed squelch/no-squelch detection threshold	<i>Full-/High-speed Signaling Levels</i> <sup>(1)</sup> , (specification refers to peak differential signal amplitude), measured at 240 MHz with increasing amplitude, U_SQUELCH_THRESHOLD_Px setting 100, V <sub>CM</sub> = -50 mV to 500 mV	104	125	150	mV
V <sub>HSDSC</sub>	High-speed disconnect detection threshold	<i>Full-/High-speed Signaling Levels</i> <sup>(1)</sup> , (specification refers to differential signal amplitude). (HW Default), U_DISCONNECT_THRESHOLD_Px setting 0000, V <sub>CM</sub> =200 mV to 600 mV	525	575	625	mV
V <sub>HSDSC</sub>	High-speed disconnect detection threshold	<i>Full-/High-speed Signaling Levels</i> <sup>(1)</sup> (specification refers to differential signal amplitude). (+25.6%), U_DISCONNECT_THRESHOLD_Px setting 1000, V <sub>CM</sub> =280 mV to 680 mV	685	757	846	mV

## 6.5 Electrical Characteristics (続き)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EQ_UHS	USB high-speed data receiver equalization, (measured indirectly through jitter)	240 MHz, U_EQ_Px setting 000	-0.37	0.06	0.57	dB
EQ_UHS	USB High-speed data receiver equalization, (measured indirectly through jitter)	240 MHz, U_EQ_Px setting 010	0.62	1.09	1.57	dB
<b>USB OUTPUT LEVELS HS</b>						
V_HSOH	High-speed data signaling high	Full-/High-speed Signaling Levels <sup>(1)</sup> , measured single-ended peak voltage per USB 2.0 test measurement spec, U_HS_TX_AMPLITUDE_Px setting 0011, PE disabled, Test load is an ideal 45 Ω to GND on DP and DN	360	400	440	mV
V_HSOH	High-speed data signaling high	Full-/High-speed Signaling Levels <sup>(1)</sup> , measured single ended peak voltage per USB 2.0 test measurement spec, U_HS_TX_AMPLITUDE_Px setting 1100, PE disabled, Test load is an ideal 45 Ω to GND on DP and DN	441	490	539	mV
V_HSOD	High-speed data signaling swing	Measured p-p, 0%, U_HS_TX_AMPLITUDE_Px setting 0011, PE disabled, Test load is an ideal 45 Ω to GND on DP and DN.	720	800	880	mV
V_HSOD	High-speed data signaling swing	Measured p-p, 22.5%, U_HS_TX_AMPLITUDE_Px setting 1100, PE disabled, Test load is an ideal 45 Ω to GND on DP and DN.	882	980	1078	mV
V_HSQL	High-speed data signaling low, driver is off termination is on (measured single ended)	Full-/High-speed Signaling Levels <sup>(1)</sup> , PE disabled, test load is an ideal 45 Ω to GND on DP and DN.	-10		10	mV
V_CHIRPJ	Host or hub chirp J level (differential voltage)	Full-/High-speed Signaling Levels <sup>(1)</sup> , (PE is disabled. swing setting has no impact but slew rate control has impact), Test load is an ideal 1.5 kΩ pull up on DP.	700	900	1100	mV
V_CHIRPK	Device chirp K level (differential voltage)	Full-/High-speed Signaling Levels <sup>(1)</sup> , (PE is disabled. swing setting has no impact but slew rate control has impact), Test load is an ideal 45 Ω to GND on DP and DN.	-900	-760	-500	mV
V_CHIRPK	Host or hub Chirp K level (differential voltage)	Full-/High-speed Signaling Levels <sup>(1)</sup> , (PE is disabled. swing setting has no impact but slew rate control has impact), Test load is an ideal 1.5 kΩ pull up on DP.	-900	-700	-500	mV
U2_TXPE	High-speed TX pre-emphasis	U_HS_TX_PRE_EMPHASIS_Px setting 000, test load is an ideal 45 Ω to GND on DP and DN.	0.25	0.5	0.75	dB
U2_TXPE	High-speed TX pre-emphasis	U_HS_TX_PRE_EMPHASIS_Px setting 100, test load is an ideal 45 Ω to GND on DP and DN.	1.7	2.1	2.5	dB
U2_TXPE_UI	High-speed TX pre-emphasis width	U_HS_TX_PE_WIDTH_Px setting 11 (measured with PE=2.5 dB setting of 101), Test load is an ideal 45 Ω to GND on DP and DN.	0.54	0.65	0.77	UI
<b>eUSB2 TERMINATION</b>						
R_SRC_HS	High-speed transmit source termination impedance	High-Speed Tx Electrical Specification <sup>(2)</sup>	33	40	47	Ω

## 6.5 Electrical Characteristics (続き)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta R_{SRC\_HS}$	High-speed source impedance mismatch	High-Speed Tx Electrical Specification <sup>(2)</sup>			4	$\Omega$
$R_{RCV\_DIF}$	High-speed differential receiver termination (repeater)	High-Speed Rx Electrical Specification <sup>(2)</sup>	74	80	86	$\Omega$
$R_{PD}$	Pull-down resistors on eDP/eDN	Pull-down <sup>(2)</sup> , active during LS, FS and HS	6	8	10	k $\Omega$
$R_{SRC\_LSFS}$	Transmit output impedance	Low-Speed /Full-Speed DC Specifications for 1.2 V $\pm$ 10% <sup>(2)</sup> , TX output impedance	28	44	59	$\Omega$
$C_{IO\_eDx}$	Differential Capacitance	Measured with VNA at 240 MHz, Driver Hi-Z (VCM = 120 mV to 450 mV), measured differentially.		3.9	5.2	pF
<b>eUSB2 FS/LS INPUT LEVELS</b>						
$V_{IL}$	Single-ended input low	Low-Speed /Full-Speed DC Specifications for 1.2 V $\pm$ 10% <sup>(2)</sup>	-0.1		0.399	V
$V_{IL}$	Single-ended input low	Low-Speed /Full-Speed DC Specifications for 1.0 V $\pm$ 10% <sup>(2)</sup>	-0.1		0.332	V
$V_{IH}$	Single-ended input high	Low-Speed /Full-Speed DC Specifications for 1.2 V $\pm$ 10% <sup>(2)</sup>	0.819		1.386	V
$V_{IH}$	Single-ended input high	Low-Speed /Full-Speed DC Specifications for 1.0 V $\pm$ 10% <sup>(2)</sup>	0.682		1.1	V
$V_{HYS}$	Receive single-ended hysteresis voltage	Low-Speed /Full-Speed DC Specifications for 1.2 V $\pm$ 10% <sup>(2)</sup>	43.2			mV
$V_{HYS}$	Receive single-ended hysteresis voltage	Low-Speed /Full-Speed DC Specifications for 1.0 V $\pm$ 10% <sup>(2)</sup>	38			mV
<b>eUSB2 FS/LS OUTPUT LEVELS</b>						
$V_{OL}$	Single-ended output low	Low-Speed /Full-Speed DC Specifications for 1.2 V $\pm$ 10% <sup>(2)</sup>			0.1	V
$V_{OL}$	Single-ended output low	Low-Speed /Full-Speed DC Specifications for 1.0 V $\pm$ 10% <sup>(2)</sup>			0.1	V
$V_{OH}$	Single-ended output high	Low-Speed /Full-Speed DC Specifications for 1.2 V $\pm$ 10% <sup>(2)</sup>	0.918		1.32	V
$V_{OH}$	Single-ended output high	Low-Speed /Full-Speed DC Specifications for 1.0 V $\pm$ 10% <sup>(2)</sup>	0.765		1.1	V
<b>eUSB2 HS INPUT LEVELS</b>						
$V_{RX\_CM}$	Receive DC common mode range (low)	High-Speed Rx Electrical Specification <sup>(2)</sup> (normative), low DC common mode RX must tolerate			120	mV
$V_{RX\_CM}$	Receive DC common mode range (high)	High-Speed Rx Electrical Specification <sup>(2)</sup> (normative), high DC common mode RX must tolerate	280			mV
$V_{CM\_RX\_AC}$	Receiver AC common mode (50 MHz–480 MHz)	High-Speed Rx Electrical Specification <sup>(2)</sup> (informative), across the DC common-mode range of 120 mV to 280 mV. (RX capability tested with intentional TX rise/fall time mismatch and prop delay mismatch)	-60		60	mV
$C_{RX\_CM}$	Receive center-tapped capacitance	High-Speed Rx Electrical Specification <sup>(2)</sup> (informative)	15		50	pF



## 6.5 Electrical Characteristics (続き)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>EHSSQ</sub>	Squelch/No-squelch detect threshold	<i>High-Speed Rx Electrical Specification</i> <sup>(2)</sup> , (measured as differential peak voltage at 240 MHz with increasing amplitude) E_SQUELCH_THRESHOLD_Px setting 100, V <sub>CM</sub> = 120 mV to 450 mV	60	81	97	mV
V <sub>EHSSQ</sub>	Squelch/No-squelch detect threshold	<i>High-Speed Rx Electrical Specification</i> <sup>(2)</sup> , (measured as differential peak voltage at 240 MHz with increasing amplitude) E_SQUELCH_THRESHOLD_Px setting 110, V <sub>CM</sub> = 120 mV to 450 mV	47	67	83	mV
EQ <sub>EHS</sub>	eUSB2 high-speed data receiver equalization, (measured indirectly through jitter)	240 MHz E_EQ_P1x setting 0000	-0.2	0.34	0.73	dB
<b>eUSB2 HS OUTPUT LEVELS</b>						
V <sub>EHSOD</sub>	Transmit differential (terminated)	Measured p2p, R <sub>L</sub> = 80 Ω, E_HS_TX_AMPLITUDE_Px setting 011, ideal 80 Ω Rx differential termination load	378	420	462	mV
E <sub>TXPE</sub>	High-speed TX Pre-emphasis	E_HS_TX_PRE_EMPHASIS_Px setting 000	-0.2	0	0.2	dB
E <sub>TXPE_UI</sub>	High-speed TX Pre-emphasis width	E_HS_TX_PE_WIDTH_Px setting 00	0.29	0.40	0.59	UI
V <sub>E_TX_CM</sub>	Transmit DC common mode	<i>High-Speed Tx Electrical Specification</i> <sup>(2)</sup>	170		230	mV

- (1) USB 2.0 Promoter Group 2000, USB 2.0 Specification USB 2.0 Promoter Group  
 (2) USB Implementers Forum (2018). Embedded USB2 (eUSB2) Physical Layer Supplement to the USB Revision 2.0 Specification, Rev. 1.2 USB Implementers Forum

## 6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>USB (DP, DN), HS Driver Switching Characteristics</b>						
T <sub>HSR</sub>	Rise time (10% – 90%)	Data Signal Rise and Fall, Eye Patterns <sup>(1)</sup> , U_HS_TX_SLEW_RATE_Px setting 11, ideal 45 Ω to GND loads on DP and DN, pre-emphasis disabled.	530	625	740	ps
T <sub>HSF</sub>	Fall time (10% – 90%)	Data Signal Rise and Fall, Eye Patterns, U_HS_TX_SLEW_RATE_Px setting 11, ideal 45 Ω to GND loads on DP and DN, pre-emphasis disabled.	530	625	740	ps
<b>USB (DP, DN), FS Driver Switching Characteristics</b>						
T <sub>FR</sub>	Rise time (10% – 90%)	Data Signal Rise and Fall Time and Full-speed Load <sup>(1)</sup>	4		20	ns
T <sub>FF</sub>	Fall time (10% – 90%)	Data Signal Rise and Fall Time and Full-speed Load <sup>(1)</sup>	4		20	ns
T <sub>FRFM</sub>	(T <sub>FR</sub> /T <sub>FM</sub> )	Data Signal Rise and Fall, Eye Patterns <sup>(1)</sup> , excluding the first transition from the Idle state	90		111.1	%
<b>USB (DP, DN), LS Driver Switching Characteristics</b>						
T <sub>LR</sub>	Rise time (10% – 90%)	Data Signal Rise and Fall Time and Full-speed Load <sup>(1)</sup>	75		300	ns
T <sub>LF</sub>	Fall time (10% – 90%)	Data Signal Rise and Fall Time and Full-speed Load <sup>(1)</sup>	75		300	ns
<b>eUSB2 (eDP, eDN), HS Driver Switching Characteristics</b>						
T <sub>EHSRF</sub>	Rise/fall time (20% – 80%)	Full-Speed/Low-Speed Electrical Specification <sup>(2)</sup> , ideal 80 Ω Rx differential termination E_HS_TX_SLEW_RATE_Px setting = 01	355	440	525	ps
T <sub>EHSRF_M</sub> M	Transmit rise/fall mismatch	Full-Speed/Low-Speed Electrical Specification <sup>(2)</sup> , rise/fall mismatch = absolute delta of (rise – fall time) / (average of rise and fall time).			25	%
<b>eUSB2 (eDP, eDN), LS/FS Driver Switching Characteristics</b>						
T <sub>ERF</sub>	Rise/fall time (10% – 90%)	Low-Speed /Full-Speed DC Specifications for 1.2 V ± 10% <sup>(2)</sup>	2		6	ns
T <sub>ERF_MM</sub>	Transmit rise/fall mismatch	Low-Speed /Full-Speed DC Specifications for 1.2 V ± 10% <sup>(2)</sup>			25	%
<b>I2C (SDA)</b>						
T <sub>r</sub>	Rise time (STD)	Bus Speed = 100 kHz, C <sub>L</sub> = 200 pF, R <sub>PU</sub> = 4 kΩ, I <sub>OL</sub> ≅ 1 mA	600			ns
T <sub>r</sub>	Rise time (FM)	Bus Speed = 400 kHz, C <sub>L</sub> = 200 pF, R <sub>PU</sub> = 2.2 kΩ, I <sub>OL</sub> ≅ 2 mA	180			ns
T <sub>r</sub>	Rise time (FM+)	Bus Speed = 1 MHz, C <sub>L</sub> = 10 pF, R <sub>PU</sub> = 1 kΩ, I <sub>OL</sub> ≅ 4 mA	72			ns
T <sub>r</sub>	Rise time (STD)	Bus Speed = 100 kHz, C <sub>L</sub> = 200 pF, R <sub>PU</sub> = 4 kΩ, I <sub>OL</sub> ≅ 2 mA			1000	ns
T <sub>r</sub>	Rise time (FM)	Bus Speed = 400 kHz, C <sub>L</sub> = 200 pF, R <sub>PU</sub> = 1 kΩ, I <sub>OL</sub> ≅ 8 mA			300	ns
T <sub>r</sub>	Rise time (FM+)	Bus Speed = 1 MHz, C <sub>L</sub> = 50 pF, R <sub>PU</sub> = 1 kΩ, I <sub>OL</sub> ≅ 4 mA			120	ns
T <sub>f</sub>	Fall time (STD)	Bus Speed = 100 kHz, C <sub>L</sub> = 200 pF, R <sub>PU</sub> = 2.2 kΩ, I <sub>OL</sub> ≅ 4 mA			106.5	ns

## 6.6 Switching Characteristics (続き)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_f$	Fall time (FM)	Bus Speed = 400 kHz, $C_L = 200$ pF, $R_{PU} = 1$ k $\Omega$ , $I_{OL} \cong 8$ mA			106.5	ns
$T_f$	Fall time (FM+)	Bus Speed = 1 MHz, $C_L = 90$ pF, $R_{PU} = 1$ k $\Omega$ , $I_{OL} \cong 8$ mA			81.5	ns
$T_f$	Fall time (STD)	Bus Speed = 100 kHz, $C_L = 10$ pF, $R_{PU} = 4$ k $\Omega$ , $I_{OL} \cong 2$ mA	6.5			ns
$T_f$	Fall time (FM)	Bus Speed = 400 kHz, $C_L = 10$ pF, $R_{PU} = 2.2$ k $\Omega$ , $I_{OL} \cong 4$ mA	6.5			ns
$T_f$	Fall time (FM+)	Bus Speed = 1 MHz, $C_L = 10$ pF, $R_{PU} = 1$ k $\Omega$ , $I_{OL} \cong 8$ mA	6.5			ns

- (1) USB 2.0 Promoter Group 2000, USB 2.0 Specification USB 2.0 Promoter Group
- (2) USB Implementers Forum (2018). Embedded USB2 (eUSB2) Physical Layer Supplement to the USB Revision 2.0 Specification, Rev. 1.2 USB Implementers Forum

## 6.7 Timing Requirements

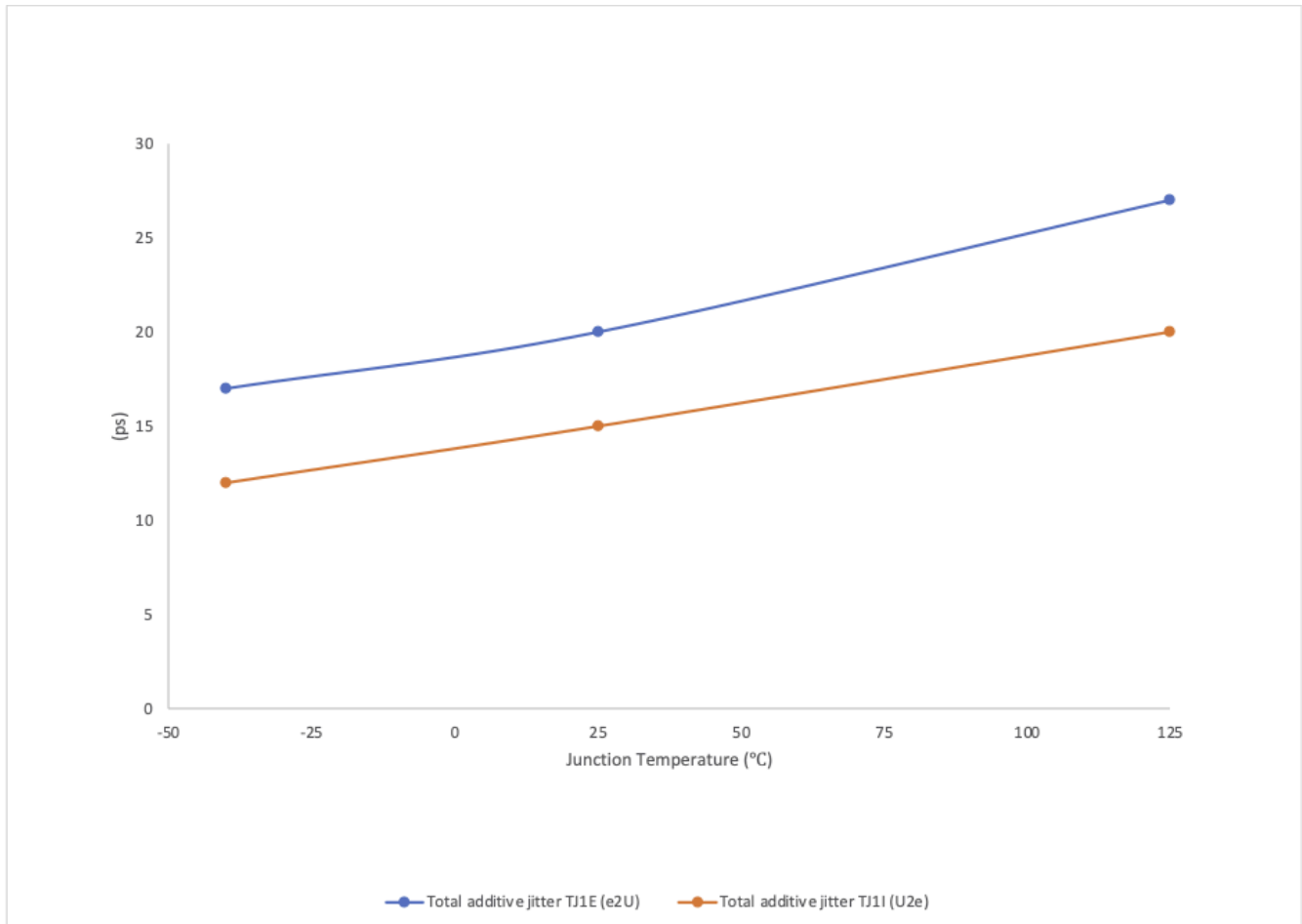
		MIN	NOM	MAX	UNIT
<b>I/O TIMING</b>					
t_GPIO_PW	Minimum GPIO pulse width for interrupt event	8			µs
<b>RESET TIMING</b>					
t_VDD1V8_RAMP	Ramp time for VDD1V8 to reach minimum 1.62 V			2	ms
t_VDD3V3_RAMP	Ramp time for VDD3V3 to reach minimum 3.0 V			2	ms
t_aRESETB	Duration for RESETB to be asserted low to complete reset while powered	10			us
t_RH_READY	Time for the device to be ready to accept RAP and I <sup>2</sup> C requests and eUSB2 interface to be ready after RESETB is de-asserted or (VDD1V8 and VDD3V3) reach the minimum recommended voltages, whichever is later.			3	ms
t_RS_READY	Time for the device to be ready to accept RAP and I <sup>2</sup> C requests and eUSB2 interface to be ready after a soft reset through I <sup>2</sup> C.			350	µs
<b>REPEATER TIMING</b>					
T <sub>J1E</sub>	Total additive jitter for eUSB2 to USB 2.0 (output jitter – input jitter) of the repeater.		20	42	ps
T <sub>J1I</sub>	Total additive jitter for USB 2.0 to eUSB2 (output jitter – input jitter) of the repeater.		17	42	ps
T <sub>e_to_U_DJ1</sub>	eUSB2 to USB 2.0 repeater FS jitter to next transition (Per <i>Low-Speed /Full-Speed DC Specifications for 1.2 V ± 10%</i> <sup>(1)</sup> condition for supply and GND delta).	-6.0		+6.0	ns
T <sub>U_to_e_DJ1</sub>	USB 2.0 to eUSB2 repeater FS jitter to next transition (Per <i>Low-Speed /Full-Speed DC Specifications for 1.2 V ± 10%</i> <sup>(1)</sup> condition for supply and GND delta).	-3.0		+3.0	ns
T <sub>DJ2_e2U</sub>	repeater FS paired transition jitter in eUSB2 to USB 2.0 direction (relaxed relative to THDJ2 defined by USB 2.0 ± 1 ns). eUSB2 in 1.2 V signaling mode.	-1.5		+1.5	ns
T <sub>DJ2_U2e</sub>	repeater FS paired transition jitter in USB 2.0 to eUSB2 direction (relaxed relative to THDJ2 defined by USB 2.0 ± 1 ns). eUSB2 in 1.2 V signaling mode.	-1.5		+1.5	ns
<b>MODE TIMING</b>					
T <sub>MODE_SWITCH</sub>	Time needed to change mode from UART bypass mode to and from USB mode			1	µs
T <sub>UART_START</sub>	Time needed to start transmitting UART data, post toggling GPIO0 to '0' when in UART strap mode (SCL=1, SDA=0 at power-up)			2	ms
<b>I2C (FM+)</b>					
t <sub>SU_STA</sub>	Start setup time, SCL (T <sub>r</sub> =72 ns – 120 ns), SDA (T <sub>r</sub> =6.5 ns – 81.5 ns), 1 MHz FM+	260			ns
t <sub>SU_STO</sub>	Stop setup time, SCL (T <sub>r</sub> =72 ns – 120 ns), SDA (T <sub>r</sub> =6.5 ns – 81.5 ns), 1 MHz FM+	260			ns
t <sub>HD_STA</sub>	Start hold time, SCL (T <sub>r</sub> =72 ns – 120 ns), SDA (T <sub>r</sub> =6.5 ns – 81.5 ns), 1 MHz FM+	260			ns
t <sub>SU_DAT</sub>	Data input or false start/stop, setup time, SCL (T <sub>r</sub> =72 ns – 120 ns), SDA (T <sub>r</sub> =6.5 ns – 81.5 ns), 1 MHz FM+	50			ns
t <sub>HD_DAT</sub>	Data input or False start/stop, hold time, SCL (T <sub>r</sub> =72 ns – 120 ns), SDA (T <sub>r</sub> =6.5 ns – 81.5 ns), 1 MHz FM+	0			ns
t <sub>VD_DAT</sub> , t <sub>VD_ACK</sub>	SDA output delay, SCL (T <sub>r</sub> =72 ns – 120 ns), SDA (T <sub>r</sub> =6.5 ns – 81.5 ns), 1 MHz FM+	20		450	ns
t <sub>HD_DAT_SL</sub>	Data hold time when device is transmitting	6.67			ns
t <sub>SP</sub>	Glitch width suppressed	50		91	ns
t <sub>BUF</sub>	Bus free time between a STOP and START condition (Master minimum spec that device must tolerate)	0.5			µs

## 6.7 Timing Requirements (続き)

		MIN	NOM	MAX	UNIT
t <sub>LOW</sub>	Low period for SCL clock (minimum spec that device must tolerate)	0.5			μs
t <sub>HIGH</sub>	High period for SCL clock (minimum spec that device must tolerate)	0.26			μs
<b>I2C (FM)</b>					
t <sub>SU_STO</sub>	Stop setup time, SCL (T <sub>r</sub> =180 ns – 300 ns), SDA (T <sub>f</sub> =6.5 ns – 106.5 ns), 400 kHz FM	600			ns
t <sub>HD_STA</sub>	Start hold time, SCL (T <sub>r</sub> =180 ns – 300 ns), SDA (T <sub>f</sub> =6.5 ns – 106.5 ns), 400 kHz FM	600			ns
t <sub>SU_STA</sub>	Start setup time, SCL (T <sub>r</sub> =180 ns – 300 ns), SDA (T <sub>f</sub> =6.5 ns – 106.5 ns), 400 kHz FM	600			ns
t <sub>SU_DAT</sub>	Data input or false start/stop, setup time, SCL (T <sub>r</sub> =180 ns – 300 ns), SDA (T <sub>f</sub> =6.5 ns – 106.5 ns), 400 kHz FM	100			ns
t <sub>HD_DAT</sub>	Data input or false start/stop, hold time, SCL (T <sub>r</sub> =180 ns – 300 ns), SDA (T <sub>f</sub> =6.5 ns – 106.5 ns), 400 kHz FM	0			ns
t <sub>VD_DAT</sub> , t <sub>VD_ACK</sub>	SDA output delay, SCL (T <sub>r</sub> =180 ns – 300 ns), SDA (T <sub>f</sub> =6.5 ns – 106.5 ns), 400 kHz FM	20		900	ns
t <sub>HD_DAT_SL</sub>	Data hold time when device is transmitting	13.5			ns
t <sub>SP</sub>	Glitch width suppressed	50		91	ns
t <sub>BUF</sub>	Bus free time between a STOP and START condition (minimum spec that device must tolerate)	1.3			μs
t <sub>LOW</sub>	Low period for SCL clock (minimum spec that device must tolerate)	1.3			μs
t <sub>HIGH</sub>	High period for SCL clock (Master minimum spec that device must tolerate)	0.6			μs
<b>I2C (STD)</b>					
t <sub>SU_STO</sub>	Stop setup time, SCL (T <sub>r</sub> =600 ns – 1000 ns), SDA (T <sub>f</sub> =6.5 ns – 106.5 ns), 100 kHz STD	4			μs
t <sub>HD_STA</sub>	Start hold time, SCL (T <sub>r</sub> =600 ns – 1000 ns), SDA (T <sub>f</sub> =6.5 ns – 106.5 ns), 100 kHz STD	4			μs
t <sub>SU_STA</sub>	Start setup time, SCL (T <sub>r</sub> =600 ns – 1000 ns), SDA (T <sub>f</sub> =6.5 ns – 106.5 ns), 100 kHz STD	4.7			μs
t <sub>SU_DAT</sub>	Data input or false start/stop, setup time, SCL (T <sub>r</sub> =600 ns – 1000 ns), SDA (T <sub>f</sub> =6.5 ns – 106.5 ns), 100 kHz STD	250			ns
t <sub>HD_DAT</sub>	Data input or false start/stop, hold time, SCL (T <sub>r</sub> =600 ns – 1000 ns), SDA (T <sub>f</sub> =6.5 ns – 106.5 ns), 100 kHz STD	5			μs
t <sub>VD_DAT</sub> , t <sub>VD_ACK</sub>	SDA output delay, SCL (T <sub>r</sub> =600 ns – 1000 ns), SDA (T <sub>f</sub> =6.5 ns – 106.5 ns), 100 kHz STD			3.45	μs
t <sub>HD_DAT_SL</sub>	Data hold time when device is transmitting	13.5			ns
t <sub>SP</sub>	Glitch width suppressed	50		91	ns
t <sub>BUF</sub>	Bus free time between a STOP and START condition (minimum spec that device must tolerate)	4.7			μs
t <sub>LOW</sub>	Low period for SCL clock (minimum spec that device must tolerate)	4.7			μs
t <sub>HIGH</sub>	High period for SCL clock (minimum spec that device must tolerate)	4.0			μs

- (1) USB Implementers Forum (2018). Embedded USB2 (eUSB2) Physical Layer Supplement to the USB Revision 2.0 Specification, Rev. 1.2 USB Implementers Forum

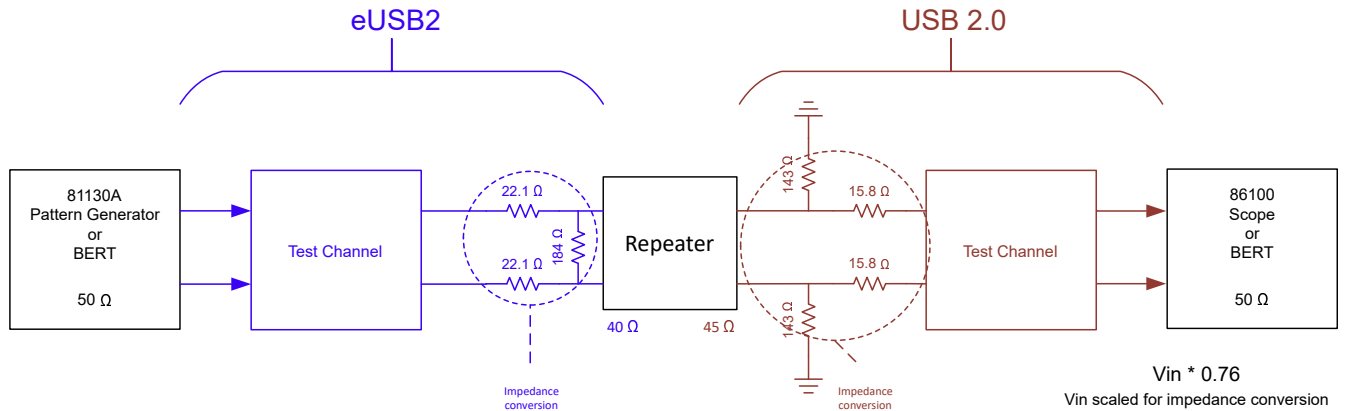
## 6.8 Typical Characteristics



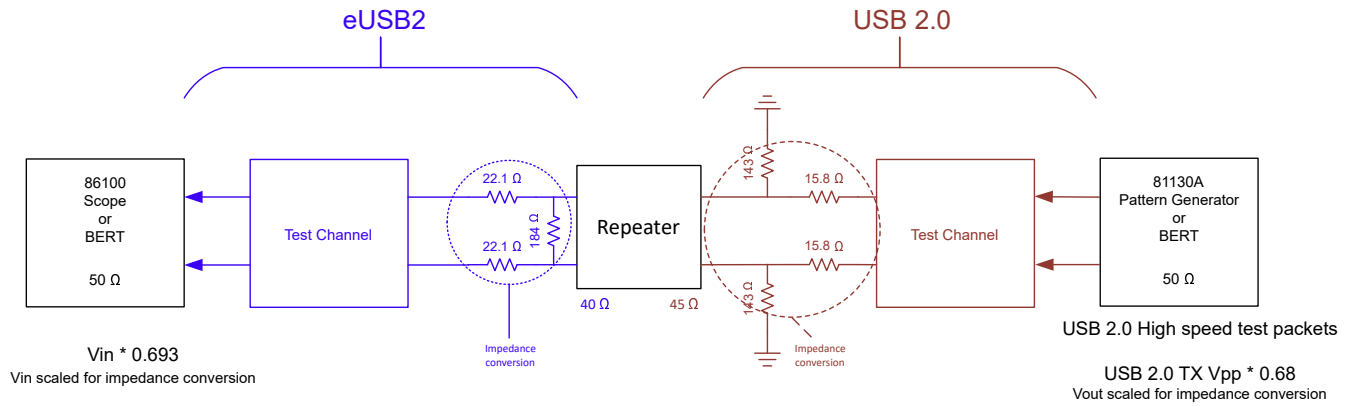
TJ1E is for egress direction from eUSB2 to USB and TJ1I is for ingress direction from USB to eUSB2

### 6-1. Total Additive Jitter (Typical)

## 7 Parameter Measurement Information



7-1. USB 2.0 TX Output (Egress) Jitter, Eye Mask Test Setup



7-2. eUSB2 TX Output (Ingress) Jitter, Eye Mask Test Setup

## 8 Detailed Description

### 8.1 Overview

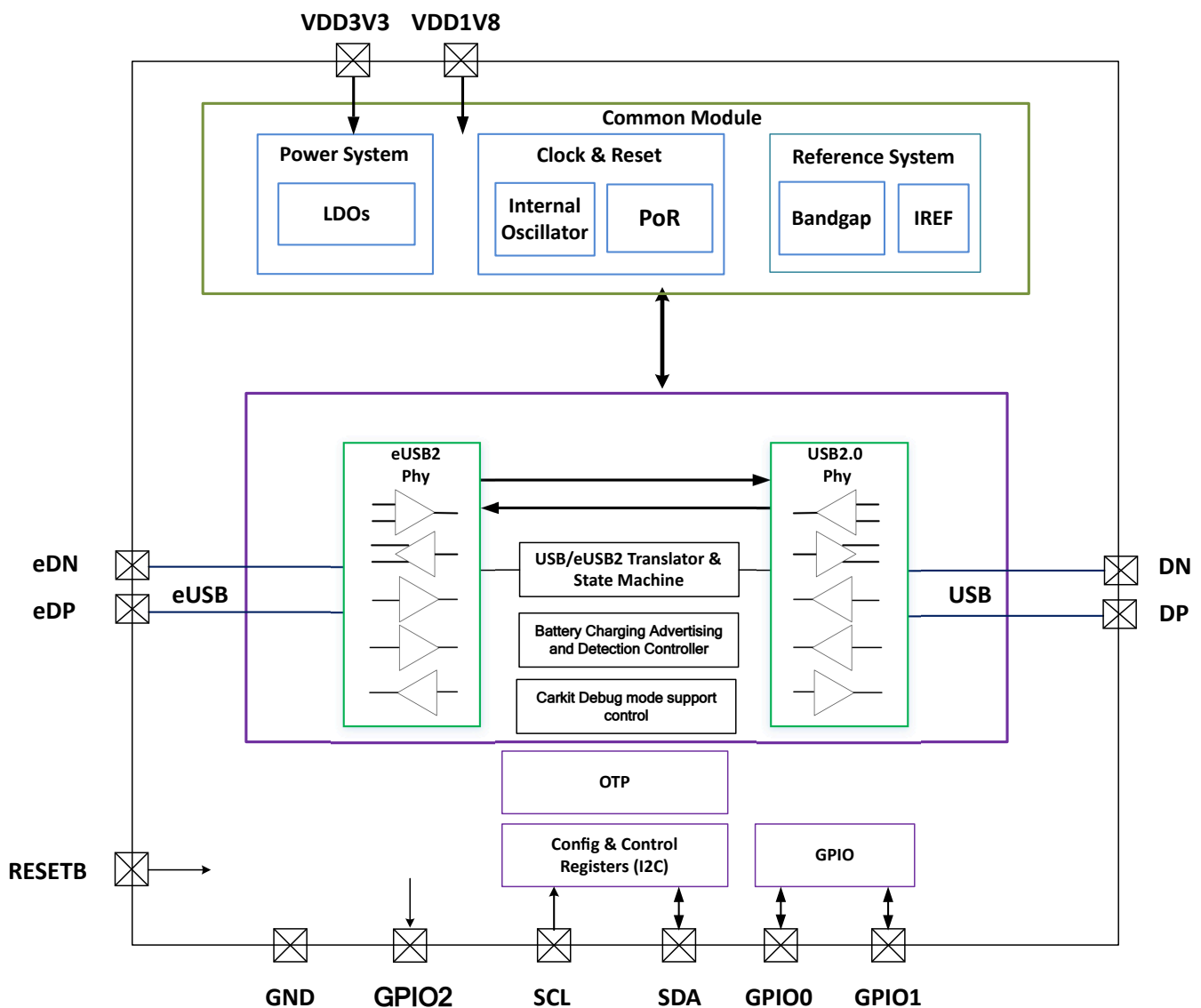
The TUSB2E11 is an eUSB2 to USB 2.0 repeater that resides between the SoC with an eUSB2 port and an external connector that supports USB 2.0. The device can be configured by the register access protocol (RAP) or through the I<sup>2</sup>C. The repeater is configurable as either a host or device repeater (DRD repeater).

I<sup>2</sup>C port supports up to 1MHz (fast mode plus) for internal register access. A subset of internal registers can be accessed through the register access protocol. Simultaneous register access using RAP and through the I<sup>2</sup>C is supported with RAP having priority over I<sup>2</sup>C.

To power up in I<sup>2</sup>C mode, make sure both SDA and SCL have pullup resistors to appropriate I<sup>2</sup>C bus voltage.

GPIO2 output pin can be configured to provide an active low open-drain or selectable active low or active high push-pull level sensitive interrupt output to the SoC.

### 8.2 Functional Block Diagram





### 8.3 Feature Description

The TUSB2E11 is an USB compliant eUSB2 to USB 2.0 repeater supporting both device and host modes. Both USB and eUSB2 offer fully tunable TX and RX through I<sup>2</sup>C. Additionally, USB TX and RX can be tuned when I<sup>2</sup>C is not used.

### 8.4 Device Functional Modes

#### 8.4.1 Repeater Mode

Upon de-assertion of RESETB or software reset and after t<sub>RH\_READY</sub> or t<sub>RS\_READY</sub>, the TUSB2E11 enables and enters the default state. In the default state, the TUSB2E11 is ready to accept eUSB2 packets, RAP, and I<sup>2</sup>C requests. The repeater will either be in host repeater mode or peripheral repeater mode depending on the receipt of either host mode enable or peripheral mode enable.

When the TUSB2E11 is repeating high-speed packets, either from eUSB2 to USB 2.0 or from USB 2.0 to eUSB2, up to 4UI (may include partial UI) of HS SOP can be truncated. This is the same as a standard USB 2.0 HUB operating in high speed mode which can truncate up to 4UI.

When the TUSB2E11 is repeating high-speed packets from eUSB2 to USB 2.0, up to 1.6UI of random dribble bits (may include partial UI) can be introduced after HS EOP. This is the less than a standard USB 2.0 HUB operating in high speed mode which can have up to 4UI of random dribble bits.

When the TUSB2E11 is repeating high-speed packets from USB 2.0 to eUSB2, up to 5UI of random dribble bits (may include partial UI) can be introduced after HS EOP. This is more than a standard USB 2.0 HUB operating in high speed mode which can have up to 4UI of random dribble bits. eDSPr/eUSPr receiving eUSB2 high-speed packets should ignore 5UI of dribble bits after detecting no stuffed bit insertion indicating HS EOP.

**表 8-1. Number of Hubs Supported with Host and Peripheral Repeater**

Number of eUSB2 Repeaters	Number of Hubs Operating at HS	Number of Hubs Operating at FS	
1	4	2	Number of hubs operating at FS is reduced due to T <sub>e_to_U_DJ1</sub> and T <sub>RJR1</sub> . Number of hubs operating at HS is reduced due to 2 3 1 SOP truncation and EOP dribble
2	3	1	
0	5	5	non-eUSB2 system for reference

#### 8.4.2 Power Down Mode

RESETB can be used as a power down pin when asserted low. Power down mode puts the TUSB2E11 in lowest power mode.

#### 8.4.3 Disabled Mode

The repeater can be disabled by setting DISABLE bit through the I<sup>2</sup>C.

#### 8.4.4 UART Mode

In I<sup>2</sup>C mode GPIO0 defaults to being an enable control for Carkit UART mode. GPIO0 is an active low signal to enable Carkit UART mode. GPIO0 is intended to be controlled through APU or SoC. When APU or SoC is not powered on or the firmware has not been loaded, the GPIO0 is low, enabling the UART mode to allow APU or SoC debug interface to be accessed through the USB port.

Default Carkit UART direction is DP → eDP (RX) and eDN → DN (TX).

On the rising edge of GPIO0, followed by T<sub>MODE\_SWITCH</sub>, the TUSB2E11 enables and enters the default state. In the default state, the TUSB2E11 is ready to accept eUSB2 port reset, configuration or RAP. The repeater mode will be configured as host or peripheral depending on the eUSB2-defined configuration received from eUSBr and acknowledged by the repeater.

UART mode enable is controlled through GPIO0 after power up. This can be changed through UART\_use\_bit1\_P1 bit in UART-PORT1 register, so UART mode enable can be controlled through a register instead of GPIO0.

#### 8.4.5 Auto-Resume ECR

Optional host repeater auto-resume is supported by the TUSB2E11 in L1/L2 by driving Resume K at D+/D- until SOResume is received from eDSPr. In addition, the TUSB2E11 eUSPh holds the Remote Wake line state until SOResume is received from eDSPr.

This auto-resume feature provides host controller extra time to exit low power state and issue SOResume while the TUSB2E11 UDSP drives resume within 1 ms (TURSM) hub resume timing requirement. To take advantage of this low power feature, host controller shall implement low power mechanism to detect wake on eDSPr lines while host controller is in low power state.

This auto-resume is not needed if host controller is capable of initiating SOResume within 1 ms of detecting Remote Wake on eDSPr.

This auto-resume is enabled by default but can be disabled via bit 6 of register 0x78. This auto-resume ECR mode is disabled when L2 interrupt mode is enabled. When L2 interrupt mode is enabled, resume K at D+/D- is still driven when Remote wake is detected on UDSP but eUSPh is held at SE0 instead of in Remote Wake state. See the *L2 State Interrupt Modes* section for more details.

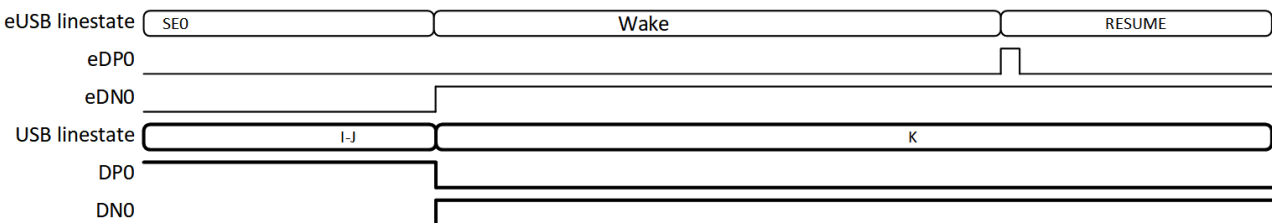


図 8-1. Timing Diagram for Auto-Resume for HS/FS

#### 8.4.6 L2 State Interrupt Modes

To prevent signaling on eUSB2 while the eDSP is powered off, make sure both L2 remote wake interrupt and disconnect event interrupt modes are enabled. The special remote wake sequence when L2 remote wake interrupt mode is enabled.

- System enables interrupt USB\_REMOTE\_WAKE\_P1.
- Repeater is in host mode and has received a CM.L2.
- Repeater detects wake on USB 2.0
- Repeater asserts interrupt.
- Repeater reflects *resume* on USB 2.0, but does not signal wake on eUSB2.
- Repeater waits for eDSPr to signal start of resume with no intervening configuration, connect, or reset sequence.

- Repeater and eDSP follow normal eUSB2 protocol to signal resume starting and ending in L0.

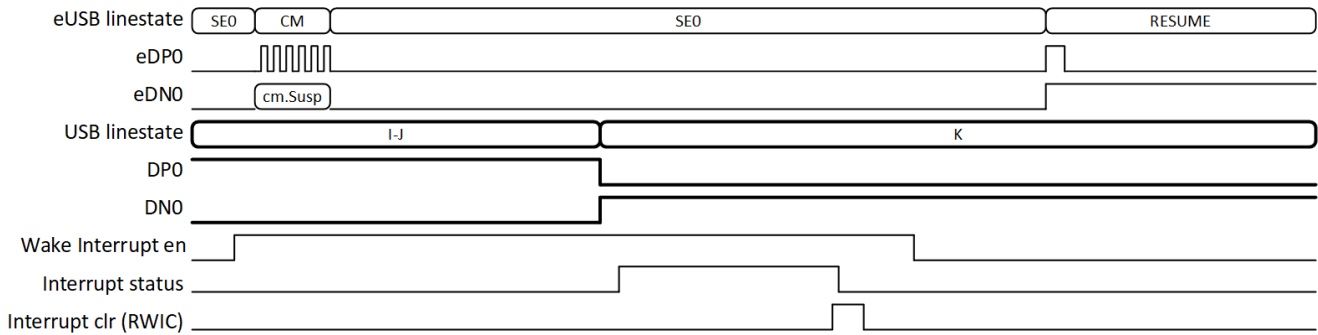


図 8-2. Timing Diagram for Wake Interrupt for HS/FS

The special wake on disconnect sequence when disconnect event interrupt mode is enabled

- System enables interrupt USB\_DISCONNECT\_P1.
- Repeater is in host mode and has received a CM.L2.
- Repeater detects SE0 for disconnect on USB 2.0.
- Repeater asserts interrupt.
- Interrupt must be cleared prior to eDSPr reinitializing the TUSB2E11 as a host.
- Repeater does not signal or report USB 2.0 SE0 on eUSB2.
- Repeater waits for eDSPr to power up, which starts with port reset announcement.
- Repeater and eDSP follow normal eUSB2 protocol, ending in unconnected state of host mode.

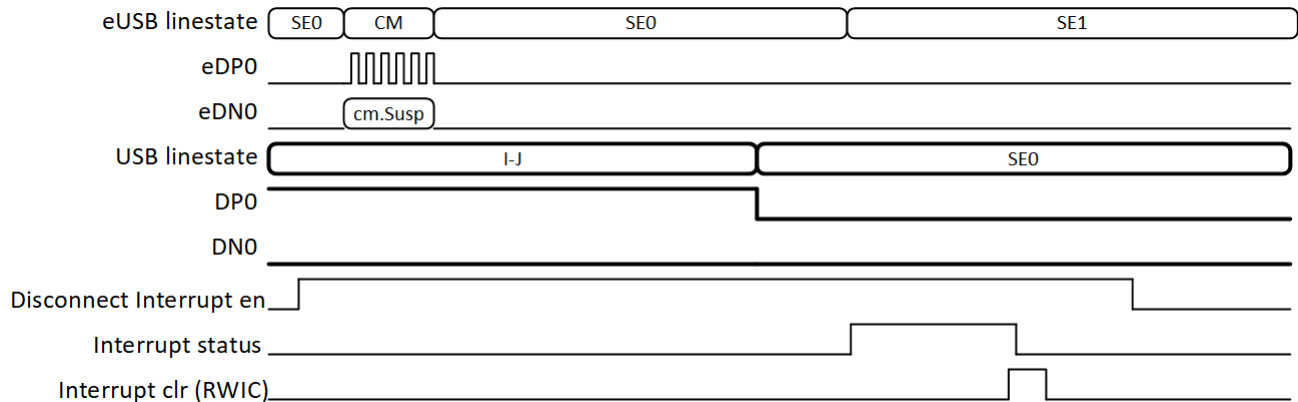
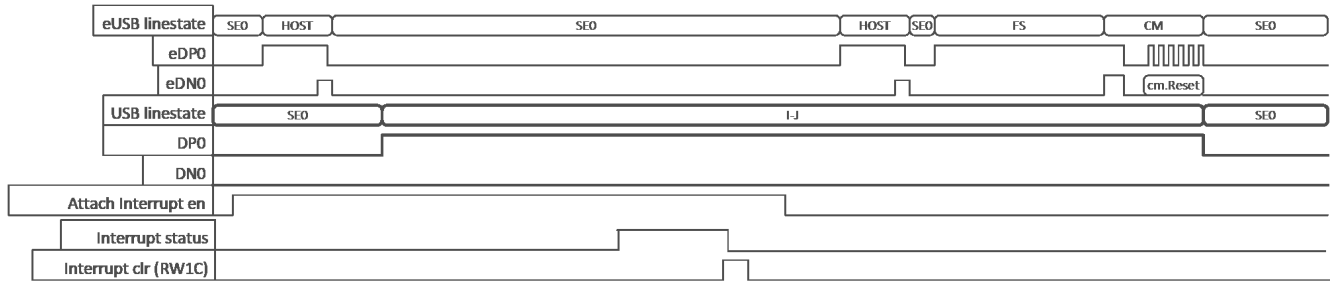


図 8-3. Timing Diagram for Disconnect Interrupt for HS/FS

#### 8.4.7 Attach Detect Interrupt Mode

When attach event detect is enabled, the TUSB2E11 issues an interrupt event instead of signaling attach on eUSB2.

- System enables interrupt USB\_DETECT\_ATTACH\_P1. Interrupt has to be enabled prior to any connect event.
- Repeater is in host mode.
- Repeater detects attach on USB 2.0.
- Repeater debounces attach for 60µs and asserts interrupt instead of signaling attach on eUSB2.
- Interrupt must be disabled prior to eDSPr reinitializing as a host to process attach through normal mechanism.



**8-4. Timing Diagram for Attach Detect Interrupt for HS/FS**

### 8.4.8 GPIO Mode

#### GPIO0

The GPIO0 pin is in input mode at power up, and is sampled during reset.

The GPIO0 defaults to active low UART mode (bypass mode) enable control after power up. This can be changed through the `UART_use_bit1_P1` bit in `UART-PORT1` register, so GPIO0 can be repurposed. Refer to [UART Mode](#).

The GPIO0 pin can be configured to be input or output mode through the I<sup>2</sup>C register write. Output event is selected through the I<sup>2</sup>C register. Refer to *GPIO0\_CONFIG register* for more information.

The GPIO0 input status change can be reported through the GPIO2 as an interrupt if enabled through the I<sup>2</sup>C. Status change trigger can be programmed to be edge trigger or level trigger through the I<sup>2</sup>C.

The GPIO0 pin in output mode defaults to open-drain output but can be configured to be push-pull output. GPIO0 pin can drive up to 3pF loads when in push-pull mode.

The GPIO0 pin reverts back to input upon RESETB assert, de-assert, or soft reset.

In non I<sup>2</sup>C mode, the GPIO0 is used for USB PHY tuning.

#### GPIO1

The GPIO1 pin is in input mode at power up, and is sampled during reset.

The GPIO1 is configured as an enable control for battery charger detection in repeater default state if `DEFAULT_STATE_BC_P1` is set to 0x01 through the `BC_CONTROL` register.

The GPIO1 pin can be configured to be input or output mode through the I<sup>2</sup>C register write. Output event is selected through the I<sup>2</sup>C register. Refer to *GPIO1\_CONFIG register*.

The GPIO1 input status change can be reported through the GPIO2 as an interrupt if enabled through the I<sup>2</sup>C. Status change trigger can be programmed to be edge trigger or level trigger through the I<sup>2</sup>C.

The GPIO1 pin in output mode defaults to open-drain output but can be configured to be push-pull output. GPIO1 pin can drive up to 3pF loads when in push-pull mode.

The GPIO1 pin reverts back to input upon RESETB assert, de-assert, or soft reset.

In non I<sup>2</sup>C mode, the GPIO1 is used for USB PHY tuning.

## GPIO2

The GPIO2 pin defaults to open drain interrupt (INT) active low output at power up but can be programmed through the I<sup>2</sup>C to be a push-pull output. In push-pull mode, the device can be programmed to be either active high or active low. The interrupt output is a level-sensitive interrupt. Trigger events can be selected through the I<sup>2</sup>C.

Connect GPIO2 to APU to use interrupt functions and a pullup resistor (open drain mode).

The GPIO2 interrupt output can be configured through the INT\_ENABLE and INT\_STATUS registers.

The GPIO2 can be configured as battery charger detect indicator instead of the interrupt output through the BC\_CONTROL register.

In non I<sup>2</sup>C mode, the GPIO2 is used for USB PHY tuning.

### 8.4.9 USB 2.0 High-Speed HOST Disconnect Detection

The USB 2.0 specification does not specify high-speed output differential swing  $V_{OD}$  during disconnect without external load. Only chirp level and the HS host disconnect threshold are specified. Specification implicitly assumes high-speed output differential swing  $V_{OD}$  doubles during disconnect. However, the high-speed output differential swing during disconnect depends on the USB 2.0 TX output swing and pre-emphasis setting, as the common-mode voltage increase saturates the output swing level. If the output swing level is saturated, the VOD may not double.

The HS host disconnect threshold shall be adjusted to provide the most margin to avoid false disconnect as well as failure to detect a disconnect. See [表 8-2](#).

**表 8-2. Recommended USB 2.0 High-speed HOST Disconnect Thresholds per USB HSTX Amplitude and Pre-Emphasis**

USB HS TX Amplitude (Vp-p)	USB HS TX Pre-Emphasis					
	0.5dB (0h)	0.9dB (1h)	1.2dB (2h)	1.7dB (3h)	2.1dB (4h)	2.5dB (5h)
740mV (0h)	545mV (1h)	545mV (1h)	545mV (1h)	545mV (1h)	545mV (1h)	545mV (1h)
760mV (1h)	565mV (2h)	565mV (2h)	565mV (2h)	565mV (2h)	565mV (2h)	565mV (2h)
780mV (2h)	585mV (3h)	585mV (3h)	585mV (3h)	585mV (3h)	585mV (3h)	585mV (3h)
800mV (3h)	585mV (3h)	585mV (3h)	585mV (3h)	585mV (3h)	585mV (3h)	585mV (3h)
820mV (4h)	605mV (4h)	605mV (4h)	605mV (4h)	605mV (4h)	605mV (4h)	605mV (4h)
840mV (5h)	625mV (5h)	625mV (5h)	625mV (5h)	625mV (5h)	625mV (5h)	625mV (5h)
860mV (6h)	645mV (6h)	645mV (6h)	645mV (6h)	645mV (6h)	625mV (5h)	625mV (5h)
880mV (7h)	645mV (6h)	645mV (6h)	645mV (6h)	645mV (6h)	645mV (6h)	645mV (6h)
900mV (8h)	665mV (7h)	665mV (7h)	665mV (7h)	665mV (7h)	665mV (7h)	645mV (6h)
920mV (9h)	685mV (8h)	685mV (8h)	685mV (8h)	665mV (7h)	665mV (7h)	665mV (7h)
940mV (Ah)	685mV (8h)	685mV (8h)	685mV (8h)	685mV (8h)	665mV (7h)	665mV (7h)
960mV (Bh)	705mV (9h)	705mV (9h)	705mV (9h)	685mV (8h)	685mV (8h)	665mV (7h)
980mV (Ch)	725mV (Ah)	705mV (9h)	705mV (9h)	705mV (9h)	685mV (8h)	685mV (8h)
1000mV (Dh)	725mV (Ah)	725mV (Ah)	705mV (9h)	705mV (9h)	685mV (8h)	685mV (8h)
1020mV (Eh)	725mV (Ah)	725mV (Ah)	725mV (Ah)	705mV (9h)	705mV (9h)	685mV (8h)
1040mV (Fh)	745mV (Bh)	725mV (Ah)	725mV (Ah)	705mV (9h)	705mV (9h)	685mV (8h)

### 8.4.10 Frame Based Low Power Mode

The USB2.0 standard defines high-speed microframes that occur every 125 $\mu$ s. Using a patented design, the TUSB2E11 monitors idle conditions within every high-speed microframe. The TUSB2E11 will enter a low power state if the bus is idle for greater than FRAME\_LP\_OFF\_THRESHOLD and will remain in the low power state

until the start of the next  $\mu$ SOF. This feature is enabled by default and can be disabled by clearing HOST\_FRAME\_LP\_EN or DEVICE\_FRAME\_LP\_EN bits.

表 8-3 shows an example of the typical high-speed idle power the TUSB2E11 consumes based on the value of the FRAME\_LP\_OFF\_THRESHOLD and whether or not the frame base low power is enabled. These results assume the TUSB2E11 is in host repeater mode.

**表 8-3. Typical High-Speed Idle Power for Frame Base LP Mode**

HOST_FRAME_LP_EN	FRAME_LP_OFF_THRESHOLD	1.8V current (mA)	3.3V current (mA)
0 (Disabled)	N/A	56	2.8
1 (Enabled)	0x0 (1/32)	11	2.0
1 (Enabled)	0x1 (1/16)	12	2.0
1 (Enabled)	0x2 (1/8)	15	2.1
1 (Enabled)	0x3 (1/4)	22	2.2

注

Frame based low power mode is enabled by default. If using TUSB2E11 in pin-strap mode, this feature can not be disabled. Contact [support](#) if a device variant with frame based low power mode disabled in pin-strap mode is needed.

#### 8.4.11 Battery Charging

The TUSB2E11 supports standard USB battery charging specification 1.2 (BC1.2) and the divider mode and 1.2V DCP proprietary charging protocols as listed in 表 8-4. The BC1.2 functionality includes charger advertisement and charger detection when enabled in non-I2C mode using strap (refer to 表 5-4) or I2C mode through register configuration.

When the TUSB2E11 is configured as a host repeater, the TUSB2E11 supports charger advertisement whereas when the TUSB2E11 is configured as peripheral repeater it supports charger detection. When configured as peripheral repeater, the TUSB2E11 detects charger type if Battery Charging detection in peripheral mode is enabled. The TUSB2E11 can detect ACP3, ACP2, ACP1, DCP 1.2V biased short mode, USB standard DCP short mode and CDP types of charger. When configured as a host repeater, the TUSB2E11 acts as charger advertiser if CDP is enabled. The TUSB2E11 can advertise ACP3, DCP 1.2V, DCP or CDP modes. When in an unconfigured state, the behavior of battery charging state machine is controlled by strap settings in non-I2C mode or by register settings in I2C mode. When the TUSB2E11 is in an unconfigured state charger advertisement mode, GPIO0 directs system to power-cycle VBUS to enable a portable device to exit dedicated charging port mode and switch to host or peripheral state where data transfer is possible.

**表 8-4. Battery Charging Supported Protocols**

Charging Protocol	Standard or Proprietary	Charging Current (A)	Data Transfer Allowed	Charger Detection or Advertise
SDP (Standard Downstream Port)	Standard BC1.2	0.5 or 0.9	Yes	Detection
CDP (Charging Downstream Port)	Standard BC1.2	1.5	Yes	Detection and Advertise
DCP (Dedicated Charging Port)	Standard BC1.2	1.5	No	Detection and Advertise
1.2V DCP	Proprietary	2	No	Detection and Advertise
ACP0 or Divider Mode 0	Proprietary	0.5	No	Detection
ACP1 or Divider Mode 1	Proprietary	1	No	Detection
ACP2 or Divider Mode 2	Proprietary	2.1	No	Detection
ACP3 or Divider Mode 3	Proprietary	2.4	No	Detection and Advertise

In I2C mode, the behavior of the battery charging state machine in the TUSB2E11 is controlled by the DEFAULT\_STATE\_BC\_P1, BC\_DETECTION\_EN\_P1, and CDP\_2\_EN\_P1 register fields. In the unconfigured state, the battery charging state machine also depends on EN\_BC input from GPIO1 in I2C mode.

**表 8-5. Battery Charging Behavior in I2C Mode**

GPIO1 (BC_EN)	DEFAULT_STATE_BC_P1 bit	TUSB2E11 Behavior in each state		
		Unconfigured	Host Repeater	Peripheral repeater
Low	X	No action	As per CDP_2_EN_P1.	Act as charger detector including divider mode detector once SOC directs repeater to connect when BC_DETECTION_EN_P1 set.
High	0x0	No Action		
High	0x1	Act as a charger detector including divider mode.		
High	0x2	Advertise standard DCP if 1P2V_MODE_DIS = 1, else advertise 1.2V DCP.		
High	0x3	If 1P2V_MODE_DIS = 0, then advertise ACP3 → 1.2V DCP → DCP until no connect in auto cycling mode. If 1P2V_MODE_DIS = 1 then advertise ACP3 → DCP until no connect in auto cycling mode.		

## 8.5 Manufacturing Test Modes

The following test procedures show how to use I<sup>2</sup>C to enter test modes to perform continuity test of DP/DM during manufacturing or debug. During this mode the TUSB2E11 does not operate as a repeater.

### 8.5.1 USB DP Test Procedure

I<sup>2</sup>C Commands to use DP pullup to test DP/DM continuity:

Enable GPIOs and DP Pull-up:

h00, hA0 <-set gpio0 to push-pull output mode

h40, hA0 <-set gpio1 to push-pull output mode

hD5, h28

hD6, h04

hD7, h10 <-DP pullup is now on

hCE, h18

hDC, h15 <-muxes DP / DM status onto GPIO lines

Status Readback Check:

h00 = hA0 <-DM status on bit 4 (normal, DM low)

h40 = hB0 <-DP status on bit 4 (normal, DP high)

h00 = hB0 <-DM status on bit 4 (DP + DM shorted together)

h40 = hA0 <-DP status on bit 4 (DP shorted to ground)

Exit Test Mode:

hB2, h80 <-soft reset (end test)

### 8.5.2 USB DM Test Procedure

I<sup>2</sup>C Commands to use DM pullup to test DP/DM continuity:

Enable GPIOs and DM Pull-up:

h00, hA0 <-set gpio0 to push-pull output mode

h40, hA0 <-set gpio1 to push-pull output mode

hD5, h28

hD6, h04

hD7, h08 <-DM pullup is now on

hCE, h18

hDC, h15 <-mux DP / DM status onto GPIO lines

Status Readback Check:

h00 = hB0 <-DM status on bit 4 (normal, DM high)

h40 = hA0 <-DP status on bit 4 (normal, DP low)

h40 = hB0 <-DP status on bit 4 (DP + DM shorted together)

h00 = hA0 <-DM status on bit 4 (DM shorted to ground)

Exit Test Mode:

hB2, h80 <-soft reset (end test)



## 8.6 I<sup>2</sup>C Target Interface

I<sup>2</sup>C target interface enables access to internal registers by the system application processor. The primary function of the interface is to enable configuring various PHY parameters, controlling the GPIO pins, and enabling USB-BC functions. The TUSB2E11 repeater functions operate upon power up without requiring I<sup>2</sup>C configuration.

The TUSB2E11 has I<sup>2</sup>C 7-bit target address of 0x3E. 8-bit address of Write: 0x7C and Read: 0x7D.

I<sup>2</sup>C default target address can be changed at the factory through one time programming.

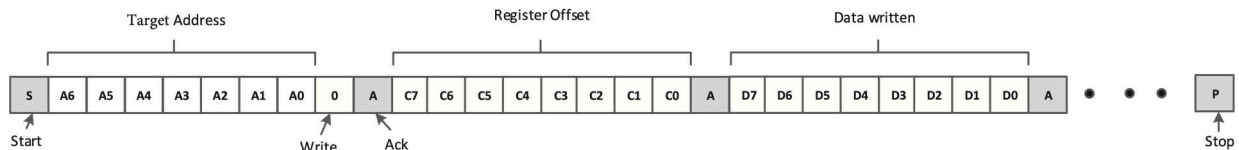
I<sup>2</sup>C drive strength can be changed through the I<sup>2</sup>C.

**表 8-6. Recommended I<sup>2</sup>C Drive Strength for I<sup>2</sup>C Bus Speed, Bus Pull Up and Bus Capacitance**

I <sup>2</sup> C FM+ (1MHz Max)	I <sup>2</sup> C drive strength (I <sub>OL</sub> ) selection			
	I <sup>2</sup> C bus pullup R <sub>PU</sub>			
C(bus)pF	1kΩ	2.2kΩ	4kΩ	7kΩ
10-50	≅8mA	≅4mA	N/A	N/A
10-90	≅8mA	N/A	N/A	N/A
10-150	N/A	N/A	N/A	N/A
10-200	N/A	N/A	N/A	N/A

I <sup>2</sup> C FM (400kHz Max)	I <sup>2</sup> C drive strength (I <sub>OL</sub> ) selection			
	I <sup>2</sup> C bus pullup R <sub>PU</sub>			
C(bus)pF	1kΩ	2.2kΩ	4kΩ	7kΩ
10-50	≅8mA	≅4mA	≅2mA	N/A
10-90	≅8mA	≅4mA	N/A	N/A
10-150	≅8mA	≅8mA	N/A	N/A
10-200	≅8mA	N/A	N/A	N/A

I <sup>2</sup> C STD (100kHz Max)	I <sup>2</sup> C drive strength (I <sub>OL</sub> ) selection			
	I <sup>2</sup> C bus pullup R <sub>PU</sub>			
C(bus)pF	1kΩ	2.2kΩ	4kΩ	7kΩ
10-50	≅8mA	≅4mA	≅2mA	≅1mA
10-90	≅8mA	≅4mA	≅2mA	≅1mA
10-150	≅8mA	≅4mA	≅2mA	≅2mA
10-200	≅8mA	≅4mA	≅2mA	≅2mA

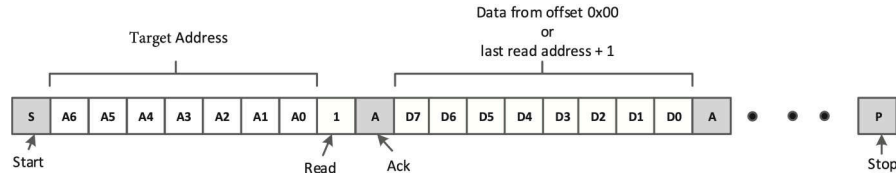


**図 8-5. I<sup>2</sup>C Write with Data**

Use the following procedure to write data to the TUSB2E11 I<sup>2</sup>C registers (refer to 図 8-5):

1. The host initiates a write operation by generating a start condition (S), followed by the TUSB2E11 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TUSB2E11 acknowledges the address cycle.
3. The host presents the register offset within the TUSB2E11 to be written, consisting of one byte of data, MSB-first.
4. The TUSB2E11 acknowledges the sub-address cycle.

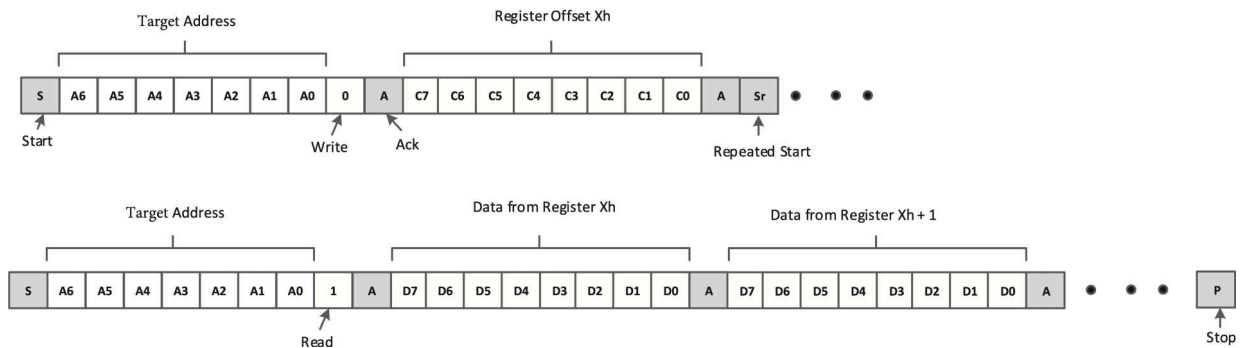
- The host presents the first byte of data to be written to the I<sup>2</sup>C register.
- The TUSB2E11 acknowledges the byte transfer.
- The host may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the TUSB2E11.
- The host terminates the write operation by generating a stop condition (P).



**図 8-6. I<sup>2</sup>C Read Without Repeated Start**

Use the following procedure to write data to the TUSB2E11 I<sup>2</sup>C registers without a repeated Start (refer [図 8-6](#)).

- The host initiates a read operation by generating a start condition (S), followed by the TUSB2E11 7-bit address and a zero-value “W/R” bit to indicate a read cycle.
- The TUSB2E11 acknowledges the 7-bit address cycle.
- Following the acknowledge the host continues sending clock.
- The TUSB2E11 transmit the contents of the memory registers MSB-first starting at register 00h or last read register offset+1. If a write to the I<sup>2</sup>C register occurred prior to the read, then the TUSB2E11 shall start at the register offset specified in the write.
- The TUSB2E11 waits for either an acknowledge (ACK) or a not-acknowledge (NACK) from the host after each byte transfer; the I<sup>2</sup>C host acknowledges reception of each data byte transfer.
- If an ACK is received, the TUSB2E11 transmits the next byte of data as long as host provides the clock. If a NAK is received, the TUSB2E11 stops providing data and waits for a stop condition (P).
- The host terminates the write operation by generating a stop condition (P).



**図 8-7. I<sup>2</sup>C Read with Repeated Start**

Use the following procedure to write data to the TUSB2E11 I<sup>2</sup>C registers with a repeated Start (refer [図 8-7](#)).

- The host initiates a read operation by generating a start condition (S), followed by the TUSB2E11 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
- The TUSB2E11 acknowledges the 7-bit address cycle.
- The host presents the register offset within the TUSB2E11 to be written, consisting of one byte of data, MSB-first.
- The TUSB2E11 acknowledges the register offset cycle.
- The host presents a repeated start condition (Sr).
- The host initiates a read operation by generating a start condition (S), followed by the TUSB2E11 7-bit address and a one-value “W/R” bit to indicate a read cycle.
- The TUSB2E11 acknowledges the 7-bit address cycle.
- The TUSB2E11 transmit the contents of the memory registers MSB-first starting at the register offset.

9. The TUSB2E11 shall wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the host after each byte transfer; the I<sup>2</sup>C host acknowledges reception of each data byte transfer.
10. If an ACK is received, the TUSB2E11 transmits the next byte of data as long as host provides the clock. If a NAK is received, the TUSB2E11 stops providing data and waits for a stop condition (P).
11. The host terminates the read operation by generating a stop condition (P).

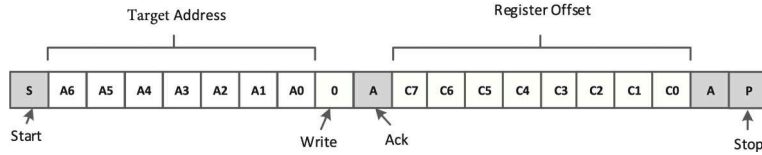


図 8-8. I<sup>2</sup>C Write Without Data

Use the following procedure to set a starting sub-address for I<sup>2</sup>C reads (refer to 図 8-8).

1. The host initiates a write operation by generating a start condition (S), followed by the TUSB2E11 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TUSB2E11 acknowledges the address cycle.
3. The host presents the register offset within the TUSB2E11 to be written, consisting of one byte of data, MSB-first.
4. The TUSB2E11 acknowledges the register offset cycle.
5. The host terminates the write operation by generating a stop condition (P).

注

After initial power-up, if no register offset is included for the read procedure (refer to 図 8-6), then reads start at register offset 00h and continue byte by byte through the registers until the I<sup>2</sup>C host terminates the read operation. During a read operation, the TUSB2E11 auto-increments the I<sup>2</sup>C internal register address of the last byte transferred independent of whether or not an ACK was received from the I<sup>2</sup>C host.

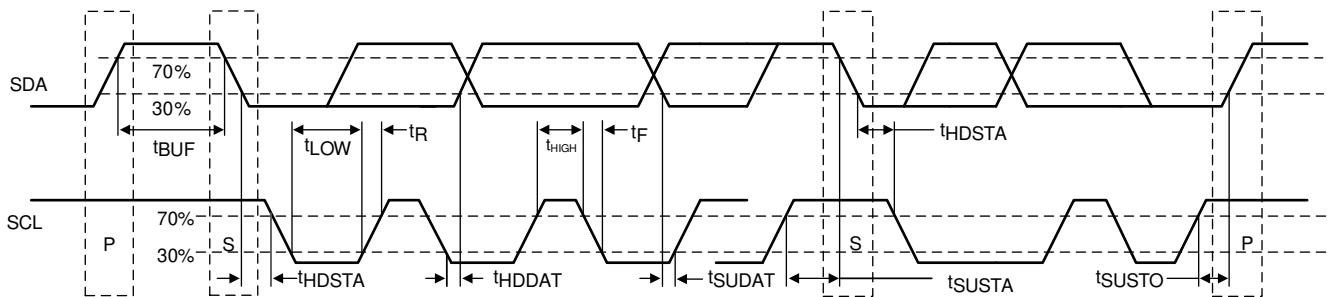


図 8-9. I<sup>2</sup>C Timing Diagram

## 9 Register Access Protocol (RAP)

The repeater in the TUSB2E11 supports the register access protocol (RAP) over eUSB2 to allow access to the related registers.

RAP accessible registers are indicated with corresponding RAP addresses in the register map. Default value of a subset of the registers are factory programmable and are indicated in register map.

## 10 Register Map

### 10.1 TUSB2E11 Registers

表 10-1 lists the TUSB2E11 registers. All register offset addresses not listed in 表 10-1 should be considered as reserved locations and the register contents should not be modified.

**表 10-1. TUSB2E11 Registers**

Offset	Acronym	Register Name	Section
70h	U_TX_ADJUST_PORT1	RAP Register for Port 1 (0h), Default through OTP	<a href="#">Go</a>
71h	U_HS_TX_PRE_EMPHASIS_P1	RAP Register for Port 1 (1h), Default through OTP	<a href="#">Go</a>
72h	U_RX_ADJUST_PORT1	RAP Register for Port 1 (2h), Default through OTP	<a href="#">Go</a>
73h	U_DISCONNECT_SQUELCH_PORT1	RAP Register for Port 1 (3h), Default through OTP	<a href="#">Go</a>
77h	E_HS_TX_PRE_EMPHASIS_P1	RAP Register for Port 1 (7h), Default through OTP	<a href="#">Go</a>
78h	E_TX_ADJUST_PORT1	RAP Register for Port 1 (8h), Default through OTP	<a href="#">Go</a>
79h	E_RX_ADJUST_PORT1	RAP Register for Port 1 (9h), Default through OTP	<a href="#">Go</a>
0h	GPIO0_CONFIG		<a href="#">Go</a>
40h	GPIO1_CONFIG		<a href="#">Go</a>
50h	UART_PORT1	RAP Register for Port 1 (20h)	<a href="#">Go</a>
B0h	REV_ID		<a href="#">Go</a>
B2h	GLOBAL_CONFIG		<a href="#">Go</a>
B3h	INT_ENABLE_1		<a href="#">Go</a>
B4h	INT_ENABLE_2		<a href="#">Go</a>
B5h	FRAME_LP_CONTROL	Controls for Frame Based LP mode	<a href="#">Go</a>
B6h	BC_CONTROL		<a href="#">Go</a>
B7h	BC_STATUS_1		<a href="#">Go</a>
A3h	INT_STATUS_1		<a href="#">Go</a>
A4h	INT_STATUS_2		<a href="#">Go</a>
60h	CONFIG_PORT1		<a href="#">Go</a>
F5h	TEST_MODE1		<a href="#">Go</a>

Complex bit access types are encoded to fit into small table cells. 表 10-2 shows the codes that are used for access types in this section.

**表 10-2. TUSB2E11 Access Type Codes**

Access Type	Code	Description
Read Type		
H	H	Set or cleared by hardware
R	R	Read
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
WtoP	W	Write
Reset or Default Value		
- n		Value after reset or the default value

### 10.1.1 GPIO0\_CONFIG Register (Offset = 00h) [Reset = 00h]

GPIO0\_CONFIG is shown in [GPIO0\\_CONFIG Register Field Descriptions](#).

Return to the [Summary Table](#).

**表 10-3. GPIO0\_CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	GPIO0_OD_PP	R/W	0h	GPIO0 output type 0h = open-drain output 1h = push pull output
6	Reserved	R	0h	Reserved
5	GPIO0_DIRECTION	R/W	0h	GPIO0 direction 0h = input 1h = output
4	GPIO0_INPUT_STATUS	RH	0h	Logical value of GPIO0 pin input (0=Low, 1=High) 0h = input is low 1h = input is high
3-0	GPIO0_OUTPUT_SELECT	R/W	0h	Dh = HIGH_OUTPUT – output is forced static high Eh = LOW_OUTPUT – output is forced static low

### 10.1.2 GPIO1\_CONFIG Register (Offset = 40h) [Reset = 00h]

GPIO1\_CONFIG is shown in [GPIO1\\_CONFIG Register Field Descriptions](#).

Return to the [Summary Table](#).

**表 10-4. GPIO1\_CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	GPIO1_OD_PP	R/W	0h	GPIO1 output type selection 0h = open-drain output 1h = push pull output
6	GPIO1_IN_TRIGGER_TYPE	R/W	0h	GPIO1 input trigger type selection for interrupt 0h = edge trigger input 1h = level trigger input (GPIO2 output reflects the input level state)
5	GPIO1_DIRECTION	R/W	0h	GPIO1 direction selection 0h = input 1h = output
4	GPIO1_INPUT_STATUS	RH	0h	Logical value of GPIO1 pin input status (0=Low, 1=High) 0h = input is low 1h = input is high

表 10-4. GPIO1\_CONFIG Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
3-0	GPIO1_OUTPUT_SELECTION	R/W	0h	<p>GPIO1 output selection</p> <p>0h = Remote wakeup – host repeater is receiving remote wake but has not seen start of resume</p> <p>1h = USB disconnect – host repeater is actively forwarding LS/FS disconnect.</p> <p>2h = USB_HS_Unsquelched – host repeater in L0 seeing USB HS or in reset seeing Chirp</p> <p>3h = PVTB – HOST repeater is actively transmitting ESE1 due to HS disconnect.</p> <p>4h = DEFAULT – waiting to be configured host/peripheral</p> <p>5h = HOST – in host repeater mode</p> <p>6h = PERIPHERAL – in peripheral repeater mode</p> <p>7h = CONNECTED – repeater is connected, connection seen acknowledged by start of reset</p> <p>8h = RESET – reset in progress, reset is detected is high, L0 is low</p> <p>9h = L0 – fully configured and repeating data, keep-alive and reset/disconnect</p> <p>Ah = L1 – device has received CM.FS/CM.L1, has stopped repeating and is waiting for wake or resume</p> <p>Bh = L2 – device has received CM.L2, has stopped repeating and is waiting for wake or resume.</p> <p>Ch = GPIO1_HS_TEST – in host repeater in L0 mode, received CM.TEST</p> <p>Dh = HIGH_OUTPUT – output is forced static high</p> <p>Eh = LOW_OUTPUT – output is forced static low</p> <p>Fh = OVP – over voltage (DP/DN voltage &gt; VOVP_TH) detected on the USB DP/DN</p>

### 10.1.3 U\_TX\_ADJUST\_PORT1 Register (Offset = 70h) [Reset = 7Ch]

U\_TX\_ADJUST\_PORT1 is shown in [表 10-5](#).

Return to the [Summary Table](#).

Hardware default value can be overridden through factory programmable OTP for this register.

表 10-5. U\_TX\_ADJUST\_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	U_HS_TERM_P1	RH/W	1h	<p>0h = 42.75Ω (typical)</p> <p>1h = 45Ω (typical) (default)</p> <p>2h = 47.25Ω (typical)</p> <p>3h = 49.5Ω (typical)</p>
5-4	U_HS_TX_SLEW_RATE_P1	RH/W	3h	<p>0h = 425 ps (typical)</p> <p>1h = 465 ps (typical)</p> <p>2h = 510 ps (typical)</p> <p>3h = 625 ps (typical) (OTP default)</p>

表 10-5. U\_TX\_ADJUST\_PORT1 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
3-0	U_HS_TX_AMPLITUDE_P1	RH/W	Ch	0h = 800mV – 7.5%, 740mV (typical) 1h = 800mV – 5.0%, 760mV (typical) 2h = 800mV – 2.5%, 780mV (typical) 3h = 800mV (USB 2.0 specification nominal), 800mV (typical) (B0 OTP default) 4h = 800mV + 2.5%, 820mV (typical) 5h = 800mV + 5.0%, 840mV (typical) 6h = 800mV + 7.5%, 860mV (typical) 7h = 800mV + 10%, 880mV (typical) 8h = 800mV + 12.5%, 900mV (typical) 9h = 800mV + 15%, 920mV (typical) Ah = 800mV + 17.5%, 940mV (typical) Bh = 800mV + 20%, 960mV (typical) Ch = 800mV + 22.5%, 980mV (typical) (B1 OTP default) Dh = 800mV + 25%, 1000mV (typical) Eh = 800mV + 27.5%, 1020mV (typical) Fh = 800mV + 30%, 1040mV (typical)

#### 10.1.4 U\_HS\_TX\_PRE\_EMPHASIS\_P1 Register (Offset = 71h) [Reset = 3Ch]

U\_HS\_TX\_PRE\_EMPHASIS\_P1 is shown in 表 10-6.

Return to the [Summary Table](#).

Hardware default value can be overridden through factory programmable OTP for this register.

表 10-6. U\_HS\_TX\_PRE\_EMPHASIS\_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CDP_2_EN_P1	RH/W	0h	0h = CDP advertising disabled 1h = CDP advertising enabled
6	Reserved	RH/W	0h	Reserved
5-4	U_HS_TX_PE_WIDTH_P1	RH/W	3h	0h = 0.35 UI (typical) 1h = 0.45 UI (typical) 2h = 0.55 UI (typical) 3h = 0.65 UI (typical) (OTP default)
3	U_HS_TX_PE_ENABLE_P1	RH/W	1h	USB HS TX pre-emphasis enable Default through OTP PE is disabled during chirp J (VCHIRPJ) or chirp K (VCHIRPK) 0h = Disabled 1h = Enabled (OTP default)
2-0	U_HS_TX_PRE_EMPHASIS_P1	RH/W	4h	0h = 0.5dB (typical) (B0 OTP default) 1h = 0.9dB (typical) 2h = 1.2dB (typical) 3h = 1.7dB (typical) 4h = 2.1dB (typical) (B1 OTP default) 5h = 2.5dB (typical) 6h = not recommended 7h = not recommended

#### 10.1.5 U\_RX\_ADJUST\_PORT1 Register (Offset = 72h) [Reset = 92h]

U\_RX\_ADJUST\_PORT1 is shown in 表 10-7.

Return to the [Summary Table](#).

Hardware default value can be overridden through factory programmable OTP for this register.

表 10-7. U\_RX\_ADJUST\_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	RH/W	9h	Reserved
3	Reserved	RH/W	0h	Reserved
2-0	U_EQ_P1	RH/W	2h	0h = 0.06dB (typical) (B0 OTP default) 1h = 0.58dB (typical) 2h = 1.09dB (typical) (B1 OTP default) 3h = 1.56dB (typical) 4h = 2.26dB (typical) 5h = 2.67dB (typical) 6h = 3.03dB (typical) 7h = 3.35dB (typical)

### 10.1.6 U\_DISCONNECT\_SQUELCH\_PORT1 Register (Offset = 73h) [Reset = 83h]

U\_DISCONNECT\_SQUELCH\_PORT1 is shown in 表 10-8.

Return to the [Summary Table](#).

Hardware default value can be overridden through factory programmable OTP for this register.

表 10-8. U\_DISCONNECT\_SQUELCH\_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	U_DISCONNECT_THRES HOLD_P1	RH/W	8h	0h = 525mV (minimum), 0% (B0 OTP default) 1h = 545mV (minimum), +4% 2h = 565mV (minimum), +8% 3h = 585mV (minimum), +11% 4h = 605mV (minimum), +15% 5h = 625mV (minimum), +19% 6h = 645mV (minimum), +23% 7h = 665mV (minimum), +27% 8h = 685mV (minimum) (B1 OTP default), +31% 9h = 705mV (minimum), +34% Ah = 725mV (minimum), +38% Bh = 745mV (minimum), +42% Ch = 765mV (minimum), +46% Dh = 785mV (minimum), +50% Eh = 805mV (minimum), +53% Fh = 825mV (minimum), +57%
3	Reserved	RH/W	0h	Reserved
2-0	U_SQUELCH_THRESHO LD_P1	RH/W	3h	0h = 130mV (minimum), +30% 1h = 124mV (minimum), +24% 2h = 117mV (minimum), +17% 3h = 111mV (minimum), +11% (B1 OTP default) 4h = 104mV (minimum), +4% (B0 OTP default) 5h = 98mV (minimum), -2% 6h = 91mV (minimum), -9% 7h = 85mV (minimum), -15%

### 10.1.7 E\_HS\_TX\_PRE\_EMPHASIS\_P1 Register (Offset = 77h) [Reset = 0h]

E\_HS\_TX\_PRE\_EMPHASIS\_P1 is shown in 表 10-9.

Return to the [Summary Table](#).

Hardware default value can be overridden through factory programmable OTP for this register.



**表 10-9. E\_HS\_TX\_PRE\_EMPHASIS\_P1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-5	E_HS_TX_PRE_EMPHASIS_P1	RH/W	0h	0h = 0dB (typical) (default) 1h = 0.67dB (typical) 2h = 1.29dB (typical) 3h = 1.87dB (typical) 4h = 2.41dB (typical) 5h = 2.92dB (typical) 6h = 3.41dB (typical) 7h = 3.86dB (typical)
4-3	E_HS_TX_PE_WIDTH_P1	RH/W	0h	0h = 0.40 UI (typical) (default) 1h = 0.5 UI (typical) 2h = 0.55 UI (typical) 3h = 0.65 UI (typical)
2-1	Reserved	RH/W	0h	Reserved
0	BC_DETECTION_ENABLE_P1	RH/W	0h	Enables battery charger (BC) detection during peripheral repeater mode. BC detection is disabled if the corresponding register is written low. Detection enable is further gated with connect announcement by SoC. After detection attempt completes, repeater enables the pull up. 0h = detection disabled. 1h = detection enabled

### 10.1.8 E\_TX\_ADJUST\_PORT1 Register (Offset = 78h) [Reset = 0Bh]

E\_TX\_ADJUST\_PORT1 is shown in [表 10-10](#).

Return to the [Summary Table](#).

Hardware default value can be overridden through factory programmable OTP for this register.

**表 10-10. E\_TX\_ADJUST\_PORT1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	Reserved	RH/W	0h	Reserved
6	Autoresume Disable	RH/W	0h	Added in B1 0h = autoresume enabled 1h = autoresume disabled
5	Reserved	RH/W	0h	Reserved
4-3	E_HS_TX_SLEW_RATE_P1	RH/W	1h	0h = 390 ps (typical) 1h = 440 ps (typical) (default) 2h = 460 ps (typical) 3h = 490 ps (typical)
2-0	E_HS_TX_AMPLITUDE_P1	RH/W	3h	0h = 360mV (typical) 1h = 380mV (typical) 2h = 400mV (typical) 3h = 420mV (typical) (default) 4h = 440mV (typical) 5h = 460mV (typical) 6h = 480mV (typical) 7h = 500mV (typical)

### 10.1.9 E\_RX\_ADJUST\_PORT1 Register (Offset = 79h) [Reset = 60h]

E\_RX\_ADJUST\_PORT1 is shown in [表 10-11](#).

Return to the [Summary Table](#).

Hardware default value can be overridden through factory programmable OTP for this register.

表 10-11. E\_RX\_ADJUST\_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	RH/W	0h	Reserved
6-4	E_SQUELCH_THRESHO LD_P1	RH/W	6h	0h = 104mV (typical) 1h = 101mV (typical) 2h = 98mV (typical) 3h = 90mV (typical) 4h = 81mV (typical) (B0 OTP default) 5h = 73mV (typical) 6h = 67mV (typical) (B1 OTP default) 7h = 60mV (typical)
3-0	E_EQ_P1	RH/W	0h	0h = 0.34dB (typical) (default) 1h = 0.71dB (typical) 2h = 1.02dB (typical) 3h = 1.36dB (typical) 4h = 1.64dB (typical) 5h = 1.94dB (typical) 6h = 2.19dB (typical) 7h = 2.45dB (typical) 8h = 2.69dB (typical) 9h = 2.93dB (typical) Ah = 3.13dB (typical) Bh = 3.35dB (typical) Ch = 3.53dB (typical) Dh = 3.72dB (typical) Eh = 3.89dB (typical) Fh = 4.07dB (typical)

#### 10.1.10 UART\_PORT1 Register (Offset = 50h) [Reset = 02h]

UART\_PORT1 is shown in 表 10-12.

Return to the [Summary Table](#).

表 10-12. UART\_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	0h	Reserved
4	uart_cross_P1	R/W	0h	Select whether plus and minus pins are crossed between USB 2.0 and eUSB2 during UART mode 0h = if UART mode is enabled, pair eD+ with D+ and eD- with D- 1h = if UART mode is enabled, pair eD+ with D- and eD- with D+
3	UART_use_bit1_P1	R/W	0h	Select whether UART enable select is set by register bit 1 or not 0h = bit 1 ignored. UART mode enabled by GPIO0 1h = bit 1 (UART_en_by_reg_not_pin_P1) enabled
2	UART_dir_not_Carkit_P1	R/W	0h	Set UART mode, direction, low for Carkit and high for opposite 0h = UART mode uses Carkit directions, D+ to eUSB2 and eD- to USB 2.0 1h = UART mode directions are opposite of Carkit, D- to eUSB2 and eD+ to USB 2.0
1	UART_en_by_reg_not_pin_P1	R/W	1h	Select whether Carkit UART mode is enabled by register or by GPIO0 pin 0h = select GPIO0 pin to enable UART mode 1h = select UART_mode_en_P1 register to enable UART mode
0	UART_mode_en_P1	R/W	0h	If GPIO0 is not selected to enable Carkit UART mode, this register enables the Carkit UART mode. 0h = disable UART mode between eUSB2 and USB 2.0 pins 1h = enable UART mode between eUSB2 and USB 2.0 pins

### 10.1.11 REV\_ID Register (Offset = B0h) [Reset = 02h]

REV\_ID is shown in [表 10-13](#).

Return to the [Summary Table](#).

**表 10-13. REV\_ID Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	REV_ID	RH	02h	Device revision. 01h = A0 02h = B0 03h = B1

### 10.1.12 GLOBAL\_CONFIG Register (Offset = B2h) [Reset = 0h]

GLOBAL\_CONFIG is shown in [表 10-14](#).

Return to the [Summary Table](#).

**表 10-14. GLOBAL\_CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	SOFT_RST	HWtoP	0h	Writing a 1 to this field is equivalent to pulsing RESETB low
6	DISABLE_P1	R/W	0h	Disabled Mode Repeater 1 (I2C remains Active) (If port is not disconnected, wait until disconnect event to disable the repeater) 0h = repeater enabled 1h = repeater disabled
5	Reserved	R	0h	Reserved
4	GPIO2_OUT_TYPE	R/W	0h	GPIO2 output type 0h = open drain 1h = push-pull
3	GPIO2_POLARITY	R/W	0h	GPIO2 pin polarity in push-pull mode only (open-drain mode is always active low) 0h = active high 1h = active low
2-0	Reserved	R	0h	Reserved

### 10.1.13 INT\_ENABLE\_1 Register (Offset = B3h) [Reset = 00h]

INT\_ENABLE\_1 is shown in [INT\\_ENABLE\\_1 Register Field Descriptions](#).

Return to the [Summary Table](#).

**表 10-15. INT\_ENABLE\_1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	GPIO1_RISING_EDGE	R/W	0h	INT_GPIO1_RISING_EDGE enable. When GPIO1_IN_TRIGGER_TYPE = 0 (Edge), this enables interrupt on Rising Edge of GPIO1. When GPIO1_IN_TRIGGER_TYPE = 1 (Level), this enables interrupt when GPIO1 = High. 0h = not enabled 1h = enabled

表 10-15. INT\_ENABLE\_1 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
6	GPIO1_FALLING_EDGE	R/W	0h	INT_GPIO1_FALLING_EDGE enable. When GPIO1_IN_TRIGGER_TYPE = 0 (Edge), this enables interrupt on Falling Edge of GPIO1. When GPIO1_IN_TRIGGER_TYPE = 1 (Level), this enables interrupt when GPIO1 = Low. 0h = not enabled 1h = enabled
5	Reserved	R	0h	Reserved
4	Reserved	R	0h	Reserved
3	USB_REMOTE_WAKE_P1	R/W	0h	INT_USB_REMOTE_WAKE_P1 enable. See <a href="#">セクション 8.4.6</a> 0h = not enabled 1h = enabled
2	USB_DISCONNECT_P1	R/W	0h	INT_USB_DISCONNECT_P1 enable. See <a href="#">セクション 8.4.6</a> 0h = not enabled 1h = enabled
1	Reserved	R	0h	Reserved
0	Reserved	R	0h	Reserved

#### 10.1.14 INT\_ENABLE\_2 Register (Offset = B4h) [Reset = 00h]

INT\_ENABLE\_2 is shown in [INT\\_ENABLE\\_2 Register Field Descriptions](#).

Return to the [Summary Table](#).

表 10-16. INT\_ENABLE\_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_OVERRIDE_EN	R/W	0h	Override GPIO2 INT output 0h = not enabled 1h = enabled See INT_VALUE
6	INT_VALUE	R/W	0h	Value to drive on GPIO2 when INT_OVERRIDE_EN=1 GPIO2 output pin indicates the interrupt assertion. The GPIO2 output pin follows the GPIO2 pin configuration. In open-drain mode the GPIO2 output pin is active low to indicate interrupt assertion. In push-pull mode, the GPIO2 output pin follows active low/high configuration to indicate GPIO2 assertion. 0h = output: interrupt not asserted 1h = output: interrupt asserted
5	BC_CHG_DET_P1	R/W	0h	INT_BC_CHG_DET_P1 enable. 0h = not enabled 1h = enabled
4	Reserved	R	0h	Reserved
3	USB_DETECT_ATTACH_P1	R/W	0h	INT_USB_DET_ATTACH_P1 enable. Enable device attach detection while eDSP is powered down See <a href="#">セクション 8.4.7</a> 0h = not enabled 1h = enabled
2	Reserved	R	0h	Reserved
1	USB_OVP_P1	R/W	0h	Over Voltage Port 1 interrupt enable 0h = not enabled 1h = enabled

**表 10-16. INT\_ENABLE\_2 Register Field Descriptions (続き)**

Bit	Field	Type	Reset	Description
0	Reserved	R	0h	Reserved

### 10.1.15 FRAME\_LP\_CONTROL Register (Offset = B5h) [Reset = A2h]

BC\_CONTROL is shown in [表 10-17](#).

Return to the [Summary Table](#).

**表 10-17. FRAME\_LP\_CONTROL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	HOST_FRAME_LP_EN	RH/W	1h	Host repeater frame-based low power enable. Default via OTP 0 = Not Enabled 1 = Enabled
6	DEVICE_FRAME_LP_EN	RH/W	0h	Peripheral repeater frame-based low power enable. Default via OTP 0 = Not Enabled 1 = Enabled
5	Reserved	R	1h	Reserved
4	Reserved	R	0h	Reserved
3-2	FRAME_LP_OFF_THRES HOLD	RH/W	0h	Idle duration as a fraction of frame length until Frame-based Low Power state entered Default via OTP 0h = 1/32 1h = 1/16 2h = 1/8 3h = 1/4
1	IDLE_LP_EN	RH/W	1h	Enable response-based low power mode Default via OTP 0h = Not enabled 1h = Enabled
0	Reserved	R	0h	Reserved

### 10.1.16 BC\_CONTROL Register (Offset = B6h) [Reset = C0]

BC\_CONTROL is shown in [BC\\_CONTROL Register Field Descriptions](#).

Return to the [Summary Table](#).

**表 10-18. BC\_CONTROL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	i2c_ds_config	RH/W	3h	I2C open-drain output drive strength selection This is intended to be set through I2C. 0h $\approx$ 1mA (typical) 1h $\approx$ 2mA (typical) 2h $\approx$ 4mA (typical) 3h $\approx$ 8mA (typical) (default)

表 10-18. BC\_CONTROL Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
5-4	DEFAULT_STATE_BC_P1	RH/W	0h	Battery charger advertisement or detection selected for default state of eUSB2 repeater 0h = neither detect nor advertise charger 1h = detect charger starting when GPIO1 goes high. 2h = advertise short mode DCP. DCP is 1.2V if 1P2V_MODE is '1' else pure BC 1.2 DCP 3h = auto-cycle ACP3 to short mode DCP. Short mode passes through 1.2V DCP for 12 seconds prior to pure BC 1.2 DCP if 1P2V_MODE is '1'
3	VBUS_CONTROL_POLARITY	RH/W	0h	Select polarity of VBUS control output pin 0h = active high 1h = active low
2	1P2V_MODE_DIS	RH/W	0h	Disable advertising 1.2V mode in default state whether enabled to auto-cycle or not 0h = 1.2V mode enabled 1h = 1.2V mode disabled
1	INT_PIN_FUNCTION	RH/W	0h	Select function of GPIO2 pin in I2C mode 0h = INT (interrupt) 1h = CHG_DET (Charger Detected)
0	CHG_DET_POLARITY	RH/W	0h	Select polarity of CHG_DET I2C mode status output pin 0h = active low 1h = active high

**10.1.17 BC\_STATUS\_1 Register (Offset = B7h) [Reset = 00h]**

BC\_STATUS\_1 is shown in [BC\\_STATUS\\_1 Register Field Descriptions](#).

Return to the [Summary Table](#).

表 10-19. BC\_STATUS\_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	RH	0h	Reserved
6-4	CHARGER_TYPE_DET_P1	RH	0h	Type of battery charger detected on Port 1 0h = SDP – 500mA 1h = divider 0 – 500mA 2h = divider 1 – 1 A 3h = CDP – 1.5 A 4h = BC 1.2 DCP – 1.5 A 5h = 1.2V pullup and short – 2 A 6h = divider 2 – 2.1 A 7h = divider 3 – 2.4 A
3	Reserved	RH	0h	Reserved
2-0	Auto_DCP_STATE_P1	RH	0h	State of auto-DCP sequence on Port 1 0h = no advertisement 5h = divider 3 (2.4 A) 6h = 1.2V pullup and short 7h = BC 1.2 DCP

### 10.1.18 INT\_STATUS\_1 Register (Offset = A3h) [Reset = 00h]

INT\_STATUS\_1 is shown in [INT\\_STATUS\\_1 Register Field Descriptions](#).

Return to the [Summary Table](#).

**表 10-20. INT\_STATUS\_1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	INT_GPIO1_RISING_EDGE	R/W1C	0h	GPIO1 Rising Edge enable 0h = no interrupt 1h = interrupt
6	INT_GPIO1_FALLING_EDGE	R/W1C	0h	GPIO1 Falling Edge enable 0h = no interrupt 1h = interrupt
5	Reserved	R	0h	Reserved
4	Reserved	R	0h	Reserved
3	INT_USB_REMOTE_WAKE_P1	R/W1C	0h	Remote Wake Event Detect on USB Port 1 See <a href="#">セクション 8.4.6</a> 0h = no interrupt 1h = interrupt
2	INT_USB_DISCONNECT_P1	R/W1C	0h	Disconnect event has occurred on Port 1 See <a href="#">セクション 8.4.6</a> 0h = no interrupt 1h = interrupt
1-0	Reserved	R	0h	Reserved

### 10.1.19 INT\_STATUS\_2 Register (Offset = A4h) [Reset = 00h]

INT\_STATUS\_2 is shown in [INT\\_STATUS\\_2 Register Field Descriptions](#).

Return to the [Summary Table](#).

**表 10-21. INT\_STATUS\_2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	Reserved	R	0h	Reserved
5	INT_BC_CHG_DET_P1	R/W1C	0h	Detected battery charger on Port 1 0h = no interrupt 1h = interrupt
4	Reserved	R	0h	Reserved
3	INT_USB_DET_ATTACH_P1	R/W1C	0h	Device Attach event has occurred on Port 1 See <a href="#">セクション 8.4.7</a> 0h = no interrupt 1h = interrupt
2	Reserved	R	0h	Reserved
1	INT_USB_OVP_P1	R/W1C	0h	Over voltage condition has occurred (DP/DN) 0h = no interrupt 1h = interrupt
0	Reserved	R	0h	Reserved

### 10.1.20 CONFIG\_PORT1 Register (Offset = 60h) [Reset = 00h]

CONFIG\_PORT1 is shown in [CONFIG\\_PORT1 Register Field Descriptions](#).

Return to the [Summary Table](#).

表 10-22. CONFIG\_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R	0h	Reserved
4-3	HOST_DEVICE_P1	RH	0h	Port1 is configured as a Host repeater or a Device repeater 0h = not configured 1h = host repeater 2h = device repeater 3h = reserved
2-1	Reserved	R	0h	Reserved
0	CDP_2_STATUS_P1	RH	0h	Primary detection detected on port1 if CDP_2_EN_P1=1 0h = CDP primary detection detected 1h = CDP primary detection not detected

### 10.1.21 TEST\_MODE1 Register (Offset = F5h) [Reset = 3Xh]

TEST\_MODE1 is shown in [TEST\\_MODE1 Register Field Descriptions](#).

Return to the [Summary Table](#).

表 10-23. TEST\_MODE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R/W	0h	Reserved, make sure to rewrite what was read
3	FORCE_HS_L0	R/W	0h	Force repeater into high-speed L0 state for test purposes only. 0h = normal repeater mode (setting this bit to 0 does not return the device to normal repeater mode, the device required a hard reset, soft reset or power cycled) 1h = forced high-speed L0 mode
2-0	Reserved	R/W	Xh	Variant ID. 00h = 1.2V I/O 02h = 1.8V I/O Must not change the value, rewrite the value that is read.





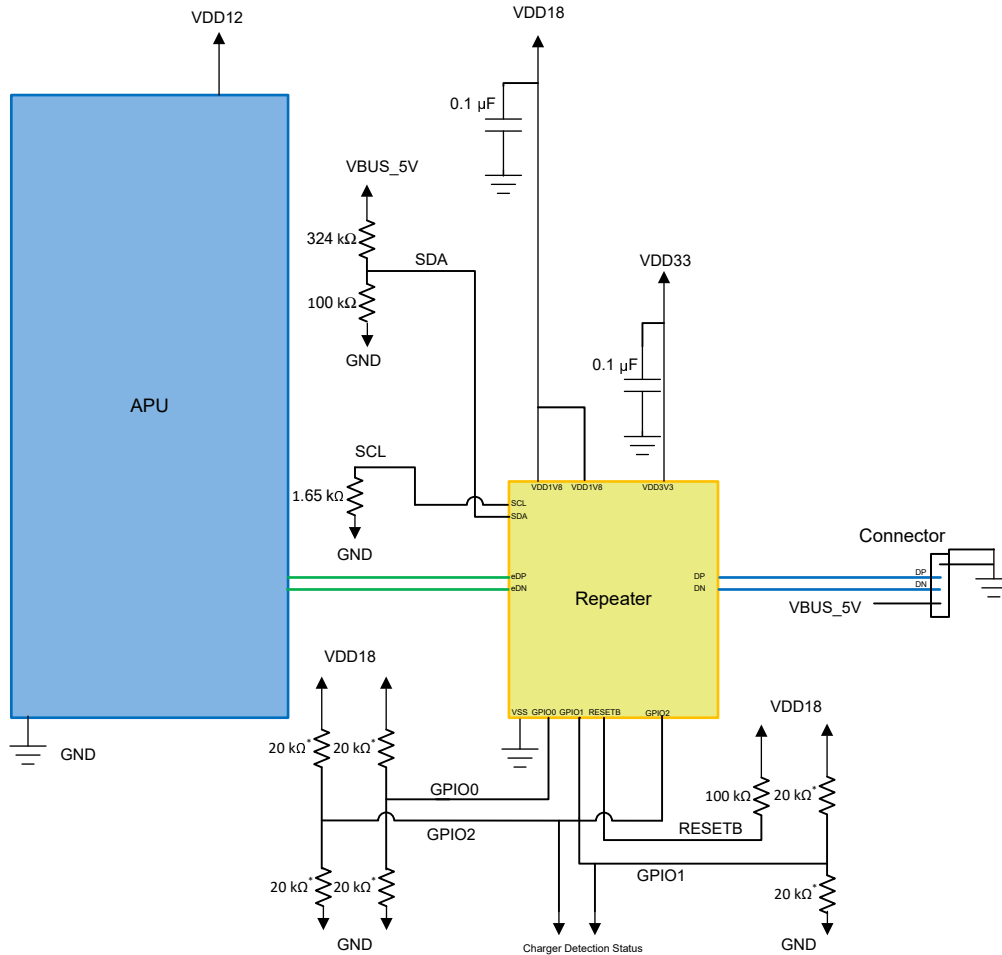


図 11-2. Typical System Implementation Using 1.8V Variant without I<sup>2</sup>C (Configured for Charger Detection)

The 0.1μF recommendation per supply pin is based on capacitor placement of 2 mm or less trace length away. If the placement of the capacitor is further away, then the value of the capacitor needs to be redetermined to account for the additional trace inductance and maintain resonance around 12MHz. Additionally, make sure the system power design has adequate bulk capacitance to account for maximum transient current expected by the device when transitioning from low power mode to active mode. GPIO2 can be optionally used as interrupt output. Select the pullup and pulldown resistors on GPIO[0:2] based on the USB PHY tuning needs. Use SDA for Vbus\_valid detection with a voltage divider. GPIO1 and GPIO2 can be routed as needed for charger detection status. Pull-down resistor value on SCL determines the battery charging mode.

### 11.2.1 Design Requirements

The TUSB2E11 requires a valid reset signal as described in the [Power Supply Recommendations](#) section.

For design examples, use the parameters shown in 表 11-1, 表 11-2, and 表 11-3.

表 11-1. Design Parameters for High Loss USB 2.0 System Using I<sup>2</sup>C

PARAMETER		VALUE <sup>(1)</sup>	
V <sub>DD3V3</sub>		3.3V ±10%	
V <sub>DD1V8</sub>		1.8V ±5%	
I <sup>2</sup> C support required in system (Yes or No)		Yes	
Parameter	Register	Setting	Value

表 11-1. Design Parameters for High Loss USB 2.0 System Using I<sup>2</sup>C (続き)

PARAMETER			VALUE <sup>(1)</sup>
USB 2.0 TX Swing (peak to peak)	U_TX_ADJUST_PORT1 (Offset = 70h)	7Ch	980mVp-p
USB 2.0 TX Pre-emphasis	U_HS_TX_PRE_EMPHASIS_P1 (Offset = 71h)	3Ch	2.1dB
USB 2.0 RX Equalization	U_RX_ADJUST_PORT1 (Offset = 72h)	92h	1.09dB
USB 2.0 HS host disconnect threshold (peak differential)	U_DISCONNECT_SQUELCH_PORT1 (Offset = 73h)	83h	685mV
USB 2.0 HS squelch/RX sensitivity threshold (peak differential)	U_DISCONNECT_SQUELCH_PORT1 (Offset = 73h)	83h	111mV

表 11-2. Design Parameters for Medium Loss USB 2.0 System Using I<sup>2</sup>C

PARAMETER			VALUE <sup>(1)</sup>
V <sub>DD3V3</sub>			3.3V ±10%
V <sub>DD1V8</sub>			1.8V ±5%
I <sup>2</sup> C support required in system (Yes or No)			Yes
Parameter	Register	Setting	Value
USB 2.0 TX Swing (peak to peak)	U_TX_ADJUST_PORT1 (Offset = 70h)	79h	920mVp-p
USB 2.0 TX Pre-emphasis	U_HS_TX_PRE_EMPHASIS_P1 (Offset = 71h)	39h	0.9dB
USB 2.0 RX Equalization	U_RX_ADJUST_PORT1 (Offset = 72h)	92h	1.09dB
USB 2.0 HS host disconnect threshold (peak differential)	U_DISCONNECT_SQUELCH_PORT1 (Offset = 73h)	83h	685mV
USB 2.0 HS squelch/RX sensitivity threshold (peak differential)	U_DISCONNECT_SQUELCH_PORT1 (Offset = 73h)	83h	111mV

(1) These parameters are starting values for a high loss system. Further tuning might be required based on specific loss profile and measurements.

表 11-3. Design Parameters for Medium Loss USB 2.0 System without I<sup>2</sup>C and Configured for Charger Detection

PARAMETER				VALUE <sup>(1)</sup>
V <sub>DD3V3</sub>				3.3V ±10%
V <sub>DD1V8</sub>				1.8V ±5%
I <sup>2</sup> C support required in system (Yes or No)				No
SCL (pulldown resistor to ground)				1.65kΩ
SDA (pulldown resistor to ground)				100kΩ
SDA (pullup resistor to VBUS5V)				324kΩ
Parameter	GPIO0	GPIO1	GPIO2	Value
USB 2.0 TX Swing (peak to peak)	Float	Pull-up	Pull-up	920mVp-p
USB 2.0 TX Pre-emphasis	Float	Pull-up	Pull-up	0.9dB
USB 2.0 RX Equalization	Float	Pull-up	Pull-up	1.09dB
USB 2.0 HS host disconnect threshold (peak differential)	Float	Pull-up	Pull-up	685mV
USB 2.0 HS squelch/RX sensitivity threshold (peak differential)	Float	Pull-up	Pull-up	98mV

(1) These parameters are starting values for a medium loss system. Further tuning might be required based on specific loss profile and measurements.



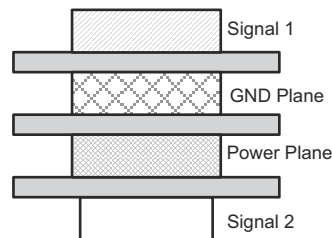
I<sup>2</sup>C/RAP and eUSB2 interfaces are ready after `tRH_READY` upon soft reset through the I<sup>2</sup>C.

Upon de-assertion of RESETB (after `tRH_READY`) or software reset (after `tRH_READY`), the TUSB2E11 enables and enters the default state. In the default state, the TUSB2E11 is ready to accept eUSB2 packets, RAP and I<sup>2</sup>C requests. The repeater can either be in host repeater mode or device repeater mode depending on the receipt of either host mode enable or peripheral mode enable.

## 11.4 Layout

### 11.4.1 Layout Guidelines

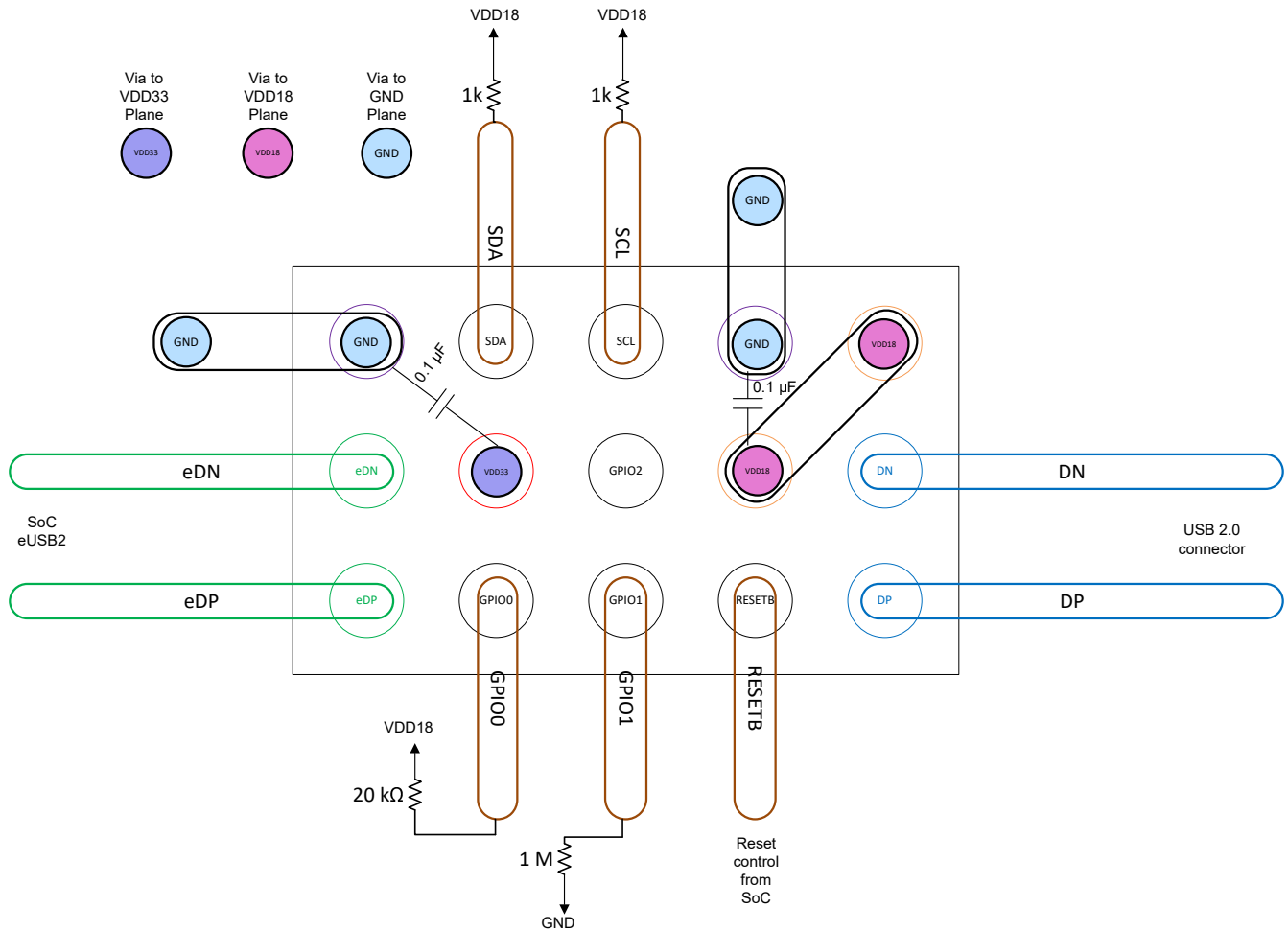
1. Place supply bypass capacitors as close to VDD1V8 and VDD3V3 pins as possible and avoid placing the bypass caps near the eDP/eDN and DP/DN traces.
2. Route the high-speed USB signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around the via to minimize the capacitance. Each via introduces discontinuities in the transmission line of the signal and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.
3. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.
4. Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.
5. Avoid stubs on the high-speed USB signals due to signal reflections. If a stub is unavoidable, then the stub must be less than 200 mil.
6. Route all high-speed USB signal traces over continuous GND planes, with no interruptions.
7. Avoid crossing over anti-etch, commonly found with plane splits.
8. Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in [Figure 11-5](#).



**Figure 11-5. Four-Layer Board Stack-Up**

### 11.4.2 Example Layout for Application with 1.8V I<sup>2</sup>C Variant

☒ 11-6 shows how GPIO2 can be optionally used as an open drain interrupt output with a pullup resistor to VDD18.



☒ 11-6. Example Layout for Application with 1.8V I<sup>2</sup>C Variant

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

### 12.2 Documentation Support

#### 12.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [High-Speed Interface Layout Guidelines application note](#)
- USB 2.0 Promoter Group (2000). [USB 2.0 Specification](#) USB 2.0 Promoter Group
- USB Implementers Forum (2018). [Embedded USB2 \(eUSB2\) Physical Layer Supplement to the USB Revision 2.0 Specification, Rev. 1.2](#) USB Implementers Forum

#### 12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

#### 12.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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#### 12.5 Trademarks

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#### 12.7 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 13 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (January 2024) to Revision D (April 2024)	Page
• Added section on Frame Based power mode.....	29
• Added section on Battery Charging.....	30

- Added offset 0xB5 to the register map..... 36
- 

#### Changes from Revision B (August 2023) to Revision C (January 2024) Page

- Changed I<sup>2</sup>C 7-bit target address from: 0x5E to: 0x3E..... 33
- 

#### Changes from Revision A (June 2022) to Revision B (August 2023) Page

- パッケージリード サイズを含めるよう「パッケージ情報」表を更新..... 1
  - Clarify ROC for RESETB..... 9
  - Updated register F5h to indicate OPN variants..... 36
- 

#### Changes from Revision \* (November 2021) to Revision A (June 2022) Page

- データシートの最初の公開リリース..... 1
- 

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB2E111YCGR	ACTIVE	DSBGA	YCG	15	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-20 to 85	T2E111A	<a href="#">Samples</a>
TUSB2E112YCGR	ACTIVE	DSBGA	YCG	15	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-20 to 85	T2E112	<a href="#">Samples</a>
TUSB2E112YCGT	ACTIVE	DSBGA	YCG	15	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-20 to 85	T2E112	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

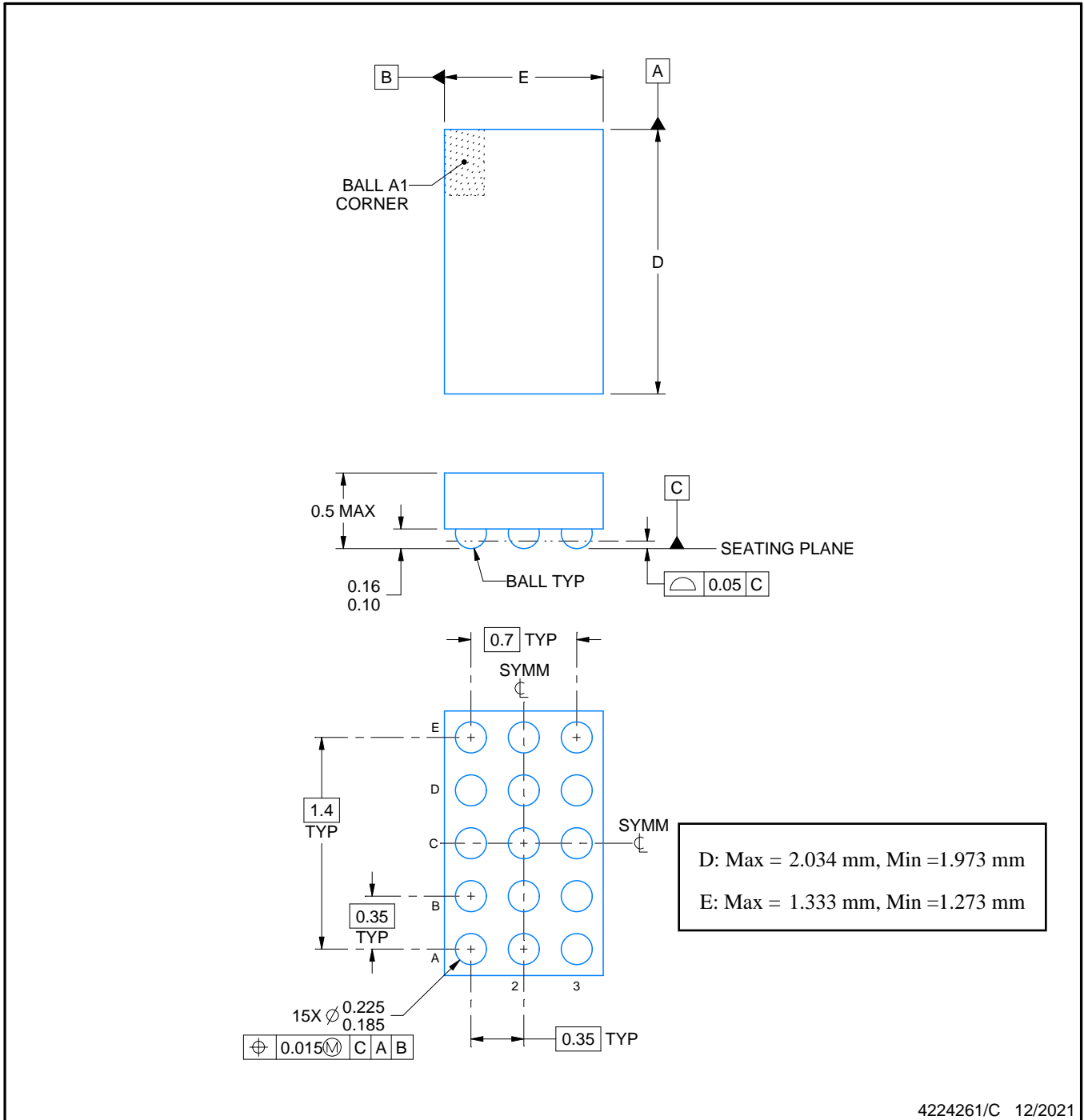
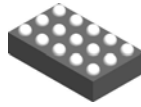

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB2E111YCGR	DSBGA	YCG	15	3000	180.0	8.4	1.42	2.16	0.65	4.0	8.0	Q1
TUSB2E112YCGR	DSBGA	YCG	15	3000	180.0	8.4	1.42	2.16	0.65	4.0	8.0	Q1
TUSB2E112YCGT	DSBGA	YCG	15	250	180.0	8.4	1.42	2.16	0.65	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB2E111YCGR	DSBGA	YCG	15	3000	182.0	182.0	20.0
TUSB2E112YCGR	DSBGA	YCG	15	3000	182.0	182.0	20.0
TUSB2E112YCGT	DSBGA	YCG	15	250	182.0	182.0	20.0



NOTES:

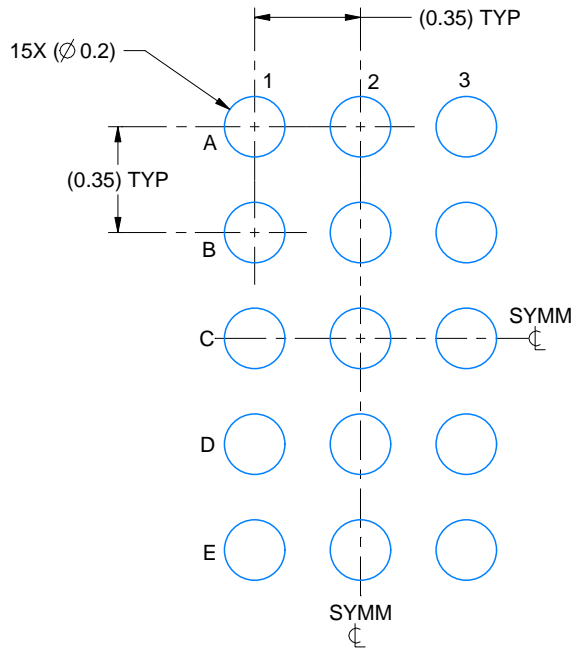
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

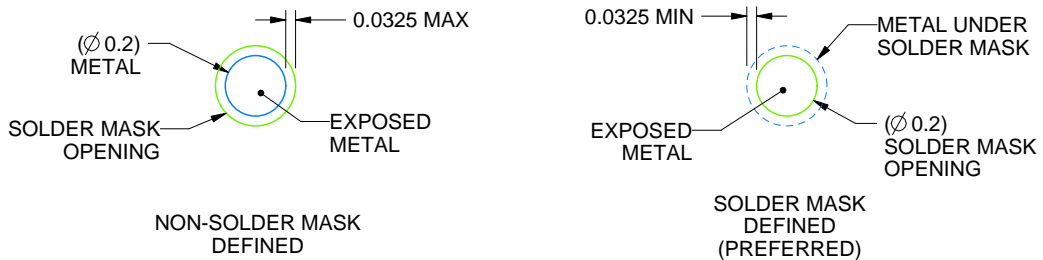
YCG0015

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 40X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

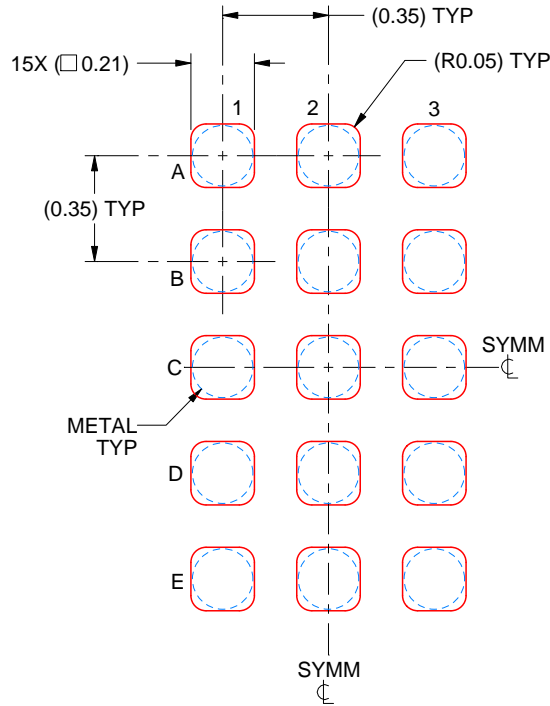
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YCG0015

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.075 mm THICK STENCIL  
SCALE: 40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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