TUSB2E221 USB 2.0-eUSB2 デュアル リピータ

1 特長

- USB 2.0 および eUSB2 (rev 1.2) 準拠
- ロースピード (LS)、フルスピード (FS)、ハイスピード (HS) をサポート
- クラス最高の高速合計ジッタ:20ps
- レジスタ アクセス プロトコル レセプタ対応
- 独立型デュアル リピータ
- 2:2 クロスバー マルチプレクサ (DSBGA パッケージのみ)
- ホスト モードおよびデバイス モード (DRD) をサポート
- VIOSEL ピンを使用して、1.2V～1.8V の制御または I^2C レベルを選択
- I^2C かストラップ ピンかを自動検出
  - USB 2.0 ハイスピード チャネル補償設定用の 3 本のストラップ ピン
  - I^2C デバイス インターフェイスを使用すると、より柔軟な設定が可能
- さまざまなデバイス バリアントを用意
  - eUSB2 1.0V または 1.2V 信号インターフェイス
  - 4 つの eUSB2 トレース損失補償レベルで多様な製品フォーム ファクタに対応:2.5、5、7.5、10 インチ
- 自動再開 ECR と L2 割り込み再開モードをサポート
- CTA-936 USB Carkit UART のサポート
- オプションの BC1.2 CDP バッテリ充電および検出サポート
- デバッグ用 EQ ピンのオプションの GPIO モードと、EQ0/1 経由の I^2C ↔ GPIO
- I^2C からアクセスできる製造試験用のデバッグ機能

2 アプリケーション

- 通信機器
- エンタープライズ システム
- ノート PC およびデスクトップ PC
- 産業用
- タブレット
- ポータブル エレクトロニクス

3 概要

TUSB2E221 は、低電圧プロセスを使用する新しいプロセッサに USB 2.0 準拠ポートを実装できます。

TUSB2E221 は、デバイス モードとホスト モードの両方をサポートする USB の eUSB2-USB 2.0 リピータです。TUSB2E221 は、USB ロースピード (LS) 信号、フルスピード (FS) 信号、ハイスピード (HS) 信号をサポートしています。

TUSB2E221 は、1.2V のシングルエンド信号で動作する eUSB2 eDSPr または eUSPr と接続するように設計されています。

TUSB2E221 は、堅牢な相互運用性、最適な性能、消費電力を実現するために、特許申請中の複数の設計を採用しています。

I^2C インターフェイスを使用しないシステムでは、このデバイスは最大 17.5Ω の USB 2.0 チャネル等価直列抵抗 (ESR) に対応する 3 本のストラップ ピンによる 8 つの個別設定を提供します。このデバイスは、最大 10 インチまでのさまざまなレベルの eUSB2 トレース長補償機能を備えるバリアントが利用可能です。

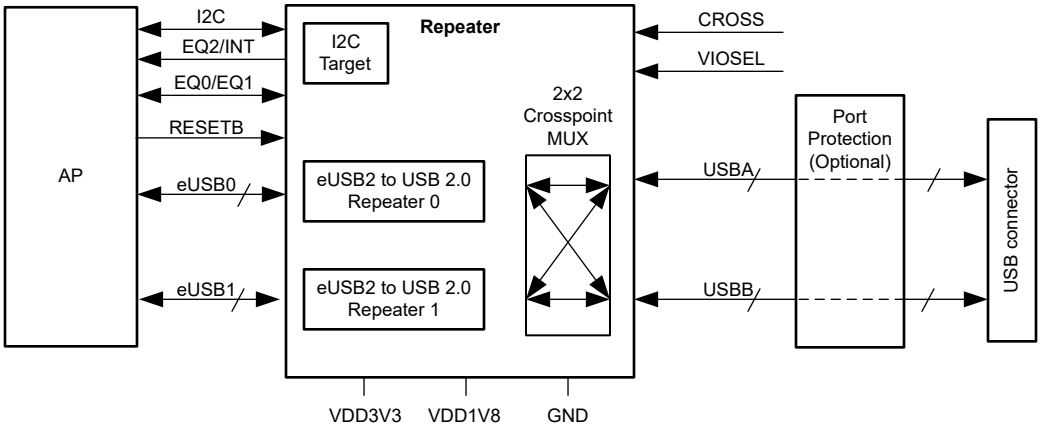
I^2C インターフェイスにより、さらに柔軟にデバイスの RX および TX 設定を微調整できます。利用可能な設定は、RX イコライゼーション、RX スケルチ スレッショルド、RX 切断スレッショルド、TX 振幅、TX スルーレート、TX プリエンファシスです。

各種のデバッグ オプションが利用可能であり、3 本の EQ ピンを使用してさまざまな USB バス状態や割り込みを監視するように構成できるほか、CTA-936 UART モード制御で SoC デバッグ機能を実現できます。EQ0 および EQ1 は、汎用 I^2C から GPIO へのブリッジとして使用できます。

パッケージ情報

部品番号	パッケージ(1)	パッケージ サイズ(2)
TUSB2E221	VBW (WQFN、20)(3)	3mm × 3mm
	YCG (DSBGA、25)	2mm × 2mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
(3) このパッケージはプレビューのみです。



概略回路図

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4 Device Variants

The following table describes the key differences between the TUSB2E221x device variants

表 4-1. Device Variant Information

Orderable Device	Package Type	Package Drawing	Register Map Default	7-bit I²C Address	eUSB2 LS/FS Voltage	Device Marking
TUSB2E221	WCSP	YCG	CAT2	0x4F	1.2V	2E221W2
TUSB2E221	WQFN	VBW	CAT2	0x4F	1.2V	2E221V2

For more information and availability of device variants such as eUSB2 1.0V signaling interface, different 7-bit I2C addresses, and lower power internal embedded applications, see *サポート・リソース*.

表 4-2. Register Map Defaults

I2C Offset	CAT2
0x30	0x79
0x31	0x39
0x32	0xD4
0x33	0x75
0x37	0x40
0x38	0x4C
0x39	0x22
0x10	0x50
0x70	0x79
0x71	0x39
0x72	0x94
0x73	0x75
0x77	0x40
0x78	0x4C
0x79	0x22
0x50	0x50

5 Pin Configuration and Functions

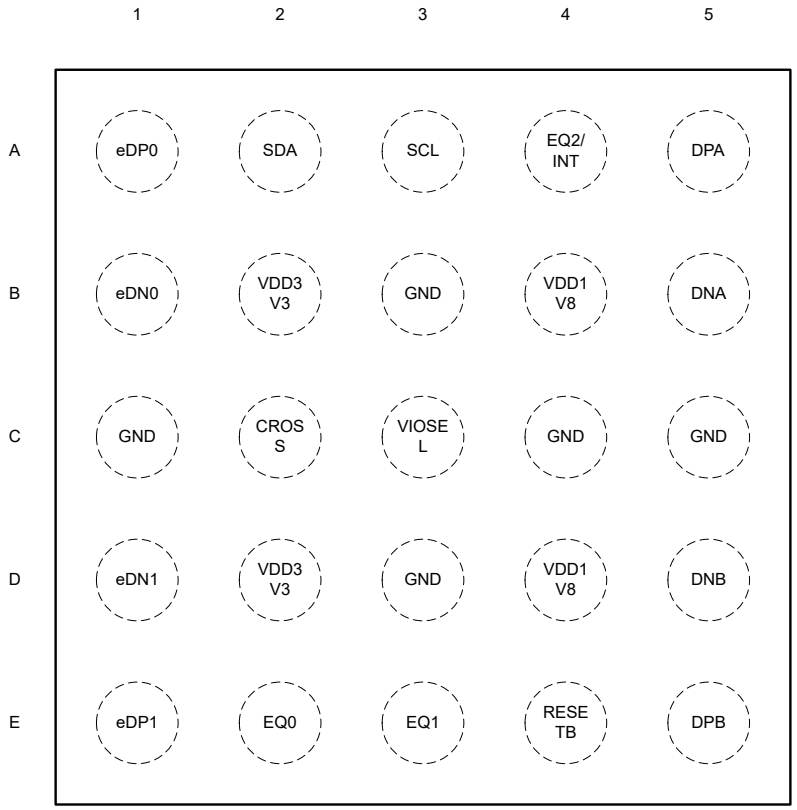


図 5-1. YCG Package, 25-Pin DSBGA (Top View)

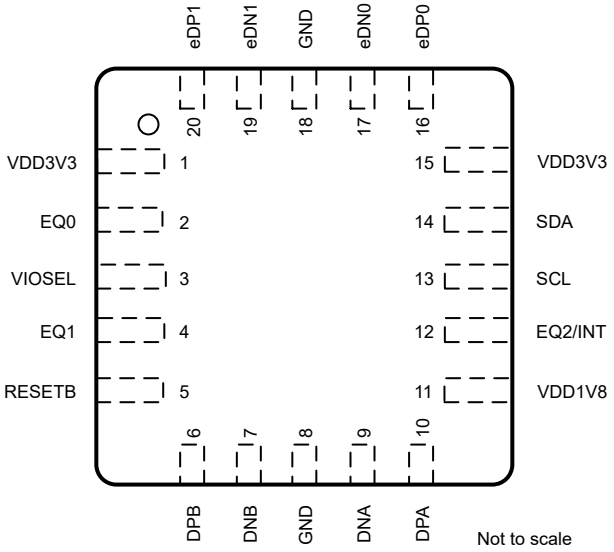


図 5-2. VBW Package 20-Pin WQFN(1) (Top View)

表 5-1. Pin Functions

PIN			I/O	RESET STATE	ASSOCIATED ESD SUPPLY	DESCRIPTION
NAME	VBW[1]	YCG				
CROSS	–	C2	Digital Input	N/A	VDD3V3	Indicates mux orientation. Used to specify orientation of internal Crossbar switch CROSS = Low: eUSB0 «–» USBA and eUSB1 «–» USBB CROSS = High: eUSB0 «–» USBB and eUSB1«–» USBA Sampled at deassertion of RESETB
DNA	9	B5	Analog I/O	Hi-Z	VDD3V3	USB port A D- pin
DPA	10	A5	Analog I/O	Hi-Z	VDD3V3	USB port A D+ pin
DNB	7	D5	Analog I/O	Hi-Z	VDD3V3	USB port B D- pin
DPB	6	E5	Analog I/O	Hi-Z	VDD3V3	USB port B D+ pin
eDN0	17	B1	Analog I/O	Hi-Z	VDD1V8	eUSB2 port 0 D- pin
eDP0	16	A1	Analog I/O	Hi-Z	VDD1V8	eUSB2 port 0 D+ pin
eDN1	19	D1	Analog I/O	Hi-Z	VDD1V8	eUSB2 port 1 D- pin
eDP1	20	E1	Analog I/O	Hi-Z	VDD1V8	eUSB2 port 1 D+ pin
EQ0	2	E2	Digital I/O	Internal pulldown 1MΩ typical (disabled after reset)	VDD3V3	(See 表 5-2)
EQ1	4	E3	Digital I/O	Internal pulldown 1MΩ typical (disabled after reset)	VDD3V3	(See 表 5-2)
EQ2/INT	12	A4	Digital I/O	Internal pulldown 1MΩ typical (disabled after reset)	VDD3V3	I^2C Mode: Open Drain active low level sensitive interrupt output to system non-I^2C Mode: (See 表 5-2)
GND	8	B3	GND	N/A	N/A	GND
		C1				
		C4				
	18	C5				
		D3				
RESETB	5	E4	Digital Input	N/A	VDD1V8	Active Low Reset. After the RESETB deassertion, both repeaters will be enabled and be in eUSB2 default mode awaiting configuration from eDSPr or eUSPr.
SCL	13	A3	Digital I/O	Internal pulldown 1MΩ typical (disabled after reset)	VDD3V3	I^2 clock Open drain I/O.
SDA	14	A2	Digital I/O	Internal pulldown 1MΩ typical (disabled after reset)	VDD3V3	Bidirectional I^2C data. Open drain I/O. Pulled up to I^2C rail through an external resistor

Device Mode Matrix (See 表 5-2)

SCL	SDA	Mode
Low	Low	Non-I^2C USB Repeater (See 表 5-3)
Low	High	Non-I^2C USB Repeater (See 表 5-3) BC 1.2 CDP advertising enabled in host mode
High	Low	Non-I^2C USB Repeater (See 表 5-5)
High	High	I^2C Enabled

表 5-1. Pin Functions (続き)

PIN			I/O	RESET STATE	ASSOCIATED ESD SUPPLY	DESCRIPTION
NAME	VBW[1]	YCG				
VDD1V8	11	B4 D4	PWR	N/A	N/A	1.8V analog supply voltage
VDD3V3	1 15	B2 D2	PWR	N/A	N/A	3.3V supply voltage
VIOSEL	3	C3	Digital Input	N/A	VDD3V3	VIOSEL is used to select digital I/O input voltage for GPIOs, CROSS and I^2C VIOSEL = VSS sets device into 1.2V I/O mode VIOSEL = VDD1V8 sets device into 1.8V I/O mode VIOSEL pin is real time control and not only latched at powered on reset. Be careful when this pin changes dynamically after power-on-reset because the output voltage may change from 1.2V to 1.8V.

(1) The VBW (WQFN) package is preview only.

表 5-2. Device Mode Configuration

SCL	SDA	EQ0	EQ1	EQ2	eUSB0	eUSB1	I2C Interface	USBA and USBB CDP advertising in host mode
Low/Float	Low/Float	USB2 PHY Configuration			USB repeater	USB repeater	Disabled	Disabled
Low/Float	High	USB2 PHY Configuration			USB repeater	USB repeater	Disabled	Enabled
High	Low/Float	eUSB PHY Configuration		High-Z	USB repeater	USB repeater	Disabled	Disabled
High	High	Low/Float	Low/Float	INT interrupt output	USB repeater	USB repeater	Enabled	Per register
High	High	High	Low/Float	INT interrupt output	Carkit UART bypass	USB repeater	Enabled	Per register
High	High	Low/Float	High	INT interrupt output	USB repeater	Carkit UART bypass	Enabled	Per register
High	High	High	High	INT interrupt output	Carkit UART bypass	Carkit UART bypass	Enabled	Per register

The eUSB phy configurations used 表 5-3 assumes the channel between the device and host is 5 inches FR4.

表 5-3. USB2 PHY Configuration

EQ0	EQ1	EQ2	USB2 PHY Compensation Level	eUSB0/1 channel	USB ESR[1] (Ω)
Low/Float	Low/Float	Low/Float	Level 0	5 inches FR4	USB A: 2.5 USB B: 2.5
High	Low/Float	Low/Float	Level 1	5 inches FR4	USB A: 10 USB B: 10
Low/Float	High	Low/Float	Level 2	5 inches FR4	USB A: 17.5 USB B: 17.5
High	High	Low/Float	Level 3	5 inches FR4	USB A: 10 USB B: 17.5
Low/Float	Low/Float	High	Level 4	5 inches FR4	USB A: 2.5 USB B: 10
High	Low/Float	High	Level 5	5 inches FR4	USB A: 10 USB B: 2.5
Low/Float	High	High	Level 6	5 inches FR4	USB A: 17.5 USB B: 2.5

表 5-3. USB2 PHY Configuration (続き)

EQ0	EQ1	EQ2	USB2 PHY Compensation Level	eUSB0/1 channel	USB ESR(1) (Ω)
High	High	High	Level 7	5 inches FR4	USB A: 2.5 USB B: 17.5

(1) Equivalent series resistance (ESR) is the combination of any resistance between the device and the USB connector such as switches, multipliexers, just to name a few.

表 5-4. USB2 PHY Compensation Levels

	USB2 PHY Compensation Levels							
Register	Level 0	Level 1	Level 2	Level 3	Level 4	Level 5	Level 6	Level 7
E_EQ_Px	Register Default	Register Default	Register Default	Register Default	Register Default	Register Default	Register Default	Register Default
E_HS_TX_AMPLITUDE_Px	Register Default	Register Default	Register Default	Register Default	Register Default	Register Default	Register Default	Register Default
E_HS_TX_PRE_EMPHASIS_Px	Register Default	Register Default	Register Default	Register Default	Register Default	Register Default	Register Default	Register Default
U_EQ_Px	USB A: 0x0 USB B: 0x0	USB A: 0x2 USB B: 0x2	USB A: 0x5 USB B: 0x5	USB A: 0x5 USB B: 0x2	USB A: 0x2 USB B: 0x0	USB A: 0x0 USB B: 0x2	USB A: 0x0 USB B: 0x5	USB A: 0x5 USB B: 0x0
U_SQUELCH_THRESHOLD_Px	USB A: 0x4 USB B: 0x4	USB A: 0x5 USB B: 0x5	USB A: 0x6 USB B: 0x6	USB A: 0x6 USB B: 0x5	USB A: 0x5 USB B: 0x4	USB A: 0x4 USB B: 0x5	USB A: 0x4 USB B: 0x6	USB A: 0x6 USB B: 0x4
U_DISCONNECT_THRESHOLD_Px	USB A: 0x5 USB B: 0x5	USB A: 0x8 USB B: 0x8	USB A: 0x8 USB B: 0x8	USB A: 0x8 USB B: 0x8	USB A: 0x8 USB B: 0x5	USB A: 0x5 USB B: 0x8	USB A: 0x5 USB B: 0x8	USB A: 0x8 USB B: 0x5
U_HS_TX_AMPLITUDE_Px	USB A: 0x5 USB B: 0x5	USB A: 0x9 USB B: 0x9	USB A: 0xD USB B: 0xD	USB A: 0xD USB B: 0x9	USB A: 0x9 USB B: 0x5	USB A: 0x5 USB B: 0x9	USB A: 0x5 USB B: 0xD	USB A: 0xD USB B: 0x5
U_HS_TX_PRE_EMPHASIS_Px	USB A: 0x0 USB B: 0x0	USB A: 0x1 USB B: 0x1	USB A: 0x3 USB B: 0x3	USB A: 0x3 USB B: 0x1	USB A: 0x1 USB B: 0x0	USB A: 0x0 USB B: 0x1	USB A: 0x0 USB B: 0x3	USB A: 0x3 USB B: 0x0

表 5-5. eUSB PHY Configuration

EQ0	EQ1	EQ2	eUSB PHY Compensation Level	eUSB0 ESR(1) (Ω)	eUSB1 ESR (1) (Ω)	USBA (DPA/DNA) ESR (1) (Ω)	USBB (DPB/DNB) ESR (1) (Ω)
Low/Float	Low/Float	Low/Float	Level 0	2.5	2.5	2.5	2.5
High	Low/Float	Low/Float	Level 1	7.5	7.5	2.5	2.5
Low/Float	High	Low/Float	Level 2	15	15	2.5	2.5
High	High	Low/Float	Level 3	25	25	2.5	2.5

(1) Equivalent series resistance (ESR) is the combination of any resistance between the device and the USB connector or between device and the SOC such as switches, multipliexers, just to name a few.

表 5-6. eUSB PHY Compensation Levels

	eUSB PHY Compensation Levels			
Register	Level 0	Level 1	Level 2	Level 3
E_EQ_Px	0x1	0x3	0x7	0x10
E_HS_TX_AMPLITUDE_Px	0x3	0x3	0x5	0x7
E_HS_TX_PRE_EMPHASIS_Px	0x1	0x2	0x4	0x6
U_EQ_Px	Register Default	Register Default	Register Default	Register Default
U_SQUELCH_THRESHOLD_Px	Register Default	Register Default	Register Default	Register Default
U_DISCONNECT_THRESHOLD_Px	Register Default	Register Default	Register Default	Register Default
U_HS_TX_AMPLITUDE_Px	Register Default	Register Default	Register Default	Register Default
U_HS_TX_PRE_EMPHASIS_Px	Register Default	Register Default	Register Default	Register Default

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range	V_{DD3V3}	–0.3	4.32	V
Analog Supply voltage range	V_{DD1V8}	–0.3	2.1	V
Voltage range	DPA, DNA, DPB, DNB (with OVP enabled), 1000 total number of short events and cumulative duration of 1000 hrs.	–0.3	6	V
Voltage range	eDP0, eDN0, eDP1, eDN1	–0.3	1.6	V
Voltage range	CROSS, RESETB, EQ0, EQ1, SCL, SDA, EQ2/INT, VIOSEL	–0.3	2.1	V
Junction temperature	$T_{J(max)}$		125	°C
Storage temperature	T_{stg}	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD3V3}	Supply voltage (VDD3V3)	3.0	3.3	3.6	V
V_{DD1V8}	Analog Supply voltage (VDD1V8)	1.62	1.8	1.98	V
$V_{\_I2C\_Pullup}$	I2C and GPIO open-drain bus voltage (1.2V mode), VIOSEL=VSS	1.08	1.2	1.32	V
$V_{\_I2C\_Pullup}$	I2C and GPIO open-drain bus voltage (1.8V mode), VIOSEL=VDD1V8	1.62	1.8	1.98	V
T_A	Operating free-air temperature	–40		85	°C
T_J	Junction temperature	–40		105	°C
T_{CASE}	Case temperature	–40		105	°C
T_{PCB}	PCB temperature (1mm away from the device)	–40		92	°C

6.4 Thermal Information

THERMAL METRIC(1)		TUSB2E221 VBW (WQFN) 20 PINS	TUSB2E221 YCG (DSBGA) 25 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	71.9	73.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.9	0.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.7	18.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	30.9	18.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
$P_{WC\_1\_1V8}$	Absolute worst case power consumption - One Repeater (VDD1V8 only)	VIOSEL is high or low, I2C interface active, GPIOs in output mode, one repeater is disable and one repeater in HS mode with USB transmitting, maximum RX EQ, TX VOD and PE settings, maximum transition density.			275	mW
$P_{WC\_1\_3V3}$	Absolute worst case power consumption - One Repeater (VDD3V3 only)	VIOSEL is high or low, I2C interface active, GPIOs in output mode, one repeater is disable and one repeater in HS mode with USB transmitting, maximum RX EQ, TX VOD and PE settings, maximum transition density.			25	mW
$P_{WC\_2\_1V8}$	Absolute worst case power consumption - Two Repeaters (VDD1V8 only)	VIOSEL is high or low, I2C interface active, GPIOs in output mode, both repeaters in HS mode with USB transmitting, maximum RX EQ, TX VOD and PE settings, maximum transition density.			550	mW
$P_{WC\_2\_3V3}$	Absolute worst case power consumption - Two Repeaters (VDD3V3 only)	VIOSEL is high or low, I2C interface active, GPIOs in output mode, both repeaters in HS mode with USB transmitting, maximum RX EQ, TX VOD and PE settings, maximum transition density.			50	mW
$P_{HS\_IOC\_1}$	USB Audio ISOC High -Speed - one repeater only	Maximum TX Vod/Maximum TX PE for both USB and eUSB2. Averaged over 8ms and only 1uFrame with data packet. Toffthreshold = 1/32. Host Peripheral mode. Frame Based Low power mode enabled			70	mW
$P_{HS\_IDLE\_LP\_1}$	High Speed Idle (Host Mode) - one repeater	L0.Idle. T_A = 85°C. (Typical at 25°C). Default PHY tuning settings for eUSB2 and USB. Frame based and response based low power mode enabled		26	70	mW
$P_{HS\_IDLE\_LP\_1}$	High Speed Idle (Peripheral Mode) - one repeater	L0.Idle. T_A = 85°C. (Typical at 25°C). Default PHY tuning settings for eUSB2 and USB. Frame based low power mode disabled and response based low power mode enabled		108	200	mW
P_{PD}	Powered down	Device powered, RESETB=Low, T_A=25°C, (DP/DN Voltage ≤ VDD3V3).			10	µW

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_{Disabled}$	Disabled	Device powered, I2C/GPIO interfaces functional but idle, both repeaters are disabled put into their lowest power state and non-functional. T_A=25°C, (DP/DN Voltage ≤ VDD3V3).			100	µW
P_{Detach_1}	USB unconnected - One Repeater	I2C/GPIO interfaces idle, one repeater is disabled and one repeater is connected to a eUSB PHY and waiting for a USB attach event. T_A = 25°C, (DP/DN Voltage ≤ VDD3V3)			100	µW
P_{Detach_2}	USB unconnected - Two Repeater	I2C/GPIO interfaces idle, both repeaters connected to a eUSB PHY and waiting for a USB attach event. T_A = 25°C, (DP/DN Voltage ≤ VDD3V3)			150	µW
$P_{Suspend\_2}$	L2 Suspend	I2C/GPIO interfaces idle, USB link is in L2, both repeaters monitoring for a resume/remote wake event. T_A = 25°C, (DP/DN Voltage ≤ VDD3V3)			150	µW
P_{Sleep_2}	L1 Sleep P_{sleep_2}	I2C/GPIO interfaces idle, both repeaters are supporting a USB connection, USB link is in L1, both repeaters monitoring for a L1 exit event. T_A = 25°C, (DP/DN Voltage ≤ VDD3V3)			6	mW
$P_{LS\_Active\_1}$	Low Speed Active - One Repeater	I2C/GPIO interfaces idle, one repeater is disabled, other repeater in LS mode, maximum transition density. T_A = 85°C.			52	mW
$P_{FS\_Active\_1}$	Full Speed Active - One Repeater	I2C/GPIO interfaces idle, one repeater is disabled, one repeater in FS mode, maximum transition density. T_A = 85°C.			52	mW
$P_{FS\_Active\_2}$	Full Speed Active - Two Repeater	I2C/GPIO interfaces idle, Both repeaters in FS mode, maximum transition density. T_A = 85°C.			68	mW
DIGITAL INPUTS						
V_{IH}	High level input voltage	CROSS, EQ0, EQ1 (1.2V input mode, VIOSEL=VSS)	0.702			V
V_{IH}	High level input voltage	CROSS, EQ0, EQ1 (1.8V input mode, VIOSEL=VDD1V8)	1.053			V
V_{IL}	Low-level input voltage	CROSS, EQ0, EQ1 (1.2V input mode, VIOSEL=VSS)			0.462	V
V_{IL}	Low-level input voltage	CROSS, EQ0, EQ1 (1.8V input mode, VIOSEL=VDD1V8)			0.693	V
V_{IL}	Low-level input voltage	VIOSEL (1.8V input)			0.613	V
V_{IH}	High level input voltage	VIOSEL (1.8V input)	1.053			V
V_{IL}	Low-level input voltage	RESETB (1.2V or 1.8V input mode)			0.35	V
V_{IH}	High level input voltage	RESETB (1.2V or 1.8V input mode)	0.75			V
I_{IH}	High level input current	V_{IH} = 1.98V, VDD3V3=3.0V or 0V, VDD1V8=1.62V or 0V CROSS, RESETB, EQ0, EQ1			0.5	µA
I_{IL}	Low level input current	V_{IL} = 0V, VDD3V3=3.0V or 0V, VDD1V8=1.62V or 0V CROSS, RESETB, EQ0, EQ1			0.5	µA
DIGITAL OUTPUTS						
V_{OH}	High level output voltage	EQ0, EQ11, EQ2/INT, push-pull I/O mode (I_{OH} = 20µA and maximum 3pF C_{load}) (1.2V output mode)	0.81			V

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	EQ0, EQ1, EQ2/INT, push-pull I/O mode (I_{OH} = 20µA and maximum 3pF C_{load}) (1.8V output mode)	1.21			V
V_{OL}	Low level output voltage	EQ0, EQ1, EQ2/INT, push-pull I/O mode (I_{OL} = 1mA) (1.2V output mode)			0.25	V
V_{OL}	Low level output voltage	EQ0, EQ1, EQ2/INT, push-pull I/O mode (I_{OL} = 1mA) (1.8V output mode)			0.35	V
I_{OL_PP}	Low level output current in push-pull mode	EQ0, EQ1, EQ2/INT (1.2V mode) VIOSEL=GND, VOL=0.4	2.5	4	6	mA
I_{OL_PP}	Low level output current in push-pull mode	EQ0, EQ1, EQ2/INT (1.8V mode) VIOSEL=VDD1V8, VOL=0.4	4	6	8	mA
I_{OH_PP}	High level output current in push-pull mode	EQ0, EQ1, EQ2/INT, push-pull I/O mode (1.2V output mode) VIOSEL=GND	22			µA
I_{OH_PP}	High level output current in push-pull mode	EQ0, EQ1, EQ2/INT, push-pull I/O mode (1.8V output mode) VIOSEL=VDD1V8	50			µA
I_{OL}	Output current in open-drain mode	EQ0, EQ1, EQ2/INT, VOL=0.4V, VIOSEL=VDD1V8, 1.8V mode	4	10	16	mA
I_{OL}	Output current in open-drain mode	EQ0, EQ1, EQ2/INT, VOL=0.4V, VIOSEL=GND, 1.2V mode	4	9.2	16	mA
I2C (SDA, SCL)						
V_{IL}	Low level input voltage, VIOSEL=VSS	SDA, SCL, $V_{\_I2C\_Pullup}$ = 1.08V to 1.32V			0.387	V
V_{IL}	Low level input voltage, VIOSEL=VDD1V8	SDA, SCL, $V_{\_I2C\_Pullup}$ = 1.62V to 1.96V			0.588	V
V_{IH}	High level output voltage, VIOSEL=VSS	SDA, SCL, $V_{\_I2C\_Pullup}$ = 1.08V to 1.32V	0.833			V
V_{IH}	High level output voltage, VIOSEL=VDD1V8	SDA, SCL, $V_{\_I2C\_Pullup}$ = 1.62V to 1.98V	1.372			V
V_{HYS}	Input hysteresis, VIOSEL=VSS	$V_{\_I2C\_Pullup}$ = 1.08V to 1.32V	0.020			V
V_{HYS}	Input hysteresis, VIOSEL=VDD1V8	$V_{\_I2C\_Pullup}$ = 1.62V to 1.98V	0.098			V
I_{IH}	High level input leakage current	V_{IH} = 1.98V			0.5	µA
I_{IL}	Low level input leakage current	V_{IL} = 0V			0.5	µA
I_{OL}	Open-drain drive strength	VOL = 0.4V, VIOSEL = VDD1V8, 1.8V mode	8	10	12.6	mA
I_{OL}	Open-drain drive strength	VOL = 0.4V, VIOSEL= GND, 1.2V mode	6.8	9	11.9	mA
USBA (DPA, DNA), USBB (DPB, DNB)						
Z_{inp_Dx}	Impedance to GND, no pull up/down	Vin=3.6V, V_{DD3V3}=3.0V USB 2.0 Spec Section 7.1.6 (1)	390			kΩ
C_{IO_Dx}	Capacitance to GND	Measured with VNA at 240MHz, Driver Hi-Z			10	pF
R_{PUI}	Bus pull-up resistor on upstream facing port (idle)	USB 2.0 Spec Section 7.1.5 (1)	0.92	1.1	1.475	kΩ
R_{PUR}	Bus pull-up resistor on upstream facing port (receiving)	USB 2.0 Spec Section 7.1.5 (1)	1.525	2.2	2.99	kΩ
R_{PD}	Bus pull-down resistor on downstream facing port	USB 2.0 Spec Section 7.1.5 (1)	14.35	19	24.6	kΩ
V_{HSTERM}	Termination voltage in high speed	USB 2.0 Spec Section 7.1.6.2 (1), The output voltage in the high-speed idle state	–10		10	mV
USB TERMINATION						
Z_{HSTERM_P}	Driver output resistance (which also serves as high speed termination)	(VOH= 0 to 600mV) USB 2.0 Spec Section 7.1.1.1 (1), Default, U_HS_TERM_Px Setting 01	40.6	45	49.4	Ω

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_{HSTERM_N}	Driver output resistance (which also serves as high speed termination)	(VOH= 0 to 600mV) USB 2.0 Spec Section 7.1.1.1 (1), Default, U_HS_TERM_Px Setting 01	40.6	45	49.4	Ω
USBA, USBB INPUT LEVELS LS/FS						
V_{IH}	High (driven)	USB 2.0 Spec Section 7.1.4 (1) (measured at connector)	2			V
V_{IHZ}	High (floating)	USB 2.0 Spec Section 7.1.4 (1) (HOST downstream port pull down resistor enabled and external device pull up 1.5kΩ +/-5% to 3.0V to 3.6V).	2.7		3.6	V
V_{IL}	Low	USB 2.0 Spec Section 7.1.4 (1)			0.8	V
V_{DI}	Differential input sensitivity (hysteresis is off)	|(D+)-(D-)|; USB 2.0 Spec Figure 7-19 (1); (measured at connector) V_{CM}=0.8V to 2.0V			0.2	V
USBA, USBB OUTPUT LEVELS LS/FS						
V_{OL}	Low	USB 2.0 Spec Section 7.1.1 (1), (measured at connector with RL of 1.425kΩ to 3.6V.)	0		0.3	V
V_{OH}	High (Driven)	USB 2.0 Spec Section 7.1.1 (1) (measured at connector with RL of 14.25kΩ to GND.)	2.8		3.6	V
Z_{FSTERM}	Driver series output resistance	USB 2.0 Spec Section 7.1.1 (1), Measured it during VOL or VOH	28		46	Ω
V_{CRS2}	Output signal crossover voltage	Measured as in USB 2.0 Spec Section 7.1.1 Figure 7-8 (1); Excluding the first transition from the Idle state. With external 1.5kΩ pullup on DP to 3.0V	1.3		2	V
V_{CRS}	Output signal crossover voltage	Measured as in USB 2.0 Spec Section 7.1.1 Figure 7-8 (1); Excluding the first transition from the Idle state	1.3		2	V
USBA, USBB INPUT LEVELS HS						
V_{HSSQ}	High-speed squelch/no-squelch detection threshold	USB 2.0 Spec Section 7.1.7.2 (specification refers to peak differential signal amplitude) (1), measured at 240MHz with increasing amplitude, U_SQUELCH_THRESHOLD_Px Setting 100, V_{CM} = –50mV to 500mV	104	126	150	mV
V_{HSDSC}	High speed disconnect detection threshold	USB 2.0 Spec Section 7.1.7.2 (specification refers to differential signal amplitude) (1). (+22.4%), U_DISCONNECT_THRESHOLD_Px Setting 0111, V_{CM} = 367mV to 770mV	697	732	760	mV
$EQ_{\_UHS}$	USB high-speed data receiver equalization, (measured indirectly through jitter)	240MHz, U_EQ_Px Setting 010	0.62	1.09	1.57	dB
USBA, USBB OUTPUT LEVELS HS						
V_{HSOD}	High-speed data signaling swing	Measured p-p, 10%, U_HS_TX_AMPLITUDE_Px Setting 0111, PE disabled,Test load is an ideal 45ohm to GND on DP and DN.	792	880	968	mV
V_{HSOL}	High-speed data signaling low, driver is off termination is on (measured single ended)	USB 2.0 Spec Section 7.1.7.2 (1), PE disabled, Test load is an ideal 45Ω to GND on DP and DN.	–10		10	mV

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CHIRPJ}	Host/ Hub Chirp J level (differential voltage)	USB 2.0 Spec Section 7.1.7.2 (1) (PE is disabled. Swing setting has no impact but slew rate control has impact), Test load is an ideal 1.5kΩ pullup on DP.	700	900	1100	mV
V_{CHIRPK}	Device Chirp K level (differential voltage)	USB 2.0 Spec Section 7.1.7.2 (1) (PE is disabled. Swing setting has no impact but slew rate control has impact), Test load is an ideal 45Ω to GND on DP and DN.	–900	–760	–500	mV
V_{CHIRPK}	Host/Hub Chirp K level (differential voltage)	USB 2.0 Spec Section 7.1.7.2 (1) (PE is disabled. Swing setting has no impact but slew rate control has impact), Test load is an ideal 1.5kΩ pullup on DP.	–900	–700	–500	mV
$U2\_TX_{PE}$	High-speed TX Pre-emphasis	U_HS_TX_PRE_EMPHASIS_Px Setting 001,Test load is an ideal 45Ω to GND on DP and DN.	0.62	0.9	1.2	dB
$U2\_TX_{PE\_UI}$	High-speed TX Pre-emphasis	U_HS_TX_PE_WIDTH_Px Setting 00 (measured with PE=2.5dB setting of 101), Test load is an ideal 45Ω to GND on DP and DN.	0.25	0.35	0.41	UI
$U2\_TX_{PE\_UI}$	High-speed TX Pre-emphasis width	U_HS_TX_PE_WIDTH_Px Setting 01 (measured with PE=2.5dB setting of 101), Test load is an ideal 45Ω to GND on DP and DN.	0.35	0.45	0.55	UI
$U2\_TX_{PE\_UI}$	High-speed TX Pre-emphasis width	U_HS_TX_PE_WIDTH_Px Setting 10 (measured with PE=2.5dB setting of 101), Test load is an ideal 45Ω to GND on DP and DN.	0.44	0.55	0.67	UI
$U2\_TX_{PE\_UI}$	High-speed TX Pre-emphasis width	U_HS_TX_PE_WIDTH_Px Setting 11 (measured with PE=2.5dB setting of 101), Test load is an ideal 45Ω to GND on DP and DN.	0.54	0.65	0.77	UI
$U2\_TX_{CM}$	High-speed TX DC Common Mode	All Swing settings with PE disabled	100	200	300	mV
eUSB2 TERMINATION						
R_{SRC_HS}	High-speed transmit source termination impedance	eUSB2 Spec Section 7.1.1 (2)	33	40	47	Ω
ΔR_{SRC_HS}	High-speed source impedance mismatch	eUSB2 Spec Section 7.1.1 (2)			4	Ω
R_{RCV_DIF}	High-speed differential receiver termination (repeater)	eUSB2 Spec Section 7.1.2 (2)	74	80	86	Ω
R_{PD}	Pulldown resistors on eDP/eDN	eUSB2 Spec Section 7.3 (2), active during LS, FS and HS	6	8	10	kΩ
R_{SRC_LSFS}	Transmit output impedance	eUSB2 Spec Section 7.2.1 (2), Table 7-13 TX output impedance to match spec version 1.10	28	44	59	Ω
C_{IO_eDx}	Differential capacitance	Measured with VNA at 240MHz, Driver Hi-Z (VCM = 120mV to 450mV), Measured differentially.		3.7	5	pF
eUSB0, eUSB1 FS/LS INPUT LEVELS						
V_{IL}	Single-ended input low	eUSB2 Spec Section 7.2.1, Table 7-13 (2)	–0.1		0.399	V
V_{IH}	Single-ended input high	eUSB2 Spec Section 7.2.1, Table 7-13 (2)	0.819		1.386	V
V_{HYS}	Receive single-ended hysteresis voltage	eUSB2 Spec Section 7.2.1, Table 7-13 (2)	43.2			mV
eUSB0, eUSB1 FS/LS OUTPUT LEVELS						

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Single-ended output low	eUSB2 Spec Section 7.2.1, Table 7-13 (2)			0.1	V
V_{OH}	Single-ended output high	eUSB2 Spec Section 7.2.1, Table 7-13 (2)	0.918		1.32	V
eUSB0, eUSB1 HS INPUT LEVELS						
$V_{CM\_RX\_AC}$	Receiver AC common mode (50MHz-480MHz)	eUSB2 Spec Section 7.1.2 (informative) (2), across the DC common mode range of 120mV to 280mV. (RX capability tested with intentional TX Rise/Fall Time mismatch and prop delay mismatch)	–60		60	mV
C_{RX_CM}	Receive center-tapped capacitance	eUSB2 Spec Section 7.1.2 (informative) (2)	15		50	pF
V_{EHSSQ}	Squelch/No-squelch detect threshold	eUSB2 Spec Section 7.1.2 (2), (measured as differential peak voltage at 240MHz with increasing amplitude), V_{CM} = 120mV to 450mV	47	66	83	mV
EQ_{EHS}	eUSB2 High-speed data receiver equalization, (measured indirectly through jitter)	240MHz E_EQ_P1x Setting 0010	0.59	1.12	1.4	dB
eUSB0, eUSB1 HS OUTPUT LEVELS						
V_{EHSOD}	Transmit differential (terminated)	Measured p2p, R_L = 80Ω, E_HS_TX_AMPLITUDE_ Px setting 100, ideal 80Ω Rx differential termination load	396	440	484	mV
E_TXPE	High-speed TX Pre-emphasis	E_HS_TX_PRE_EMPHASIS_Px Setting 010	1.01	1.29	1.57	dB

(1) USB 2.0 Promoter Group 2000, USB 2.0 Specification USB 2.0 Promoter Group
(2) USB Implementers Forum (2018). Embedded USB2 (eUSB2) Physical Layer Supplement to the USB Revision 2.0 Specification, Rev. 1.2 USB Implementers Forum

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DPA, DNA, DPB, DNB, HS Driver Switching Characteristics						
T_{HSR}	Rise Time (10% - 90%)	USB 2.0 Spec Section 7.1.2 (1), U_HS_TX_SLEW_RATE_Px Setting 11, ideal 45Ω to GND loads on DP and DN, Pre-emphasis disabled.	530	625	740	ps
T_{HSF}	Fall Time (10% - 90%)	USB 2.0 Spec Section 7.1.2 (1), U_HS_TX_SLEW_RATE_Px Setting 11, ideal 45Ω to GND loads on DP and DN, Pre-emphasis disabled.	530	625	740	ps
DPA, DNA, DPB, DNB, FS Driver Switching Characteristics						
T_{FR}	Rise Time (10% - 90%)	USB 2.0 Spec Figure 7-8; Figure 7-9 (1)	4		20	ns
T_{FF}	Fall Time (10% - 90%)	USB 2.0 Spec Figure 7-8; Figure 7-9 (1)	4		20	ns
T_{FRFM}	(T_{FR}/T_{FM})	USB 2.0 Spec 7.1.2 (1), Excluding the first transition from the Idle state	90		111.1	%
DPA, DNA, DPB , DNB, LS Driver Switching Characteristics						
T_{LR}	Rise Time (10% - 90%)	USB 2.0 Spec Figure 7-8 (1)	75		300	ns
T_{LF}	Fall Time (10% - 90%)	USB 2.0 Spec Figure 7-8 (1)	75		300	ns
eDP0, eDN0, eDP1, eDN1, HS Driver Switching Characteristics						
T_{EHSRF}	Rise/Fall Time (20% - 80%)	eUSB2 Spec Section 7.2.1 (2), ideal 80Ω Rx differential termination E_HS_TX_SLEW_RATE_Px Setting = 01	355	440	525	ps
T_{EHSRF_MM}	Transmit rise/fall mismatch	eUSB2 Spec Section 7.2.1 (2), Rise/fall mismatch = absolute delta of (rise – fall time) / (average of rise and fall time).			25	%
eDP0, eDN0, eDP1, eDN1, LS/FS Driver Switching Characteristics						
T_{ERF}	Rise/Fall Time (10% - 90%)	eUSB2 Spec Section 7.2.1 (2)	2		6	ns
T_{ERF_MM}	Transmit rise/fall mismatch	eUSB2 Spec Section 7.2.1 (2)			25	%
I2C (SDA)						
T_r	Rise Time (STD)	Bus Speed = 100kHz, C_L= 200pF, R_{PU} = 4kΩ, I_{OL} = ~1mA	600			ns
T_r	Rise Time (FM)	Bus Speed = 400kHz, C_L= 200pF, R_{PU} = 2.2kΩ, I_{OL} = ~2mA	180			ns
T_r	Rise Time (FM+)	Bus Speed = 1MHz, C_L= 10pF, R_{PU} = 1kΩ, I_{OL} = ~4mA	72			ns
T_r	Rise Time (STD)	Bus Speed = 100kHz, C_L= 200pF, R_{PU} = 4kΩ, I_{OL} = ~2mA			1000	ns
T_r	Rise Time (FM)	Bus Speed = 400kHz, C_L= 200pF, R_{PU} = 1kΩ, I_{OL} = ~8mA			300	ns
T_r	Rise Time (FM+)	Bus Speed = 1MHz, C_L= 50pF, R_{PU} = 1kΩ, I_{OL} = ~4mA			120	ns
T_f	Fall Time (STD)	Bus Speed = 100kHz, C_L= 200pF, R_{PU} = 2.2kΩ, I_{OL} = ~4mA			106.5	ns
T_f	Fall Time (FM)	Bus Speed = 400kHz, C_L= 200pF, R_{PU} = 1kΩ, I_{OL} = ~8mA			106.5	ns
T_f	Fall Time (FM+)	Bus Speed = 1MHz, C_L= 90pF, R_{PU} = 1kΩ, I_{OL} = ~8mA			81.5	ns
T_f	Fall Time (STD)	Bus Speed = 100kHz, C_L= 10pF, R_{PU} = 4kΩ, , I_{OL} = ~2mA	6.5			ns
T_f	Fall Time (FM)	Bus Speed = 400kHz, C_L= 10pF, R_{PU} = 2.2kΩ, I_{OL} = ~4mA	6.5			ns

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_f	Fall Time (FM+)	Bus Speed = 1MHz, C_L= 10pF, R_{PU} = 1kΩ, I_{OL} = ~8mA		6.5		ns

(1) USB 2.0 Promoter Group 2000, USB 2.0 Specification USB 2.0 Promoter Group
(2) USB Implementers Forum (2018). Embedded USB2 (eUSB2) Physical Layer Supplement to the USB Revision 2.0 Specification, Rev. 1.2 USB Implementers Forum

6.7 Timing Requirements

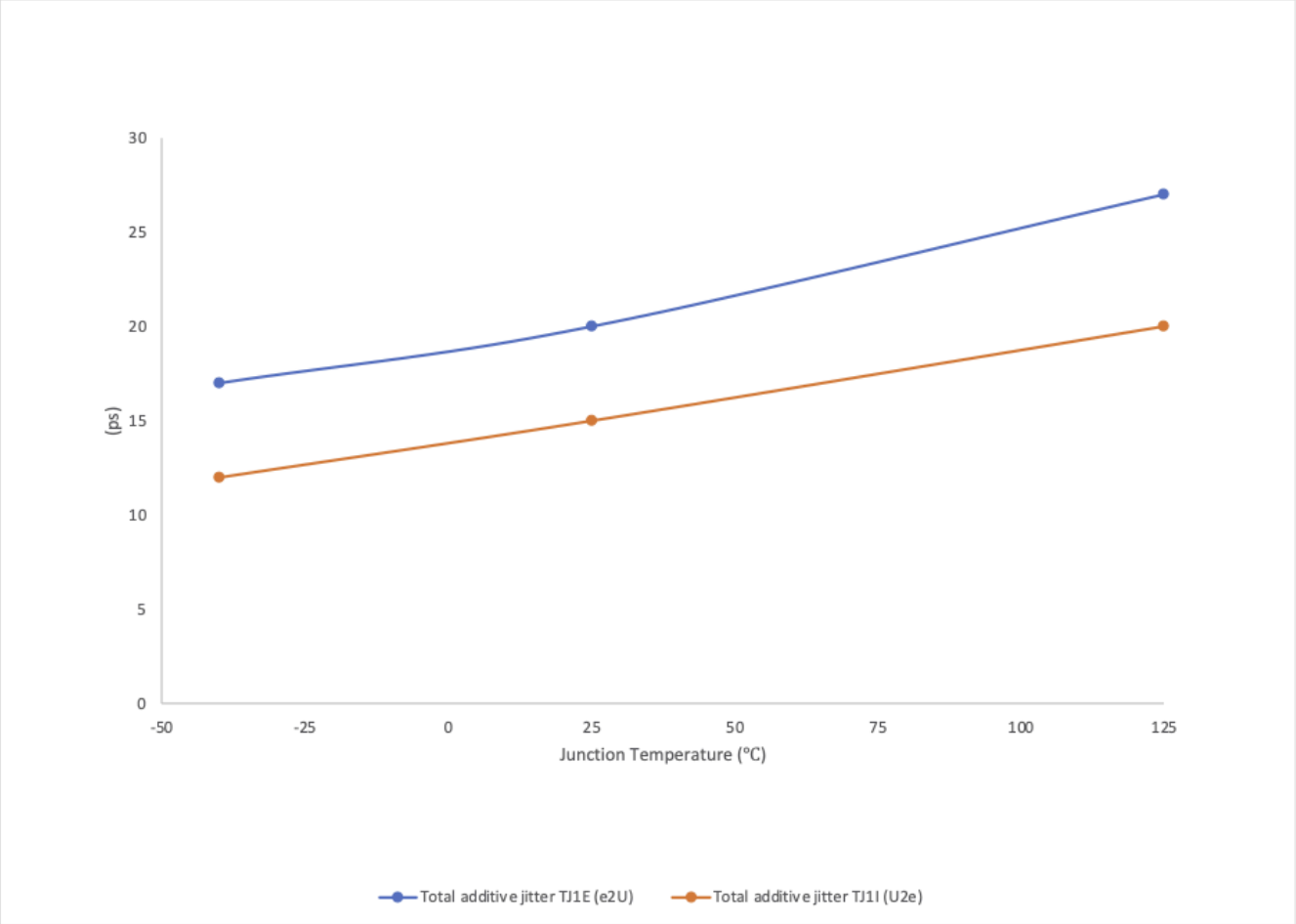
		MIN	NOM	MAX	UNIT
I/O TIMING					
t_{GPIO_PW}	Minimum GPIO pulse width for INT event	8			µs
RESET TIMING					
t_{VDD1V8_RAMP}	Ramp time for VDD1V8 to reach minimum 1.62V			2	ms
t_{VDD3V3_RAMP}	Ramp time for VDD3V3 to reach minimum 3.0V			2	ms
t_{su_CROSS}	Setup time for CROSS sampled at the deassertion of RESETB	0			ms
t_{hd_CROSS}	Hold time for CROSS sampled at the deassertion of RESETB	3			ms
$t_{aRESETB}$	Duration for RESETB to be asserted low to complete reset while powered	10			µs
t_{RH_READY}	Time for device to be ready to accept RAP and I2C requests and eUSB2 interface to be ready after RESETB is deasserted or (VDD1V8 and VDD3V3) reach minimum recommended voltages, whichever is later			3	ms
t_{RS_READY}	Time for device to be ready to accept RAP and I2C requests and eUSB2 interface to be ready after soft reset through I2C			350	µs
REPEATER TIMING					
T_{J1E}	Total additive jitter for eUSB2 to USB 2.0 (output jitter - input jitter) of repeater when one of the two repeater is disabled. (must also include all complete SOP bits and measured with eUSB2 TX rise/fall time skew and intra-pair prop delay skew, refer to $V_{CM\_RX\_AC}$) [RX EQ disabled, TX PE disabled, VOD nominal setting and no input or output channel]. Egress setup diagram		25	42	ps
T_{J1I}	Total additive jitter for USB to eUSB2 (output jitter - input jitter) of repeater when one of the two repeater is disabled. [RX EQ disabled, TX PE disabled, VOD nominal setting and no input or output channel]. Ingress setup diagram		25	42	ps
T_{J2E}	Total additive jitter for eUSB2 to USB (output jitter - input jitter) of repeater when both repeaters are active. [RX EQ disabled, TX PE disabled, VOD nominal setting and no input or output channel]			60	ps
T_{J2I}	Total additive jitter for USB to eUSB2 (output jitter - input jitter) of repeater when both repeaters are active. [RX EQ disabled, TX PE disabled, VOD nominal setting and no input or output channel]			60	ps
$T_{e\_to\_U\_DJ1}$	eUSB2 to USB 2.0 repeater FS jitter to next transition (Per eUSB2 spec 1.1 Table 7-13 Note 1 & 2 condition for Supply and GND delta (1))	–6.0		+6.0	ns
$T_{U\_to\_e\_DJ1}$	USB 2.0 to eUSB2 repeater FS jitter to next transition (Per eUSB2 spec 1.1 Table 7-13 Note1 & 2 condition for Supply and GND delta (1))	–3.0		+3.0	ns
T_{DJ2_e2U}	Repeater FS paired transition jitter in eUSB2 to USB 2.0 direction (Relaxed relative to THDJ2 defined by USB 2.0 +/-1ns)	–1.5		+1.5	ns
T_{DJ2_U2e}	Repeater FS paired transition jitter in USB 2.0 to eUSB2 direction (Relaxed relative to THDJ2 defined by USB 2.0 +/-1ns)	–1.5		+1.5	ns
MODE TIMING					
T_{MODE_SWITCH}	Time needed to change mode from UART bypass mode to and from USB mode			1	µs
T_{UART_START}	Time needed to start transmitting UART data after entering UART bypass mode			2	ms
I2C (FM+)					
t_{SU_STA}	Start setup time, SCL (T_r=72ns to 120ns), SDA (T_f=6.5ns to 81.5ns), 1MHz FM+	260			ns
t_{SU_STO}	Stop setup time, SCL (T_r=72ns to 120ns), SDA (T_f=6.5ns to 81.5ns), 1MHz FM+	260			ns
t_{HD_STA}	Start hold time, SCL (T_r=72ns to 120ns), SDA (T_f=6.5ns to 81.5ns), 1MHz FM+	260			ns

		MIN	NOM	MAX	UNIT
t_{SU_DAT}	Data input or False start/stop, setup time, SCL (T_r=72ns to 120ns), SDA (T_f=6.5ns to 81.5ns), 1MHz FM+	50			ns
t_{HD_DAT}	Data input or False start/stop, hold time, SCL (T_r=72ns to 120ns), SDA (T_f=6.5ns to 81.5ns), 1MHz FM+	0			ns
t_{VD_DAT}, t_{VD_ACK}	SDA output delay, SCL (T_r=72ns to 120ns), SDA (T_f=6.5ns to 81.5ns), 1MHz FM+	20		450	ns
$t_{HD\_DAT\_SL}$	Data hold time when device is transmitting	6.67			ns
t_{SP}	Glitch width suppressed	50		91	ns
t_{BUF}	Bus free time between a STOP and START condition (host minimum spec that device must tolerate)	0.5			µs
t_{LOW}	Low Period for SCL clock (host minimum spec that device must tolerate)	0.5			µs
t_{HIGH}	High Period for SCL clock (host minimum spec that device must tolerate)	0.26			µs
I2C (FM)					
t_{SU_STO}	Stop setup time, SCL (T_r=180ns to 300ns), SDA (T_f=6.5ns to 106.5ns), 400kHz FM	600			ns
t_{HD_STA}	Start hold time, SCL (Tr=180ns to 300ns), SDA (Tf=6.5ns to 106.5ns), 400kHz FM	600			ns
t_{SU_STA}	Start setup time, SCL (T_r=180ns to 300ns), SDA (T_f=6.5ns to 106.5ns), 400kHz FM	600			ns
t_{SU_DAT}	Data input or False start/stop, setup time, SCL (T_r=180ns to 300ns), SDA (T_f=6.5ns to 106.5ns), 400kHz FM	100			ns
t_{HD_DAT}	Data input or False start/stop, hold time, SCL (T_r=180ns to 300ns), SDA (T_f=6.5ns to 106.5ns), 400kHz FM	0			ns
t_{VD_DAT}, t_{VD_ACK}	SDA output delay, SCL (T_r=180ns to 300ns), SDA (T_f=6.5ns to 106.5ns), 400kHz FM	20		900	ns
$t_{HD\_DAT\_SL}$	Data hold time when device is transmitting	13.5			ns
t_{SP}	Glitch width suppressed	50		91	ns
t_{BUF}	Bus free time between a STOP and START condition (host minimum spec that device must tolerate)	1.3			µs
t_{LOW}	Low Period for SCL clock (host minimum spec that device must tolerate)	1.3			µs
t_{HIGH}	High Period for SCL clock (host minimum spec that device must tolerate)	0.6			µs
I2C (STD)					
t_{SU_STO}	Stop setup time, SCL (T_r=600ns to 1000ns), SDA (T_f=6.5ns to 106.5ns), 100kHz STD	4			µs
t_{HD_STA}	Start hold time, SCL (Tr=600ns to 1000ns), SDA (Tf=6.5ns to 106.5ns), 100kHz STD	4			µs
t_{SU_STA}	Start setup time, SCL (T_r=600ns to 1000ns), SDA (T_f=6.5ns to 106.5ns), 100kHz STD	4.7			µs
t_{SU_DAT}	Data input or False start/stop, setup time, SCL (T_r=600ns to 1000ns), SDA (T_f=6.5ns to 106.5ns), 100kHz STD	250			ns
t_{HD_DAT}	Data input or False start/stop, hold time, SCL (T_r=600ns to 1000ns), SDA (T_f=6.5ns to 106.5ns), 100kHz STD	5			µs
t_{VD_DAT}, t_{VD_ACK}	SDA output delay, SCL (T_r=600ns to 1000ns), SDA (T_f=6.5ns to 106.5ns), 100kHz STD			3.45	µs
$t_{HD\_DAT\_SL}$	Data hold time when device is transmitting	13.5			ns
t_{SP}	Glitch width suppressed	50		91	ns
t_{BUF}	Bus free time between a STOP and START condition (host minimum spec that device must tolerate)	4.7			µs
t_{LOW}	Low Period for SCL clock (host minimum spec that device must tolerate)	4.7			µs

		MIN	NOM	MAX	UNIT
t_{HIGH}	High Period for SCL clock (host minimum spec that device must tolerate)	4.0			µs

(1) USB Implementers Forum (2018). Embedded USB2 (eUSB2) Physical Layer Supplement to the USB Revision 2.0 Specification, Rev. 1.2 USB Implementers Forum

6.8 Typical Characteristics



TJ1E is for egress direction from eUSB2 to USB and TJ1I is for ingress direction from USB to eUSB2

図 6-1. Total Additive Jitter (Typical)

7 Parametric Measurement Information

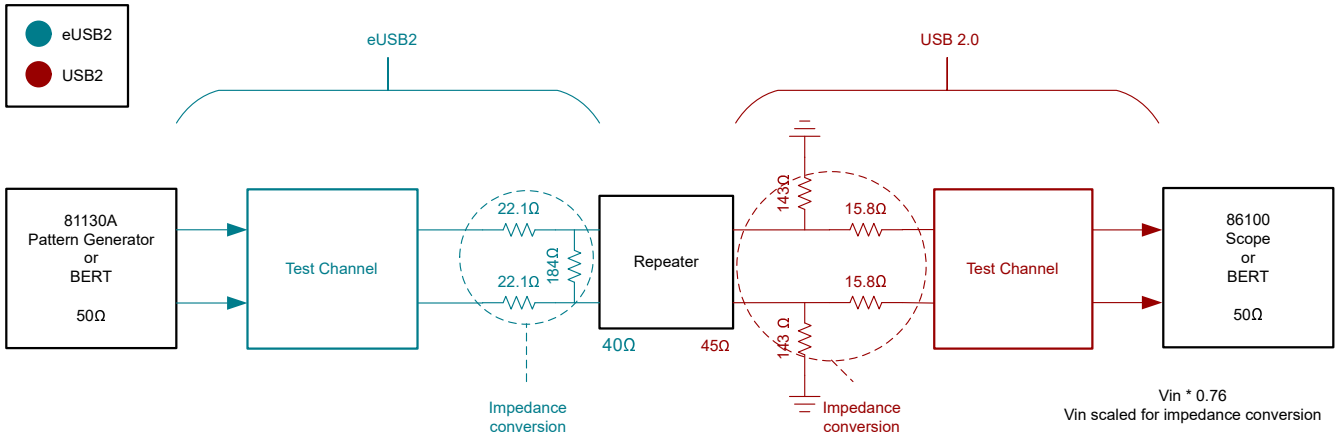


図 7-1. USB 2.0 TX Output (Egress) Jitter, Eye Mask Test Setup

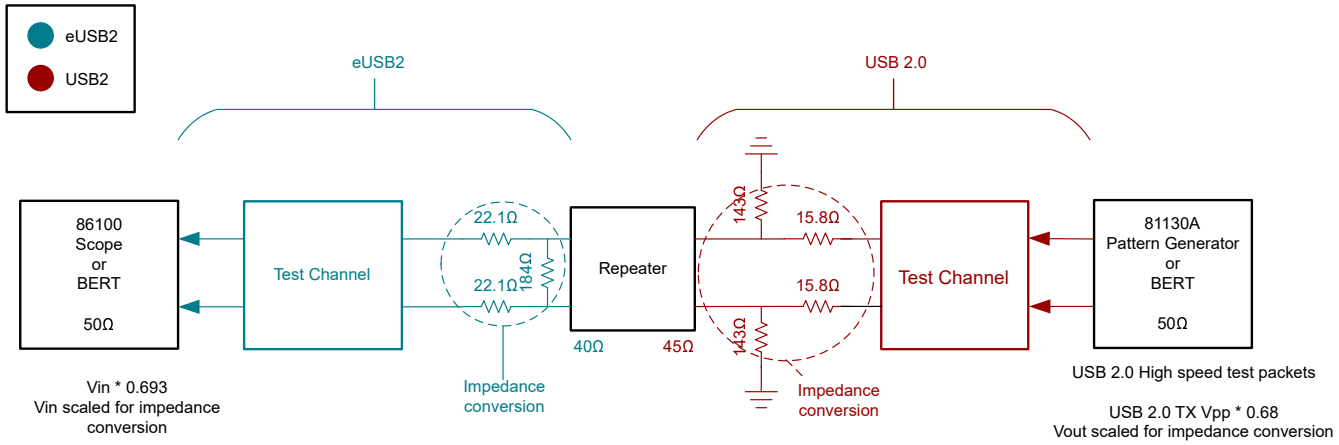


図 7-2. eUSB2 TX Output (Ingress) Jitter, Eye Mask Test Setup

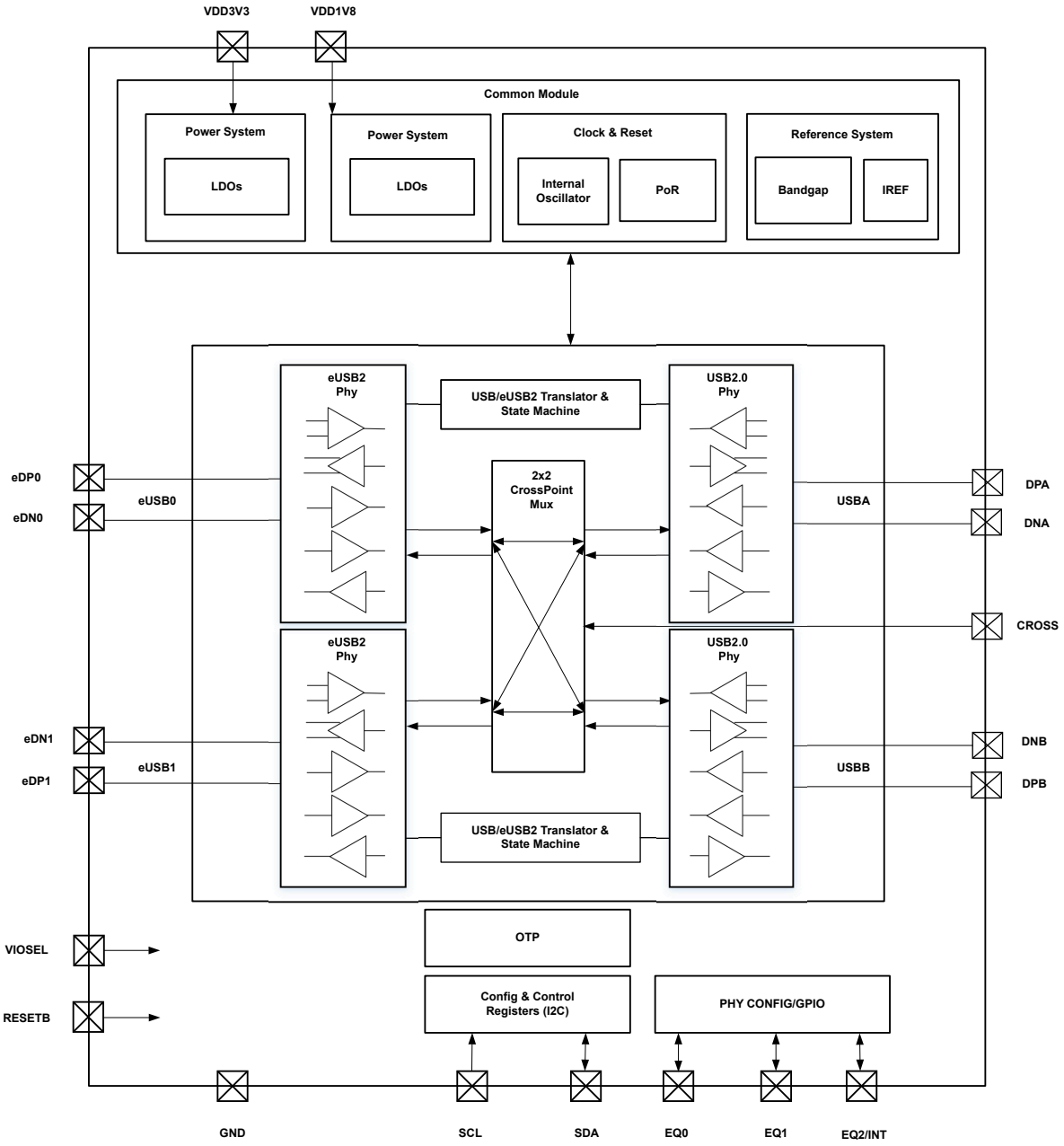
8 Detailed Description

8.1 Overview

The TUSB2E221 is a dual eUSB2 to USB 2.0 repeater that resides between SoC with one or two eUSB2 port and an external connector that supports USB 2.0. Each repeater is independently configurable as either a host or device repeater (DRD repeater).

The USB 2.0 ports A and B can be swapped by an internal crossbar switch by configuring CROSS pin at reset. The CROSS pin is ignored after power up reset.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 USB 2.0

The TUSB2E221 supports two USB 2.0 ports. Each port supports low-speed, full-speed and high-speed operations.

8.3.2 eUSB2

The TUSB2E221 supports two eUSB2 ports with low-speed, full-speed and high-speed operations.

8.3.3 Cross MUX

The TUSB2E221 supports a cross mux functionality that can map either of the two eUSB2 ports to the two USB 2.0 ports providing design flexibility.

8.4 Device Functional Modes

8.4.1 Repeater Mode

After the RESETB deassertion and $t_{\_RH\_READY}$, the TUSB2E221 is enabled and enters the default state, ready to accept eUSB2 packets.

表 8-1. Number of Hubs Supported with Host and/or Peripheral Repeater

Number of eUSB2 Repeaters	Number of Hubs Operating at HS	Number of Hubs Operating at FS	
1	4	2	Number of hubs operating at FS is reduced due to $T_{e\_to\_U\_DJ1}$ and T_{RJR1}. Number of hubs operating at HS is reduced due to SOP truncation and EOP dribble
2	3	1	
0	5	5	non-eUSB2 system for reference

8.4.2 Power-Down Mode

RESETB can be used as a power-down pin when asserted low. Power-down mode puts the TUSB2E221 in the lowest power mode.

8.4.3 UART Mode

In I^2C mode GPIO0 defaults as an enable control for Carkit UART mode. GPIO0 is an active low signal to enable Carkit UART mode. GPIO0 can be controlled through APU or SoC. When APU or SoC is not powered on or the firmware has not been loaded, GPIO0 is low. When GPIO0 is low, the UART mode allows access to the APU or SoC debug interface through the USB port.

Default Carkit UART direction is DP → eDP (RX) and eDN → DN (TX).

On the rising edge of GPIO0, followed by T_{MODE_SWITCH}, the TUSB2E221 is enabled and enters the default state, ready to accept eUSB2 port reset, configuration or RAP. The repeater mode is configured as host or peripheral depending on the eUSB2-defined configuration received from eUSBr and acknowledged by the repeater.

UART mode enable is controlled through GPIO0 after power up. This can be changed through UART_use_bit1_Px bit in UART-PORTx register, so UART mode enable can be controlled through a register instead of GPIO0.

8.4.4 Auto-Resume ECR

Optional host repeater auto-resume is supported by the TUSB2E221 in L1/L2 by driving Resume K at D+/D- until SOResume is received from eDSPr. In addition, the TUSB2E221 eUSPh will hold Remote Wake line state until SORresume is received from eDSPr.

This auto-resume feature provides the host controller extra time to exit low power state and issue SOResume while the TUSB2E221 UDSP drives resume within 1ms (T_{URSM}) hub resume timing requirement. To take advantage of this low power feature, the host controller implements low power mechanism to detect wake on eDSPr lines while host controller is in low power state.

This auto-resume feature is not required if host controller is capable of initiating SOResume within 1ms of detecting Remote Wake on eDSPr.

This auto-resume ECR mode is disabled when L2 interrupt mode is enabled. When L2 interrupt mode is enabled, resume K at D+/D- is still driven when Remote wake is detected on UDSP but eUSPh is held at SE0 instead of in Remote Wake state. See the *L2 State Interrupt Modes* section for more details.

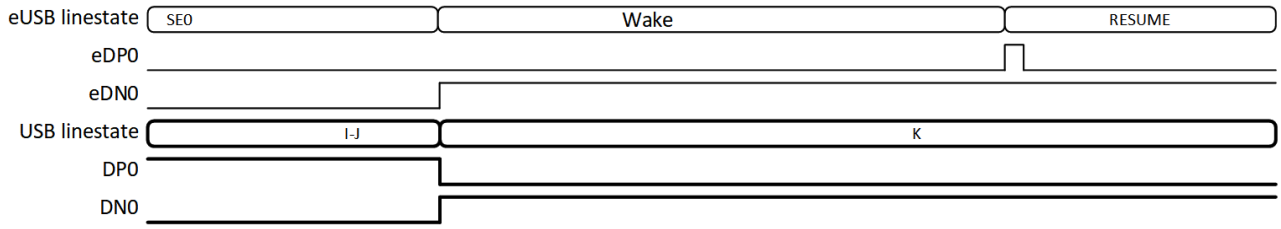


図 8-1. Timing Diagram for Auto-Resume for HS/FS

8.4.5 L2 State Interrupt Modes

To prevent signaling on eUSB2 while the eDSP is powered off, enable both L2 remote wake interrupt and disconnect event interrupt modes. The special remote wake sequence when L2 remote wake interrupt mode is enabled.

- System enables interrupt USB_REMOTE_WAKE_Px.
- Repeater is in host mode and has received a CM.L2.
- Repeater detects wake on USB 2.0
- Repeater asserts interrupt.
- Repeater reflects *resume* on USB 2.0, but does not signal wake on eUSB2.
- Repeater waits for eDSPr to signal start of resume with no intervening configuration, connect, or reset sequence.
- Repeater and eDSP follow normal eUSB2 protocol to signal resume starting and ending in L0.

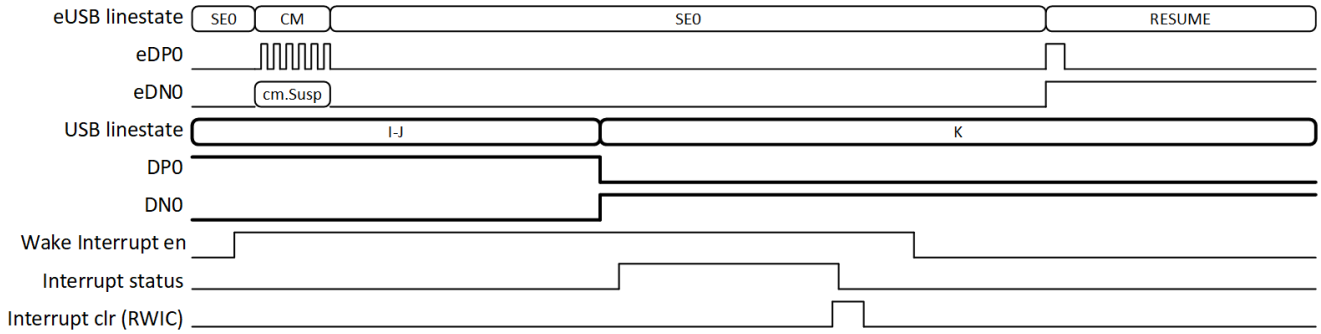


図 8-2. Timing Diagram for Wake Interrupt for HS/FS

The special wake on disconnect sequence when disconnect event interrupt mode is enabled

- System enables interrupt USB_DISCONNECT_Px.
- Repeater is in host mode and has received a CM.L2.
- Repeater detects SE0 for disconnect on USB 2.0.
- Repeater asserts interrupt.
- Interrupt must be cleared prior to eDSPr reinitializing the TUSB2E221 as a host.
- Repeater does not signal or report USB 2.0 SE0 on eUSB2.
- Repeater waits for eDSPr to power up, which starts with port reset announcement.
- Repeater and eDSP follow normal eUSB2 protocol, ending in unconnected state of host mode.

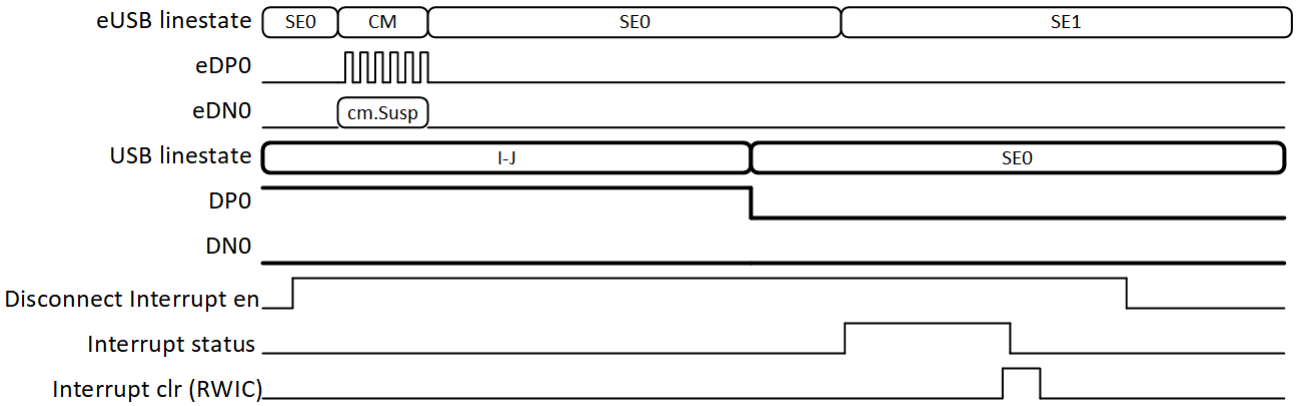


図 8-3. Timing Diagram for Disconnect Interrupt for HS/FS

8.4.6 Attach Detect Interrupt Mode

When attach event detect is enabled the TUSB2E221 issues an interrupt event instead of signaling attach on eUSB2.

- System enables interrupt USB_DETECT_ATTACH_Px. Interrupt must be enabled prior to any connect event.
- Repeater is in host mode.
- Repeater detects attach on USB 2.0.
- Repeater debounces attach for 60µs and asserts interrupt instead of signaling attach on eUSB2.
- Interrupt must be disabled prior to eDSPr reinitializing as a host to process attach through normal mechanism.

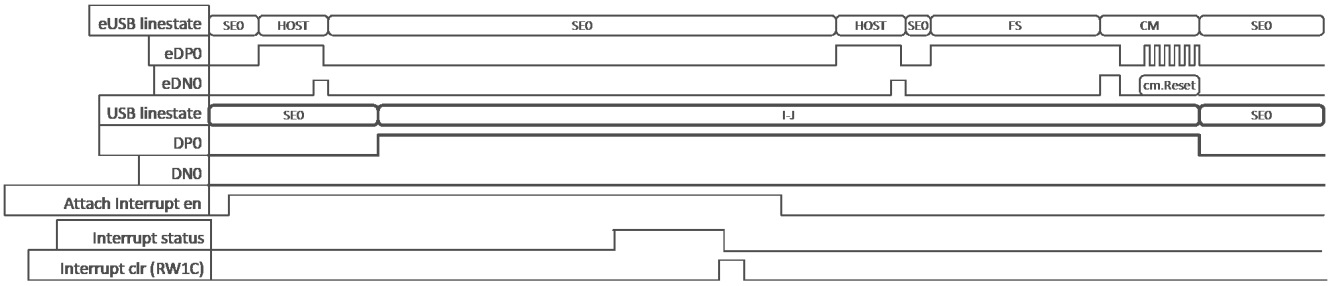


図 8-4. Timing Diagram for Attach Detect Interrupt for HS/FS

8.4.7 GPIO Mode

8.4.7.1 EQ0 as GPIO0

The EQ0 pin enters input mode at power up and is sampled during reset.

The EQ0 defaults to active high UART mode (bypass mode) enable control for eUSB2 port0 after power up in I^2C mode.

The EQ0 pin can be configured to be input or output mode through the I^2C register write. The output event is selected through the I^2C register. Refer to the GPIO0_CONFIG register for more information.

The EQ0 input status change can be reported through the EQ2/INT as an interrupt if enabled through the I^2C. The status change trigger can be programmed to be edge trigger or level trigger through the I^2C.

The EQ0 pin in output mode defaults to open-drain output but can be configured to be push-pull output. The EQ0 pin can drive up to 3pF loads when in push-pull mode.

The EQ0 pin reverts back to input upon RESETB assert, deassert, or soft reset.

In non I^2C mode, the EQ0 pin is used for USB PHY tuning.

8.4.7.2 EQ1 as GPIO1

The EQ1 pin enters input mode at power up and is sampled during reset.

The EQ1 defaults to active high UART mode (bypass mode) enable control for eUSB2 port1 after power up in I^2C mode.

The EQ1 pin can be configured to be input or output mode through the I^2C register write. The output event is selected through the I^2C register. Refer to the GPIO1_CONFIG register.

The EQ1 input status change can be reported through the EQ2/INT as an interrupt if enabled through the I^2C. The status change trigger can be programmed to be an edge trigger or level trigger through the I^2C.

The EQ1 pin in output mode defaults to open-drain output but can be configured to be push-pull output. EQ1 pin can drive up to 3pF loads when in push-pull mode.

The EQ1 pin reverts back to input upon RESETB assert, deassert, or soft reset.

In non I^2C mode, the EQ1 pin is used for USB PHY tuning.

8.4.7.3 EQ2/INT as GPIO2

The EQ2/INT pin defaults to open-drain interrupt (INT) active low output at power up but can be programmed through the I^2C to be a push-pull output. In push-pull mode, the EQ2/INT pin can be programmed to be either active high or active low. Interrupt output is a level-sensitive interrupt. Trigger events can be selected through the I^2C.

Connect EQ2/INT to APU to use interrupt functions and a pullup resistor (open-drain mode).

EQ2/INT interrupt output can be configured through the *INT_ENABLE_1*/2 and *INT_STATUS*_1/2 registers.

In non I^2C mode, EQ2/INT pin is used for USB PHY tuning.

8.4.8 CROSS

The CROSS pin will control the orientation of the integrated cross bar mux.

After the RESETDB deassertion followed by internally generated reset signal and 1ms delay, the CROSS pin is sampled and latched.

The system must make sure that CROSS meets $t_{\_su\_CROSS}$ and $t_{\_hd\_CROSS}$ with respect to power supply ramp and RESETB deassertion per *Power Supply Recommendations*.

Changes to the state of the CROSS input while RESETB is high are ignored.

表 8-2. eUSB2 to USB Mapping

	CROSS = 0	CROSS = 1
eUSB0 (eDP0, eDN0)	USBA (DPA, DNA)	USBB (DPB, DNB)
eUSB1 (eDP1, eDN1)	USBB (DPB, DNB)	USBA (DPA, DNA)

8.4.9 USB 2.0 High-Speed HOST Disconnect Detection

USB 2.0 specification does not specify high-speed output differential swing V_{OD} during disconnect without external load. Only chirp level and HS host disconnect threshold are specified. Specification implicitly assumes high-speed output differential swing V_{OD} will double during disconnect. However, the high-speed output differential swing during disconnect depends on the USB 2.0 TX output swing and pre-emphasis setting, as the common-mode voltage increase can saturate the output swing level and may not double.

The high-speed host disconnect threshold can be adjusted to provide the most margin to avoid false disconnect as well as failure to detect a disconnect. See 表 8-3.

表 8-3. Recommended USB 2.0 High-Speed HOST Disconnect Thresholds per USB HSTX Amplitude and Pre-Emphasis

	USB HS TX Pre-Emphasis					
USB HS TX Amplitude (Vp-p)	**0.5dB (0h)**	**0.9dB (1h)**	**1.2dB (2h)**	**1.7dB (3h)**	**2.1dB (4h)**	**2.5dB (5h)**
740mV (0h)	545mV (1h)	545mV (1h)	545mV (1h)	545mV (1h)	545mV (1h)	545mV (1h)
760mV (1h)	565mV (2h)	565mV (2h)	565mV (2h)	565mV (2h)	565mV (2h)	565mV (2h)
780mV (2h)	585mV (3h)	585mV (3h)	585mV (3h)	585mV (3h)	585mV (3h)	585mV (3h)
800mV (3h)	585mV (3h)	585mV (3h)	585mV (3h)	585mV (3h)	585mV (3h)	585mV (3h)
820mV (4h)	605mV (4h)	605mV (4h)	605mV (4h)	605mV (4h)	605mV (4h)	605mV (4h)
840mV (5h)	625mV (5h)	625mV (5h)	625mV (5h)	625mV (5h)	625mV (5h)	625mV (5h)
860mV (6h)	645mV (6h)	645mV (6h)	645mV (6h)	645mV (6h)	625mV (5h)	625mV (5h)
880mV (7h)	645mV (6h)	645mV (6h)	645mV (6h)	645mV (6h)	645mV (6h)	645mV (6h)
900mV (8h)	665mV (7h)	665mV (7h)	665mV (7h)	665mV (7h)	665mV (7h)	645mV (6h)
920mV (9h)	685mV (8h)	685mV (8h)	685mV (8h)	665mV (7h)	665mV (7h)	665mV (7h)
940mV (Ah)	685mV (8h)	685mV (8h)	685mV (8h)	685mV (8h)	665mV (7h)	665mV (7h)
960mV (Bh)	705mV (9h)	705mV (9h)	705mV (9h)	685mV (8h)	685mV (8h)	665mV (7h)
980mV (Ch)	725mV (Ah)	705mV (9h)	705mV (9h)	705mV (9h)	685mV (8h)	685mV (8h)
1000mV (Dh)	725mV (Ah)	725mV (Ah)	705mV (9h)	705mV (9h)	685mV (8h)	685mV (8h)
1020mV (Eh)	725mV (Ah)	725mV (Ah)	725mV (Ah)	705mV (9h)	705mV (9h)	685mV (8h)
1040mV (Fh)	745mV (Bh)	725mV (Ah)	725mV (Ah)	705mV (9h)	705mV (9h)	685mV (8h)

8.4.10 Frame Based Low Power Mode

The USB2.0 standard defines high-speed microframes that occur every 125µs. Using a patented design, the TUSB2E221 monitors idle conditions within every high-speed microframe. The TUSB2E221 will enter a low power state if the bus is idle for greater than 7.8125µs and will remain in the low power state until the start of the next µSOF. This feature is enabled by default and can be disabled by clearing HOST_FRAME_LP_EN_Px or DEVICE_FRAME_LP_EN_Px bits.

表 8-4 shows an example of the typical high-speed idle power the TUSB2E221 consumes based on whether or not the frame based low power is enabled. These results assume the TUSB2E221 is in host repeater mode.

表 8-4. Typical Single Port High-Speed Idle Power for Frame Base LP Mode

HOST_FRAME_LP_EN_Px	1.8V current (mA)	3.3V current (mA)
0 (Disabled)	56	2.8

表 8-4. Typical Single Port High-Speed Idle Power for Frame Base LP Mode (続き)

HOST_FRAME_LP_EN_Px	1.8V current (mA)	3.3V current (mA)
1 (Enabled)	12	2.0

注

Frame based low power mode is enabled by default. If using TUSB2E221 in pin-strap mode, this feature can not be disabled. Contact support if a device variant with frame based low power mode disabled in pin-strap mode is needed.

8.5 Programming

8.5.1 I²C Target Interface

I²C target interface enables access to internal registers by the system application processor. The primary function of the interface is to enable configuring various PHY parameters, controlling the GPIO pins, and enabling USB-BC functions. The TUSB2E221 repeater functions operates after power up without requiring I²C configuration.

The TUSB2E221 has I²C 7-bit target address of 0x4F. 8-bit address of Write: 0x9E and Read: 0x9F.

I²C default target address can be changed at the factory through one-time programming.

I²C drive strength can be changed through the I²C.

表 8-5. Recommended I²C Drive Strength for I²C Bus Speed, Bus Pullup and Bus Capacitance

I²C FM+ (1MHz Max)	I²C drive strength (I_{OL}) selection			
	I2C bus pullup R_{PU}			
C(bus) pF	1kΩ	2.2kΩ	4kΩ	7kΩ
10-50	≅8mA	≅4mA	N/A	N/A
10-90	≅8mA	N/A	N/A	N/A
10-150	N/A	N/A	N/A	N/A
10-200	N/A	N/A	N/A	N/A

I²C FM (400kHz Max)	I²C drive strength (I_{OL}) selection			
	I²C bus pullup R_{PU}			
C(bus) pF	1kΩ	2.2kΩ	4kΩ	7kΩ
10-50	≅8mA	≅4mA	≅2mA	N/A
10-90	≅8mA	≅4mA	N/A	N/A
10-150	≅8mA	≅8mA	N/A	N/A
10-200	≅8mA	N/A	N/A	N/A

I²C STD (100kHz Max)	I²C drive strength (I_{OL}) selection			
	I²C bus pullup R_{PU}			
C(bus) pF	1kΩ	2.2kΩ	4kΩ	7kΩ
10-50	≅8mA	≅4mA	≅2mA	≅1mA
10-90	≅8mA	≅4mA	≅2mA	≅1mA
10-150	≅8mA	≅4mA	≅2mA	≅2mA
10-200	≅8mA	≅4mA	≅2mA	≅2mA

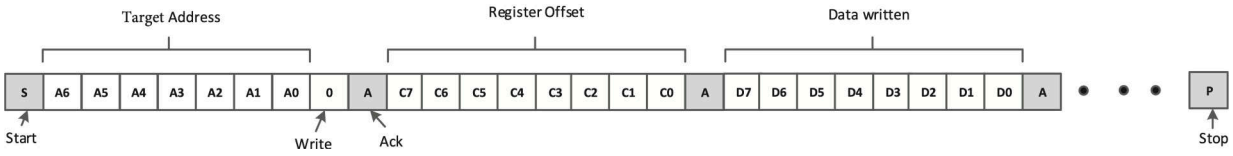


図 8-5. I²C Write with Data

Use this procedure to write data to TUSB2E221 I²C registers (refer to 図 8-5):

1. The host initiates a write operation by generating a start condition (S), followed by the TUSB2E221 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TUSB2E221 acknowledges the address cycle.
3. The host presents the register offset within the TUSB2E221 to be written, consisting of one byte of data, MSB-first.
4. The TUSB2E221 acknowledges the sub-address cycle.
5. The host presents the first byte of data to be written to the I²C register.
6. The TUSB2E221 acknowledges the byte transfer.
7. The host may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the TUSB2E221.
8. The host terminates the write operation by generating a stop condition (P).

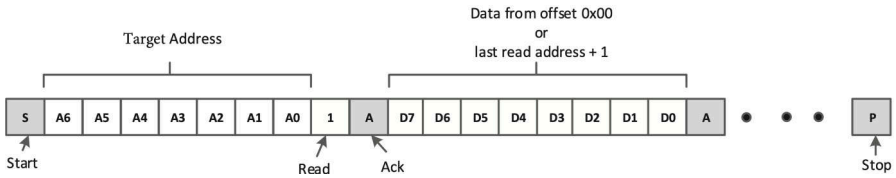


図 8-6. I²C Read Without Repeated Start

Use this procedure to read the TUSB2E221 I²C registers without a repeated Start (refer 図 8-6).

1. The host initiates a read operation by generating a start condition (S), followed by the TUSB2E221 7-bit address and a zero-value “W/R” bit to indicate a read cycle.
2. The TUSB2E221 acknowledges the 7-bit address cycle.
3. Following the acknowledge the host continues sending clock.
4. The TUSB2E221 transmit the contents of the memory registers MSB-first starting at register 00h or last read register offset+1. If a write to the I²C register occurred prior to the read, then the TUSB2E221 shall start at the register offset specified in the write.
5. The TUSB2E221 waits for either an acknowledge (ACK) or a not-acknowledge (NACK) from the host after each byte transfer; the I²C host acknowledges reception of each data byte transfer.
6. If an ACK is received, the TUSB2E221 transmits the next byte of data as long as host provides the clock. If a NAK is received, the TUSB2E221 stops providing data and waits for a stop condition (P).
7. The host terminates the write operation by generating a stop condition (P).

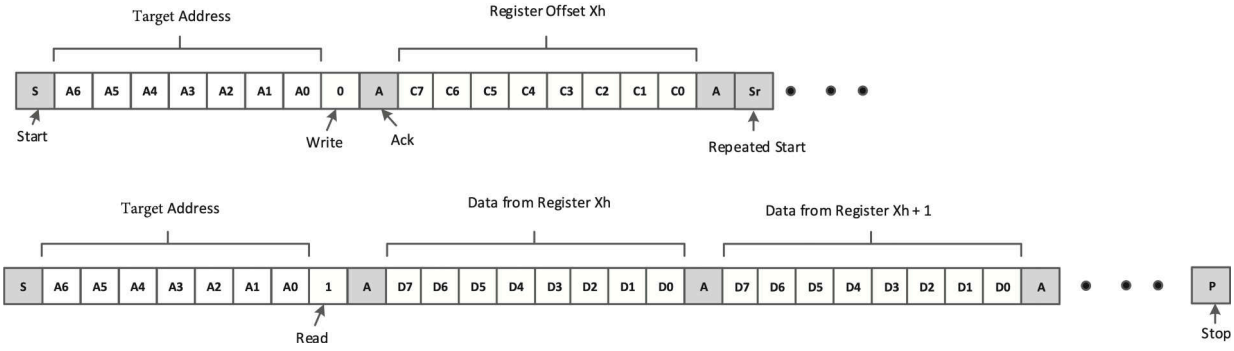


図 8-7. I²C Read with Repeated Start

Use this procedure to read the TUSB2E221 I2C registers with a repeated Start (refer 図 8-7).

1. The host initiates a read operation by generating a start condition (S), followed by the TUSB2E221 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TUSB2E221 acknowledges the 7-bit address cycle.
3. The host presents the register offset within the TUSB2E221 to be written, consisting of one byte of data, MSB-first.
4. The TUSB2E221 acknowledges the register offset cycle.
5. The host presents a repeated start condition (Sr).
6. The host initiates a read operation by generating a start condition (S), followed by the TUSB2E221 7-bit address and a one-value “W/R” bit to indicate a read cycle.
7. The TUSB2E221 acknowledges the 7-bit address cycle.
8. The TUSB2E221 transmit the contents of the memory registers MSB-first starting at the register offset.
9. The TUSB2E221 shall wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the host after each byte transfer; the I2C host acknowledges reception of each data byte transfer.
10. If an ACK is received, the TUSB2E221 transmits the next byte of data as long as host provides the clock. If a NAK is received, the TUSB2E221 stops providing data and waits for a stop condition (P).
11. The host terminates the read operation by generating a stop condition (P).

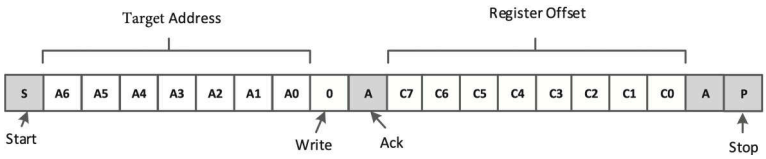


図 8-8. I2C Write Without Data

Use this procedure to set a starting sub-address for I2C reads (refer to 図 8-8).

1. The host initiates a write operation by generating a start condition (S), followed by the TUSB2E221 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TUSB2E221 acknowledges the address cycle.
3. The host presents the register offset within the TUSB2E221 to be written, consisting of one byte of data, MSB-first.
4. The TUSB2E221 acknowledges the register offset cycle.
5. The host terminates the write operation by generating a stop condition (P).

注

After initial power-up, if no register offset is included for the read procedure (refer to 図 8-6), then reads start at register offset 00h and continue byte by byte through the registers until the I2C host terminates the read operation. During a read operation, the TUSB2E221 auto-increments the I2C internal register address of the last byte transferred independent of whether or not an ACK was received from the I2C host.

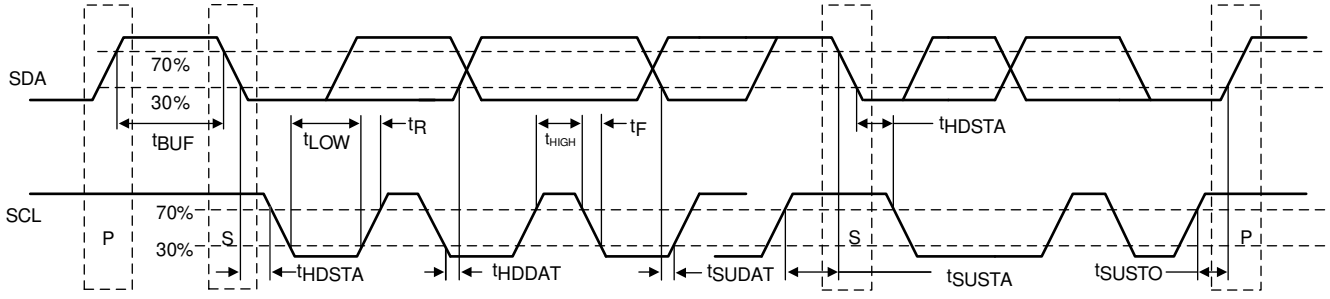


図 8-9. I2C Timing Diagram

8.5.2 Register Access Protocol (RAP)

Each repeater in the TUSB2E221 supports the register access protocol (RAP) over eUSB2 to allow access to the related registers. Only the registers associated with each repeater is accessible through RAP. Registers for the other repeater or the chip top level are not accessible through RAP.

RAP accessible registers are indicated with corresponding RAP addresses in the register map. Default value of a subset of the registers are factory programmable and are indicated in register map.

9 Register Map

9.1 TUSB2E221 Registers

表 9-1 lists the memory-mapped registers for the TUSB2E221 registers. All register offset addresses not listed in 表 9-1 should be considered as reserved locations and the register contents should not be modified.

表 9-1. TUSB2E221 Registers

Offset	Acronym	Register Name	Section
0h	GPIO0_CONFIG	RAP Register for Port 0 (Write = 0h, Read = 30h)	Go
10h	LOPWR_N_UART_P0		Go
20h	CONFIG_PORT0	RAP Register for Port 0 (Write = 20h, Read = 10h)	Go
30h	U_TX_ADJUST_PORT0	RAP Register for Port 0 (Write = 30h, Read = 0h), Default through OTP	Go
31h	U_HS_TX_PRE_EMPHASIS_P0	RAP Register for Port 0 (Write = 31h, Read = 1h), Default through OTP	Go
32h	U_RX_ADJUST_PORT0	RAP Register for Port 0 (Write = 32h, Read = 2h), Default through OTP	Go
33h	U_DISCONNECT_SQUELCH_PORT0	RAP Register for Port 0 (Write = 33h, Read = 3h), Default through OTP	Go
37h	E_HS_TX_PRE_EMPHASIS_P0	RAP Register for Port 0 (Write = 37h, Read = 7h), Default through OTP	Go
38h	E_TX_ADJUST_PORT0	RAP Register for Port 0 (Write = 38h, Read = 8h), Default through OTP	Go
39h	E_RX_ADJUST_PORT0	RAP Register for Port 0 (Write = 39h, Read = 9h), Default through OTP	Go
40h	GPIO1_CONFIG	RAP Register for Port 1 (Write = 0h, Read = 30h)	Go
50h	LOPWR_N_UART_P1		Go
60h	CONFIG_PORT1	RAP Register for Port 1 (Write = 20h, Read = 10h)	Go
70h	U_TX_ADJUST_PORT1	RAP Register for Port 1 (Write = 30h, Read = 0h), Default through OTP	Go
71h	U_HS_TX_PRE_EMPHASIS_P1	RAP Register for Port 1 (Write = 31h, Read = 1h), Default through OTP	Go
72h	U_RX_ADJUST_PORT1	RAP Register for Port 1 (Write = 32h, Read = 2h), Default through OTP	Go
73h	U_DISCONNECT_SQUELCH_PORT1	RAP Register for Port 1 (Write = 33h, Read = 3h), Default through OTP	Go
77h	E_HS_TX_PRE_EMPHASIS_P1	RAP Register for Port 1 (Write = 37h, Read = 7h), Default through OTP	Go
78h	E_TX_ADJUST_PORT1	RAP Register for Port 1 (Write = 38h, Read = 8h), Default through OTP	Go
79h	E_RX_ADJUST_PORT1	RAP Register for Port 1 (Write = 39h, Read = 9h), Default through OTP	Go
A3h	INT_STATUS_1		Go
A4h	INT_STATUS_2		Go
B0h	REV_ID		Go
B2h	GLOBAL_CONFIG		Go
B3h	INT_ENABLE_1		Go
B4h	INT_ENABLE_2		Go

Complex bit access types are encoded to fit into small table cells. 表 9-2 shows the codes that are used for access types in this section.

表 9-2. TUSB2E221 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
WtoPH	W toPH	Write Pulse high
Reset or Default Value		
-n		Value after reset or the default value

9.1.1 GPIO0_CONFIG Register (Offset = 0h) [Reset = 00h]

GPIO0_CONFIG is shown in 表 9-3.

Return to the Summary Table.

表 9-3. GPIO0_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO0_OD_PP	R/W	0h	GPIO0 Output Type 0h = Open drain output 1h = Push pull output
6	GPIO0_IN_TRIGGER_TYPE	R/W	0h	GPIO0 Input Trigger Type for Interrupt 0h = Edge trigger input 1h = Level trigger input (INT output will reflect the input level state)
5	GPIO0_DIRECTION	R/W	0h	GPIO0 Direction 0h = Input 1h = Output
4	GPIO0_INPUT_STATUS	RH	0h	Logical Value of GPIO0 pin input (0=Low, 1=High) 0h = Input is low 1h = Input is high

表 9-3. GPIO0_CONFIG Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
3-0	GPIO0_OUTPUT_SELECT	R/W	0h	GPIO0 Output Selection 0h = Remote Wakeup - host repeater is receiving remote wake but has not seen start of resume 1h = USB disconnect - host repeater is actively forwarding LS/FS disconnect. 2h = USB_HS_Unsquelched - host repeater in L0 seeing USB HS or in reset seeing Chirp 3h = PVTB - HOST repeater is actively transmitting ESE1 due to HS disconnect. 4h = DEFAULT - waiting to be configured host/peripheral 5h = HOST - in host repeater mode 6h = PERIPHERAL - in peripheral repeater mode 7h = CONNECTED - repeater is connected, connection seen acknowledged by start of reset 8h = RESET - reset in progress, reset is detected is high, L0 is low 9h = L0 - fully configured and repeating data, keep-alive and reset/ disconnect Ah = L1 -device has received CM.FS/CM.L1,has stopped repeating and is waiting for wake/resume Bh = L2 - device has received CM.L2, has stopped repeating and is waiting for wake/resume. Ch = GPIO0_HS_TEST - in host repeater in L0 mode, received CM.TEST Dh = HIGH_OUTPUT - output is forced static high Eh = LOW_OUTPUT - output is forced static low Fh = OVP - over voltage (DP/DN voltage > VOVP_TH) detected on the USB DP/DN

9.1.2 LOPWR_N_UART_P0 Register (Offset = 10h) [Reset = 50h]

LOPWR_N_UART_P0 is shown in 表 9-4.

Return to the Summary Table.

表 9-4. LOPWR_N_UART_P0 Register Field Descriptions

Bit	Field	Type	Reset	Default from OTP (Y/N)	Description
7	RESERVED	R	0h		Reserved
6	HOST_FRAME_LP_EN_P0	RH/W	1h	Y	Host repeater frame-based Low Power enable Default through OTP 0h = Not Enabled 1h = Enabled
5	DEVICE_FRAME_LP_EN_P0	RH/W	0h	Y	Peripheral repeater frame-based Low Power enable Default through OTP 0h = Not Enabled 1h = Enabled
4	IDLE_LP_EN_P0	RH/W	1h	Y	enable response-based Low Power mode Default through OTP 0h = Not Enabled 1h = Enabled
3	UART_GPI_POLARITY_P0	RH/W	0h	Y	Select polarity of pin to enable UART mode Default through OTP 0h = GPIO0 pin enables UART mode when 1 1h = GPIO0 pin enables UART mode when 0
2	UART_DP_PU_EN_P0	RH/W	0h	Y	Select whether DP pullup is enabled during UART mode Default through OTP 0h = disable DP pullup during UART mode 1h = enable DP pullup during UART mode

表 9-4. LOPWR_N_UART_P0 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Default from OTP (Y/N)	Description
1	UART_en_by_reg_not_pin_P0	RH/W	0h	Y	Select whether UART mode is enabled by register or by GPIO0 pin Default through OTP 0h = select UART_mode_en_P0 register to enable UART mode 1h = select GPIO0 pin to enable UART mode
0	UART_mode_en_P0	RH/W	0h	Y	If GPIO0 is not selected to enable UART mode, this register will enable it. Default through OTP 0h = disable UART mode between eUSB2 and USB 2.0 pins 1h = enable UART mode between eUSB2 and USB 2.0 pins

9.1.3 CONFIG_PORT0 Register (Offset = 20h) [Reset = 00h]

CONFIG_PORT0 is shown in 表 9-5.

Return to the Summary Table.

表 9-5. CONFIG_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	Reserved
6-5	RESERVED	R	0h	Reserved
4-3	HOST_DEVICE_P0	RH	0h	Port0 is configured as a Host repeater or a Device repeater 0h = Not configured 1h = Host repeater 2h = Device repeater 3h = Reserved
2-1	RESERVED	R	0h	Reserved
0	CDP_2_STATUS_P0	RH	0h	Primary detection detected on port0 if CDP_2_EN_P0=1 0h = CDP primary detection detected 1h = CDP primary detection not detected

9.1.4 U_TX_ADJUST_PORT0 Register (Offset = 30h) [Reset = 77h]

U_TX_ADJUST_PORT0 is shown in 表 9-6.

Return to the Summary Table.

Hardware default value can be overridden through factory programmable OTP for this register.

表 9-6. U_TX_ADJUST_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Default from OTP (Y/N)	Description
7-6	U_HS_TERM_P0	RH/W	1h	Y	Z_{HSTERM} adjustment USB HS Termination Adjustment (-5% to 10% in 5% steps) Default through OTP 0h = 42.75 Ω (typical) 1h = 45 Ω (typical) (hw default) 2h = 47.25 Ω (typical) 3h = 49.5 Ω (typical)

表 9-6. U_TX_ADJUST_PORT0 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Default from OTP (Y/N)	Description
5-4	U_HS_TX_SLEW_RATE_P0	RH/W	3h	Y	T_{HSR} adjustment USB HS TX Slew Rate (350ps - 575ps) Default through OTP 0h = 350ps (typical) 1h = 425ps (typical) 2h = 500ps (typical) 3h = 575ps (typical) (hw default)
3-0	U_HS_TX_AMPLITUDE_P0	RH/W	7h	Y	V_{EHSOD} adjustment USB HS TX Amplitude, measured p-p USB 2.0 spec nominal will be 800mV (-7.5% to 30% in 2.5% steps) Default through OTP This setting has no effect on amplitude during chirp J (VCHIRPJ) or chirp K (VCHIRPK) 0h = 800mV - 7.5% , 740mV (typical) 1h = 800mV - 5.0% , 760mV (typical) 2h = 800mV - 2.5% , 780mV (typical) 3h = 800mV (USB 2.0 spec nominal) , 800mV (typical) (hw default) 4h = 800mV + 2.5% , 820mV (typical) 5h = 800mV + 5.0% , 840mV (typical) 6h = 800mV + 7.5% , 860mV (typical) 7h = 800mV + 10% , 880mV (typical) 8h = 800mV + 12.5% , 900mV (typical) 9h = 800mV + 15% , 920mV (typical) Ah = 800mV + 17.5% , 940mV (typical) Bh = 800mV + 20% , 960mV (typical) Ch = 800mV + 22.5% , 980mV (typical) Dh = 800mV + 25% , 1000mV (typical) Eh = 800mV + 27.5% , 1020mV (typical) Fh = 800mV + 30% , 1040mV (typical)

9.1.5 U_HS_TX_PRE_EMPHASIS_P0 Register (Offset = 31h) [Reset = 39h]

U_HS_TX_PRE_EMPHASIS_P0 is shown in 表 9-7.

Return to the Summary Table.

Hardware default value can be overridden through factory programmable OTP for this register.

表 9-7. U_HS_TX_PRE_EMPHASIS_P0 Register Field Descriptions

Bit	Field	Type	Reset	Default from OTP (Y/N)	Description
7	RESERVED	RH/W	0h		Reserved
6	CDP_1_EN_P0	RH/W	0h	Y	Enables CDP using method 1 on port0 Default through OTP 0h = CDP using method 1 not enabled (hw default) 1h = CDP using method 1 enabled
5-4	U_HS_TX_PE_WIDTH_P0	RH/W	3h	Y	$U2_{TXPE\_UI}$ Adjustment USB HS TX Pre-emphasis Width Default through OTP 0h = 0.35 UI (typical) 1h = 0.45 UI (typical) 2h = 0.55 UI (typical) 3h = 0.65 UI (typical) (hw default)

表 9-7. U_HS_TX_PRE_EMPHASIS_P0 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Default from OTP (Y/N)	Description
3	U_HS_TX_PE_ENABLE_P0	RH/W	1h	Y	USB HS TX Pre-emphasis Enable Default through OTP PE is disabled during chirp J (VCHIRPJ) or chirp K (VCHIRPK) 0h = Disabled (hw default) 1h = Enabled
2-0	U_HS_TX_PRE_EMPHASIS_P0	RH/W	1h	Y	U2$_{TXPE}$ Adjustment USB HS TX Pre-emphasis (0.5dB-4.0dB) Default through OTP PE is disabled during chirp J (VCHIRPJ) or chirp K (VCHIRPK) 0h = 0.5dB (typical) (hw default) 1h = 0.9dB (typical) 2h = 1.2dB (typical) 3h = 1.7dB (typical) 4h = 2.1dB (typical) 5h = 2.5dB (typical) 6h = 3.2dB (typical) 7h = 4.0dB (typical)

9.1.6 U_RX_ADJUST_PORT0 Register (Offset = 32h) [Reset = D2h]

U_RX_ADJUST_PORT0 is shown in 表 9-8.

Return to the Summary Table.

Hardware default value can be overridden through factory programmable OTP for this register.

表 9-8. U_RX_ADJUST_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Default from OTP (Y/N)	Description
7-6	i2c_ds_config	RH/W	3h	Y	I2C open drain output drive strength selection This is intended to be set through I2C. (The pin can be set through RAP only if repeater 0 is enabled) Default through OTP 0h = ~1mA (typical) 1h = ~2mA (typical) 2h = ~4mA (typical) 3h = ~8mA (typical) (hw default)
5-4	RESERVED	RH/W	1h		Reserved
3	RESERVED	RH/W	0h		Reserved
2-0	U_EQ_P0	RH/W	2h	Y	EQ$_{UHS}$ Adjustment USB RX Equalizer Control (0-3.35dB) Default through OTP 0h = 0.06dB (typical) (hw default) 1h = 0.58dB (typical) 2h = 1.09dB (typical) 3h = 1.56dB (typical) 4h = 2.26dB (typical) 5h = 2.67dB (typical) 6h = 3.03dB (typical) 7h = 3.35dB (typical)

9.1.7 U_DISCONNECT_SQUELCH_PORT0 Register (Offset = 33h) [Reset = 74h]

U_DISCONNECT_SQUELCH_PORT0 is shown in 表 9-9.

Return to the Summary Table.

Hardware default value can be overridden through factory programmable OTP for this register.

表 9-9. U_DISCONNECT_SQUELCH_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Default from OTP (Y/N)	Description
7-4	U_DISCONNECT_THRESHOLD_P0	RH/W	7h	Y	V_{HSDSC} Adjustment USB Minimum HS HOST Disconnect Threshold (0% to +57% in ~3.7% steps) Default through OTP 0h = 525mV (minimum), 0% (hw default) 1h = 545mV (minimum), +4% 2h = 565mV (minimum), +8% 3h = 585mV (minimum), +11% 4h = 605mV (minimum), +15% 5h = 625mV (minimum), +19% 6h = 645mV (minimum), +23% 7h = 665mV (minimum), +27% 8h = 685mV (minimum), +31% 9h = 705mV (minimum), +34% Ah = 725mV (minimum), +38% Bh = 745mV (minimum), +42% Ch = 765mV (minimum), +46% Dh = 785mV (minimum), +50% Eh = 805mV (minimum), +53% Fh = 825mV (minimum), +57%
3	RESERVED	RH/W	0h		Reserved
2-0	U_SQUELCH_THRESHOLD_P0	RH/W	4h	Y	V_{HSSQ} Adjustment USB Squelch Detection Min Threshold (+30% to -15% in ~6.5% steps) Default through OTP 0h = 130mV (minimum), +30% 1h = 124mV (minimum), +24% 2h = 117mV (minimum), +17% 3h = 111mV (minimum), +11% 4h = 104mV (minimum), +4% (hw default) 5h = 98mV (minimum), -2% 6h = 91mV (minimum), -9% 7h = 85mV (minimum), -15%

9.1.8 E_HS_TX_PRE_EMPHASIS_P0 Register (Offset = 37h) [Reset = 40h]

E_HS_TX_PRE_EMPHASIS_P0 is shown in 表 9-10.

Return to the Summary Table.

Hardware default value can be overridden through factory programmable OTP for this register.

表 9-10. E_HS_TX_PRE_EMPHASIS_P0 Register Field Descriptions

Bit	Field	Type	Reset	Default from OTP (Y/N)	Description
7-5	E_HS_TX_PRE_EMPHASIS_P0	RH/W	2h	Y	E_{TXPE} adjustment eUSB2 HS TX Pre-emphasis 0dB-3.86dB Default through OTP 0h = 0dB (typical) (hw default) 1h = 0.67dB (typical) 2h = 1.29dB (typical) 3h = 1.87dB (typical) 4h = 2.41dB (typical) 5h = 2.92dB (typical) 6h = 3.41dB (typical) 7h = 3.86dB (typical)
4-3	E_HS_TX_PE_WIDTH_P0	RH/W	0h	Y	E_{TXPE_UI} adjustment eUSB2 HS TX Pre-emphasis Width Default through OTP 0h = 0.35 UI (typical) (hw default) 1h = 0.45 UI (typical) 2h = 0.55 UI (typical) 3h = 0.65 UI (typical)
2	RESERVED	RH/W	0h		Reserved
1	RESERVED	RH/W	0h		Reserved
0	RESERVED	R	0h		

9.1.9 E_TX_ADJUST_PORT0 Register (Offset = 38h) [Reset = 0Ch]

E_TX_ADJUST_PORT0 is shown in 表 9-11.

Return to the Summary Table.

Hardware default value can be overridden through factory programmable OTP for this register.

表 9-11. E_TX_ADJUST_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Default from OTP (Y/N)	Description
7-6	RESERVED	RH/W	0h		Reserved
5	RESERVED	RH/W	0h		Reserved
4-3	E_HS_TX_SLEW_RATE_P0	RH/W	1h	Y	T_{EHSRF} Adjustment eUSB2 HS TX Slew Rate 390ps - 540ps Default through OTP 0h = 390ps (typical) 1h = 440ps (typical) (hw default) 2h = 490ps (typical) 3h = 540ps (typical)
2-0	E_HS_TX_AMPLITUDE_P0	RH/W	4h	Y	V_{EHSOD} Adjustment eUSB2 HS TX Amplitude 360mV to 500mV (p-2-p) Default through OTP 0h = 360mV (typical) 1h = 380mV (typical) 2h = 400mV (typical) 3h = 420mV (typical) (hw default) 4h = 440mV (typical) 5h = 460mV (typical) 6h = 480mV (typical) 7h = 500mV (typical)

9.1.10 E_RX_ADJUST_PORT0 Register (Offset = 39h) [Reset = 62h]

E_RX_ADJUST_PORT0 is shown in 表 9-12.

Return to the Summary Table.

Hardware default value can be overridden through factory programmable OTP for this register.

表 9-12. E_RX_ADJUST_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Default from OTP (Y/N)	Description
7	RESERVED	RH/W	0h		Reserved
6-4	E_SQUELCH_THRESHOLD_P0	RH/W	6h	Y	V_{EHSSQ} Adjustment eUSB2 HS Squelch Detection Threshold Default through OTP 0h = 104mV (typical) 1h = 101mV (typical) 2h = 98mV (typical) 3h = 90mV (typical) 4h = 81mV (typical) 5h = 73mV (typical) 6h = 67mV (typical) (hw default) 7h = 60mV (typical)
3-0	E_EQ_P0	RH/W	2h	Y	EQ_{EHS} Adjustment eUSB2 RX Equalizer Control Default through OTP 0h = 0.34dB (typical) (hw default) 1h = 0.71dB (typical) 2h = 1.02dB (typical) 3h = 1.36dB (typical) 4h = 1.64dB (typical) 5h = 1.94dB (typical) 6h = 2.19dB (typical) 7h = 2.45dB (typical) 8h = 2.69dB (typical) 9h = 2.93dB (typical) Ah = 3.13dB (typical) Bh = 3.35dB (typical) Ch = 3.53dB (typical) Dh = 3.72dB (typical) Eh = 3.89dB (typical) Fh = 4.07dB (typical)

9.1.11 GPIO1_CONFIG Register (Offset = 40h) [Reset = 00h]

GPIO1_CONFIG is shown in 表 9-13.

Return to the Summary Table.

表 9-13. GPIO1_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO1_OD_PP	R/W	0h	GPIO1 Output Type selection 0h = Open drain output 1h = Push pull output
6	GPIO1_IN_TRIGGER_TYPE	R/W	0h	GPIO1 Input Trigger Type selection for Interrupt 0h = Edge trigger input 1h = Level trigger input (INT output will reflect the input level state)
5	GPIO1_DIRECTION	R/W	0h	GPIO1 Direction selection 0h = Input 1h = Output

表 9-13. GPIO1_CONFIG Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
4	GPIO1_INPUT_STATUS	RH	0h	Logical Value of GPIO1 pin input status (0=Low, 1=High) 0h = Input is low 1h = Input is high
3-0	GPIO1_OUTPUT_SELECT	R/W	0h	GPIO1 Output Selection 0h = Remote Wakeup - host repeater is receiving remote wake but has not seen start of resume 1h = USB disconnect - host repeater is actively forwarding LS/FS disconnect. 2h = USB_HS_Unsquelched - host repeater in L0 seeing USB HS or in reset seeing Chirp 3h = PVTB - HOST repeater is actively transmitting ESE1 due to HS disconnect. 4h = DEFAULT - waiting to be configured host/peripheral 5h = HOST - in host repeater mode 6h = PERIPHERAL - in peripheral repeater mode 7h = CONNECTED - repeater is connected, connection seen acknowledged by start of reset 8h = RESET - reset in progress, reset is detected is high, L0 is low 9h = L0 - fully configured and repeating data, keep-alive and reset/ disconnect Ah = L1 -device has received CM.FS/CM.L1,has stopped repeating and is waiting for wake/resume Bh = L2 - device has received CM.L2, has stopped repeating and is waiting for wake/resume. Ch = GPIO1_HS_TEST - in host repeater in L0 mode, received CM.TEST Dh = HIGH_OUTPUT - output is forced static high Eh = LOW_OUTPUT - output is forced static low Fh = OVP - over voltage (DP/DN voltage > VOVP_TH) detected on the USB DP/DN

9.1.12 LOPWR_N_UART_P1 Register (Offset = 50h) [Reset = 50h]

LOPWR_N_UART_P1 is shown in 表 9-14.

Return to the Summary Table.

表 9-14. LOPWR_N_UART_P1 Register Field Descriptions

Bit	Field	Type	Reset	Default from OTP (Y/N)	Description
7	RESERVED	R	0h		
6	HOST_FRAME_LP_EN_P1	RH/W	1h	Y	Host repeater frame-based Low Power enable Default through OTP 0h = Not Enabled 1h = Enabled
5	DEVICE_FRAME_LP_EN_P1	RH/W	0h	Y	Peripheral repeater frame-based Low Power enable Default through OTP 0h = Not Enabled 1h = Enabled
4	IDLE_LP_EN_P1	RH/W	1h	Y	enable response-based Low Power mode Default through OTP 0h = Not Enabled 1h = Enabled
3	UART_GPI_POLARITY_P1	RH/W	0h	Y	Select polarity of pin to enable UART mode Default through OTP 0h = GPIO1 pin enables UART mode when 1 1h = GPIO1 pin enables UART mode when 0

表 9-14. LOPWR_N_UART_P1 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Default from OTP (Y/N)	Description
2	UART_DP_PU_EN_P1	RH/W	0h	Y	Select whether DP pullup is enabled during UART mode Default through OTP 0h = disable DP pullup during UART mode 1h = enable DP pullup during UART mode
1	UART_en_by_reg_not_pin_P1	RH/W	0h	Y	Select whether UART mode is enabled by register or by GPIO1 pin Default through OTP 0h = select UART_mode_en_P1 register to enable UART mode 1h = select GPIO1 pin to enable UART mode
0	UART_mode_en_P1	RH/W	0h	Y	If GPIO1 is not selected to enable UART mode, this register will enable it. Default through OTP 0h = disable UART mode between eUSB2 and USB 2.0 pins 1h = enable UART mode between eUSB2 and USB 2.0 pins

9.1.13 CONFIG_PORT1 Register (Offset = 60h) [Reset = 00h]

CONFIG_PORT1 is shown in 表 9-15.

Return to the Summary Table.

表 9-15. CONFIG_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	Reserved
6-5	RESERVED	R	0h	Reserved
4-3	HOST_DEVICE_P1	RH	0h	Port1 is configured as a Host repeater or a Device repeater 0h = Not configured 1h = Host repeater 2h = Device repeater 3h = Reserved
2-1	RESERVED	R	0h	Reserved
0	CDP_2_STATUS_P1	RH	0h	Primary detection detected on port1 if CDP_2_EN_P1=1 0h = CDP primary detection detected 1h = CDP primary detection not detected

9.1.14 U_TX_ADJUST_PORT1 Register (Offset = 70h) [Reset = 77h]

U_TX_ADJUST_PORT1 is shown in 表 9-16.

Return to the Summary Table.

Hardware default value can be overridden through factory programmable OTP for this register.

表 9-16. U_TX_ADJUST_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Default from OTP (Y/N)	Description
7-6	U_HS_TERM_P1	RH/W	1h	Y	Z_{HSTERM} adjustment USB HS Termination Adjustment (-5% to 10% in 5% steps) Default through OTP 0h = 42.75 Ω (typical) 1h = 45 Ω (typical) (hw default) 2h = 47.25 Ω (typical) 3h = 49.5 Ω (typical)

表 9-16. U_TX_ADJUST_PORT1 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Default from OTP (Y/N)	Description
5-4	U_HS_TX_SLEW_RATE_P1	RH/W	3h	Y	T_{HSR} adjustment USB HS TX Slew Rate (350ps - 575ps) Default through OTP 0h = 350ps (typical) 1h = 425ps (typical) 2h = 500ps (typical) 3h = 575ps (typical) (hw default)
3-0	U_HS_TX_AMPLITUDE_P1	RH/W	7h	Y	V_{EHSOD} adjustment USB HS TX Amplitude, measured p-p USB 2.0 spec nominal will be 800mV (-7.5% to 30% in 2.5% steps) Default through OTP This setting has no effect on amplitude during chirp J (VCHIRPJ) or chirp K (VCHIRPK) 0h = 800mV - 7.5% , 740mV (typical) 1h = 800mV - 5.0% , 760mV (typical) 2h = 800mV - 2.5% , 780mV (typical) 3h = 800mV (USB 2.0 spec nominal) , 800mV (typical) (hw default) 4h = 800mV + 2.5% , 820mV (typical) 5h = 800mV + 5.0% , 840mV (typical) 6h = 800mV + 7.5% , 860mV (typical) 7h = 800mV + 10% , 880mV (typical) 8h = 800mV + 12.5% , 900mV (typical) 9h = 800mV + 15% , 920mV (typical) Ah = 800mV + 17.5% , 940mV (typical) Bh = 800mV + 20% , 960mV (typical) Ch = 800mV + 22.5% , 980mV (typical) Dh = 800mV + 25% , 1000mV (typical) Eh = 800mV + 27.5% , 1020mV (typical) Fh = 800mV + 30% , 1040mV (typical)

9.1.15 U_HS_TX_PRE_EMPHASIS_P1 Register (Offset = 71h) [Reset = 39h]

U_HS_TX_PRE_EMPHASIS_P1 is shown in 表 9-17.

Return to the Summary Table.

Hardware default value can be overridden through factory programmable OTP for this register.

表 9-17. U_HS_TX_PRE_EMPHASIS_P1 Register Field Descriptions

Bit	Field	Type	Reset	Default from OTP (Y/N)	Description
7	RESERVED	RH/W	0h		Reserved
6	CDP_1_EN_P1	RH/W	0h	Y	Enables CDP using method 1 on port1 Default through OTP 0h = CDP using method 1 not enabled (hw default) 1h = CDP using method 1 enabled
5-4	U_HS_TX_PE_WIDTH_P1	RH/W	3h	Y	$U2_{TXPE\_UI}$ USB HS TX Pre-emphasis Width Default through OTP 0h = 0.35 UI (typical) 1h = 0.45 UI (typical) 2h = 0.55 UI (typical) 3h = 0.65 UI (typical) (hw default)

表 9-17. U_HS_TX_PRE_EMPHASIS_P1 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Default from OTP (Y/N)	Description
3	U_HS_TX_PE_ENABLE_P1	RH/W	1h	Y	USB HS TX Pre-emphasis Enable Default through OTP PE is disabled during chirp J (VCHIRPJ) or chirp K (VCHIRPK) 0h = Disabled (hw default) 1h = Enabled
2-0	U_HS_TX_PRE_EMPHASIS_P1	RH/W	1h	Y	$U2_{TXPE}$ USB HS TX Pre-emphasis (0.5dB-4.0dB) Default through OTP PE is disabled during chirp J (VCHIRPJ) or chirp K (VCHIRPK) 0h = 0.5dB (typical) (hw default) 1h = 0.9dB (typical) 2h = 1.2dB (typical) 3h = 1.7dB (typical) 4h = 2.1dB (typical) 5h = 2.5dB (typical) 6h = 3.2dB (typical) 7h = 4.0dB (typical)

9.1.16 U_RX_ADJUST_PORT1 Register (Offset = 72h) [Reset = 92h]

U_RX_ADJUST_PORT1 is shown in 表 9-18.

Return to the Summary Table.

Hardware default value can be overridden through factory programmable OTP for this register.

表 9-18. U_RX_ADJUST_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Default from OTP (Y/N)	Description
7-6	gpio_ds_config	RH/W	2h	Y	GPIOx and INT open drain output drive strength selection This is intended to be set through I2C. (The pin can be set through RAP only if repeater 1 is enabled) Default through OTP 0h = ~1mA (typical) 1h = ~2mA (typical) 2h = ~4mA (typical) (hw default) 3h = ~8mA (typical)
5-4	RESERVED	RH/W	1h		Reserved
3	RESERVED	RH/W	0h		Reserved
2-0	U_EQ_P1	RH/W	2h	Y	EQ_{UHS} Adjustment USB RX Equalizer Control (0-3.35dB) Default through OTP 0h = 0.06dB (typical) (hw default) 1h = 0.58dB (typical) 2h = 1.09dB (typical) 3h = 1.56dB (typical) 4h = 2.26dB (typical) 5h = 2.67dB (typical) 6h = 3.03dB (typical) 7h = 3.35dB (typical)

9.1.17 U_DISCONNECT_SQUELCH_PORT1 Register (Offset = 73h) [Reset = 74h]

U_DISCONNECT_SQUELCH_PORT1 is shown in 表 9-19.

Return to the Summary Table.

Hardware default value can be overridden through factory programmable OTP for this register.

表 9-19. U_DISCONNECT_SQUELCH_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Default from OTP (Y/N)	Description
7-4	U_DISCONNECT_THRESHOLD_P1	RH/W	7h	Y	V_{HSDSC} adjustment USB Minimum HS HOST Disconnect Threshold (0% to +57% in ~3.7% steps) Default through OTP 0h = 525mV (minimum), 0% (hw default) 1h = 545mV (minimum), +4% 2h = 565mV (minimum), +8% 3h = 585mV (minimum), +11% 4h = 605mV (minimum), +15% 5h = 625mV (minimum), +19% 6h = 645mV (minimum), +23% 7h = 665mV (minimum), +27% 8h = 685mV (minimum), +31% 9h = 705mV (minimum), +34% Ah = 725mV (minimum), +38% Bh = 745mV (minimum), +42% Ch = 765mV (minimum), +46% Dh = 785mV (minimum), +50% Eh = 805mV (minimum), +53% Fh = 825mV (minimum), +57%
3	RESERVED	RH/W	0h		Reserved
2-0	U_SQUELCH_THRESHOLD_P1	RH/W	4h	Y	V_{HSSQ} Adjustment USB Squelch Detection Min Threshold (+30% to -15% in ~6.5% steps) Default through OTP 0h = 130mV (minimum), +30% 1h = 124mV (minimum), +24% 2h = 117mV (minimum), +17% 3h = 111mV (minimum), +11% 4h = 104mV (minimum), +4% (hw default) 5h = 98mV (minimum), -2% 6h = 91mV (minimum), -9% 7h = 85mV (minimum), -15%

9.1.18 E_HS_TX_PRE_EMPHASIS_P1 Register (Offset = 77h) [Reset = 40h]

E_HS_TX_PRE_EMPHASIS_P1 is shown in 表 9-20.

Return to the Summary Table.

Hardware default value can be overridden through factory programmable OTP for this register.

表 9-20. E_HS_TX_PRE_EMPHASIS_P1 Register Field Descriptions

Bit	Field	Type	Reset	Default from OTP (Y/N)	Description
7-5	E_HS_TX_PRE_EMPHASIS_P1	RH/W	2h	Y	E_{TXPE} adjustment eUSB2 HS TX Pre-emphasis 0dB-3.86dB Default through OTP 0h = 0dB (typical) (hw default) 1h = 0.67dB (typical) 2h = 1.29dB (typical) 3h = 1.87dB (typical) 4h = 2.41dB (typical) 5h = 2.92dB (typical) 6h = 3.41dB (typical) 7h = 3.86dB (typical)
4-3	E_HS_TX_PE_WIDTH_P1	RH/W	0h	Y	E_{TXPE_UI} adjustment eUSB2 HS TX Pre-emphasis Width Default through OTP 0h = 0.35 UI (typical) (hw default) 1h = 0.45 UI (typical) 2h = 0.55 UI (typical) 3h = 0.65 UI (typical)
2	RESERVED	RH/W	0h		Reserved
1	RESERVED	RH/W	0h		Reserved
0	RESERVED	RH/W	0h		Reserved
0	RESERVED	RH/W	0h		Reserved

9.1.19 E_TX_ADJUST_PORT1 Register (Offset = 78h) [Reset = 0Ch]

E_TX_ADJUST_PORT1 is shown in 表 9-21.

Return to the Summary Table.

Hardware default value can be overridden through factory programmable OTP for this register.

表 9-21. E_TX_ADJUST_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Default from OTP (Y/N)	Description
7-6	RESERVED	RH/W	0h		Reserved
5	RESERVED	RH/W	0h		Reserved
4-3	E_HS_TX_SLEW_RATE_P1	RH/W	1h	Y	T_{EHSRF} Adjustment eUSB2 HS TX Slew Rate 390ps - 540ps Default through OTP 0h = 390ps (typical) 1h = 440ps (typical) (hw default) 2h = 490ps (typical) 3h = 540ps (typical)
2-0	E_HS_TX_AMPLITUDE_P1	RH/W	4h	Y	V_{EHSOD} Adjustment eUSB2 HS TX Amplitude 360mV to 500mV (p-2-p) Default through OTP 0h = 360mV (typical) 1h = 380mV (typical) 2h = 400mV (typical) 3h = 420mV (typical) (hw default) 4h = 440mV (typical) 5h = 460mV (typical) 6h = 480mV (typical) 7h = 500mV (typical)

9.1.20 E_RX_ADJUST_PORT1 Register (Offset = 79h) [Reset = 62h]

E_RX_ADJUST_PORT1 is shown in 表 9-22.

Return to the Summary Table.

Hardware default value can be overridden through factory programmable OTP for this register.

表 9-22. E_RX_ADJUST_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Default from OTP (Y/N)	Description
7	RESERVED	RH/W	0h		Reserved
6-4	E_SQUELCH_THRESHOLD_P1	RH/W	6h	Y	V_{EHSSQ} Adjustment eUSB2 HS Squelch Detection Threshold Default through OTP 0h = 104mV (typical) 1h = 101mV (typical) 2h = 98mV (typical) 3h = 90mV (typical) 4h = 81mV (typical) 5h = 73mV (typical) 6h = 67mV (typical) (hw default) 7h = 60mV (typical)
3-0	E_EQ_P1	RH/W	2h	Y	EQ_{EHS} Adjustment eUSB2 RX Equalizer Control Default through OTP 0h = 0.34dB (typical) (hw default) 1h = 0.71dB (typical) 2h = 1.02dB (typical) 3h = 1.36dB (typical) 4h = 1.64dB (typical) 5h = 1.94dB (typical) 6h = 2.19dB (typical) 7h = 2.45dB (typical) 8h = 2.69dB (typical) 9h = 2.93dB (typical) Ah = 3.13dB (typical) Bh = 3.35dB (typical) Ch = 3.53dB (typical) Dh = 3.72dB (typical) Eh = 3.89dB (typical) Fh = 4.07dB (typical)

9.1.21 INT_STATUS_1 Register (Offset = A3h) [Reset = 00h]

INT_STATUS_1 is shown in 表 9-23.

Return to the Summary Table.

表 9-23. INT_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_GPIO1_RISING_EDGE	R/W1C	0h	GPIO1 Rising Edge enable 0h = No Interrupt 1h = Interrupt
6	INT_GPIO1_FALLING_EDGE	R/W1C	0h	GPIO1 Falling Edge enable 0h = No Interrupt 1h = Interrupt
5	INT_GPIO0_RISING_EDGE	R/W1C	0h	GPIO0 Rising Edge enable 0h = No Interrupt 1h = Interrupt

表 9-23. INT_STATUS_1 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
4	INT_GPIO0_FALLING_EDGE	R/W1C	0h	GPIO0 Falling Edge enable 0h = No Interrupt 1h = Interrupt
3	INT_USB_REMOTE_WAKE_P1	R/W1C	0h	Remote Wake Event Detect on USB Port 1 0h = No Interrupt 1h = Interrupt
2	INT_USB_DISCONNECT_P1	R/W1C	0h	Disconnect event has occurred on Port 1 0h = No Interrupt 1h = Interrupt
1	INT_USB_REMOTE_WAKE_P0	R/W1C	0h	Remote Wake Event Detect on USB Port 0 0h = No Interrupt 1h = Interrupt
0	INT_USB_DISCONNECT_P0	R/W1C	0h	Disconnect event has occurred on Port 0 0h = No Interrupt 1h = Interrupt

9.1.22 INT_STATUS_2 Register (Offset = A4h) [Reset = 00h]

INT_STATUS_2 is shown in 表 9-24.

Return to the Summary Table.

表 9-24. INT_STATUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3	INT_USB_DET_ATTACH_P1	R/W1C	0h	Device Attach event has occurred on Port 1 0h = No Interrupt 1h = Interrupt
2	INT_USB_DET_ATTACH_P0	R/W1C	0h	Device Attach event has occurred on Port 0 0h = No Interrupt 1h = Interrupt
1	INT_USB_OVP_P1	R/W1C	0h	Over voltage condition (DP/DN voltage > V_{OVP_TH}) has occurred port 1 0h = No Interrupt 1h = Interrupt
0	INT_USB_OVP_P0	R/W1C	0h	Over voltage condition (DP/DN voltage > V_{OVP_TH}) has occurred port 0 0h = No Interrupt 1h = Interrupt

9.1.23 REV_ID Register (Offset = B0h) [Reset = 03h]

REV_ID is shown in 表 9-25.

Return to the Summary Table.

表 9-25. REV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	REV_ID	RH	3h	Device revision. 4h = Device Revision 4

9.1.24 GLOBAL_CONFIG Register (Offset = B2h) [Reset = 00h]

GLOBAL_CONFIG is shown in 表 9-26.

Return to the Summary Table.

表 9-26. GLOBAL_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SOFT_RST	WtoPH	0h	Writing a 1 to this field is equivalent to pulsing RESETB low
6	DISABLE_P1	R/W	0h	DIsabled Mode Repeater 1 (I2C will remain Active) (If port is not disconnected, wait until disconnect event to disable the repeater) 0h = Repeater Enabled 1h = Repeater Disabled
5	DISABLE_P0	R/W	0h	Disabled Mode Repeater 0 (I2C will remain Active) (If port is not disconnected, wait until disconnect event to disable the repeater) 0h = Repeater Enabled 1h = Repeater Disabled
4	INT_OUT_TYPE	R/W	0h	INT Output Type INT output drive strength in open drain mode will be the same as GPIO setting 0h = Open Drain 1h = push pull
3	INT_POLARITY	R/W	0h	INT pin polarity in push-pull mode only (open drain mode will always be Active low) 0h = Active High (only for push-pull) 1h = Active Low (only for push-pull, open drain will always be active low)
2	RESERVED	R/W	0h	Reserved
1-0	RESERVED	R	0h	Reserved

9.1.25 INT_ENABLE_1 Register (Offset = B3h) [Reset = 00h]

INT_ENABLE_1 is shown in 表 9-27.

Return to the Summary Table.

表 9-27. INT_ENABLE_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO1_RISING_EDGE	R/W	0h	INT_GPIO1_RISING_EDGE enable. When GPIO1_IN_TRIGGER_TYPE = 0 (Edge), this enables interrupt on Rising Edge of GPIO1. When GPIO1_IN_TRIGGER_TYPE = 1 (Level), this enables Interrupt when GPIO1 = High. 0h = Not Enabled 1h = Enabled
6	GPIO1_FALLING_EDGE	R/W	0h	INT_GPIO1_FALLING_EDGE enable. When GPIO1_IN_TRIGGER_TYPE = 0 (Edge), this enables interrupt on Falling Edge of GPIO1. When GPIO1_IN_TRIGGER_TYPE = 1 (Level), this enables Interrupt when GPIO1 = Low. 0h = Not Enabled 1h = Enabled
5	GPIO0_RISING_EDGE	R/W	0h	INT_GPIO0_RISING_EDGE enable. When GPIO0_IN_TRIGGER_TYPE = 0 (Edge), this enables interrupt on Rising Edge of GPIO0. When GPIO0_IN_TRIGGER_TYPE = 1 (Level), this enables Interrupt when GPIO0 = High. 0h = Not Enabled 1h = Enabled

表 9-27. INT_ENABLE_1 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
4	GPIO0_FALLING_EDGE	R/W	0h	INT_GPIO0_FALLING_EDGE enable. When GPIO0_IN_TRIGGER_TYPE = 0 (Edge), this enables interrupt on Falling Edge of GPIO0. When GPIO0_IN_TRIGGER_TYPE = 1 (Level), this enables Interrupt when GPIO0 = Low. 0h = Not Enabled 1h = Enabled
3	USB_REMOTE_WAKE_P1	R/W	0h	INT_USB_REMOTE_WAKE_P1 enable. See L2 State Interrupt Modes 0h = Not Enabled 1h = Enabled
2	USB_DISCONNECT_P1	R/W	0h	INT_USB_DISCONNECT_P1 enable. See L2 State Interrupt Modes 0h = Not Enabled 1h = Enabled
1	USB_REMOTE_WAKE_P0	R/W	0h	INT_USB_REMOTE_WAKE_P0 enable. See L2 State Interrupt Modes 0h = Not Enabled 1h = Enabled
0	USB_DISCONNECT_P0	R/W	0h	INT_USB_DISCONNECT_P0 enable. See L2 State Interrupt Modes 0h = Not Enabled 1h = Enabled

9.1.26 INT_ENABLE_2 Register (Offset = B4h) [Reset = 00h]

INT_ENABLE_2 is shown in 表 9-28.

Return to the Summary Table.

表 9-28. INT_ENABLE_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_OVERRIDE_EN	R/W	0h	INT pin enable 0h = Not Enabled 1h = Enabled
6	INT_VALUE	R/W	0h	Value to drive on INT when INT_OVERRIDE=1 INT output pin indicates the interrupt assertion. The pin will follow the INT pin configuration. In open drain mode, the pin is active low to indicate interrupt assertion. In push-pull mode, the pin follows active low/high configuration to indicate INT assertion. 0h = output : interrupt not asserted 1h = output : interrupt asserted
5-4	RESERVED	R	0h	Reserved
3	USB_DETECT_ATTACH_P1	R/W	0h	INT_USB_DET_ATTACH_P1 enable. Enable device attach detection while eDSP is powered down 0h = Not Enabled 1h = Enabled
2	USB_DETECT_ATTACH_P0	R/W	0h	INT_USB_DET_ATTACH_P0 enable. Enable device attach detection while eDSP is powered down 0h = Not Enabled 1h = Enabled
1	USB_OVP_P1	R/W	0h	Over Voltage Port 1 interrupt enable 0h = Not Enabled 1h = Enabled

表 9-28. INT_ENABLE_2 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
0	USB_OVP_P0	R/W	0h	Over Voltage Port 0 interrupt enable 0h = Not Enabled 1h = Enabled

10 Applications and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The TUSB2E221 can be used in either HOST or Peripheral implementation. The mode is configured by the eUSB2 SoC.

10.2 Typical Application: Dual Port System

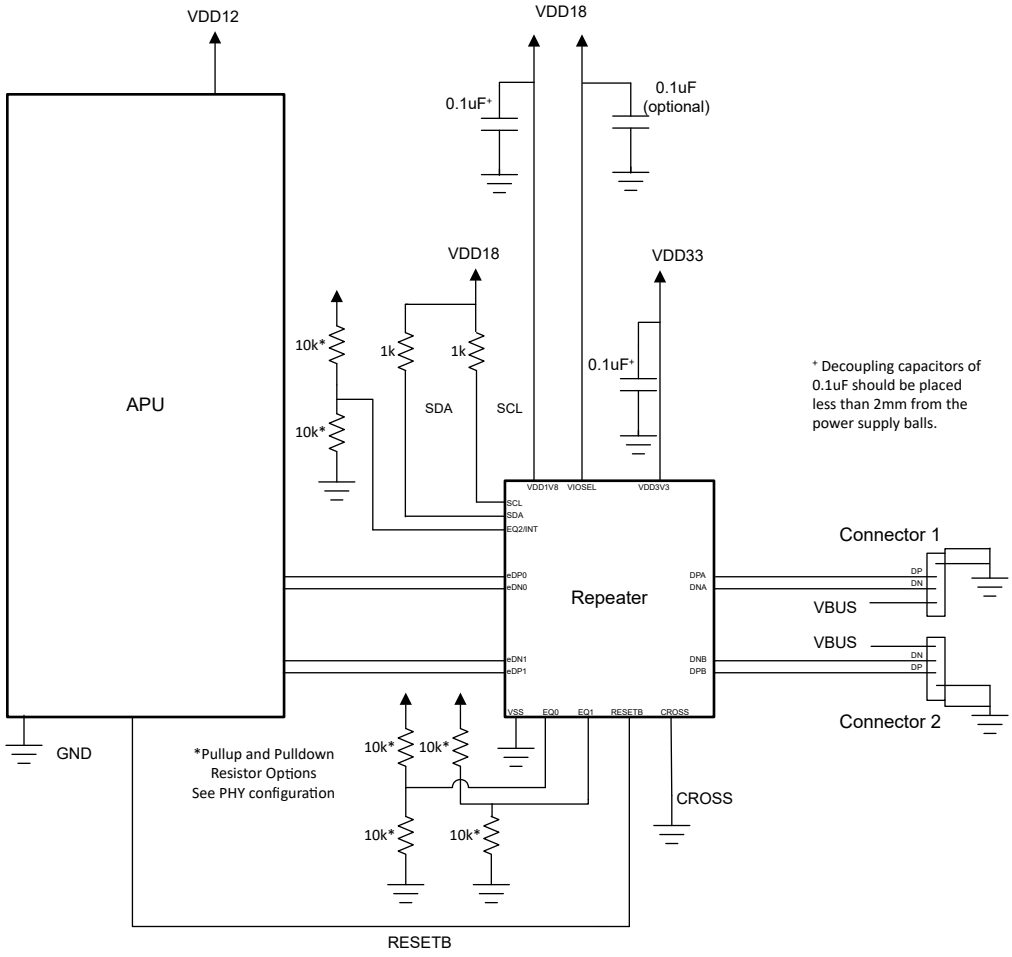


図 10-1. Typical Dual Port System Implementation with 1.8V and I²C

10.2.1 Design Requirements

The TUSB2E221 supports the eUSB2 specification. eUSB2 SoC must be compliant to the eUSB2 specification.

10.2.2 Detailed Design Procedure

The TUSB2E221 has multiple loss compensation settings for high-speed operation so make sure the selected settings match the system loss profile to optimize jitter performance. USB 2.0 high speed eye diagram measurements can be used as a guide to confirm the loss compensation is optimum for a given system.

10.2.2.1 eUSB PHY Settings Recommendation

表 10-1 shows the recommended eUSB PHY register settings for different eUSB lengths.

表 10-1. Recommended eUSB PHY Settings based on FR4 length

eUSB PHY Register	2.5 inches	5 inches	7.5 inches	10 inches
E_EQ_Px	0	2	4	6
E_HS_TX_AMPLITUDE_Px	3	4	5	6
E_HS_PRE_EMPHASIS_Px	0	2	3	4

10.2.3 Application Curve

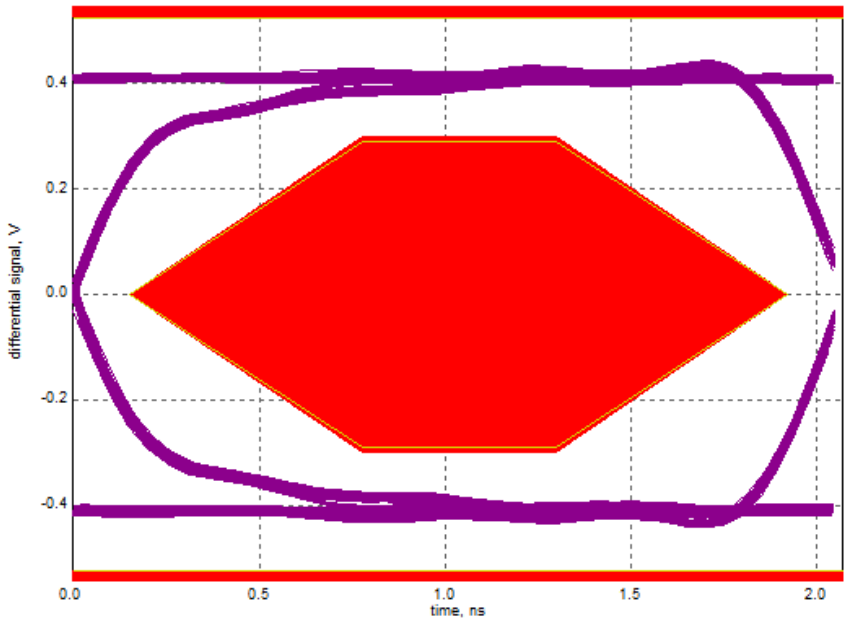


図 10-2. Typical USB 2.0 High-Speed Eye Diagram

10.3 Power Supply Recommendations

10.3.1 Power-Up Reset

The RESETB pin is an active-low reset pin that can also be used as a power-down pin.

The TUSB2E221 does not have power supply sequence requirements between VDD3V3 and VDD1V8.

Make sure the maximum VDD3V3 and VDD1V8 ramp time to reach minimum supply voltages is 2ms.

An internal power-on reset circuit along with the external RESETB input pin allows for proper initialization when RESETB is deasserted high prior to the power rails being valid. If RESETB deasserts high before the power supplies are stable, the internal power-on reset circuit can hold off internal reset until the supplies are stable.

After the RESETB deassertion, followed by internally generated reset signal and 1ms delay, CROSS pin is sampled and latched.

After the RESETB deassertion and after t_{RH_READY}, the TUSB2E221 is enabled and enters default state, ready to accept eUSB2 packets. Each repeater is either in host repeater mode or device repeater mode depending on the receipt of either host mode enable or peripheral mode enable.

10.4 Layout

10.4.1 Layout Guidelines

1. Place supply bypass capacitors as close to VDD1V8 and VDD3V3 pins as possible and avoid placing the bypass caps near the eDP/eDN and DP/DN traces.
2. Route the high-speed USB signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around the via to minimize the capacitance. Each via introduces discontinuities in the transmission line of the signal and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.
3. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.
4. Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.
5. Avoid stubs on the high-speed USB signals due to signal reflections. If a stub is unavoidable, then the stub must be less than 200 mil
6. Route all high-speed USB signal traces over continuous GND planes, with no interruptions.
7. Avoid crossing over anti-etch, commonly found with plane splits.
8. Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in 図 10-3.

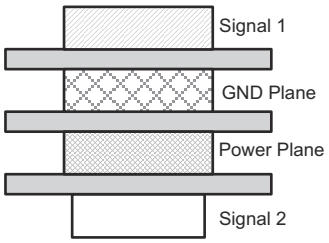


図 10-3. Four-Layer Board Stack-Up

10.4.2 Example Layout

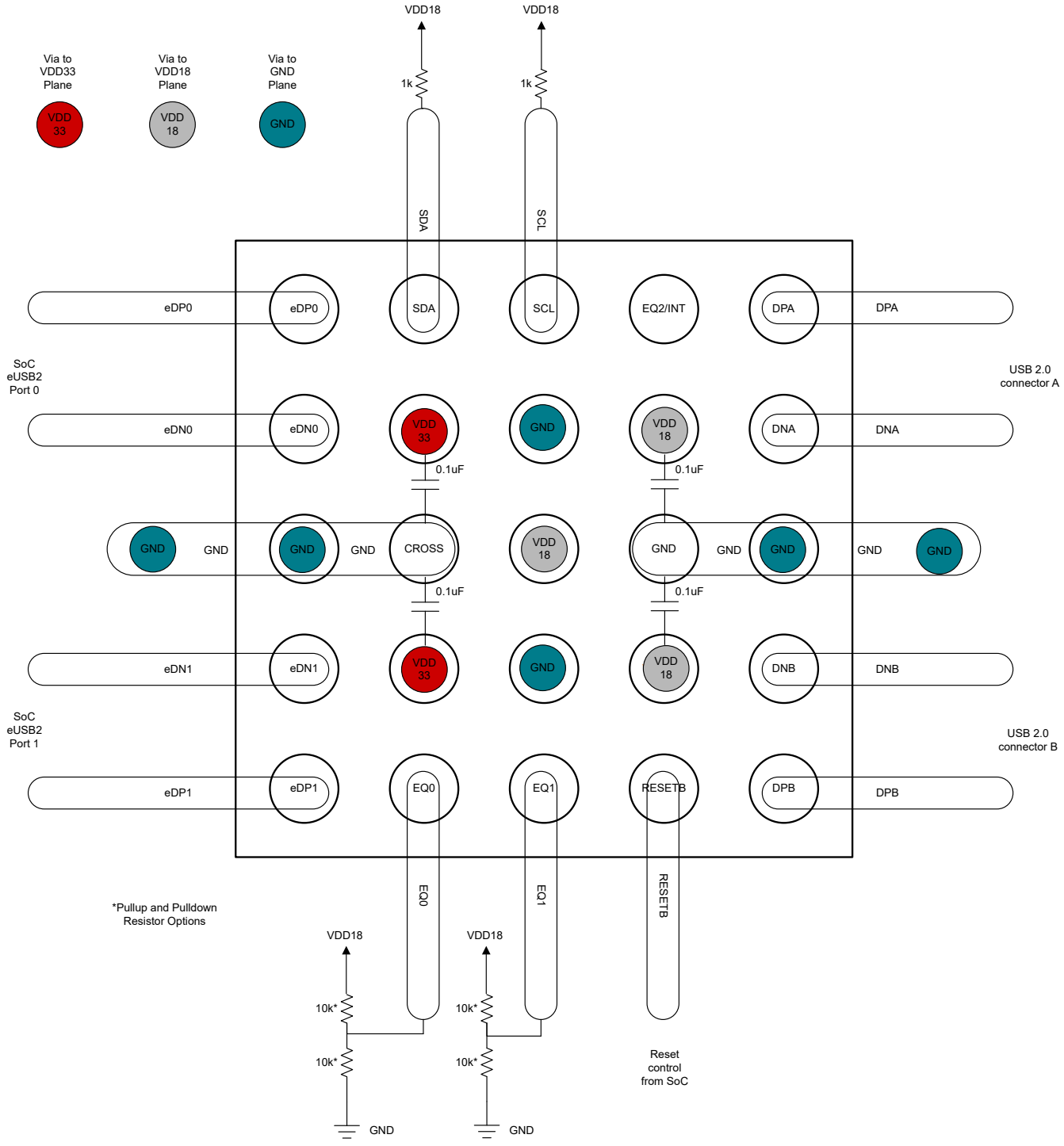


図 10-4. Example Layout for WCSP

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *USB 2.0 Board Design and Layout Guidelines*
- Texas Instruments, *High-Speed Layout Guidelines*
- Texas Instruments, *High-Speed Interface Layout Guidelines*

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Revision History

Changes from Revision A (October 2024) to Revision B (November 2024)	Page
• Added RAP address for writes	32

Changes from Revision * (June 2024) to Revision A (October 2024)	Page
• データシートのステータスを「事前情報」から「混流生産」	1
• YCG (DSBGA、25) パッケージのステータスを「プレビュー」から「アクティブ」に変更	1

13 Mechanical, Packaging, and Orderable Information

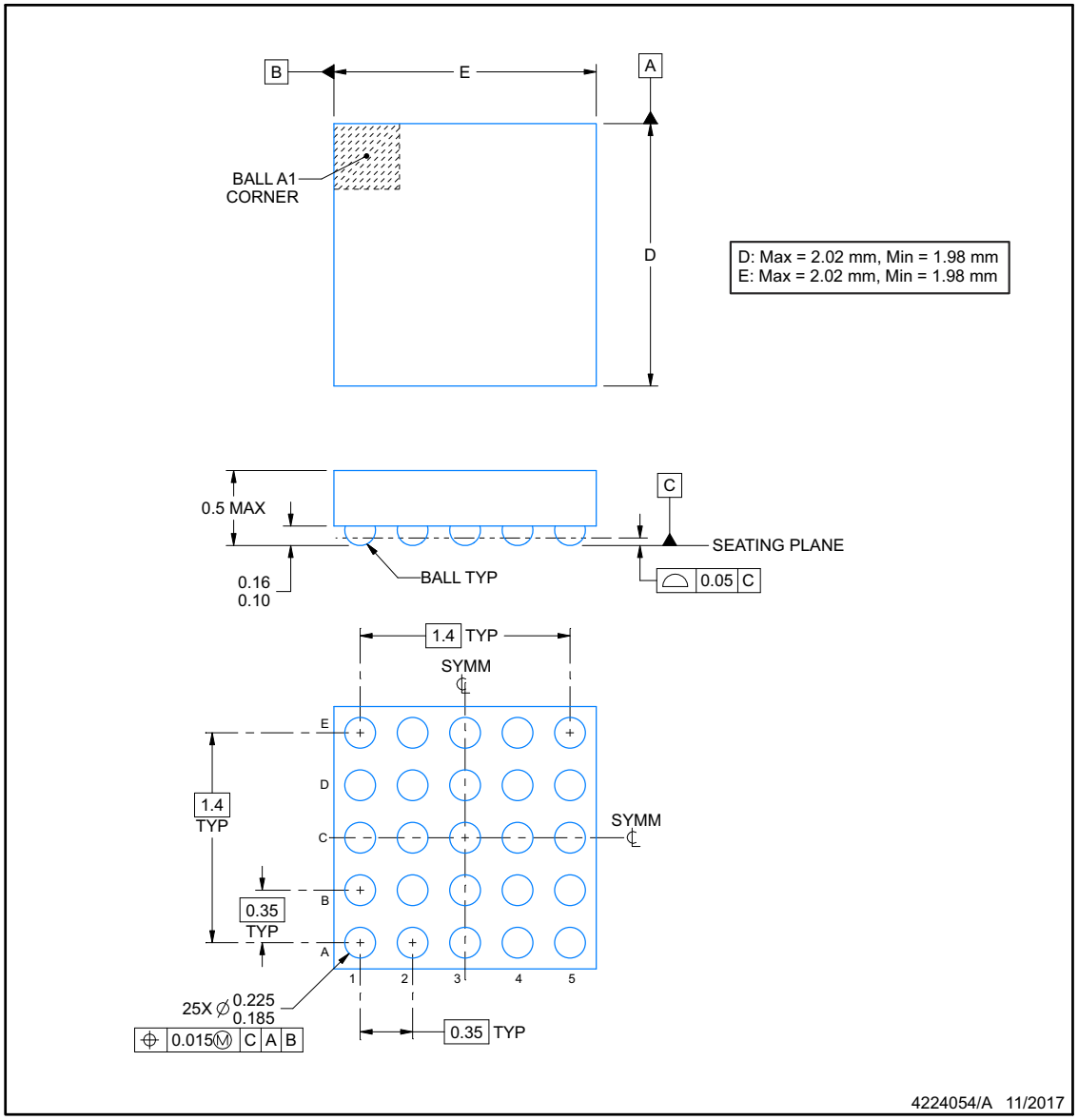
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

YCG0025

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

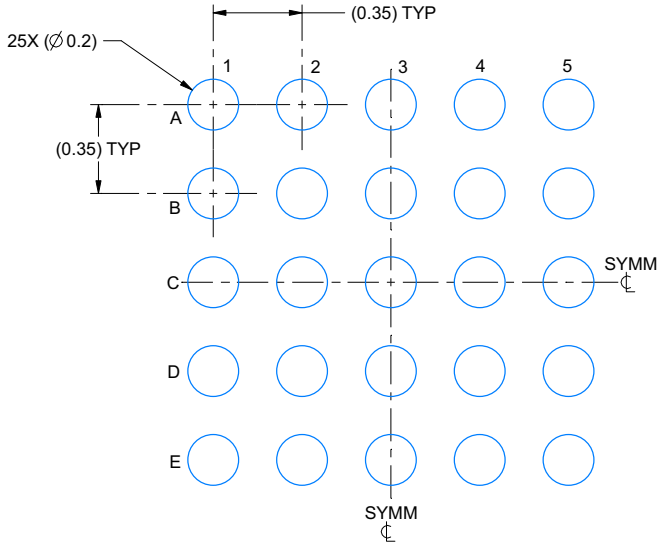
TEXAS INSTRUMENTS
www.ti.com

EXAMPLE BOARD LAYOUT

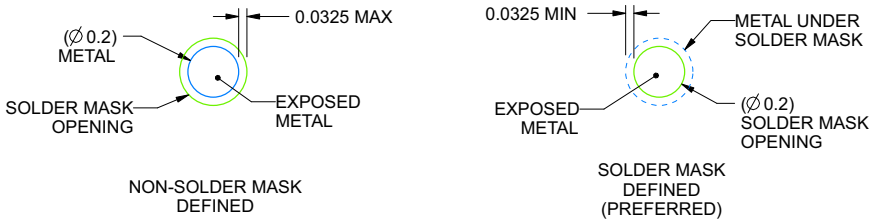
YCG0025

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS
NOT TO SCALE

4224054/A 11/2017

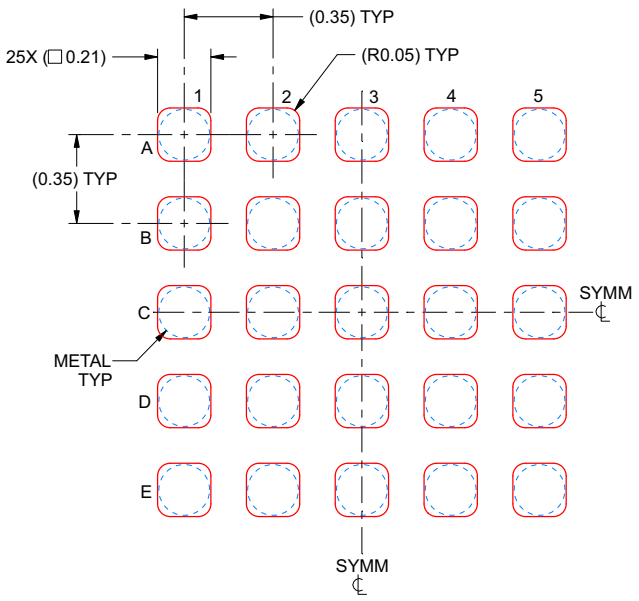
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YCG0025 **DSBGA - 0.5 mm max height**

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 40X

4224054/A 11/2017

NOTES: (continued)

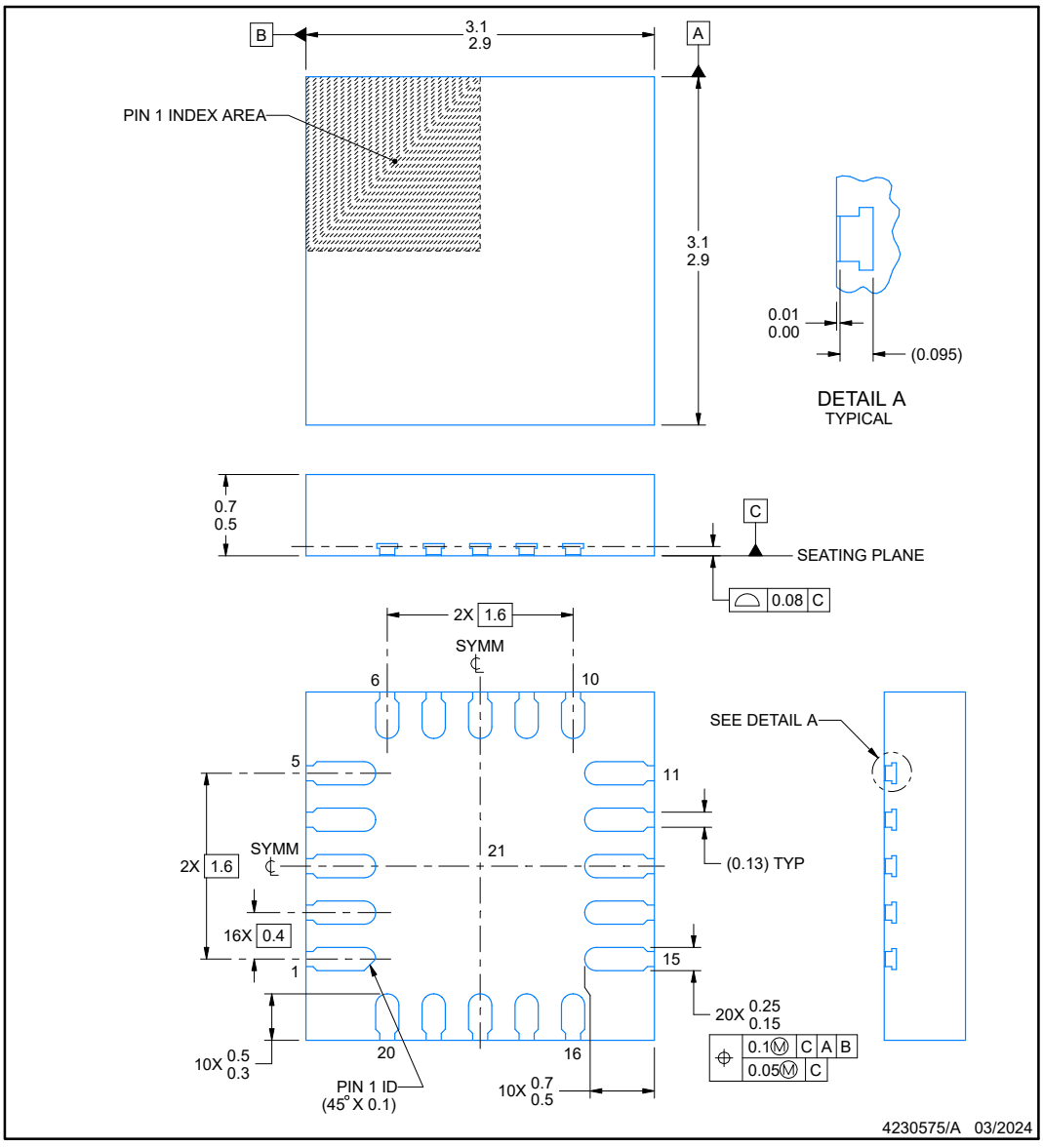
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

VBW0020A

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



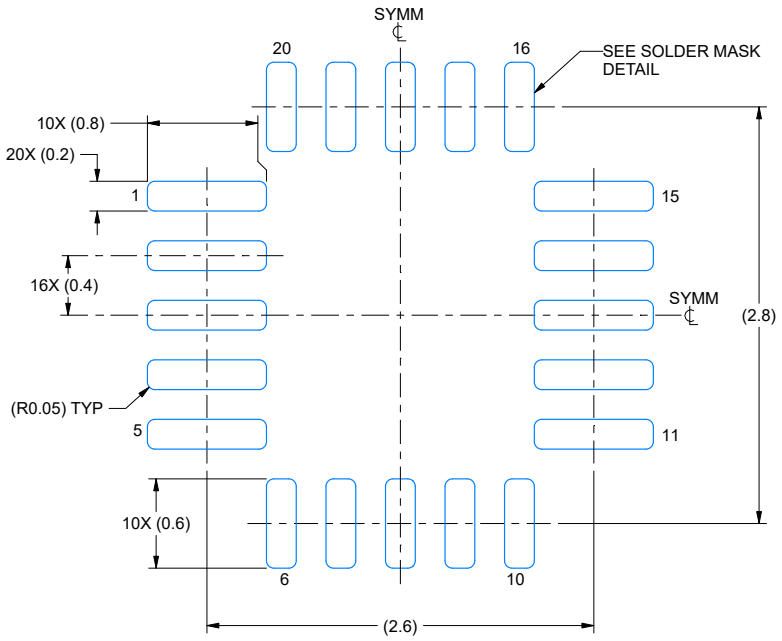
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

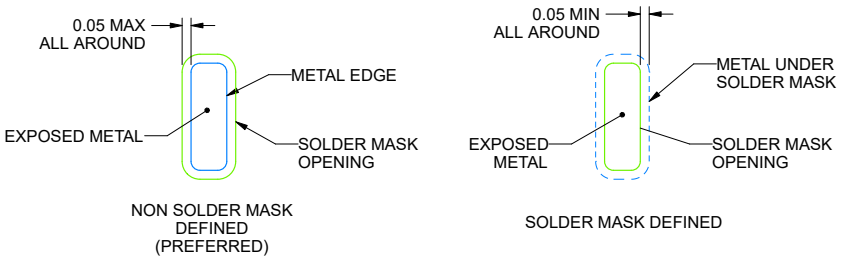
EXAMPLE BOARD LAYOUT

VBW0020A — **WQFN-FCRLF - 0.7 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



SOLDER MASK DETAILS

4230575/A 03/2024

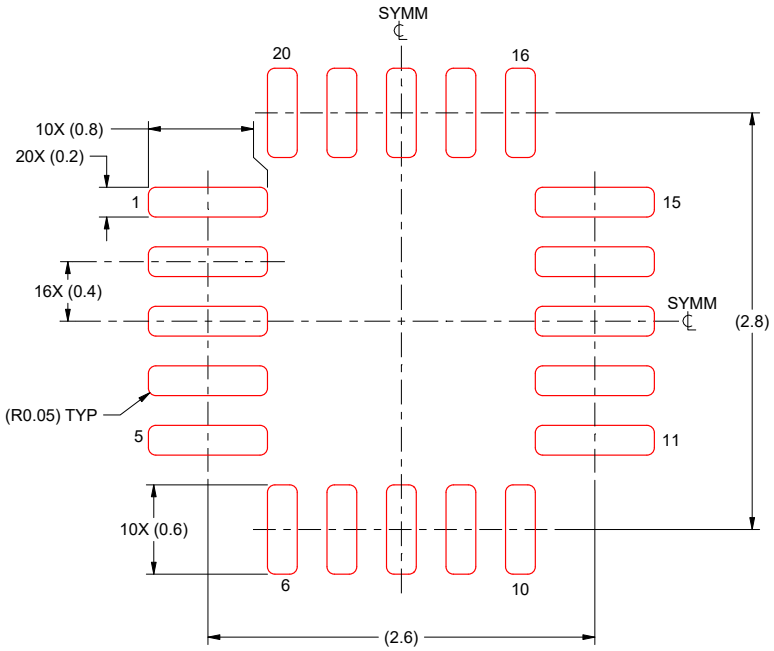
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

VBW0020A **WQFN-FCRLF - 0.7 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL
SCALE: 25X

4230575/A 03/2024

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTUSB2E2211001VBWR	ACTIVE	WQFN-FCRLF	VBW	20	3000	TBD	Call TI	Call TI	-40 to 85		Samples
TUSB2E2211001YCGR	ACTIVE	DSBGA	YCG	25	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	2E221W2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

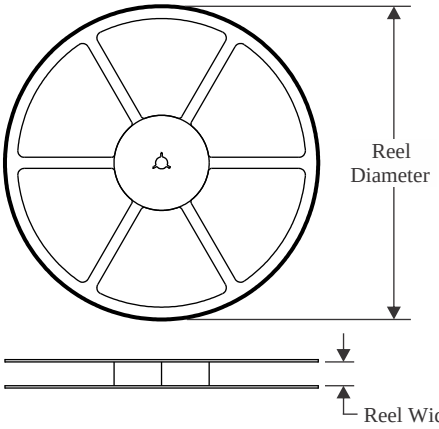
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

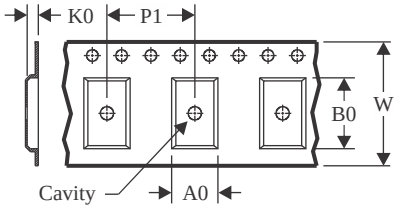
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

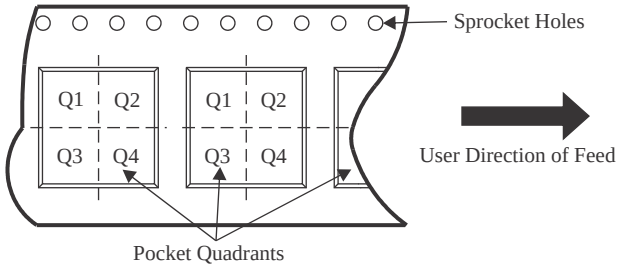


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

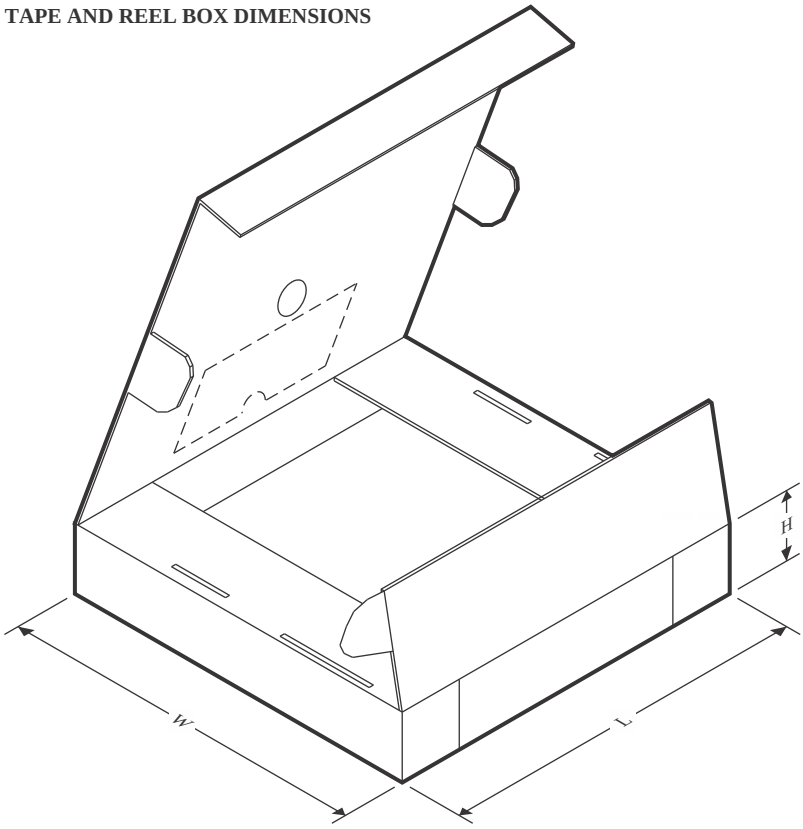
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB2E2211001YCGR	DSBGA	YCG	25	3000	180.0	8.4	2.14	2.14	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

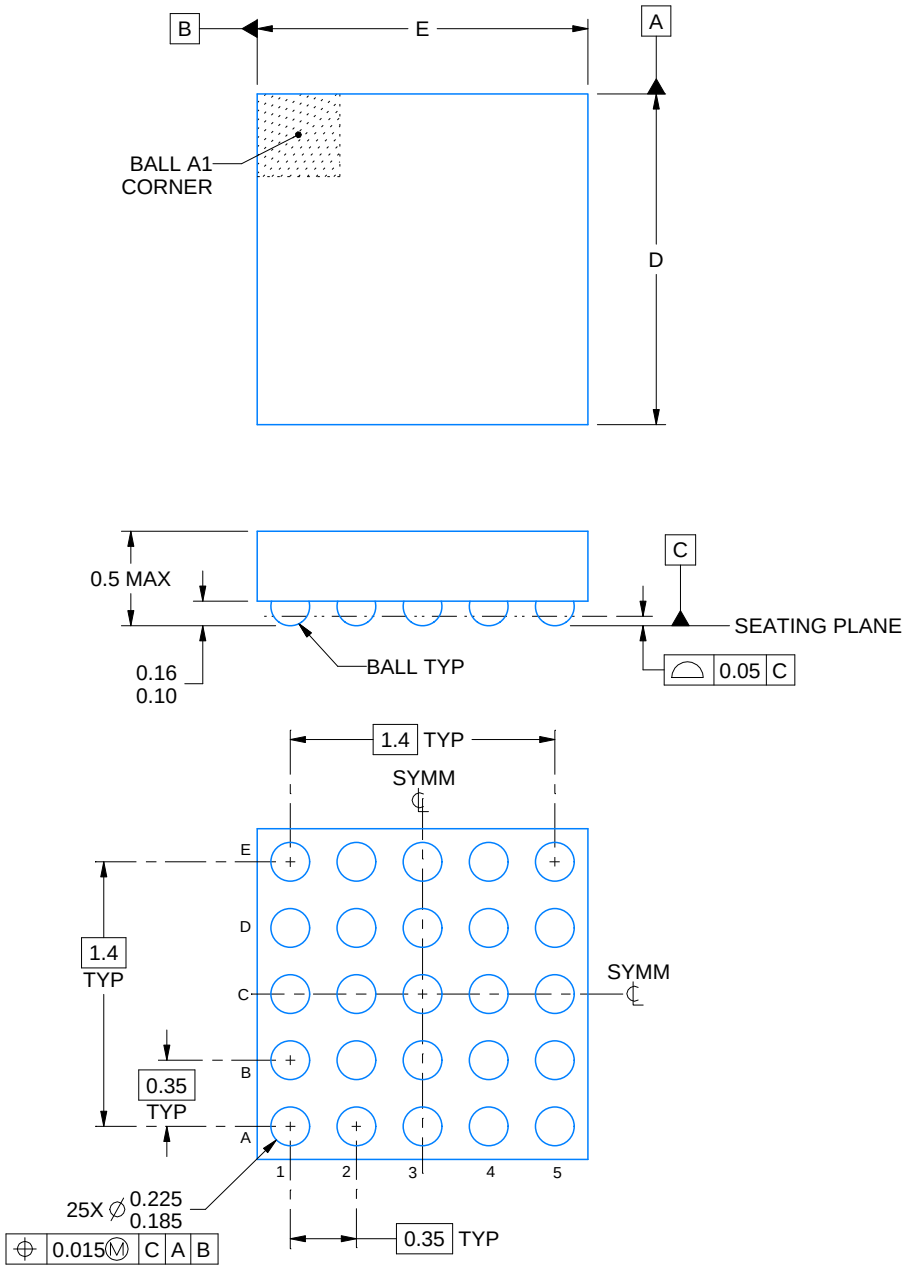
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB2E2211001YCGR	DSBGA	YCG	25	3000	182.0	182.0	20.0

YCG0025

PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4224054/A 11/2017

NOTES:

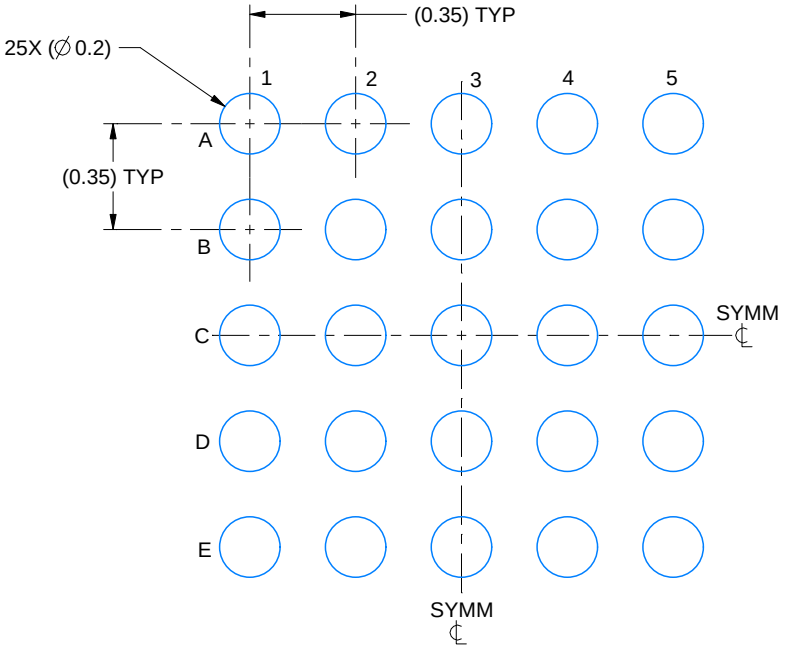
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

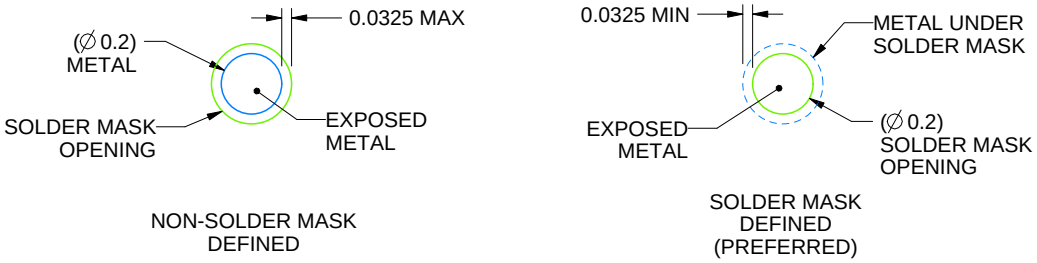
YCG0025

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS
NOT TO SCALE

4224054/A 11/2017

NOTES: (continued)

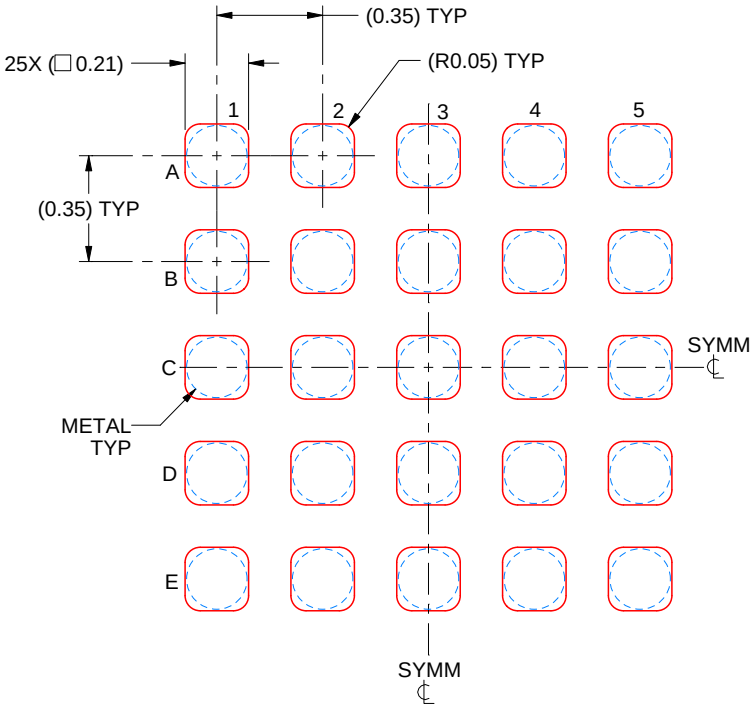
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YCG0025

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 40X

4224054/A 11/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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