

TVS0701 7V双方向フラット・クランプ・サージ保護デバイス

1 特長

- 産業用信号ライン向け1kV、42ΩのIEC 61000-4-5サージ・テストに耐える保護機能
- 双方向極性により、バイポーラ信号処理や誤配線に対して保護
- クランプ電圧：11V (サージ電流 30A、8/20μs 時)
- スタンドオフ電圧: ±7V
- 小型の 3mm×3mm SON フットプリント
- 125°C で 30A、8/20μs のサージ電流の反復ストライクを 5,000 回吸収
- 強力なサージ保護
 - IEC61000-4-5 (8/20μs): 30A
 - IEC61643-321 (10/1000μs): 15A
- 低リーク電流
 - 27°Cで0.25nA (標準値)
 - 85°Cで200nA (最大値)
- 低容量: 77pF
- レベル4 IEC 61000-4-2に準拠したESD保護機能を内蔵

2 アプリケーション

- 産業用センサ
- ソリッドステート・ドライブ
- 5V電源ライン
- 家電製品
- 医療用機器
- 電力網の保護および制御

3 概要

TVS0701デバイスは、最大30AのIEC 61000-4-5フォルト電流をシャントし、大電力の過渡事象や落雷からシステムを保護します。このデバイスは、一般的な産業用信号線のEMC要件である、42Ωのインピーダンスで結合した1kVのIEC 61000-4-5開路電圧に耐えます。TVS0701は帰還機構を使用して、フォルト中の正確なフラット・クランプを確保し、システムがさらされる電圧を、従来型のTVSダイオードよりも低く保ちます。厳格な電圧レギュレーションにより、設計者は許容電圧が低いシステム部品でも安心して選択でき、堅牢性を損なうことなくシステムのコストと複雑性を低減できます。TVS0701は±7Vの範囲で動作するため、逆配線に対する保護を必要とするシステムでも動作できます。

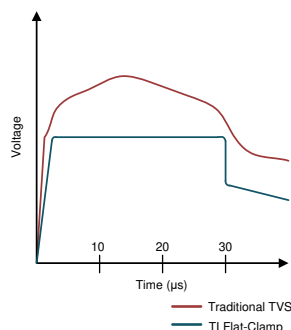
さらに、TVS0701はスペースの制約が厳しいアプリケーション用に設計された小型のSONフットプリントで供給されるため、標準のSMAおよびSMBパッケージと比較して大幅なサイズ低減が可能です。リーク電流と容量が低いことから、保護するラインへの影響も最小限に抑えられます。製品のライフサイクル全体にわたる堅牢な保護を確保するため、TIはTVS0701をテストし、125°Cで5000回の反復サージに対してデバイス性能に変化がないことを確認しています。

製品情報⁽¹⁾

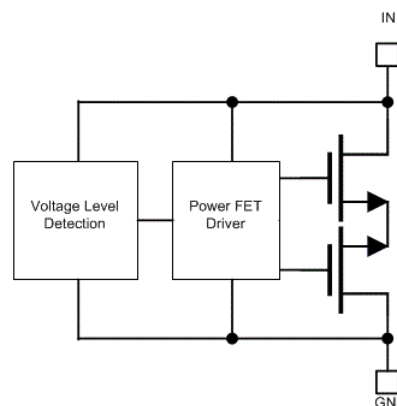
型番	パッケージ	本体サイズ(公称)
TVS0701	SON (8)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

8/20μsのサージに対する電圧クランプの応答



機能ブロック図



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4 改訂履歴

2018年9月発行のものから更新

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5 概要（続き）

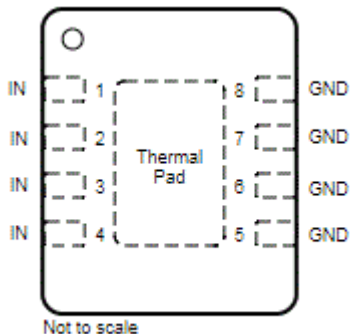
TVS0701はTIのフラット・クランプ・サージ・デバイス・ファミリの製品です。フラット・クランプ・ファミリの詳細については、『[効率的なシステム保護のためのフラット・クランプ・サージ保護技術](#)』ホワイト・ペーパーを参照してください。

6 デバイス比較表

デバイス	V_{rwm}	I_{pp} 時の V_{clamp}	I_{pp} (8/20 μ s)	V_{rwm} でのリーク電流	極性	パッケージ
TVS0500	5	9.2V	43A	0.07nA	単方向	DRV (SON-6)
TVS0701	7	11V	30A	0.25nA	双方向	DRB (SON-8)
TVS1400	14	18.6V	43A	2nA	単方向	DRV (SON-6)
TVS1401	14	20.5V	30A	1.1nA	双方向	DRB (SON-8)
TVS1800	18	22.8V	40A	0.3nA	単方向	DRV (SON-6)
TVS1801	18	27.4V	30A	0.4nA	双方向	DRB (SON-8)
TVS2200	22	27.7V	40A	3.2nA	単方向	DRV (SON-6)
TVS2201	22	29.6V	30A	2nA	双方向	DRB (SON-8)
TVS2700	27	32.5V	40A	1.7nA	単方向	DRV (SON-6)
TVS2701	27	34V	27A	0.8nA	双方向	DRB (SON-8)
TVS3300	33	38V	35A	19nA	単方向	DRV (SON-6)、YZF (WCSP)
TVS3301	33	40V	27A	2.5nA	双方向	DRB (SON-8)

7 Pin Configuration and Functions

**DRB Package
8-Pin SON
Top View**



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	DRB		
IN	1, 2, 3, 4	IN	Surge Protected Channel
GND	5, 6, 7, 8	GND	Ground
FLOAT	Exposed Thermal Pad	NC	Exposed Thermal Pad Must Be Floating

8 Specifications

8.1 Absolute Maximum Ratings

 $T_A = 27^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Maximum Surge	IEC 61000-4-5 Current (8/20 μs), $T_A < 125^\circ\text{C}$		± 30	A
	IEC 61000-4-5 Power (8/20 μs)		360	W
	IEC 61643-321 Current (10/1000 μs)		± 15	A
	IEC 61643-321 Power (10/1000 μs)		150	W
EFT	IEC 61000-4-4 EFT Protection		± 80	A
I_{BR}	DC Current		80	mA
T_A	Ambient Operating Temperature	-40	125	$^\circ\text{C}$
T_{stg}	Storage Temperature	-65	150	$^\circ\text{C}$

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings - JEDEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	± 2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	± 500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 ESD Ratings - IEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	± 8	kV
		IEC 61000-4-2 air-gap discharge	± 15	

8.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{RWM}	Reverse Stand-Off Voltage		± 7		V

8.5 Thermal Information

THERMAL METRIC ⁽¹⁾		TVS0701	UNIT
		DRB (SON)	
		8 PINS	
R_{qJA}	Junction-to-ambient thermal resistance	52.0	$^\circ\text{C}/\text{W}$
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	56.1	$^\circ\text{C}/\text{W}$
R_{qJB}	Junction-to-board thermal resistance	24.9	$^\circ\text{C}/\text{W}$
Y_{JT}	Junction-to-top characterization parameter	2.1	$^\circ\text{C}/\text{W}$
Y_{JB}	Junction-to-board characterization parameter	24.9	$^\circ\text{C}/\text{W}$
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	9.8	$^\circ\text{C}/\text{W}$

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

8.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{LEAK}	Leakage Current	Measured at V _{IN} = ±V _{RWM} , T _A = 27°C		0.25	40	nA
		Measured at V _{IN} = ±V _{RWM} , T _A = 85°C			200	
V _{BR}	Break-down Voltage	I _{IN} = ±1mA	9.3	10		V
V _{CLAMP}	Clamp Voltage	±I _{PP} IEC 61000-4-5 Surge (8/20 μs), V _{IN} = 0 V before surge, T _A = 27°C		11	11.7	V
		±I _{PP} IEC 61000-4-5 Surge (8/20 μs), V _{IN} = ±V _{RWM} before surge, T _A = 125°C			12.9	
R _{DYN}	8/20 μs surge dynamic resistance	Calculated from V _{CLAMP} at .5*I _{PP} and I _{PP} surge current, T _A = 25°C		120		mΩ
C _{IN}	Input pin capacitance	V _{IN} = V _{RWM} , f = 1 MHz, 30 mV _{pp} , IO to GND		77		pF
SR	Maximum Slew Rate	0-±V _{RWM} rising edge, sweep rise time and measure slew rate when I _{PEAK} = 1 mA, T _A = 27°C		2.5		V/μs
		0-±V _{RWM} rising edge, sweep rise time and measure slew rate when I _{PEAK} = 1 mA, T _A = 85°C		1.0		

8.7 Typical Characteristics

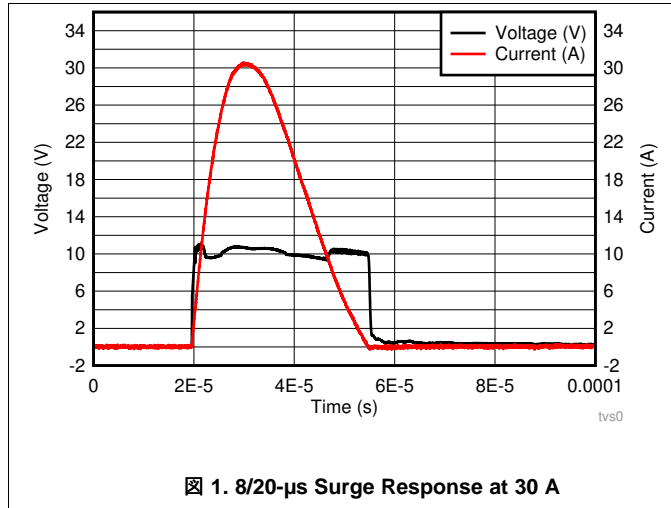


Fig 1. 8/20-µs Surge Response at 30 A

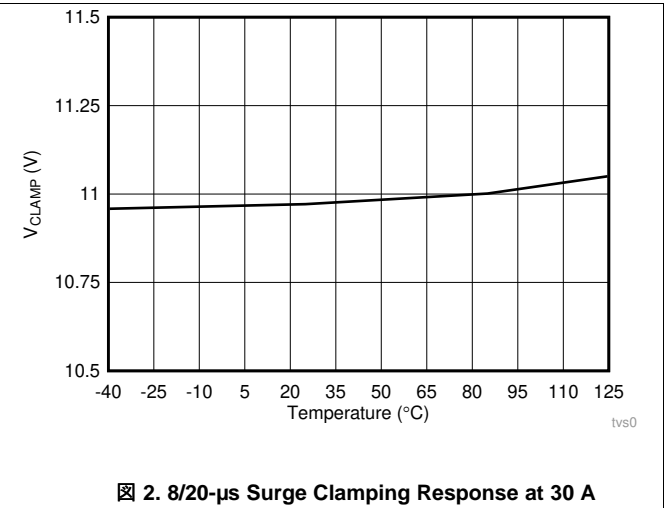
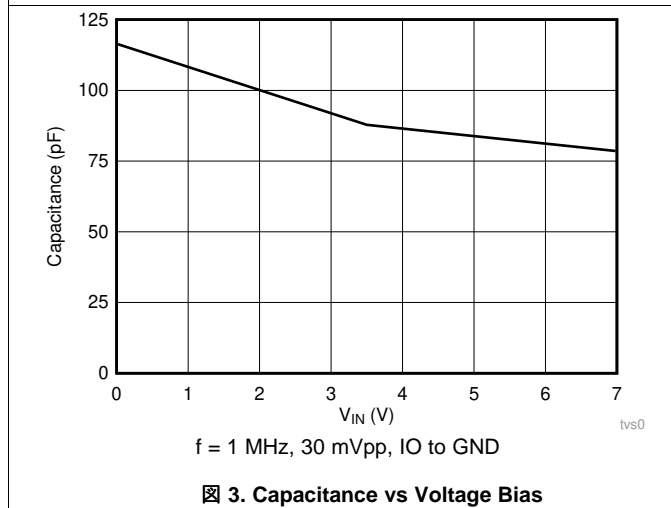


Fig 2. 8/20-µs Surge Clamping Response at 30 A



f = 1 MHz, 30 mVpp, IO to GND

Fig 3. Capacitance vs Voltage Bias

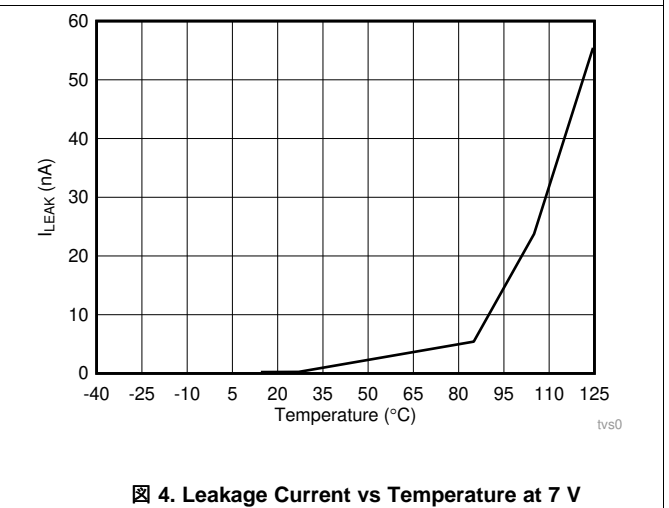


Fig 4. Leakage Current vs Temperature at 7 V

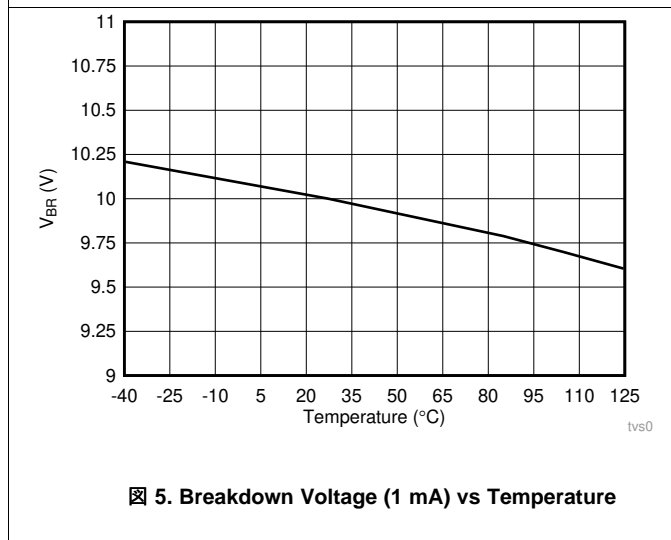


Fig 5. Breakdown Voltage (1 mA) vs Temperature

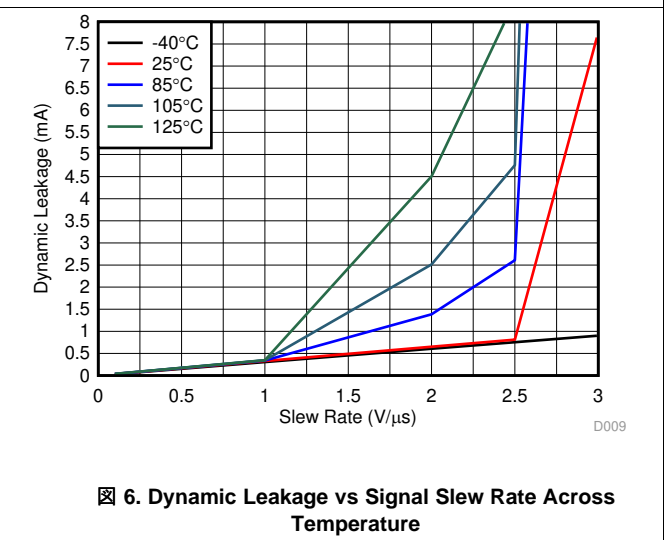


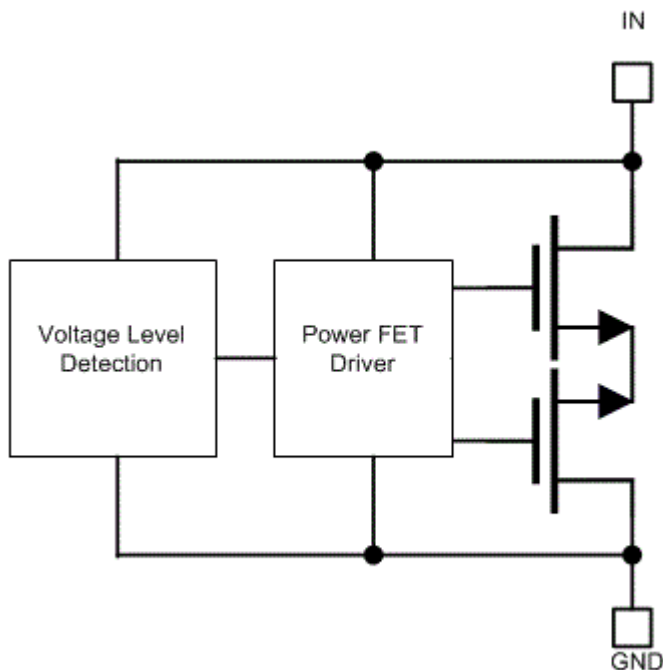
Fig 6. Dynamic Leakage vs Signal Slew Rate Across Temperature

9 Detailed Description

9.1 Overview

The TVS0701 is a bidirectional precision clamp with two integrated FETs driven by a feedback loop to tightly regulate the input voltage during an overvoltage event. This feedback loop leads to a very low dynamic resistance, giving a flat clamping voltage during transient overvoltage events like a surge.

9.2 Functional Block Diagram



9.3 Feature Description

The TVS0701 is a precision clamp that handles 30 A of IEC 61000-4-5 8/20- μ s surge pulse. The flat clamping feature helps keep the clamping voltage very low to keep the downstream circuits from being stressed. The flat clamping feature can also help end-equipment designers save cost by opening up the possibility to use lower-cost, lower voltage tolerant downstream ICs. This device provides a bidirectional operating range, with a symmetrical V_{RWM} of ± 7 V designed for applications that have bipolar input signals or that must withstand reverse wiring conditions. The TVS0701 has minimal leakage at V_{RWM} designed for applications where low leakage and power dissipation is a necessity. Built-in IEC 61000-4-2 and IEC 61000-4-4 ratings make it a robust protection solution for ESD and EFT events, and the TVS0701 wide ambient temperature range of -40°C to $+125^{\circ}\text{C}$ enables usage in harsh industrial environments.

9.4 Device Functional Modes

9.4.1 Protection Specifications

The TVS0701 is specified according to both the IEC 61000-4-5 and IEC 61643-321 standards. This enables usage in systems regardless of which standard is required by relevant product standards or best matches measured fault conditions. The IEC 61000-4-5 standard requires protection against a pulse with a rise time of 8 μ s and a half-length of 20 μ s, while the IEC 61643-321 standard requires protection against a much longer pulse with a rise time of 10 μ s and a half-length of 1000 μ s.

Device Functional Modes (continued)

The positive and negative surges are imposed to the TVS0701 by a combination wave generator (CWG) with a 2- Ω coupling resistor at different peak voltage levels. For powered-on transient tests that need power supply bias, inductances are used to decouple the transient stress and protect the power supply. The TVS0701 is post-tested by assuring that there is no shift in device breakdown or leakage at V_{RWM} .

In addition, the TVS0701 has been tested according to IEC 61000-4-5 to pass a ± 1 -kV surge test through a 42- Ω coupling resistor and a 0.5- μ F capacitor. This test is a common test requirement for industrial signal I/O lines and the TVS0701 precision clamp can be used in applications that have that requirement.

The TVS0701 integrates IEC 61000-4-2 level 4 ESD Protection and 80 A of IEC 61000-4-4 EFT Protection. These combine to ensure that the device can protect against most common transient test requirements.

For more information on TI's test methods for Surge, ESD, and EFT testing, refer to the [IEC61000-4-2](#), [IEC 61000-4-4](#) and [IEC 61000-4-5 Tests for TI's Protection Devices](#) application report.

9.4.2 Reliability Testing

To ensure device reliability, the TVS0701 is characterized against 5000 repetitive pulses of 25-A IEC 61000-4-5 8/20- μ s surge pulses at 125°C. The test is performed with less than 10 seconds between each pulse at high temperature to simulate worst-case scenarios for fault regulation. After each surge pulse, the TVS0701 clamping voltage, breakdown voltage, and leakage are recorded to ensure that there is no variation or performance degradation. By ensuring robust, reliable, high temperature protection, the TVS0701 enables fault protection in applications that must withstand years of continuous operation with no performance change.

9.4.3 Zero Derating

Unlike traditional diodes, the TVS0701 has zero derating of maximum power dissipation and ensures robust performance up to 125°C. Traditional TVS diodes lose up to 50% of their current carrying capability when at high temperatures, so a surge pulse above 85°C ambient can cause failures that are not seen at room temperature. The TVS0701 prevents this so the designer can see the surge protection regardless of temperature. Because of this, Flat-Clamp devices can provide robust protection against surge pulses that occur at high ambient temperatures, as shown in TI's [TVS Surge Protection in High-Temperature Environments](#) application report.

9.4.4 Bidirectional Operation

The TVS0701 is a bidirectional TVS with a symmetrical operating region. This allows for operation with positive and negative voltages, rather than just positive voltages like the unidirectional TVS0700. This allows for single chip protection for applications where the signal is expected to operate below 0 V or where there is a need to withstand a large common-mode voltage. In addition, there is a system requirement to be able to withstand reverse wiring conditions in many cases where a high voltage signal is accidentally applied to the system ground and a ground is accidentally applied to the input terminal. This causes a large reverse voltage on the TVS diode that the device must be able to withstand. The TVS0701 is designed to not break down or see failures under reverse wiring conditions for applications that must withstand these miswiring issues.

注

If the applied signal is not expected to go below 0 V, a unidirectional device will clamp much lower in the reverse direction and should be used. In this case, the recommended device would be the TVS0500.

9.4.5 Transient Performance

During large transient swings, the TVS0701 will begin clamping the input signal to protect downstream conditions. While this prevents damage during fault conditions, it can cause leakage when the intended input signal has a fast slew rate. To keep power dissipation low and remove the chance of signal distortion, TI recommends that the designer keep the slew rate of any input signal on the TVS0701 below 2.5 V/ μ s at room temperature and below 1 V/ μ s at 85°C shown in [Figure 6](#). Faster slew rates will cause the device to clamp the input signal and draw current through the device for a few microseconds, increasing the rise time of the signal. This will not cause any harm to the system or to the device, however, it can cause device overheating if the fast input voltage swings occur regularly.

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TVS0701 can be used to protect any power, analog, or digital signal from transient fault conditions caused by the environment or other electrical components.

10.2 Typical Application

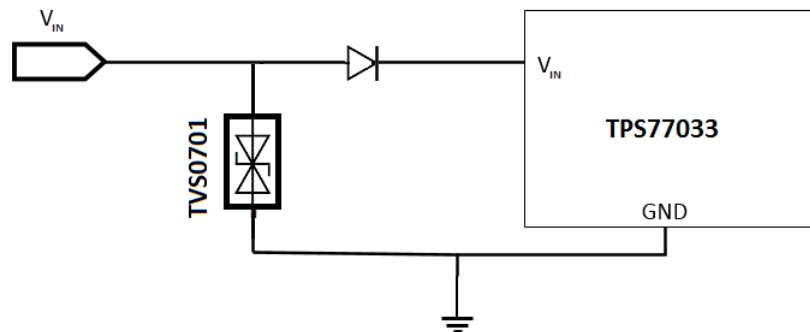


图 7. TVS0701 Application Schematic

10.2.1 Design Requirements

A typical operation for the TVS0701 would be protecting a nominal 5-V input to an LDO similar to 图 7. In this example, the TVS0701 is protecting the input to a TPS77033, a standard LDO with an input voltage range of 2.7 V to 10 V and an absolute maximum voltage of 13.5 V. The input must be protected against transient voltage surges that can be produced by an unstable supply, and the input must also be protected against reverse voltage condition that can be caused by miswiring. Without any input protection, this input voltage will rise to hundreds of volts for multiple microseconds and violate the absolute maximum input voltage and harm the device if a surge event is caused by lightning, coupling, ringing, or any other fault condition. TI's Flat-Clamp technology provides surge protection diodes that can maximize the useable voltage range and clamp at a safe level for the system.

10.2.2 Detailed Design Procedure

If the TVS0701 is in place to protect the device, the voltage will rise to the breakdown of the diode at 10 V during a surge event. The TVS0701 will then turn on to shunt the surge current to ground. With the low dynamic resistance of the TVS0701, large amounts of surge current will have minimal impact on the clamping voltage. The Specifications section guarantees absolute maximum clamping of 12.9 V during surge pulses, so there is no risk of the input to the TPS77033 about the absolute maximum of 13.5 V. This is well within the absolute maximum input voltage to ensure robust protection of the circuit.


In addition, the TVS0701 provides protection against reverse voltage application that could accidentally be caused by shorts between pins. If -7 V is applied to the V_{IN} pin, the TPS77033 will not be harmed because the series diode will prevent the voltage from being applied to the input, and the TVS0701 will not shunt current because the reverse working voltage is -7 V. If the TVS0500 or a unidirectional device is used in this case, a -7 -V short would cause the device to shunt current until it fails.

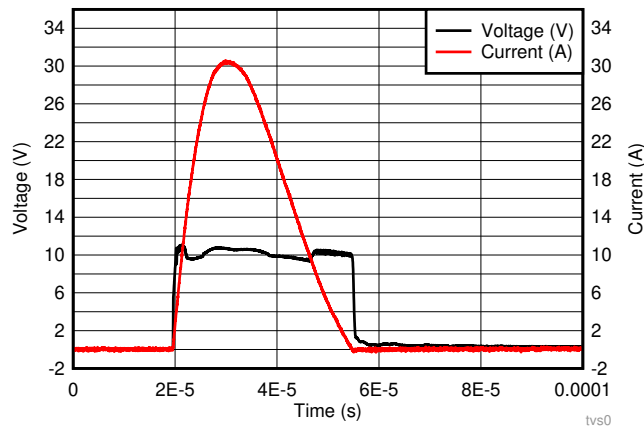
Typical Application (continued)

The small size of the device also improves fault protection by lowering the effect of fault current coupling onto neighboring traces. The small form factor of the TVS0701 allows the device to be placed extremely close to the input connector, which lowers the length of the path fault current going through the system compared to larger protection solutions.

Finally, the low leakage of the TVS0701 will have low input power losses. At 7 V, the device will see typical 0.25-nA leakage for a constant power dissipation of less than 1 nW, a negligible quantity that will not effect overall efficiency metrics or add heating concerns.

10.3 Application Curves

When a surge is applied to a system with the TVS0701, the device will clamp the overvoltage as shown in  8.



 8. Surge Clamping Response (30 A)

11 Power Supply Recommendations

The TVS0701 is a clamping device so there is no need to power it. To ensure the device functions properly, do not violate the recommended V_{IN} voltage range (-7 V to 7 V) .

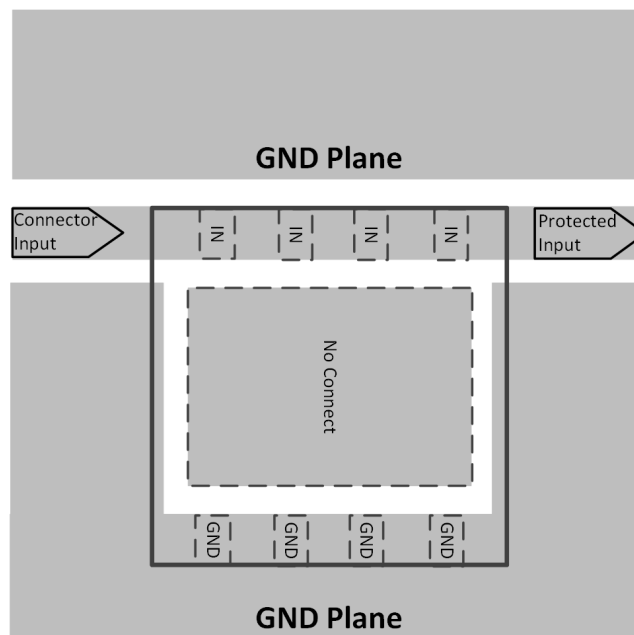
12 Layout

12.1 Layout Guidelines

The optimum placement is close to the connector. EMI during an ESD event can couple from the tested trace to other nearby unprotected traces, which could result in system failures. The PCB designer must minimize the possibility of EMI coupling by keeping all unprotected traces away from protected traces between the TVS and the connector. Route the protected traces straight. Use rounded corners with the largest radii possible to eliminate any sharp corners on the protected traces between the TVS0701 and the connector. Electric fields tend to build up on corners, which could increase EMI coupling.

Ensure that the thermal pad on the layout is floating rather than grounded. Grounding the thermal pad will impede the operating range of the TVS0701 and can cause failures when the applied voltage is negative. A floating thermal pad allows the maximum operating range without sacrificing any transient performance.

12.2 Layout Example



9. TVS0701 Layout

13 デバイスおよびドキュメントのサポート

13.1 ドキュメントのサポート

- 『効率的なシステム保護のためのフラット・クランプ・サージ保護技術』
- 『TI の保護デバイスに対する IEC61000-4-2、IEC 61000-4-4、および IEC 61000-4-5 テスト』
- 『高温環境での TVS サージ保護』

13.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

13.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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13.4 商標

E2E is a trademark of Texas Instruments.

13.5 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TVS0701DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1QCP	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TVS0701DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TVS0701DRBR	SON	DRB	8	3000	338.0	355.0	50.0

DRB 8

GENERIC PACKAGE VIEW

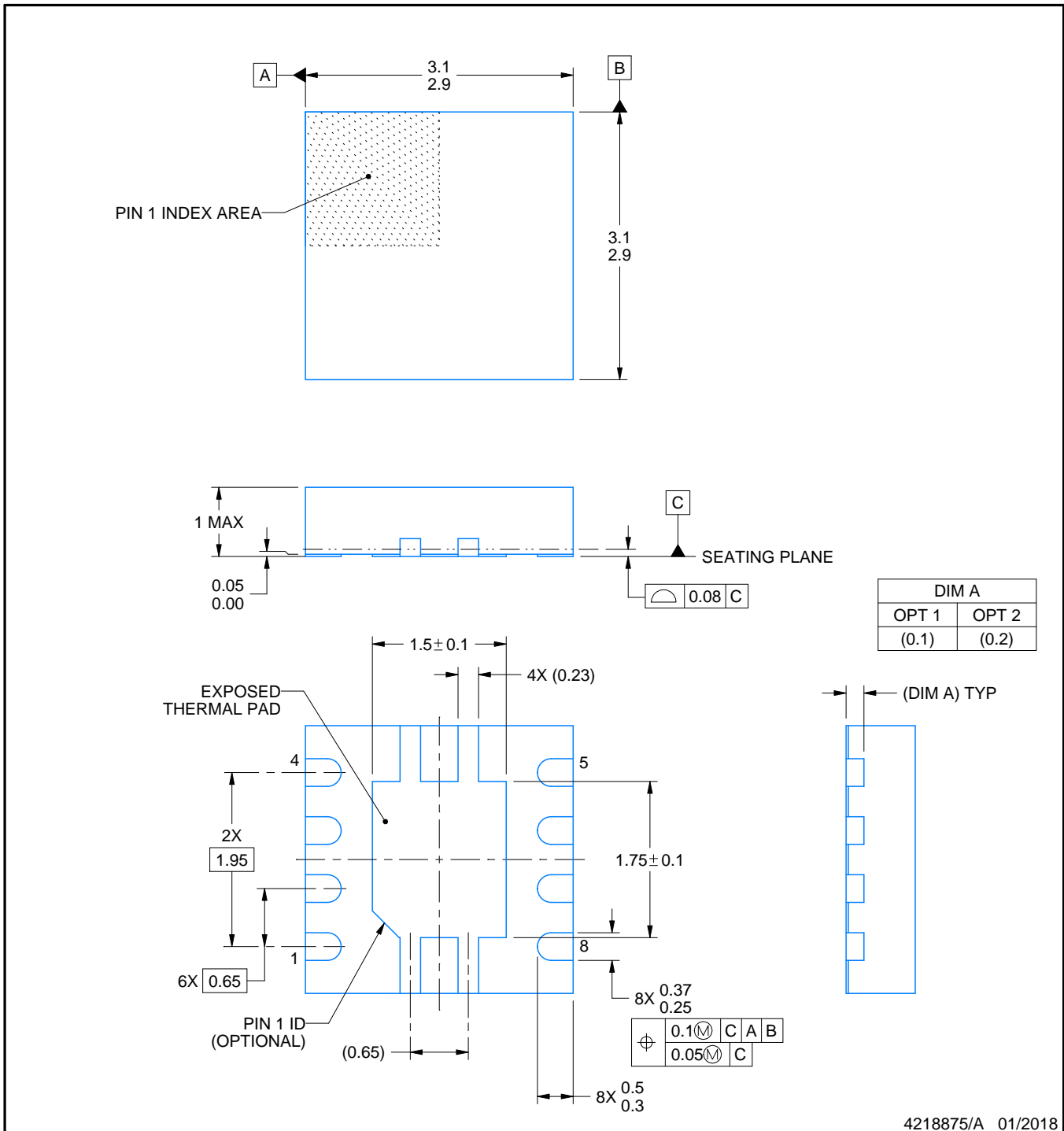
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L



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NOTES:

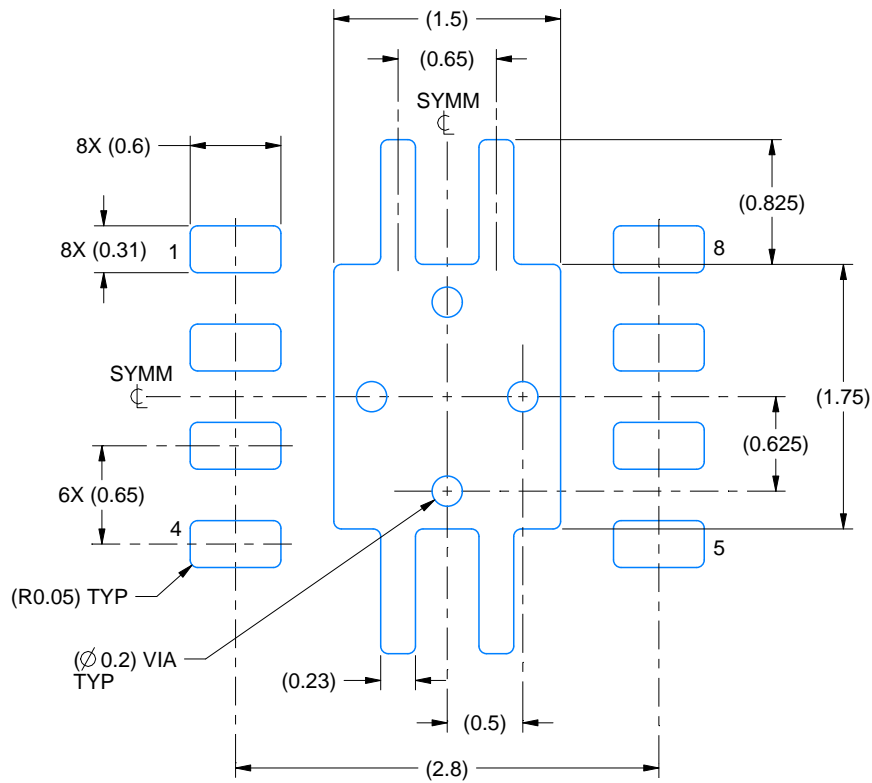
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

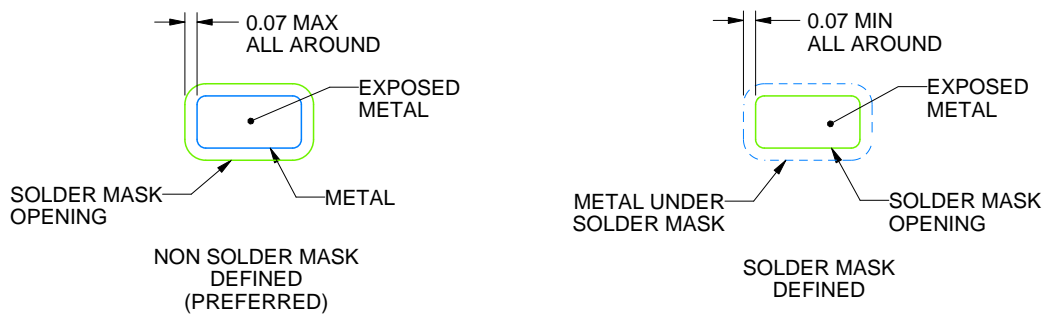
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

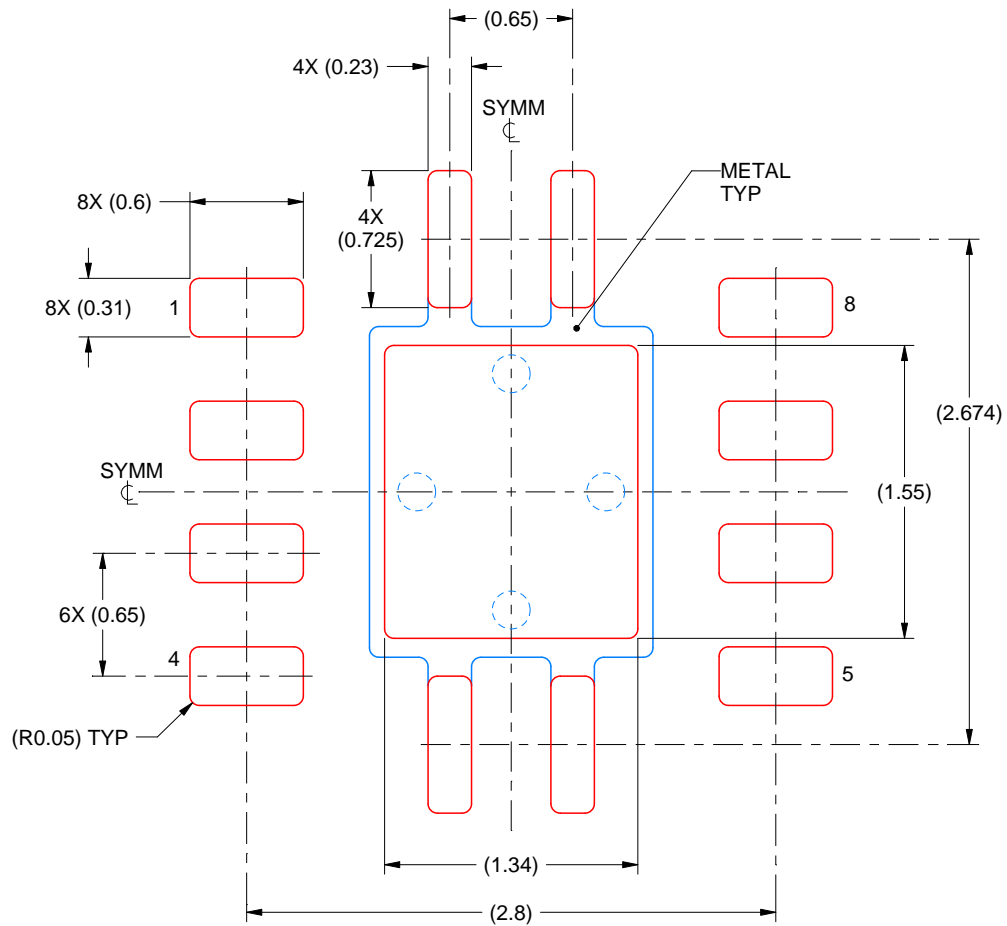
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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